CS224 – 3

LAB 6 – PRELEMINARY REPORT

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1)

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits1	Byte Offset Size in bits2	Block Replacement Policy Needed (Yes/No)
1	128	1	32	4	2^{13}	**15**	**13**	**2**	**2**	**No**
2	128	4	32	16	2^{9}	**17**	**9**	**4**	**2**	**Yes**
3	128	Full	32	16	2^{0}	**26**	**0**	**4**	**2**	**Yes**
4	256	2	64	8	2^{11}	**15**	**11**	**3**	**3**	**Yes**
5	256	4	64	32	2^{8}	**16**	**8**	**5**	**3**	**Yes**
6	256	Full	16	16	2^{0}	**27**	**0**	**4**	**1**	**Yes**

2)

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 20 24	**00**	**No**
00 00 20 42	**00**	**No**
00 00 20 68	**01**	**No**
00 00 20 04	**00**	**No**
00 00 20 0C	**01**	**No**
00 00 20 4C	**01**	**No**

3)

Memory Address Accessed (hex)	Set No.	Hit (yes/no)
00 00 00 2C	**01**	**No**
00 00 00 48	**01**	**No**
00 00 00 44	**00**	**No**
00 00 00 0C	**01**	**No**
00 00 00 04	**00**	**No**
00 00 00 0C	**01**	**Yes**

4)

a) Structure consist a **Tag**, **Index Set**, **Word Block Offset** and **Byte offset**

block size = 32 x 2 = 64 byte = 2^6 byte

number of set = Cache memory data area size / (N x (block size)) = $2^{10}/(2^3 x\ 2^6) = 2$

index set = 1 bit

word block offset = 5 bit

byte offset = 1 bit

tag = 32 – (1 + 5 + 1) = 25 bit

structure:

←Tag→←index set→←word block offset→←byte offset→

b)

structure:

←V→← D →←Age→← Tag →←Data→

D = 1 bit

V = 1 bit

Tag = 25 bit

Age for each block = $log_2 N$

Age = 3 bit

Data = 64 byte = 512 bit

Block Size = 1 + 1+ 25 + 3 + 512 = 542 bits

c)

Set Size = N x Block Size = 2^3 x 542 = 4336 bits

SRAM = (Set Size x (no of sets)) = (4336)x2 = 8672 bits

d) SRAM consist Age bits too. And they are used for LRU replacement. If we use random replacement, we do not have to use a data like Age bits. In this way, we probably have slower cache but SRAM will be smaller. For each block 3 Age bits were used which corresponds to 24 bits for each set. So, total of 48 Age bits were used in this example. Consequently, if we use random replacement SRAM will be smaller for 48 bits.