


WORK PACKAGE WP3 - SIMULATION

LEADER: LABORATOIRE MÉTHODES FORMELLES - LMF

 Participants: LMF, i3S, IRIT

 TAPAS-ANR meeting - Nice, 7-8 Janvier 2026

OUTLINE

- Task 3.1. Hierarchical clock theory
- Task 3.2. Hierarchical clock connector

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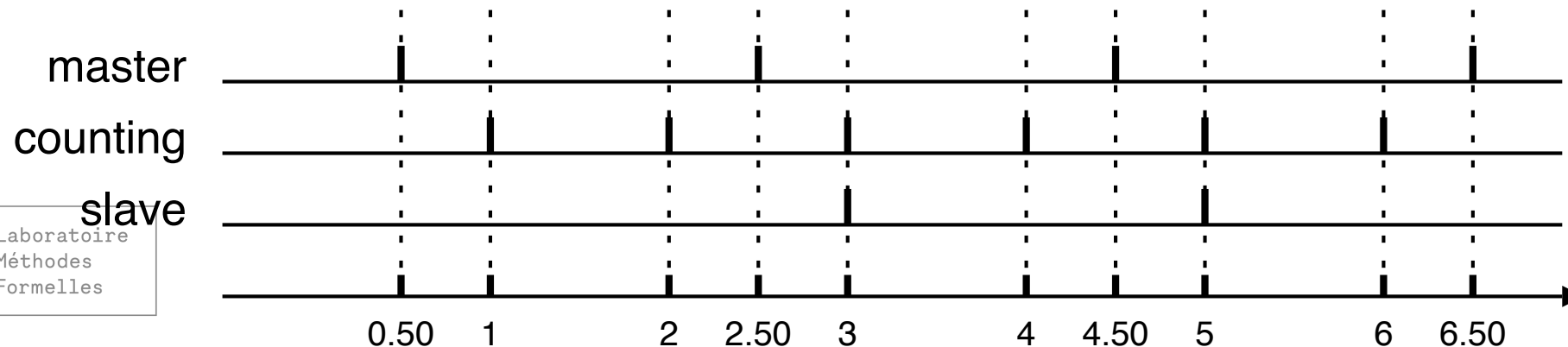
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HIERARCHICAL CLOCK THEORY

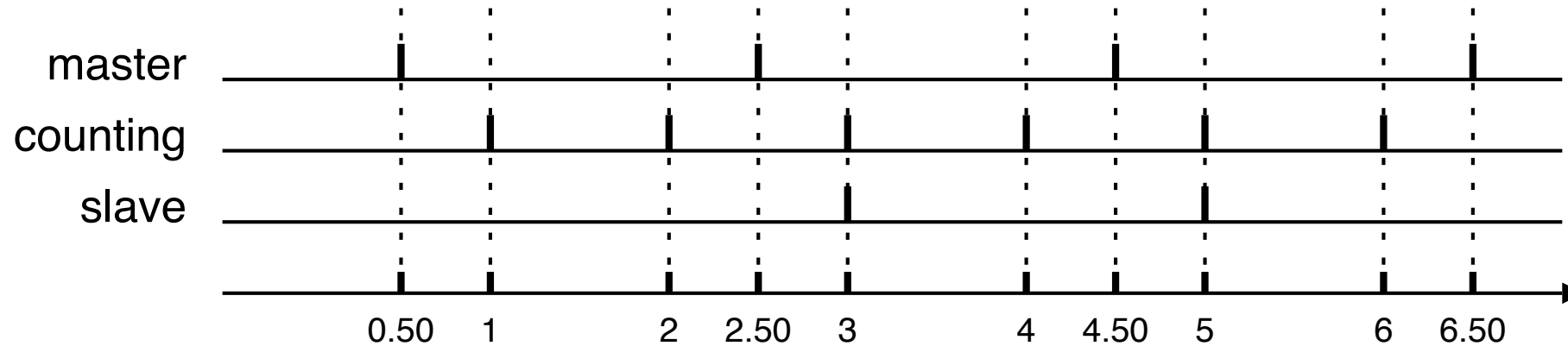
- **TESL time model**
 - time is represented through **clocks**, where each clock models the occurrence of events.

```
1 decimal-clock master periodic 2 offset 0.5
2 decimal-clock counting periodic 1 offset 1
3 tag relation master = counting
4
5 unit-clock slave
6
7 master delayed by 3 on counting implies slave
8
9 @maxstep 10
10 @tagref counting
```



HIERARCHICAL CLOCK THEORY

- **TESL time model**
 - time is represented through **clocks**, where each clock models the occurrence of events.



- Developing an **Event-B theory** to embed the **TESL language** into Event-B models
 - developing a formal model of the **semantics of TESL operators**.
 - **Event-B event executions** are defined as **ticks of the corresponding clocks**.

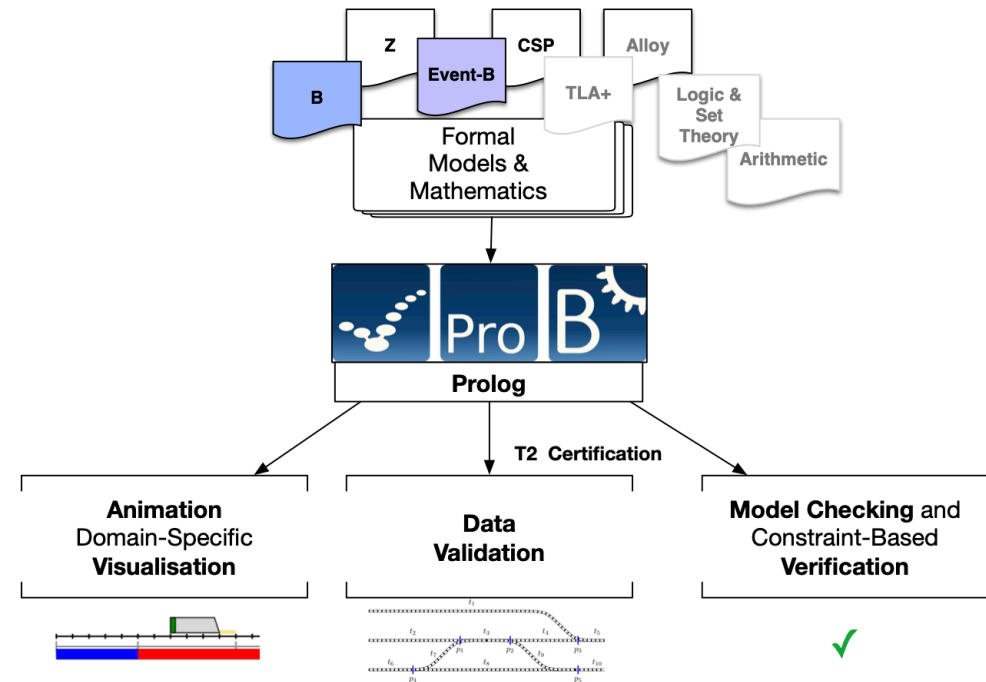
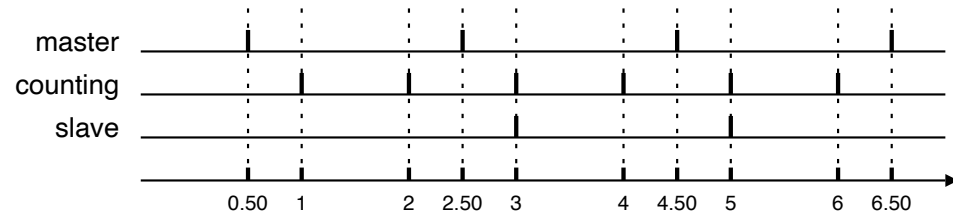
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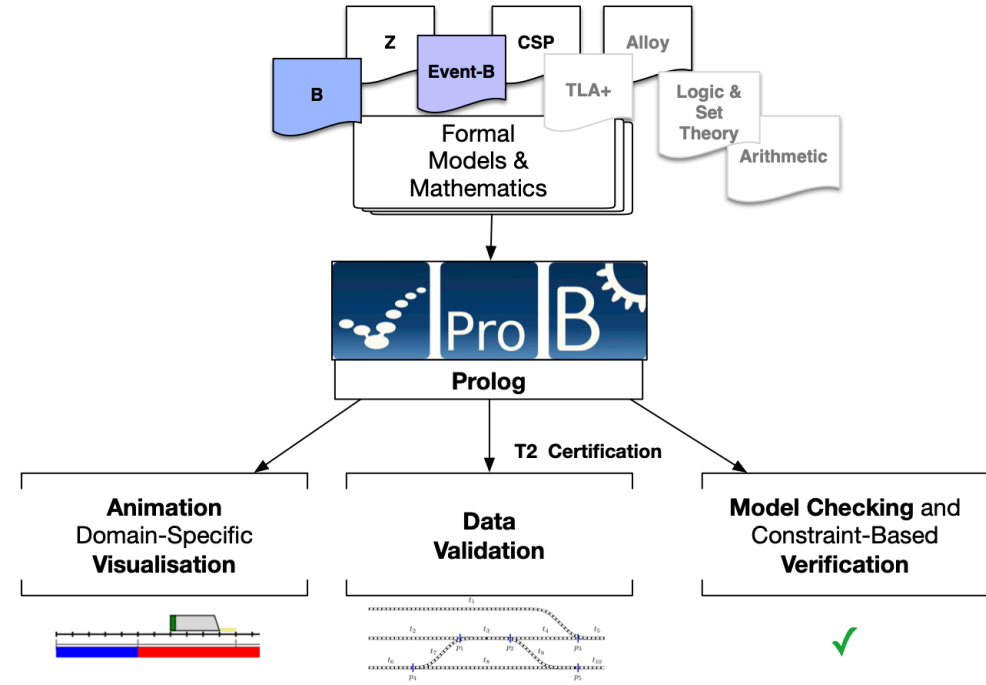
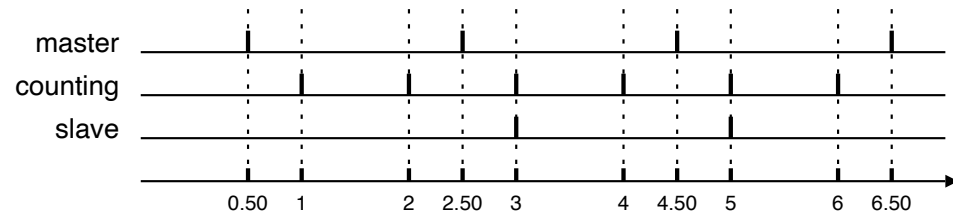
HIERARCHICAL CLOCK CONNECTOR

- **ProB** is an animator, constraint solver and model checker for the Event-B-Method.



- Integrating the **TESL solver** with the **ProB animator and model checker**

HIERARCHICAL CLOCK CONNECTOR



- The **TESL solver** generates **traces** to drive **Event-B model** animation
- Executing TESL traces → **Time-guided validation** of Event-B models using a **formal clock-based time model**