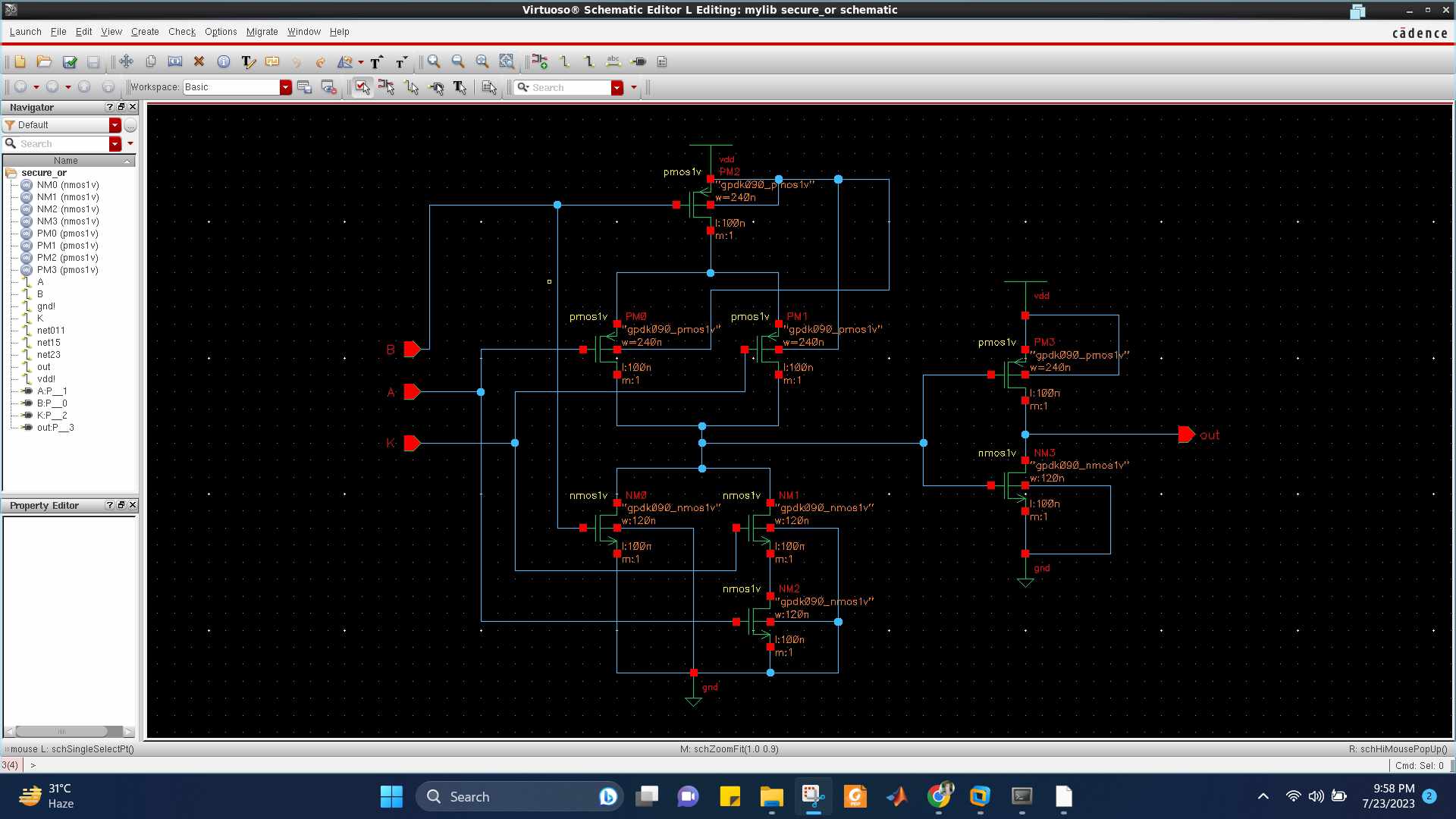
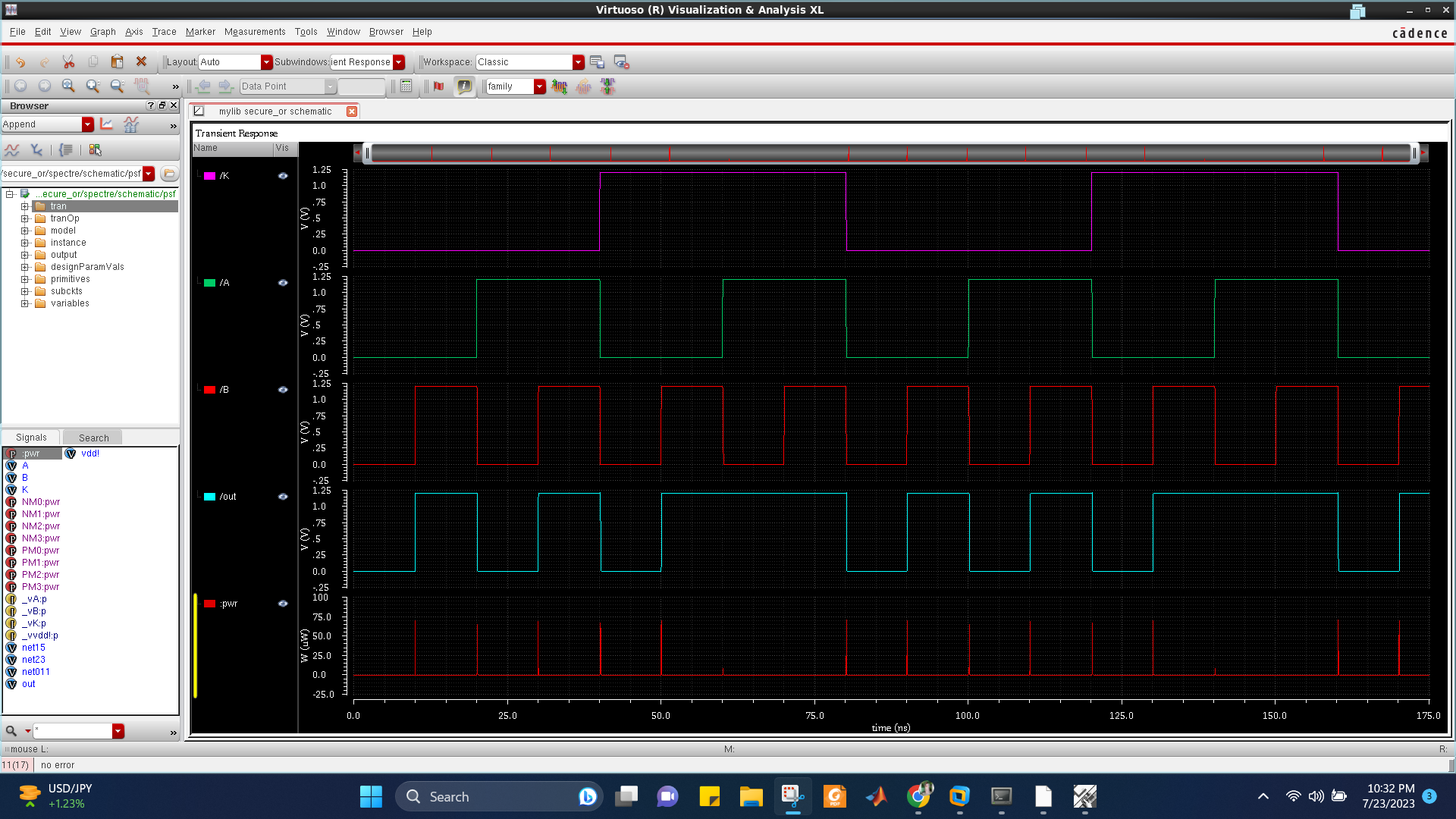
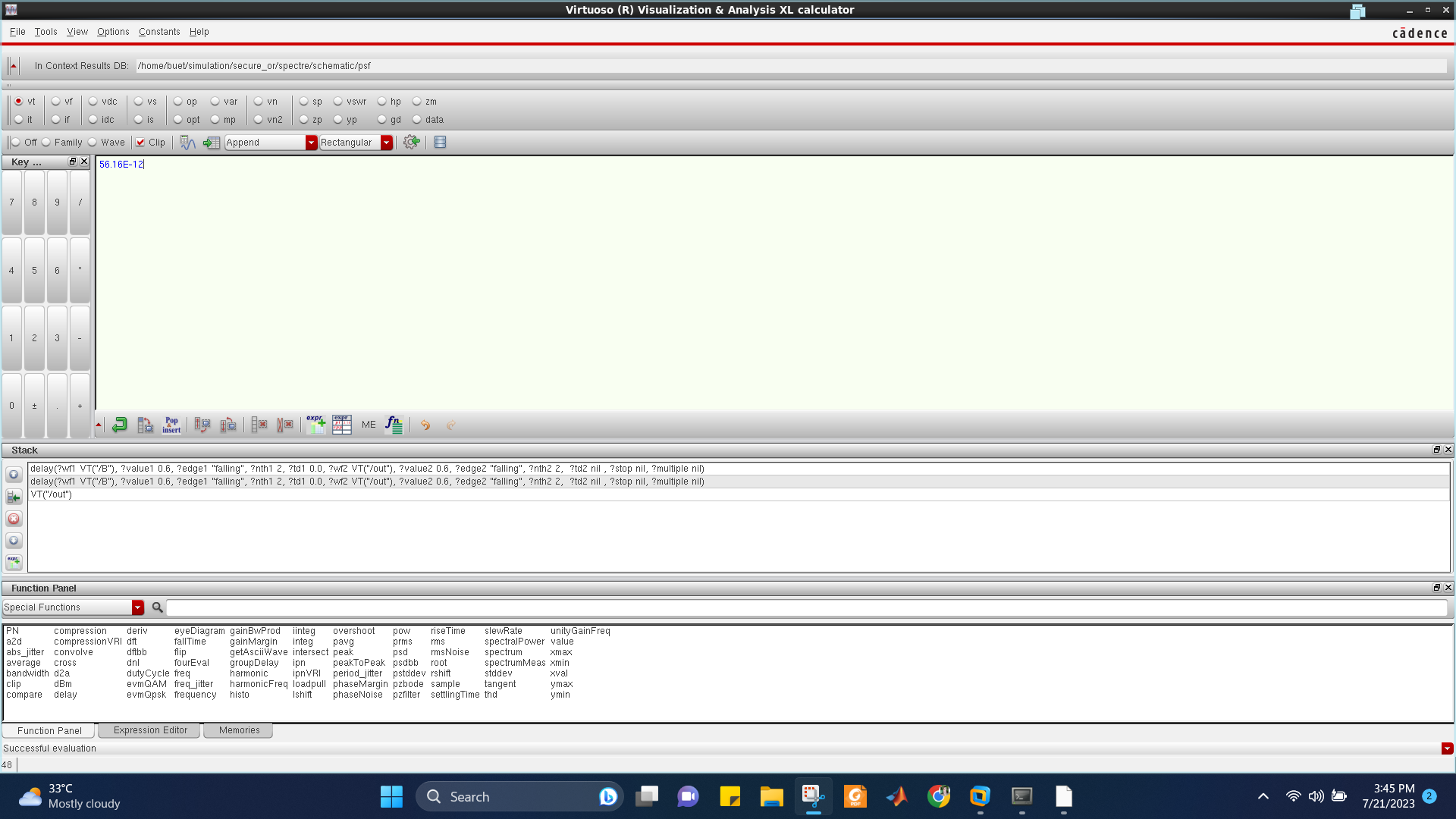
**Secure OR Schematic**

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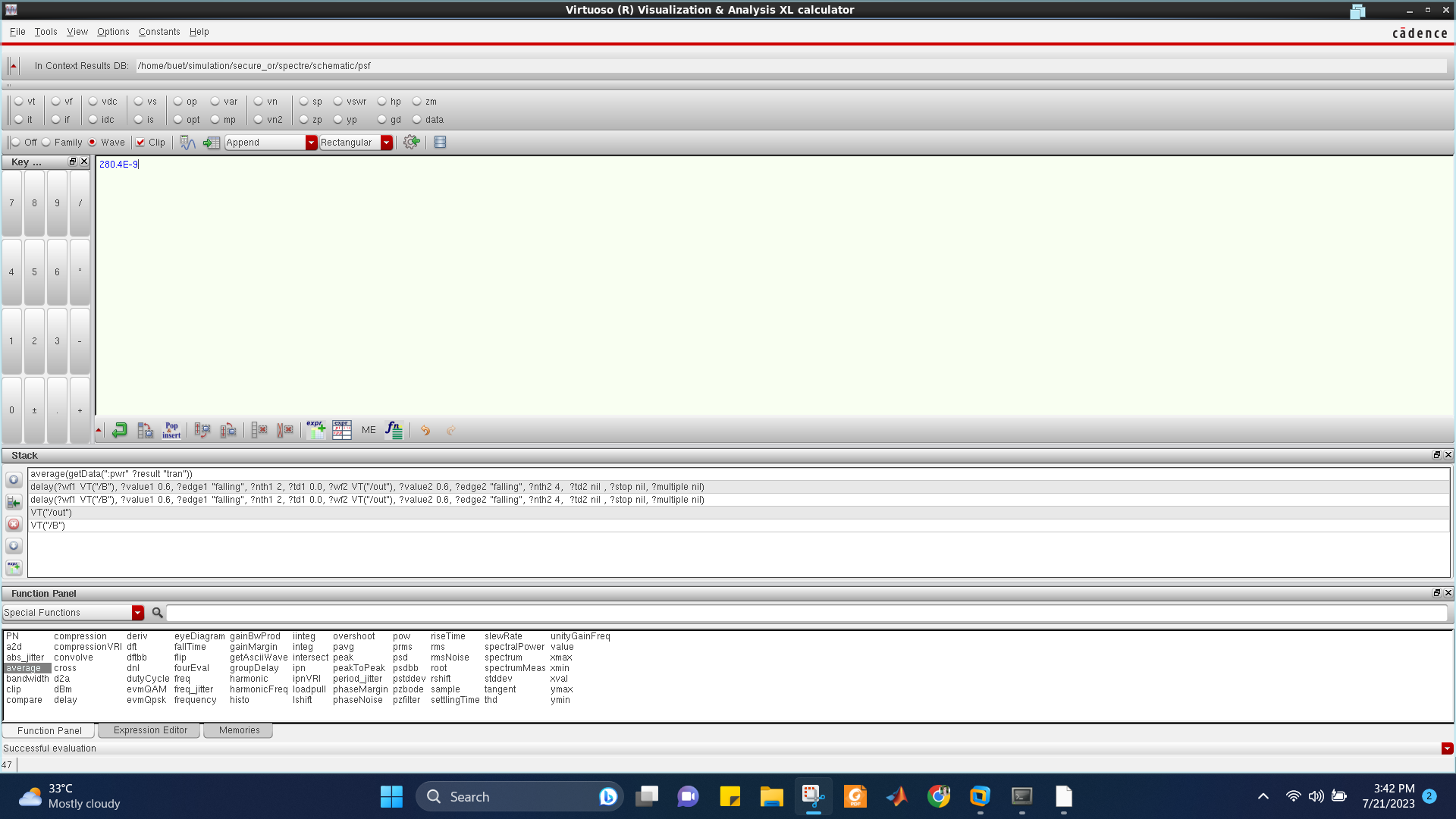
**Secure OR Waveform**

****

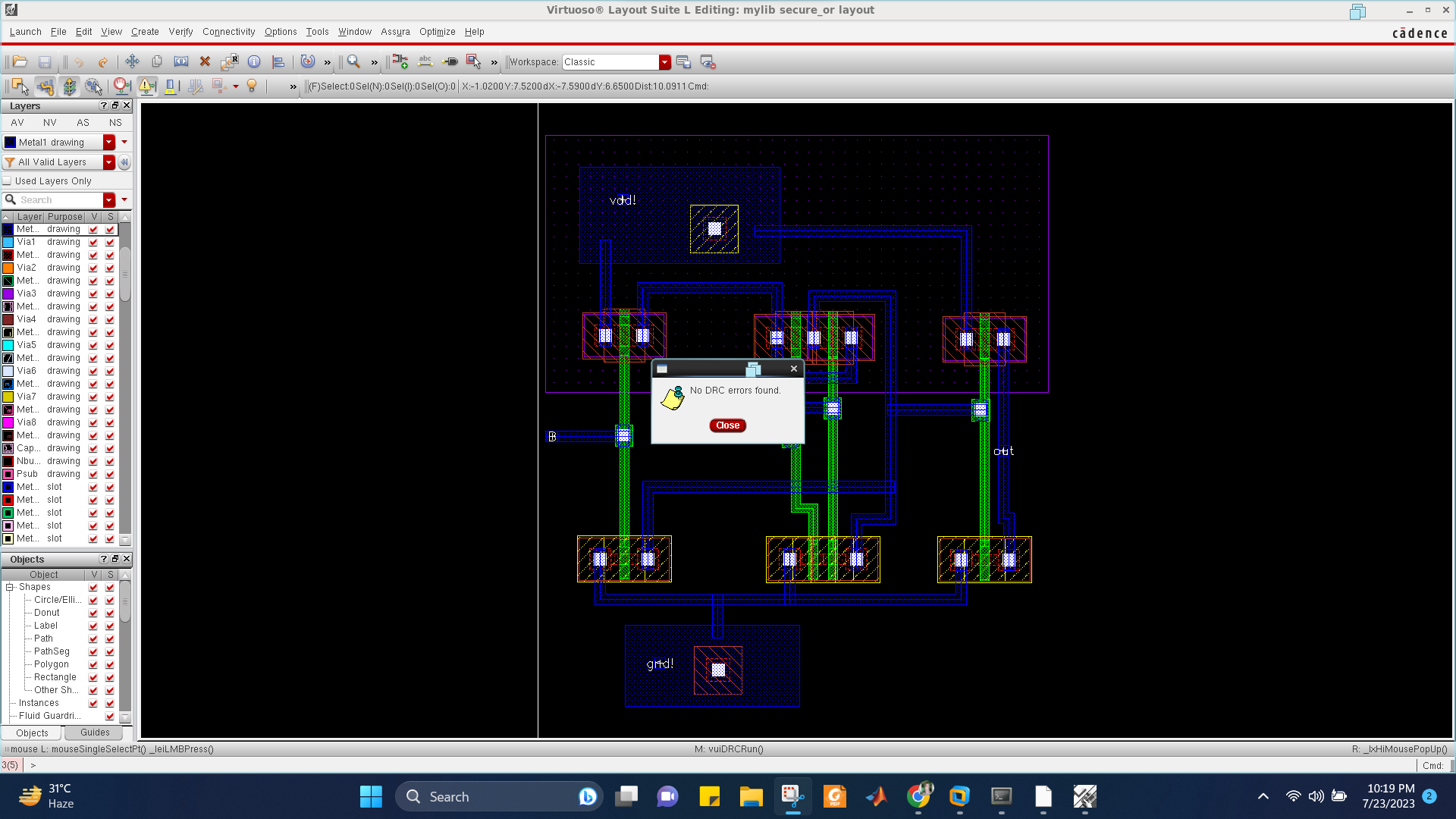
**Secure OR Propagation Delay**

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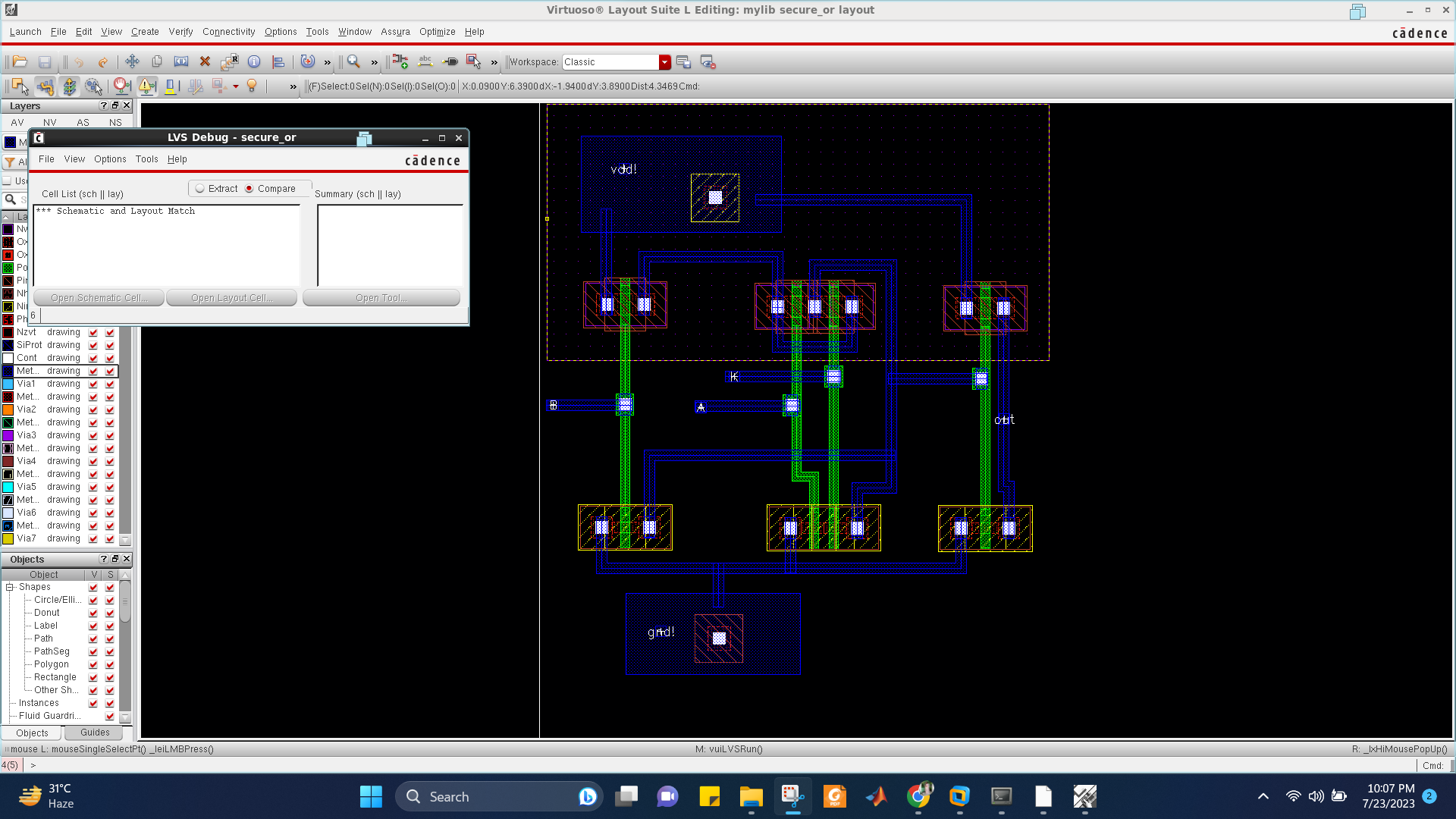
**Secure OR Average Power**

****

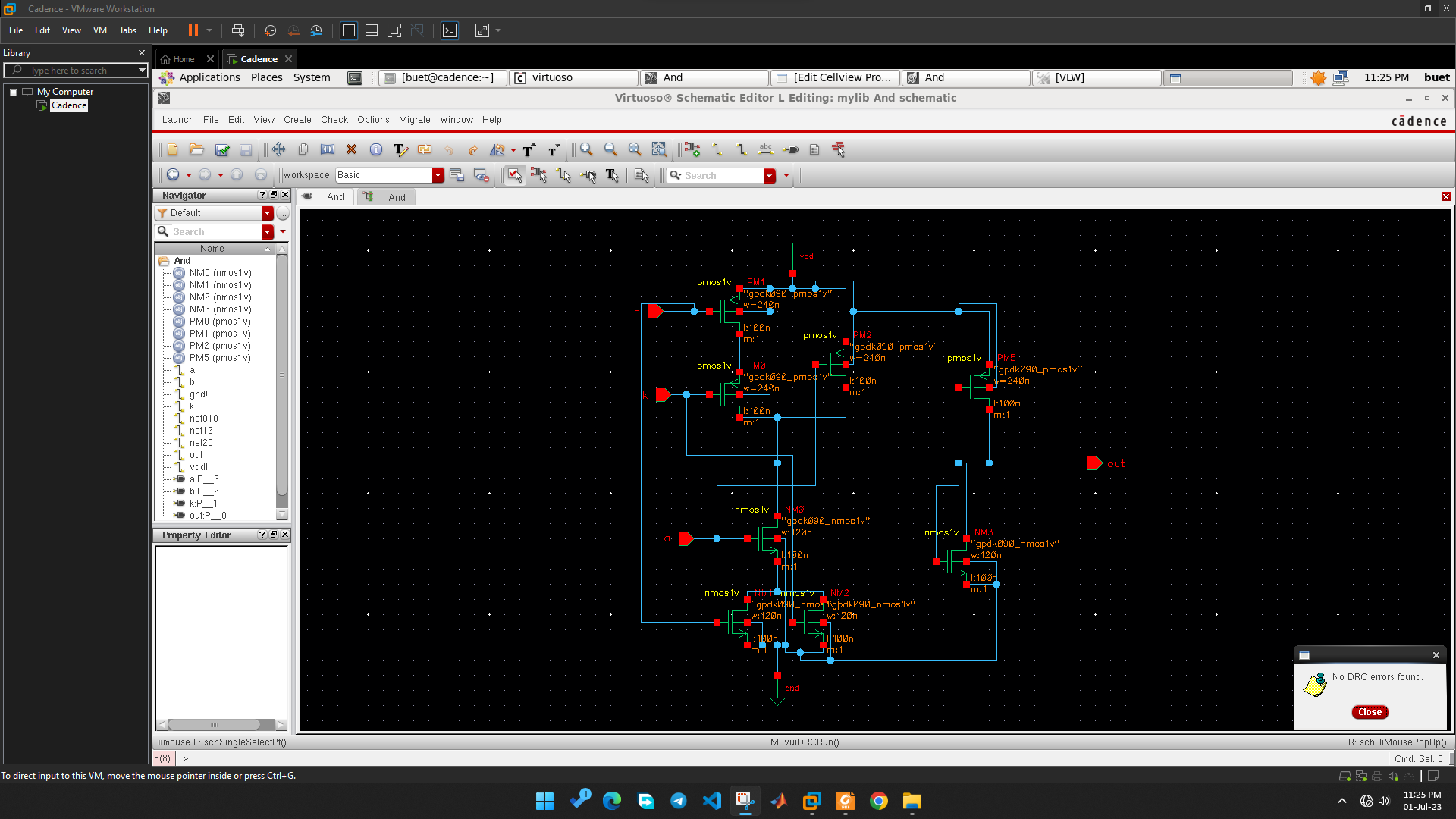
**Secure OR Layout DRC**

****

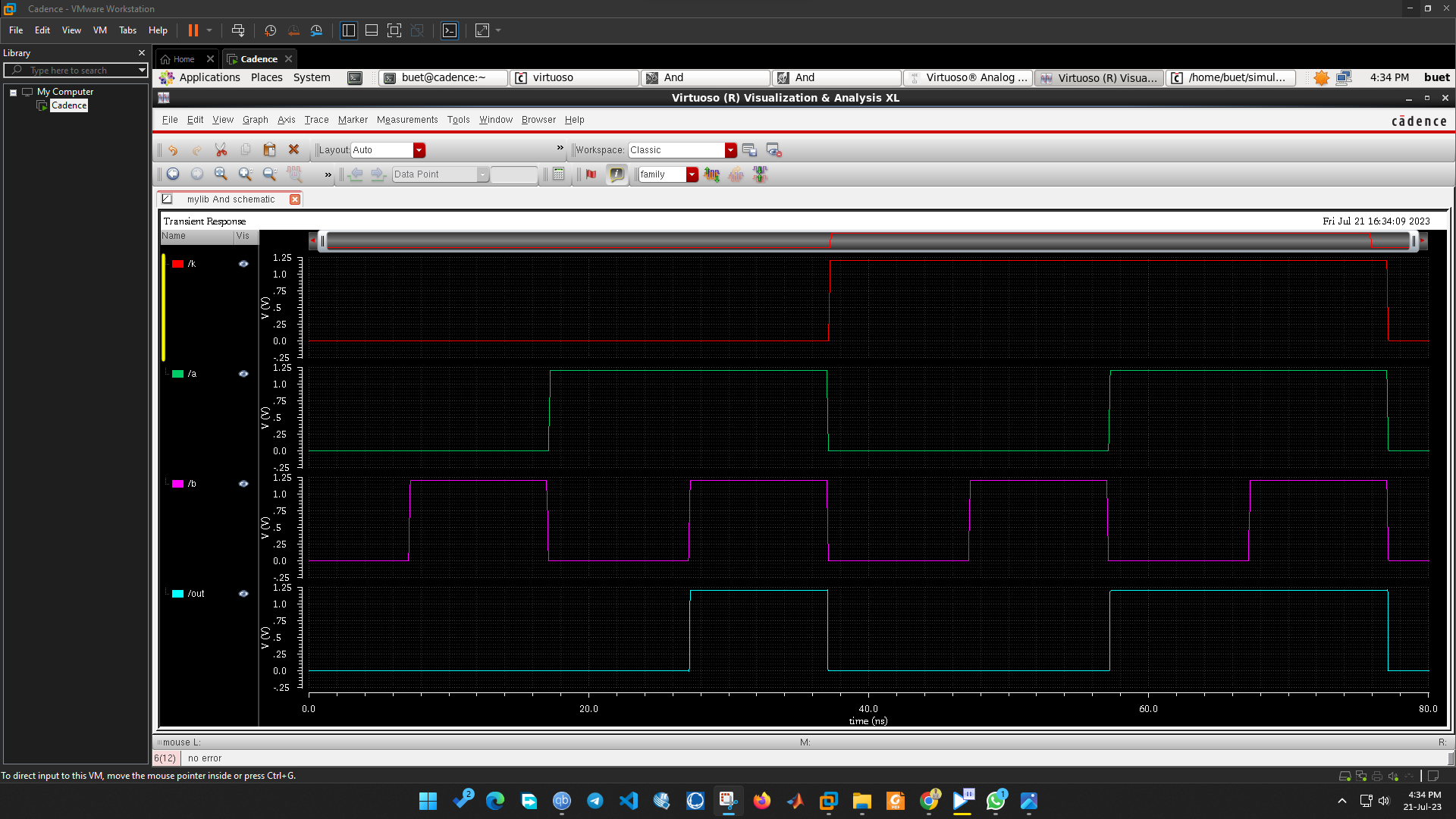
**Secure OR Layout LVS**

****

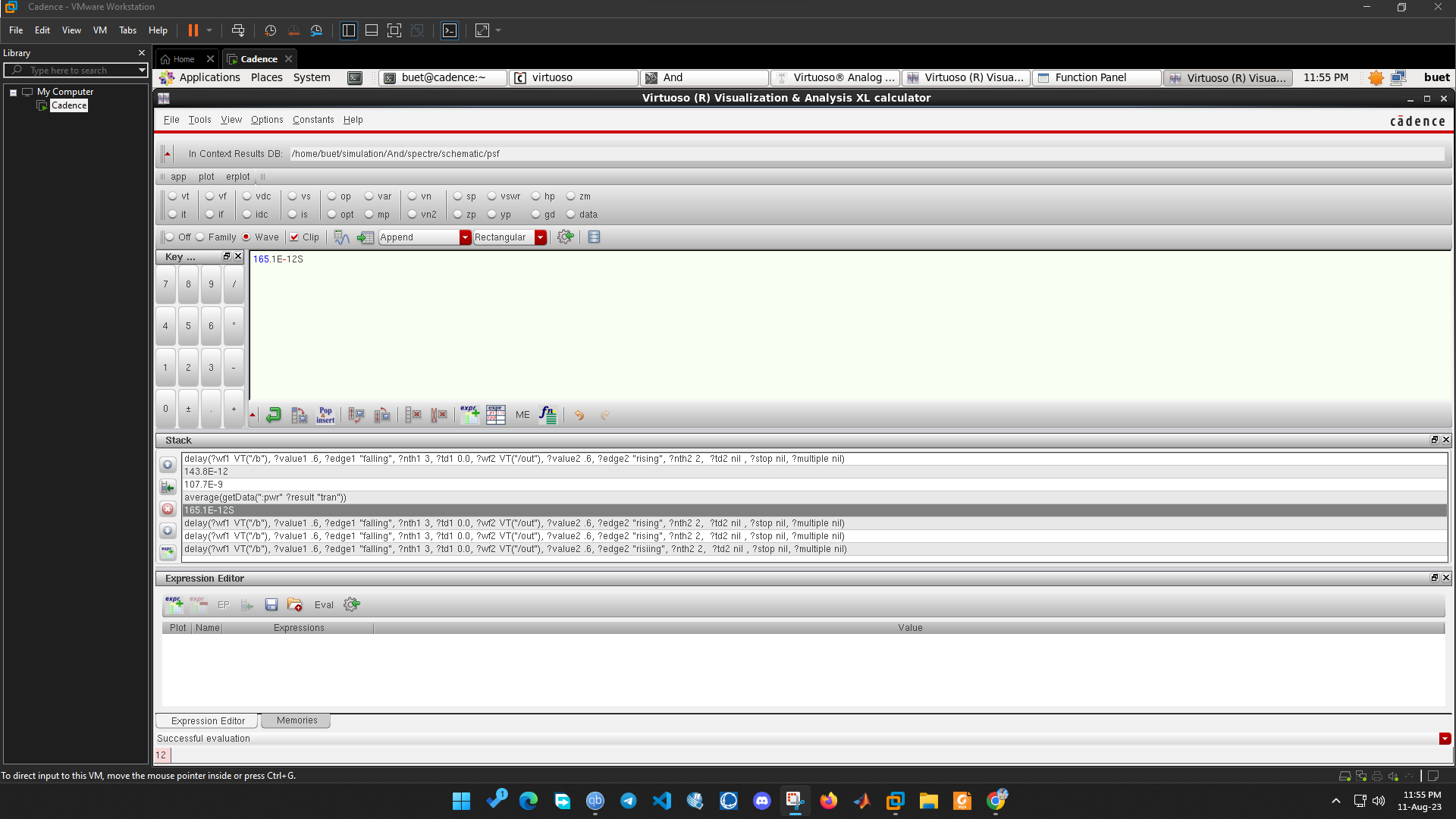
**Secure AND Schematic**

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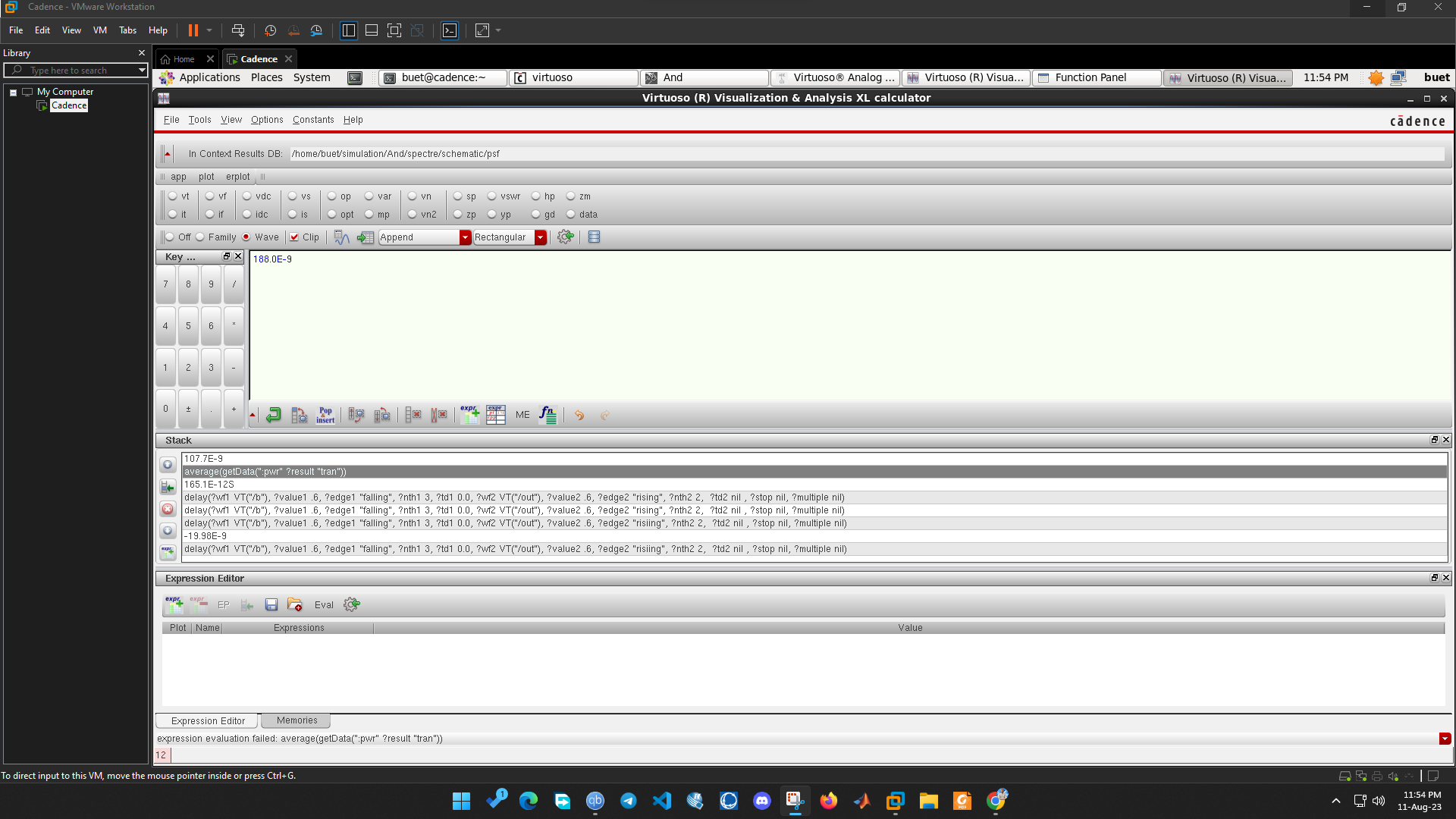
**Secure AND Waveform**

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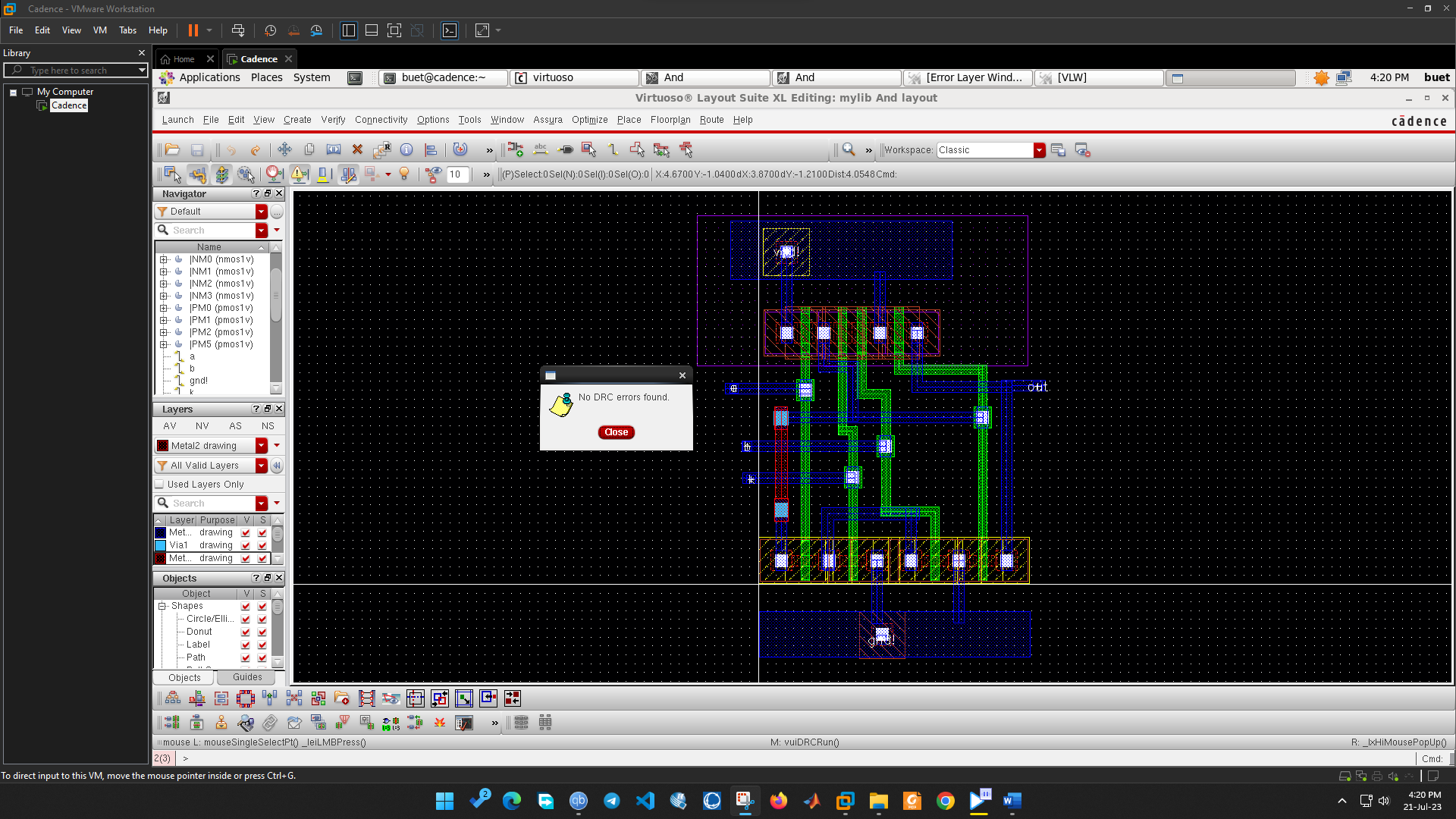
**Secure AND Propagation Delay**

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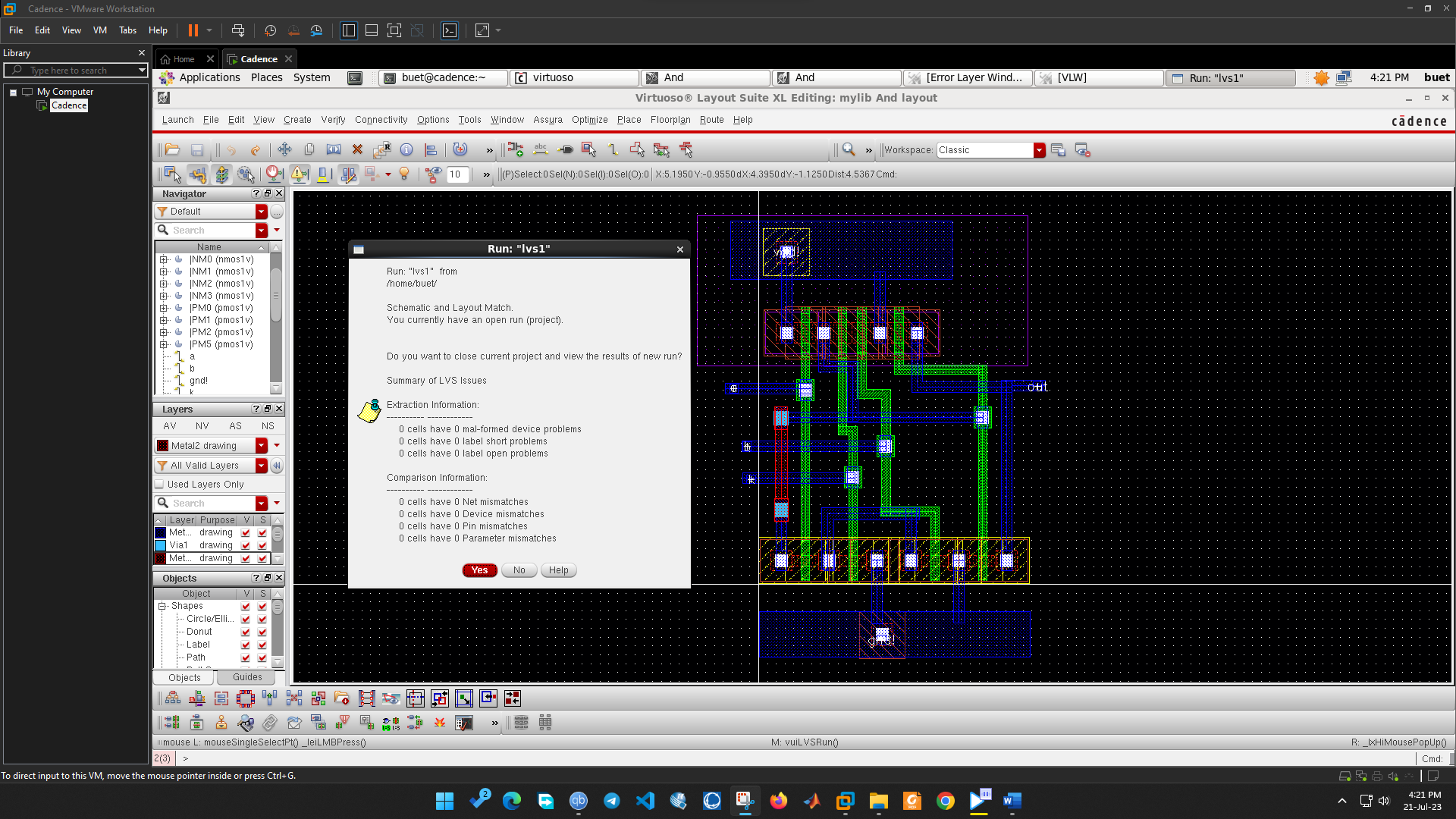
**Secure AND Average Power**

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**Secure AND Layout DRC**

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**Secure AND Layout LVS**

****

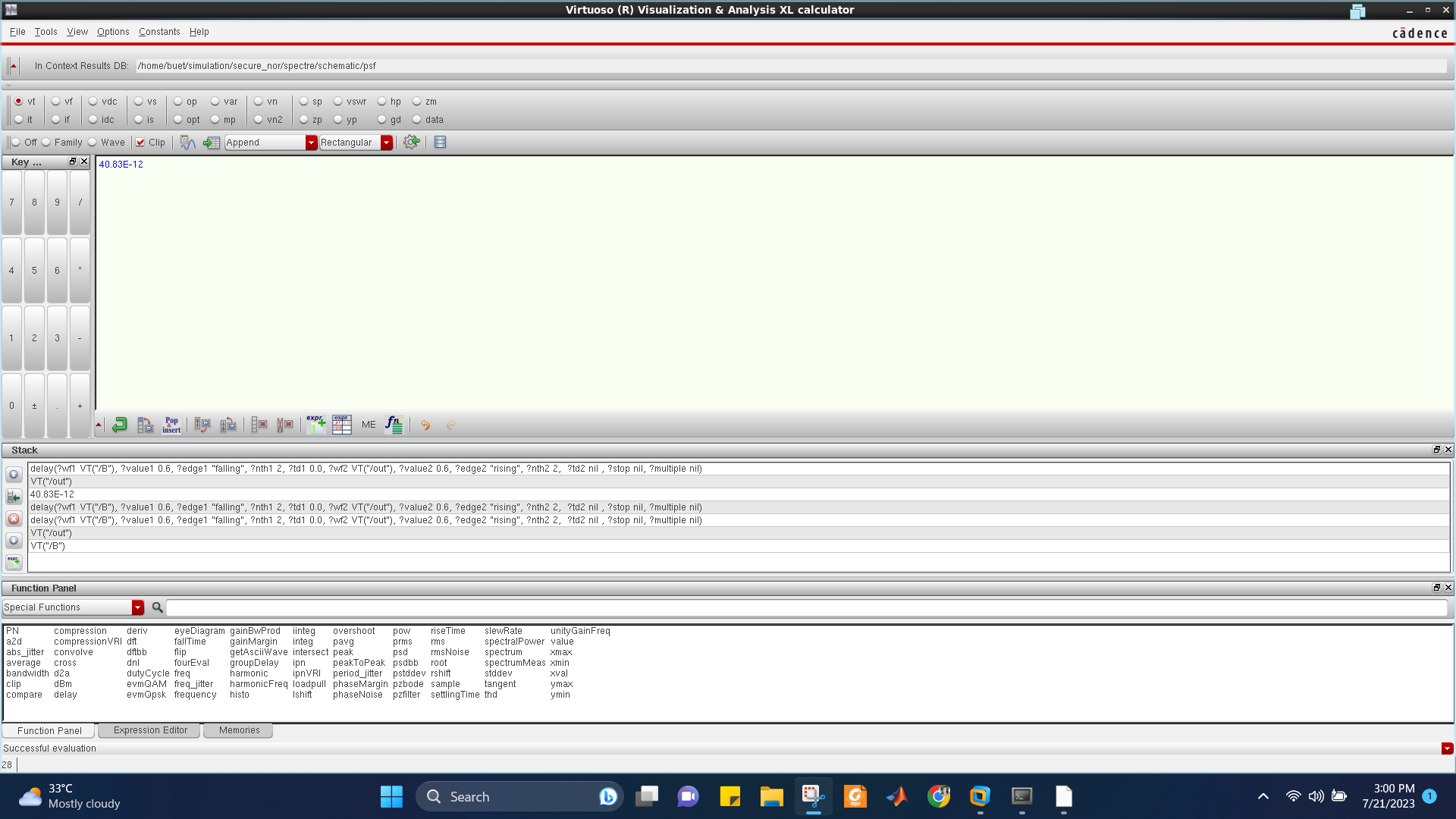
**Secure NOR Schematic**

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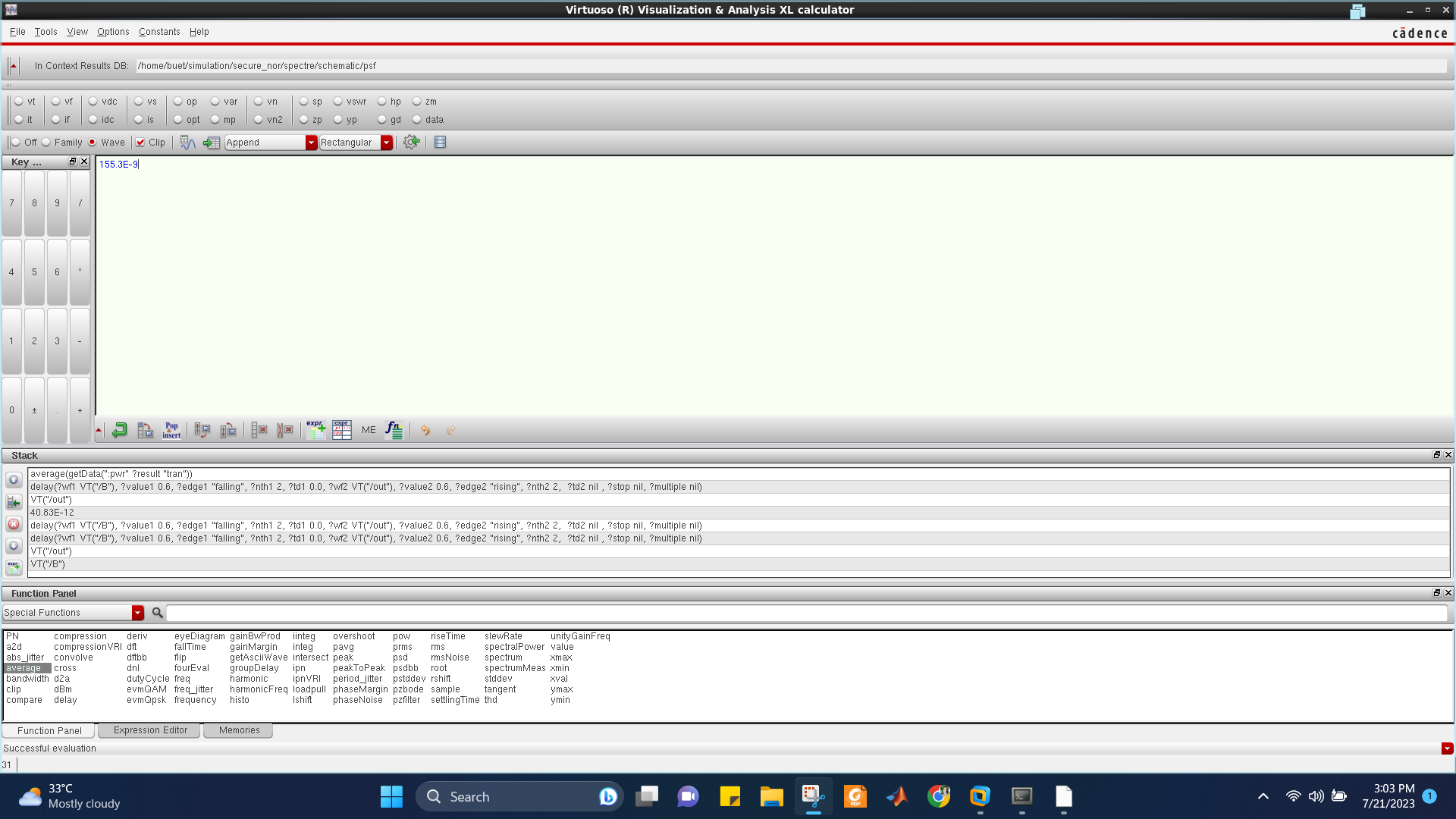
**Secure NOR Waveform**

****

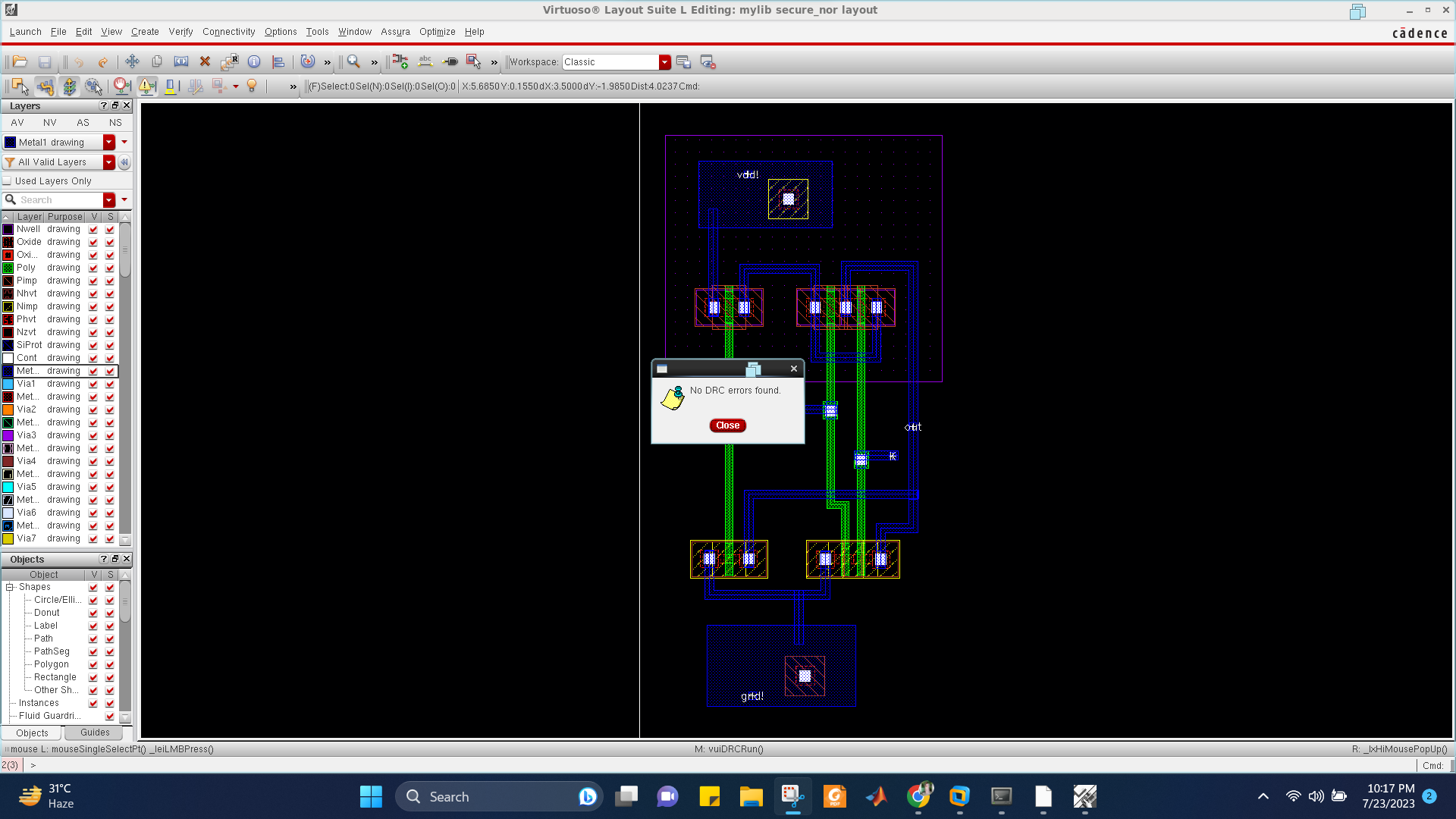
**Secure NOR Propagation Delay**

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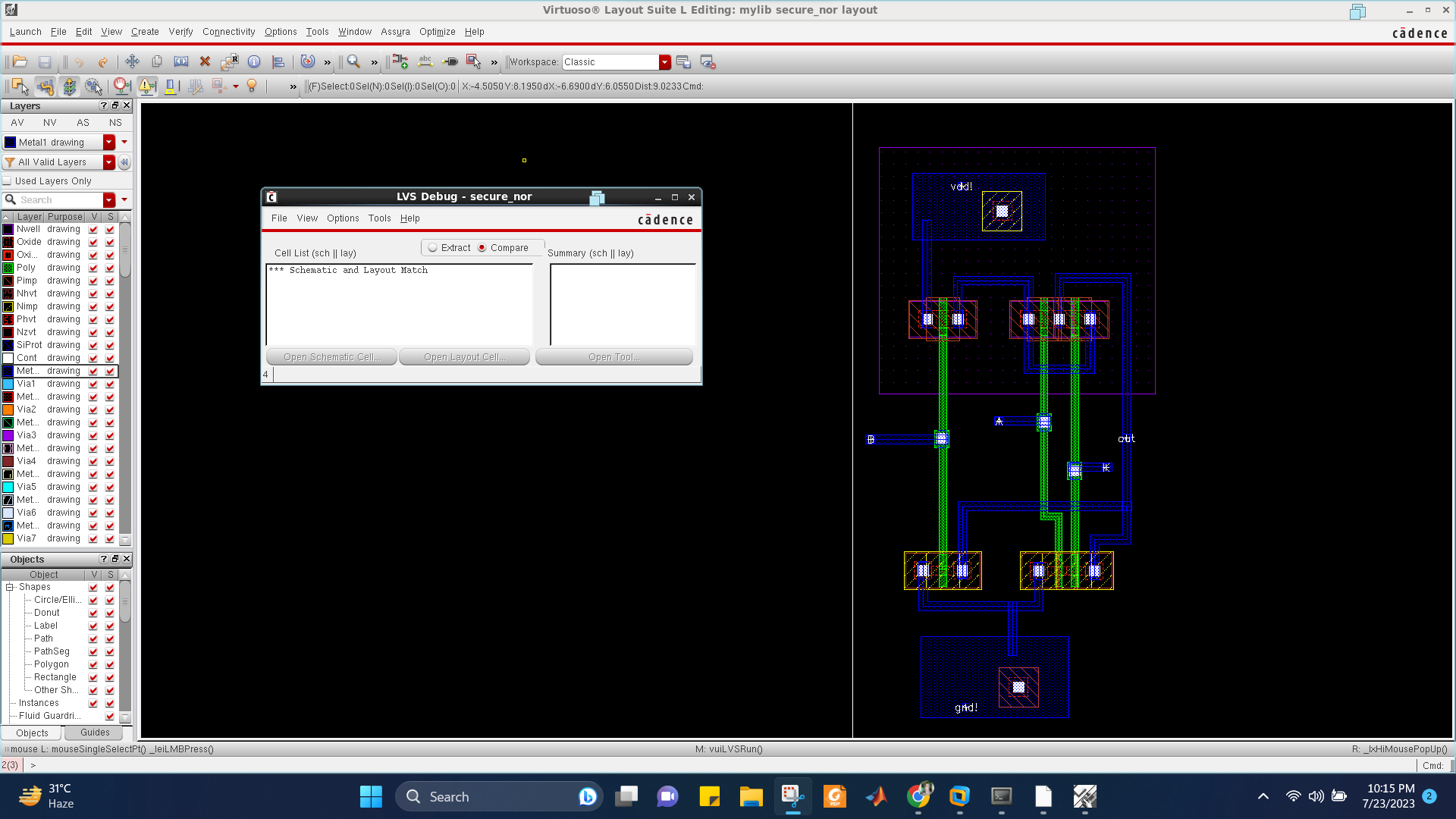
**Secure NOR Average Power**

****

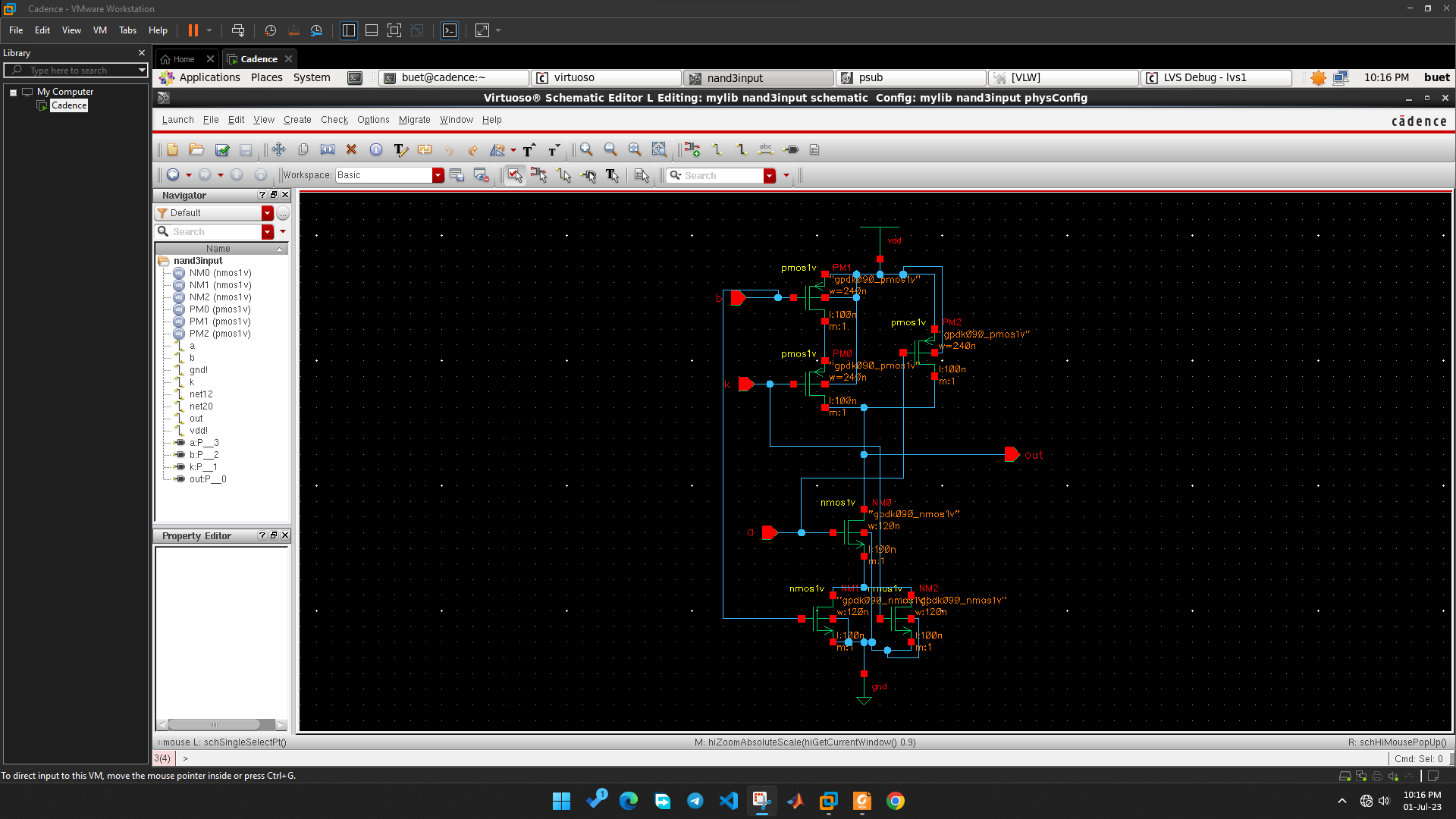
**Secure NOR Layout DRC**

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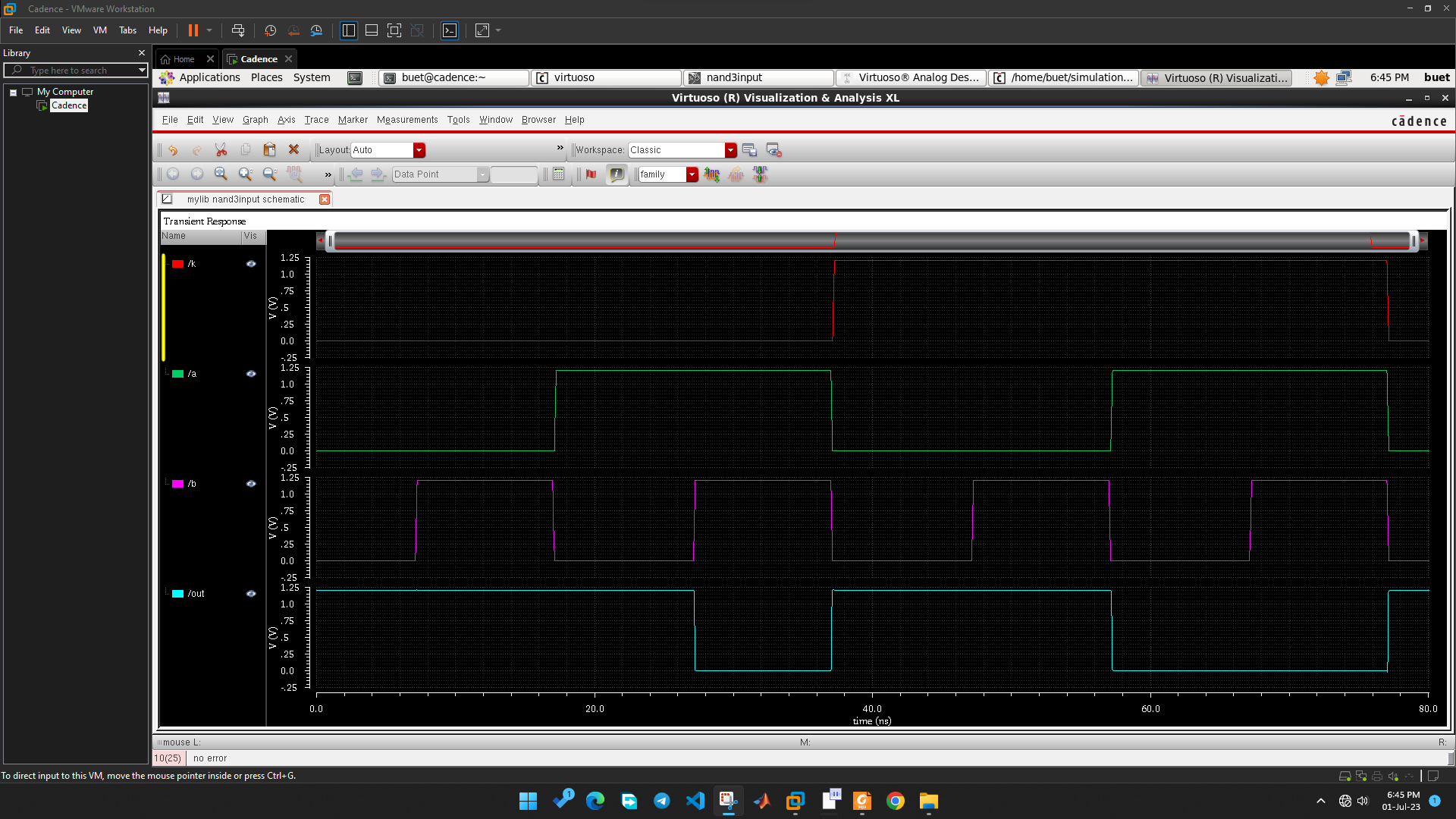
**Secure NOR Layout LVS**

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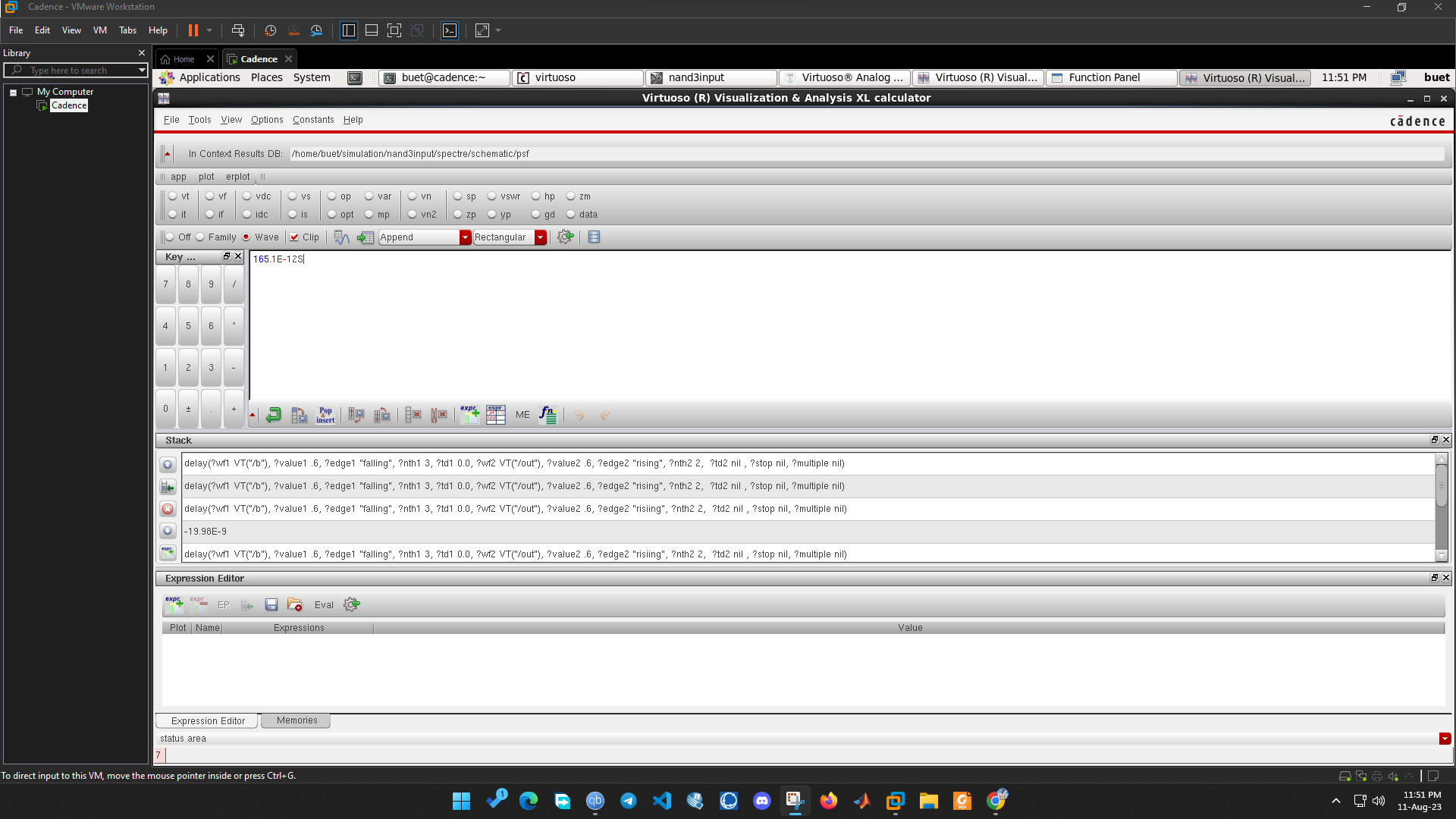
**Secure NAND Schematic**

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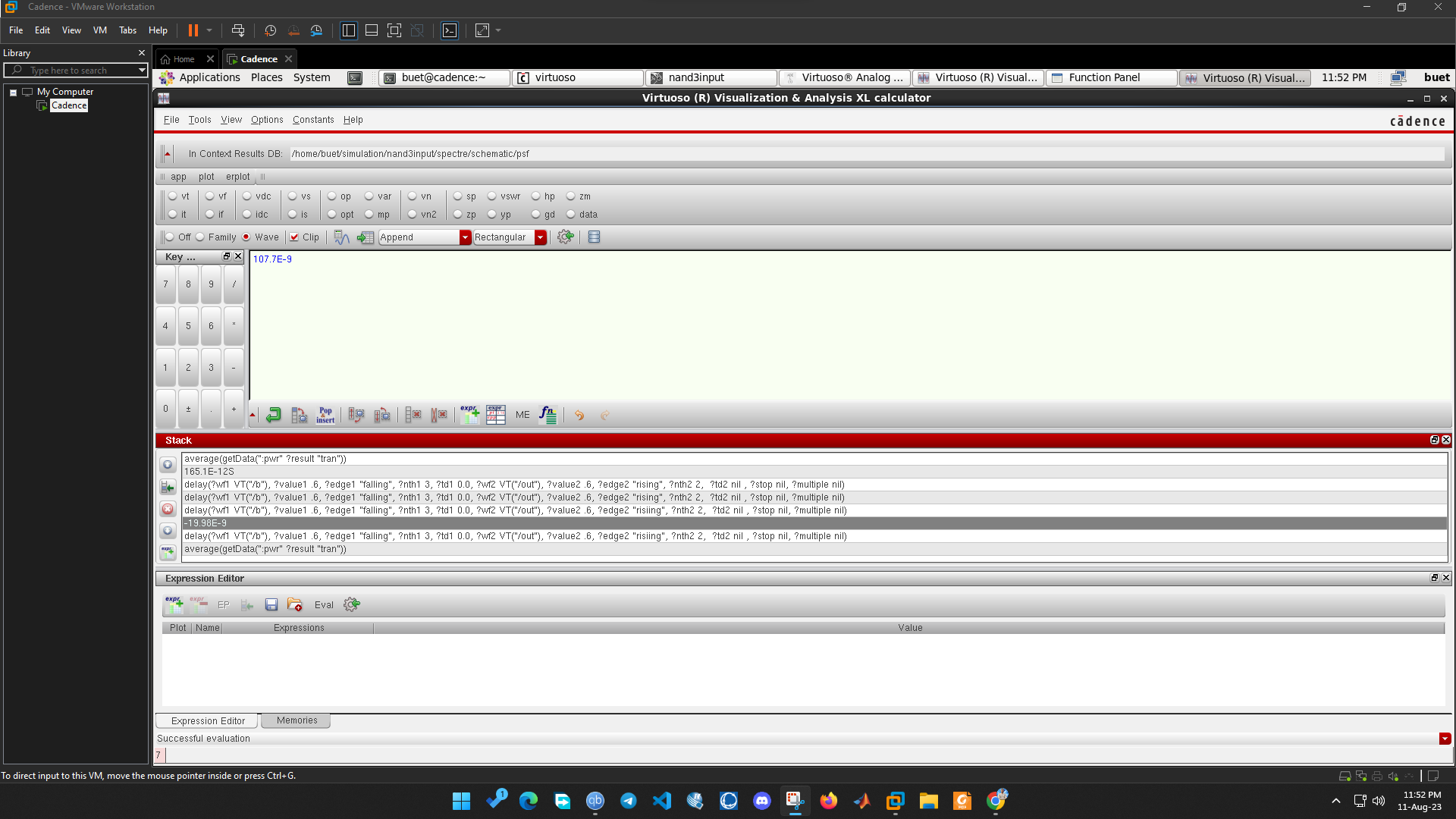
**Secure NAND Waveform**

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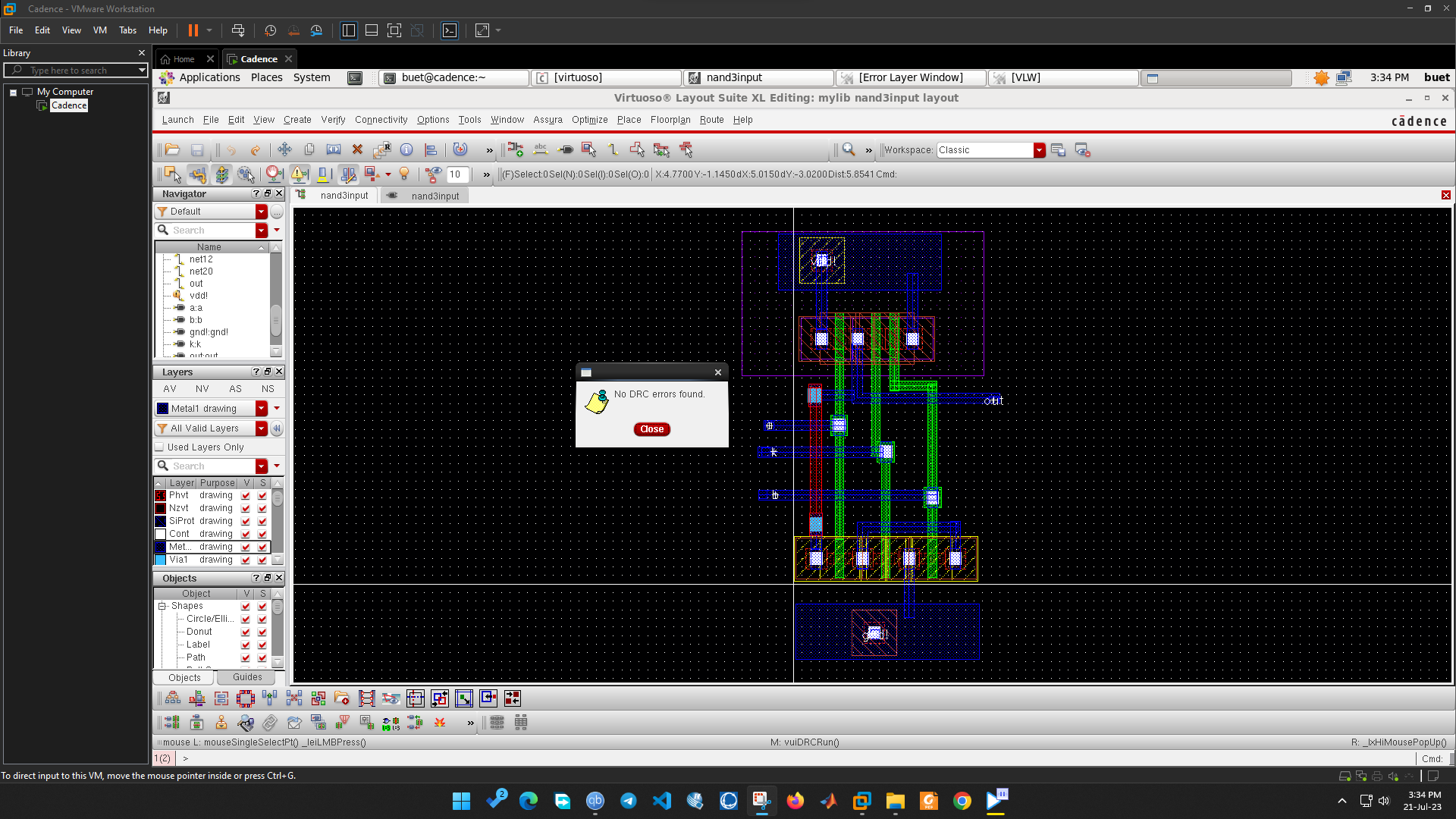
**Secure NAND Propagation Delay**

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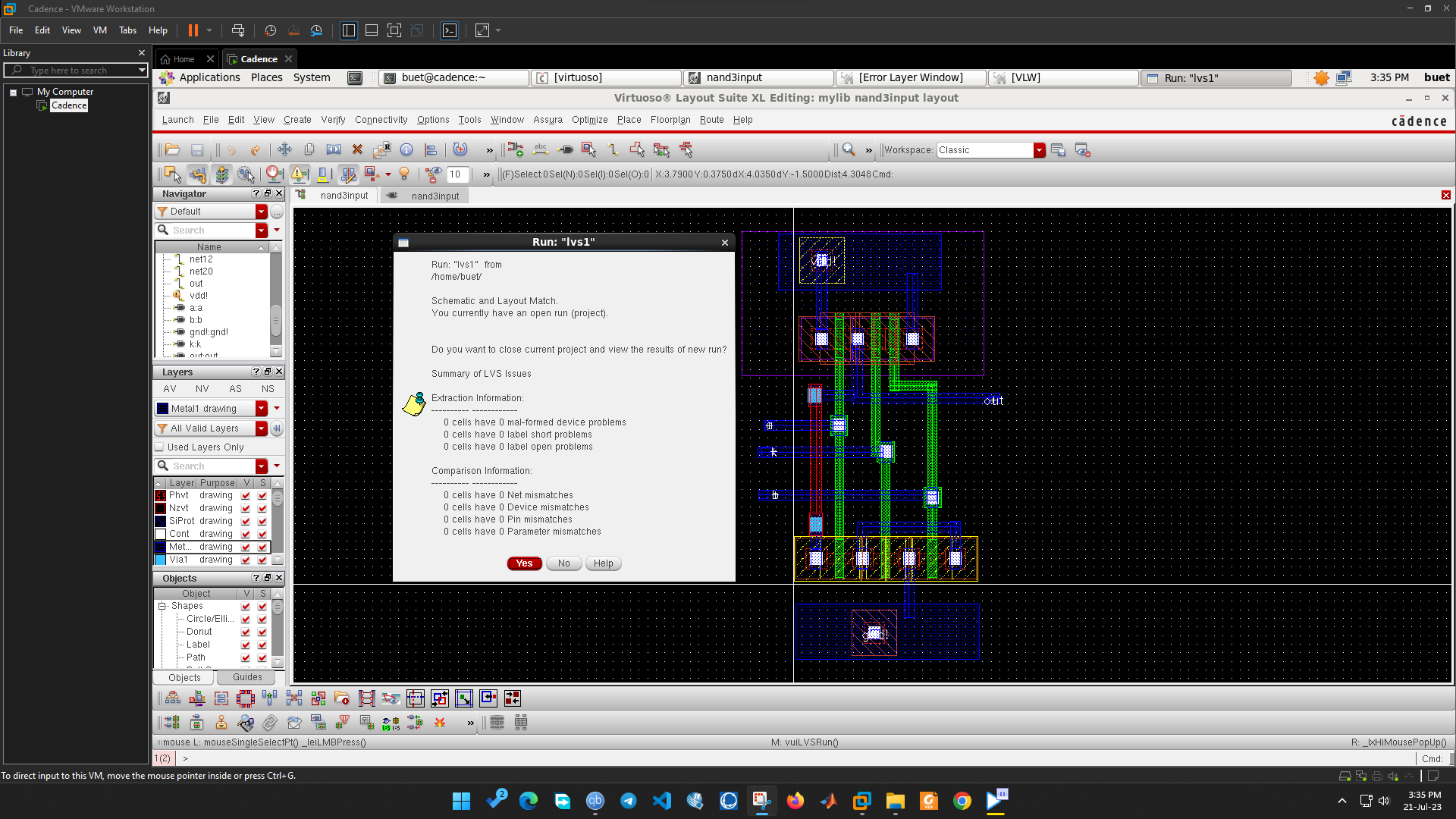
**Secure NAND Average Power**

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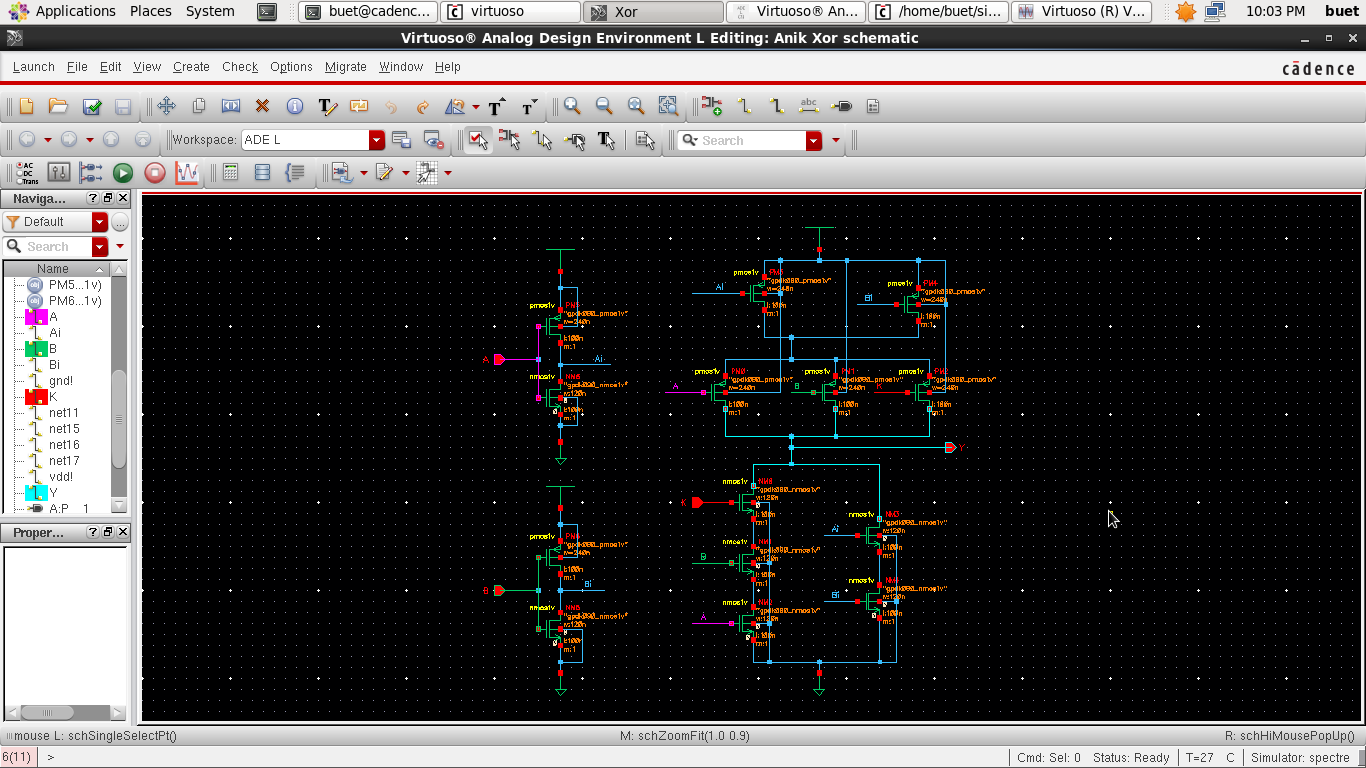
**Secure NAND Layout DRC**

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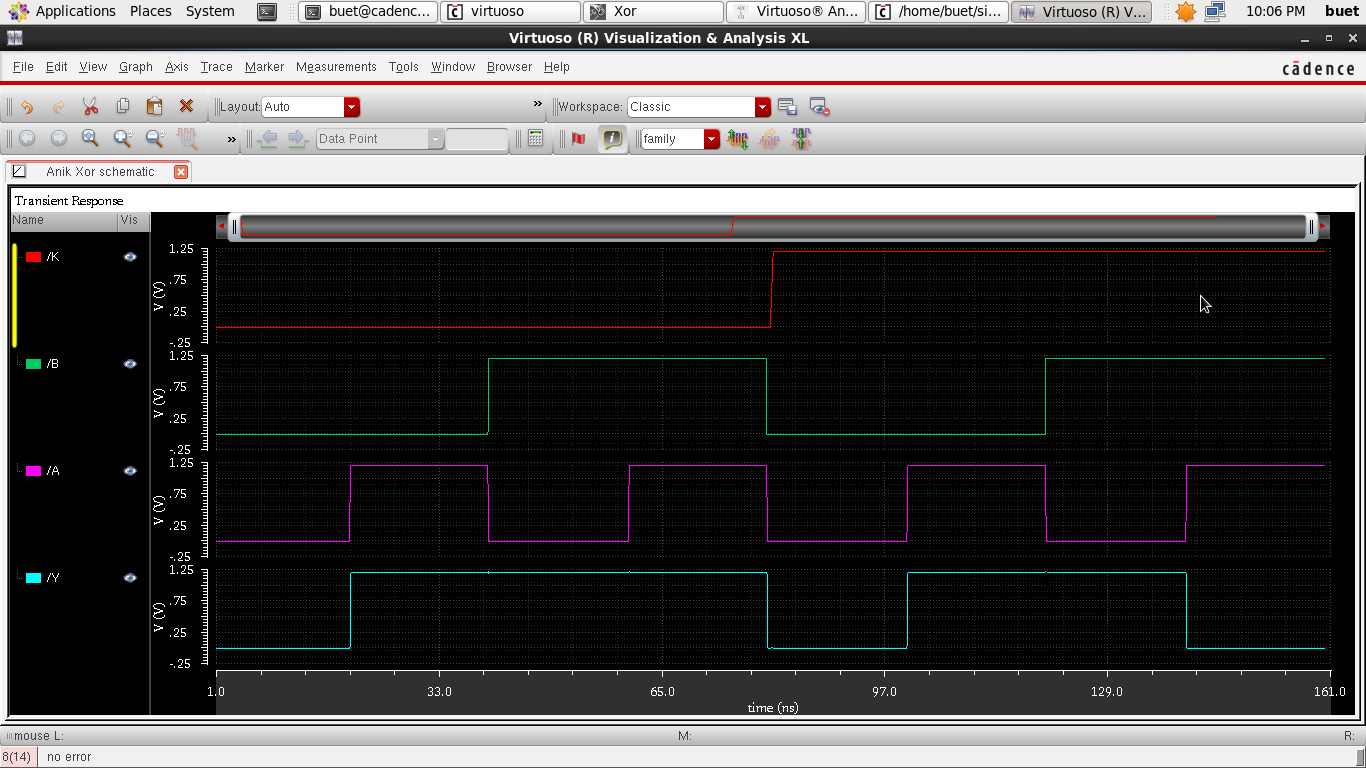
**Secure NAND Layout LVS**

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**Secure XOR Schematic**



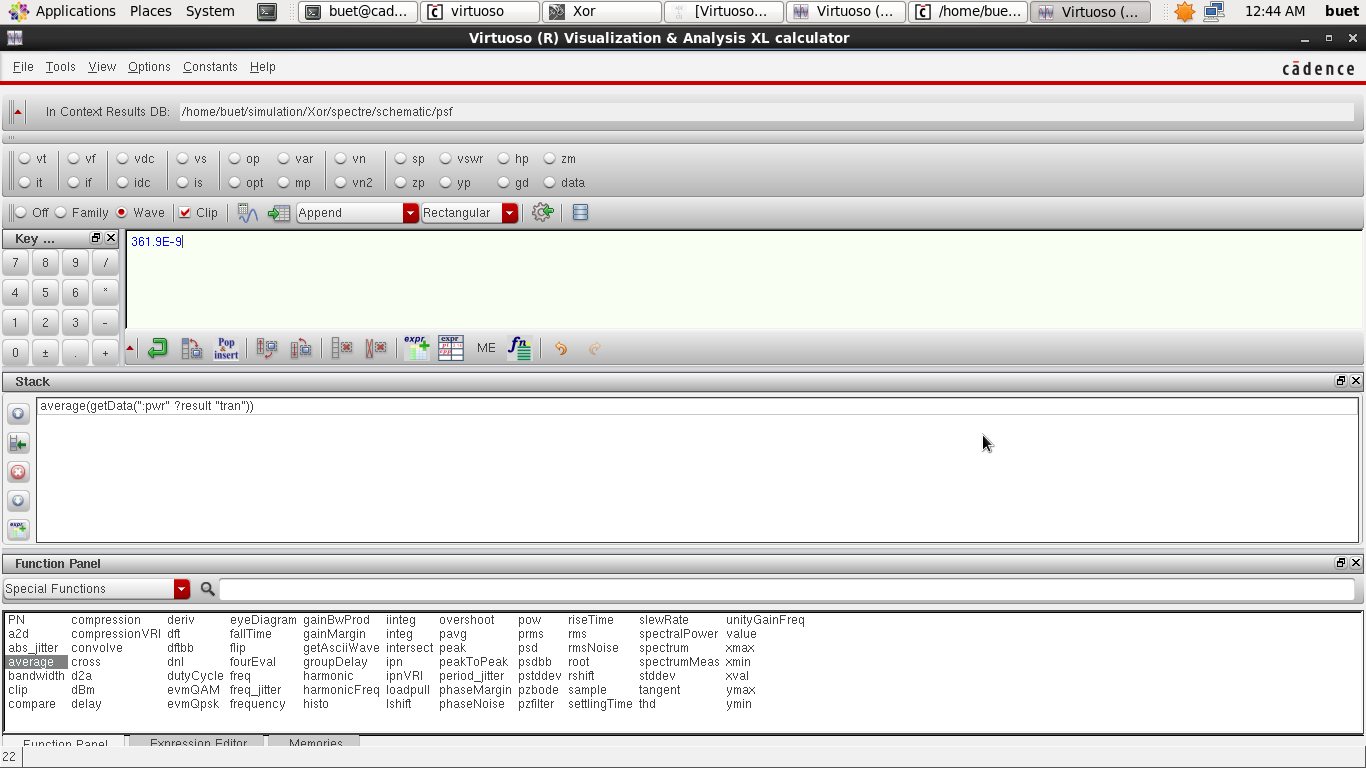
**Secure XOR Waveform**



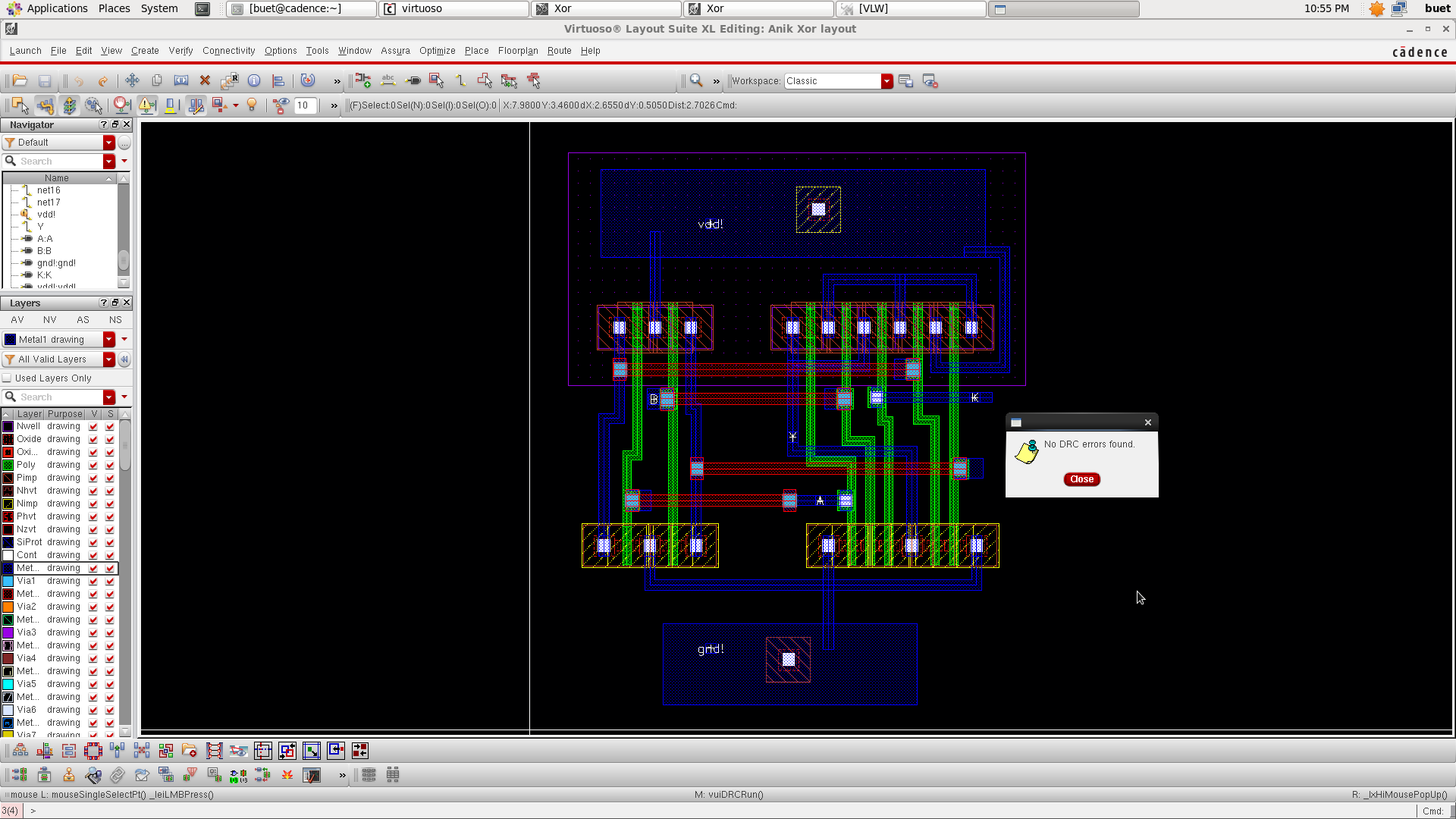
**Secure XOR Propagation Delay**



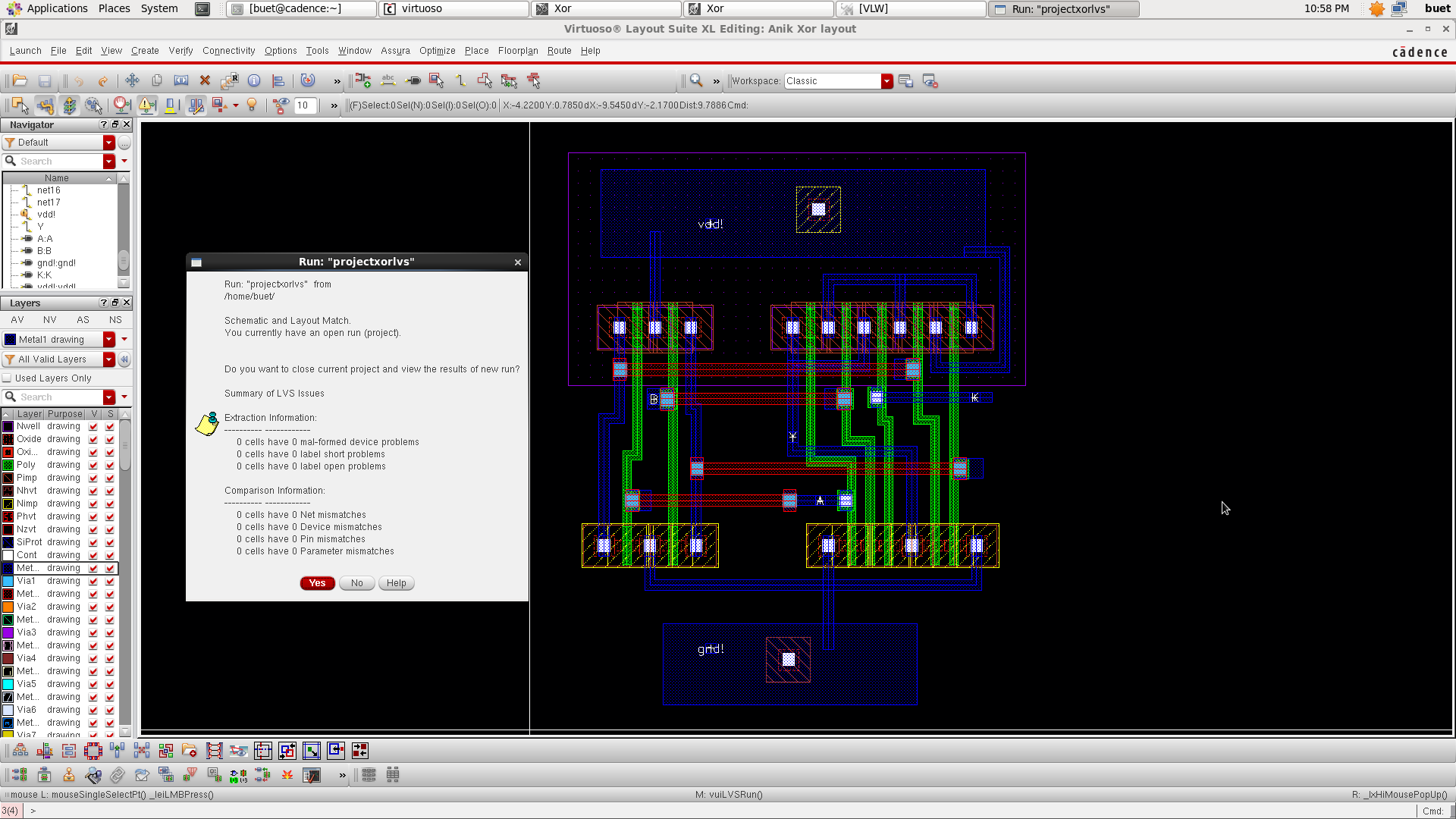
**Secure XOR Average Power**



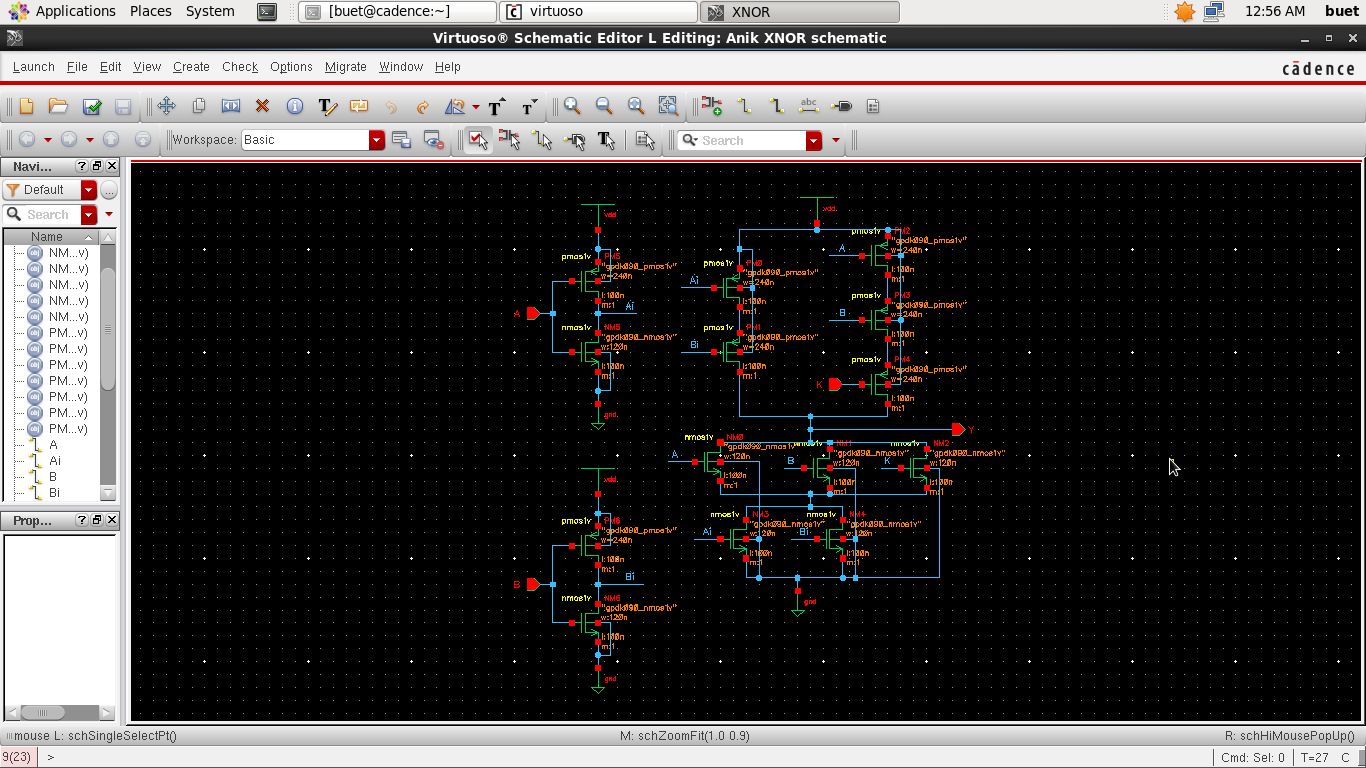
**Secure XOR Layout DRC**



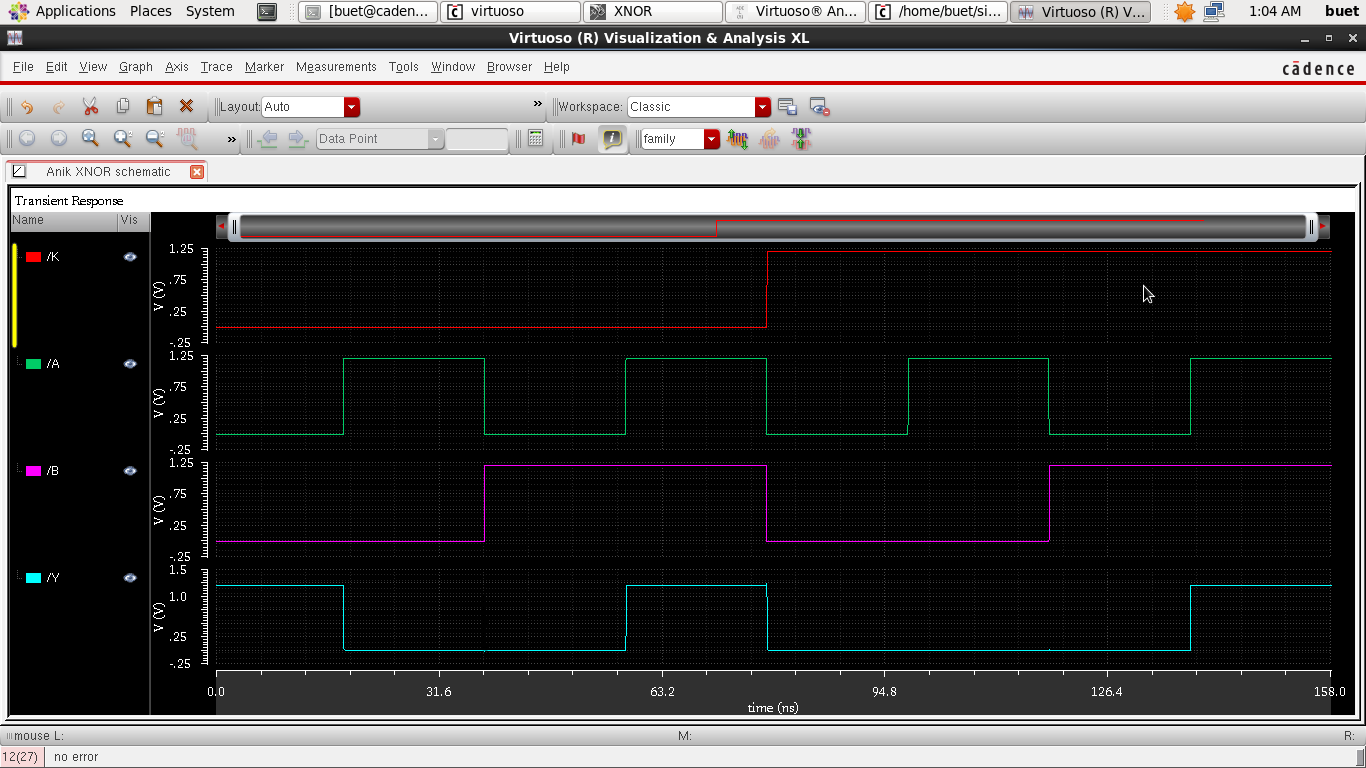
**Secure XOR Layout LVS**



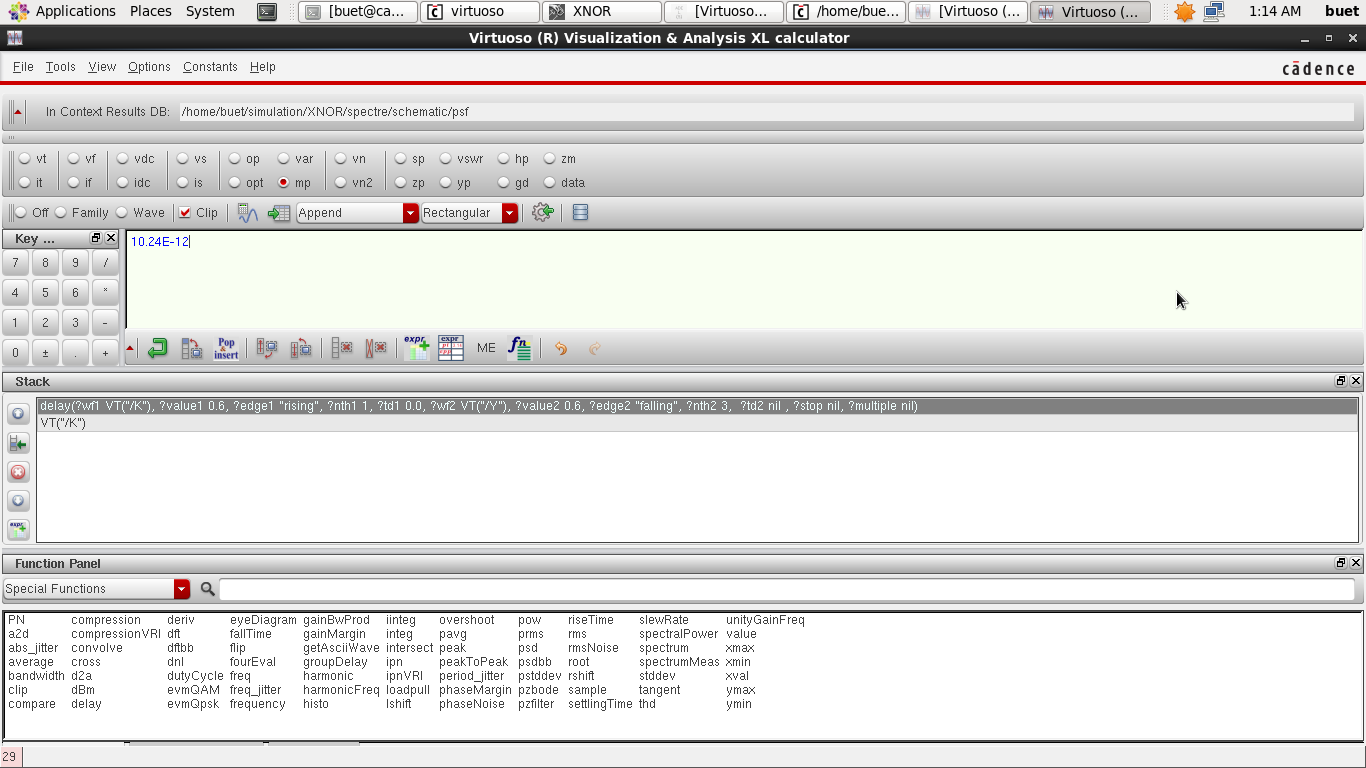
**Secure XNOR Schematic**



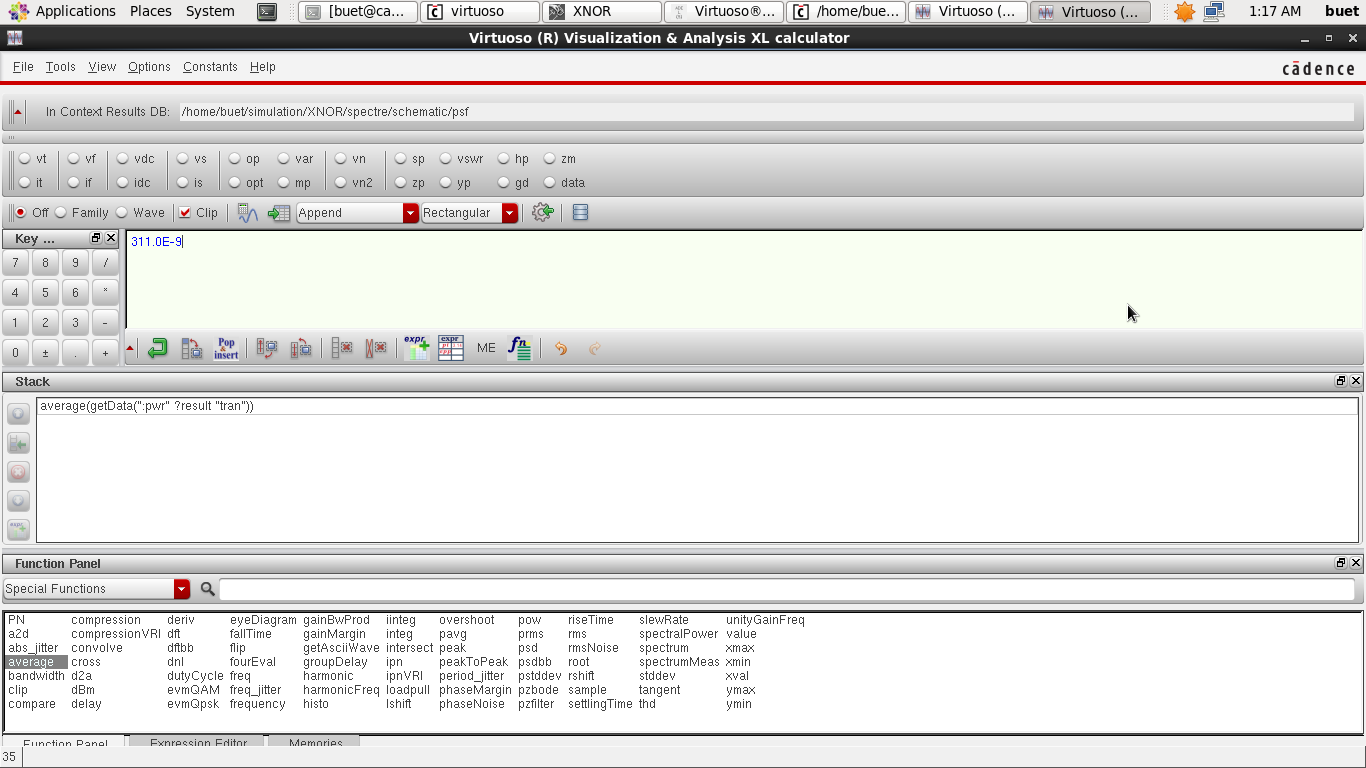
**Secure XNOR Waveform**

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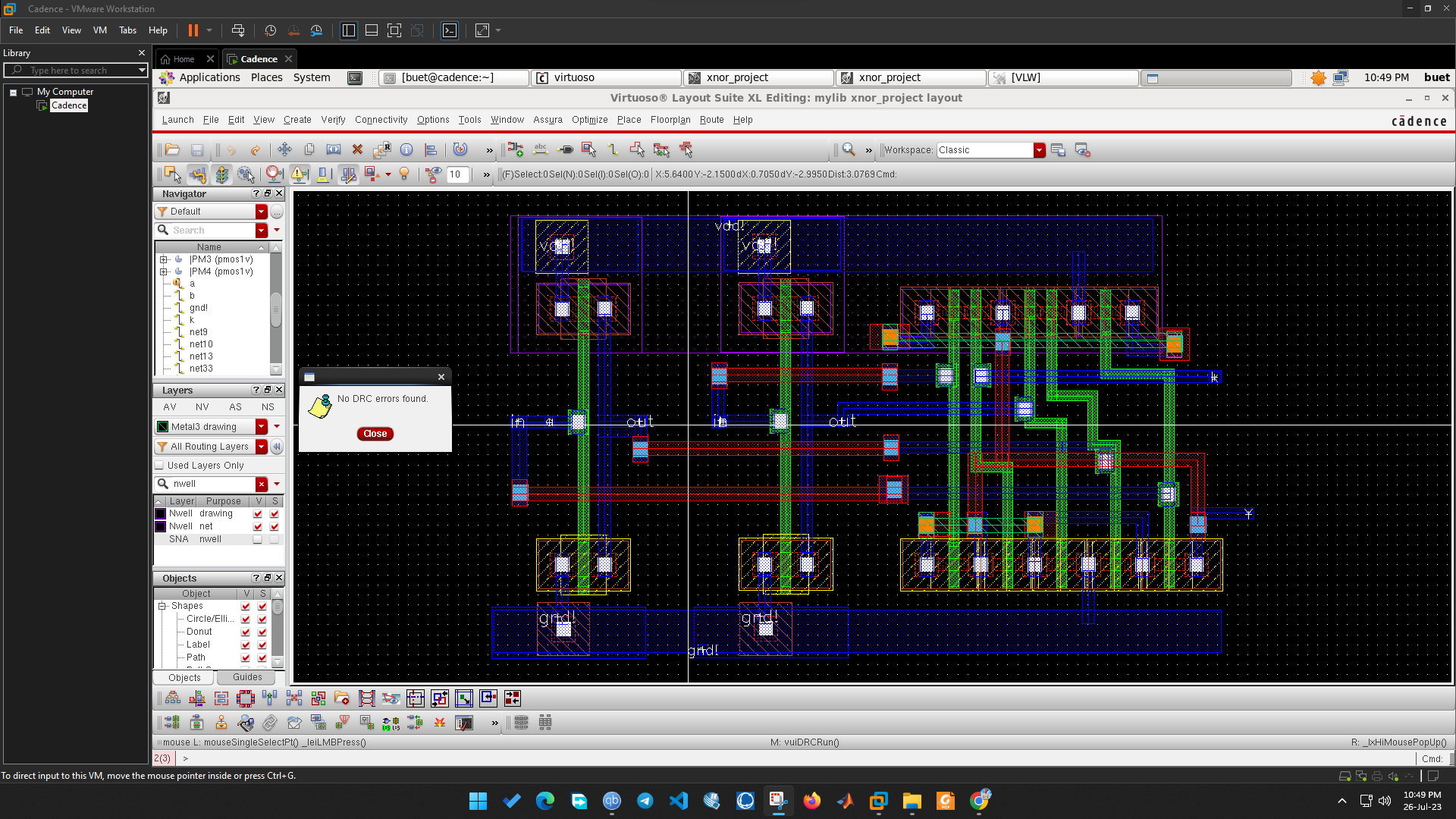
**Secure XNOR Propagation Delay**



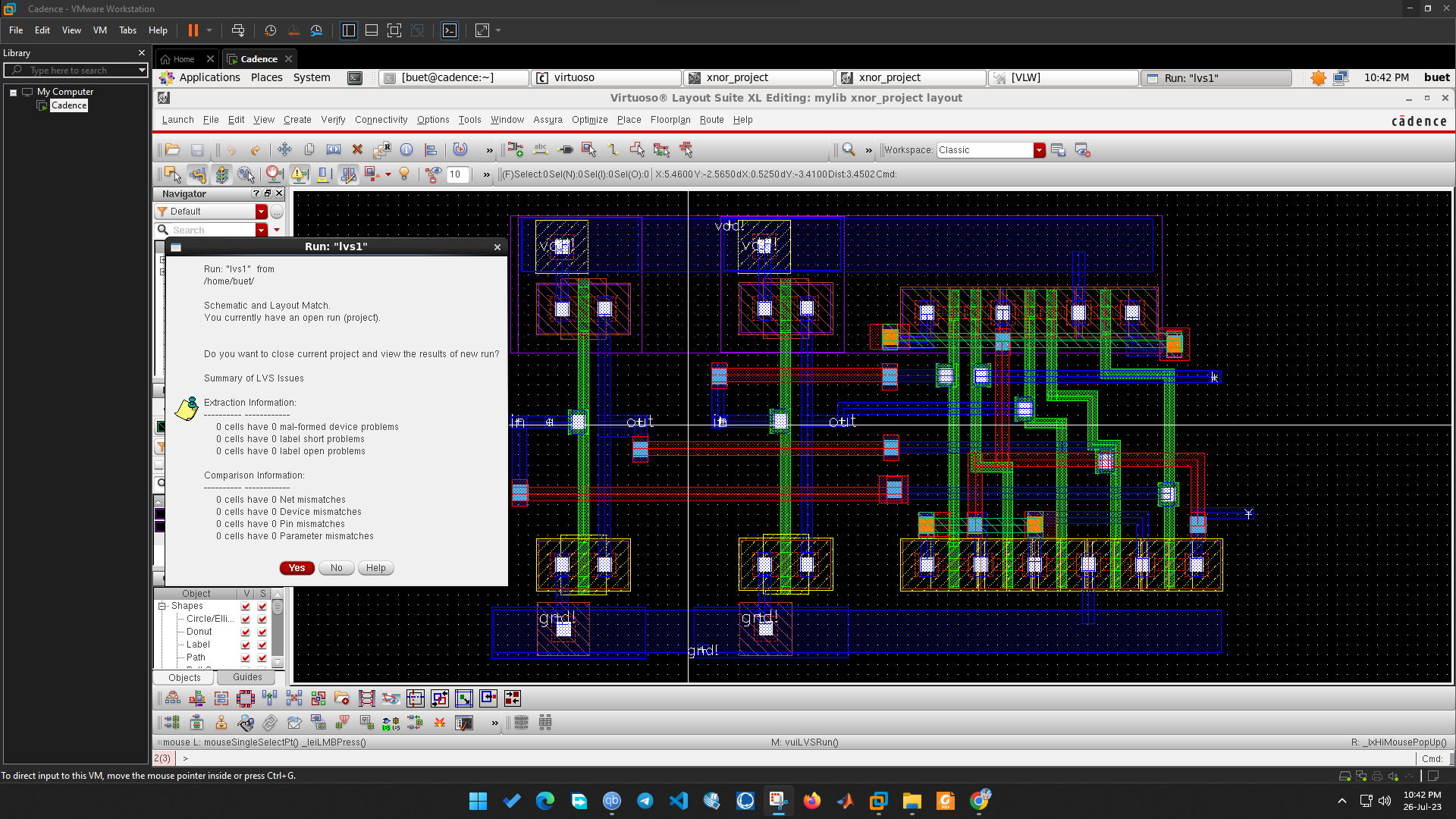
**Secure XNOR Average Power**



**Secure XNOR Layout DRC**

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**Secure XNOR Layout LVS**

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