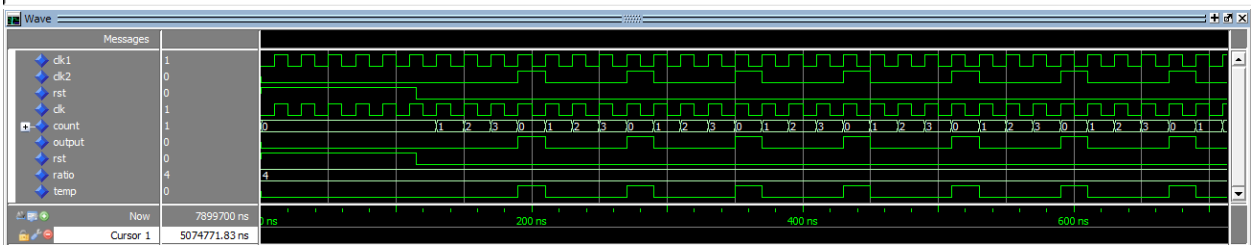
clk_div

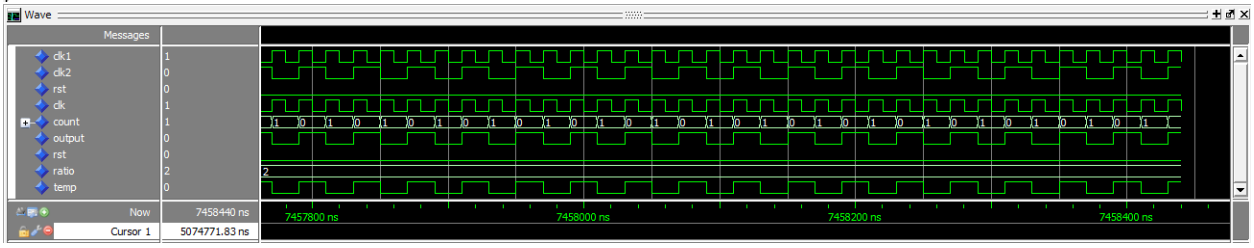
RATIO = 4

```
# Loading work.clk_div_tb(tb)
# Loading work.clk_div(str)
# Loading work.counter(bhv)
VSIM 87> run -all
# Break key hit
# Break key hit
# Break in Architecture tb at C:/Users/Nick/Documents/Spring 2016/EEL 4712/Digital-Design-Labs/Lab-4/clk_gen/clk_div_tb.vhd line 41

VSIM 88>
```



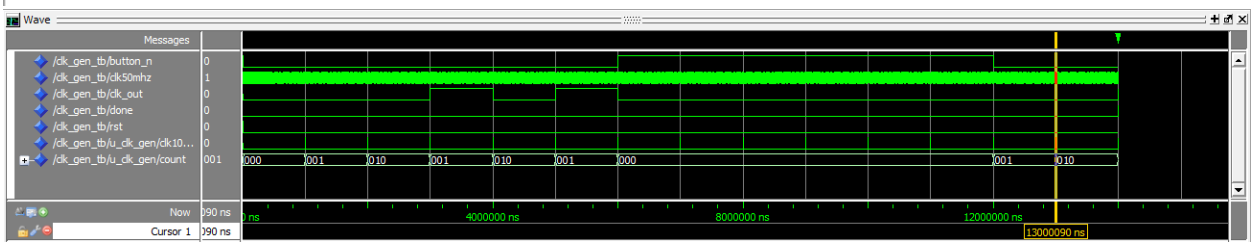
RATIO = 2

```
# Loading work.clk_div_tb(tb)
# Loading work.clk_div(str)
# Loading work.counter(bhv)
VSIM 85> run -all
# Break key hit
# Break in Process line__30 at C:/Users/Nick/Documents/Spring 2016/EEL 4712/Digital-Design-Labs/Lab-4/clk_gen/counter.vhd line 30

VSIM 86>
```



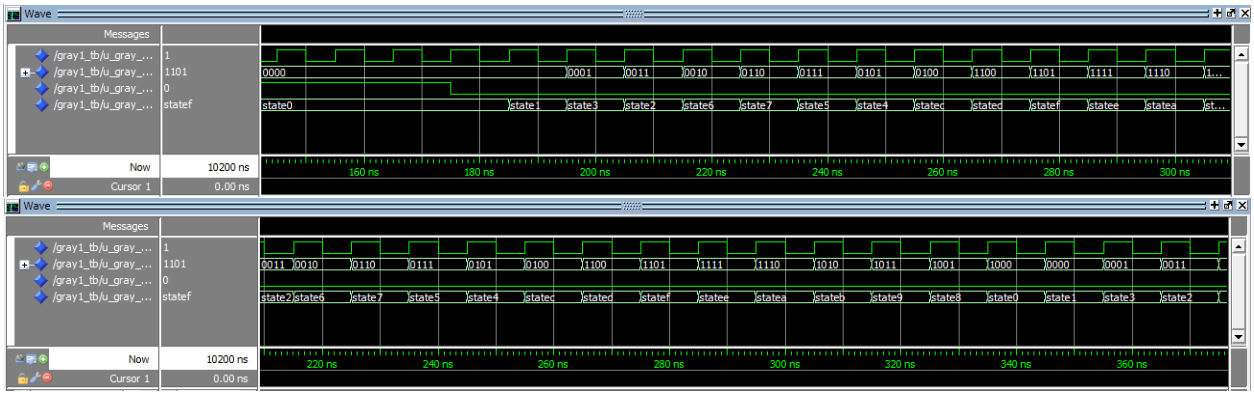
clk_gen

```
# Loading work.clk_gen_tb(tb)
# Loading work.clk_gen(str)
# Loading work.clk_div(str)
# Loading work.counter(bhv)
VSIM 142> run -all
# ** Note: DONE!
#    Time: 14000090 ns  Iteration: 4  Instance: /clk_gen_tb

VSIM 143>
```



gray1

```
# vsim work.gray1_tb
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading work.gray1_tb(tb)
# Loading work.gray1(bhv)
VSIM 52> run -all
# ** Note: SIMULATION FINISHED!
#    Time: 10195 ns  Iteration: 0  Instance: /gray1_tb

VSIM 53>
```

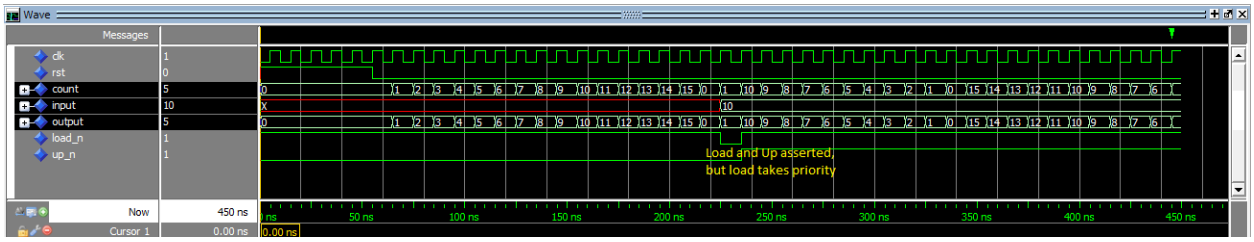


gray2

```
# vsim work.gray2_tb
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading work.gray2_tb(tb)
# Loading work.gray2(bhv)
VSIM 55> run -all
# ** Note: SIMULATION FINISHED!
#    Time: 10195 ns  Iteration: 0  Instance: /gray2_tb

VSIM 56>
```

counter

```
# vsim work.counter_tb
# Loading std.standard
# Loading ieee.std_logic_1164(body)
# Loading ieee.numeric_std(body)
# Loading work.counter_tb(tb)
# Loading work.counter(bhv)
VSIM 58> run -all
# ** Note: SIMULATION FINISHED!
#    Time: 445 ns  Iteration: 0  Instance: /counter_tb

VSIM 59>
```



top_level

The top_level entity is nothing more than an in-depth structural architecture. It creates instances of decoder7seg for each LED, and instances of clk_gen, gray2, and counter. It also defines signals and constants as necessary for internal connections. The specific connections it provides are: input 50MHz clk goes to clk_gen and is converted to the 1Hz clk, and passed as clk_gen_out. This signal is given as inputs to the clk of gray2 and counter. The output of gray2 is connected to LED3, and the output of the counter is connected to LED2, while the remaining LEDs are set to a constant 0. The three non-decoder entities all receive the same rst signal, which is the overall input rst. The counter also receives up_n and load_n from the remaining buttons (1 and 0, respectively), and receives its input signal from switches[9..6].