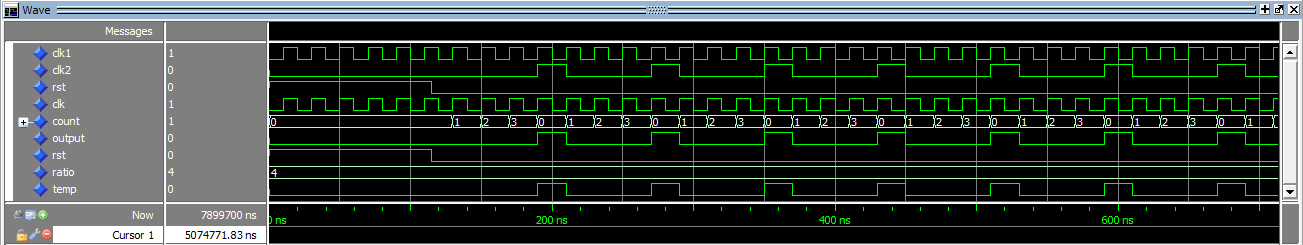
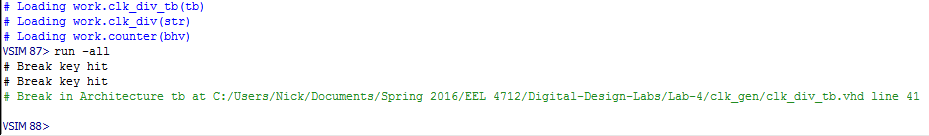
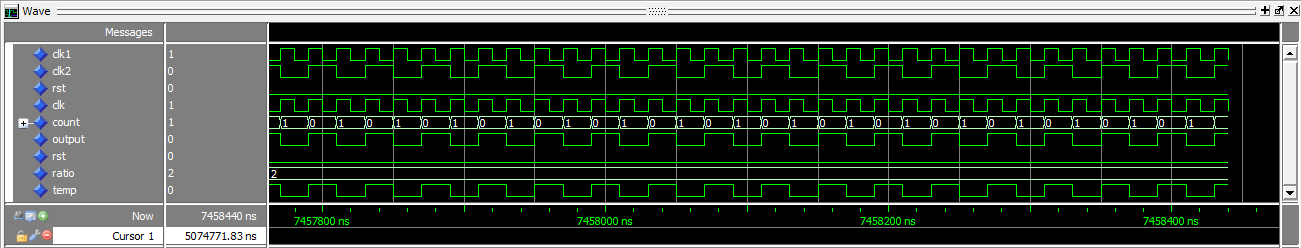
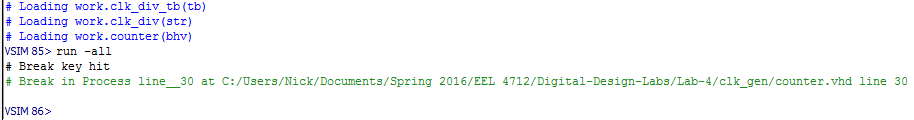
**clk\_div**

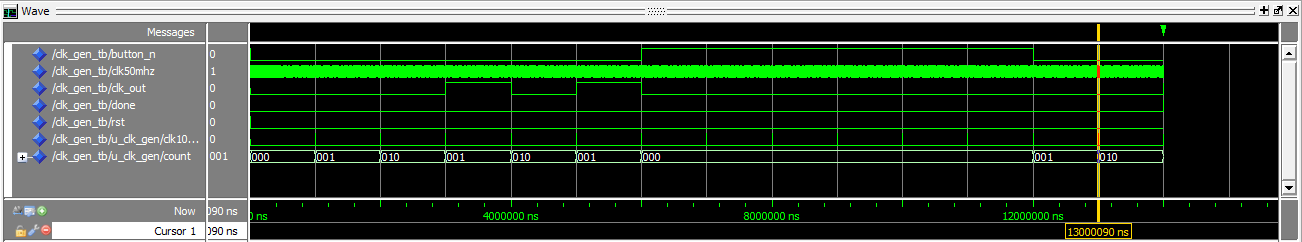
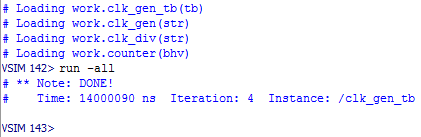
RATIO = 4



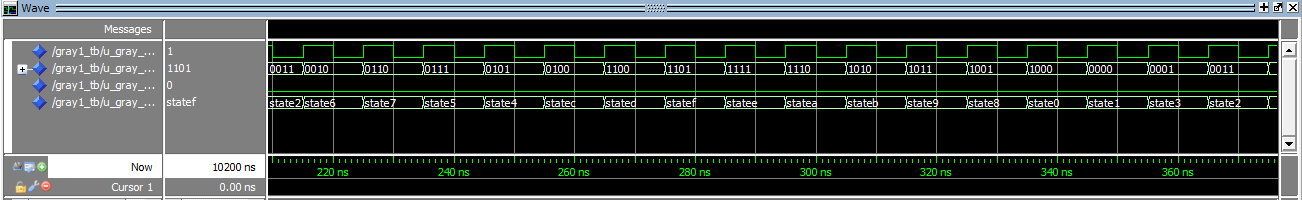
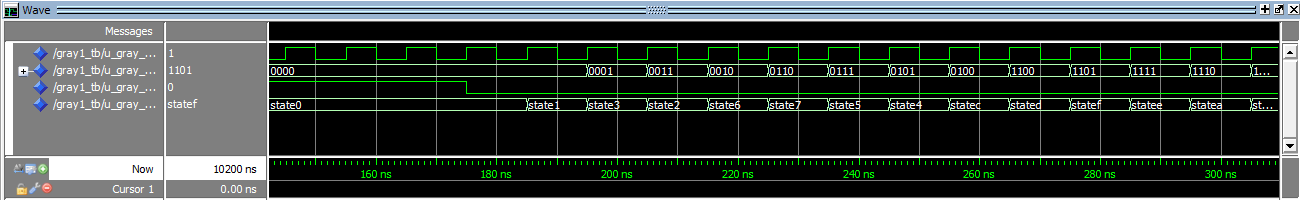
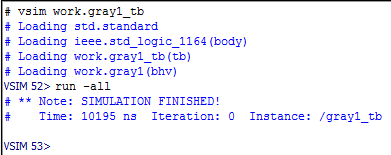
RATIO = 2



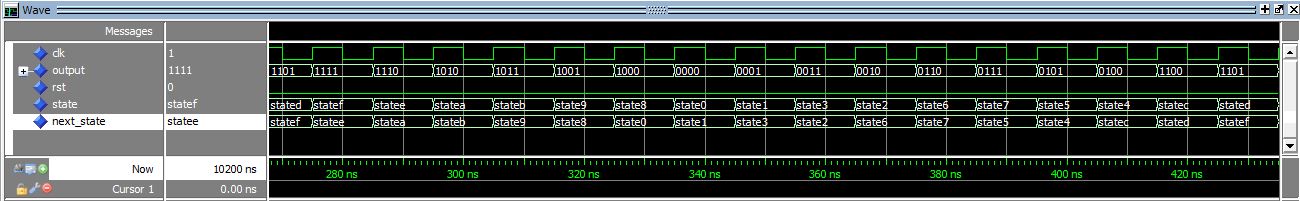
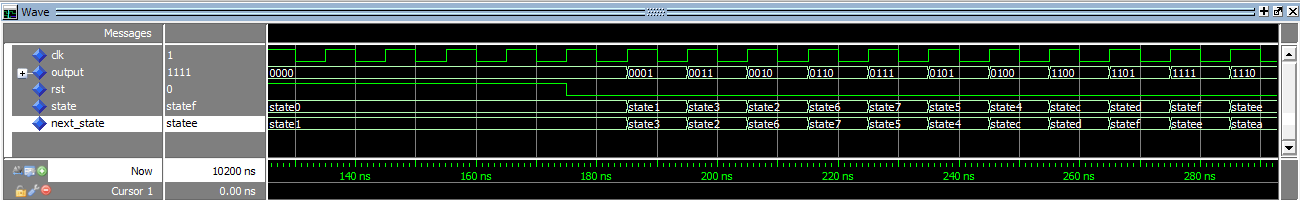
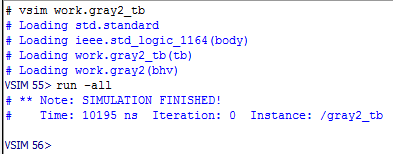
**clk\_gen**



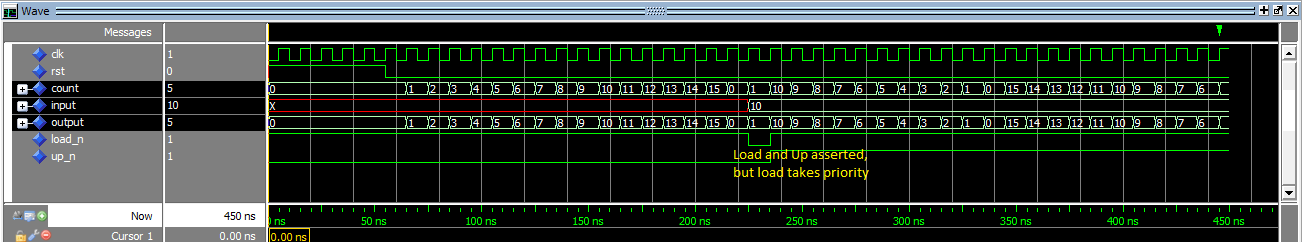
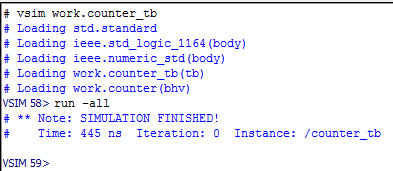
**gray1**



**gray2**



**counter**



**top\_level**

The top\_level entity is nothing more than an in-depth structural architecture. It creates instances of decoder7seg for each LED, and instances of clk\_gen, gray2, and counter. It also defines signals and constants as necessary for internal connections. The specific connections it provides are: input 50MHz clk goes to clk\_gen and is converted to the 1Hz clk, and passed as clk\_gen\_out. This signal is given as inputs to the clk of gray2 and counter. The output of gray2 is connected to LED3, and the output of the counter is connected to LED2, while the remaining LEDs are set to a constant 0. The three non-decoder entities all receive the same rst signal, which is the overall input rst. The counter also receives up\_n and load\_n from the remaining buttons (1 and 0, respectively), and receives its input signal from switches[9..6].