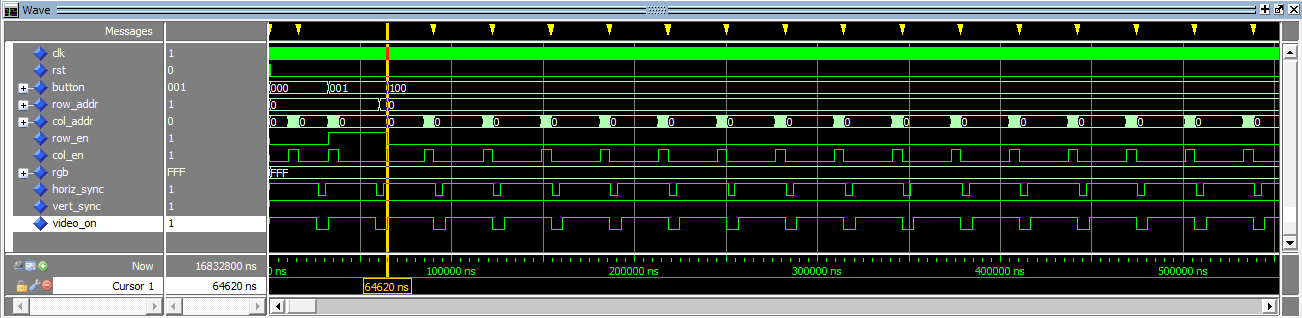
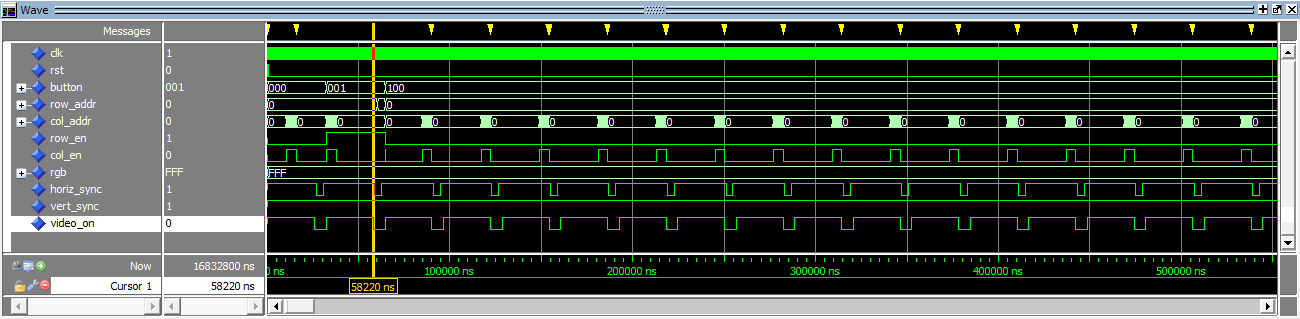
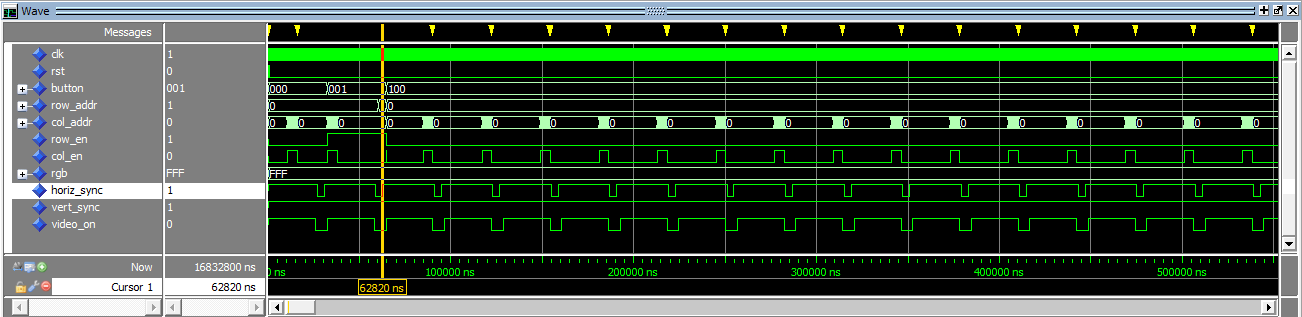
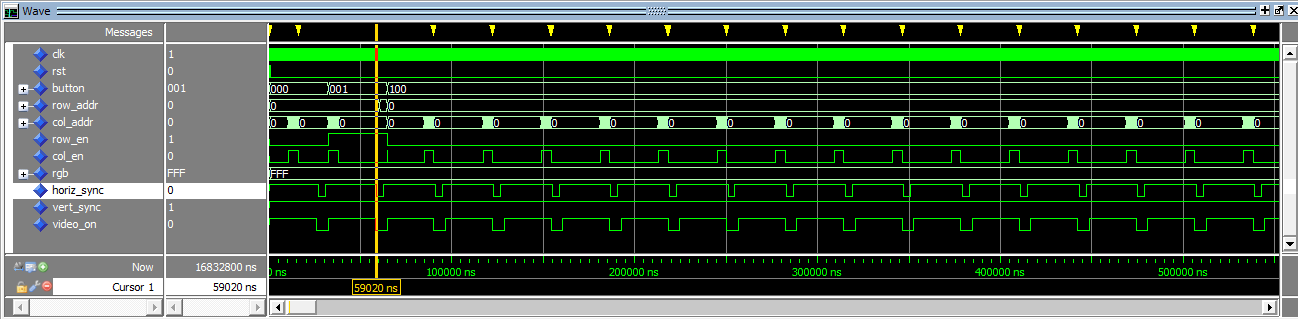
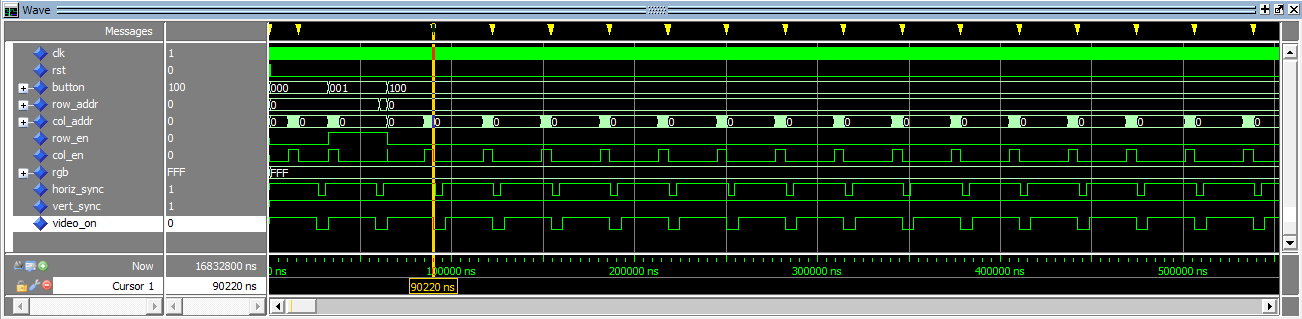
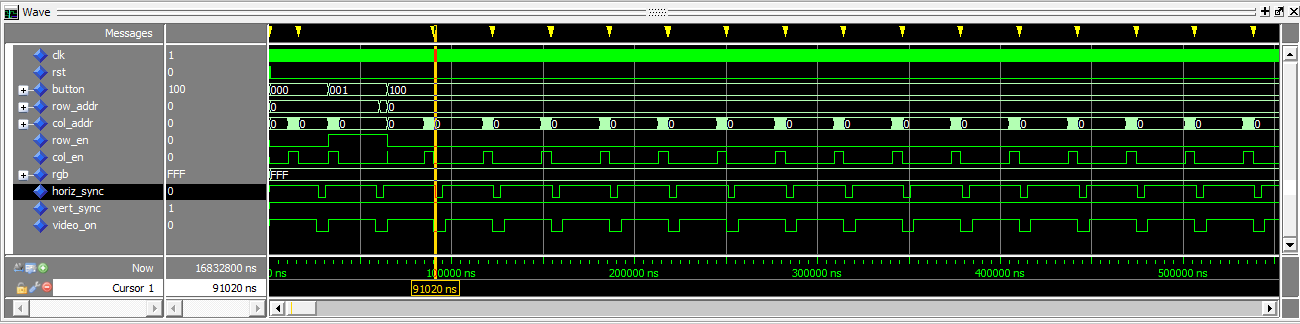
**Decoders & ROM**

Note: The yellow marks refer to a warning about the vector being truncated, but this is not an issue. Since the counts (10-bit vectors) are used by the row and column decoders, which produce 6-7-bit vectors, the warning is present, but this is a necessary truncation for forming the ROM address.



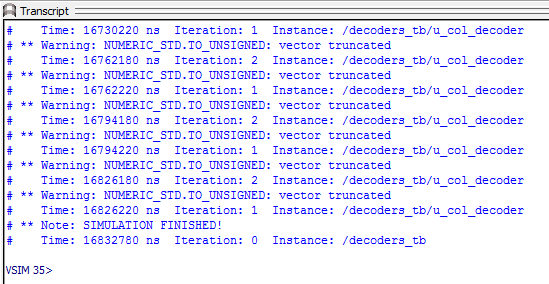


Note: Horiz\_Sync width = 62820-59020 = 3800ns ≈ 3.77μs

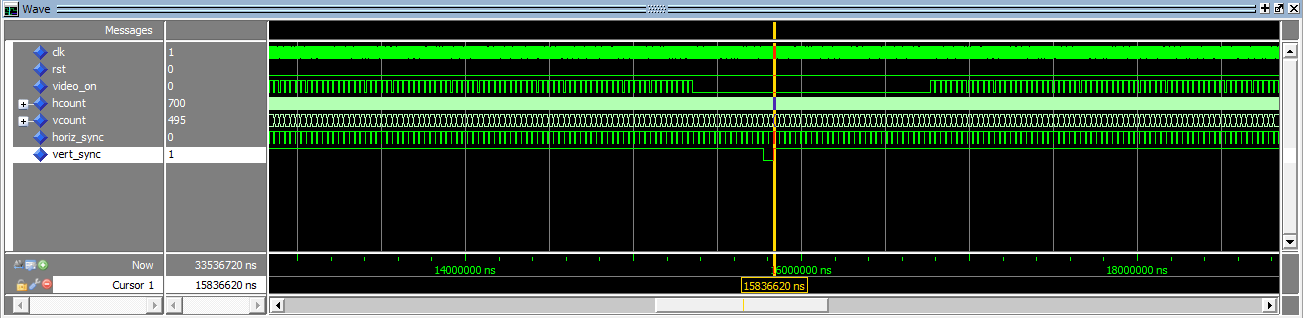
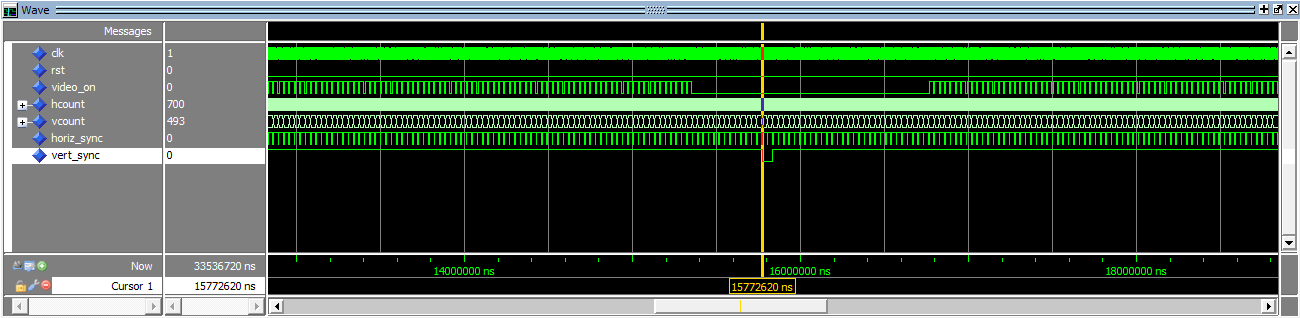
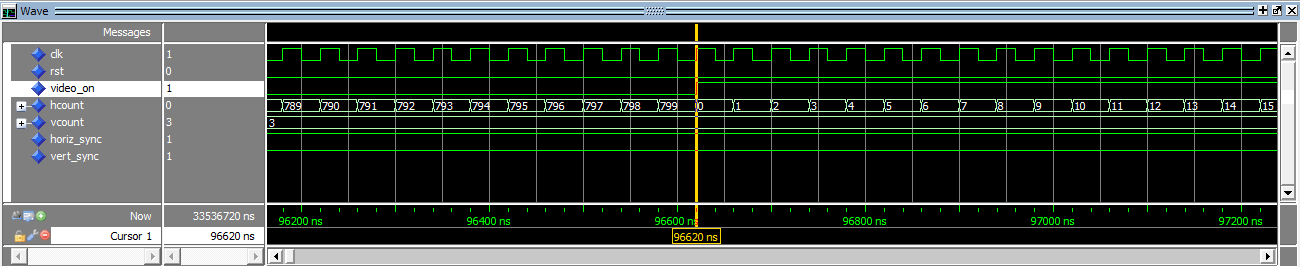
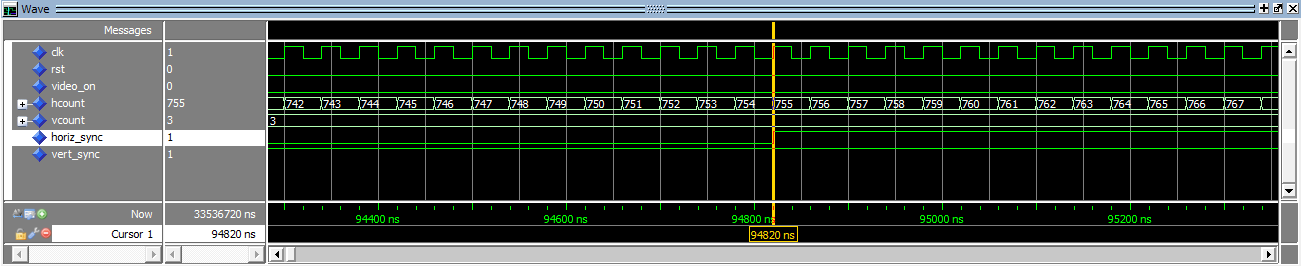
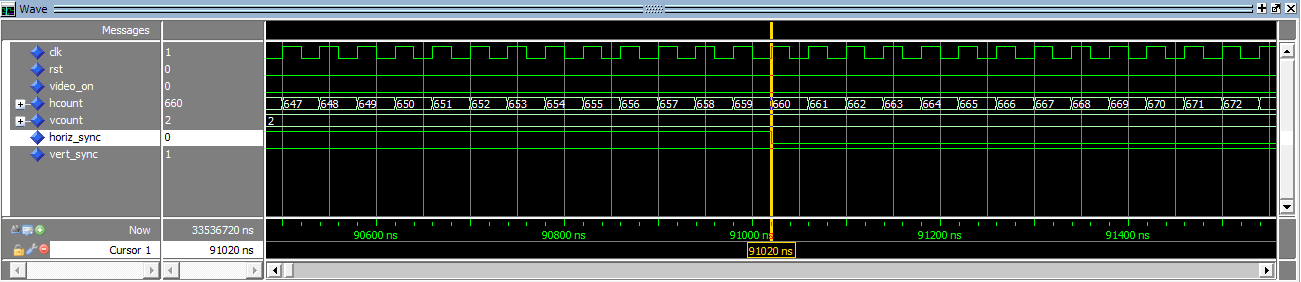
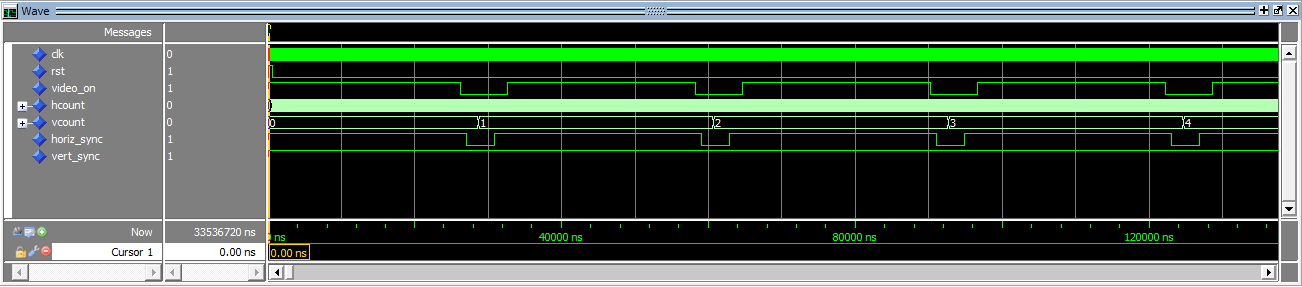


Note: Time between Horiz\_Sync’s = 91020-59020 = 32000 ≈ 31.77μs

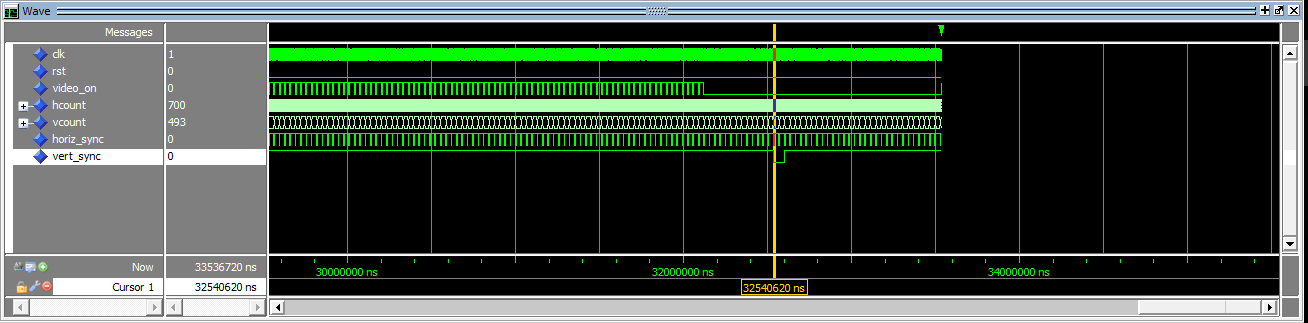
Note: The full simulation log is not show simply because of the length of the simulation and the warnings throughout.



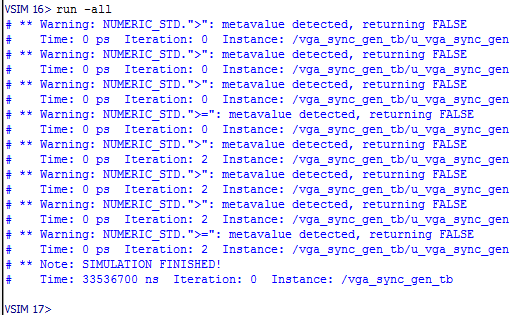
**VGA\_sync\_gen**



Note: Vert\_Sync width = 15836620-15772620 = 64000ns



Note: Time between Vert\_Sync’s = 32540620-15772620 = 16768000ns ≈ 16.6ms



**top\_level**

Note: Yellow tick marks serve the same purpose here as the with the decoders.

