

Station Test Card

REV	DATE	PAGES	DESCRIPTION
A1	APR.2017	All	INITIAL REVISION A RELEASE
A2	JUN.2017	PAGE 5 6 7	REVISION B RELEASE

Title			Station Test Card		
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B	HS-Station-Test-B				B
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10M08SAE144 TOP VIEW

Top View
Wire Bond

MAX 10

10M08SCE144C8G

IOBANK_1A
(0 assigned/8 assignable)

IOBANK_1B
(0 assigned/10 assignable)

IOBANK_2
(0 assigned/7 assignable)

IOBANK_3
(0 assigned/18 assignable)

IOBANK_4
(0 assigned/7 assignable)

IOBANK_8
(0 assigned/17 assignable)

IOBANK_7
(0 assigned/7 assignable)

IOBANK_6
(0 assigned/15 assignable)

IOBANK_5
(0 assigned/12 assignable)

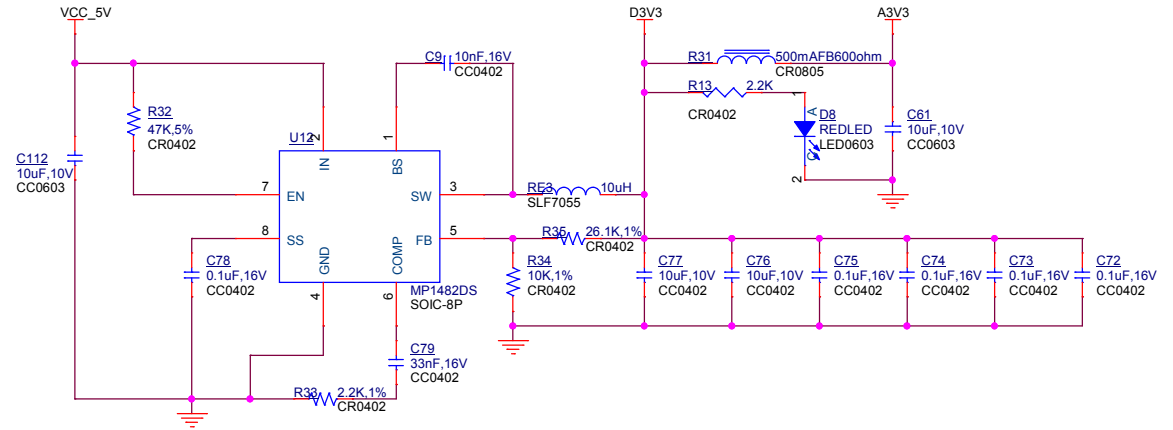
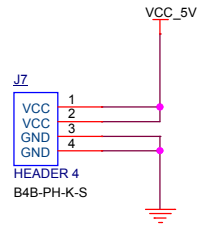
- TDI
- TCK
- TMS
- TDO
- VREF
- VCCP/VCCR/V...
- VCCA
- VCCIO
- GND

- User I/O
- User assigned I...
- Fitter assigned I...
- Unbonded pad
- Reserved pin
- Other configura...
- DEV_OE
- DEV_CLR
- DIFF_n
- DIFF_p
- CLK_n
- CLK_p
- Other PLL
- Other dual purp...

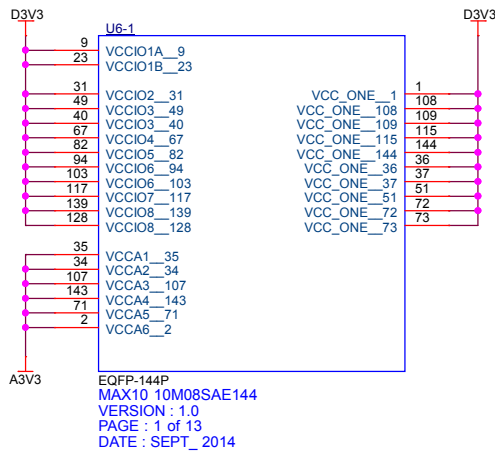
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Power

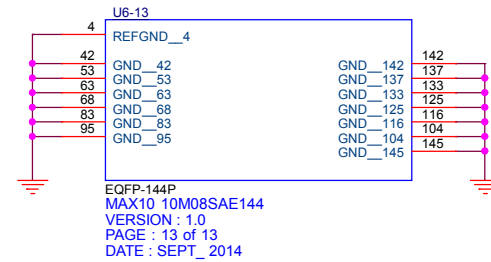
+3.3 V 2A Power



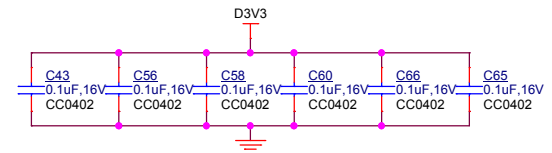
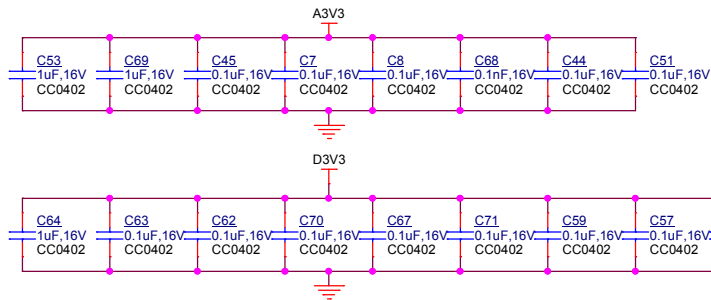
FPGA Power



FPGA GND

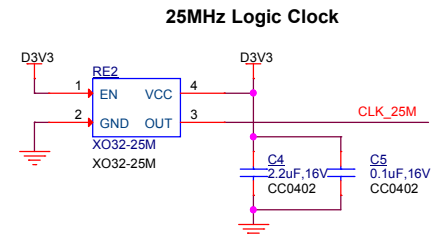
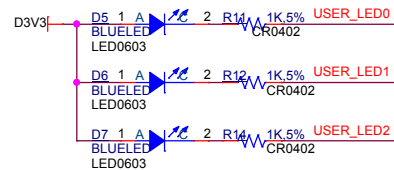
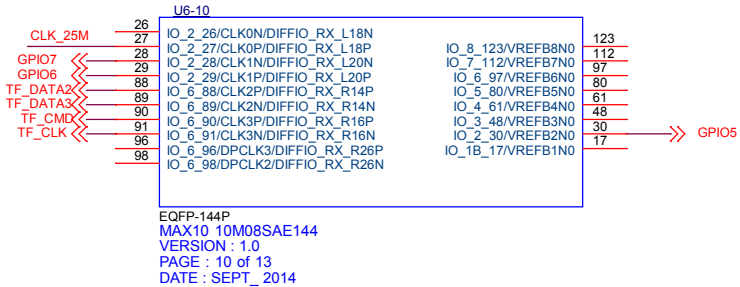
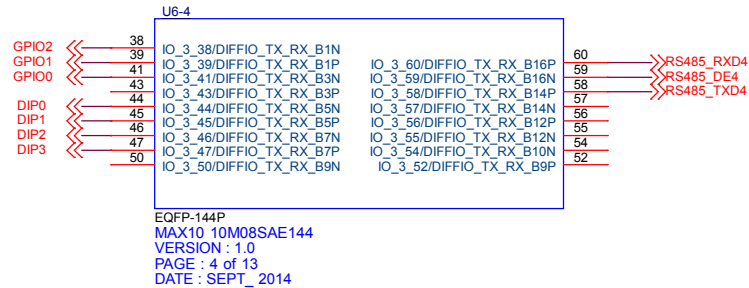
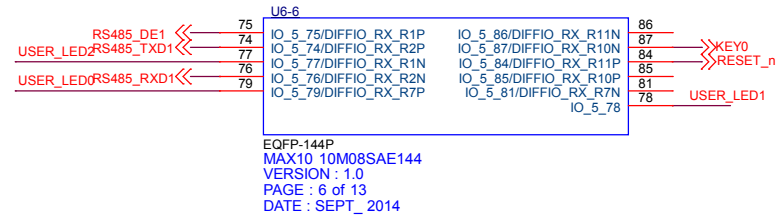
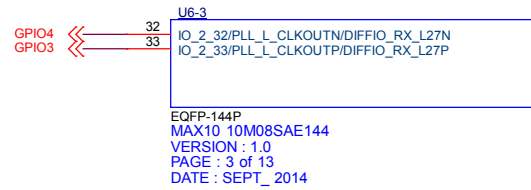
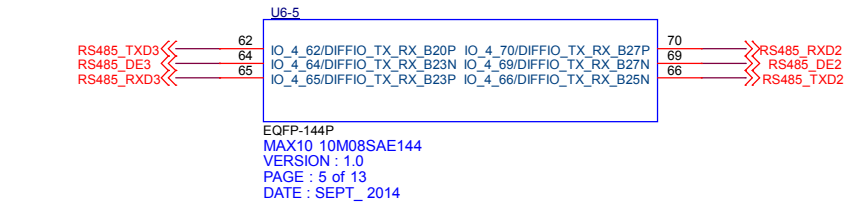
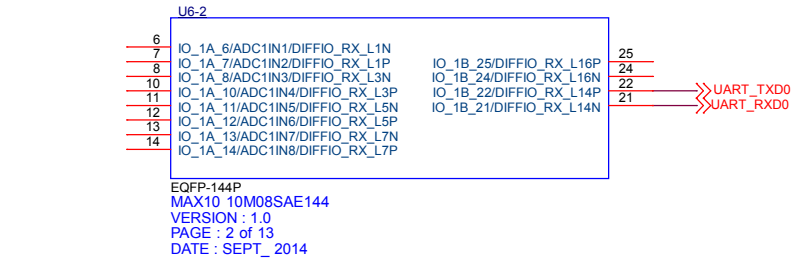


Place CAP Near FPGA



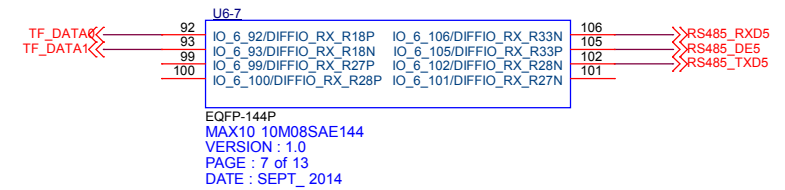
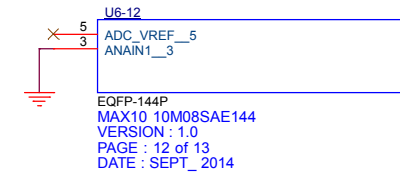
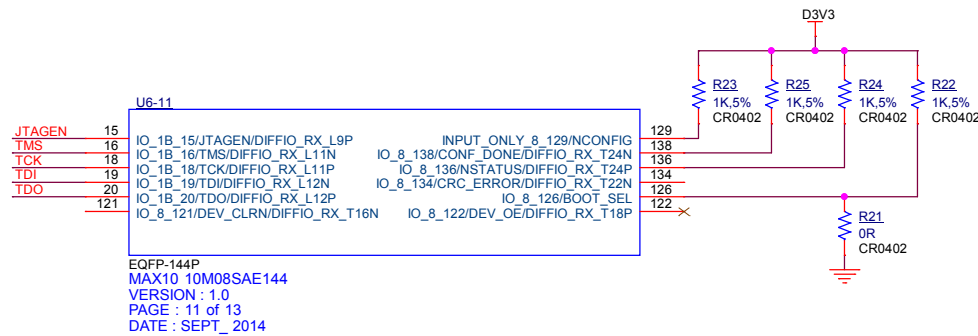
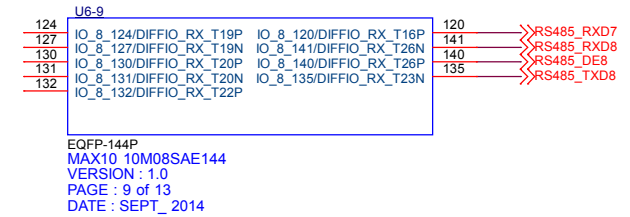
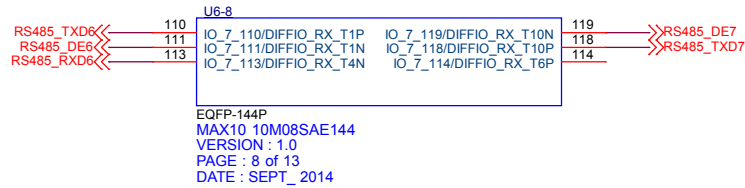
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FPGA BANK IO - PAGE1

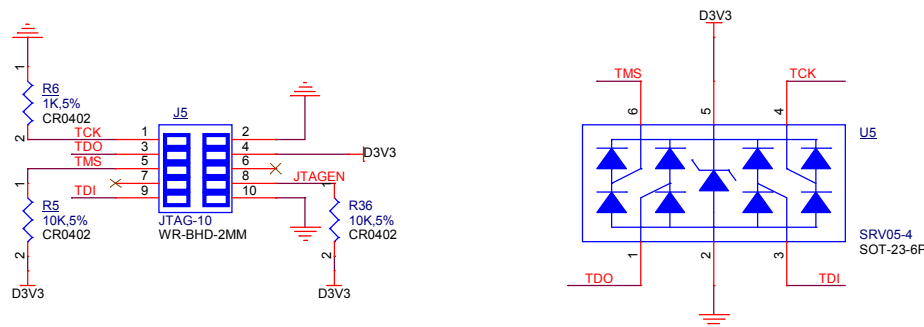


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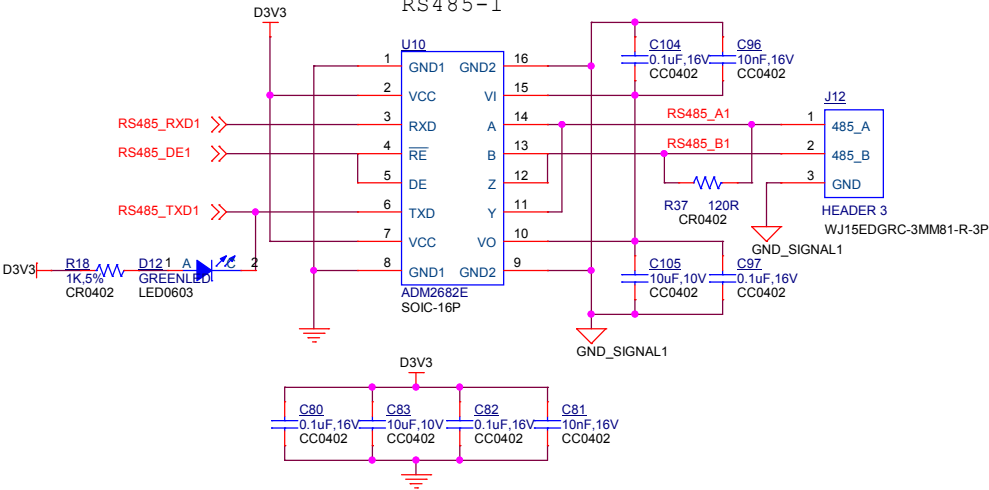
FPGA JATG



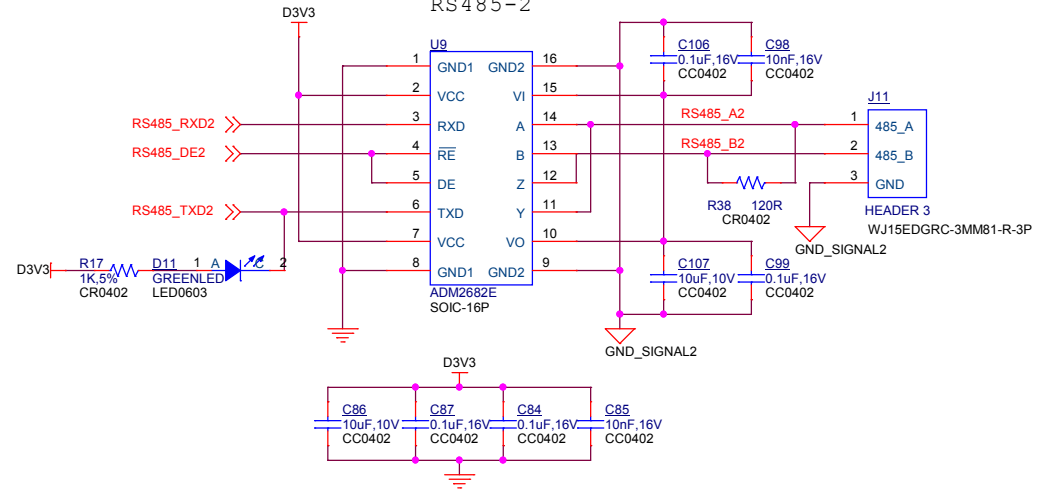
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RS485 - PAGE1

RS485-1

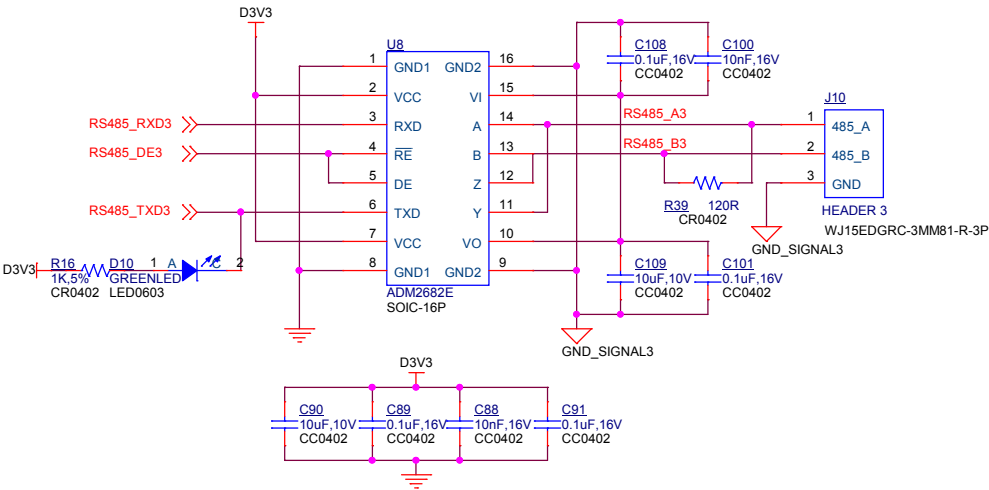


RS485-2

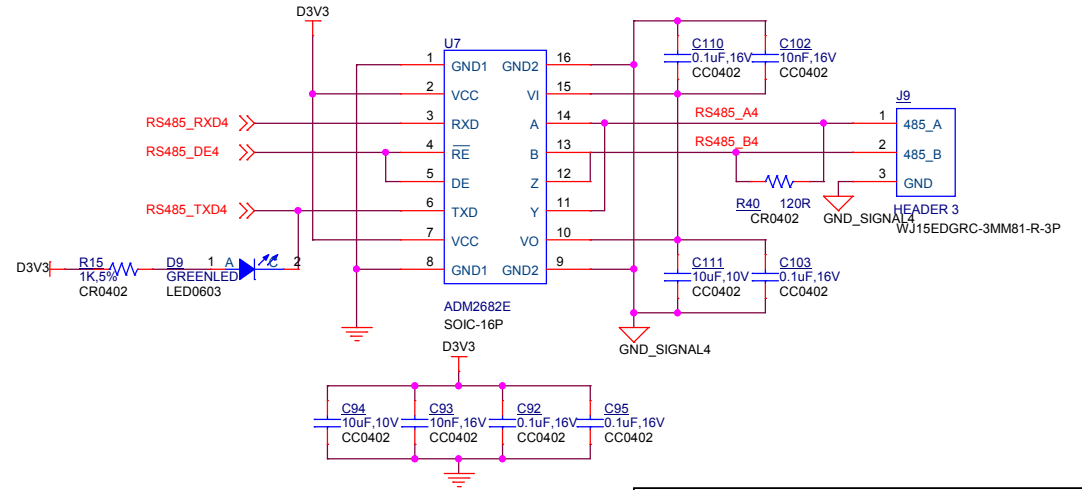


For All 485 Module: Place these CAPs
between pins 1,8 and 2,7 of chips

RS485-3



RS485-4



Title **Station Test Card**

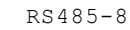
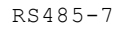
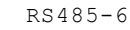
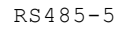
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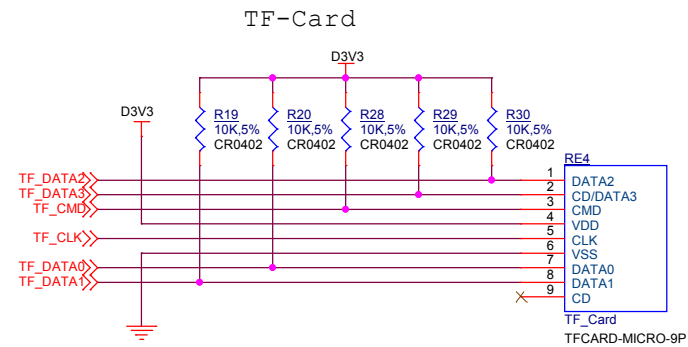
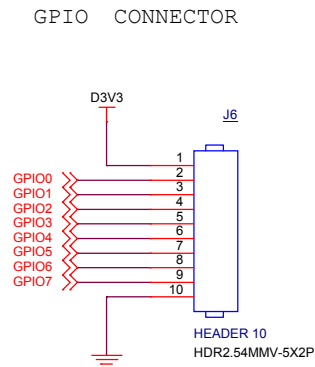
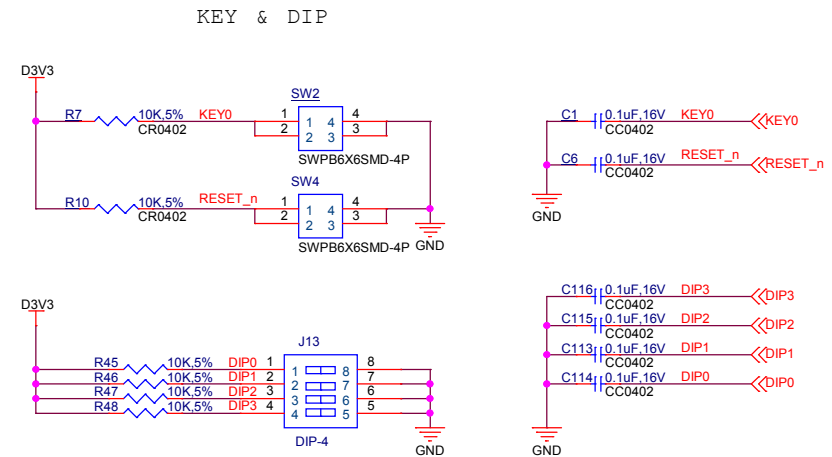
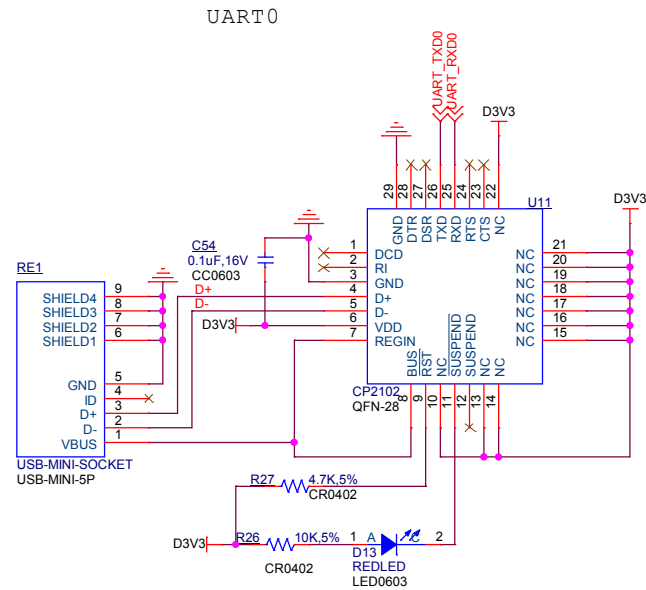
Rev B

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Peripherals



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