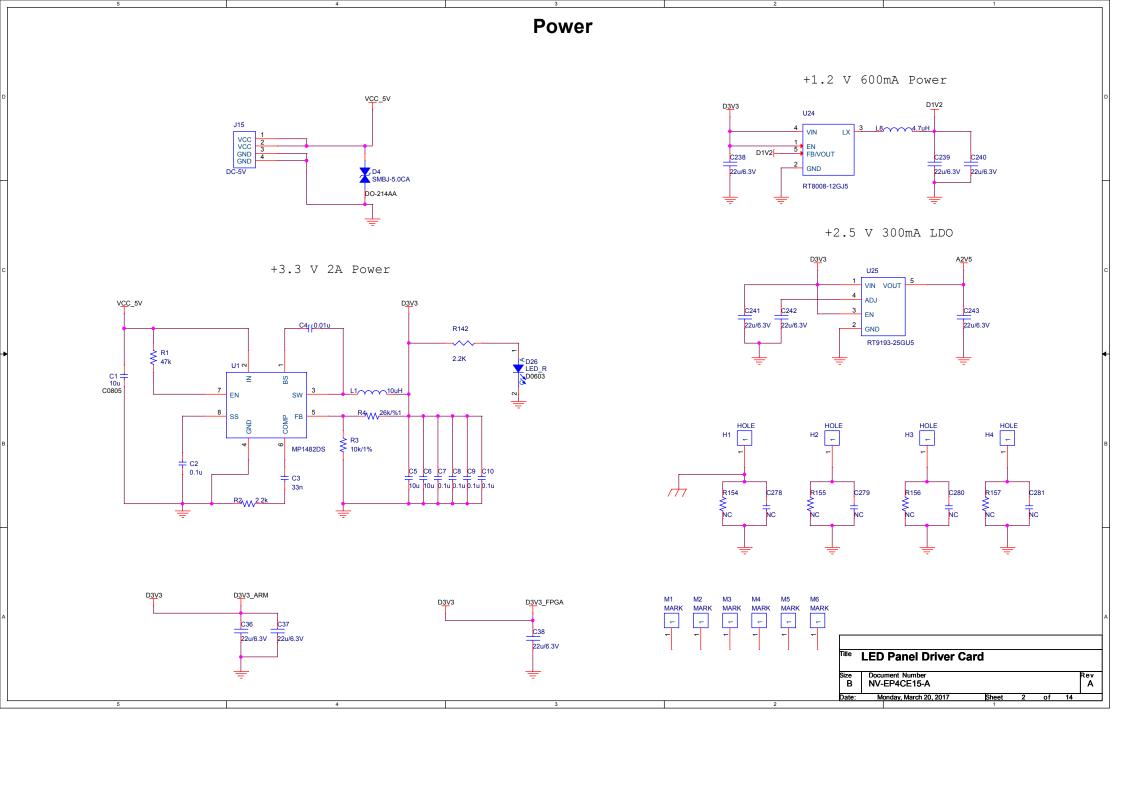
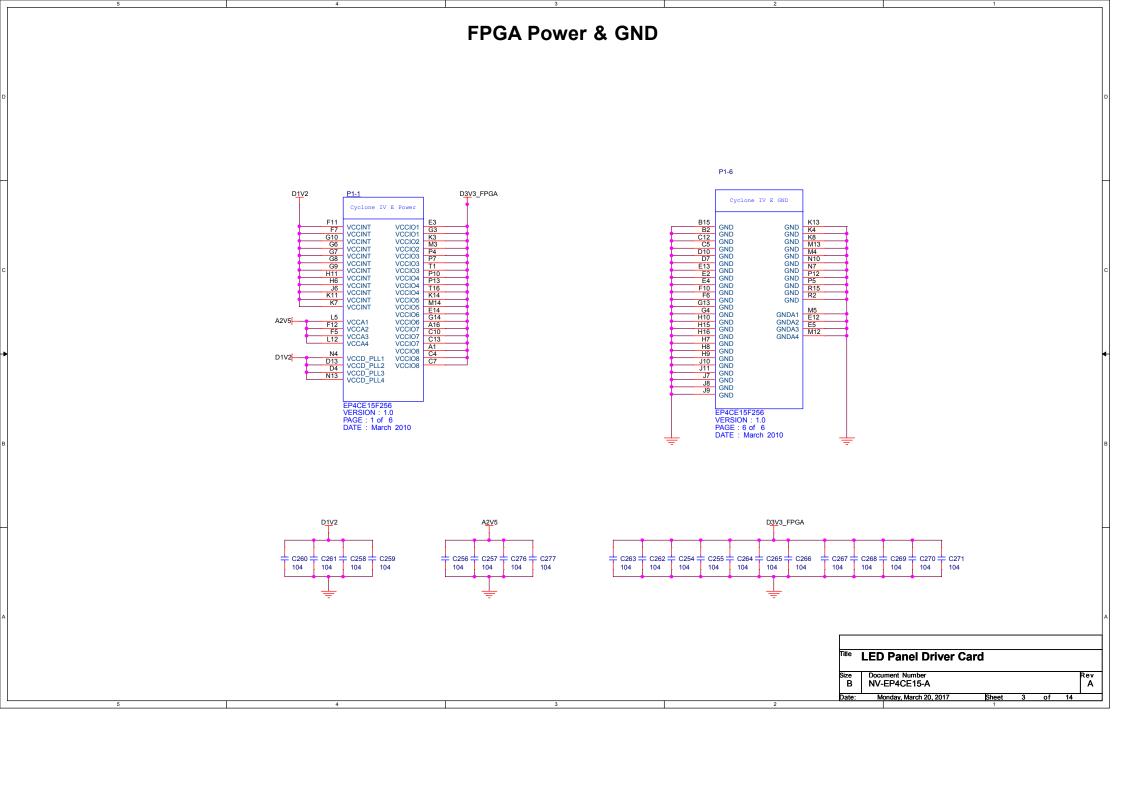
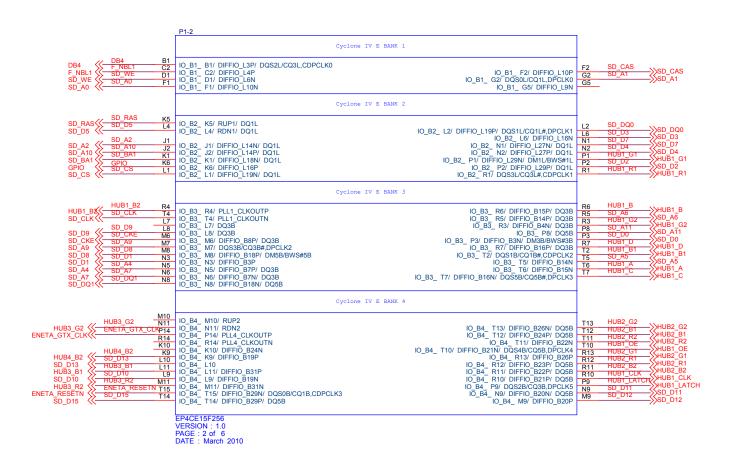
5	LED Panel Driver Card (Ethen	3 ACT NC)			2	1	
	LED Panel Driver Card (Etnen	iet NC)	REV	DATE	PAGES	DESCRIPTION	
			A1	MAR,2017	All	INITIAL REVISION A RELEASE	
			A2	FEB,2016	08 10 11	DELETE COMPONENT RELATED WITH ETHENET	
D							D
_							H
			,				
С							С
•							•
В							В
_							Н
Δ							
						Title LED Panel Driver Card	
						Size Document Number Rev B NV-EP4CE15-A A	7
	,					Date: Wednesday, April 19, 2017 Sheet 1 of 14	$\exists \mid$
5	4	3			2		





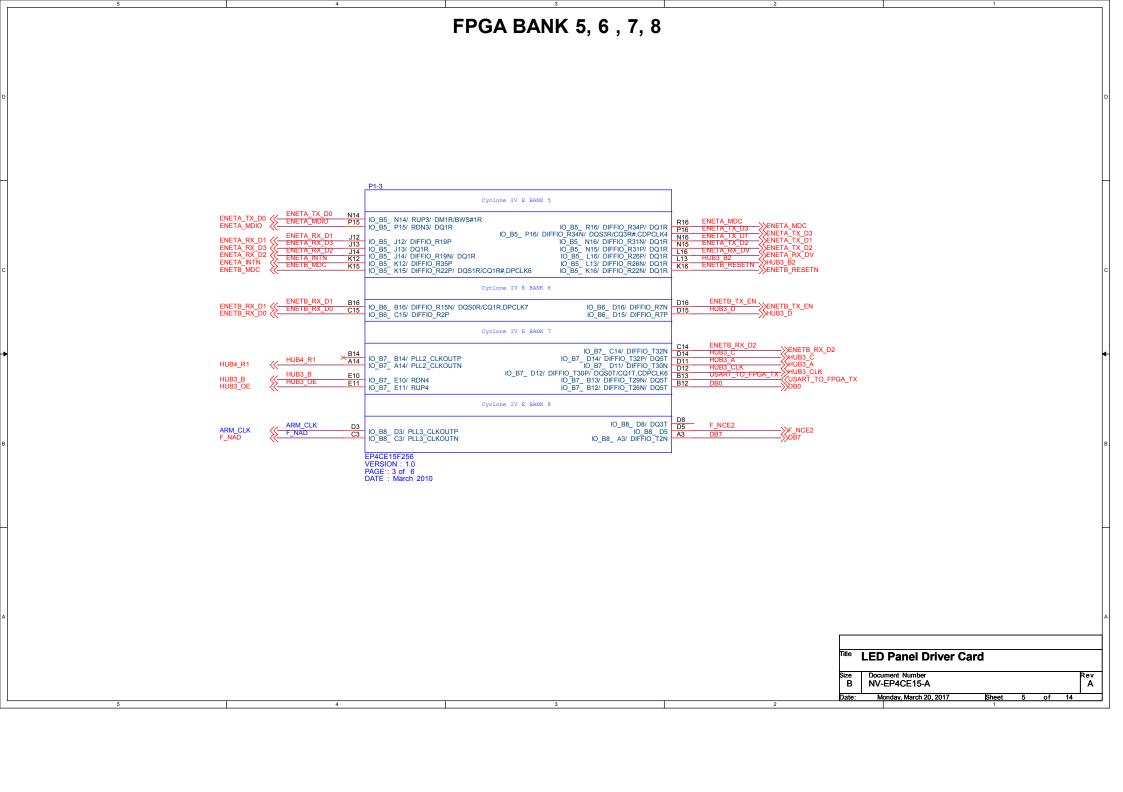
FPGA BANK 1, 2, 3, 4

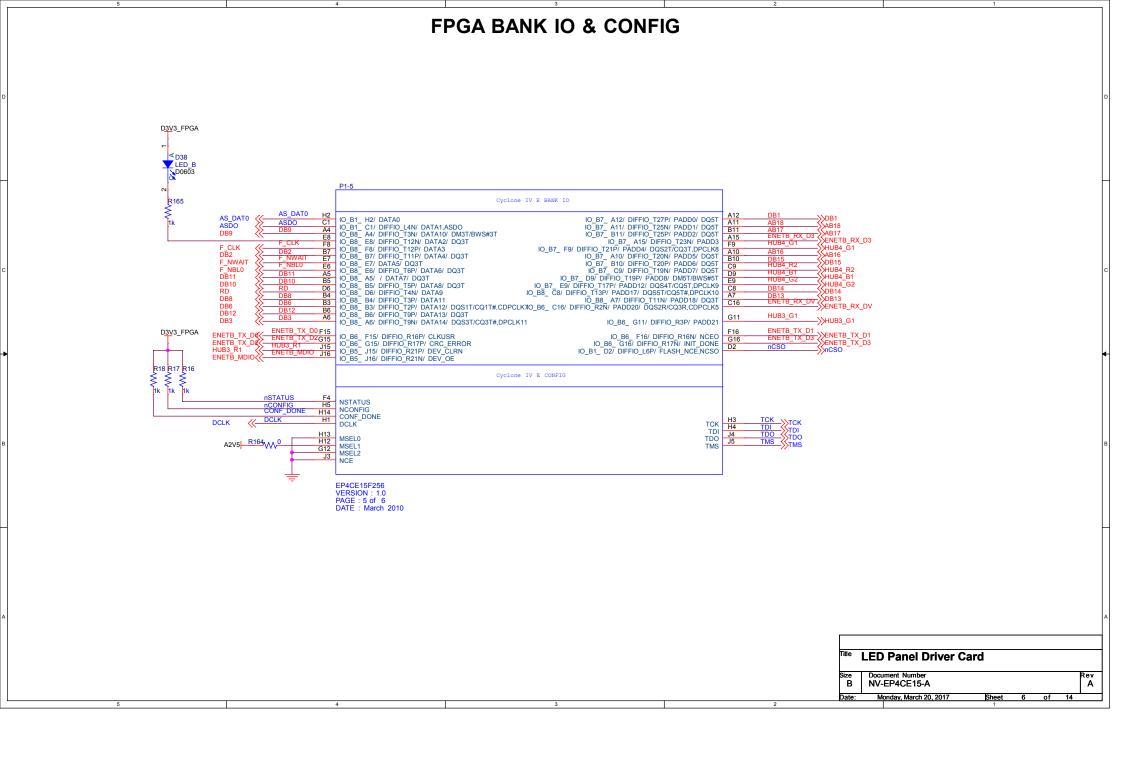


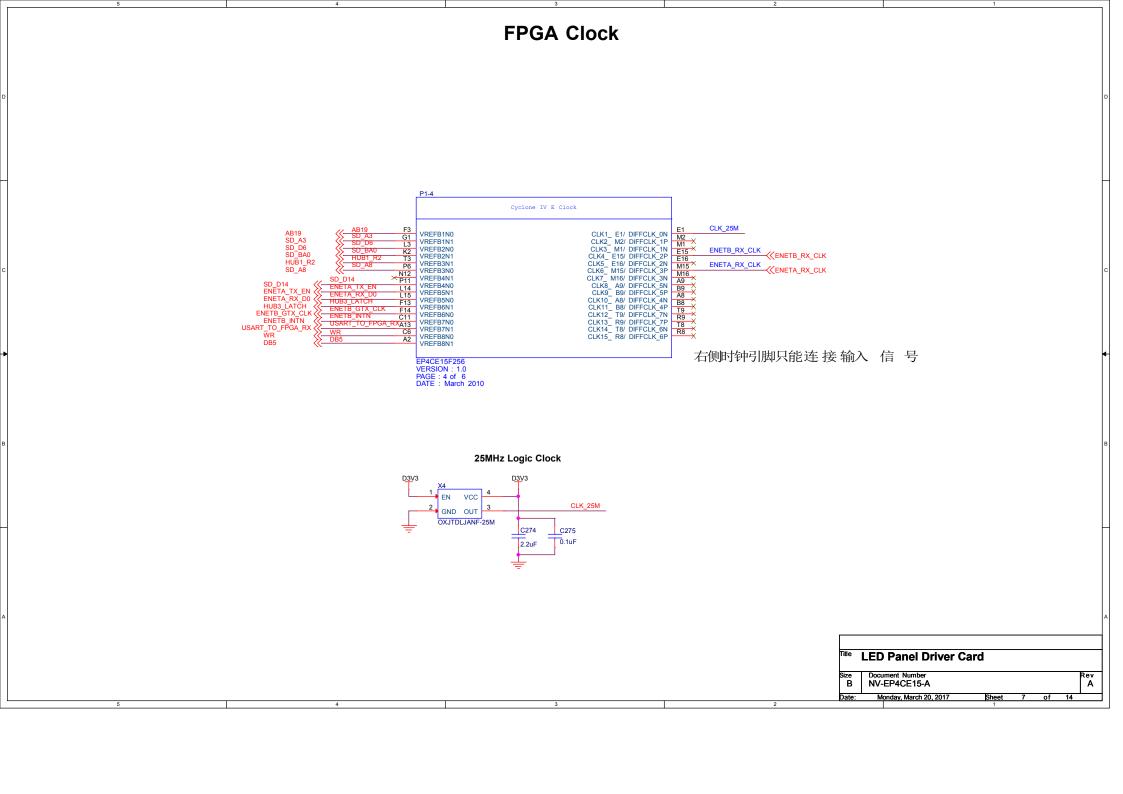
Title LED Panel Driver Card

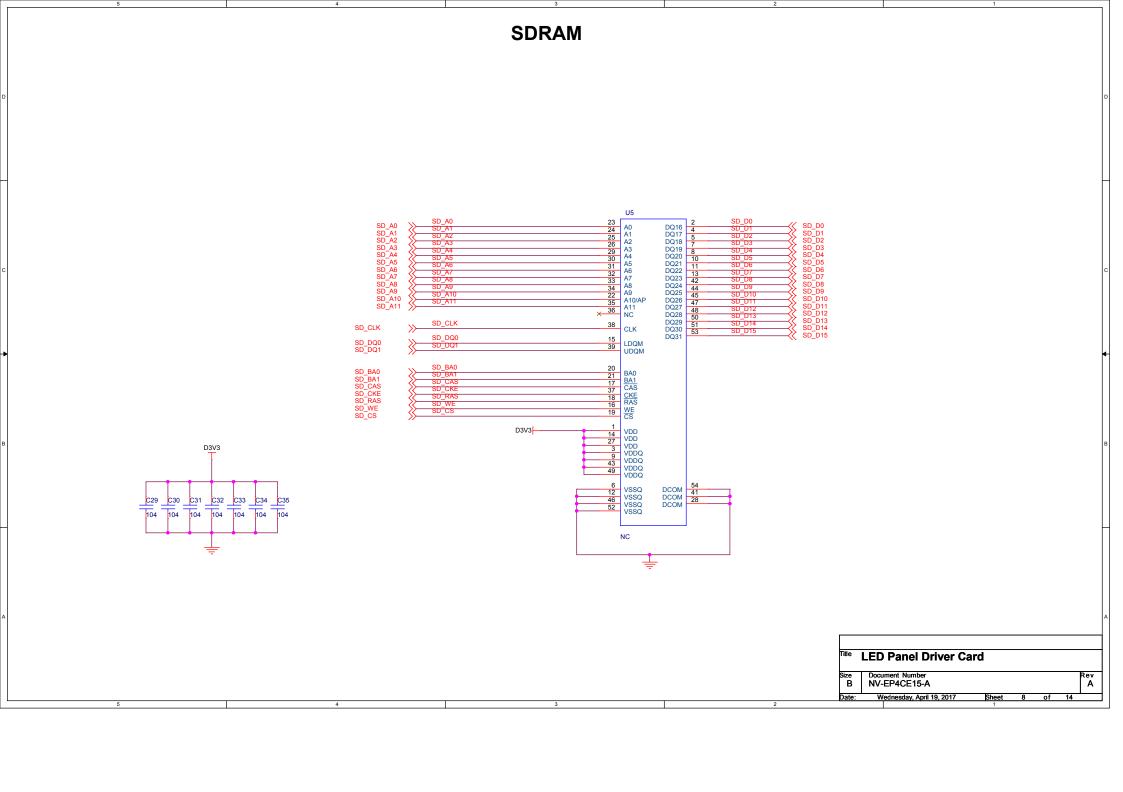
Size Document Number Rev A
Date: Monday, March 20, 2017 Sheet 4 of 14

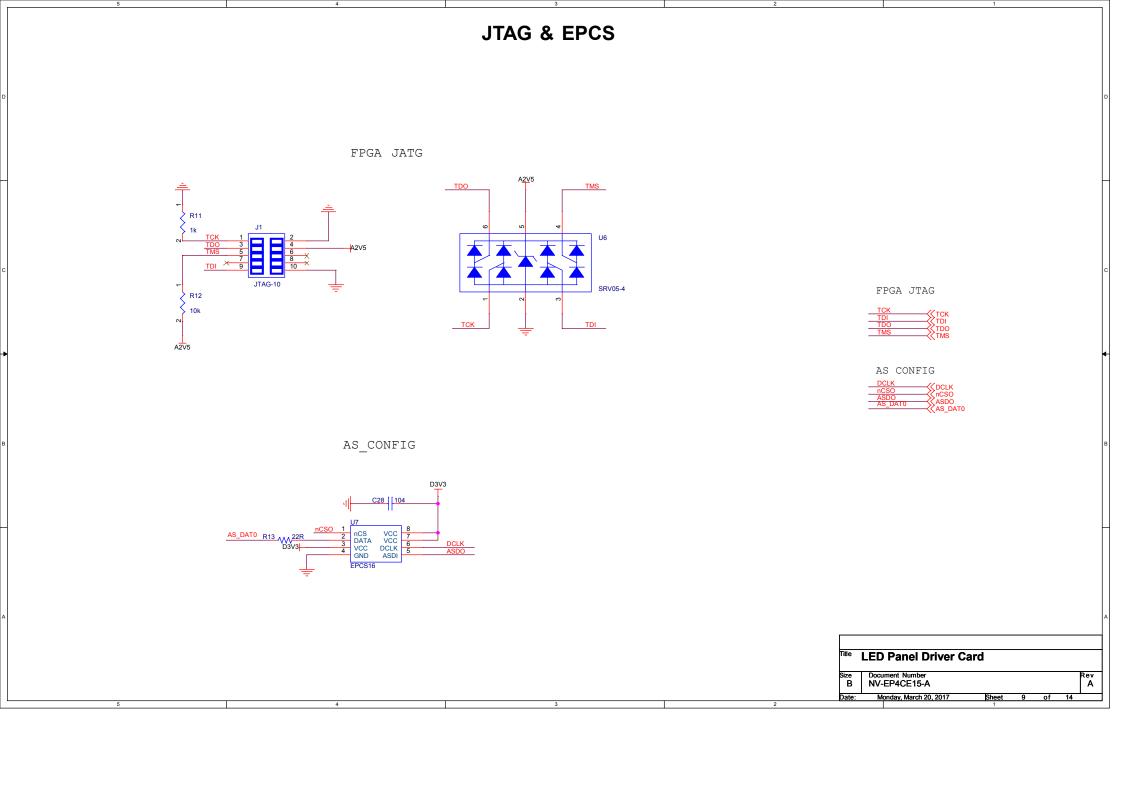
5 4 3

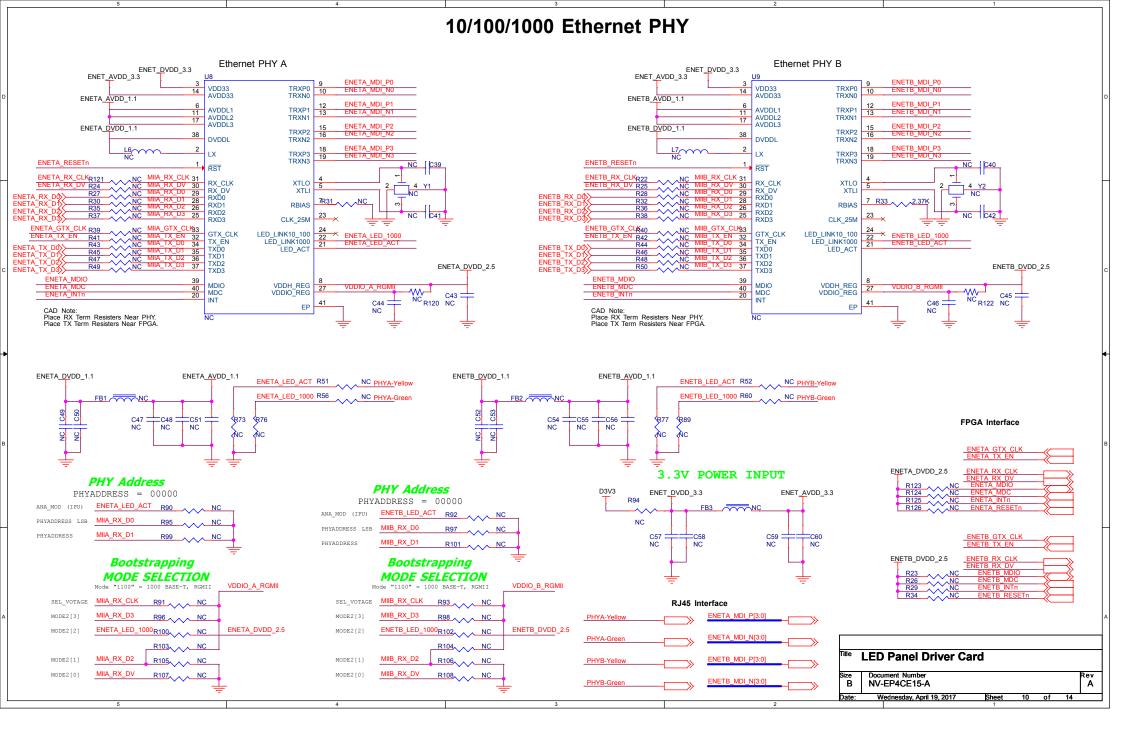


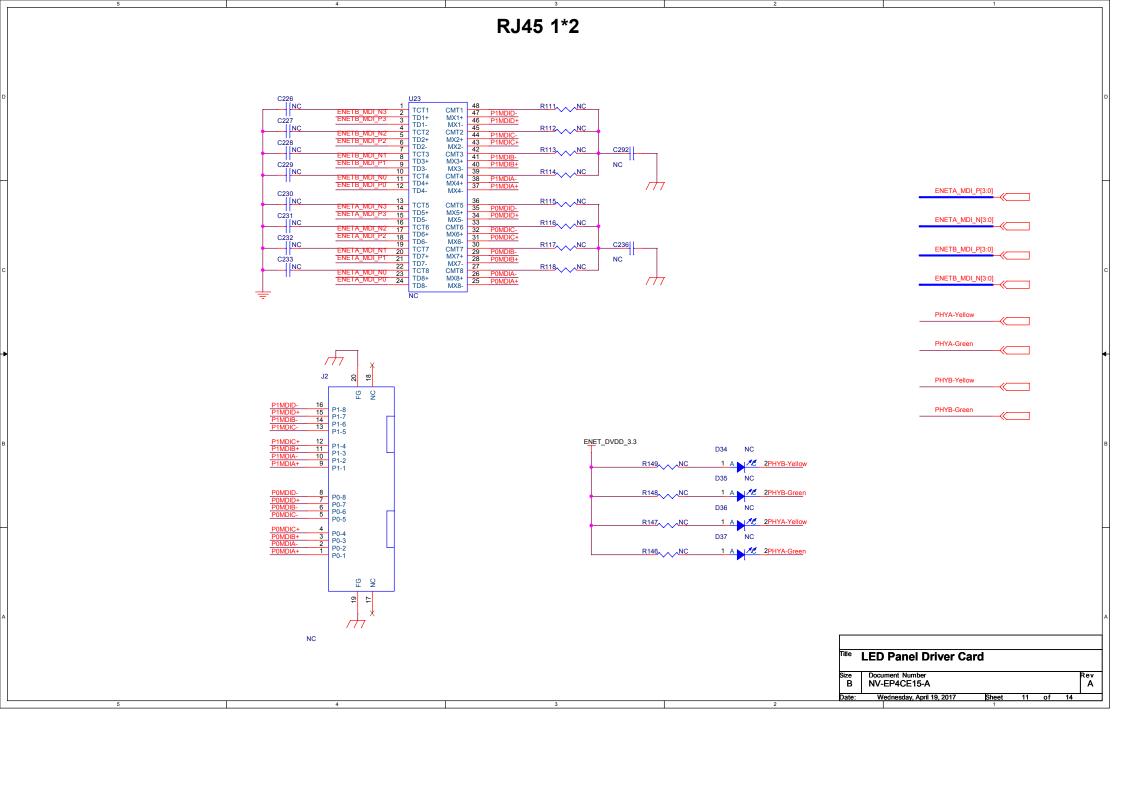


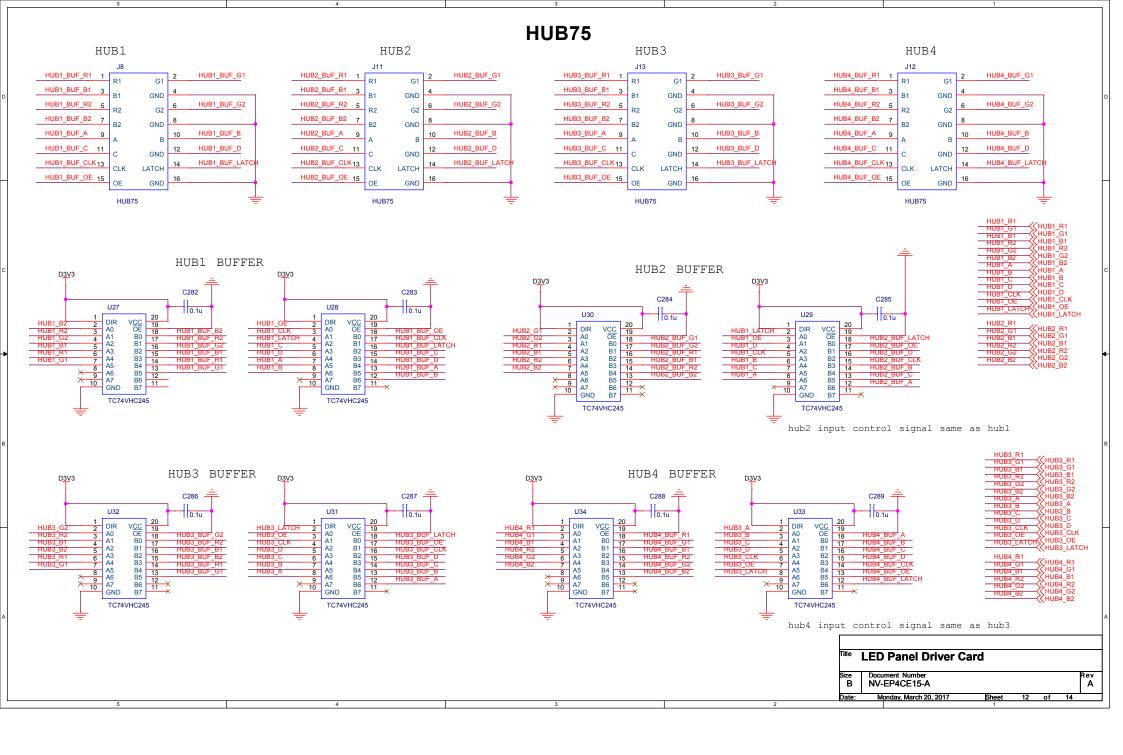












STM32 D3V3_ARM D3V3_ARM 23 PA0-WKUP/USART2_CTS/ADC12_IN0/TIM2_CH1_E* USART_TX* 26 PA1/USART2_RTS/ADC12_IN1/TIM2_CH2 USART_RX* 26 PA2/USART2_TX/ADC12_IN2/TIM2_CH3 29 A3/USART2_RX/ADC12_IN3/TIM2_CH4 29 PA4/SPI1_NSS/USART2_CK/ADC12_IN4 21 PA6/SPI1_SCK/ADC12_IN5/TIM3_CH1/TIM1_BKIN 22 PA6/SPI1_MOS/ADC12_IN0/TIM3_CH2/TIM1_CH1N 25 PA6/USART1_CK/TIM1_CH1/MCC0 D3V3_ARM PA0-WKUP/USART2_CTS/ADC12_IN0/TIM2_CH1_ETR VBAT C245 C246 C247 C244 VDD 1 VDD 2 100 C0402 C0402 L10 C0402 C0402 C0402 C0402 VDD_3 100uH VDD_4 L0805 VDD_5 68 PA9/USART1_CK/TIM1_CH1/MCO PA9/USART1_TX/TIM1_CH2 VDDA **植村** 每 个0.11吨 容分别 靠 近 USART_TO_FPGA_TX\\ USART_TO_FPGA_RX\\ CAN_RX PAGUSARTI_TX/IIMT_UF12 PA10/USARTI_RX/IIMT_UF12 PA10/USARTI_RX/IIMT_CH3 PA12/USARTI_RX/CANTX/IIMT_CH4/USBDM PA12/USARTI_RTS/CANTX/TIMT_ETR/USBDP C251 C252 VDD 1/2/3/4/5与SS 1/2/3/4/5 **外**独4**x**应靠近DD_3 与 VS S_ 3 VRFF 10nF PC6/TIM3_CH1 PC8/TIM8_CH3/SDIO_D0 PC9/TIM8_CH4/SDIO_D1 PC10/USART4_TX/SDIO_D3 PC11/USART4_RX/SDIO_D3 PC11/USART4_R VREF-C0402 C0402 PA13/JTMS/SWDIO PA13/JTMS/SVCLK PA15/JTDI/TIM2_CH1_ETR/SPI1_NSS 35 PB0/ADC12_IN8/TIM3_CH3/TIM1_CH2N 36 PB1/ADC12_IN9/TIM3_CH4/TIM1_CH3N PB2/BOOT1 PC11/USART4_RX/SDI0_D3 PC12/USART5_TX/SDI0_CK PC13-TAMPER-RTC D3V3_ARM R0402 89 PB2/B0OT1 PB3/JTD0/TRACESW0/TIM2_CH2/SPI1_SCK PB3/JTD0/I RACESWO/JINZ_CH2/SPI_SCK PB4/JNTRST/TIM3_CH1/SPI_MISO PB5/I2C1_SMBAU_TIM3_CH2/SPII_MOSI PB6/I2C1_SCL/TIM4_CH1/USART1_TX PB7/I2C1_SDA/TIM4_CH2/USART1_RX/FSMC_NAD TF_CMD >>>TF_CMD × 92 CONNECT TO FPGA | Section | Sect PD5/USART2_TX/FSMC_NWE 87 LED_R LED_R D0603 D0603 | 87 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | 975 | D0603 DB1 DB2 DB3 DB4 F R128 R127 DB5 × 53 PB14/SPI2_MISO/USART3_RTS/TIM1_CH2N PB15/SPI2_MOSI/TIM1_CH3N S DB6 R0402 R0402 PD13/TIM4_CH2/FSMC_A18 61 DB7 DB8 GPIO Μ 15 16 17 PC1/ADC12_IN11 PC2/ADC12_IN12 PD14/TIM4_CH3/FSMC_D0 62 DB9 PD15/TIM4_CH4/FSMC_D1 С DB10 18 PC2/ADC12_IN12 PC3/ADC12_IN13 PE0/TIM4_ETR/FSMC_NBL0 97 **DB11** PE1/FSMC_NBL1 PE2/TRACECK/FSMC_A23 PE3/TRACED0/FSMC_A19 3 DB12 33 PC4/ADC12_IN14 PC5/ADC12_IN15 DB13 DB14 ARM_CLK 12 PE4/TRACED1/FSMC A20 **DR15** OSC IN AB16 PE5/TRACED2/FSMC_A21

