

Station Test Card

REV	DATE	PAGES	DESCRIPTION
A1	APR.2017	All	INITIAL REVISION A RELEASE
A2	JUN.2017	PAGE 5 6 7	REVISION B RELEASE

Title

Station Test Card

Size

B

Document Number

HS-Station-Test-B

Rev

B

Date:

Monday, June 19, 2017

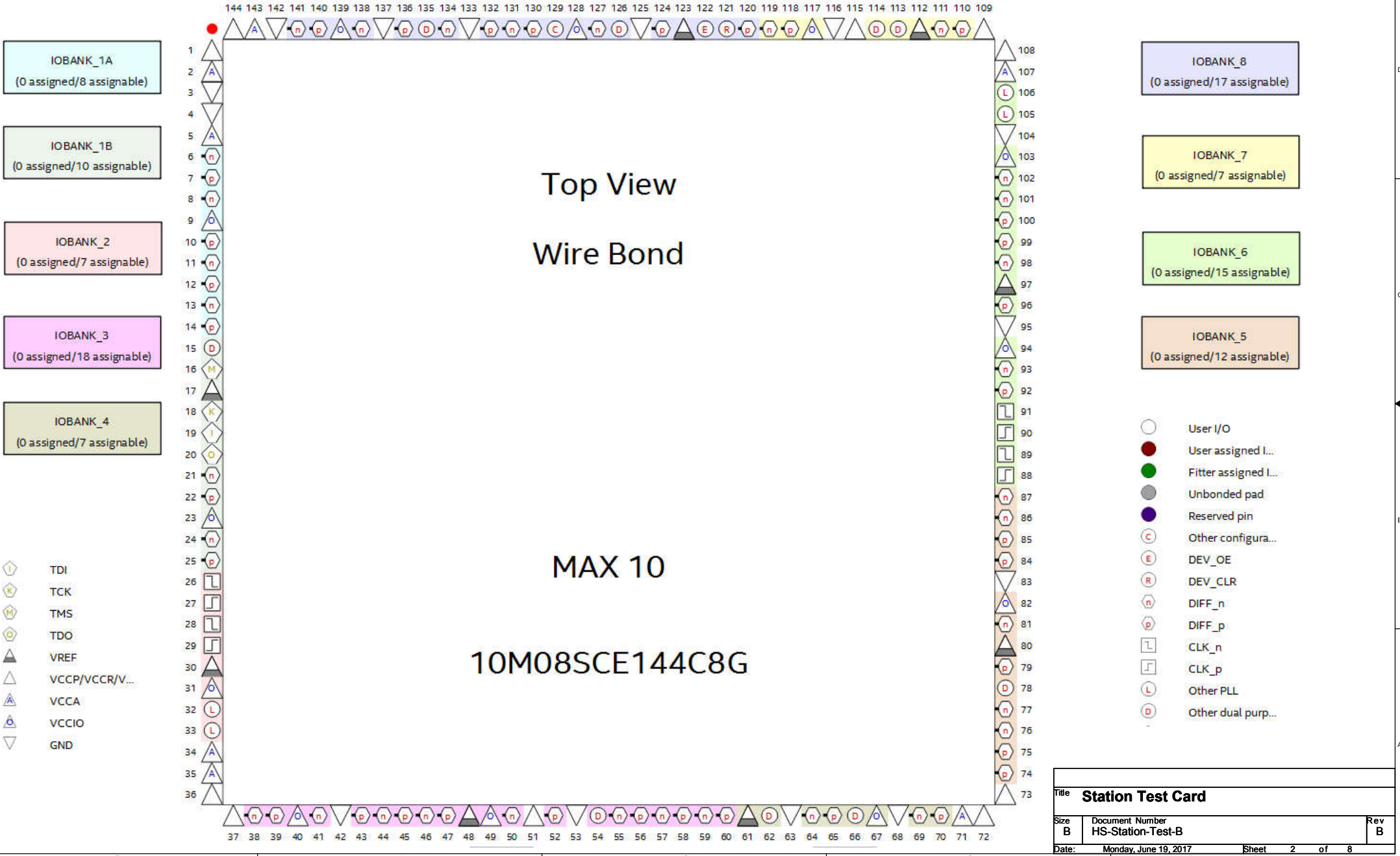
Sheet

1

of

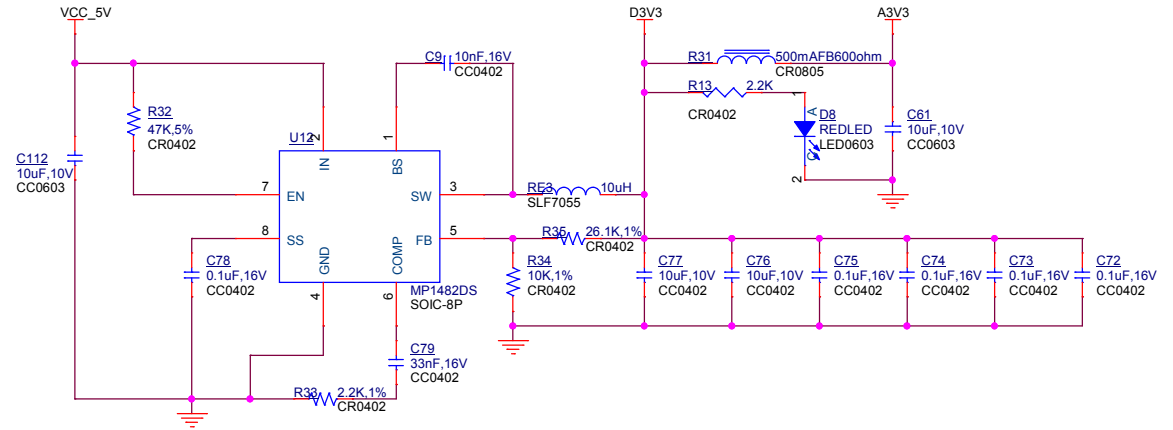
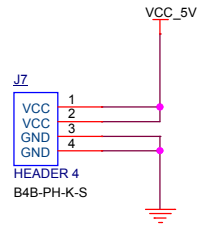
8

10M08SAE144 TOP VIEW

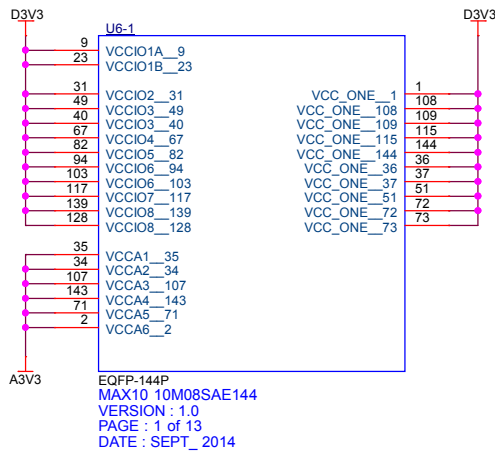


# Power

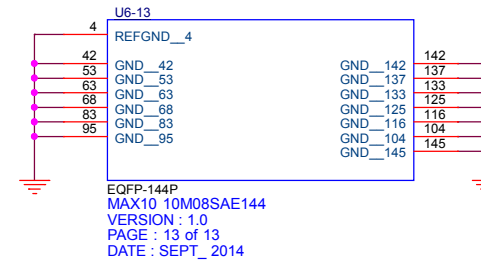
+3.3 V 2A Power



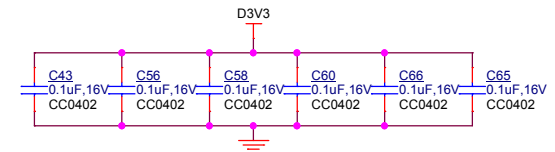
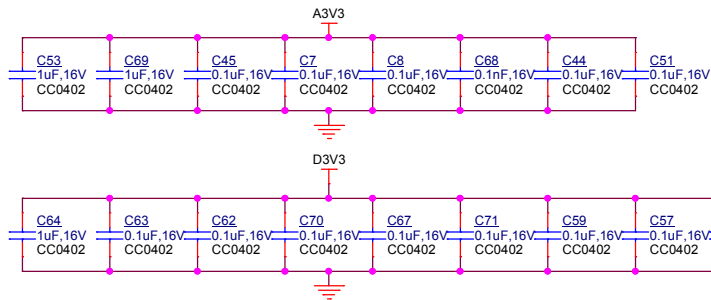
## FPGA Power



## FPGA GND

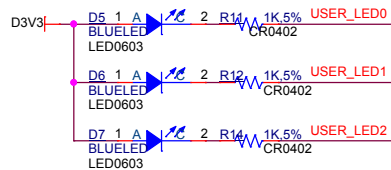
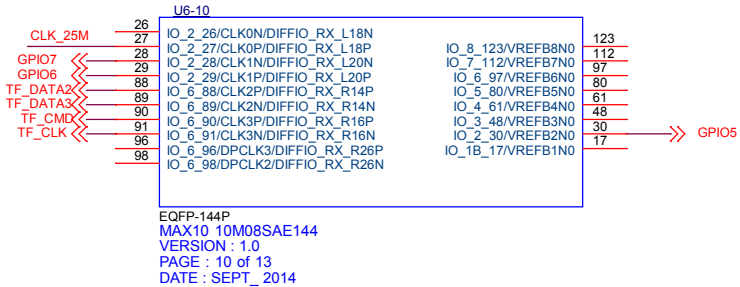
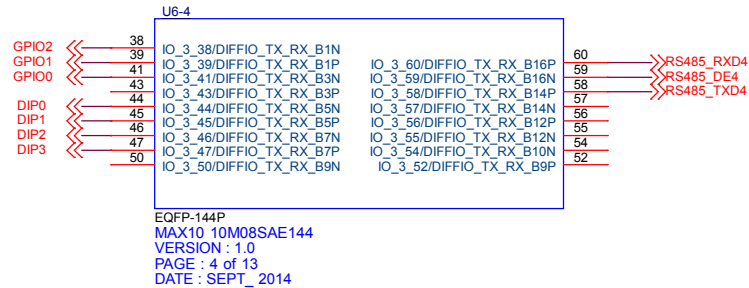
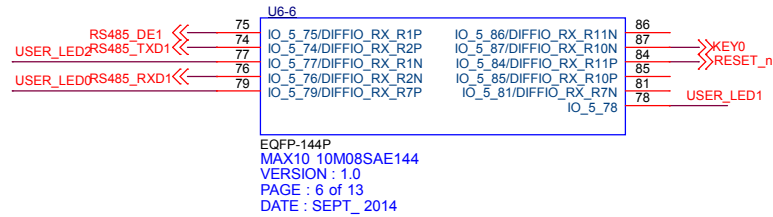
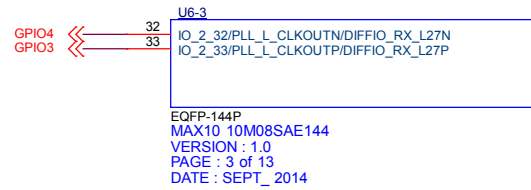
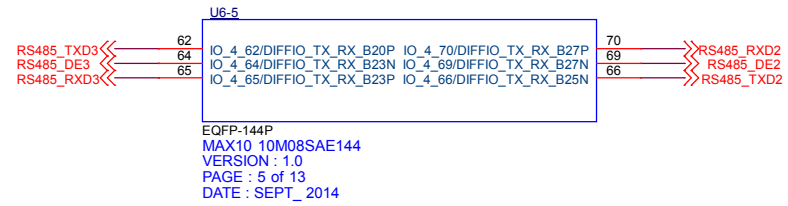
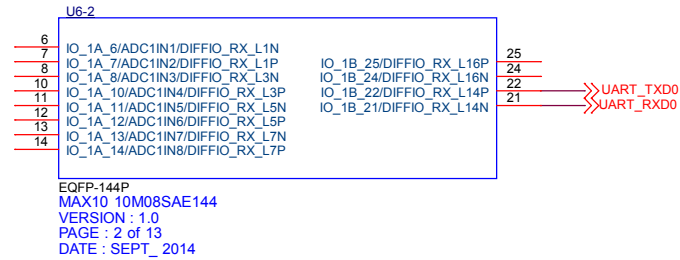


Place CAP Near FPGA

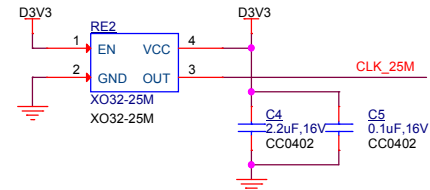


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# FPGA BANK IO - PAGE1

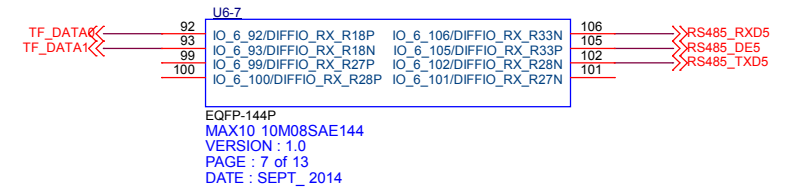
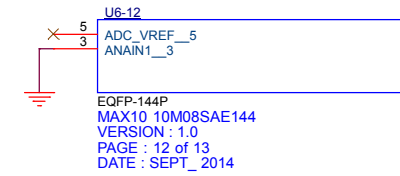
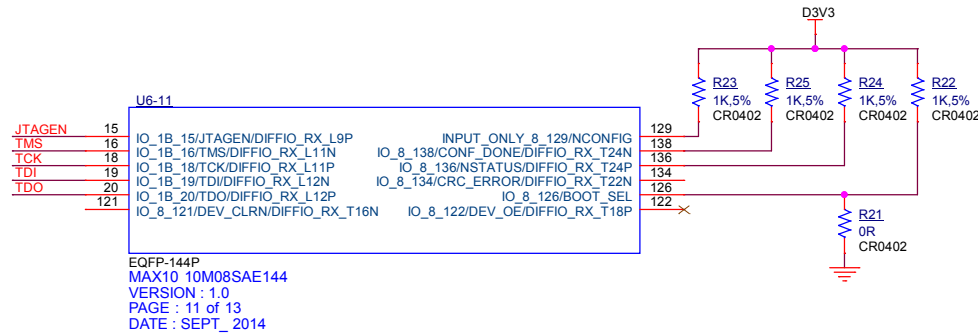
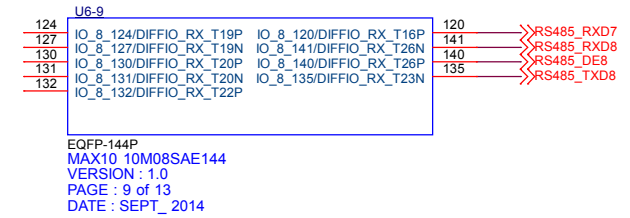
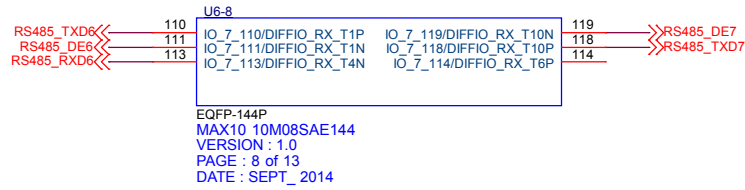


## 25MHz Logic Clock

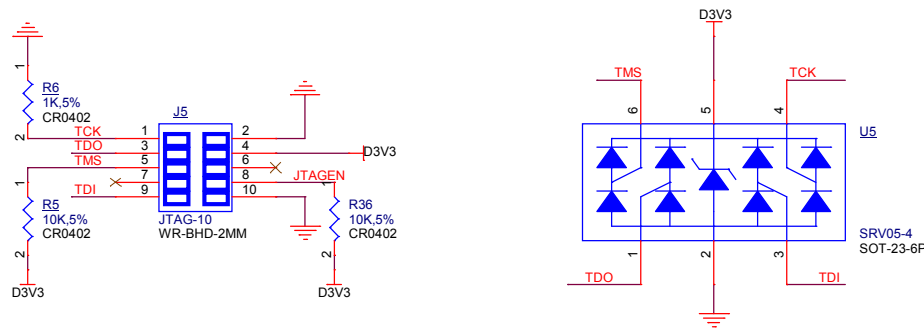


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# FPGA BANK IO - PAGE2



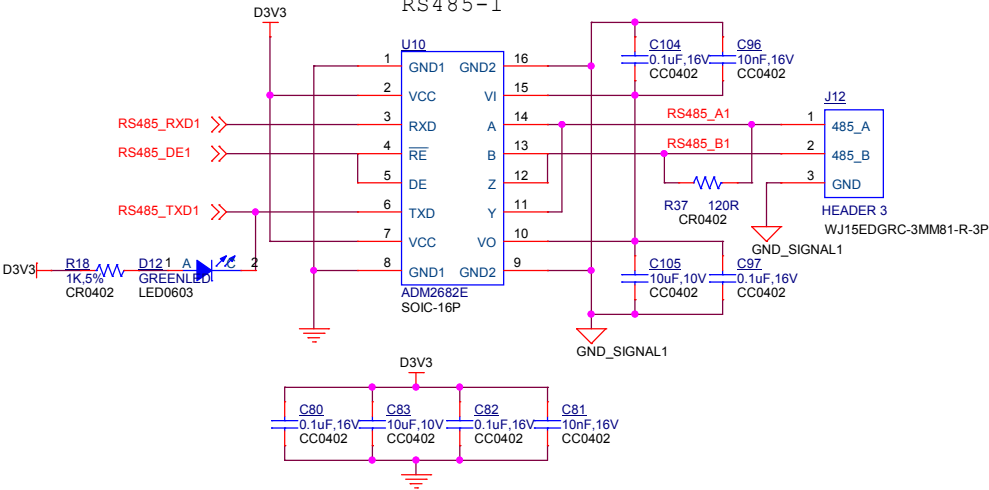
FPGA JATG



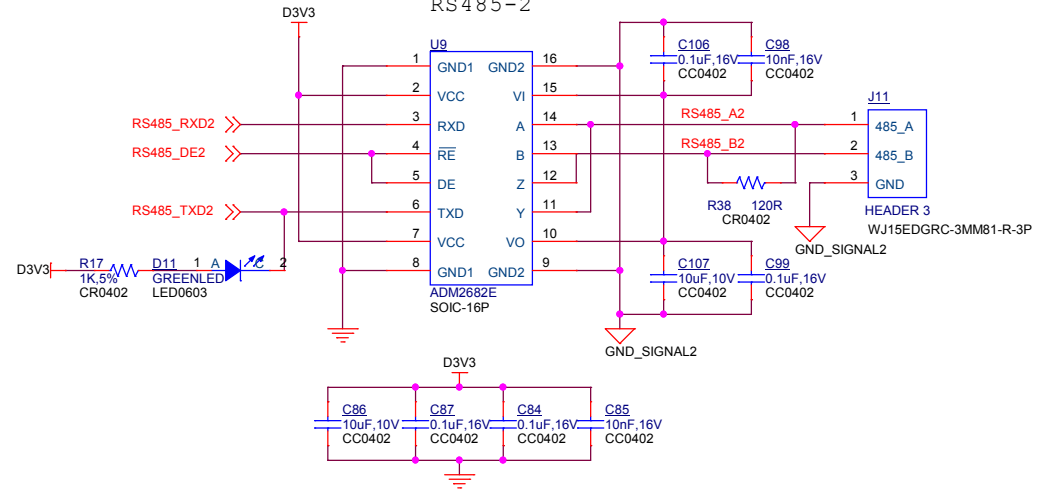
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# RS485 - PAGE1

RS485-1

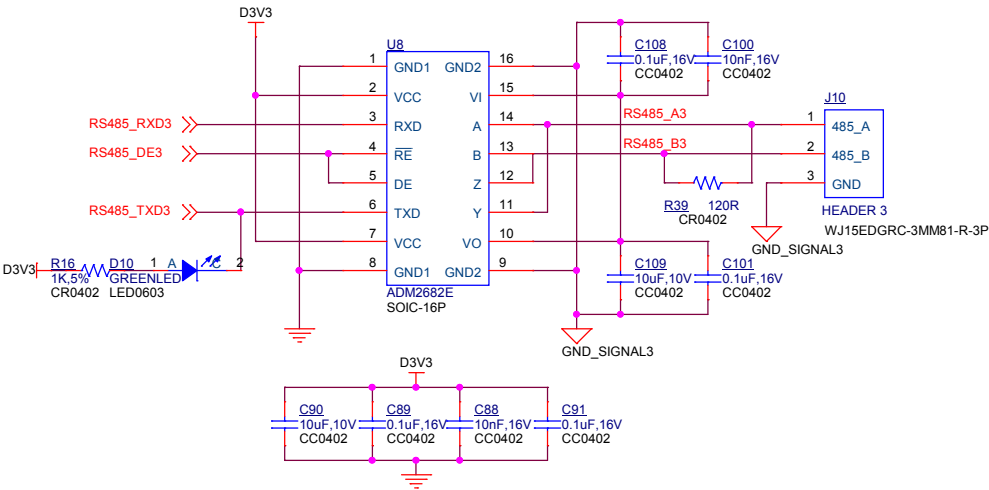


RS485-2

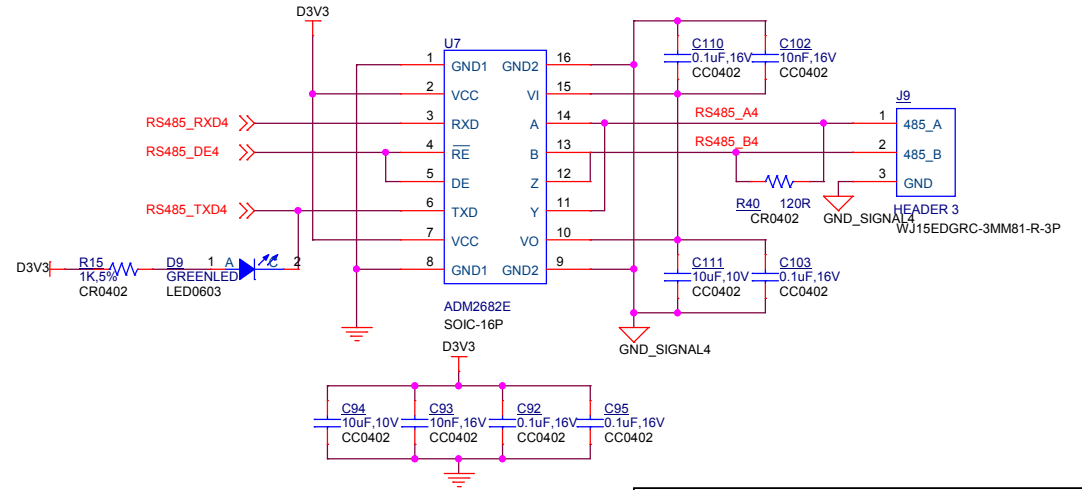


For All 485 Module: Place these CAPs  
between pins 1,8 and 2,7 of chips

RS485-3



RS485-4



Title **Station Test Card**

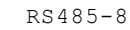
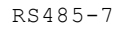
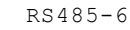
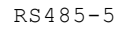
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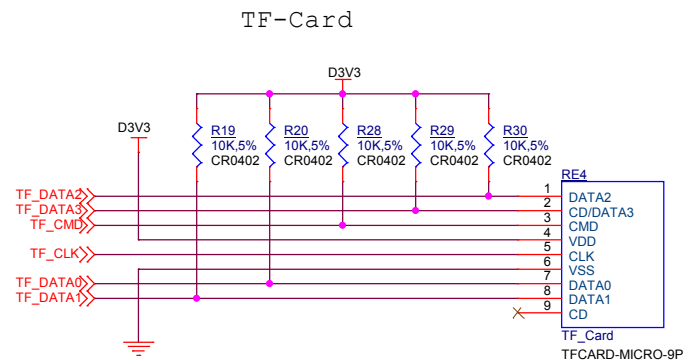
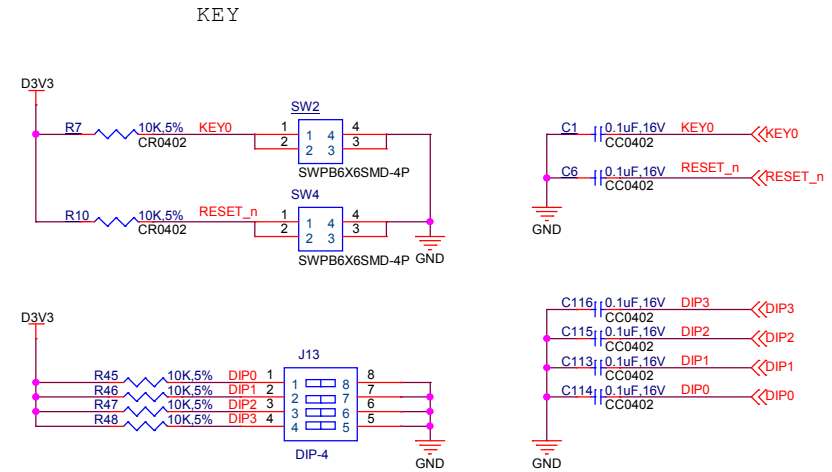
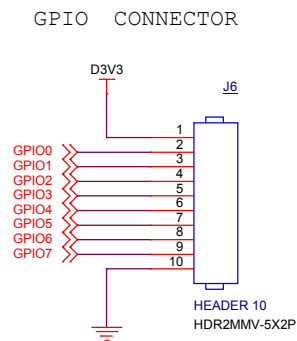
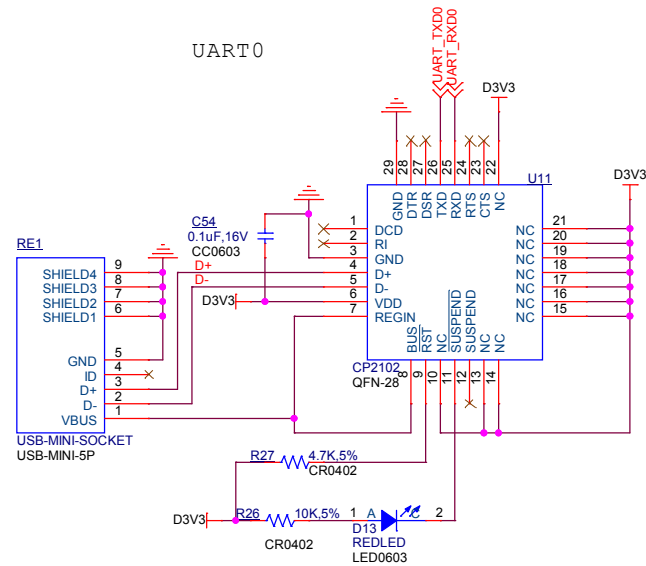
Rev B

**RS485 - PAGE2**



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## Peripherals



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<div> <div>Date:</div> <div>Tuesday, July 04, 2017</div> </div>		<div> <div>Sheet</div> <div>8</div> </div>	<div> <div>of</div> <div>8</div> </div>