

Essentials of PCB Design

03: Layout + Routing

welcome back!

schedule

A-Term

Tue, Sep. 24	Basics of PCBs 6-7PM; SH 301
Thur, Sep. 26	Designing your Project 6-7:30PM; SH 201
Tue, Oct. 1	Layout + Routing 6-7:30PM; SH 201
Thur, Oct. 3	Working with KiCad 6-7:30PM; SH 201
Mon, Oct. 7 - Fri, Oct. 11	Office Hours TBD; IEEE Lounge

B-Term

Mon, Oct. 21 - Fri, Oct. 25	Office Hours TBD; IEEE Lounge
Fri, Oct. 25	Boards Due By 10PM
Tue, Nov. 5 (Wellness Day)	Assembly TBD; AK 113

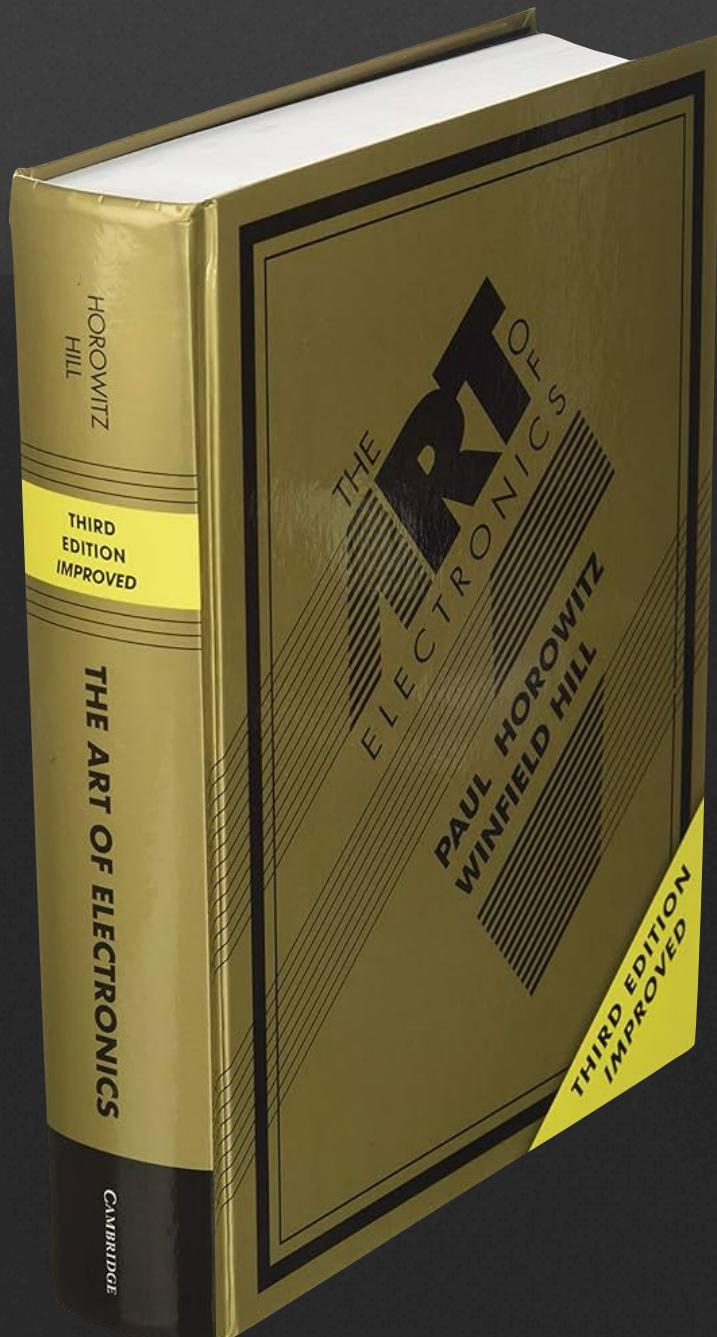
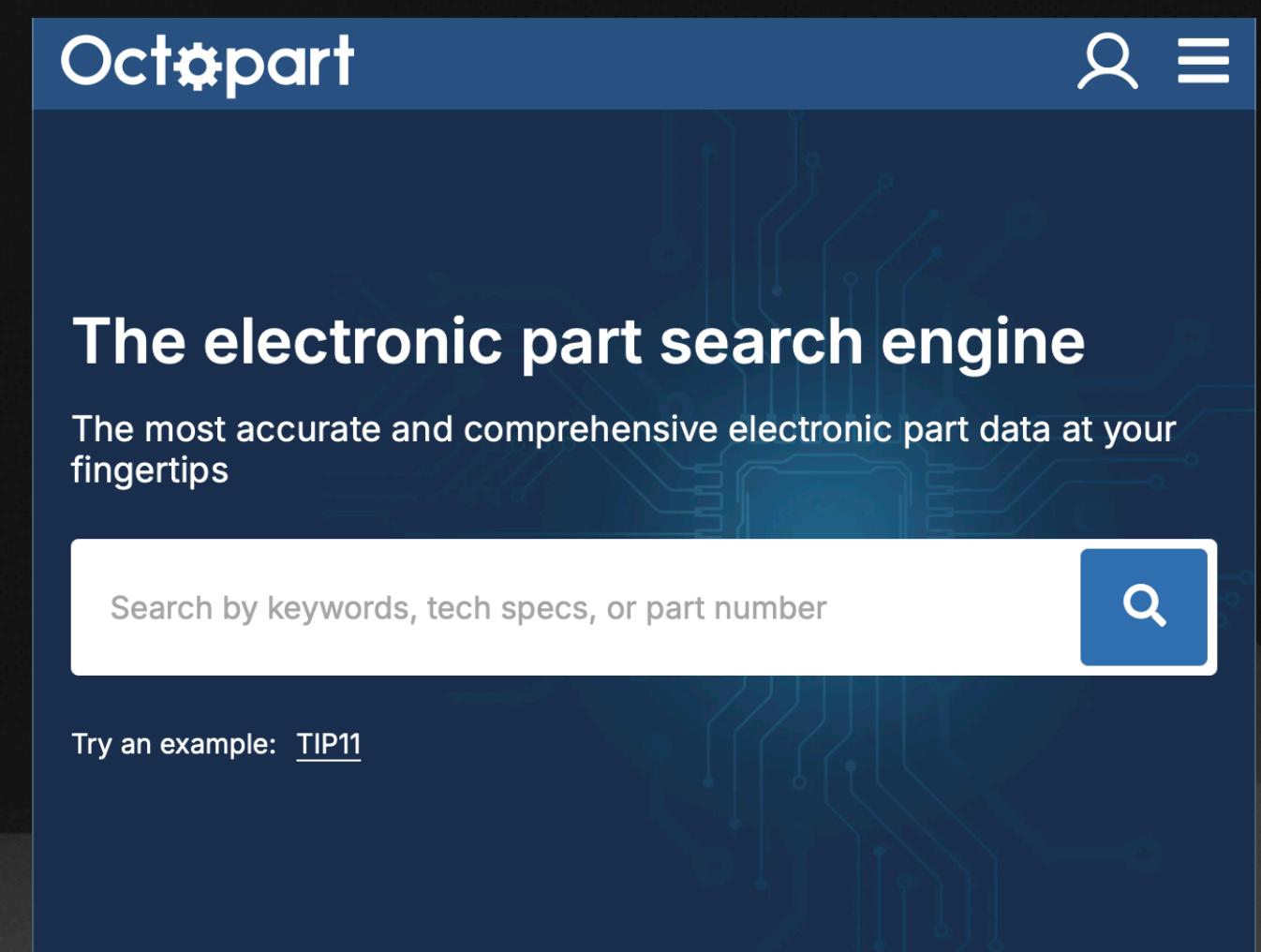
course updates

lecture 03

- Make sure you're on the email alias and **registered for a track!**
- Lecture 2 feedback 
- Echo 360 recordings are being wacky
- Make sure you have KiCad installed! (kicad.org/download)
- Pull the GitHub! (github.com/ieee-wpi/pcb)

technical resources to help you

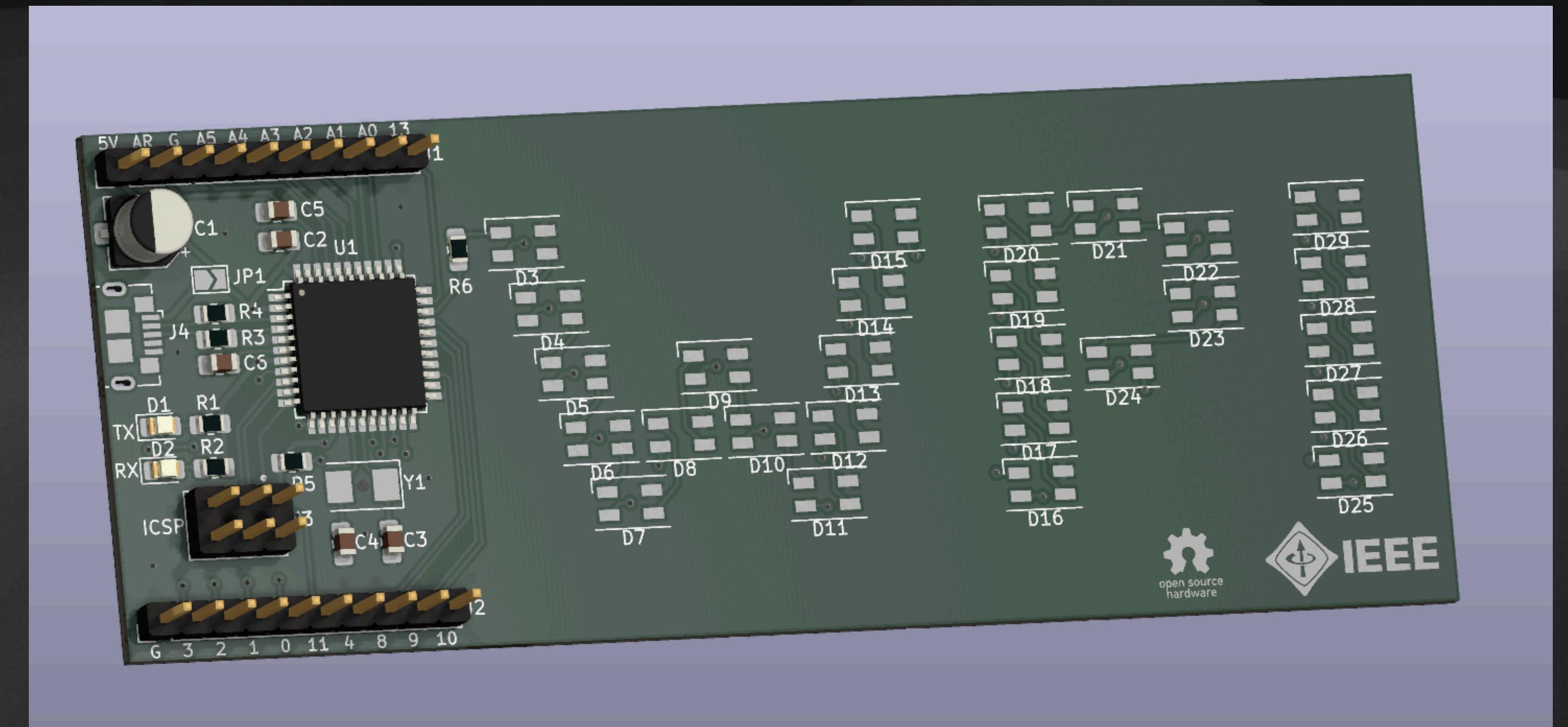
- pcb.mit.edu/resources
- Octopart
- DigiKey trace width calculator
- The Art of Electronics, Horowitz and Hill
- Open Circuits, Schlaepfer and Oskay



hardware design process

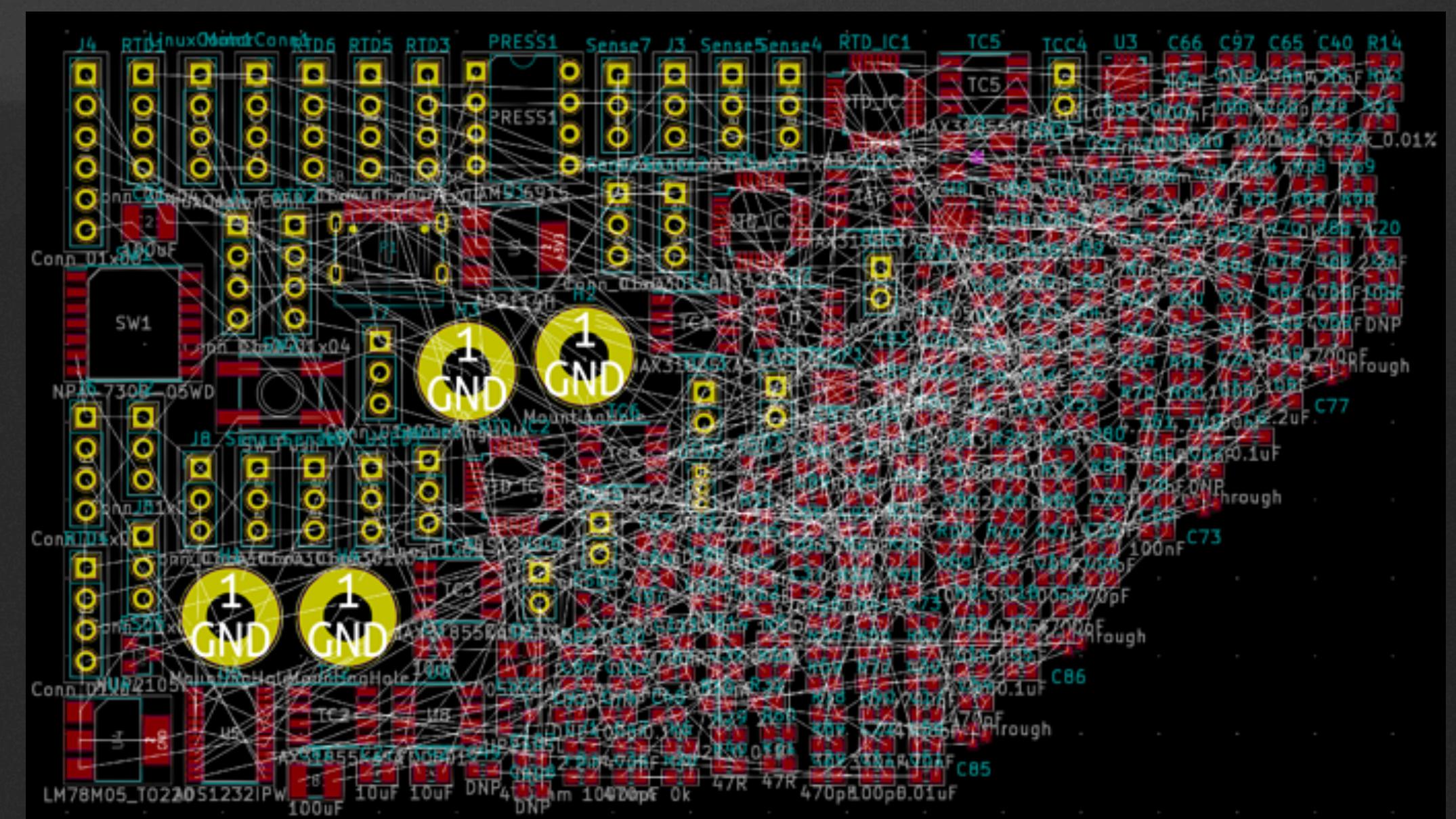
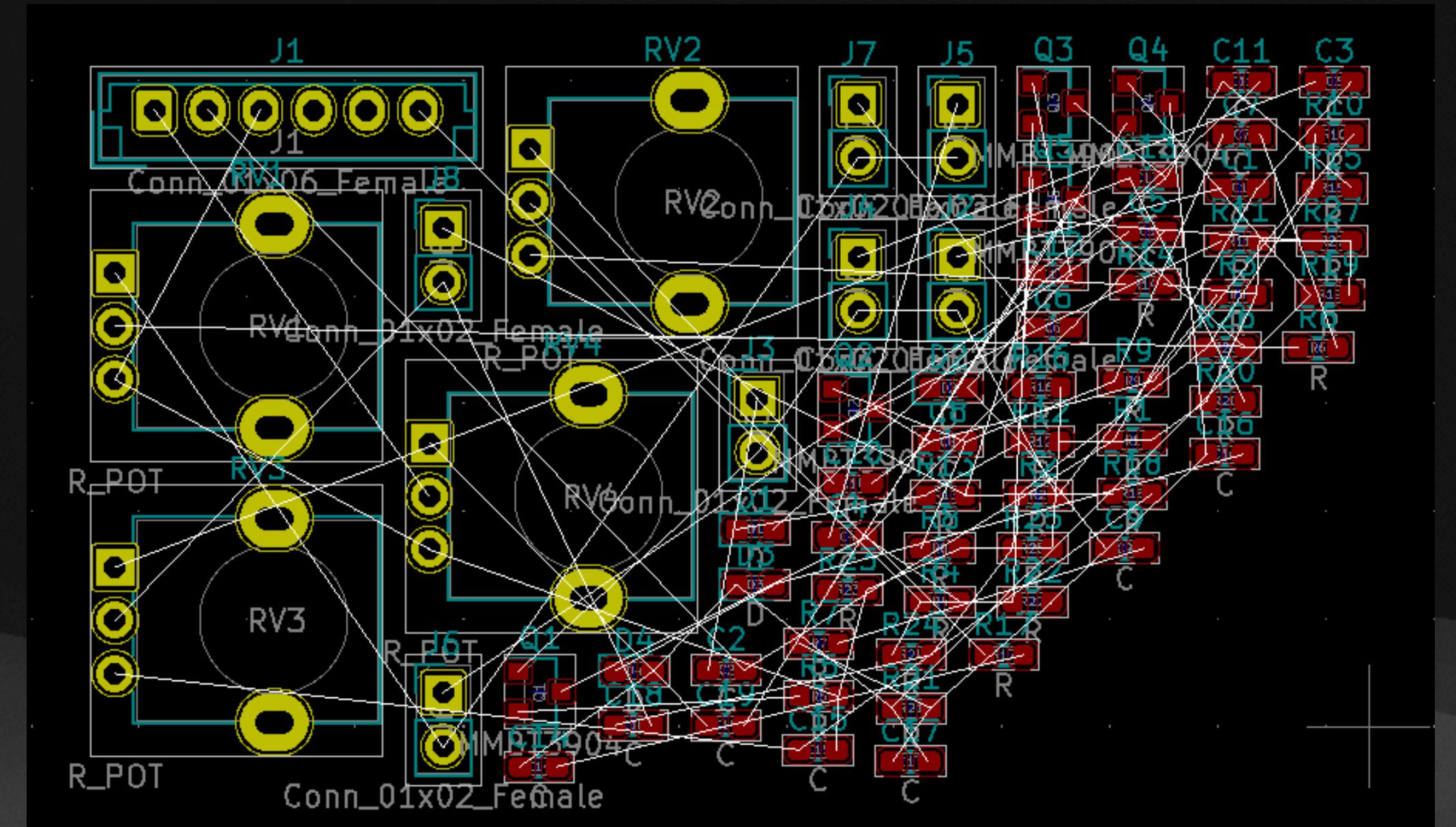
walkthrough

1. Research and Design
2. Schematic Capture
- 3. Layout**
4. Routing
5. Order
6. Assembly



layout process

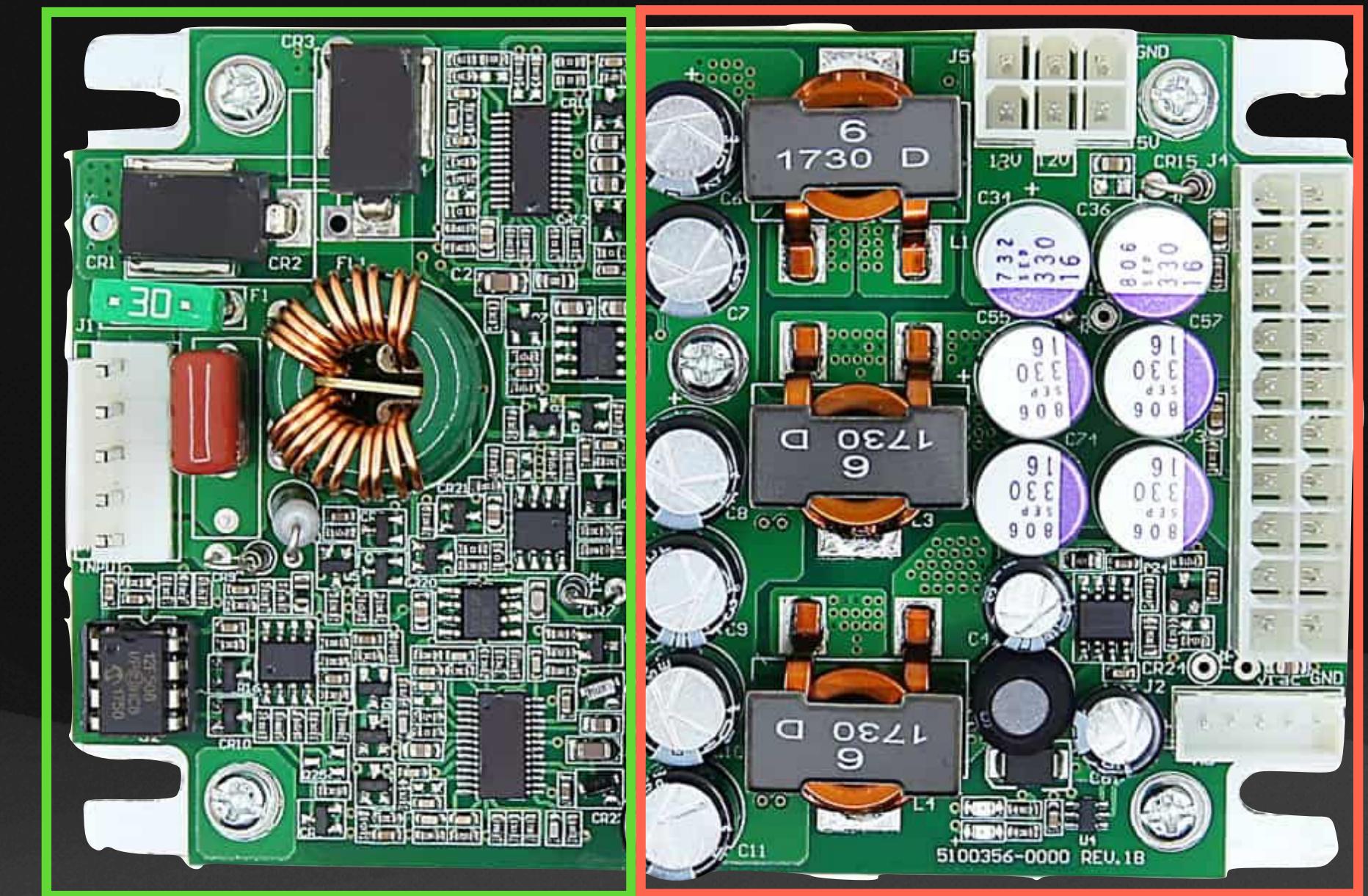
- Layout is an art
- Smart layout will save you hours of routing
- The goal here is to minimize **net intersections** by changing:
 - Component location
 - Component rotation
- Layout all your components first, **then** route!



Layout is Fun!

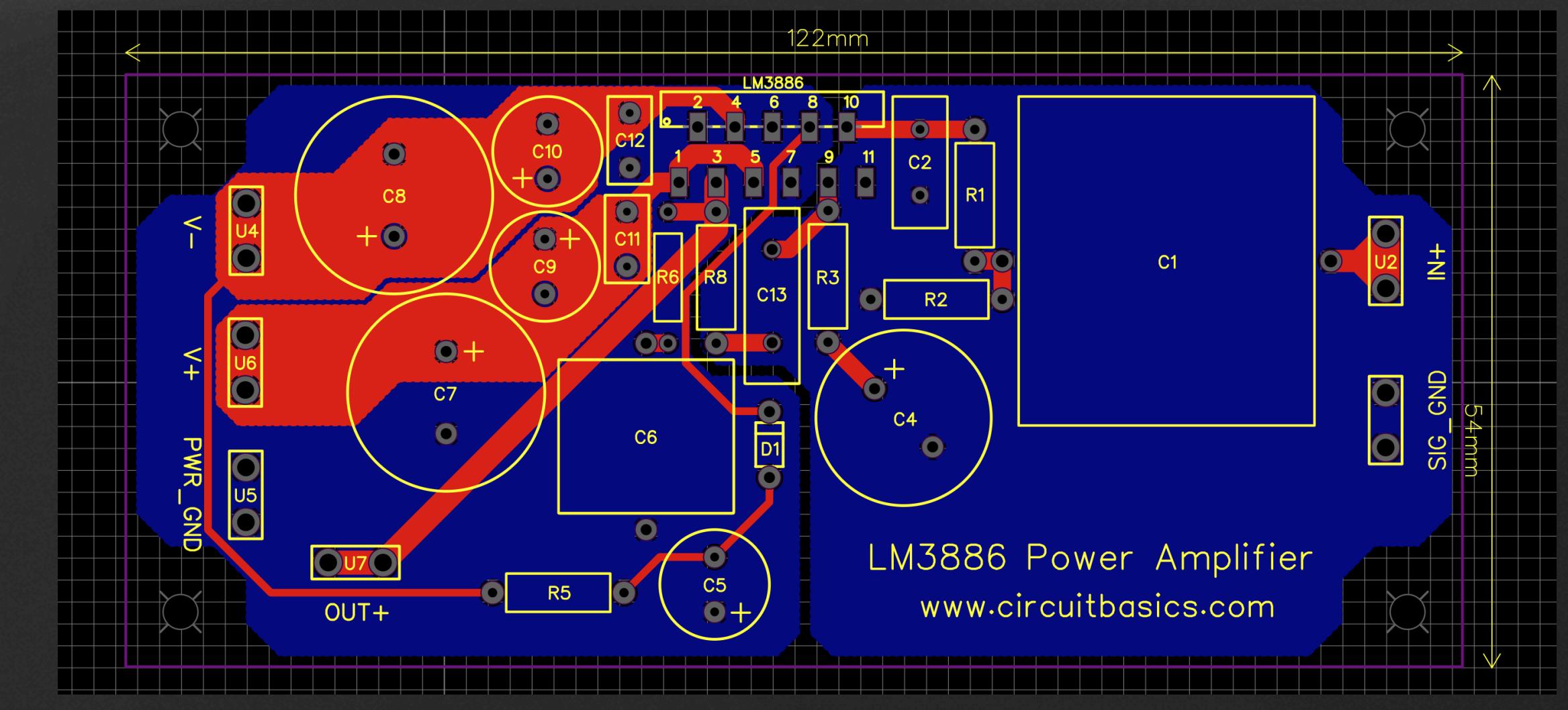
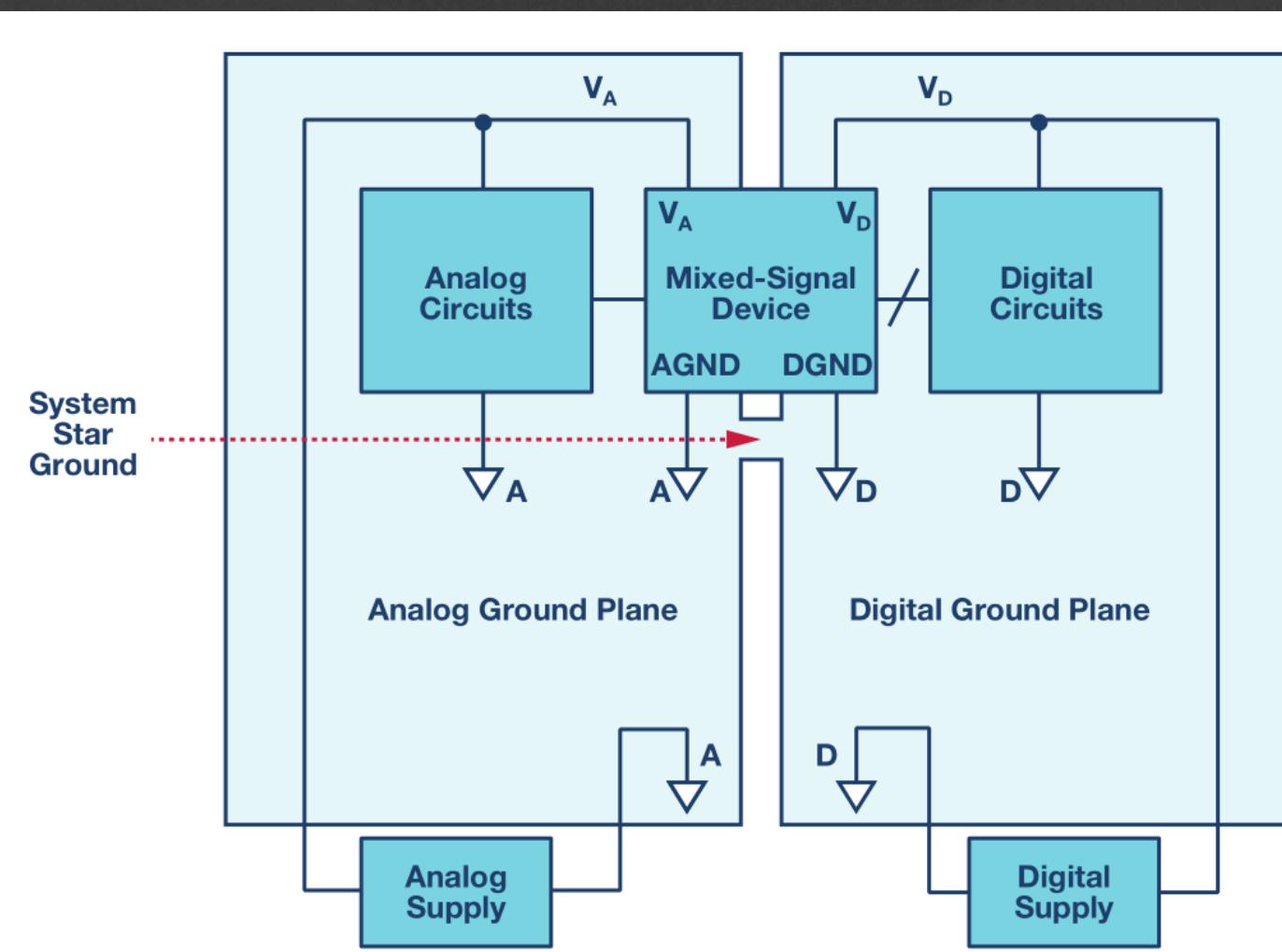
layout seperation

- About more than just connecting things...
- Separation of **power and signal**
- Separation of **digital and analog** ground



Signal

Power

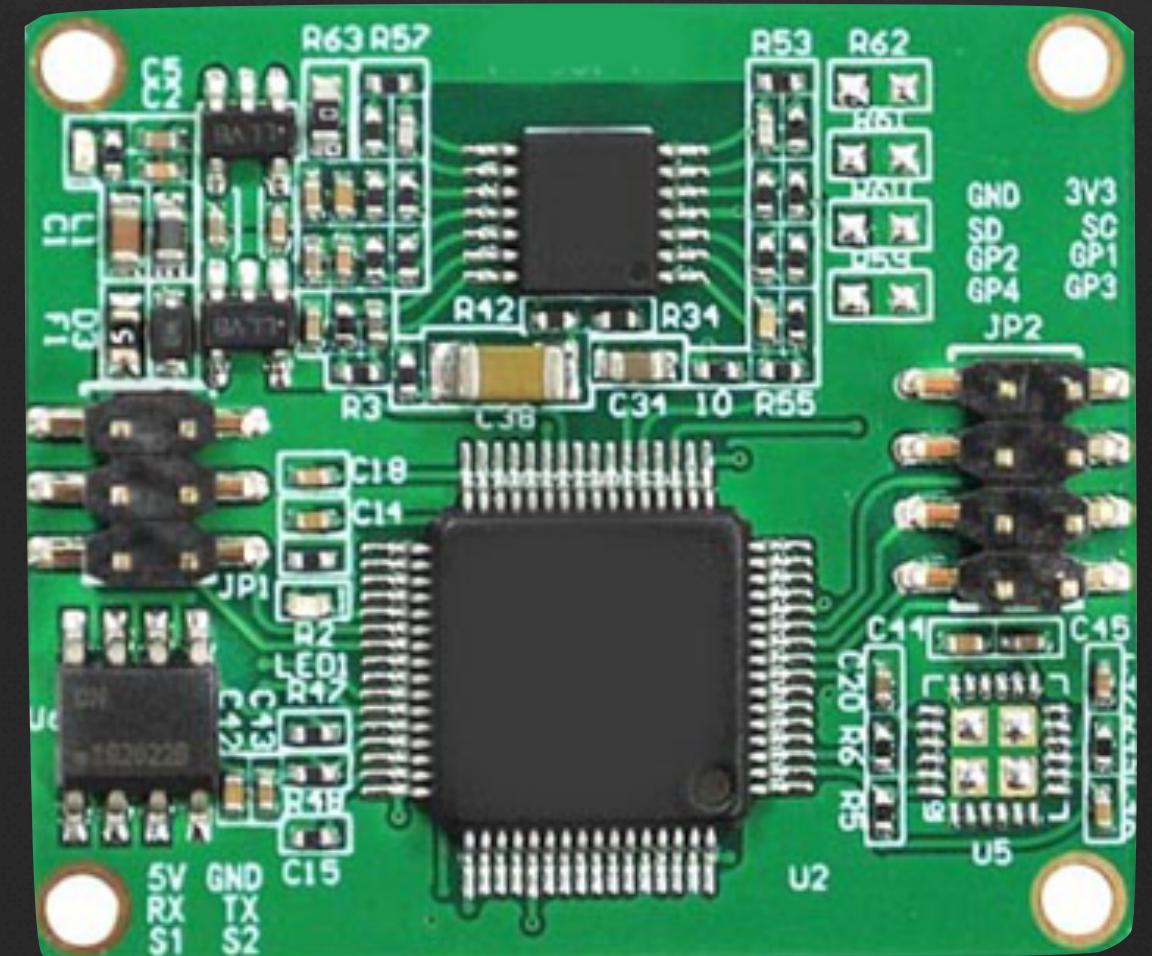
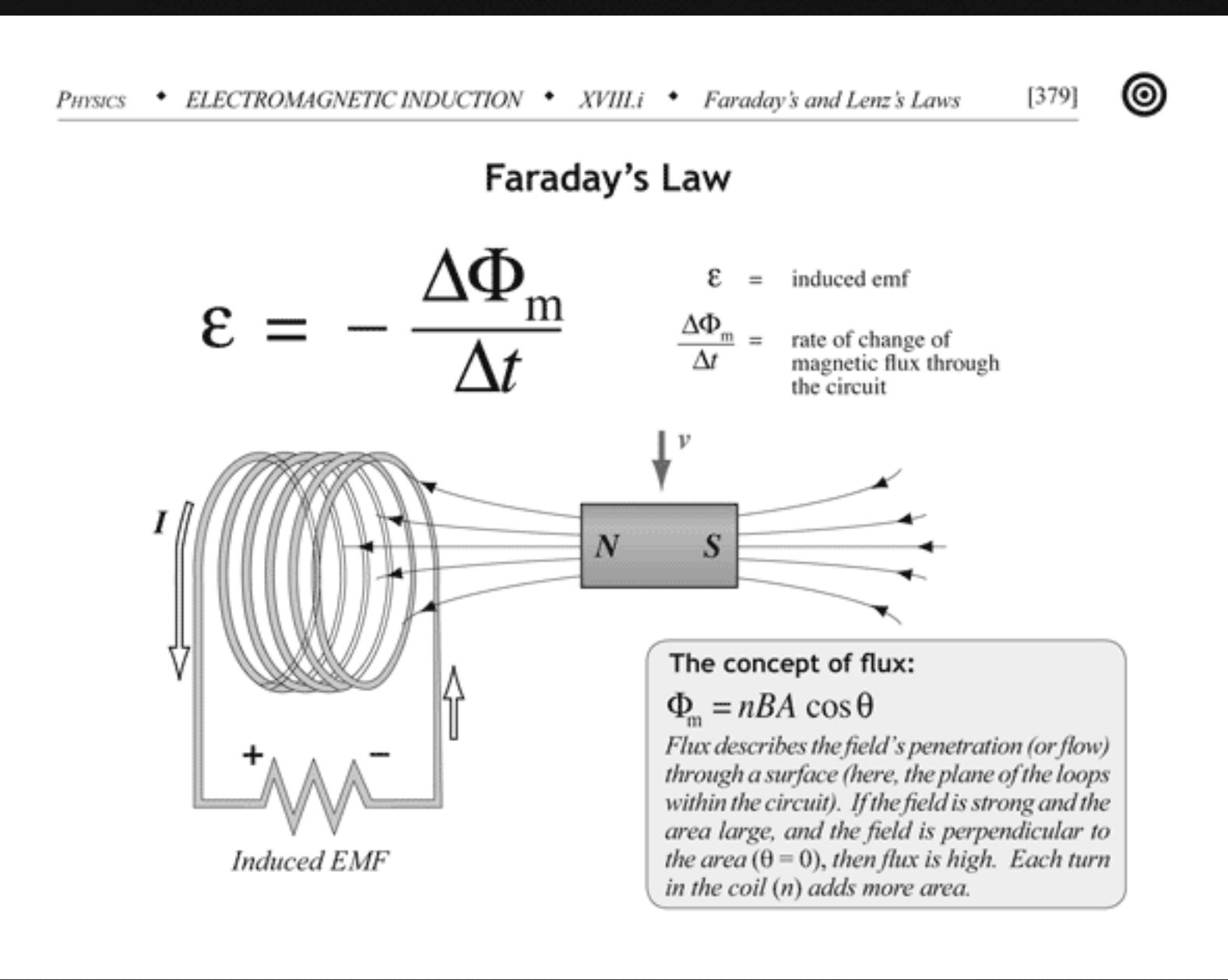


Digital GND

Analog GND

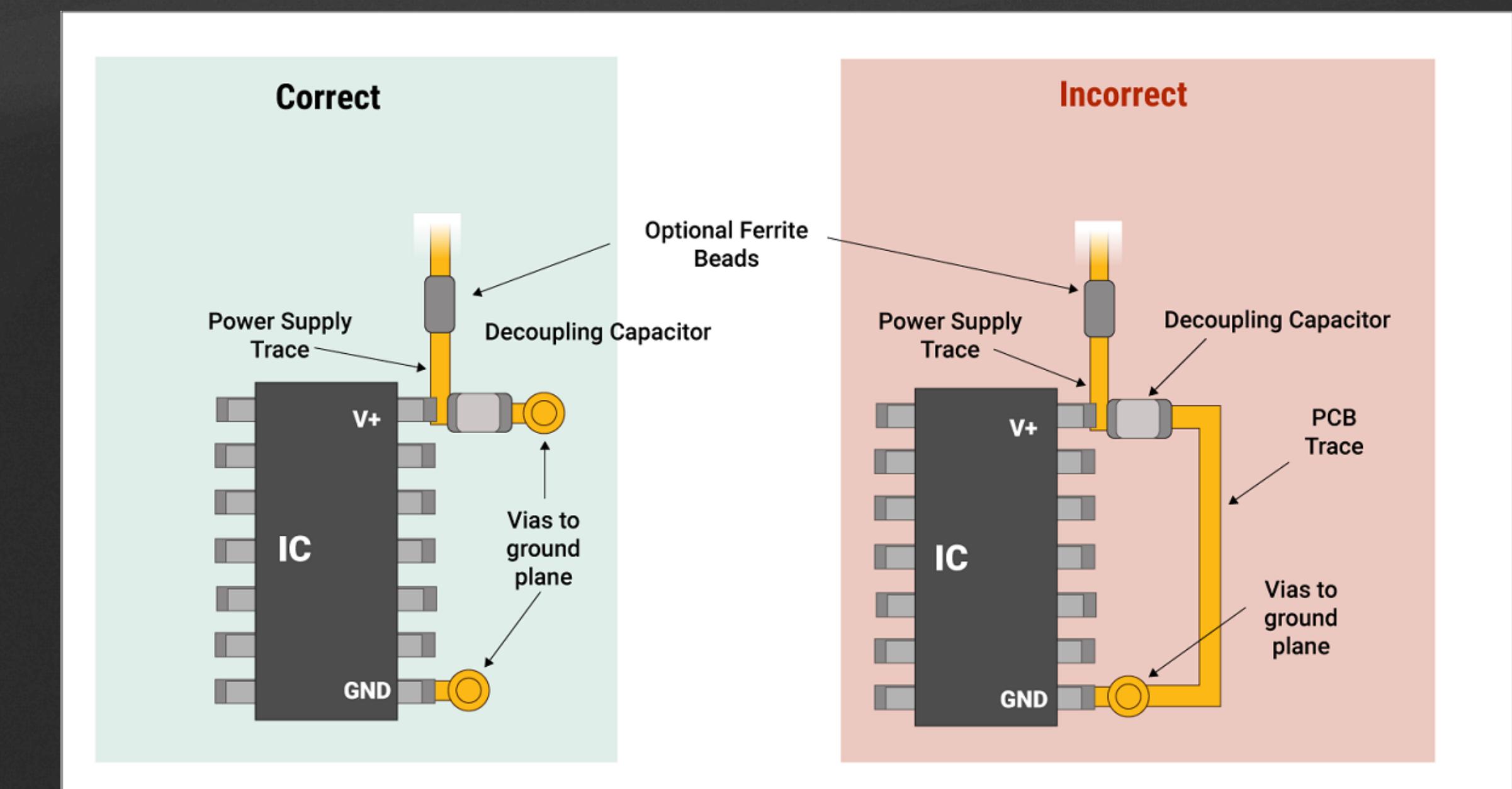
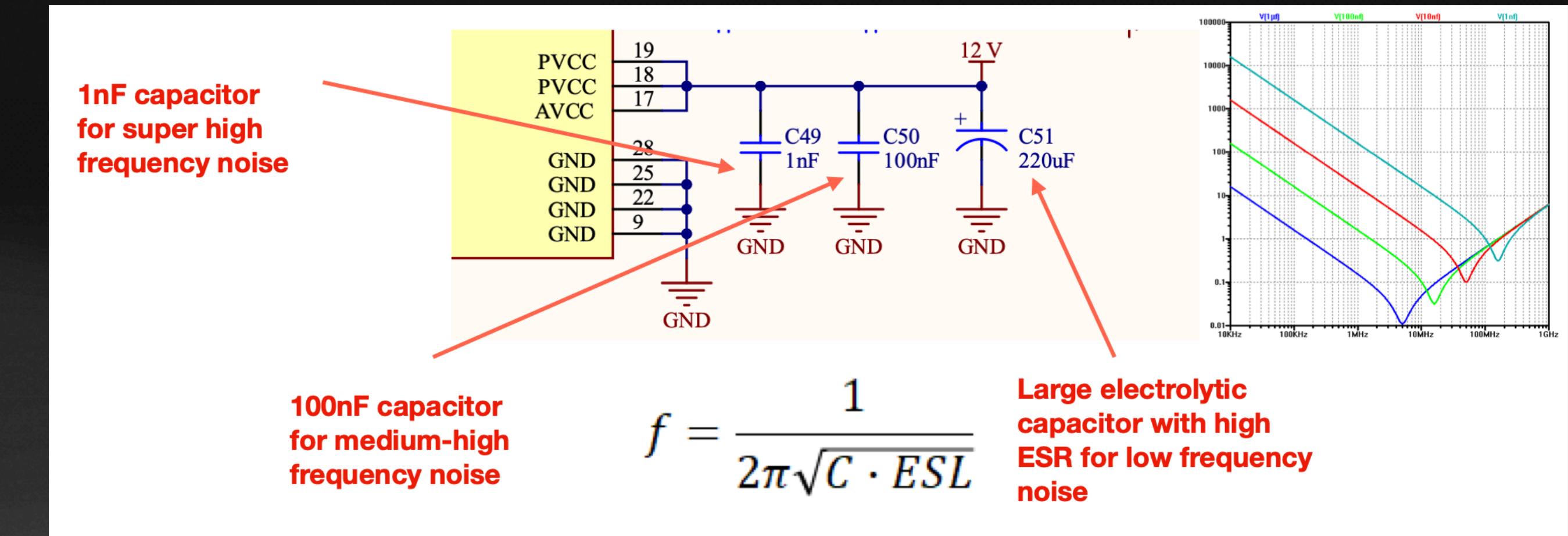
layout considerations

- Placement of sensitive components (sensors)
- Decoupling capacitor location
- Optimizing trace length; inductance loops
- Tightly package components



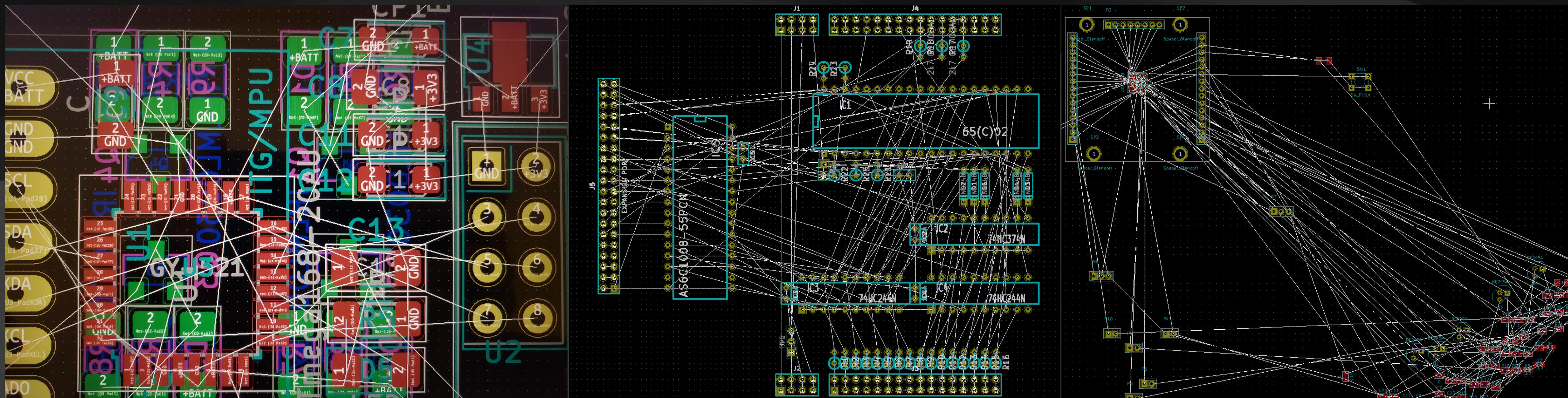
layout considerations

- Decoupling capacitor location
- Should be as close as possible to IC and ground



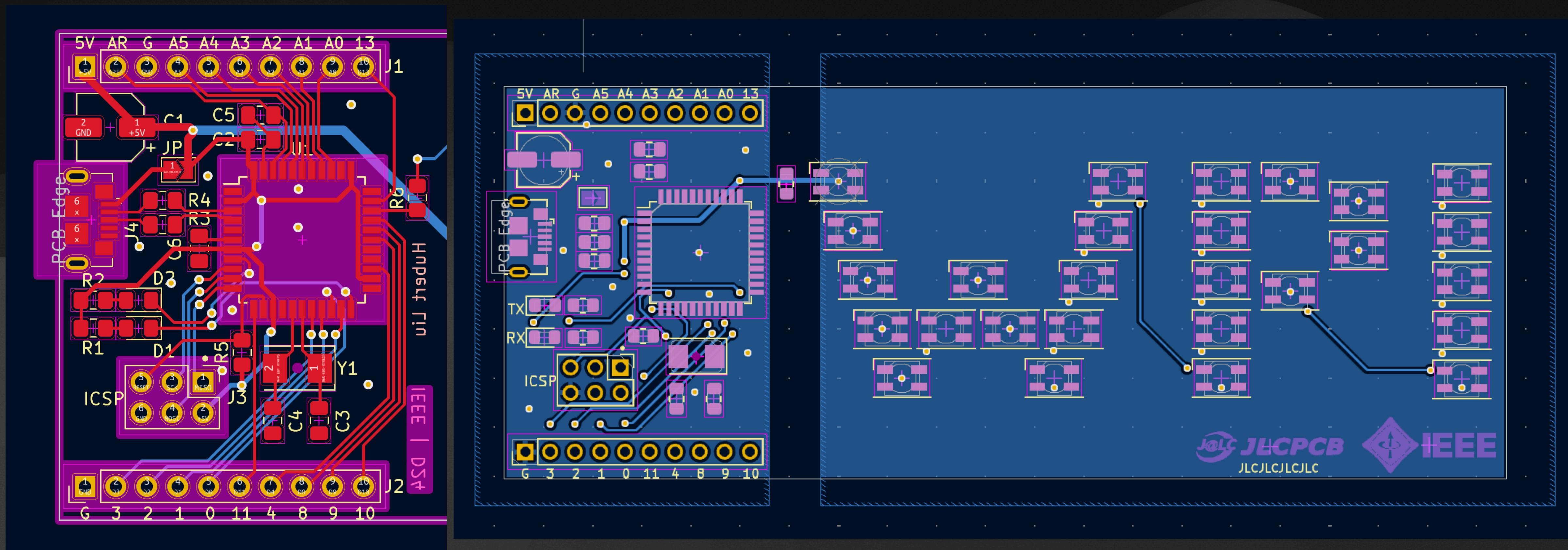
layout

the bad

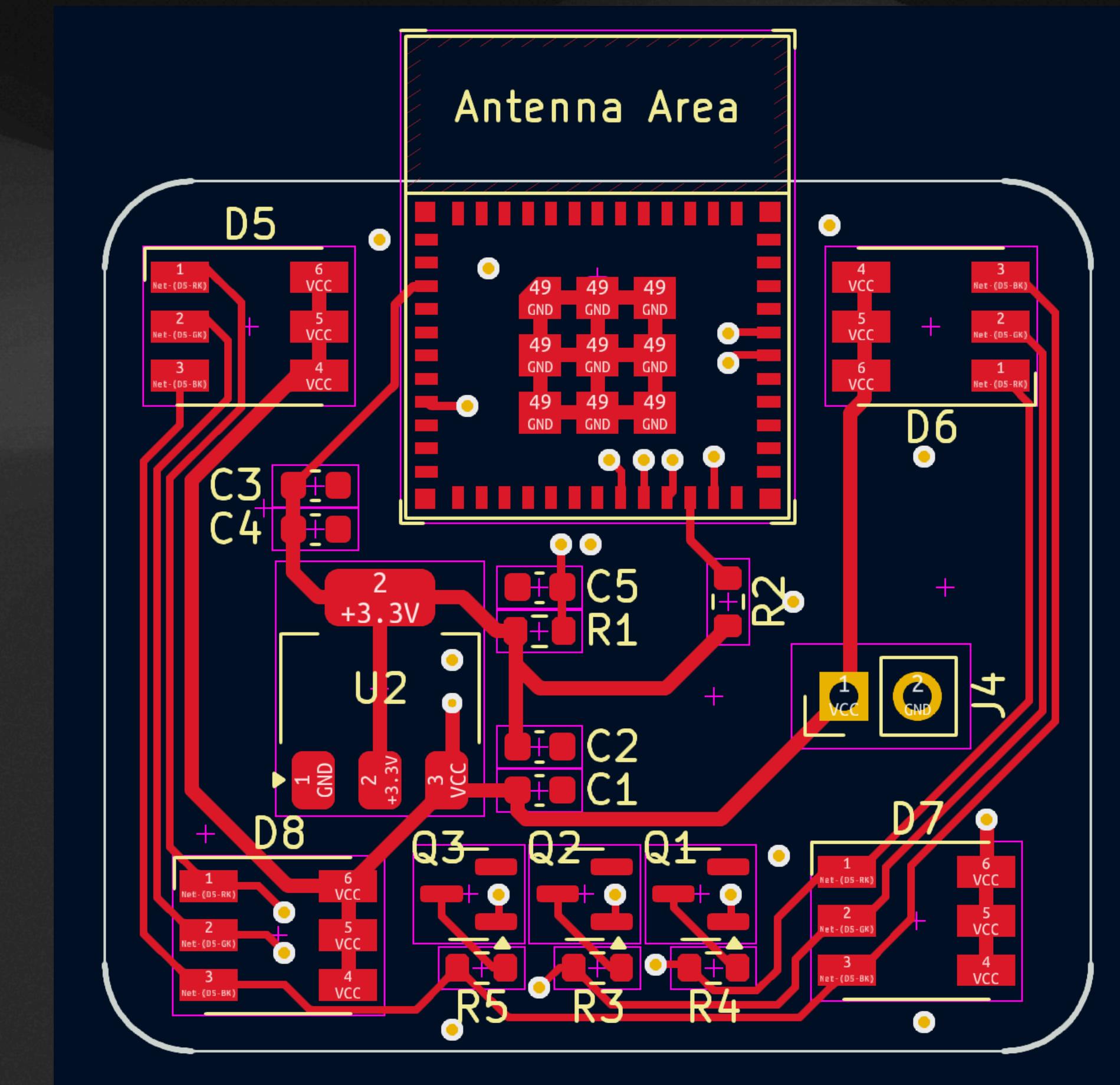
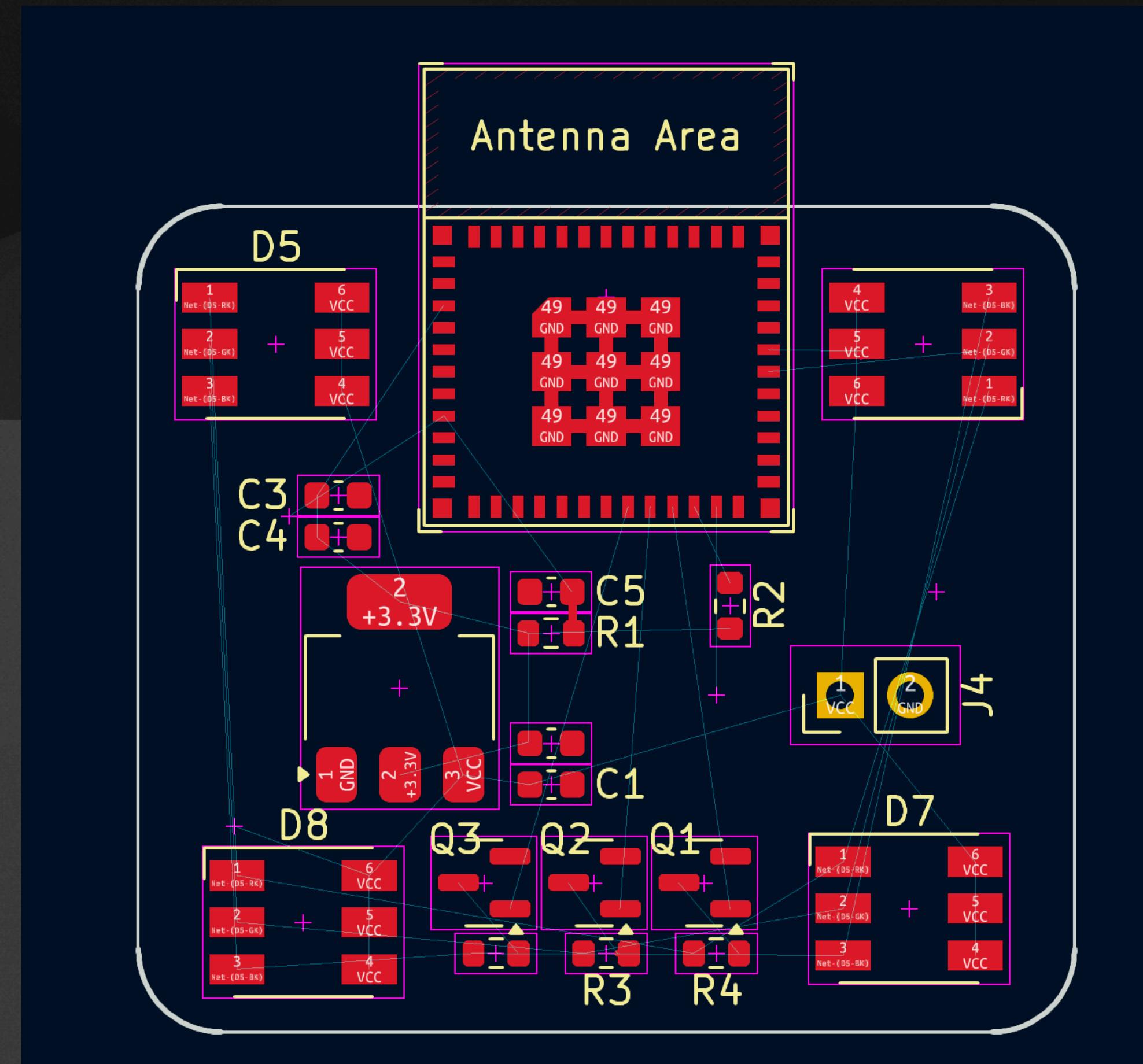


layout

the good

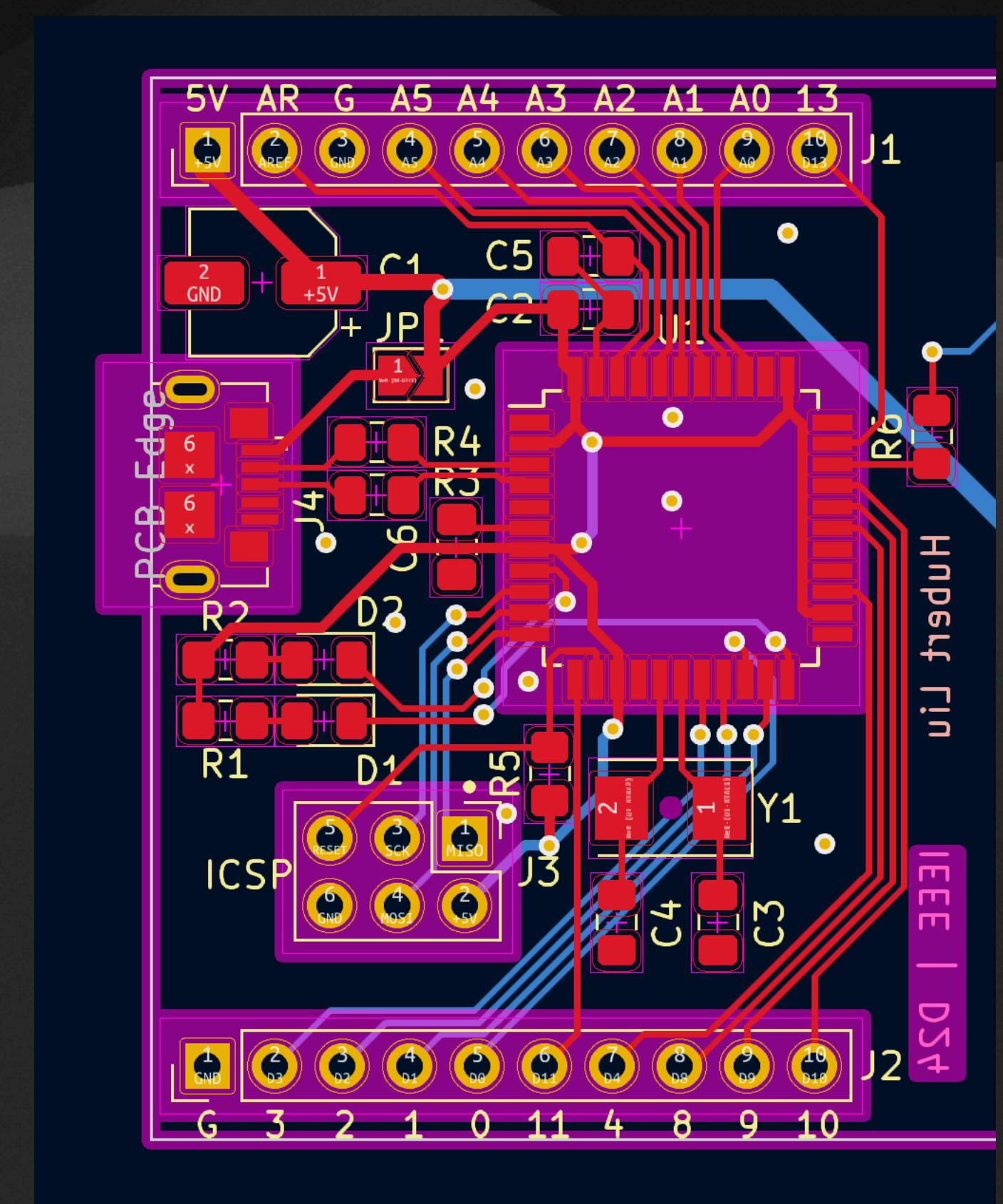
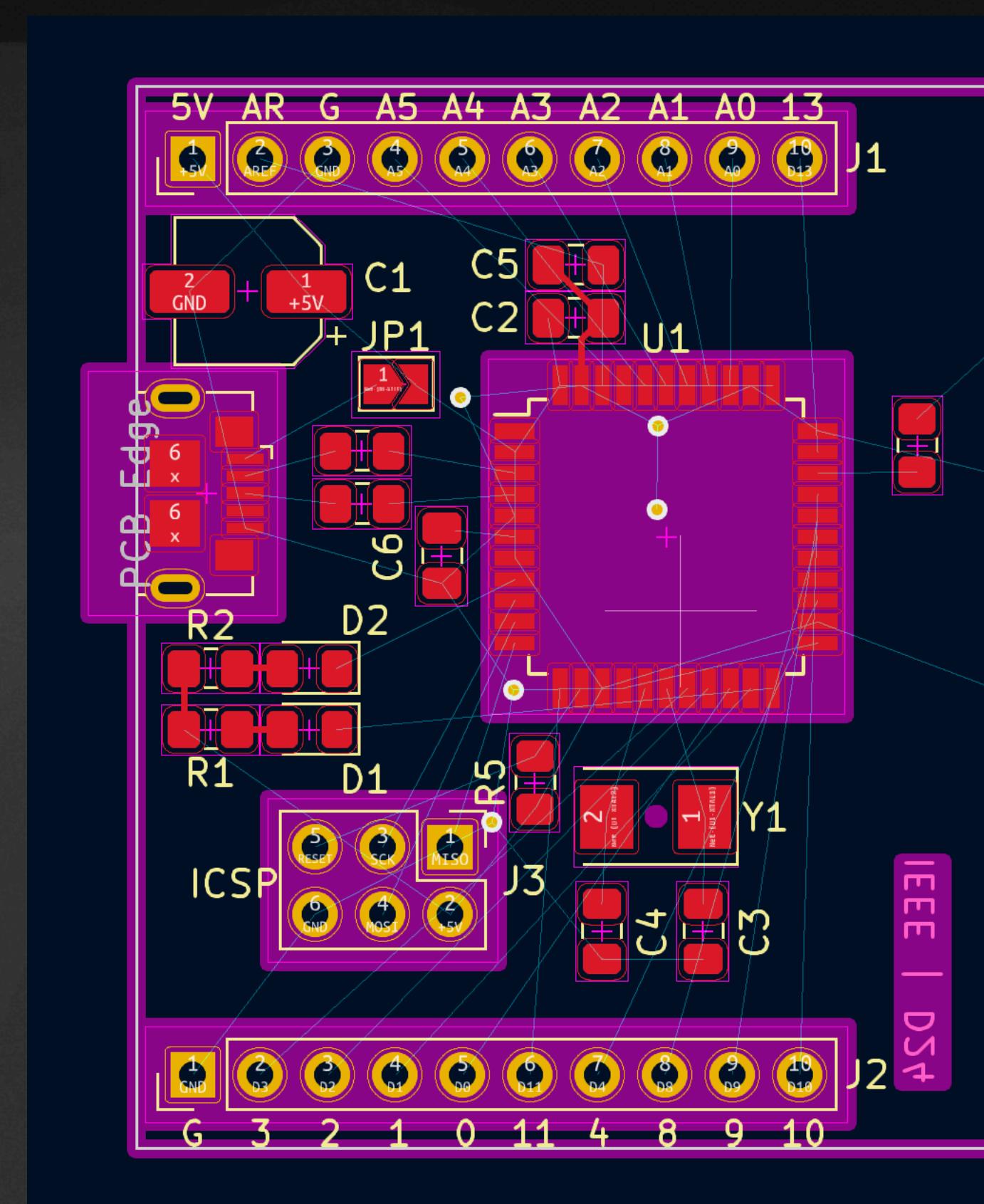
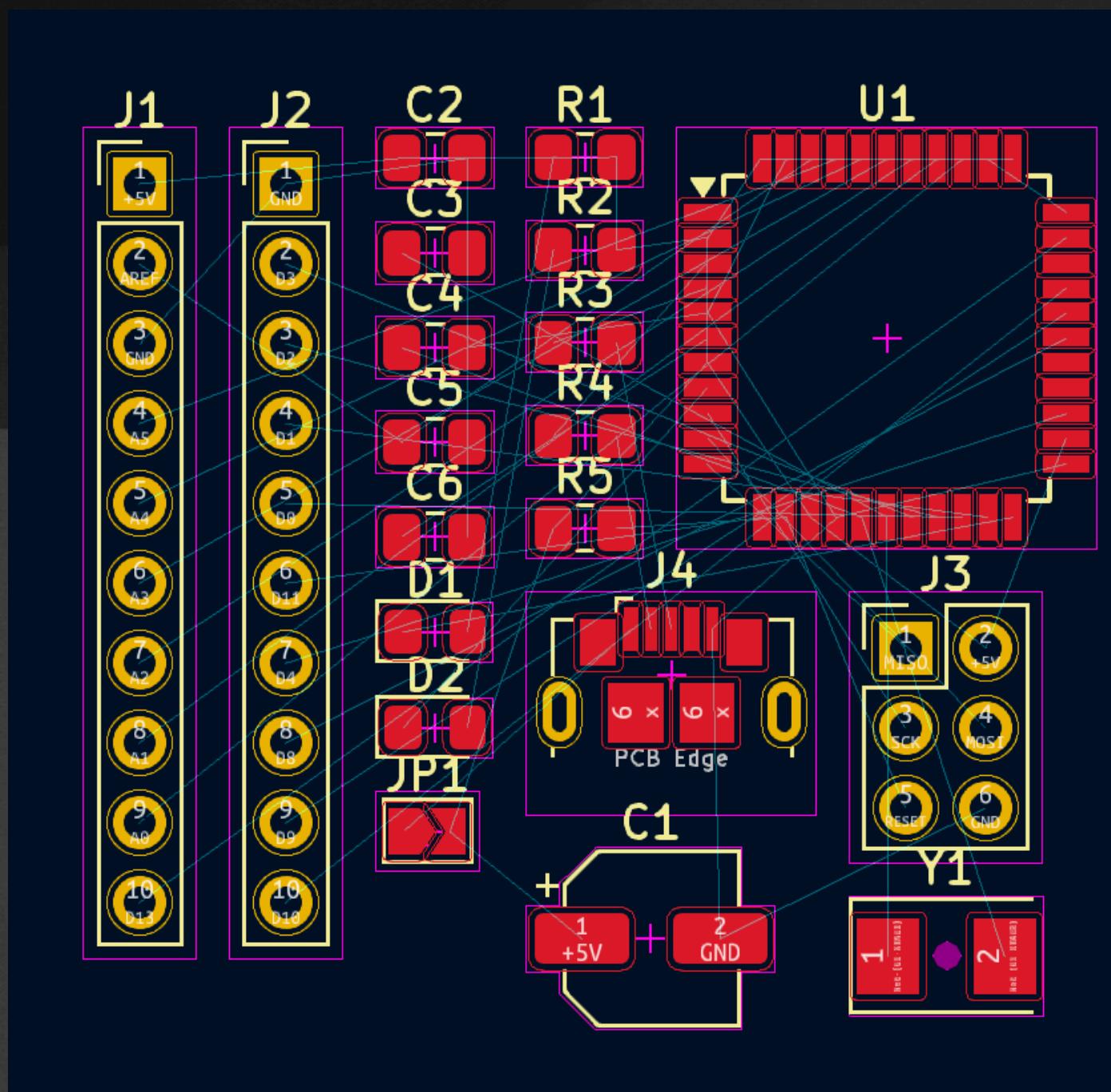


layout process



layout

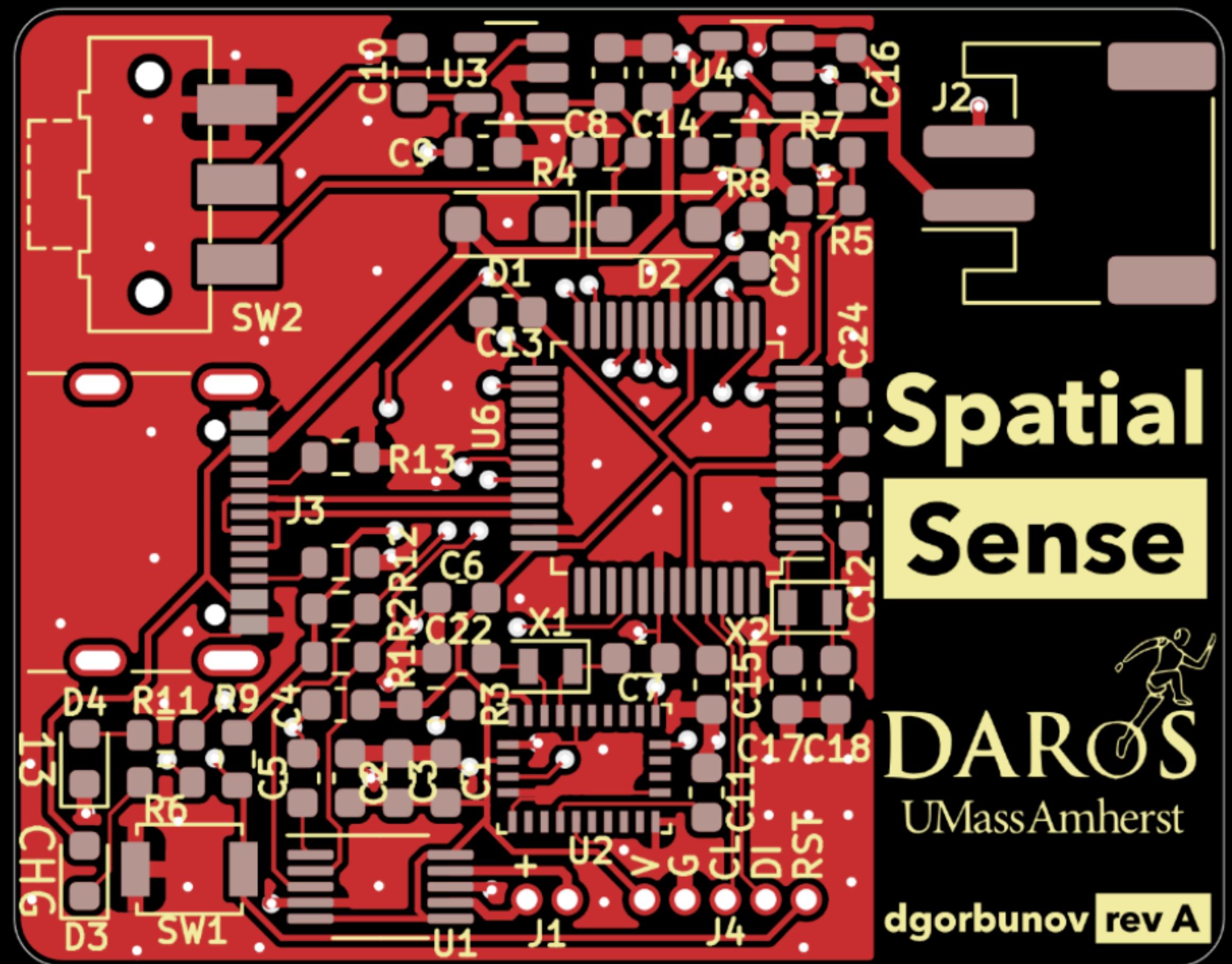
track 1 board



PCB Layout

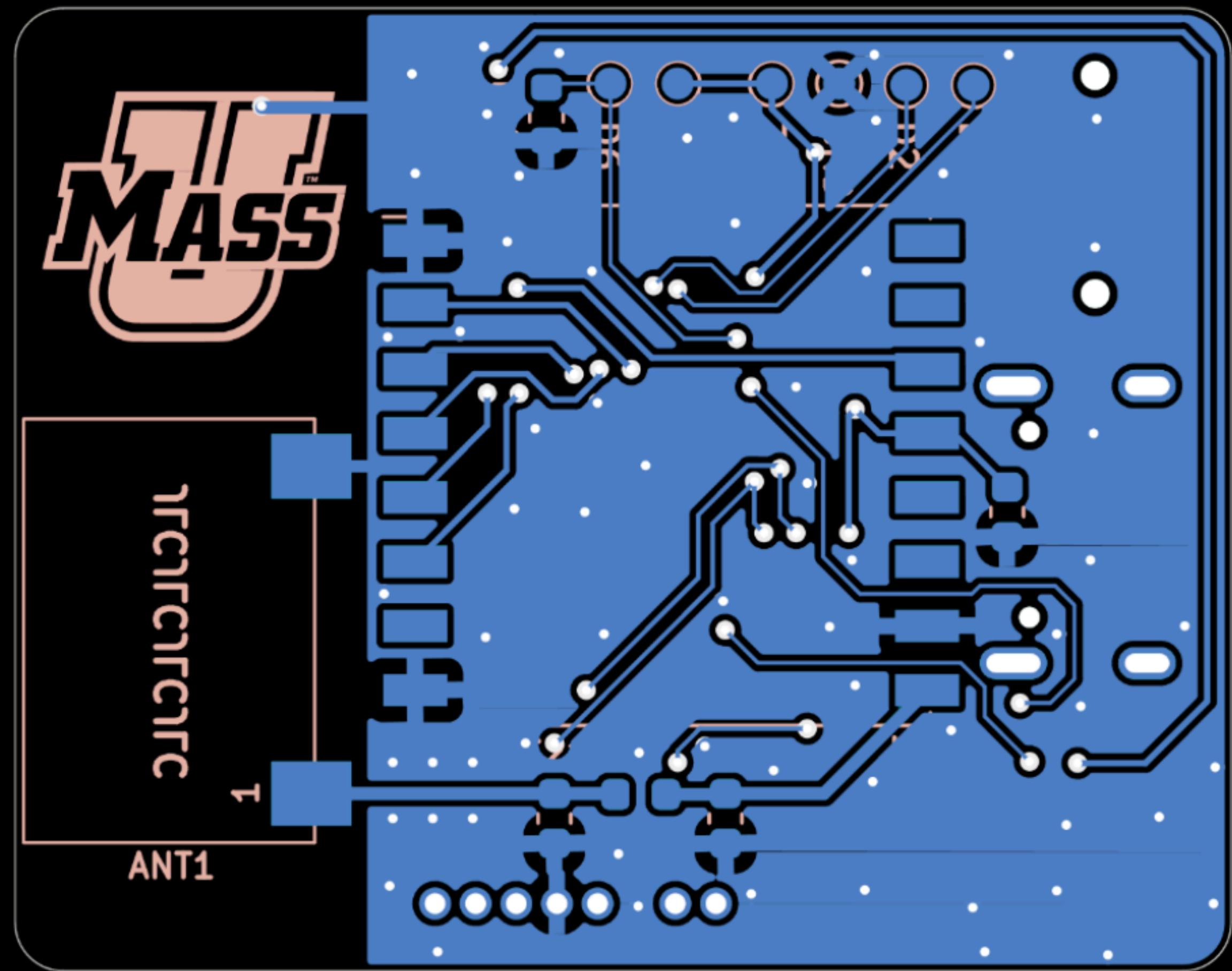
30mm

Front



38mm

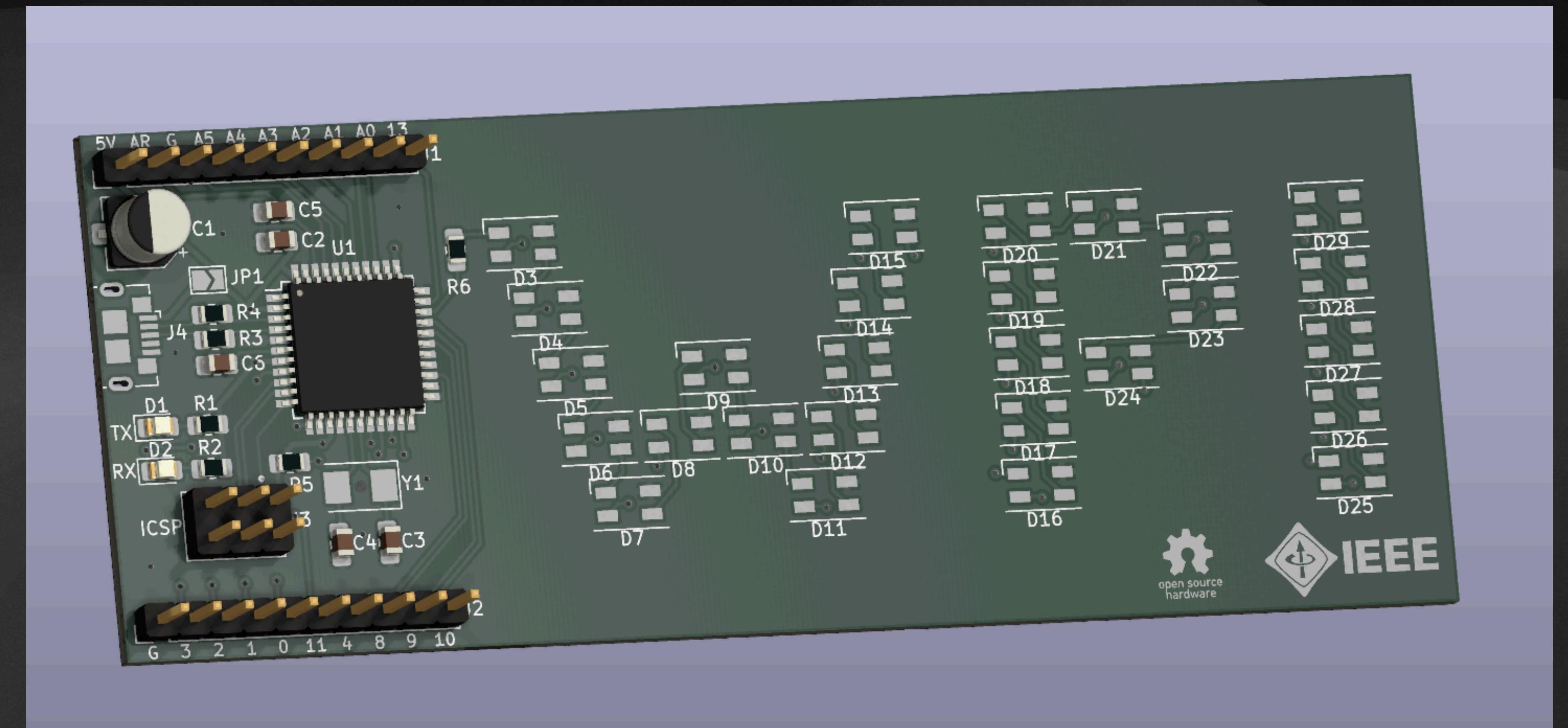
Back



hardware design process

walkthrough

1. Research and Design
2. Schematic Capture
3. Layout
- 4. Routing**
5. Order
6. Assembly

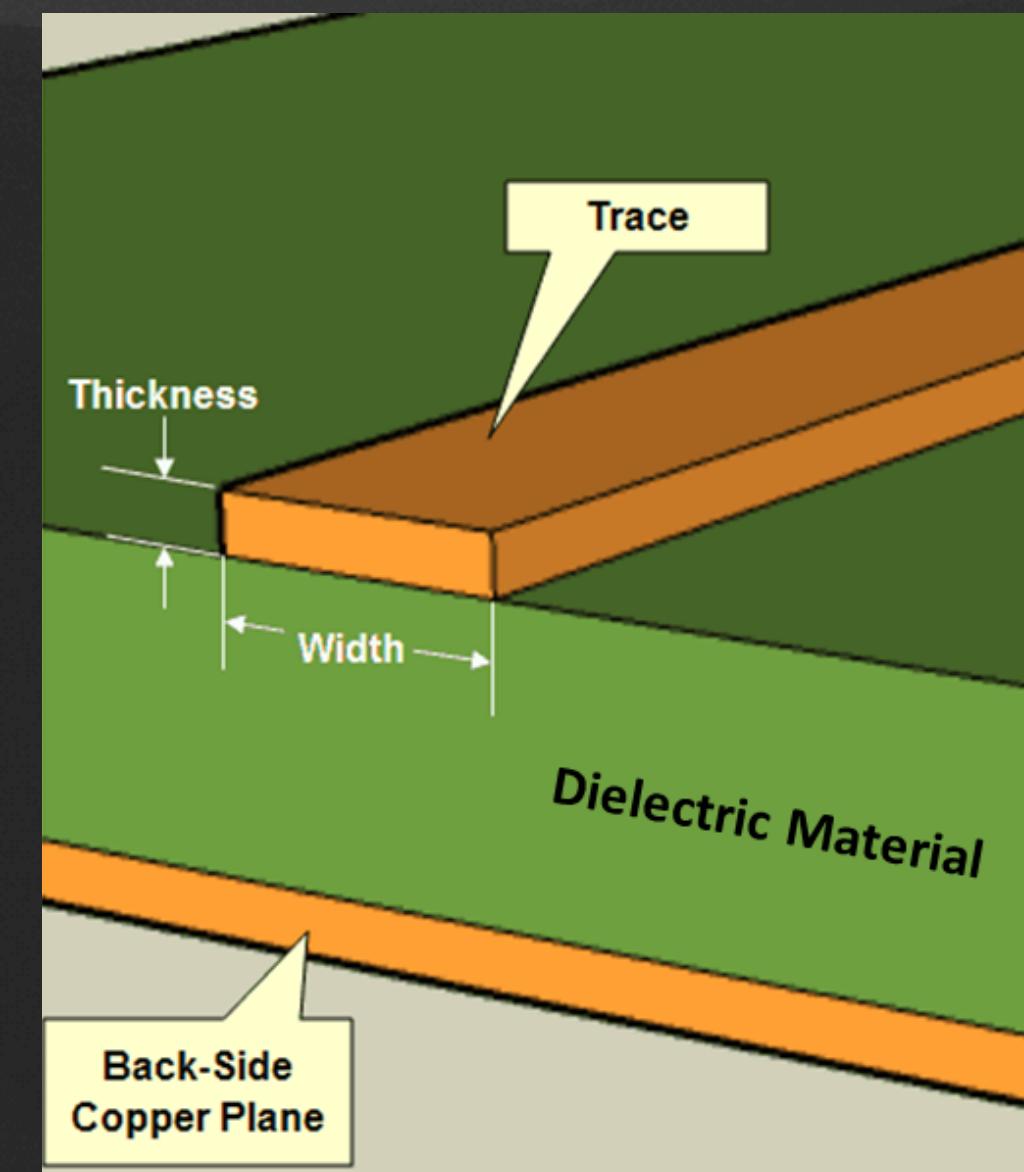


routing process

- Once you ‘untangle’ the nets, you can begin routing
- A good first step is to **disable ground nets**
- Common practice to fill unused space on the board with a ground pour, this means less routing
- Important parameter here: **trace width**
- KiCad default is fine for signal traces
- Power traces need more careful consideration
- DigiKey has a great calculator for this!

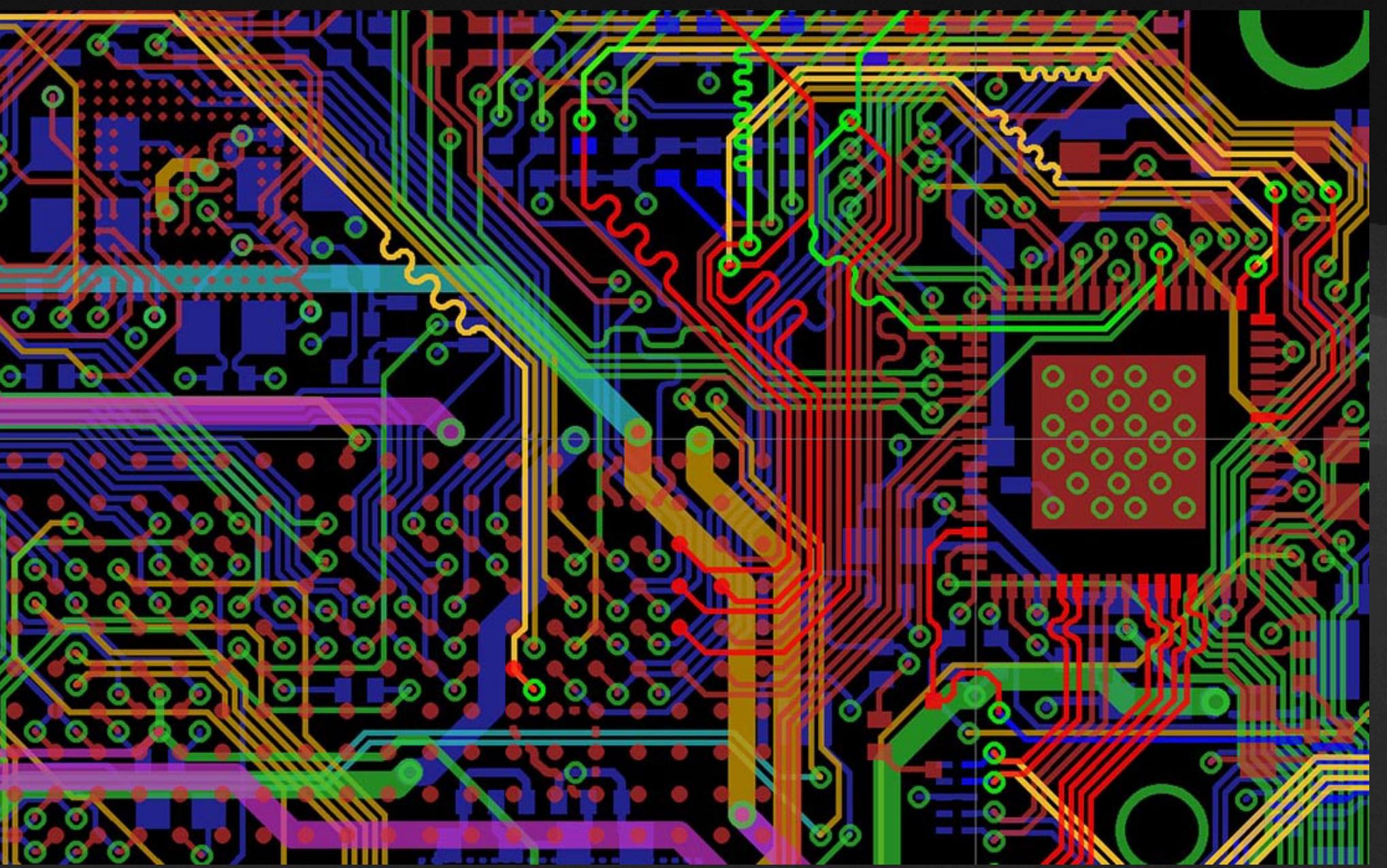
IPC Recommended Track Width For 1 oz cooper PCB and 10 °C Temperature Rise

Current/A	Track Width(mil)	Track Width(mm)
1	10	0.25
2	30	0.76
3	50	1.27
4	80	2.03
5	110	2.79
6	150	3.81
7	180	4.57
8	220	5.59
9	260	6.60
10	300	7.62



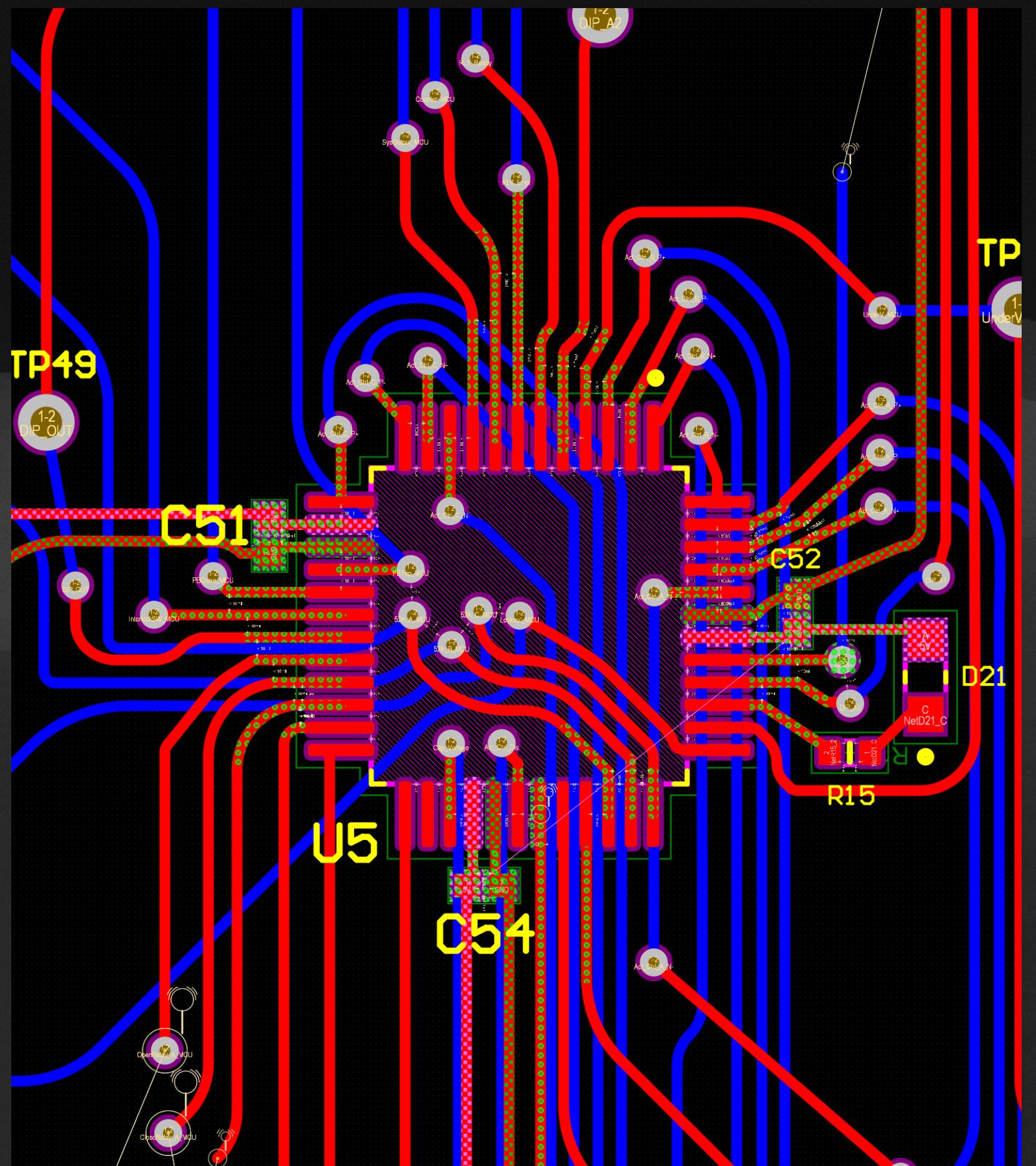
routing process

- Use vias to cross intersections
- Avoid long, looping traces
 - EMI is a consideration here
- Place similar traces next to one another
- Certain traces need special attention
 - Any signal that is high speed or differential
- Vcc and GND should always be far apart



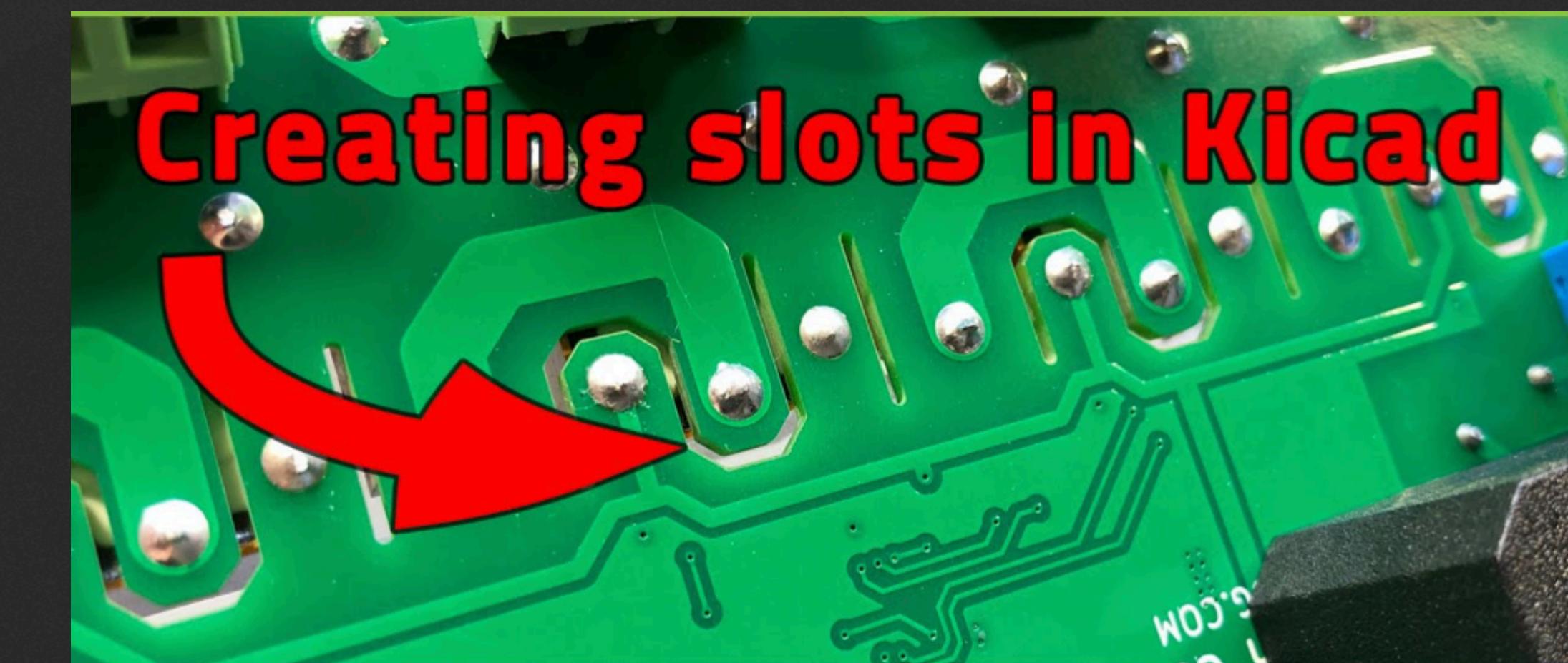
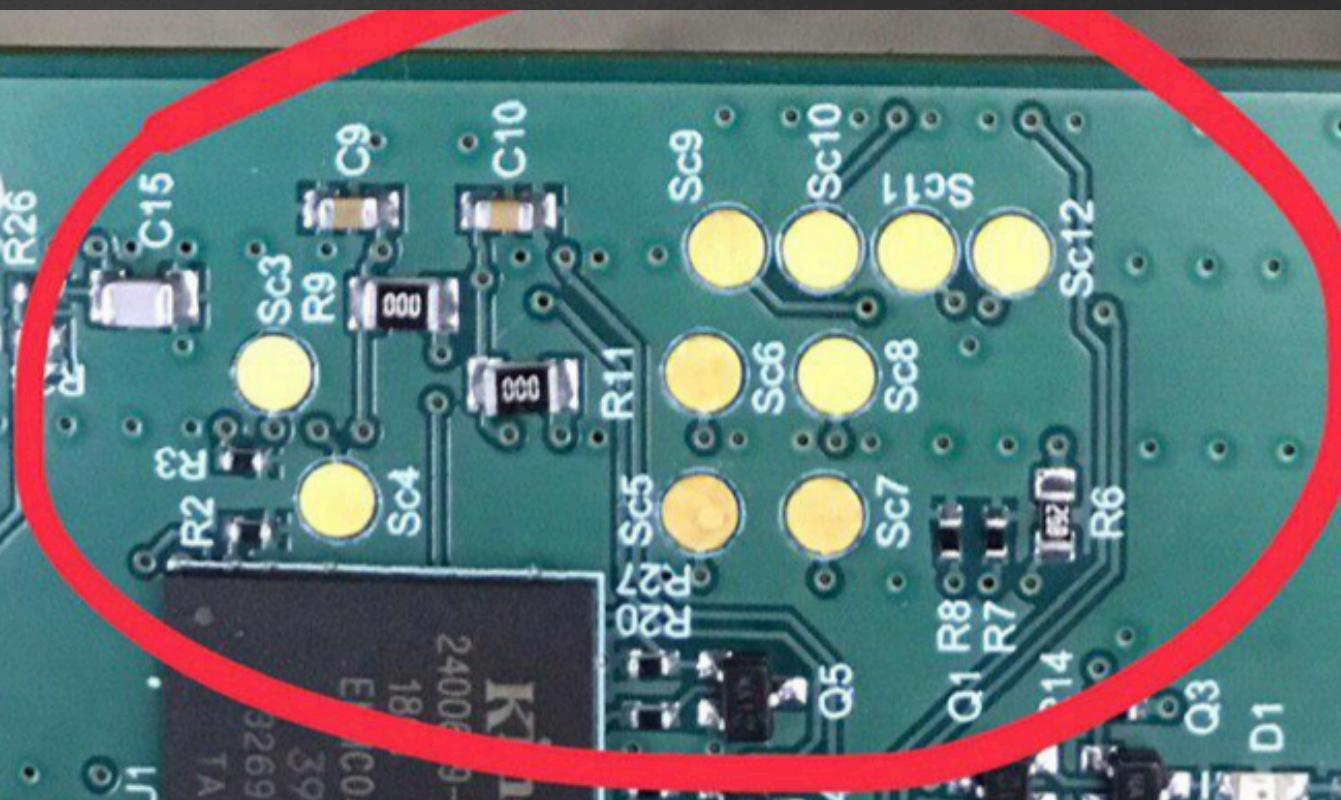
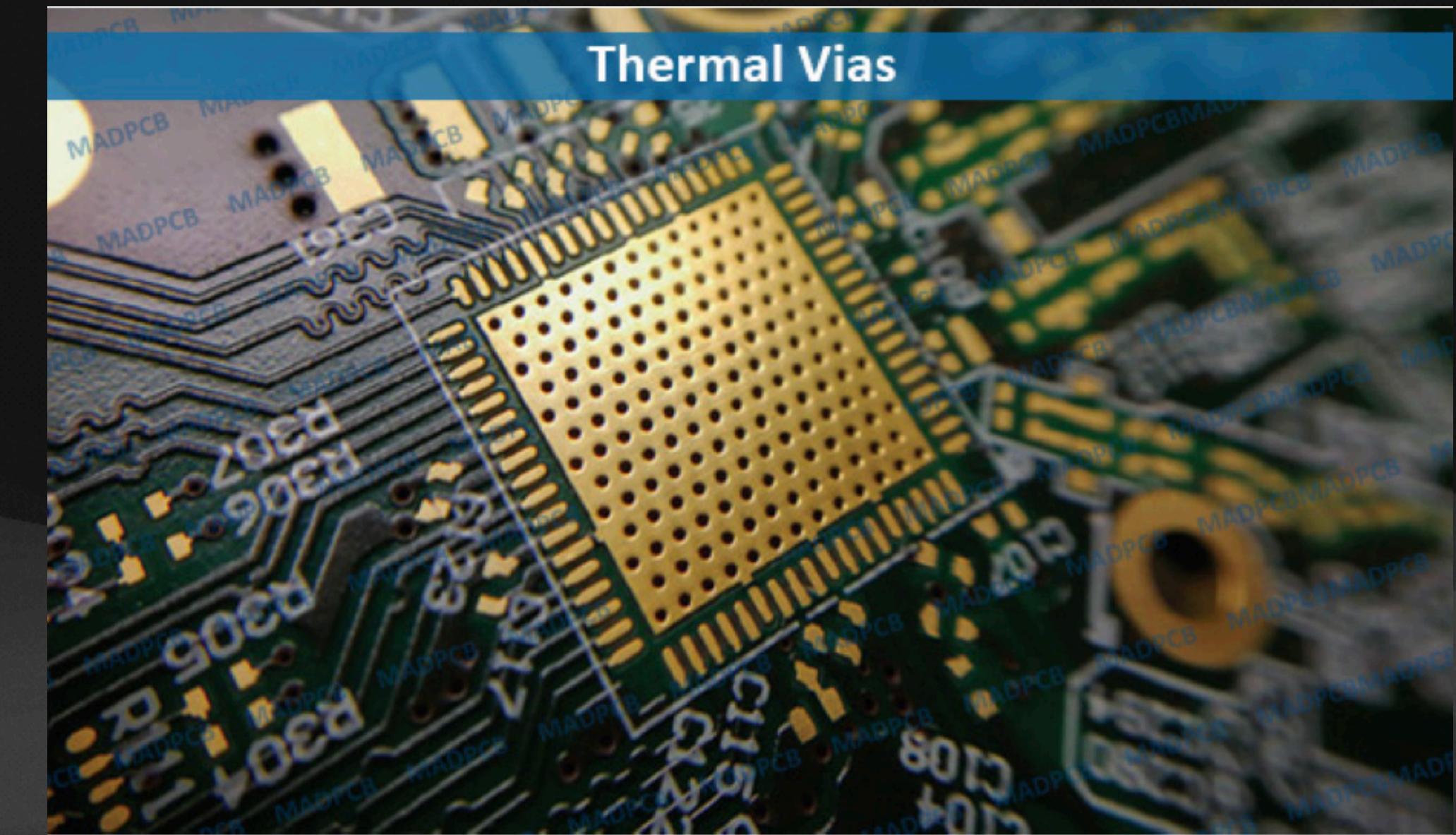
routing vias

- Common practice to have vias under microcontroller
- Route traces on other layers
- Microcontroller usually has high density of traces, will have more complicated routing than rest of board



routing considerations

- Thermal vias/thermal relief pads
- Isolation of high voltages (slots)
- Breakout/test points

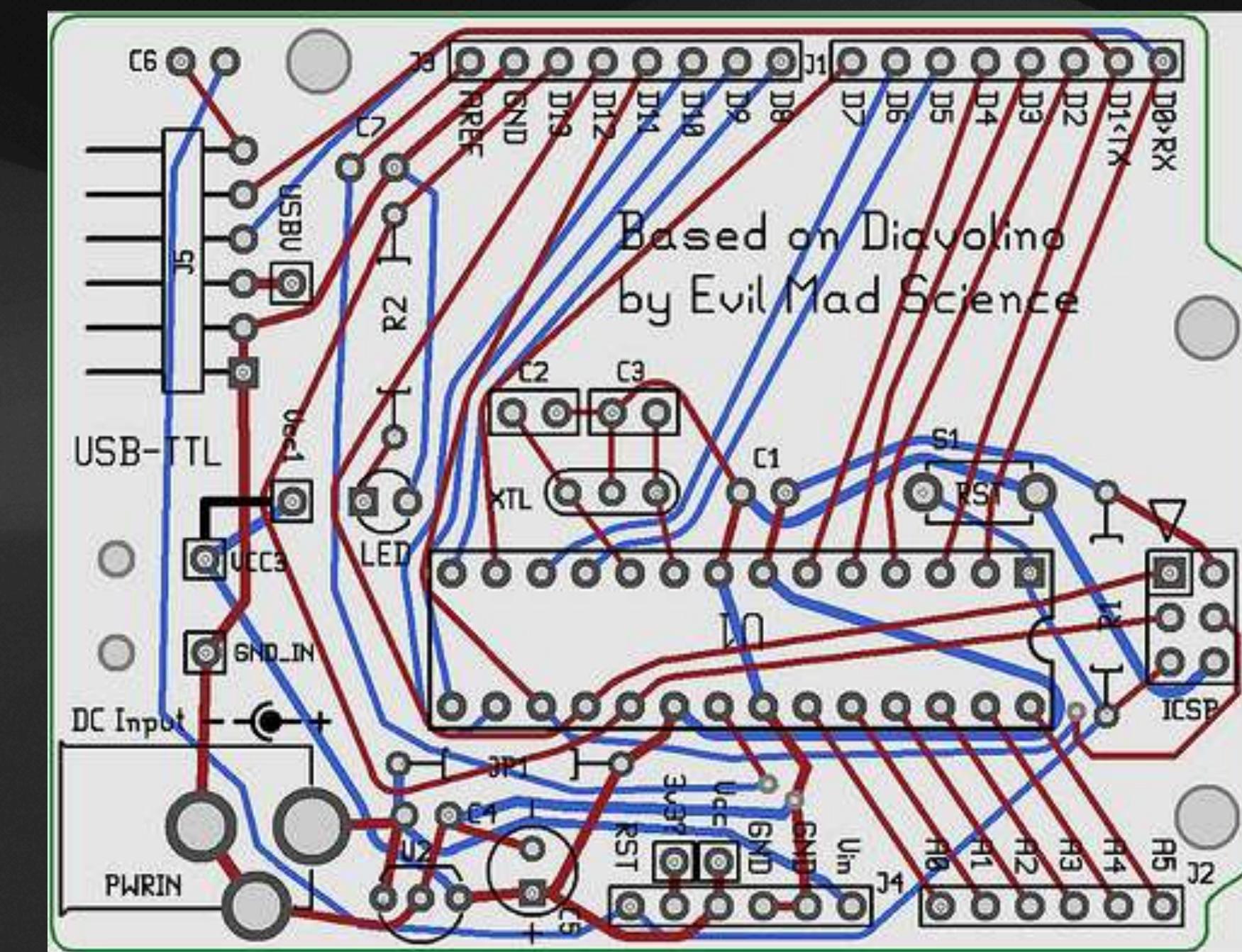
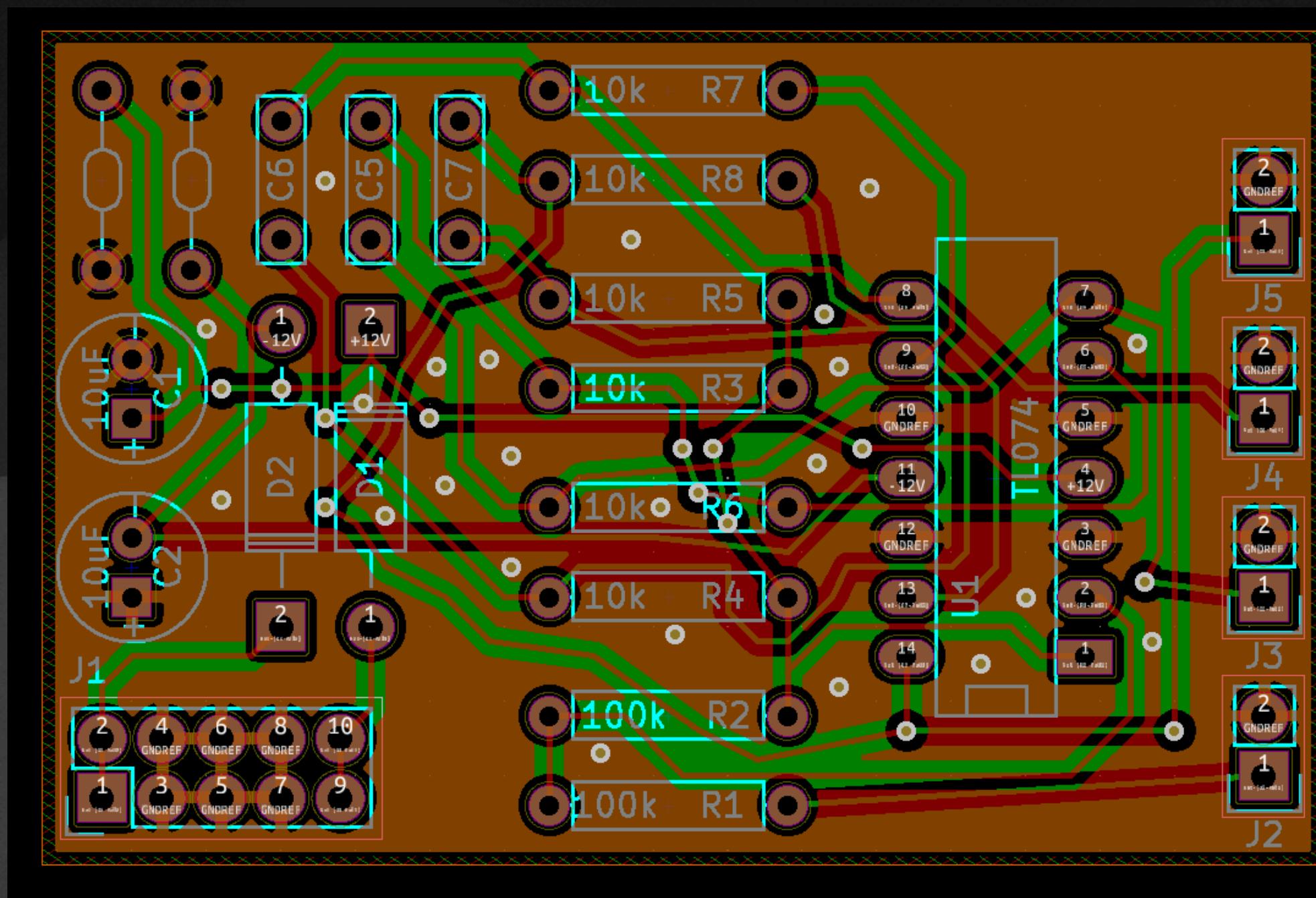


routing

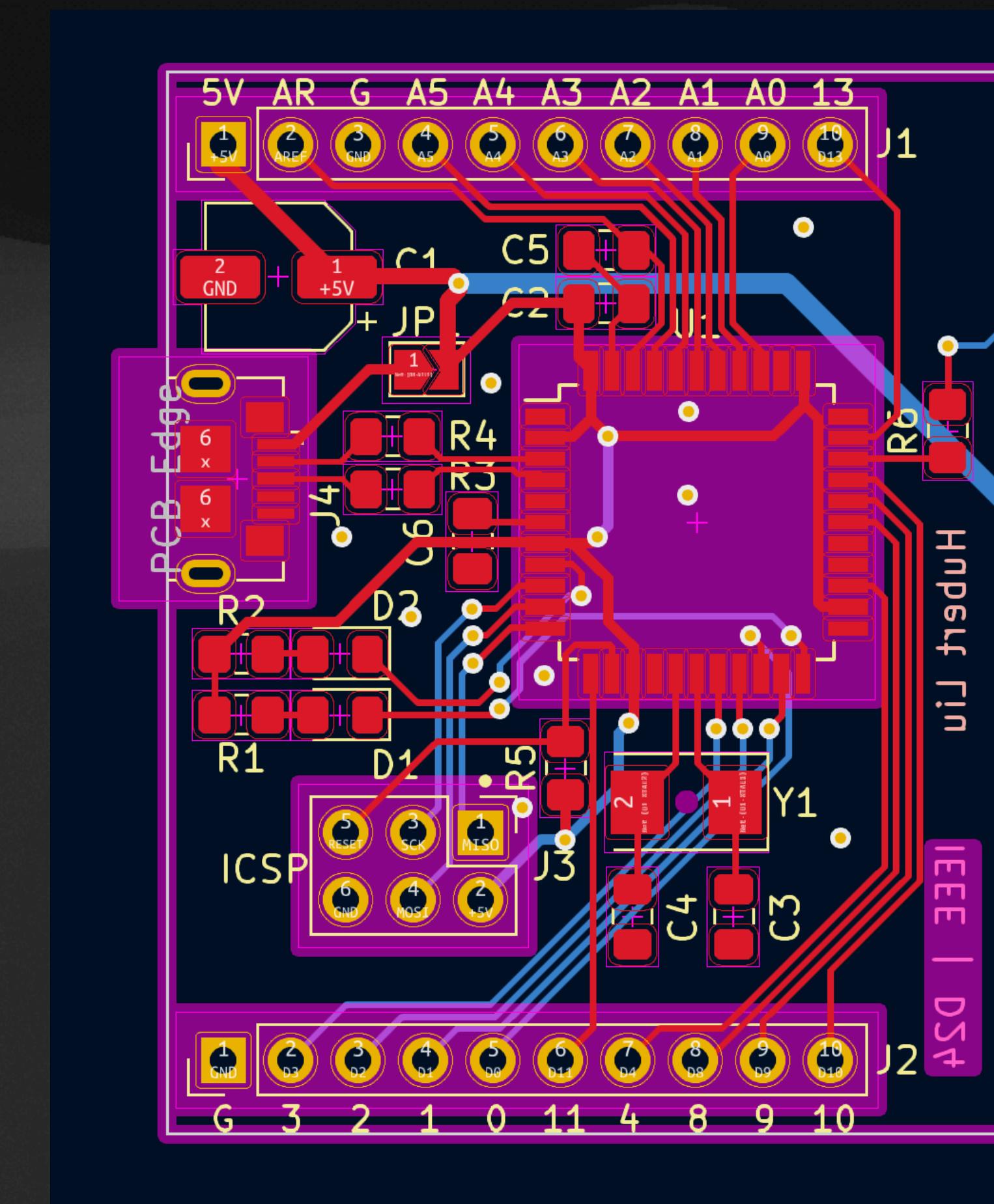
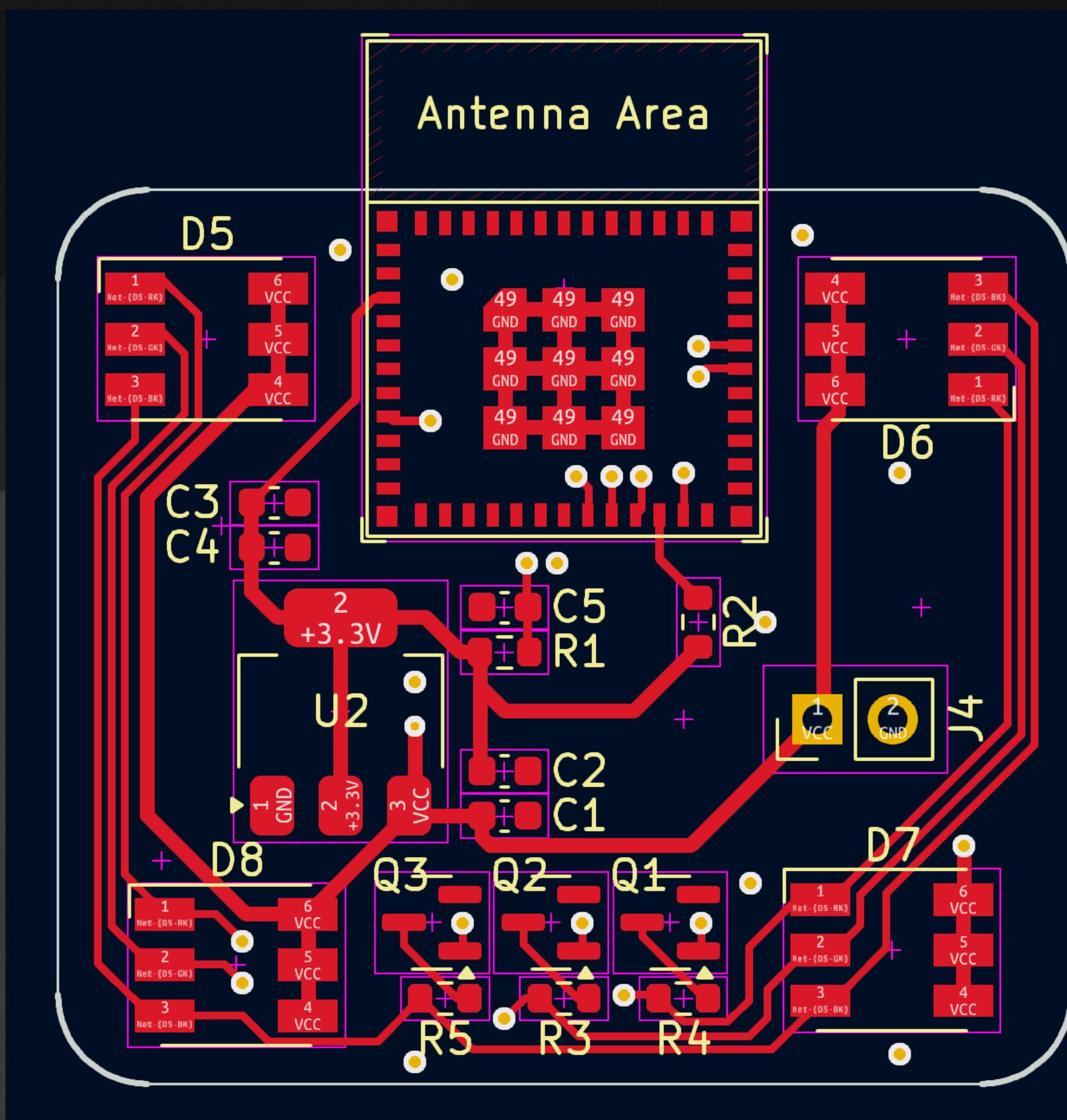
EMI

- Large ground planes -- Minimize impedance
- Separate analog, digital, and high-speed components
- Connect all components -- Avoid unwanted antennas
- Minimize signal lengths
- Avoid right-angles (including vias)
- Shielding and Filtering

routing the bad



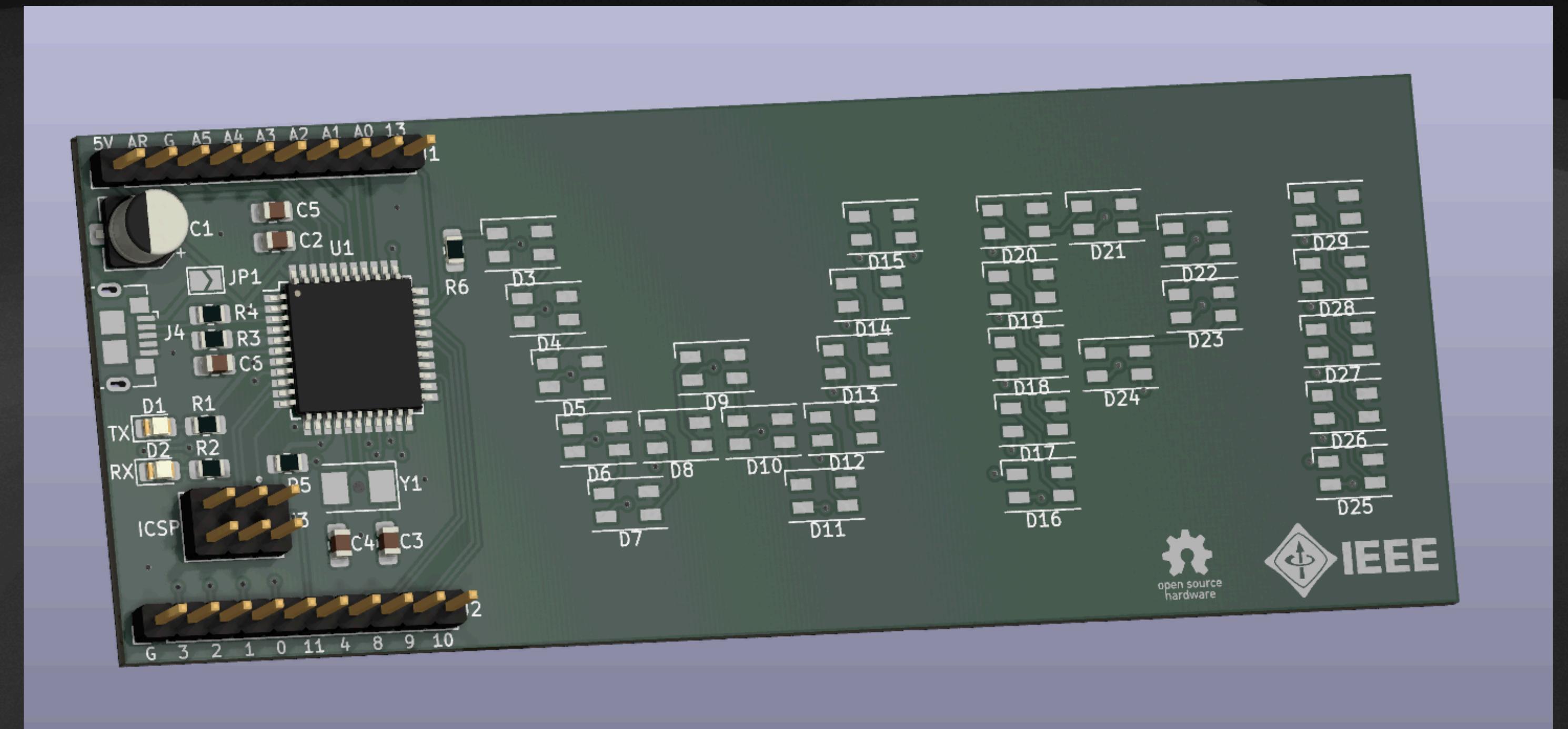
routing the good



hardware design process

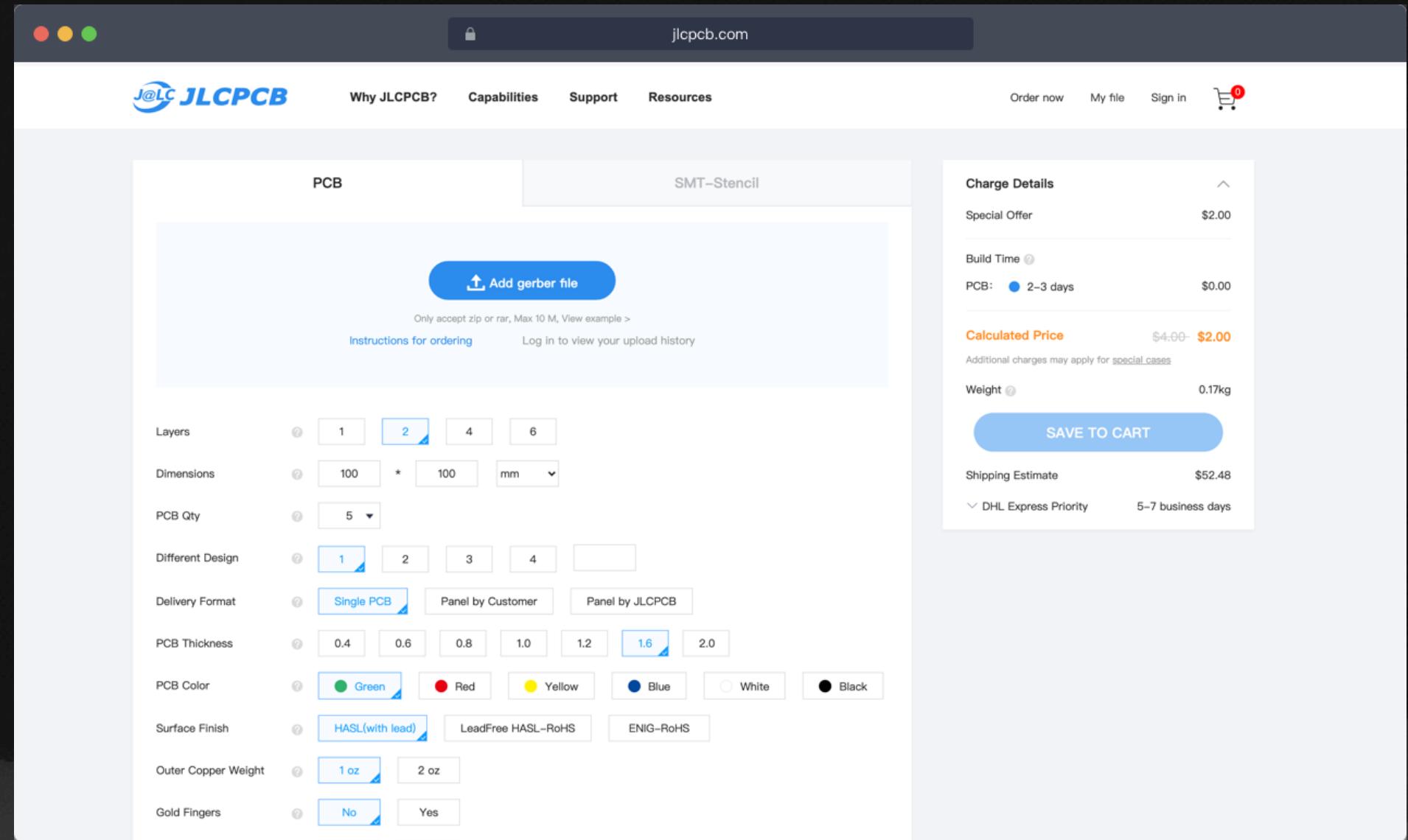
walkthrough

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2. Schematic Capture
3. Layout
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- 5. Order**
6. Assembly

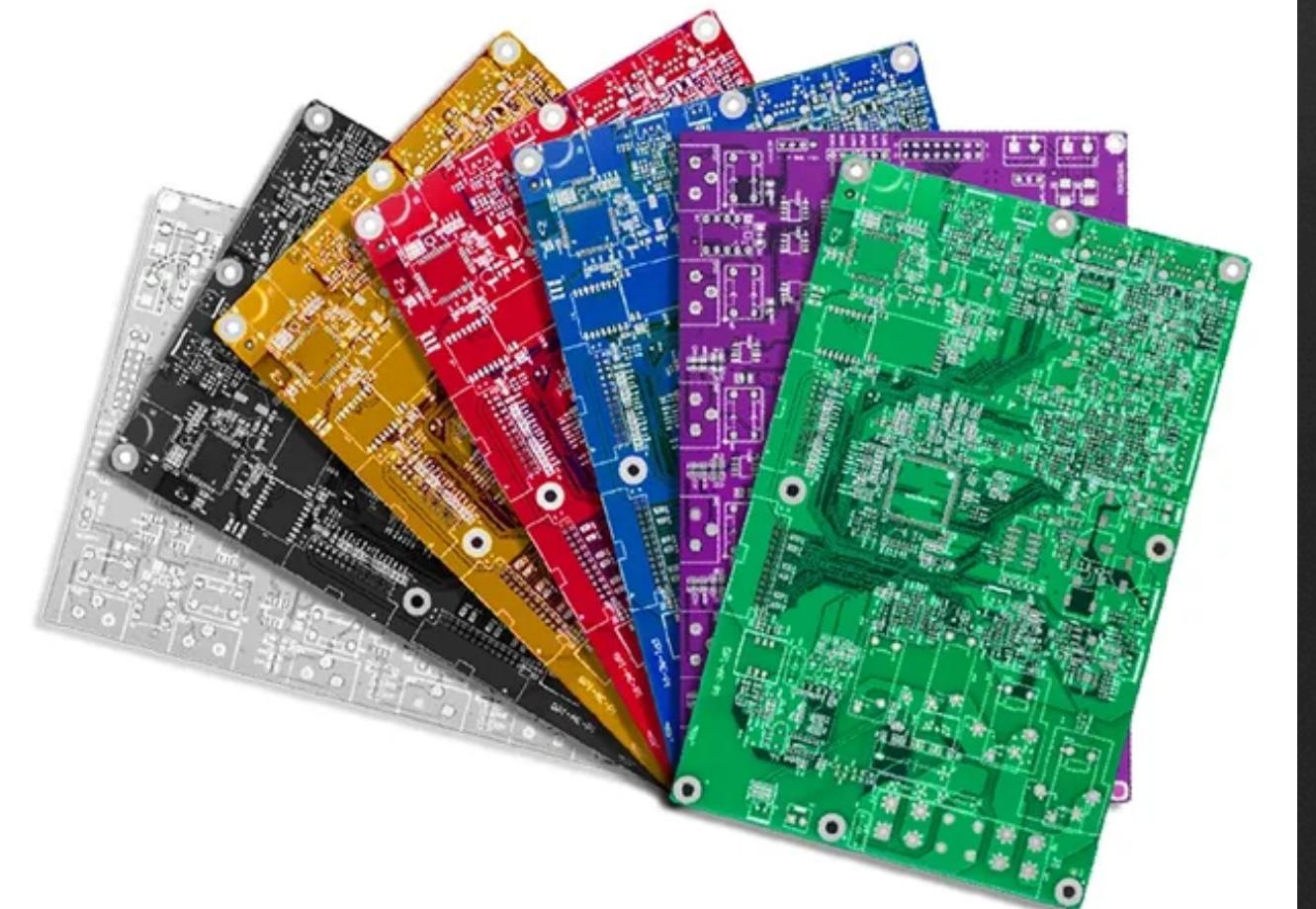


ordering your board process

- Run DRC (design rules check) using fab's specified tolerances
- Export Gerber files in KiCad, upload to fab website and specify options (stencil if needed)
- If your board violates minimum tolerances, your order will be blocked
- Chinese fabs are ridiculously cheap and usual lead time is about a week
- Order parts from your favorite distributor.



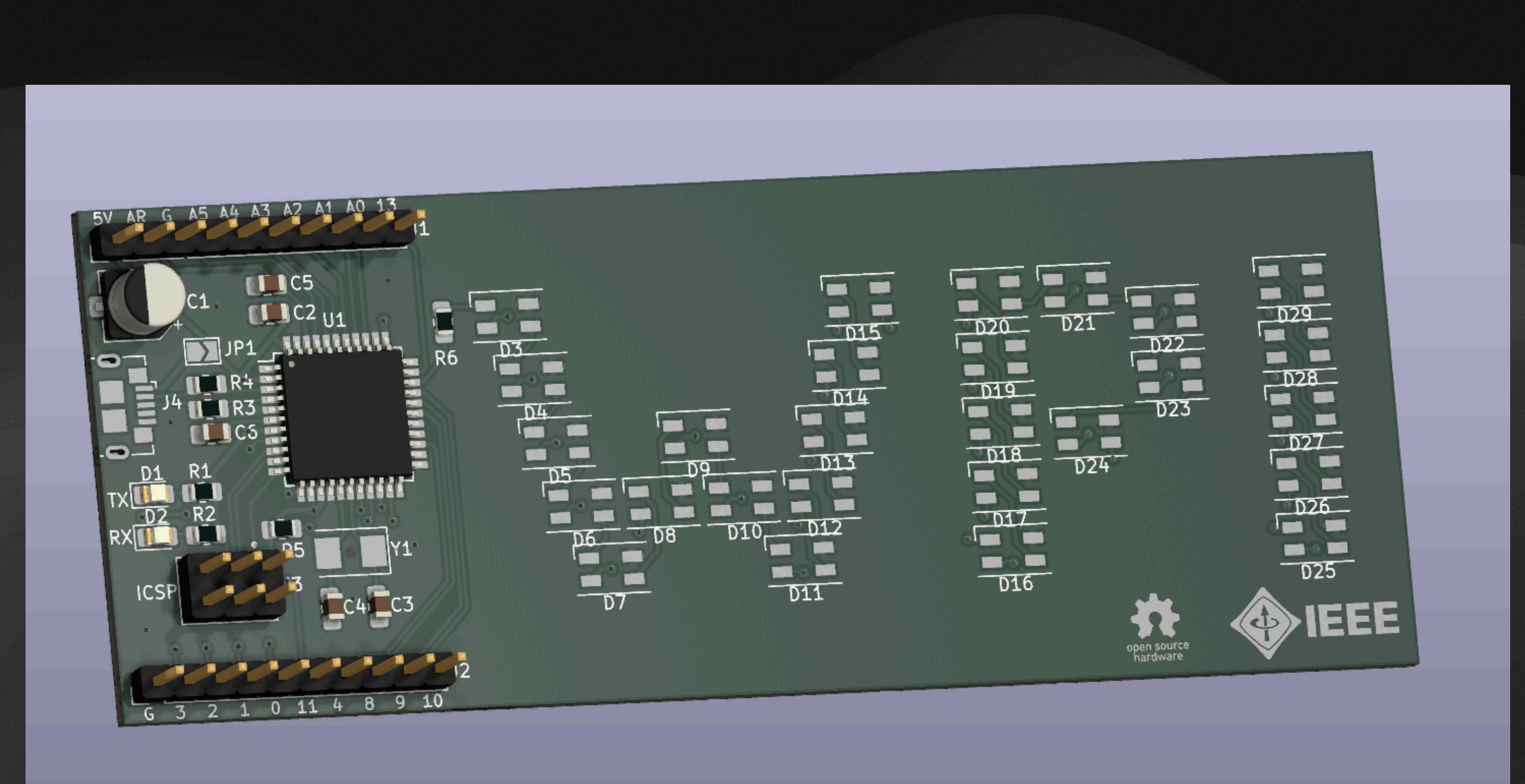
J@LC JLCPCB



hardware design process

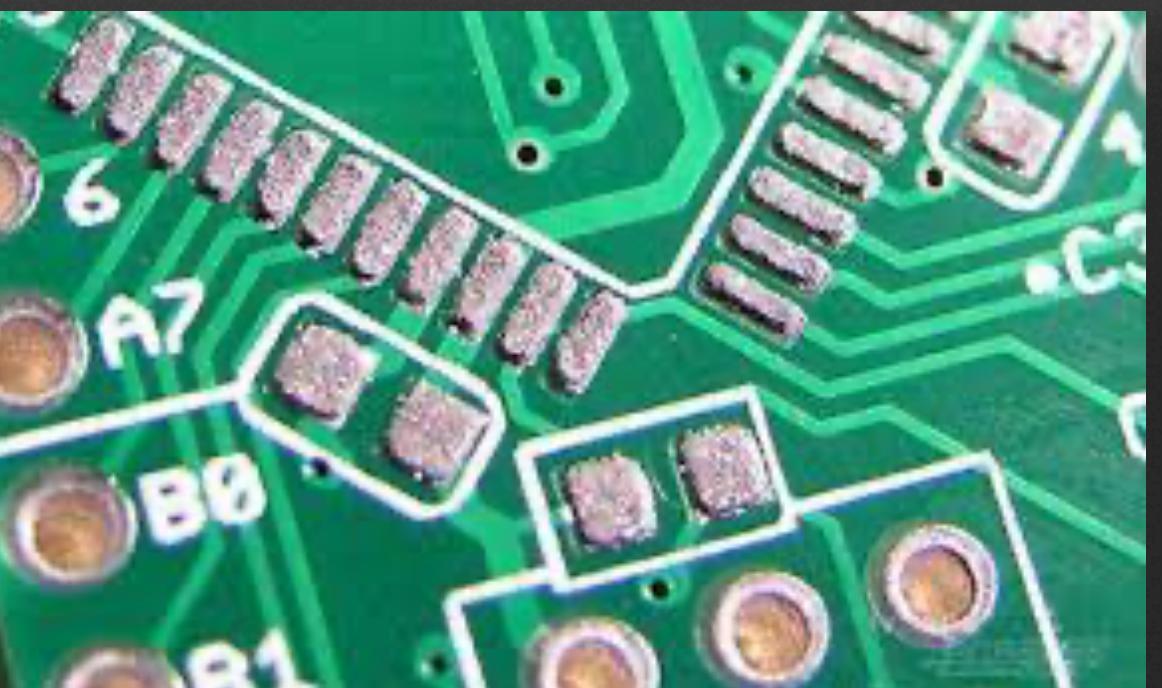
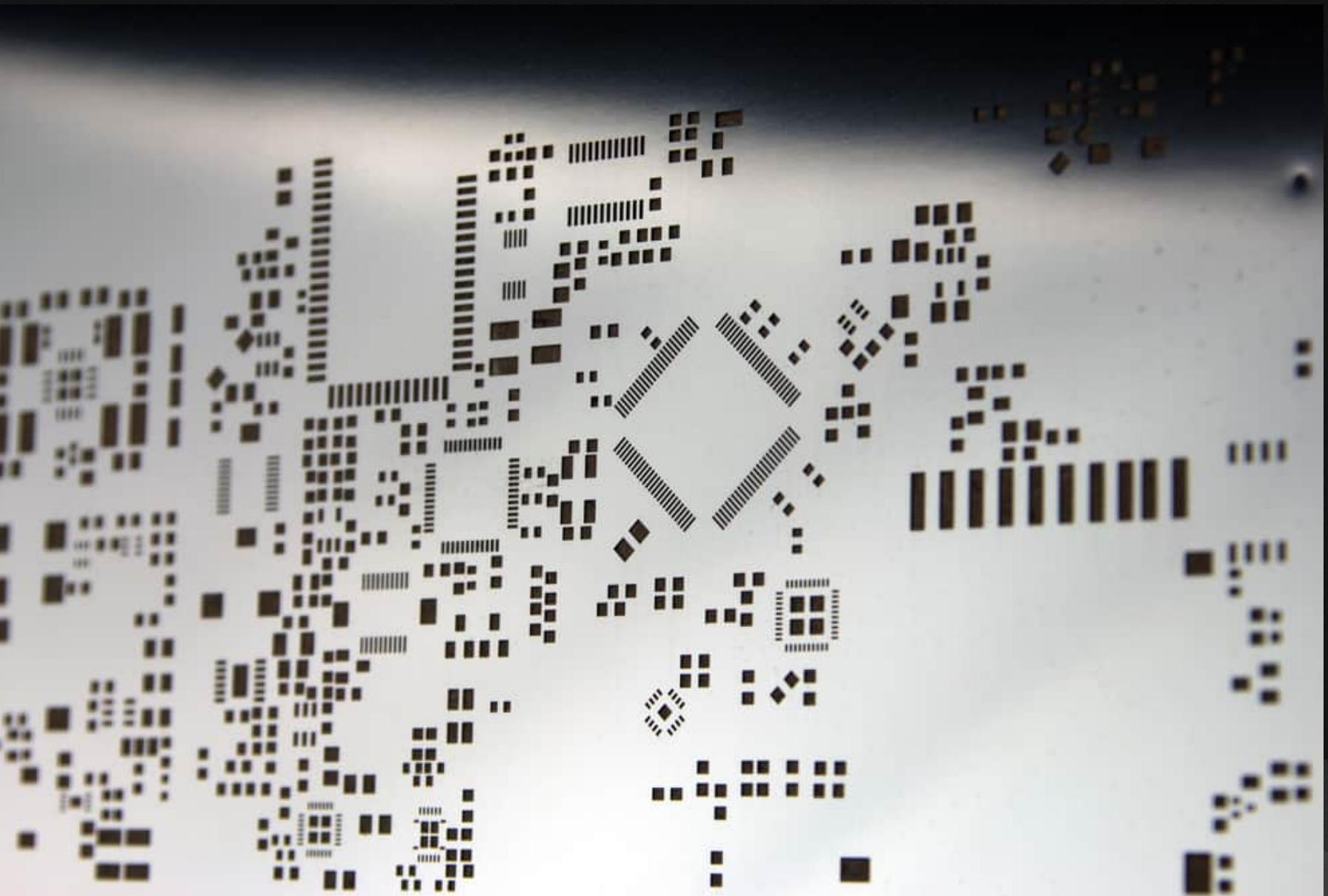
walkthrough

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assembly process

- Most SMT designs can most easily be soldered using a stencil
- Stencil has holes where component pads are
- Solder paste spread over stencil
- Components placed on solder paste
- Board place in reflow oven
- Yay it's finished!

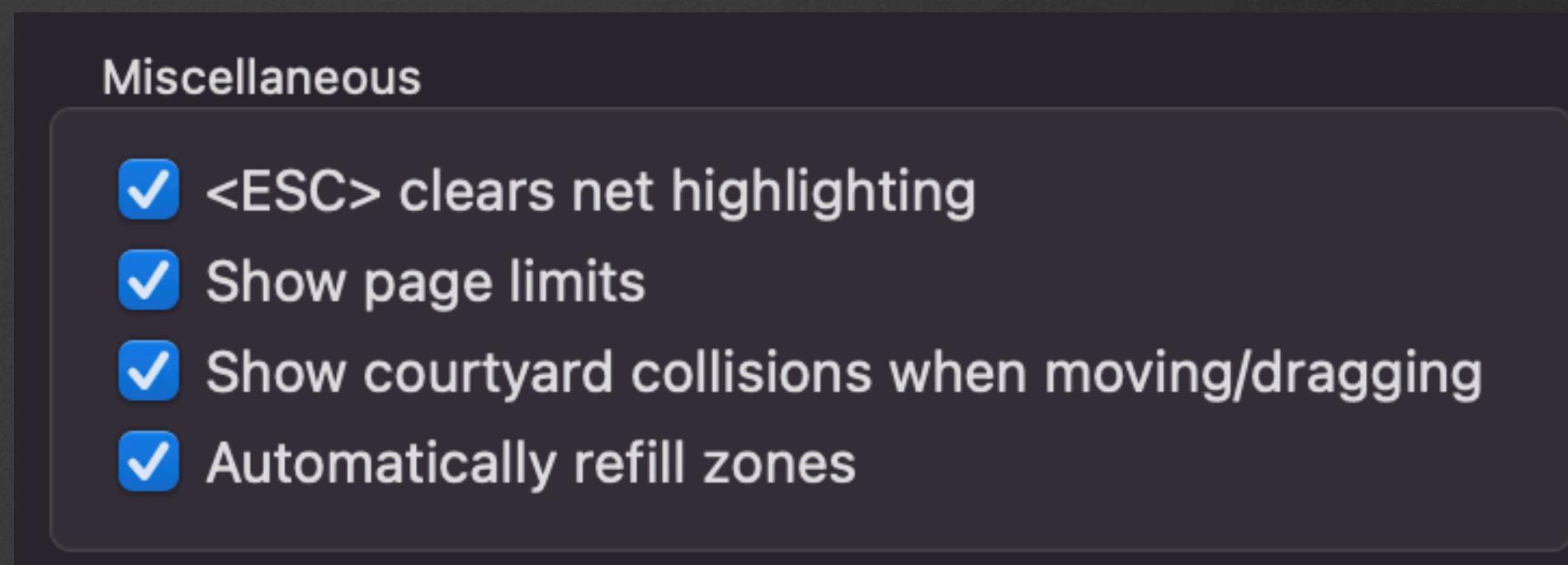


KiCad Time!

kicad: settings

configure drc, autofill zones

- File -> Board Setup... -> Design Rules
 - Should be setup correctly in downloaded files
- Disable ground nets
- Automatically refill zones
- Preferences -> Editing Options



Copper		
	Minimum clearance:	0.127 mm
	Minimum track width:	0 mm
	Minimum connection width:	0 mm
	Minimum annular width:	0.1 mm
	Minimum via diameter:	0.5 mm
	Copper to hole clearance:	0.254 mm
	Copper to edge clearance:	0.2 mm
Holes		
	Minimum through hole:	0.3 mm
	Hole to hole clearance:	0.25 mm
uVias		
	Minimum uVia diameter:	0.2 mm
	Minimum uVia hole:	0.1 mm
Silkscreen		
	Minimum item clearance:	0 mm
	Minimum text height:	0.8 mm

kicad: cheatsheet

useful keybinds

- Left click to move stuff
- Right click to move viewpoint

KiCad cheatsheet

<http://kicad-pcb.org/help/documentation/>

1) Create a project
File → New Project → New Project

2) Eeschema : draw the schematic

Add components :	A
Move item ¹ :	↑ + M
Grab item ¹ :	↑ + G
Copy item :	↑ + C
Copy selection :	↑ Shift + ↗
Delete item :	↑ + Del
Delete selection :	Ctrl + ↑ Shift + ↗
Rotate item :	↑ + R
Mirror item :	↑ + X / Y
Add wires :	W
Edit properties :	E
Edit value :	V
Add power symbols :	P
Add no-connect :	Q
Add text :	T
Add labels :	L
List of shortcuts :	?

¹grab keeps connections, move doesn't

How to load the new library in CvPcb :
Preferences → Footprint libraries
Append with wizard
Select your .pretty folder

→ Generate netlist

5) Pcbnew : design the layout

Design Rules → Design Rules + Layers Setup
→ Read netlist

Select top layer : ↑ PgUp
Select bottom layer : ↓ PgDn
Move item¹ : → + M
Grab item¹ : → + G
Copy item : → + C
Rotate item : → + R
Add tracks : X
Add via : V
Switch posture : Q
Switch track width : W
Drag track : D
Fill zones : B
3D viewer : Alt (+ ↑ Shift) + 3
¹grab keeps connections, move doesn't
(Only for AZERTY keyboards)

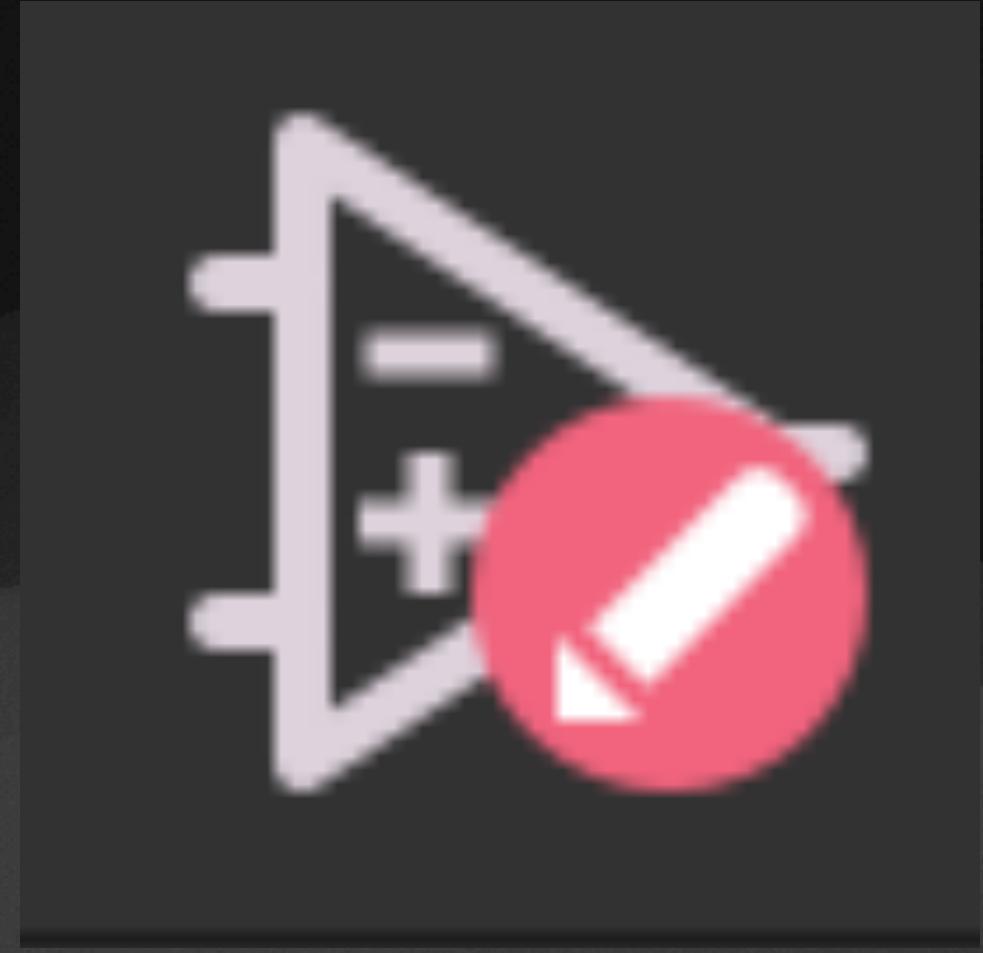
6) Export Gerbers
File → Plot
Generate Drill File + Plot → Check result using GerbView

Anthony Gautier - <http://silica.io>

kicad: schematic capture

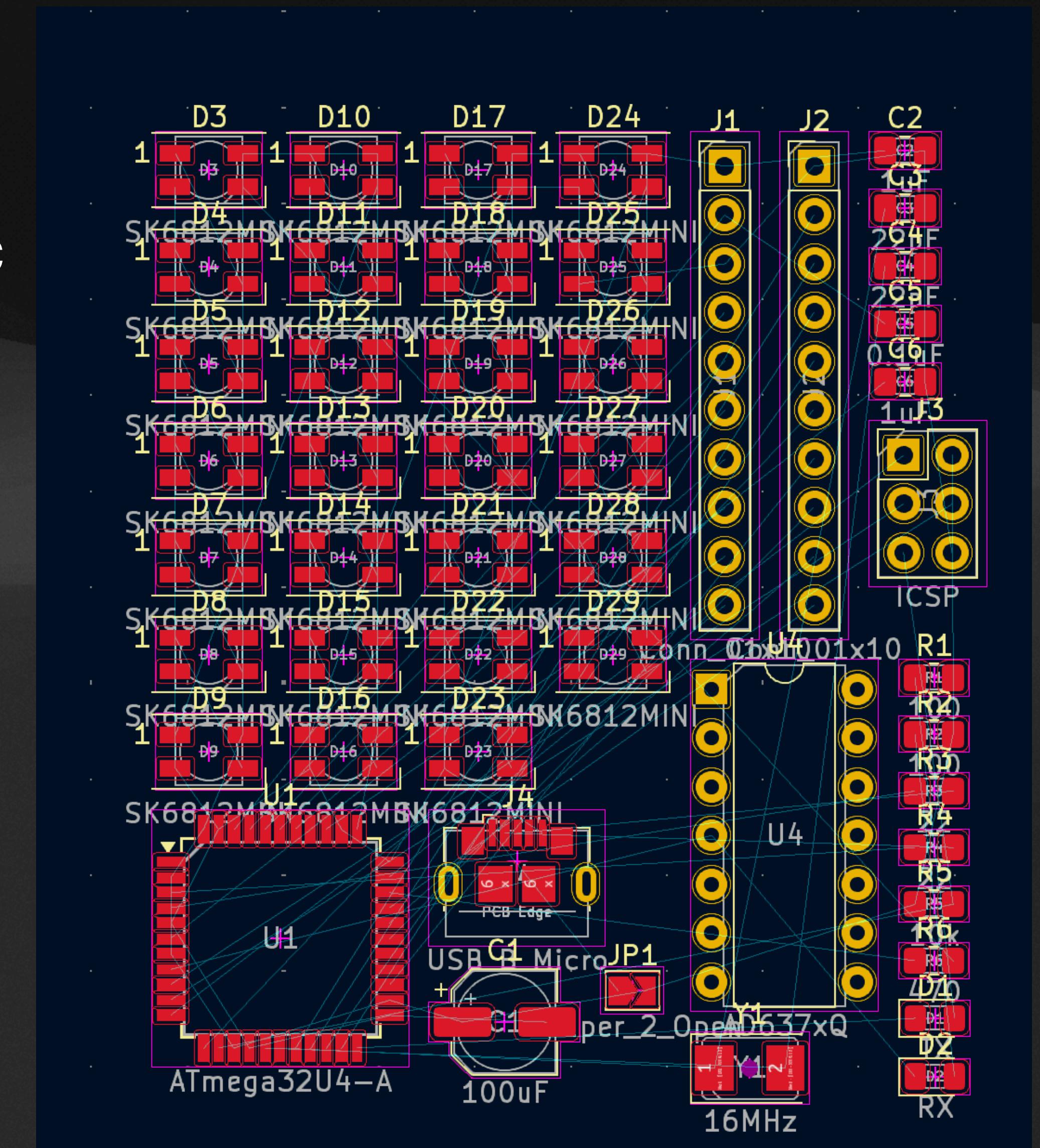
finding parts

- Almost all of the needed parts are in the symbol library
- Add symbol to the schematic



kicad: layout basics

- Update the PCB after changing the schematic
- Tools -> Update PCB from schematic (F8)
- Places all the footprints *somewhere*
- It is YOUR job to figure out how to reposition the components to make routing easier



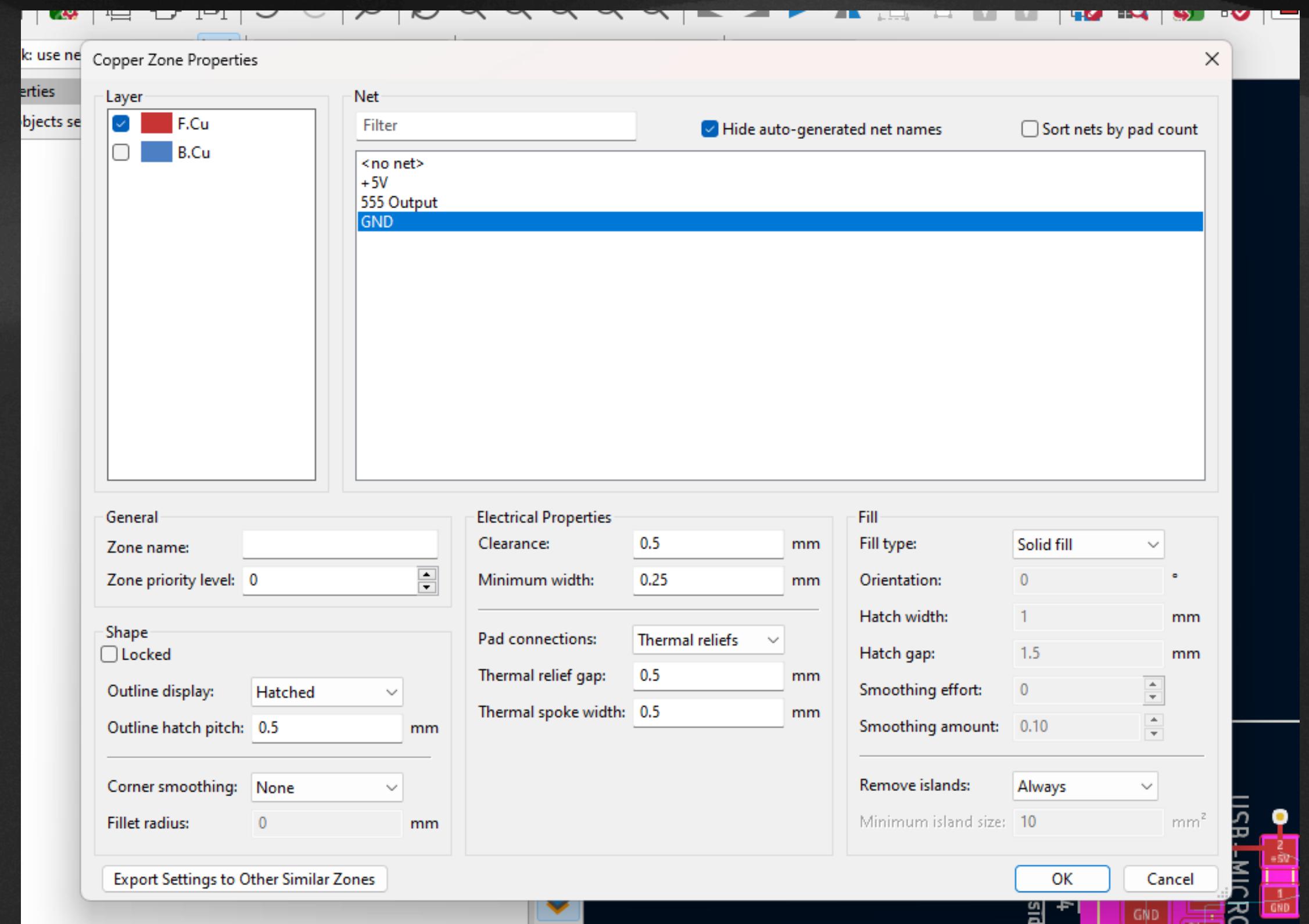
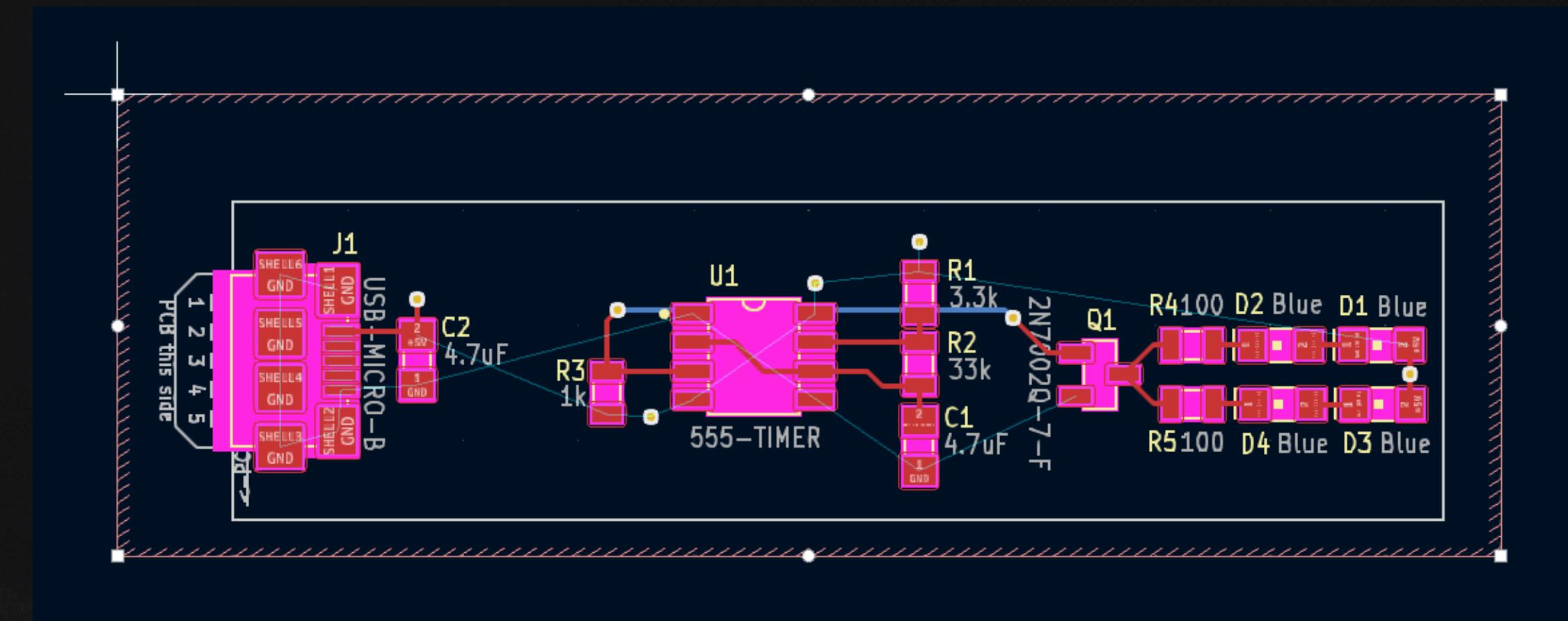
kicad: routing basics

- Press X to route a single trace
- Follow nets to see what needs to be connected
- Use vias to simplify design

kicad: pours

basics

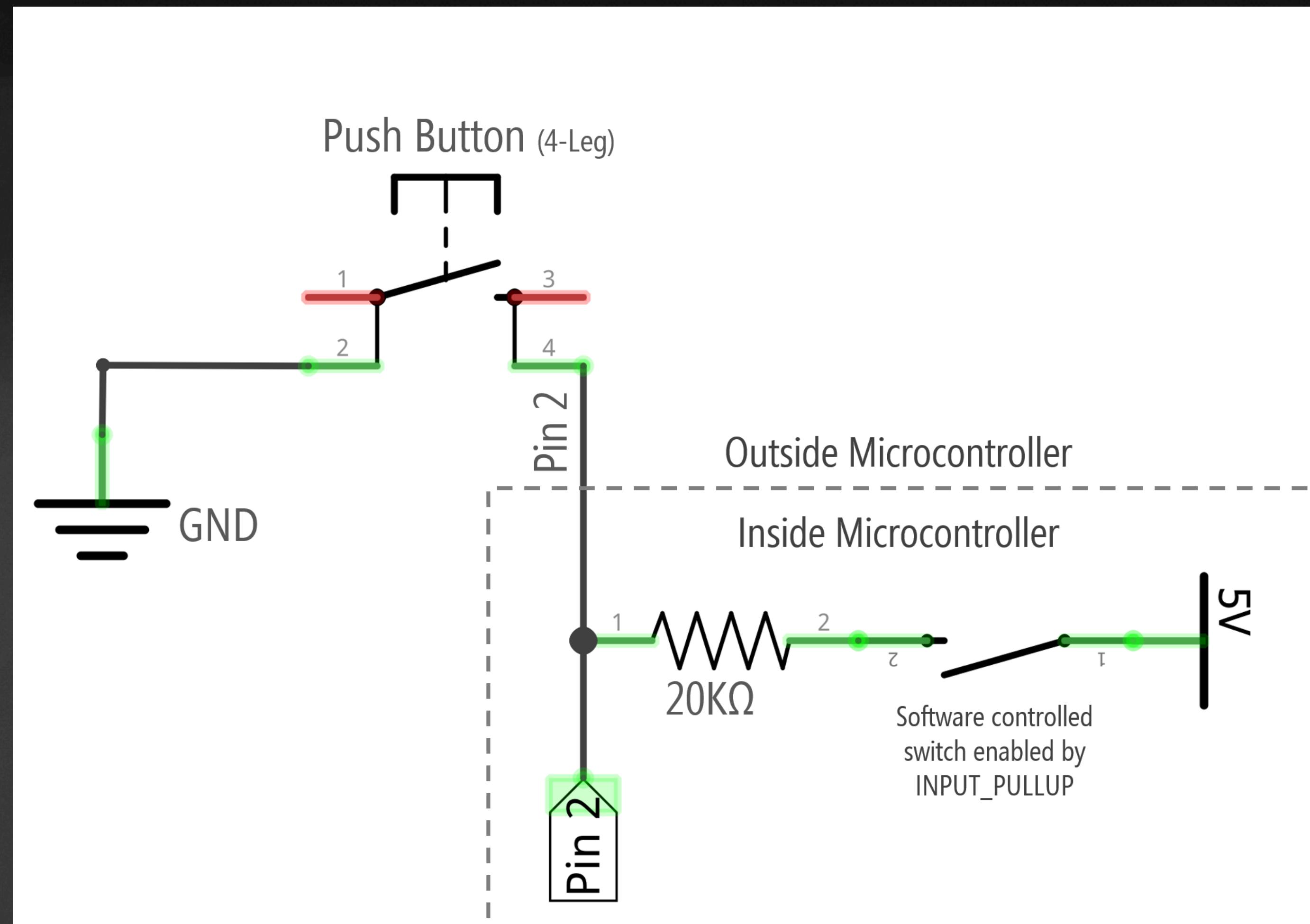
- You will need to use multiple ground pours and Vcc pours
- This will help simplify a lot of routing
- Click “Add filled zone”
- Select the correct layer and net
- Draw a zone around the desired area



practice button

- You'll be adding a button to the starter board!
- Schematic?
- Layout?
- Routing?

button schematic



button

SKU

**PTS647 Series
4.5 mm Tact Switch**

Features/Benefits

- Compact size 4.5 x 4.5 mm
- SMT terminals
- Different actuator heights
- Choice of actuation forces
- Tape & reel

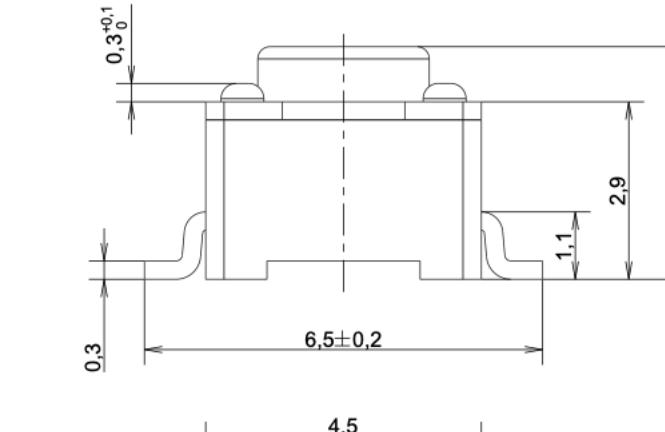
Typical Applications

- Consumer
- Industrial control panels
- Computer products

Tactile Switches

B

Part Number	Operating Force (gf)	Life	Height (H)
PTS647 SN38 SMTR2 LFS	100 +/- 50	100,000	3.8 mm
PTS647 SM38 SMTR2 LFS	180 +/- 50	100,000	3.8 mm
PTS647 SK38 SMTR2 LFS	250 +/- 50	100,000	3.8 mm
PTS647 SN50 SMTR2 LFS	100 +/- 50	100,000	5.0 mm
PTS647 SM50 SMTR2 LFS	180 +/- 50	100,000	5.0 mm
PTS647 SK50 SMTR2 LFS	250 +/- 50	100,000	5.0 mm
PTS647 SN70 SMTR2 LFS	100 +/- 50	100,000	7.0 mm
PTS647 SM70 SMTR2 LFS	180 +/- 50	100,000	7.0 mm
PTS647 SK70 SMTR2 LFS	250 +/- 50	100,000	7.0 mm



PTS 647 SN50 SMTR2 LFS



DigiKey Part Number PTS647SN50SMTR2LFSTR-ND - Tape & Reel (TR)
PTS647SN50SMTR2LFSCT-ND - Cut Tape (CT)
PTS647SN50SMTR2LFSDKR-ND - Digi-Reel®

Manufacturer C&K

Manufacturer Product Number PTS 647 SN50 SMTR2 LFS

Description SWITCH TACTILE SPST-NO 0.05A 12V

Manufacturer Standard Lead Time 9 Weeks

Customer Reference

Detailed Description Tactile Switch SPST-NO Top Actuated Surface Mount

Datasheet  [Datasheet](#)

EDA/CAD Models [PTS 647 SN50 SMTR2 LFS Models](#)

Image shown is a representation only. Exact specifications should be obtained from the product data sheet.

Walkthrough