

# Essentials of PCB Design

03: Layout + Routing

# welcome back!

## schedule

### A-Term

<b>Tue, Sep. 24</b>	Basics of PCBs <b>6-7PM; SH 301</b>
<b>Thur, Sep. 26</b>	Designing your Project <b>6-7:30PM; SH 201</b>
<b>Tue, Oct. 1</b>	Layout + Routing <b>6-7:30PM; SH 201</b>
<b>Thur, Oct. 3</b>	Working with KiCad <b>6-7:30PM; SH 201</b>
<b>Mon, Oct. 7 - Fri, Oct. 11</b>	Office Hours <b>TBD; IEEE Lounge</b>

### B-Term

<b>Mon, Oct. 21 - Fri, Oct. 25</b>	Office Hours <b>TBD; IEEE Lounge</b>
<b>Fri, Oct. 25</b>	Boards Due <b>By 10PM</b>
<b>Tue, Nov. 5 (Wellness Day)</b>	Assembly <b>TBD; AK 113</b>

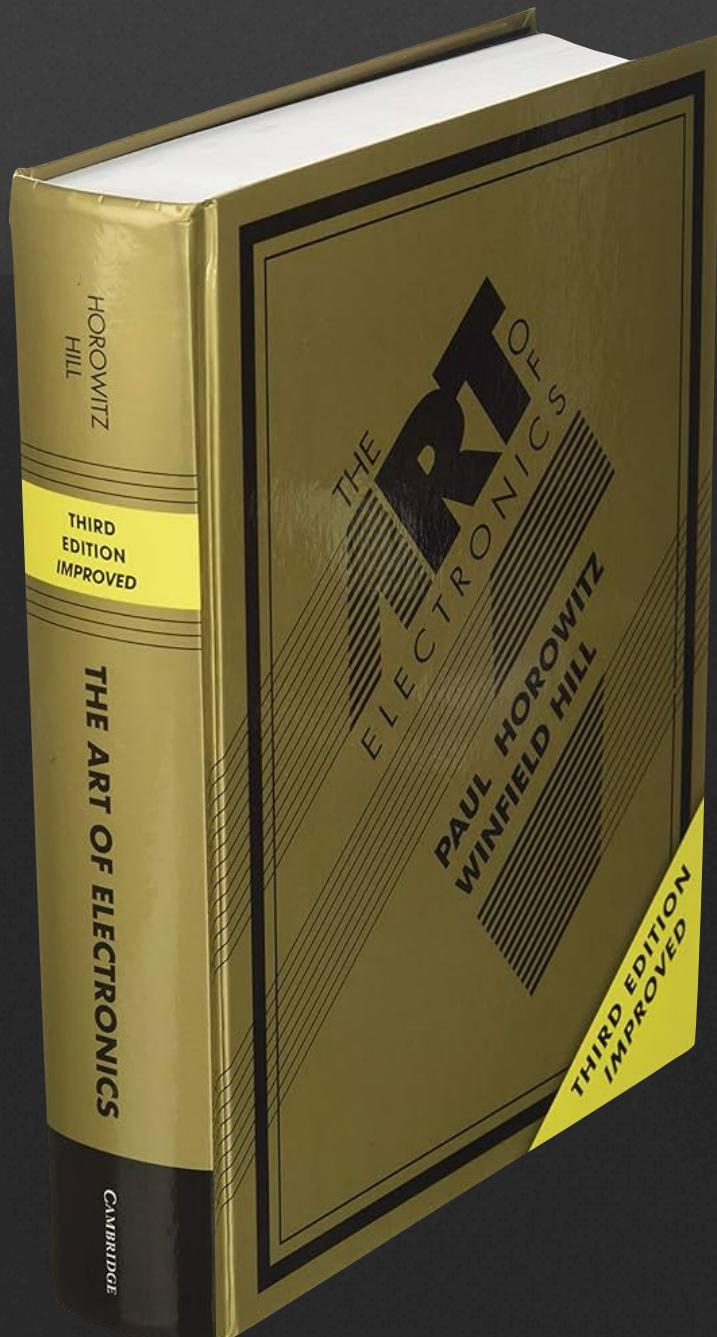
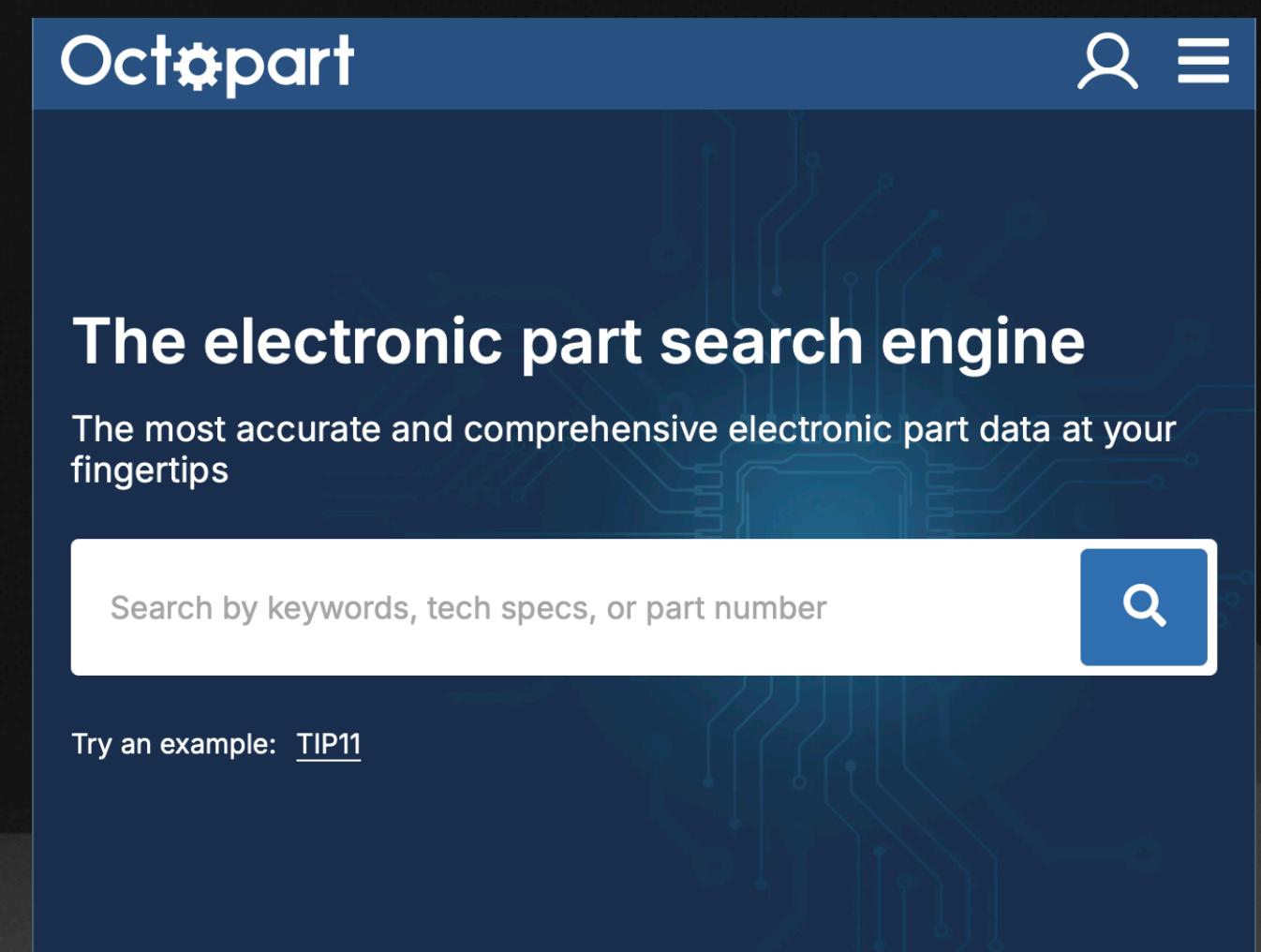
# course updates

## lecture 03

- Make sure you're on the email alias and **registered for a track!**
- Lecture 2 feedback 
- Echo 360 recordings are being wacky
- Make sure you have KiCad installed! ([kicad.org/download](http://kicad.org/download))
- Pull the GitHub! ([github.com/ieee-wpi/pcb](https://github.com/ieee-wpi/pcb))

# technical resources to help you

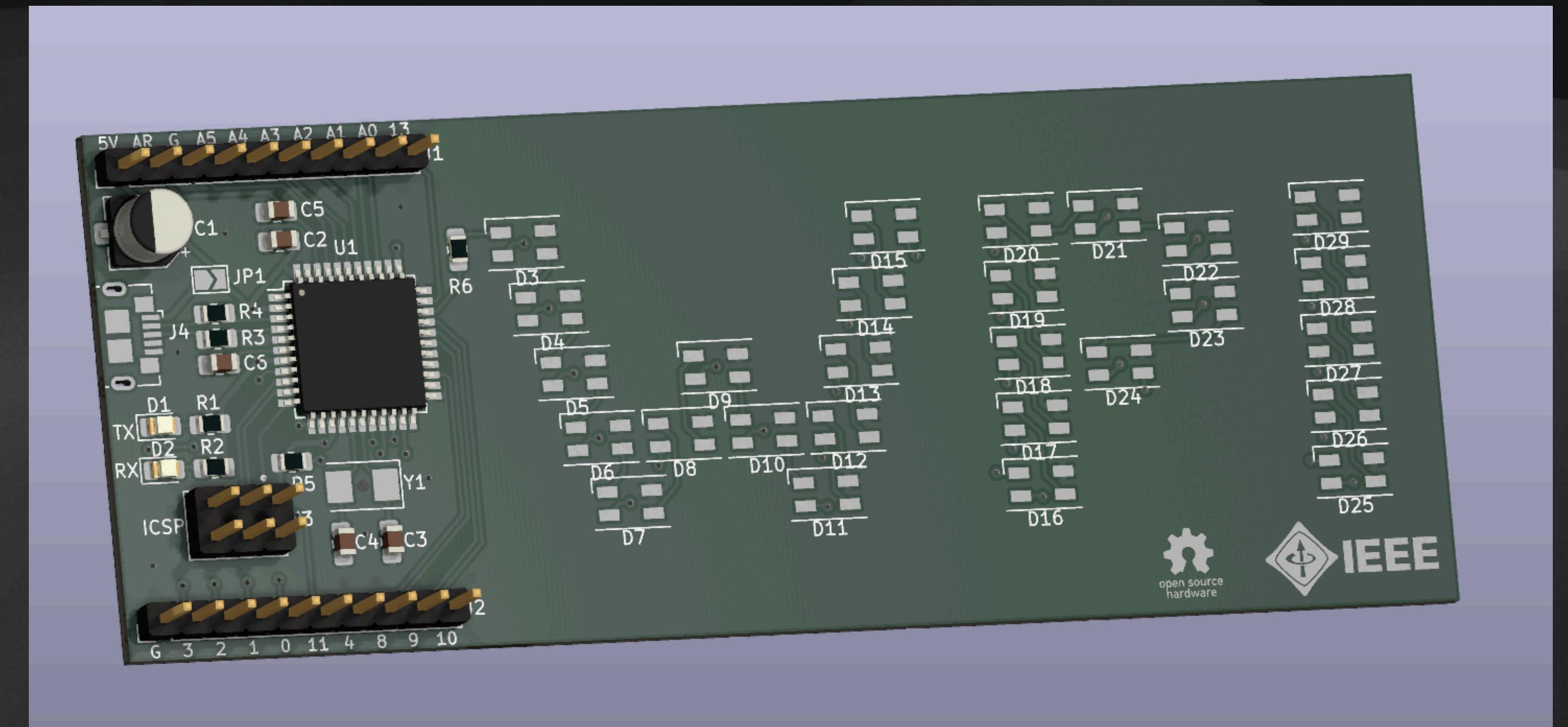
- [pcb.mit.edu/resources](http://pcb.mit.edu/resources)
- Octopart
- DigiKey trace width calculator
- The Art of Electronics, Horowitz and Hill
- Open Circuits, Schlaepfer and Oskay



# hardware design process

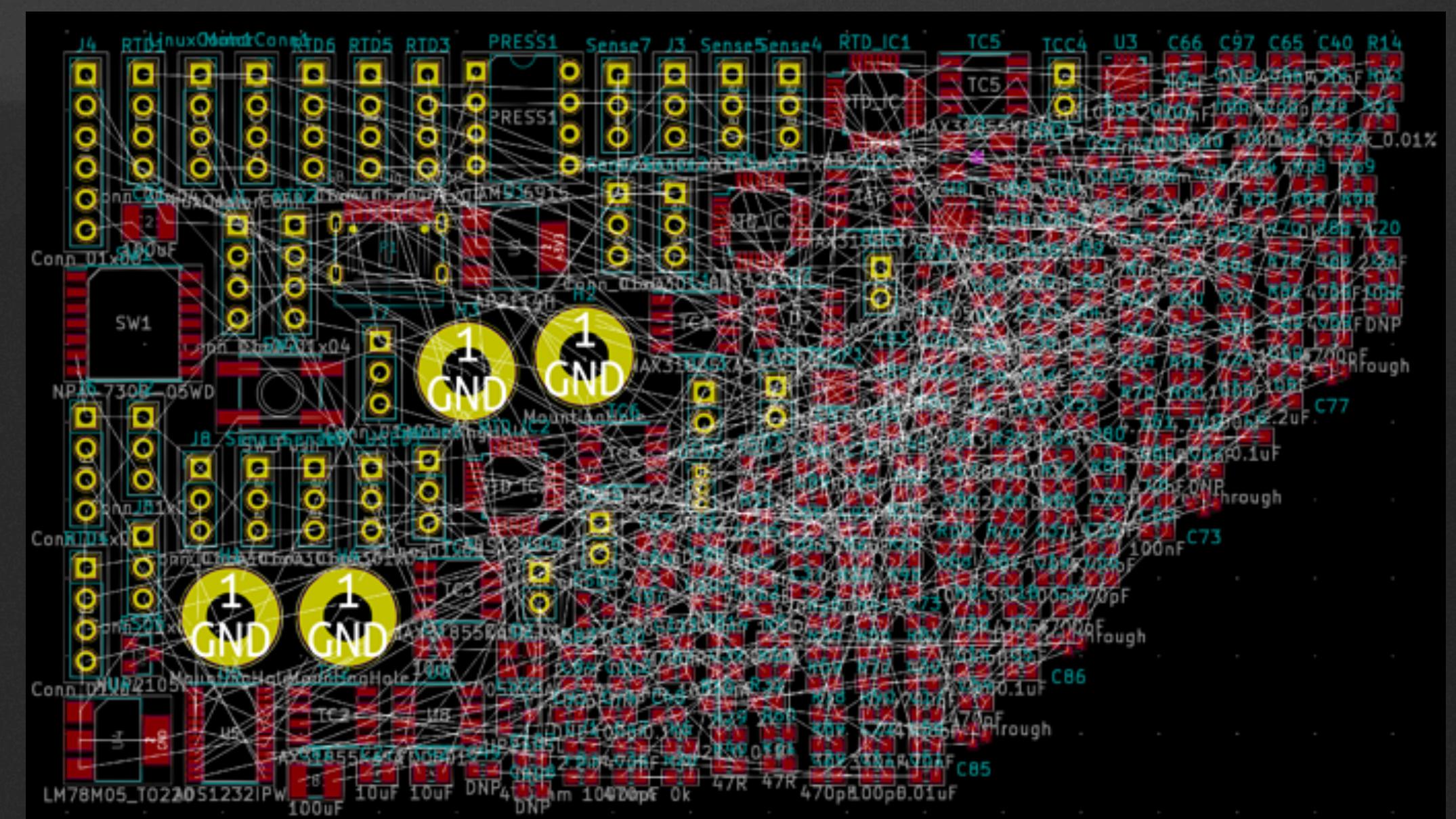
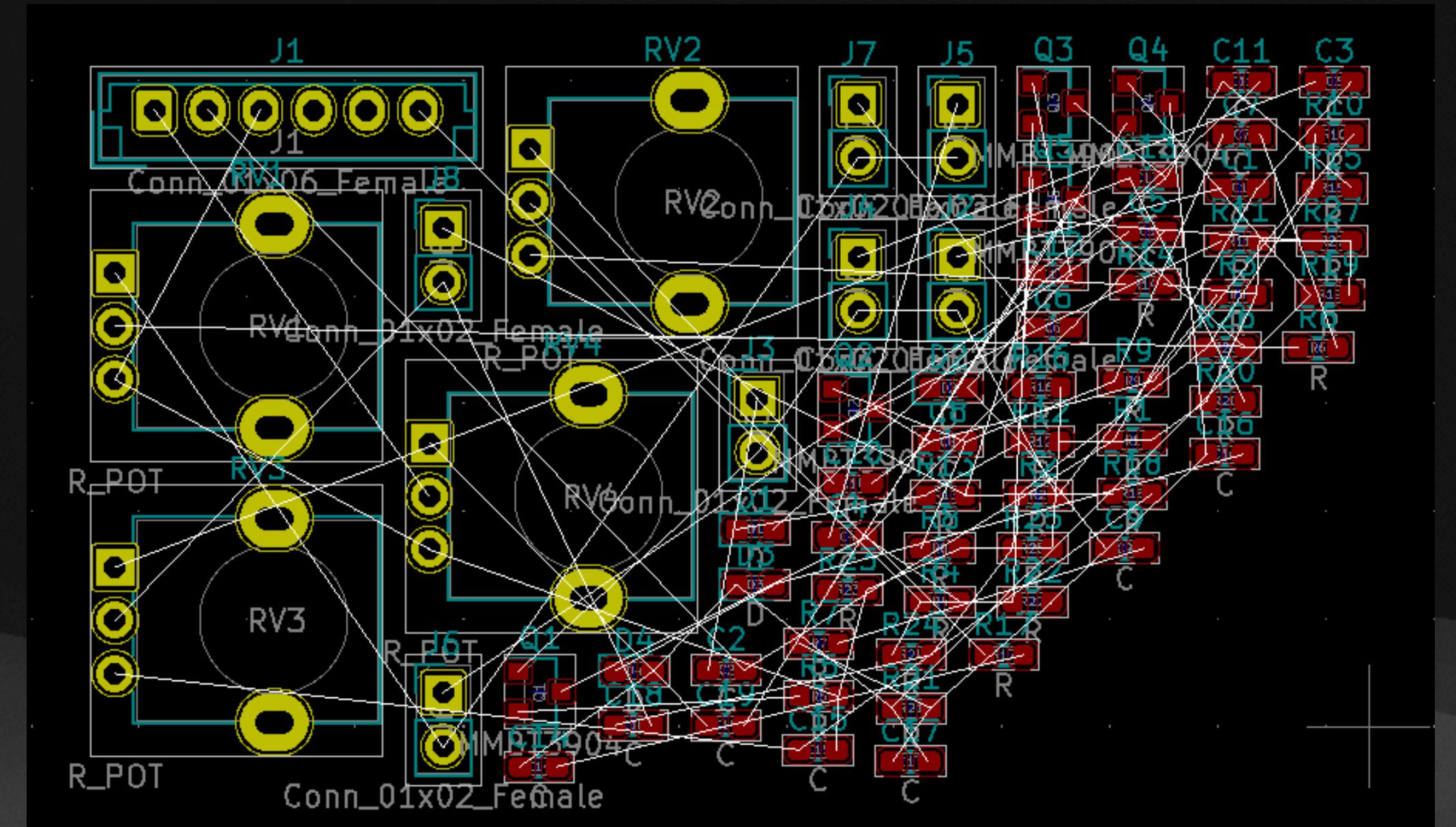
## walkthrough

1. Research and Design
2. Schematic Capture
- 3. Layout**
4. Routing
5. Order
6. Assembly



# layout process

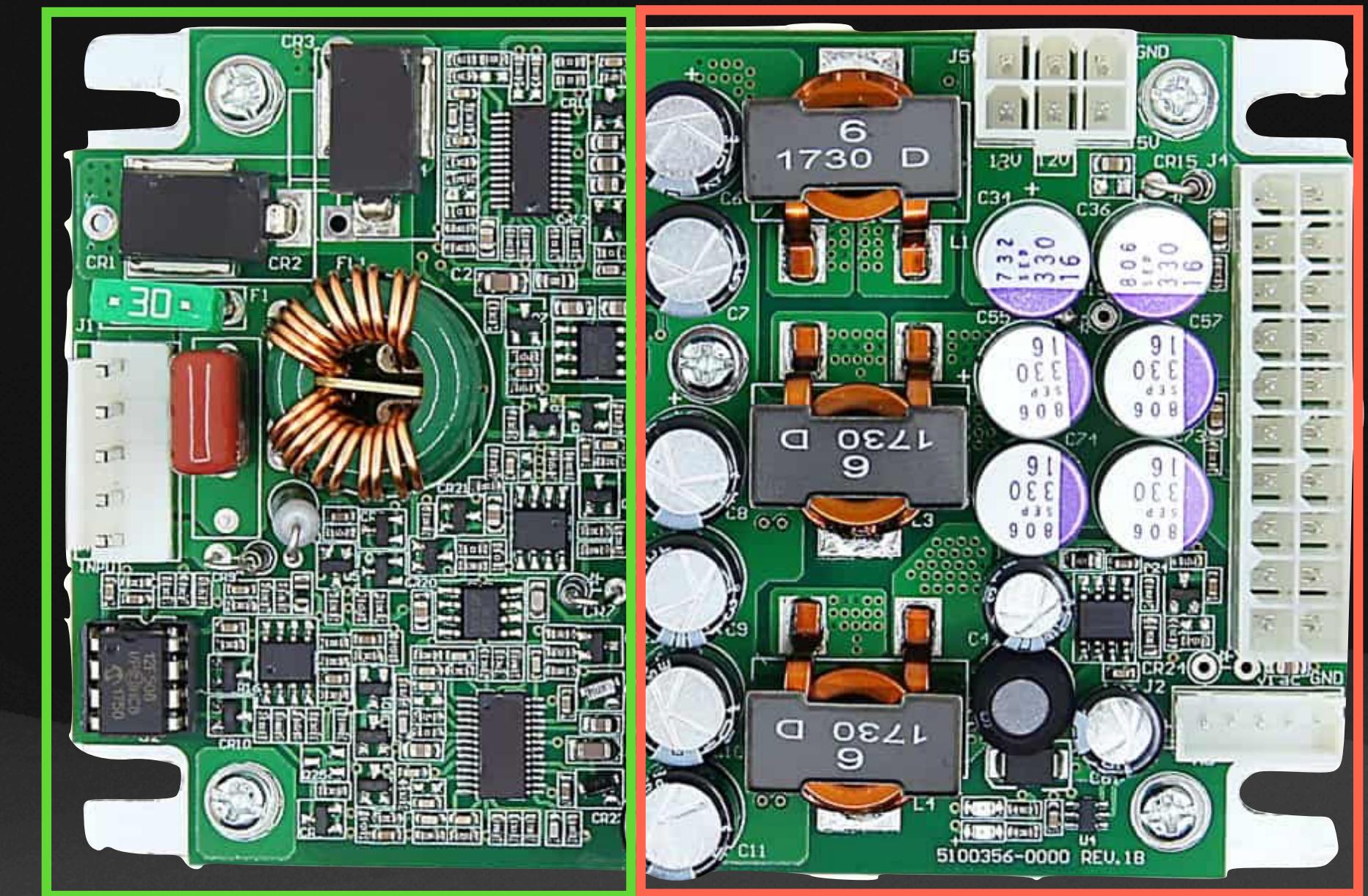
- Layout is an art
- Smart layout will save you hours of routing
- The goal here is to minimize **net intersections** by changing:
  - Component location
  - Component rotation
- Layout all your components first, **then** route!



# Layout is Fun!

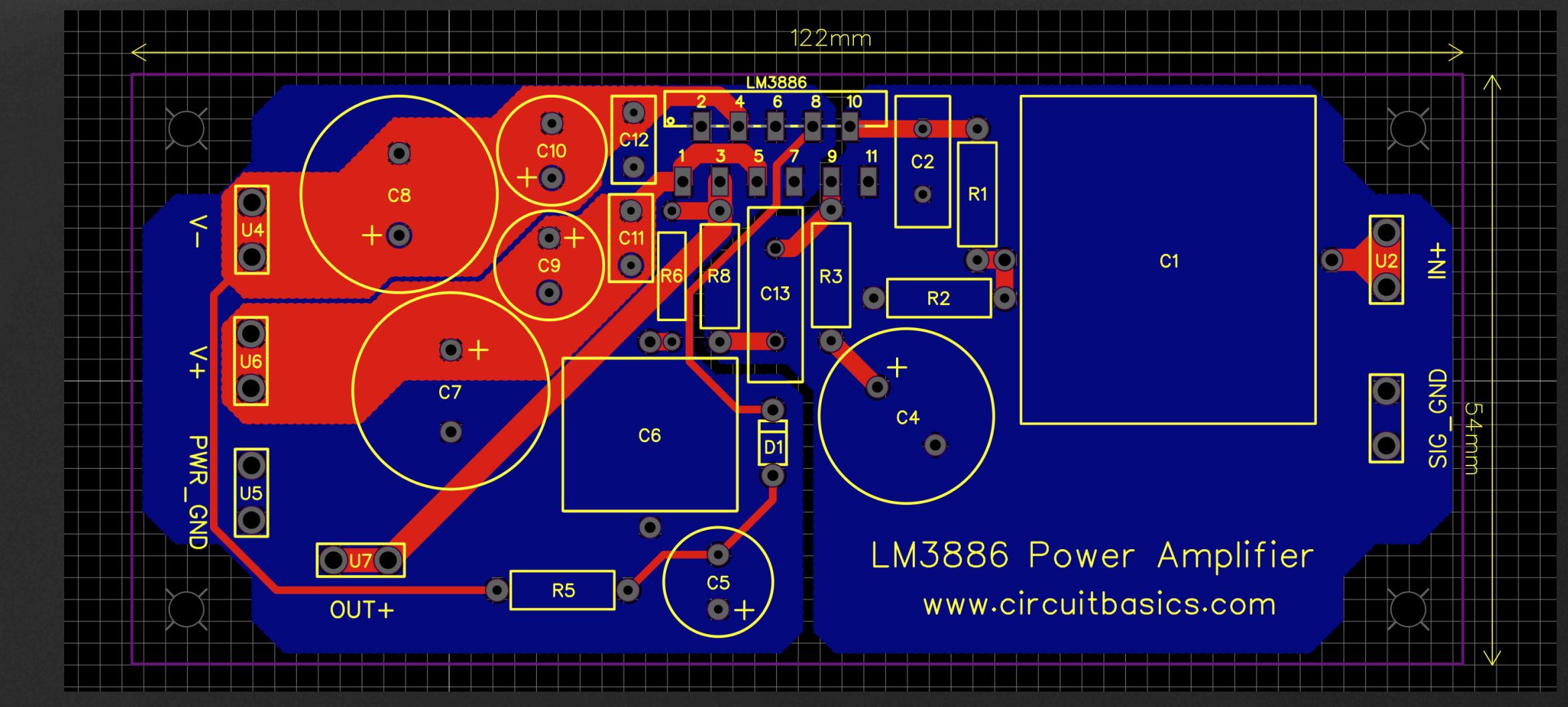
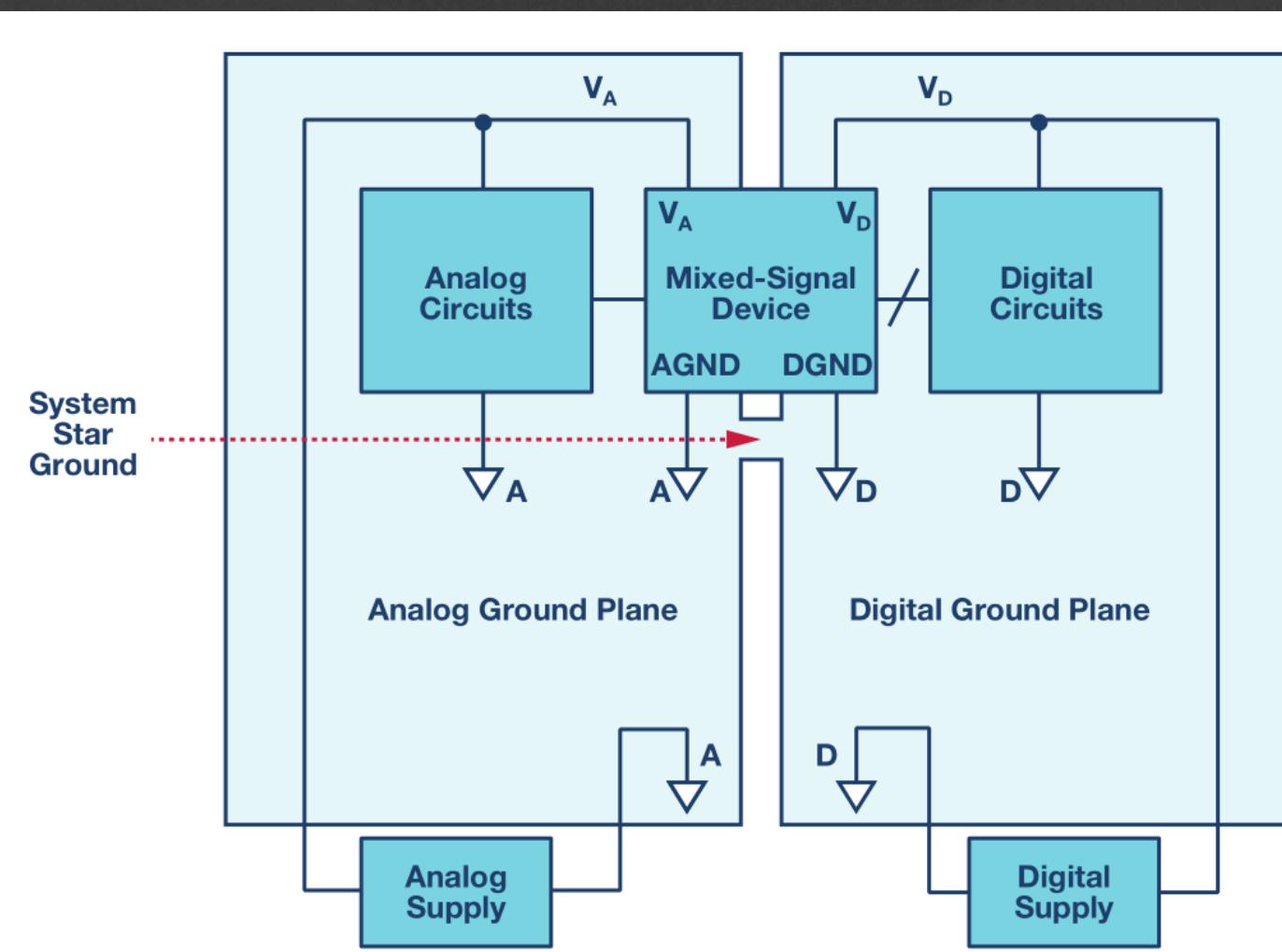
# layout seperation

- About more than just connecting things...
- Separation of **power and signal**
- Separation of **digital and analog** ground



Signal

Power

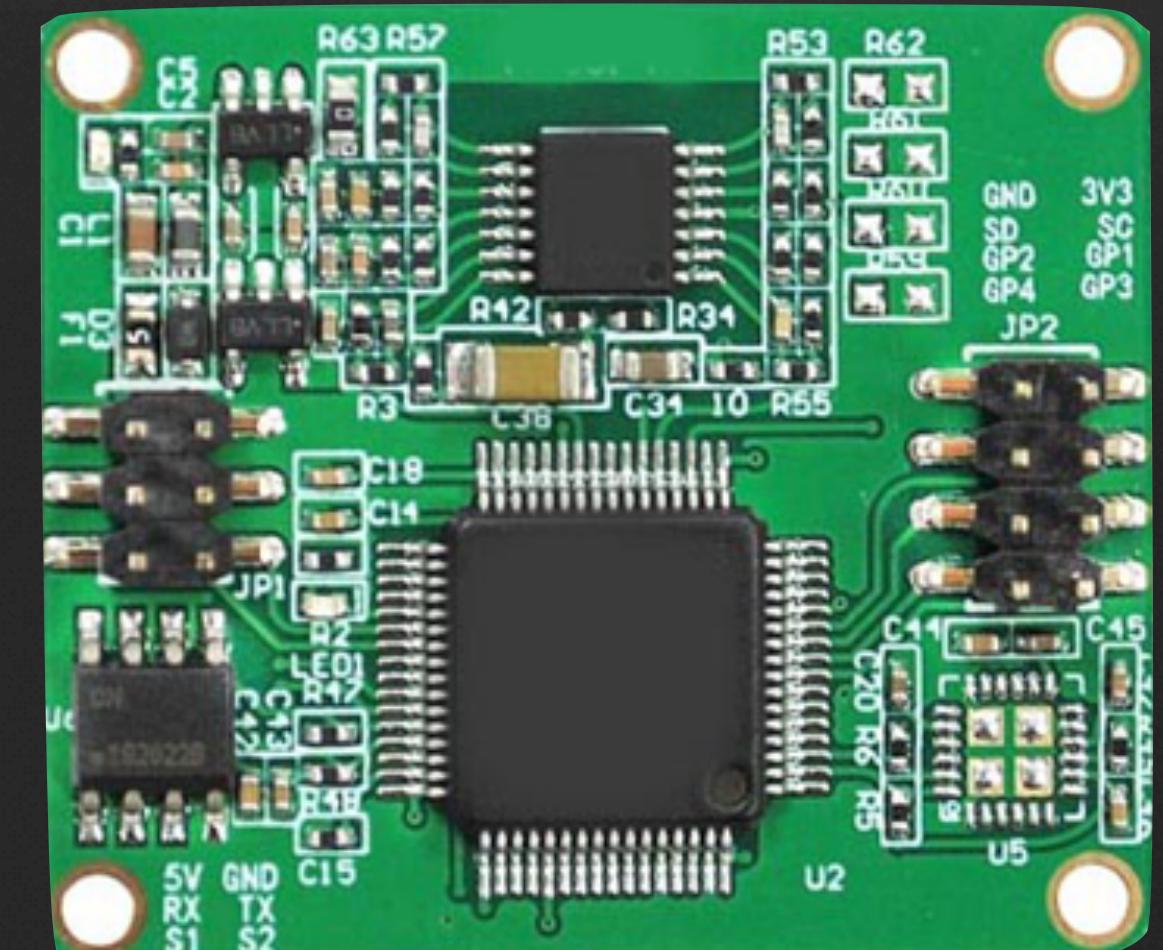
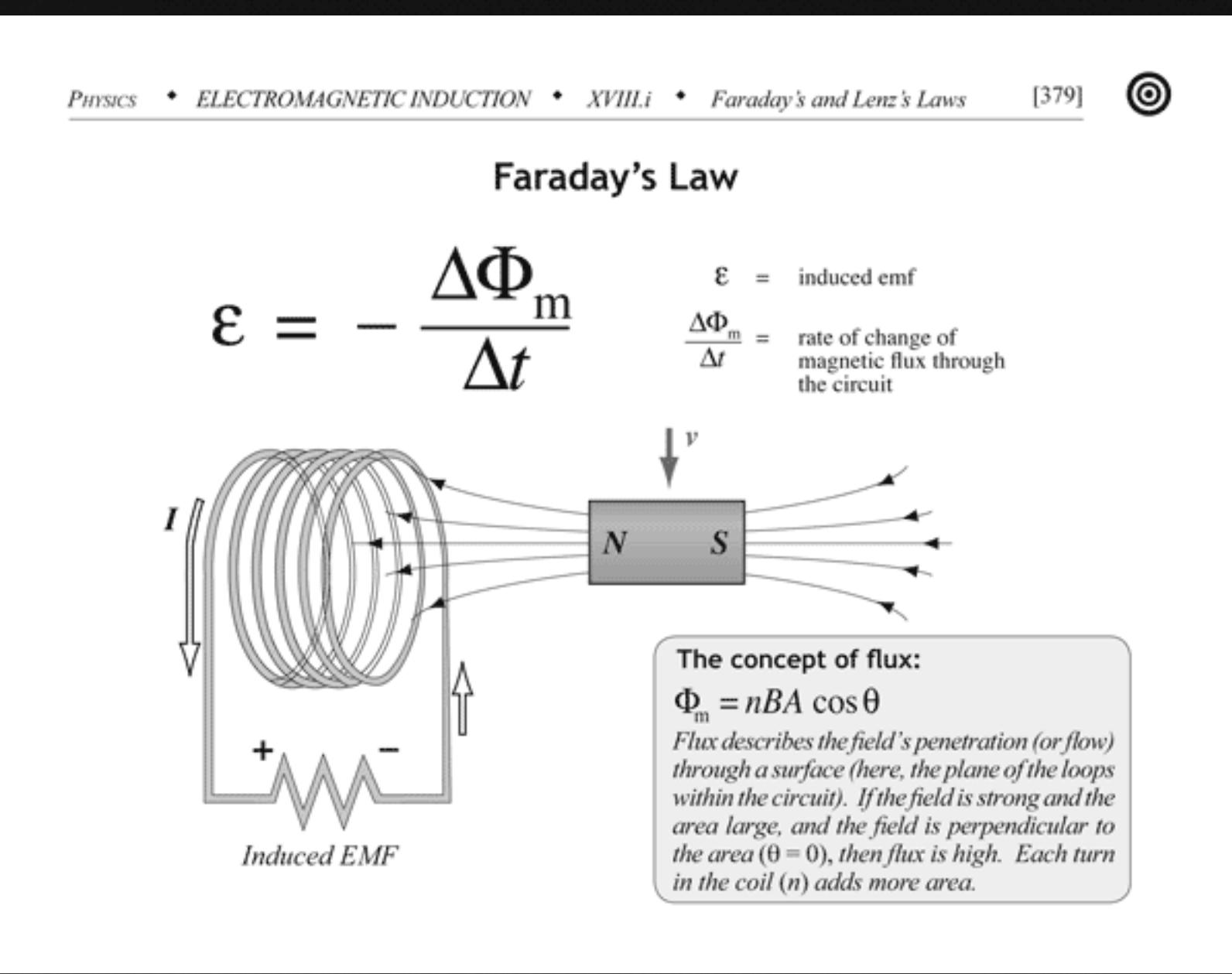


Digital GND

Analog GND

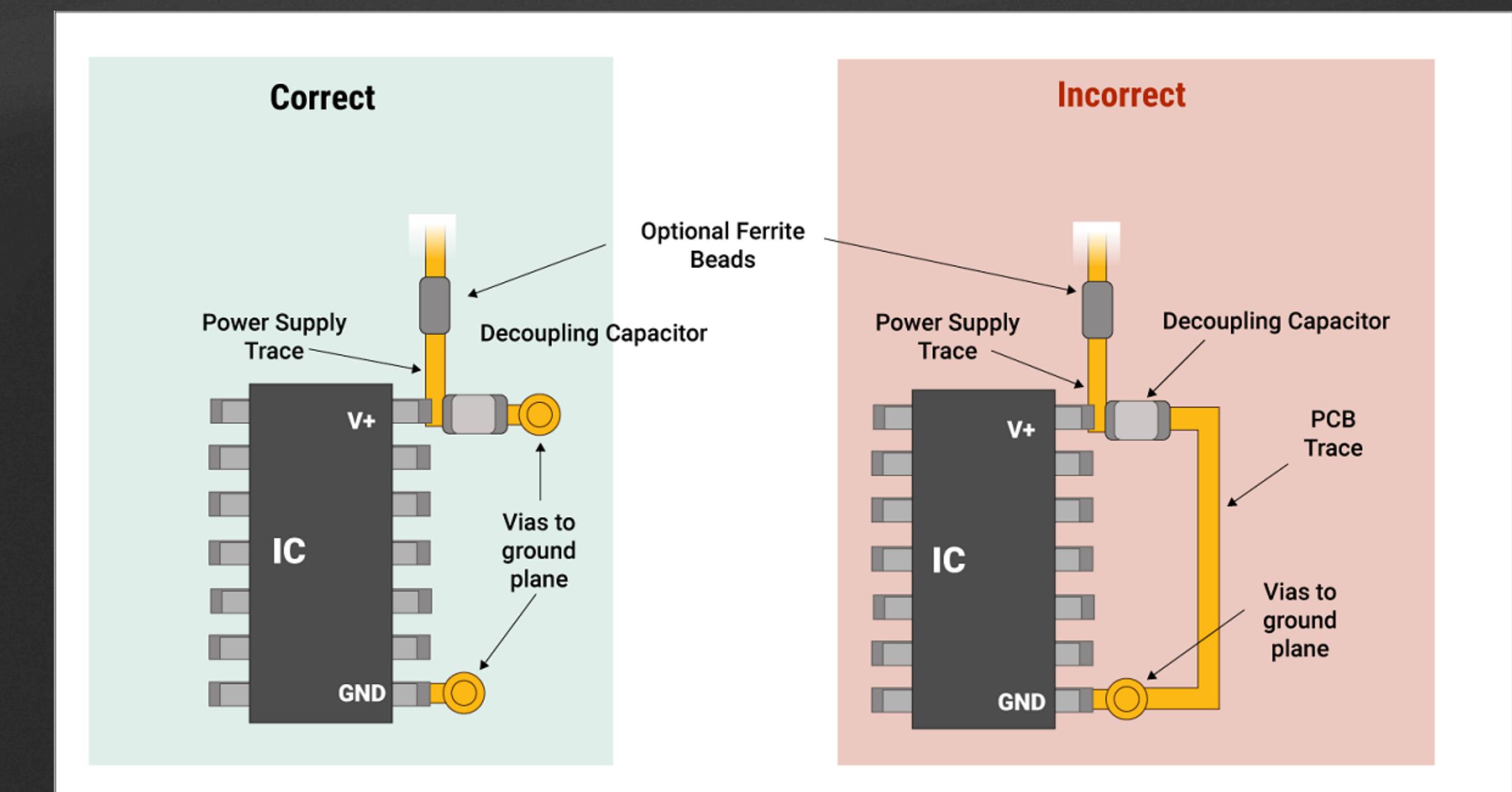
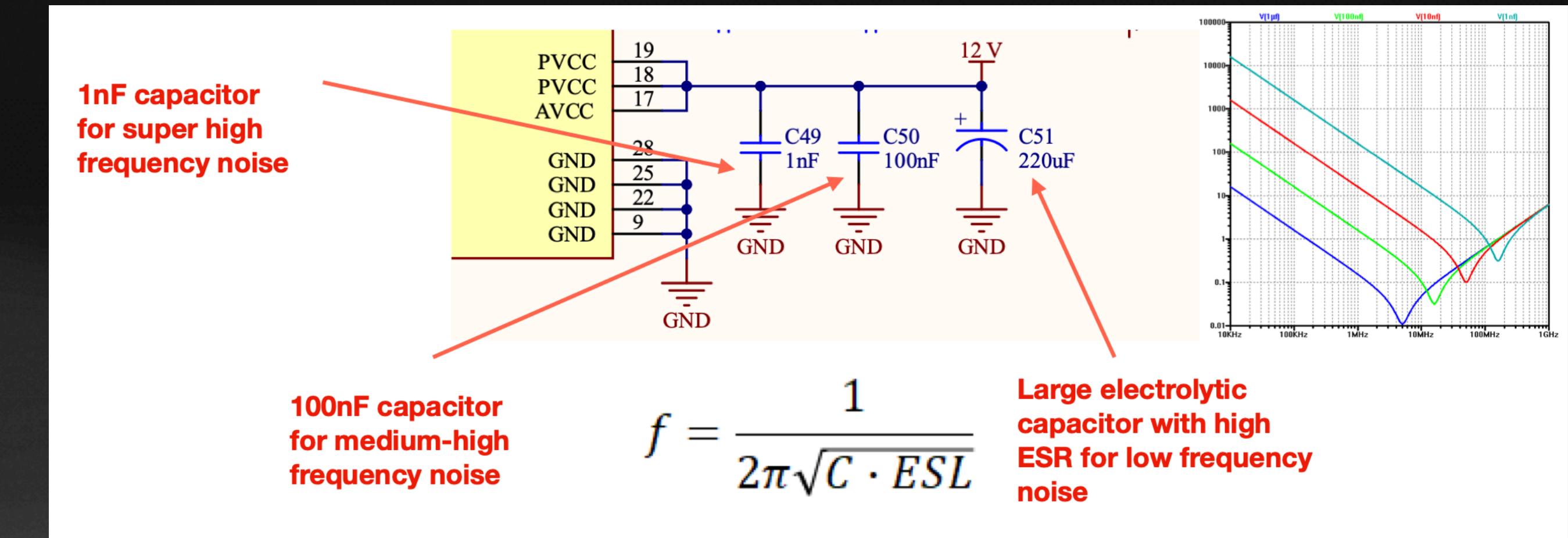
# layout considerations

- Placement of sensitive components (sensors)
- Decoupling capacitor location
- Optimizing trace length; inductance loops
- Tightly package components



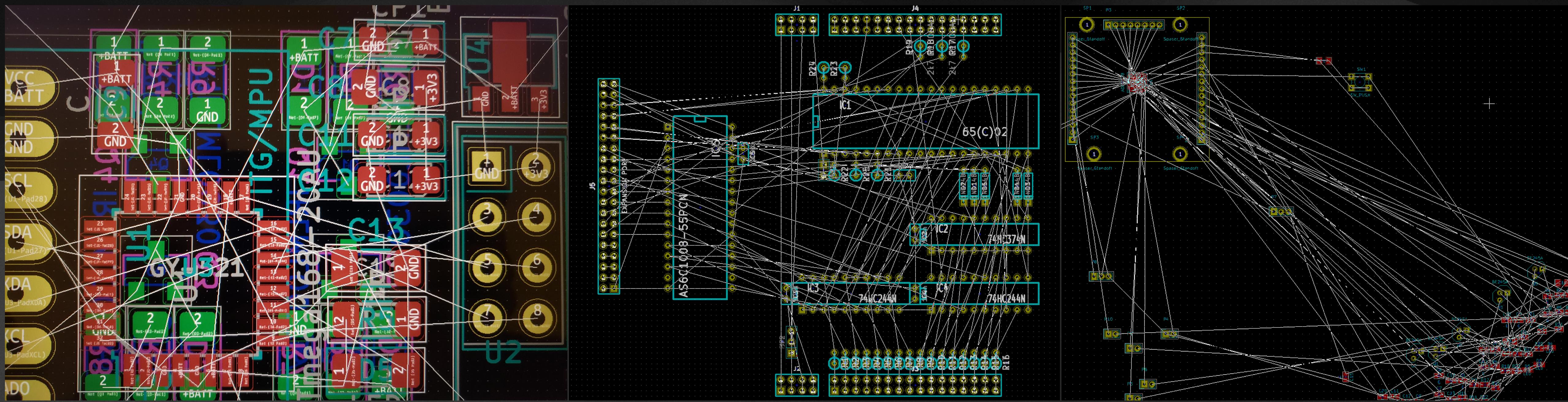
# layout considerations

- Decoupling capacitor location
- Should be as close as possible to IC and ground



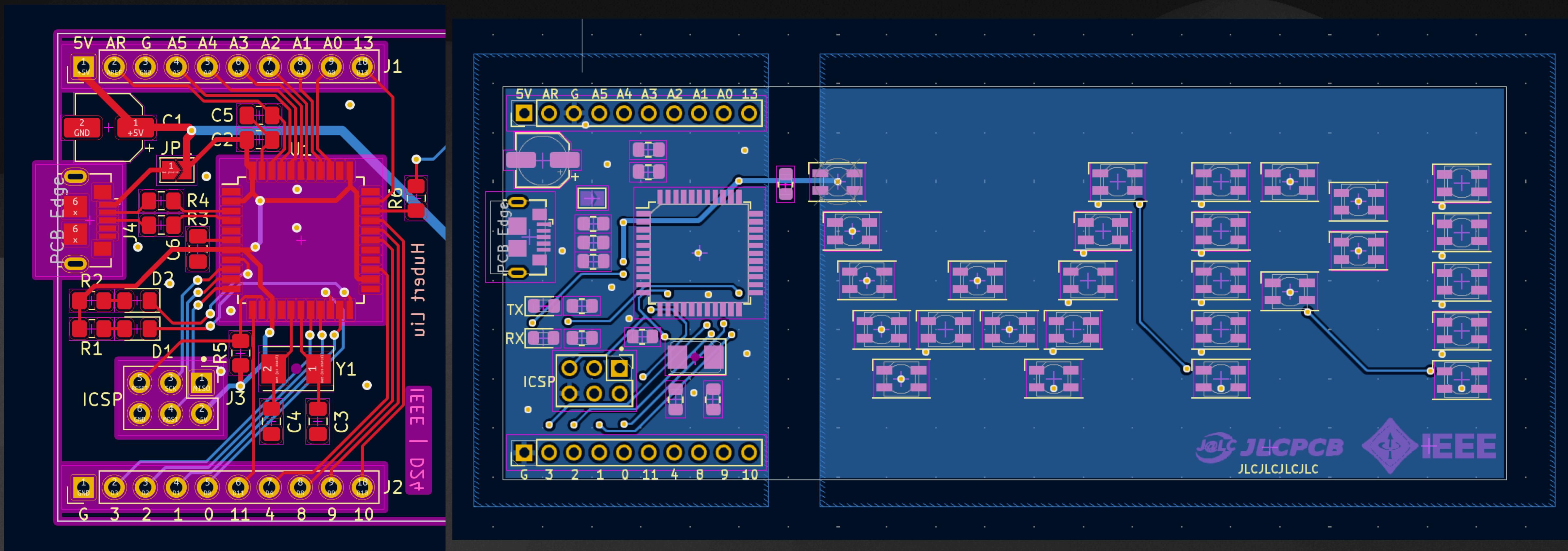
# layout

## the bad

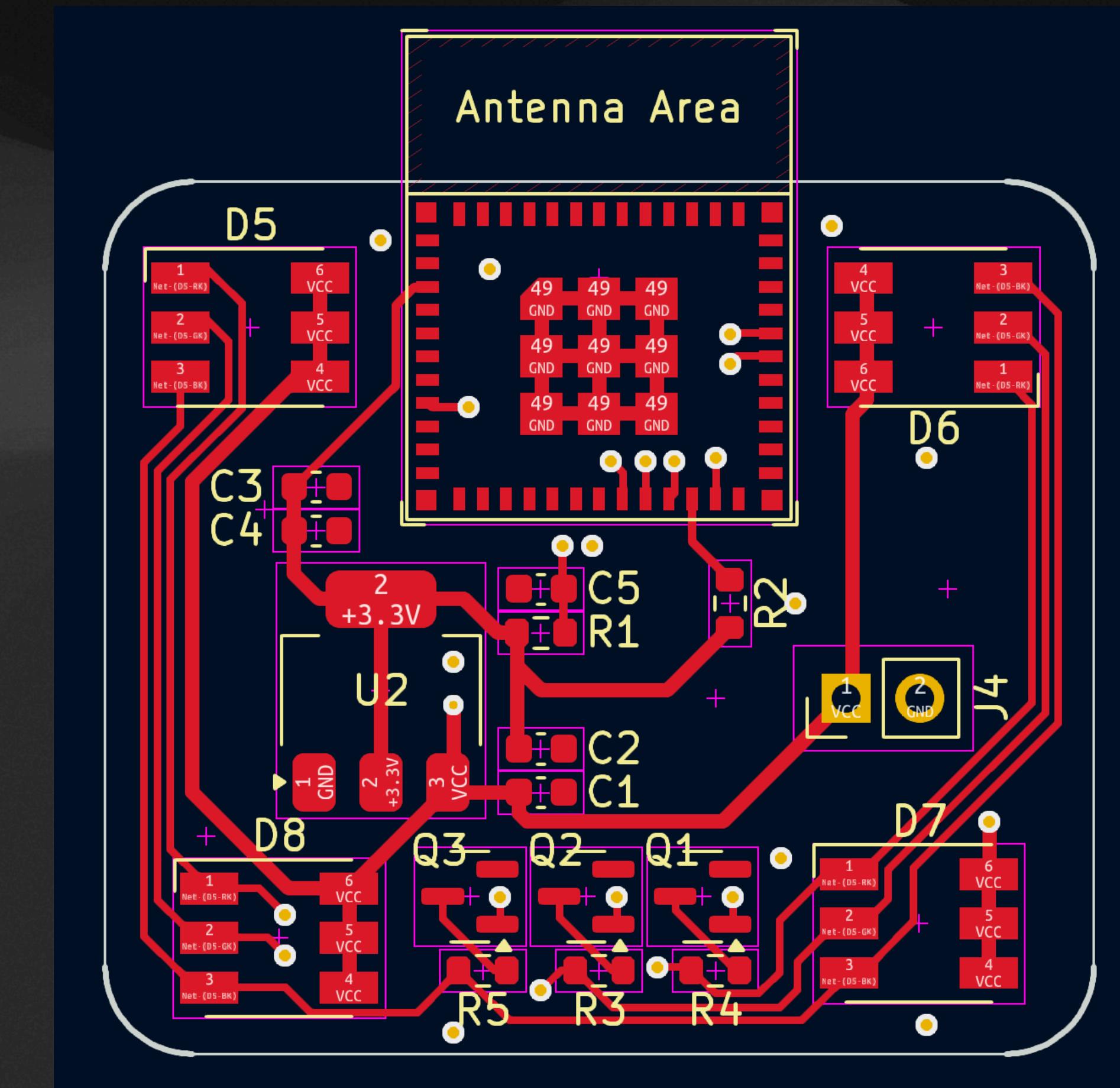
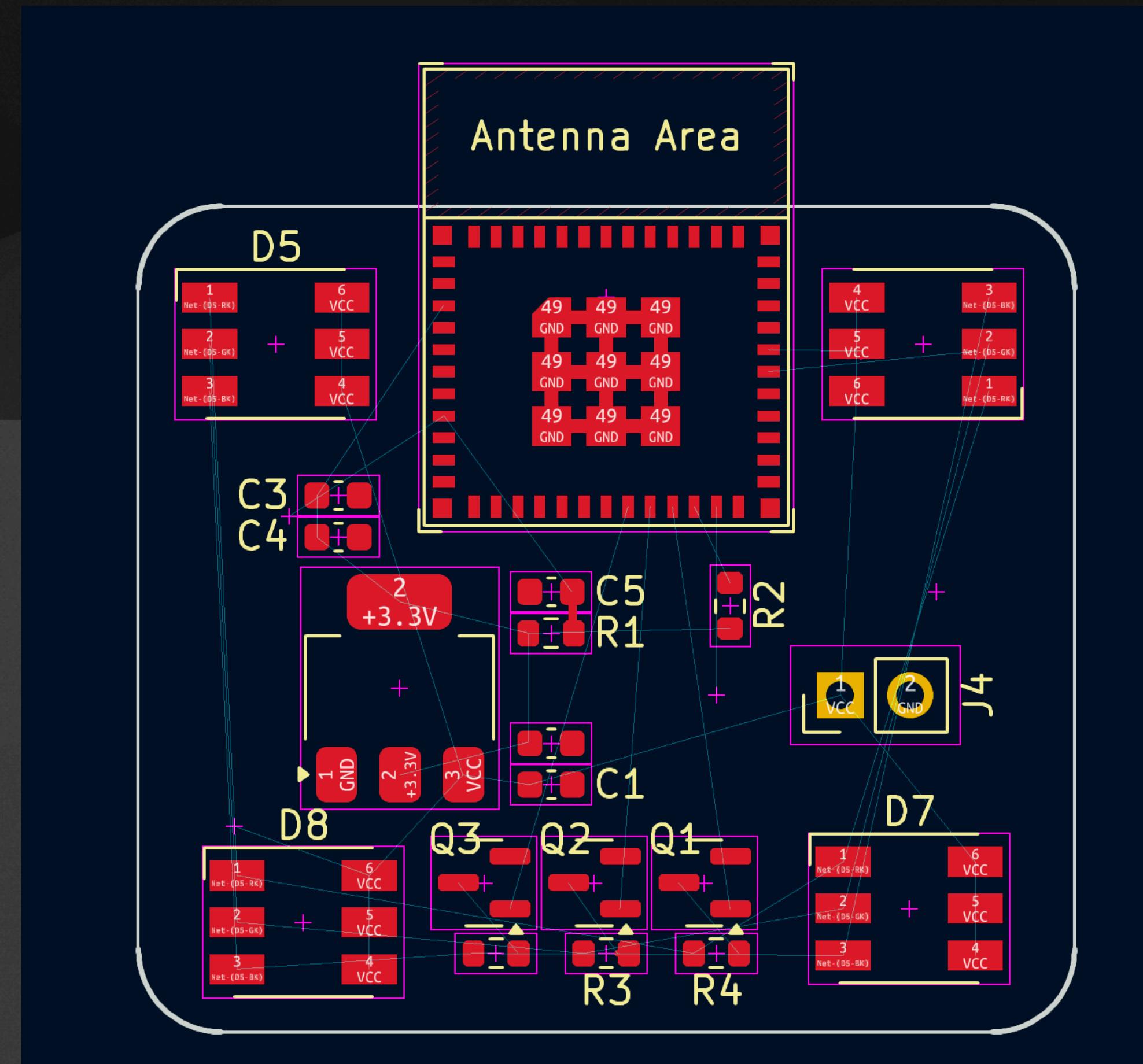


# layout

## the good

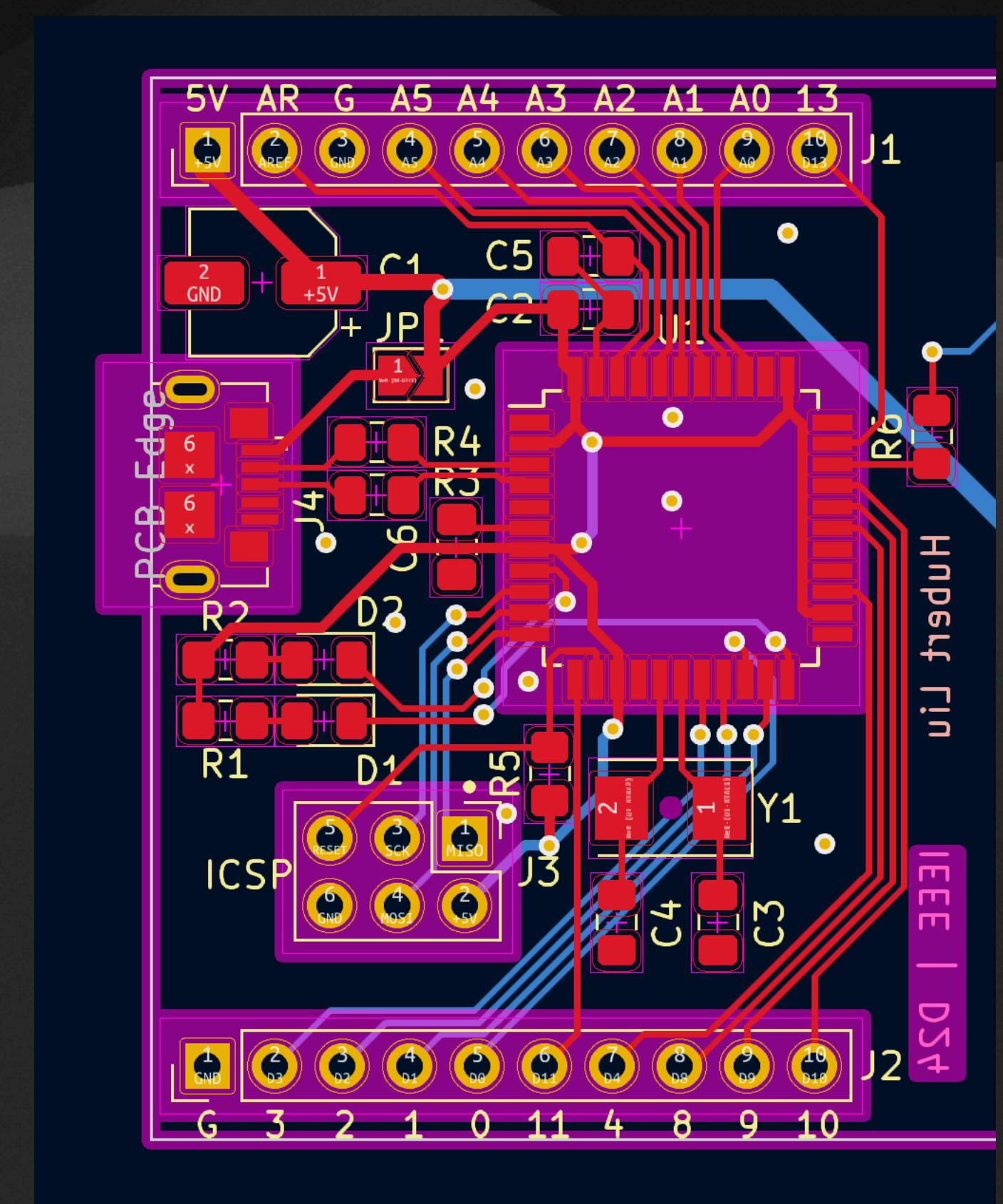
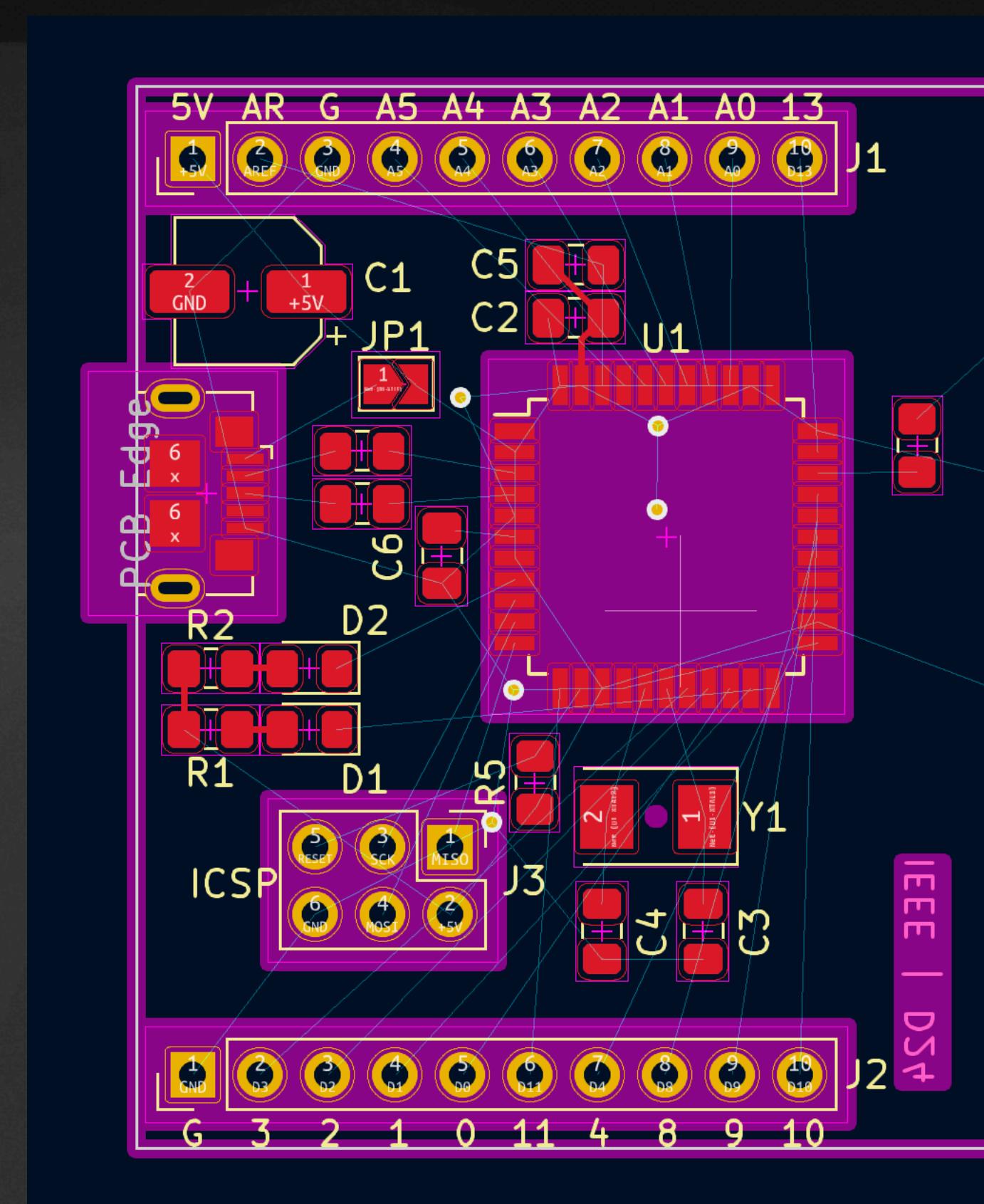
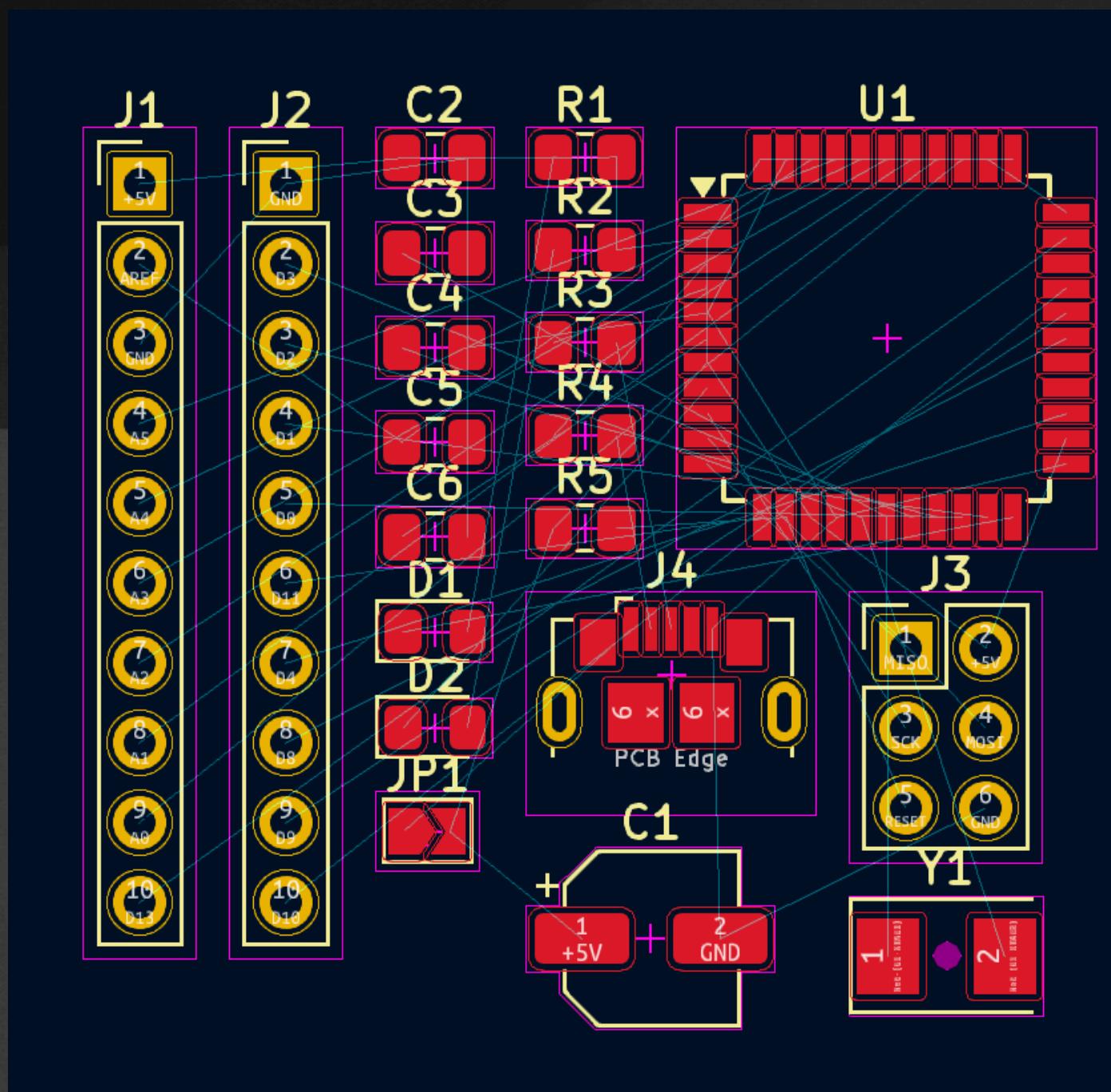


# layout process



# layout

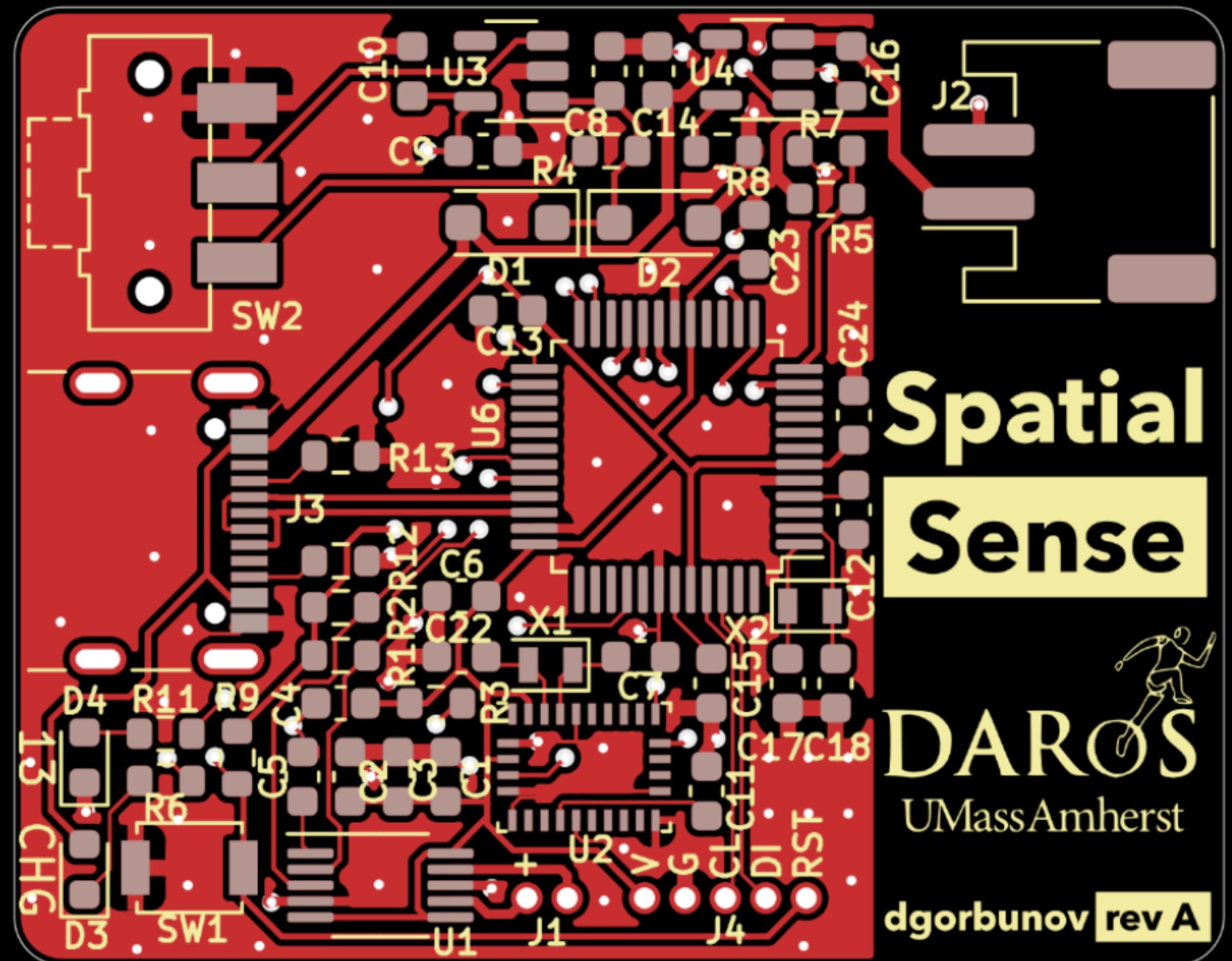
## track 1 board



# PCB Layout

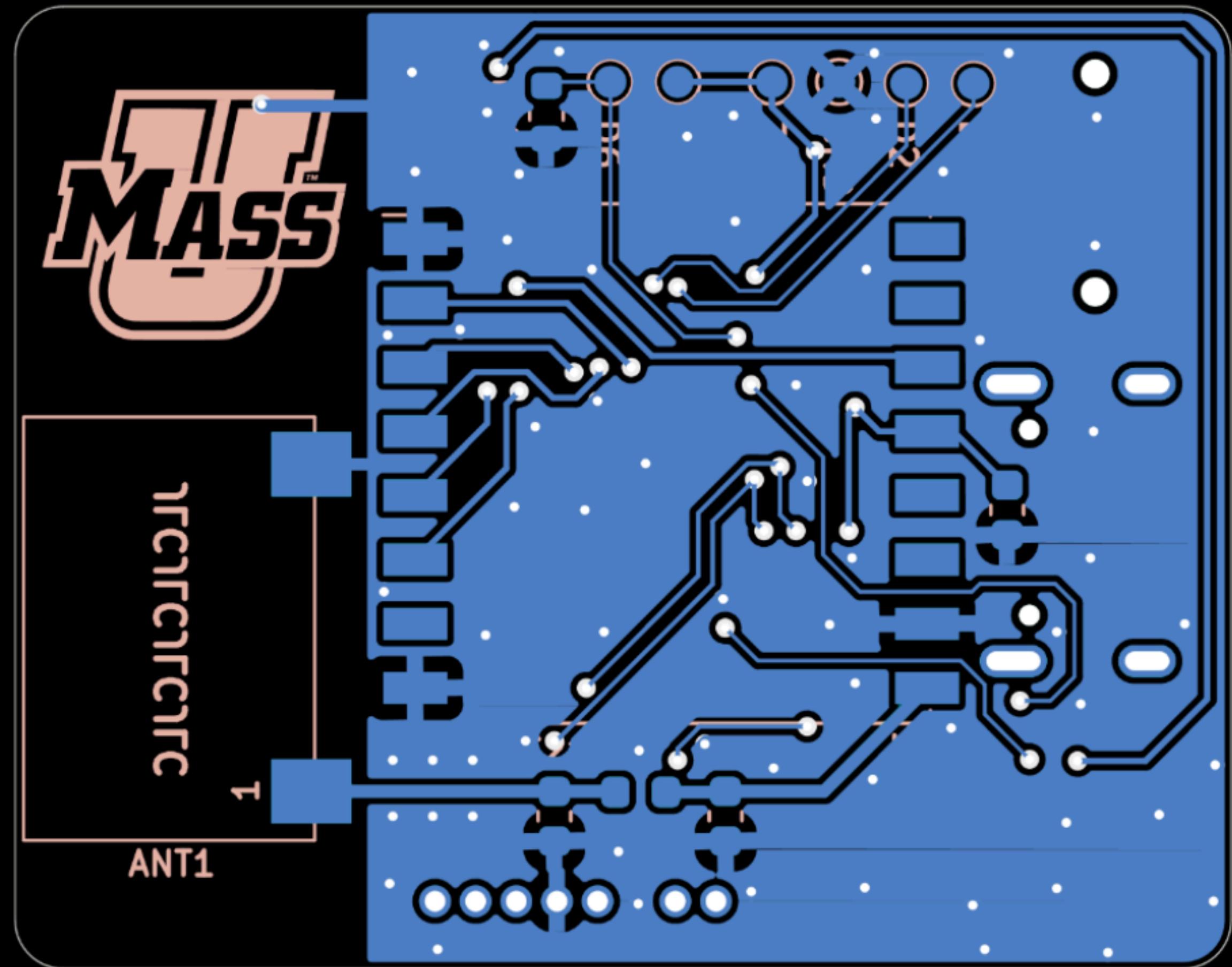
30mm

Front



38mm

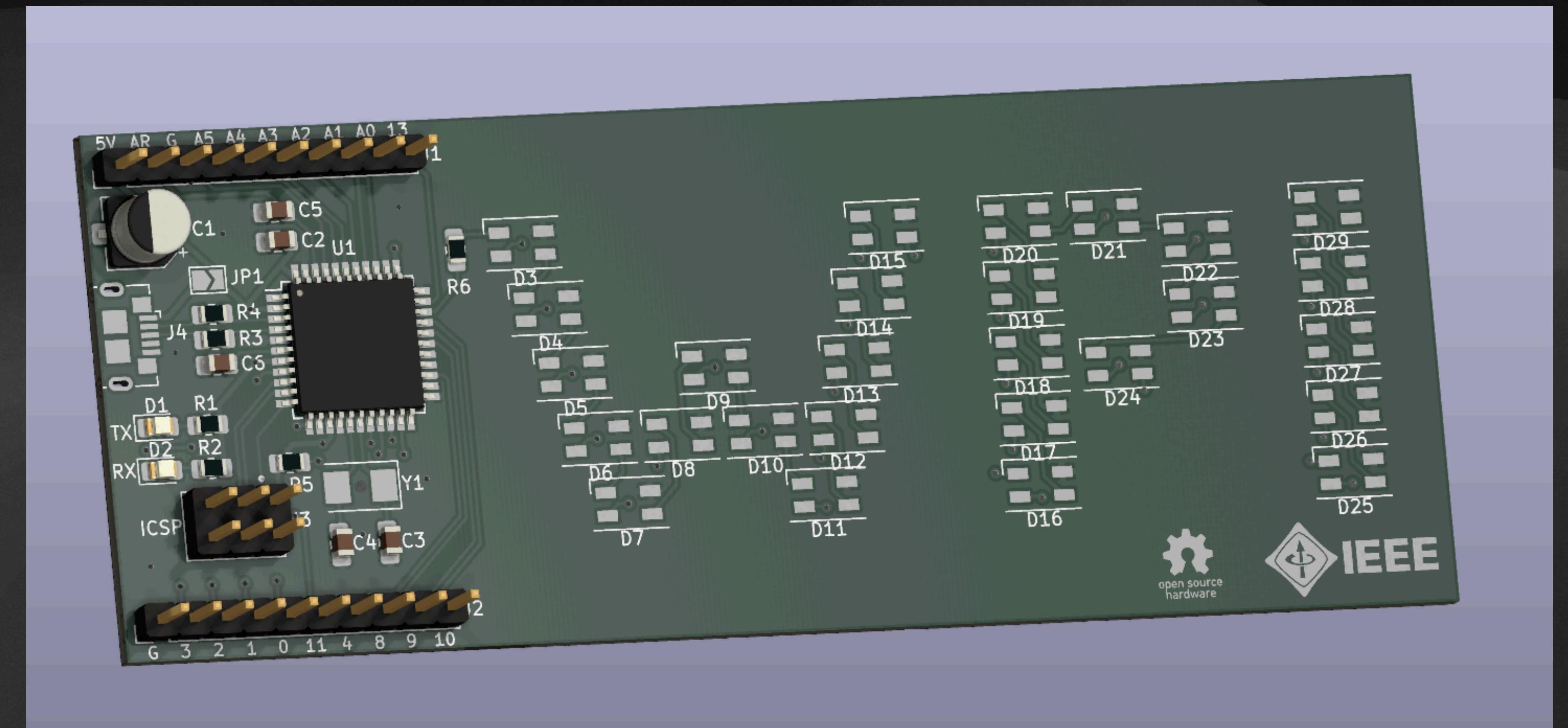
Back



# hardware design process

## walkthrough

1. Research and Design
2. Schematic Capture
3. Layout
- 4. Routing**
5. Order
6. Assembly

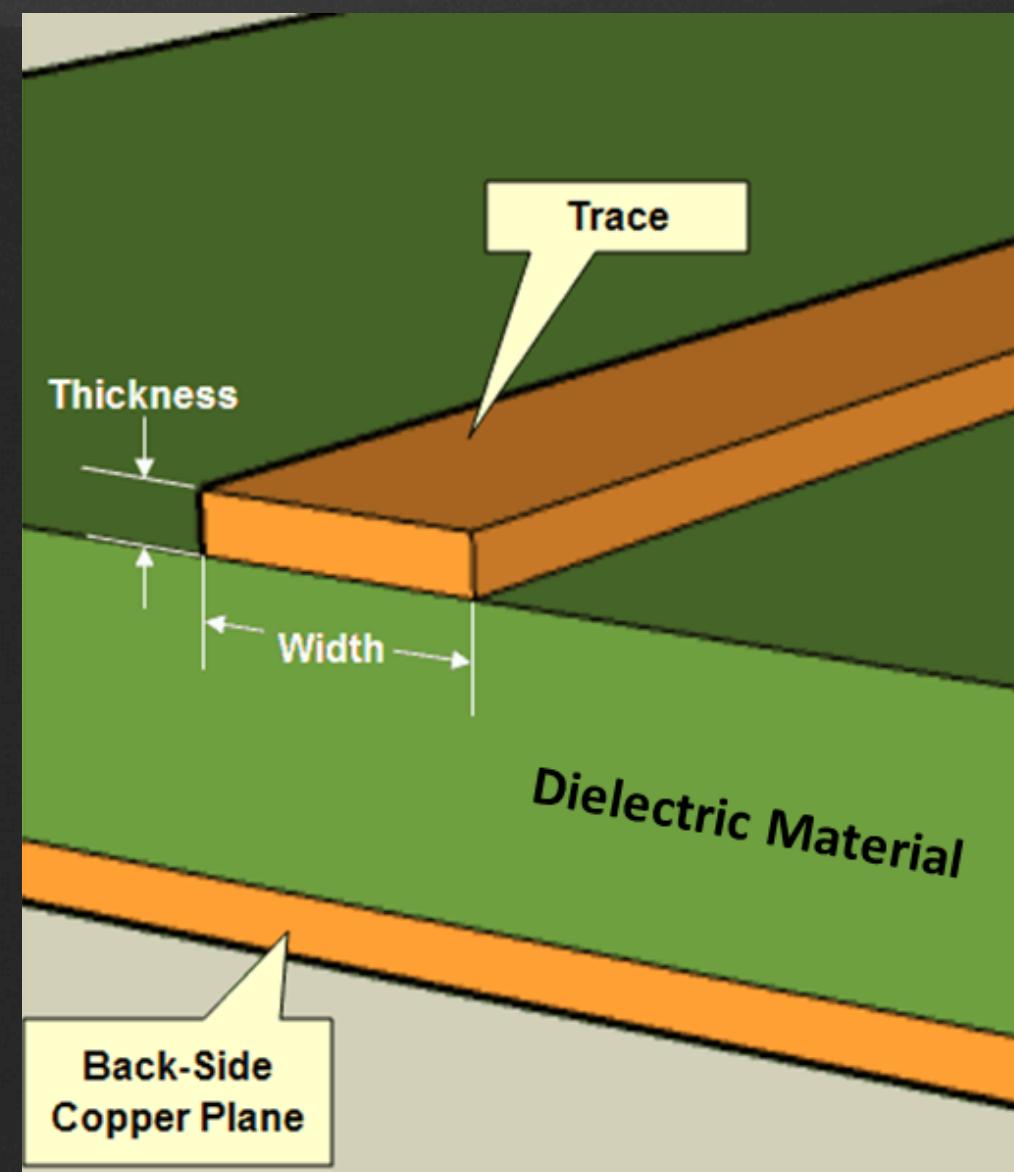


# routing process

- Once you ‘untangle’ the nets, you can begin routing
- A good first step is to **disable ground nets**
- Common practice to fill unused space on the board with a ground pour, this means less routing
- Important parameter here: **trace width**
- KiCad default is fine for signal traces
- Power traces need more careful consideration
- DigiKey has a great calculator for this!

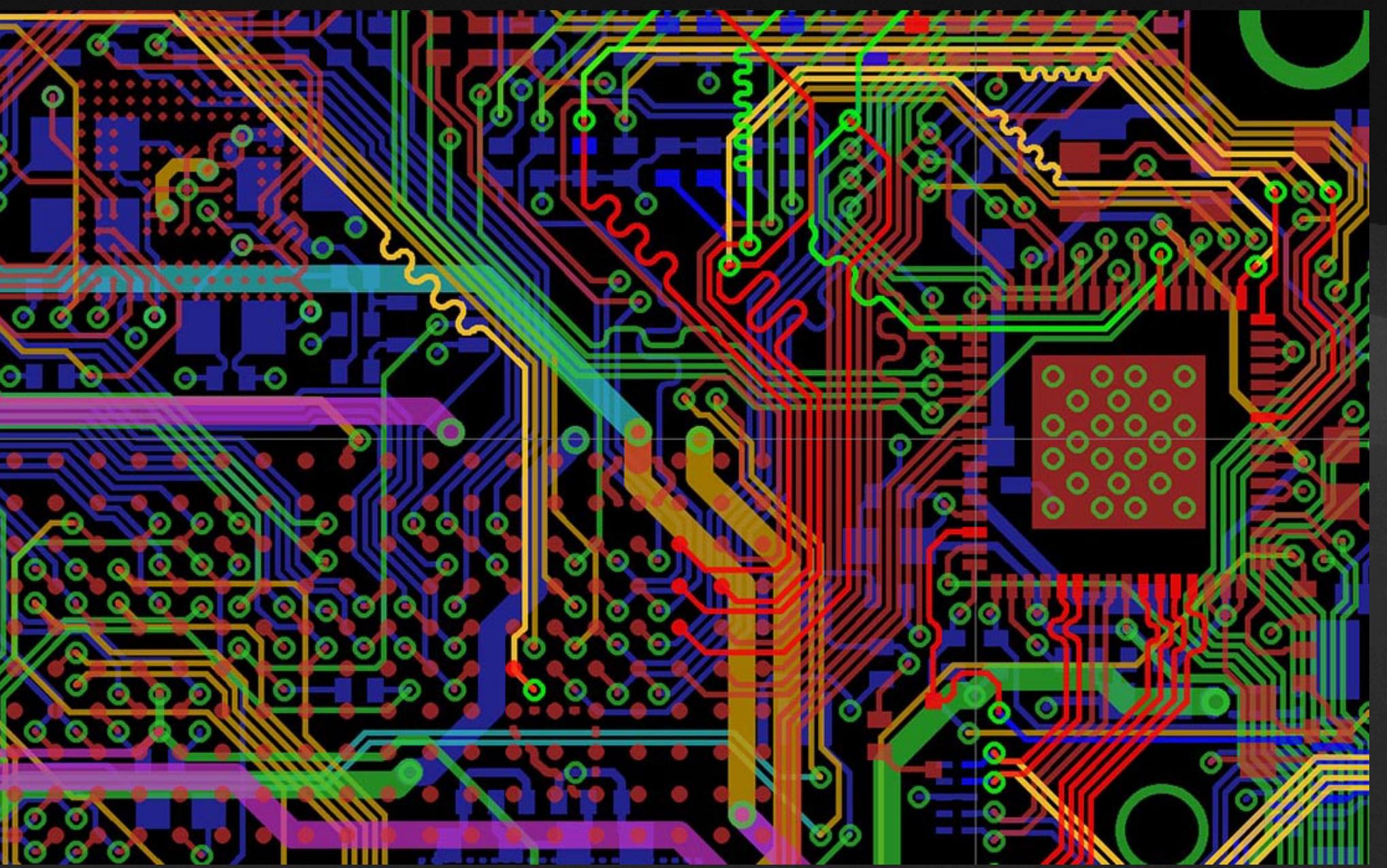
IPC Recommended Track Width For 1 oz cooper PCB and 10 °C Temperature Rise

Current/A	Track Width(mil)	Track Width(mm)
1	10	0.25
2	30	0.76
3	50	1.27
4	80	2.03
5	110	2.79
6	150	3.81
7	180	4.57
8	220	5.59
9	260	6.60
10	300	7.62



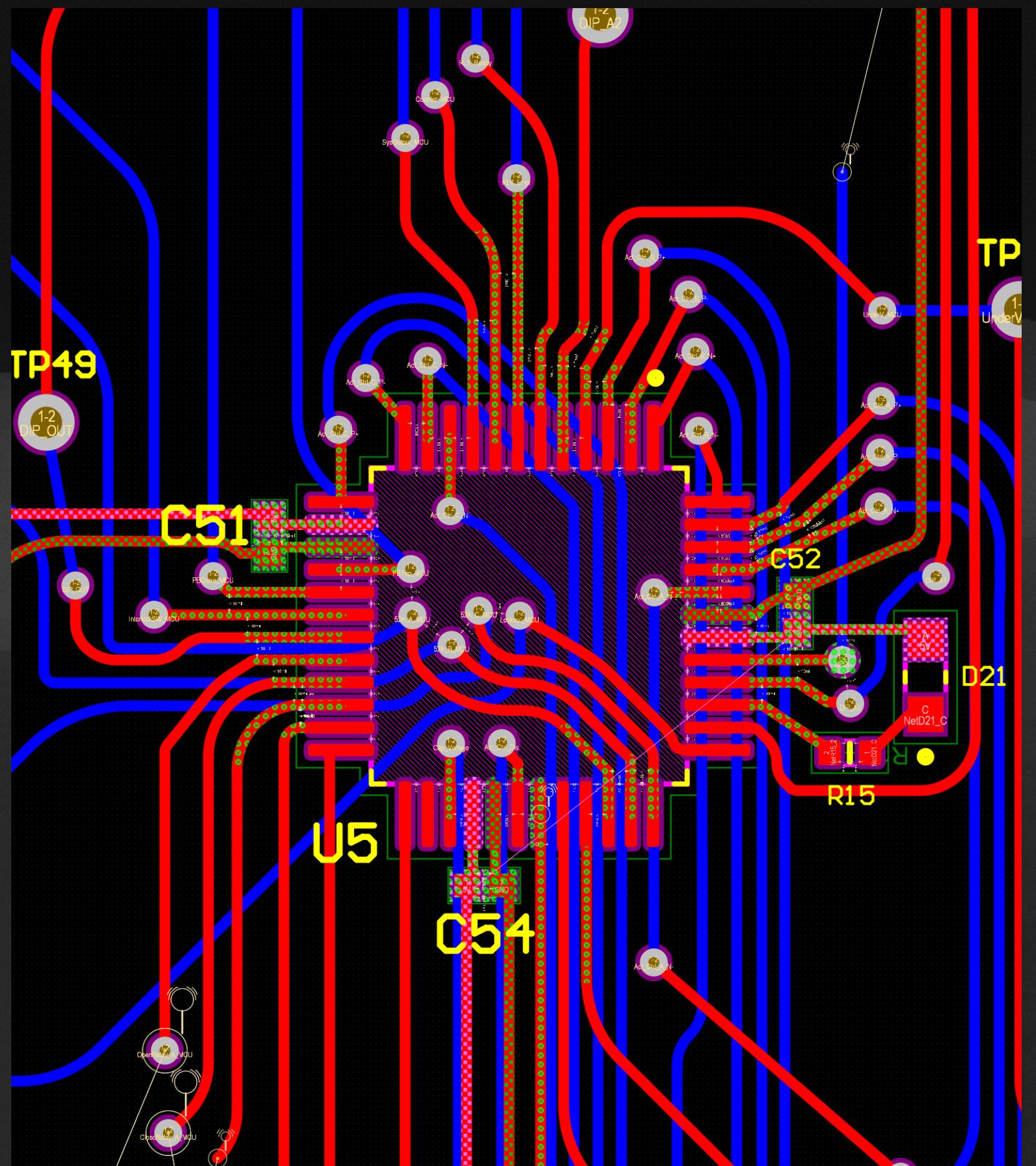
# routing process

- Use vias to cross intersections
- Avoid long, looping traces
  - EMI is a consideration here
- Place similar traces next to one another
- Certain traces need special attention
  - Any signal that is high speed or differential
- Vcc and GND should always be far apart



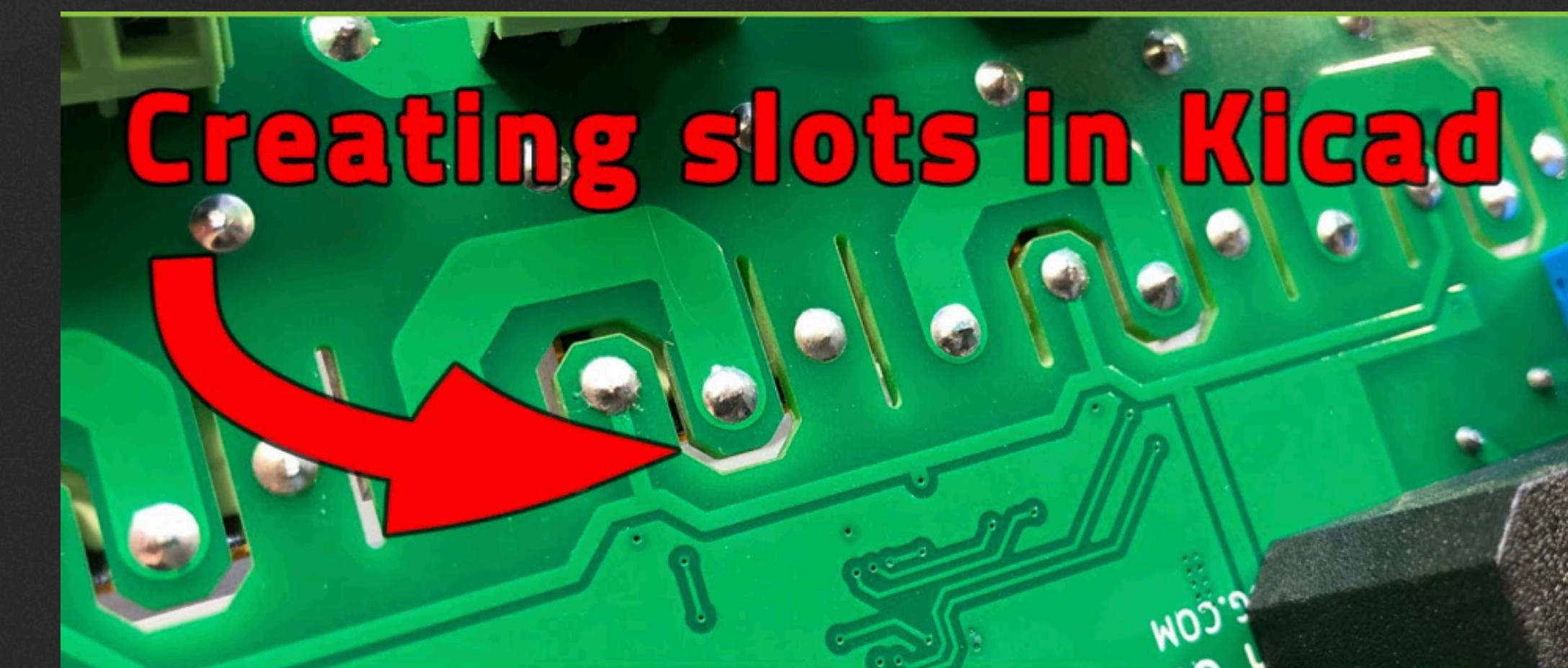
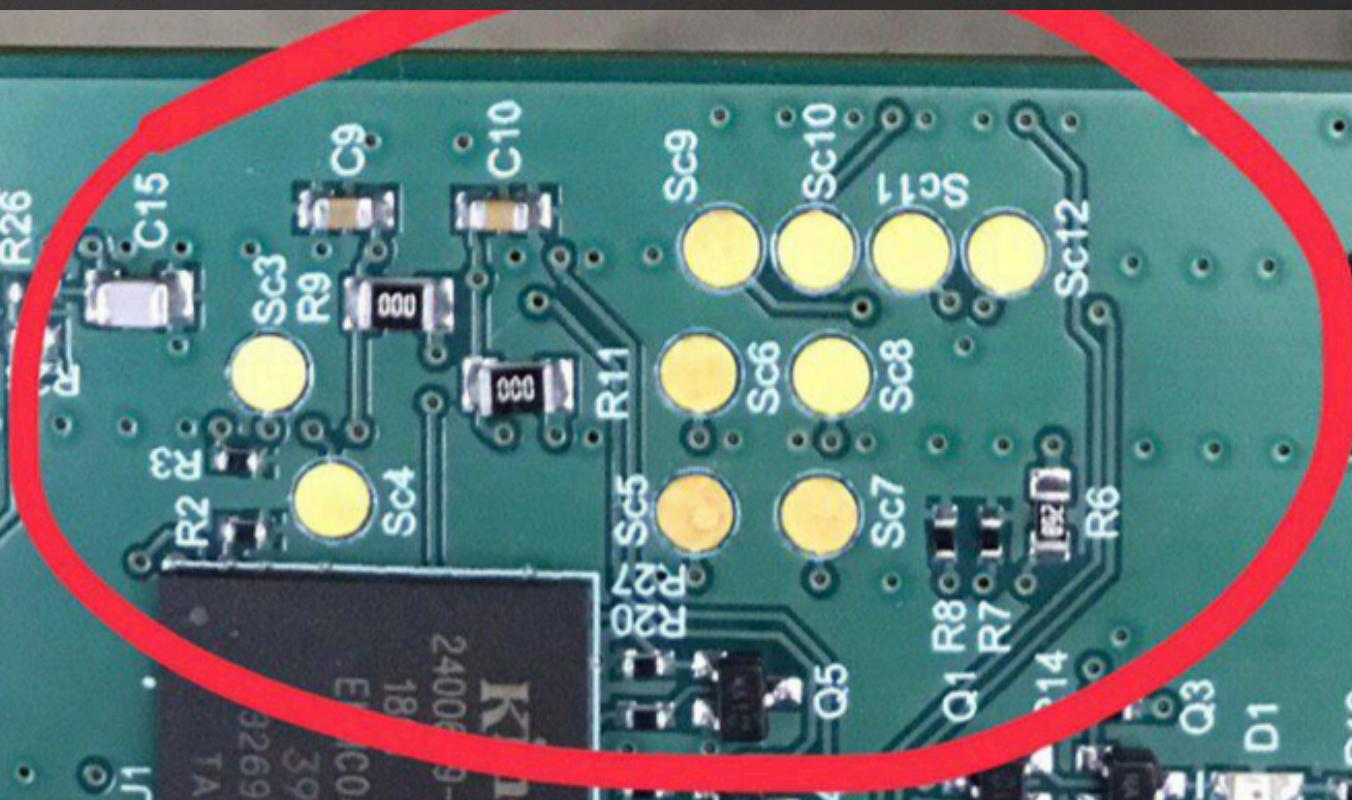
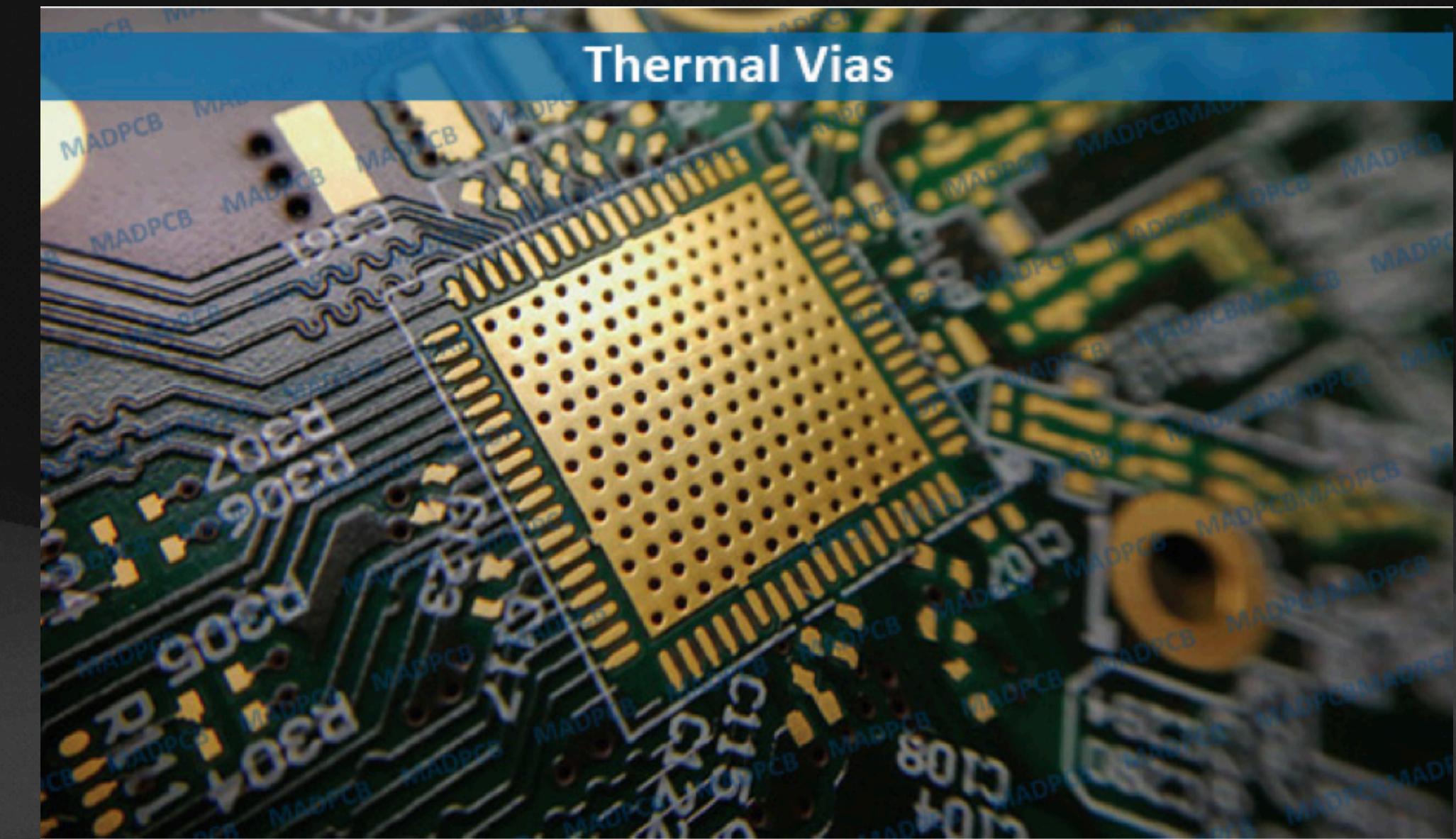
# routing vias

- Common practice to have vias under microcontroller
- Route traces on other layers
- Microcontroller usually has high density of traces, will have more complicated routing than rest of board



# routing considerations

- Thermal vias/thermal relief pads
- Isolation of high voltages (slots)
- Breakout/test points

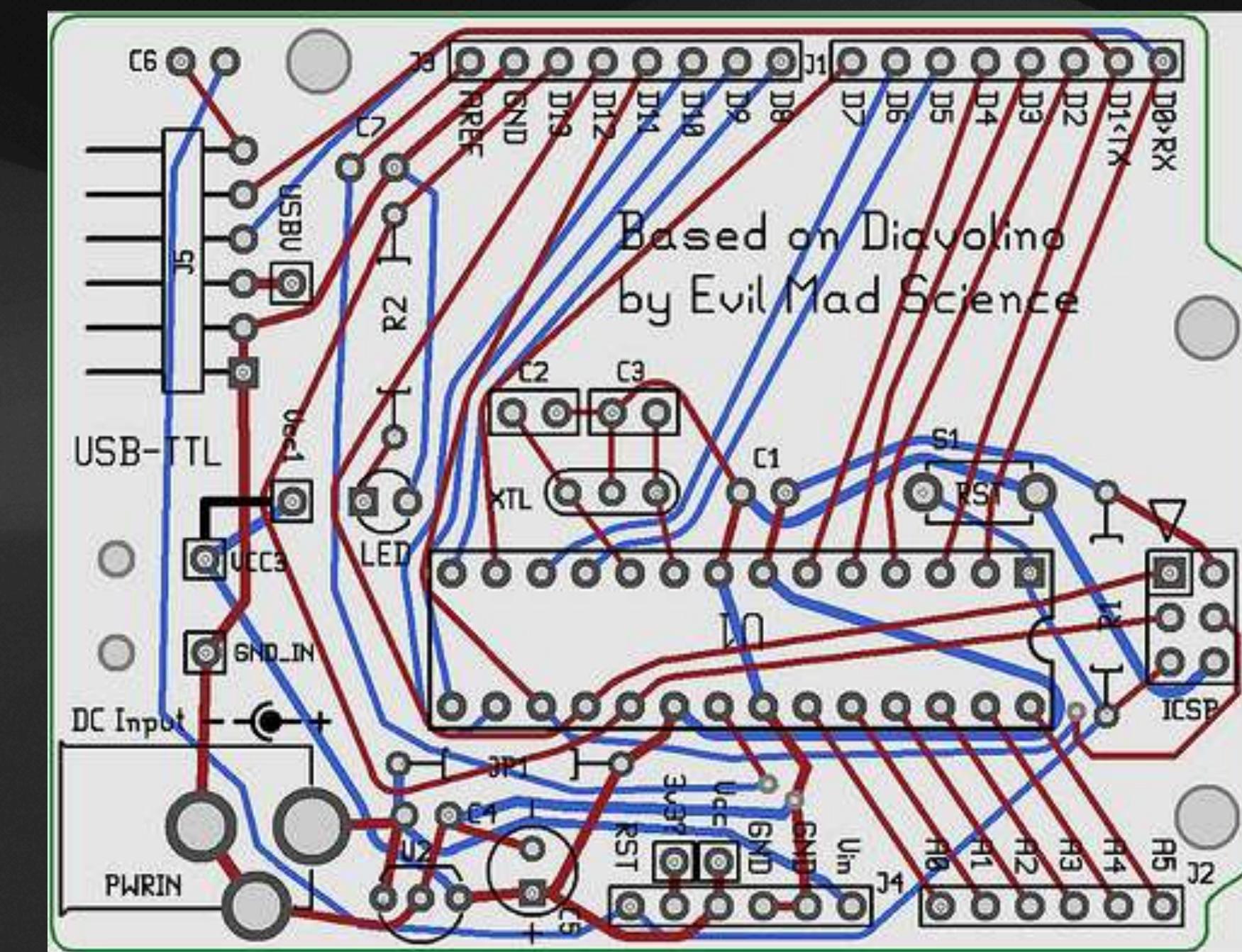
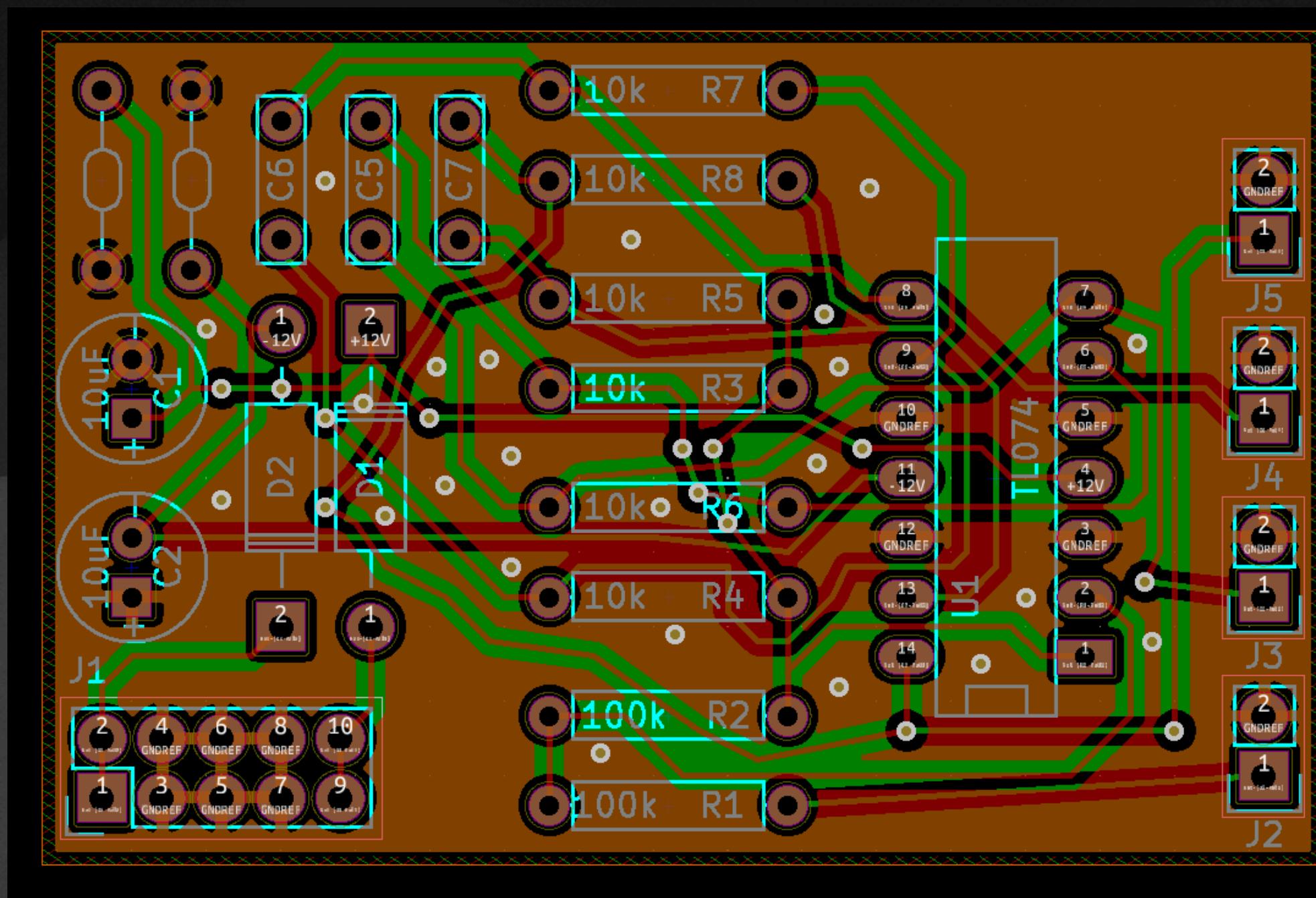


# routing

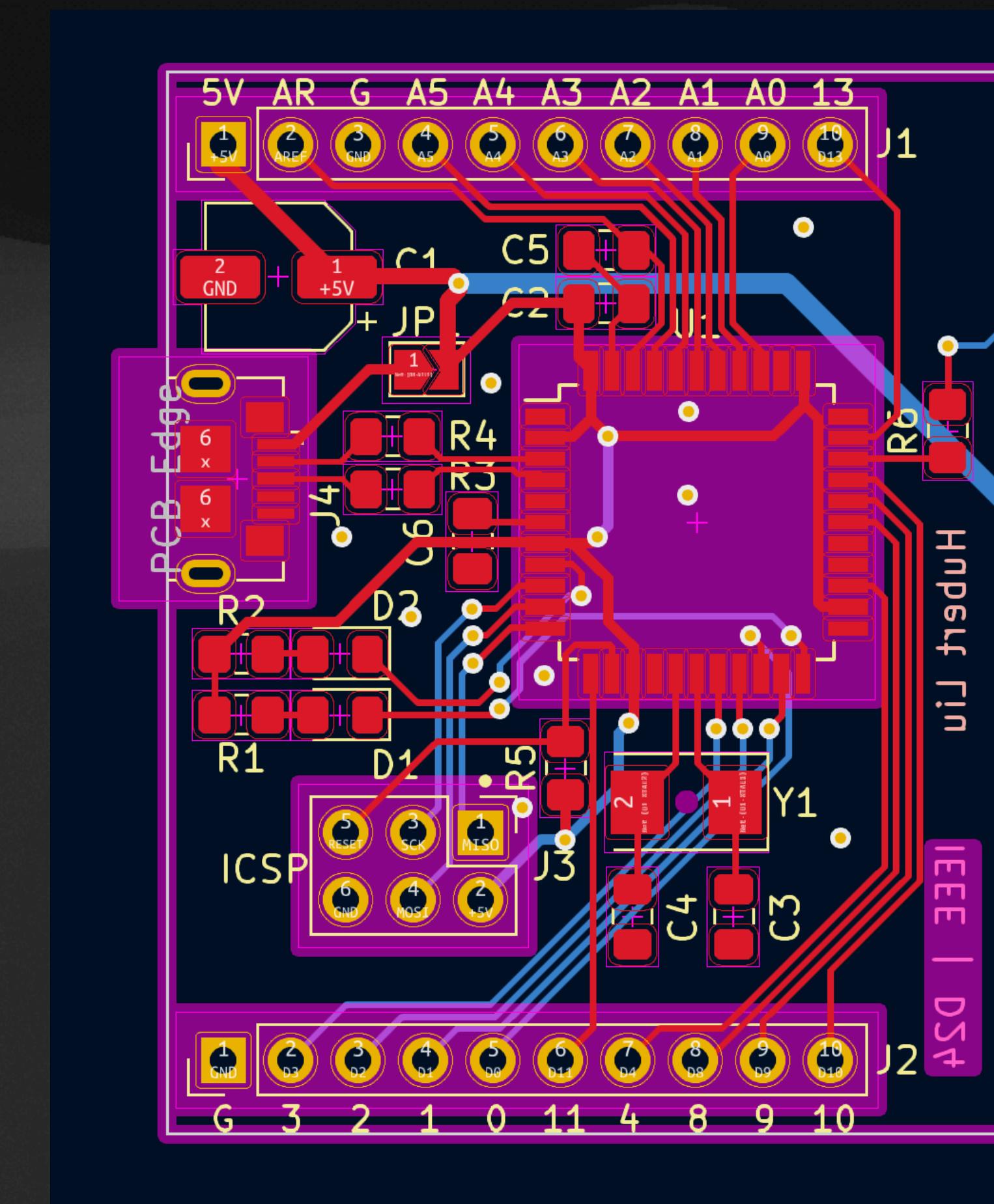
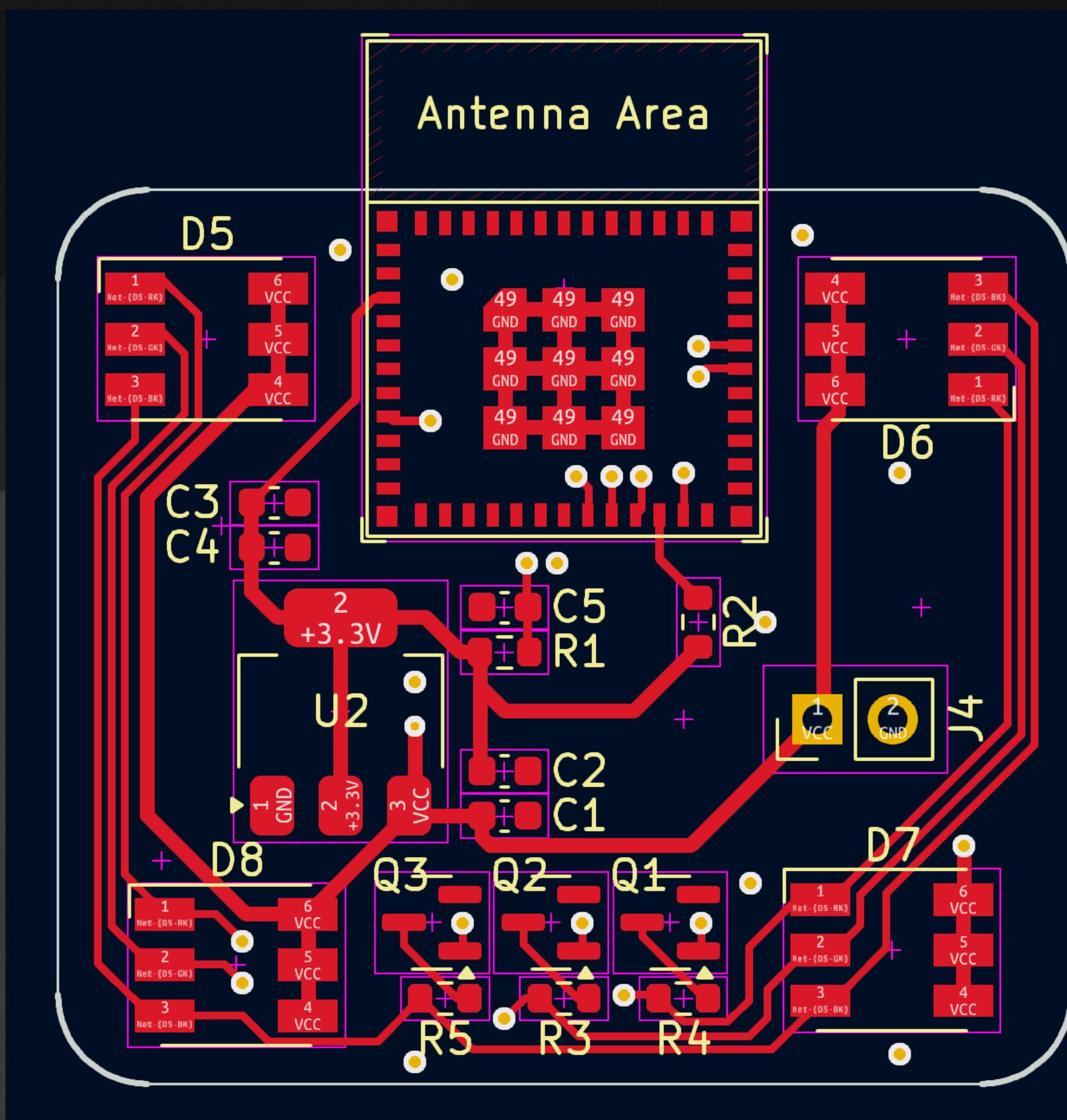
## EMI

- Large ground planes -- Minimize impedance
- Separate analog, digital, and high-speed components
- Connect all components -- Avoid unwanted antennas
- Minimize signal lengths
- Avoid right-angles (including vias)
- Shielding and Filtering

# routing the bad



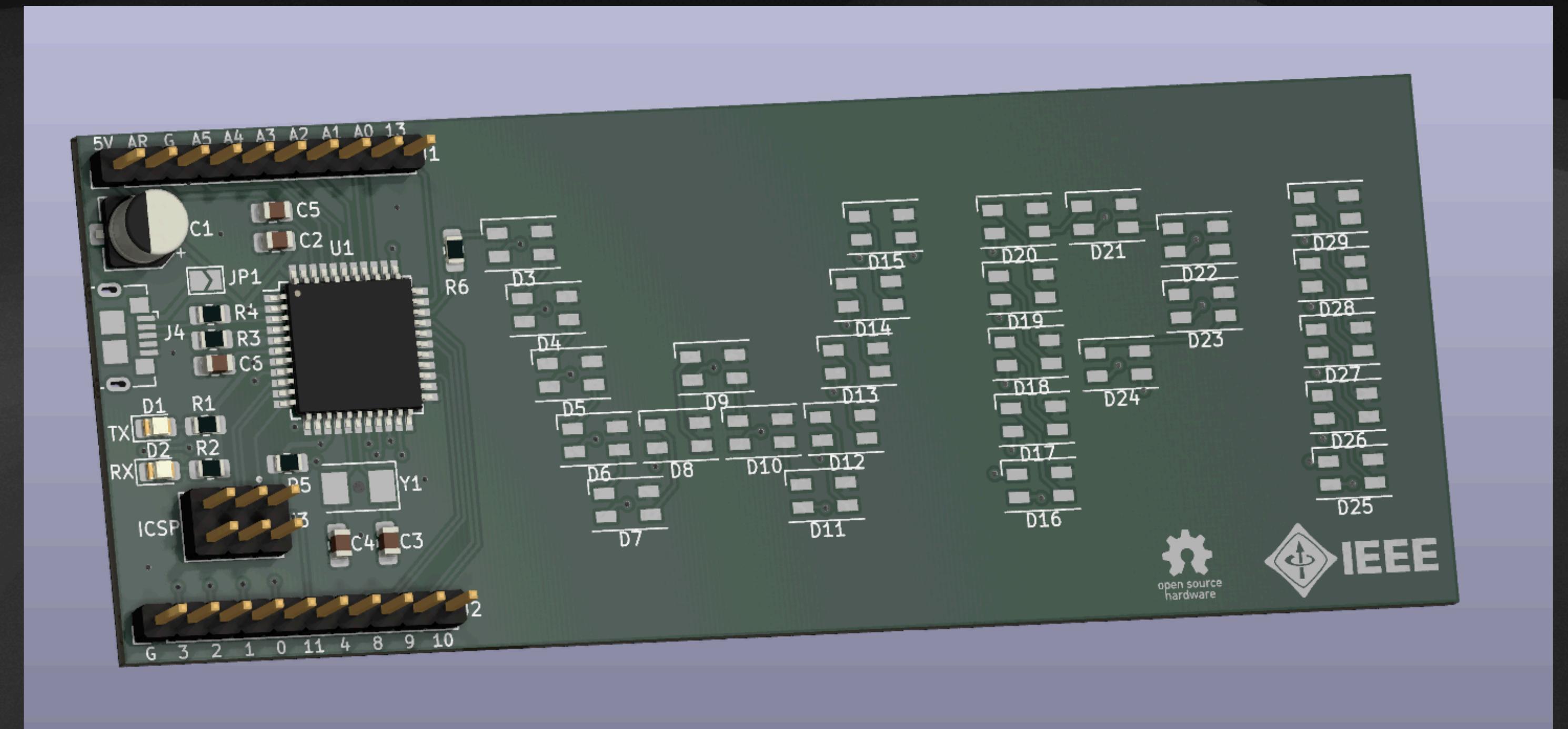
# routing the good



# hardware design process

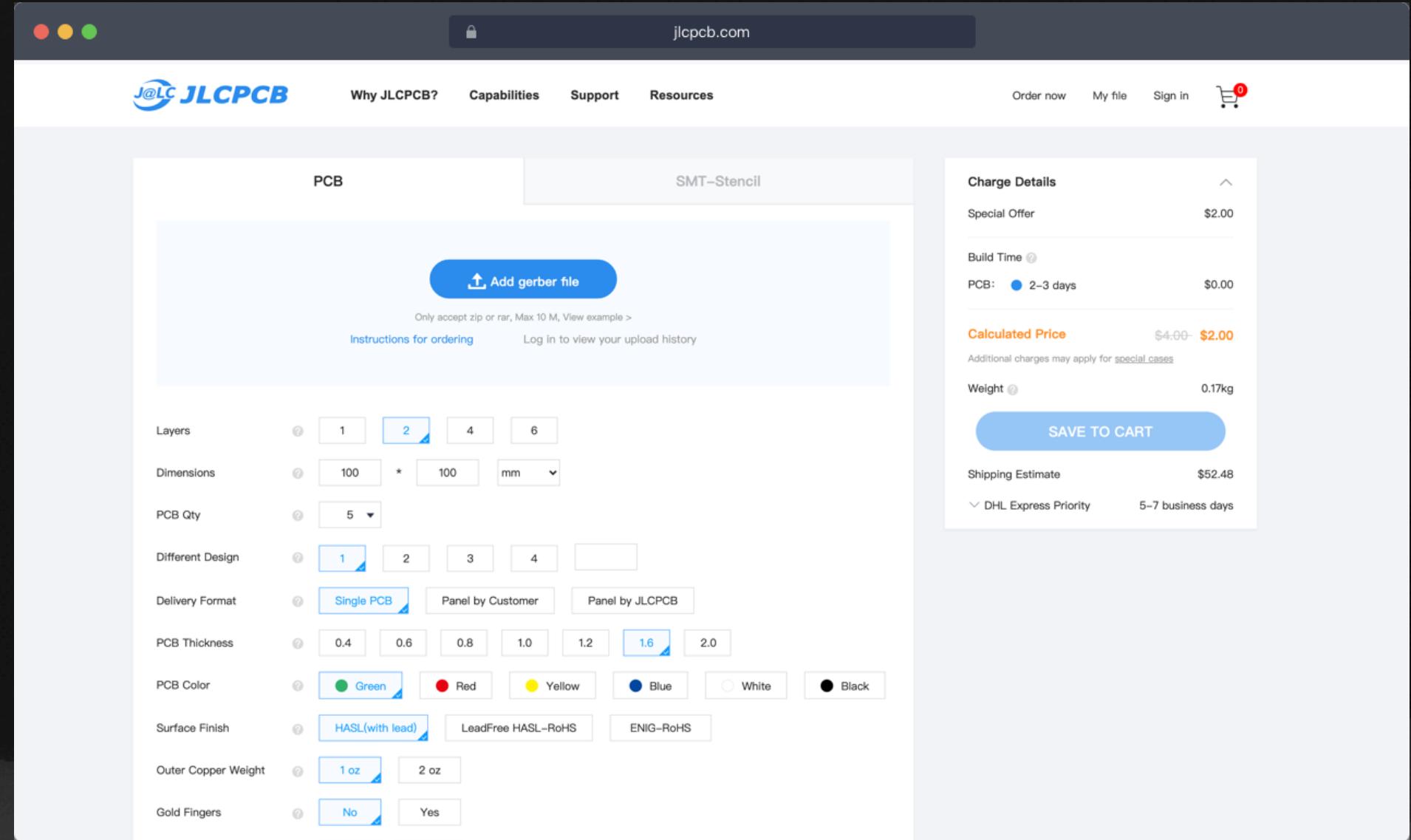
## walkthrough

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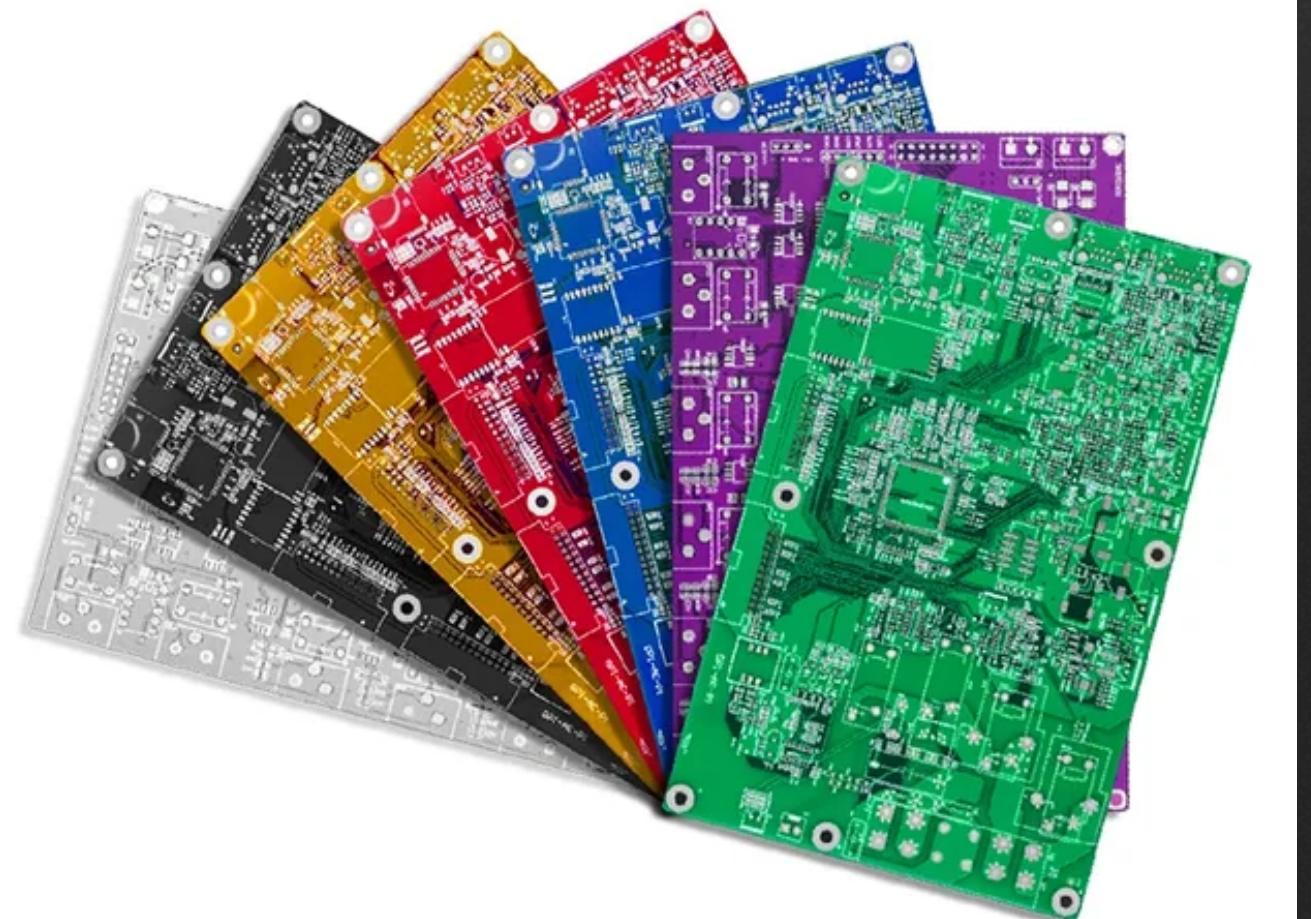


# ordering your board process

- Run DRC (design rules check) using fab's specified tolerances
- Export Gerber files in KiCad, upload to fab website and specify options (stencil if needed)
- If your board violates minimum tolerances, your order will be blocked
- Chinese fabs are ridiculously cheap and usual lead time is about a week
- Order parts from your favorite distributor.



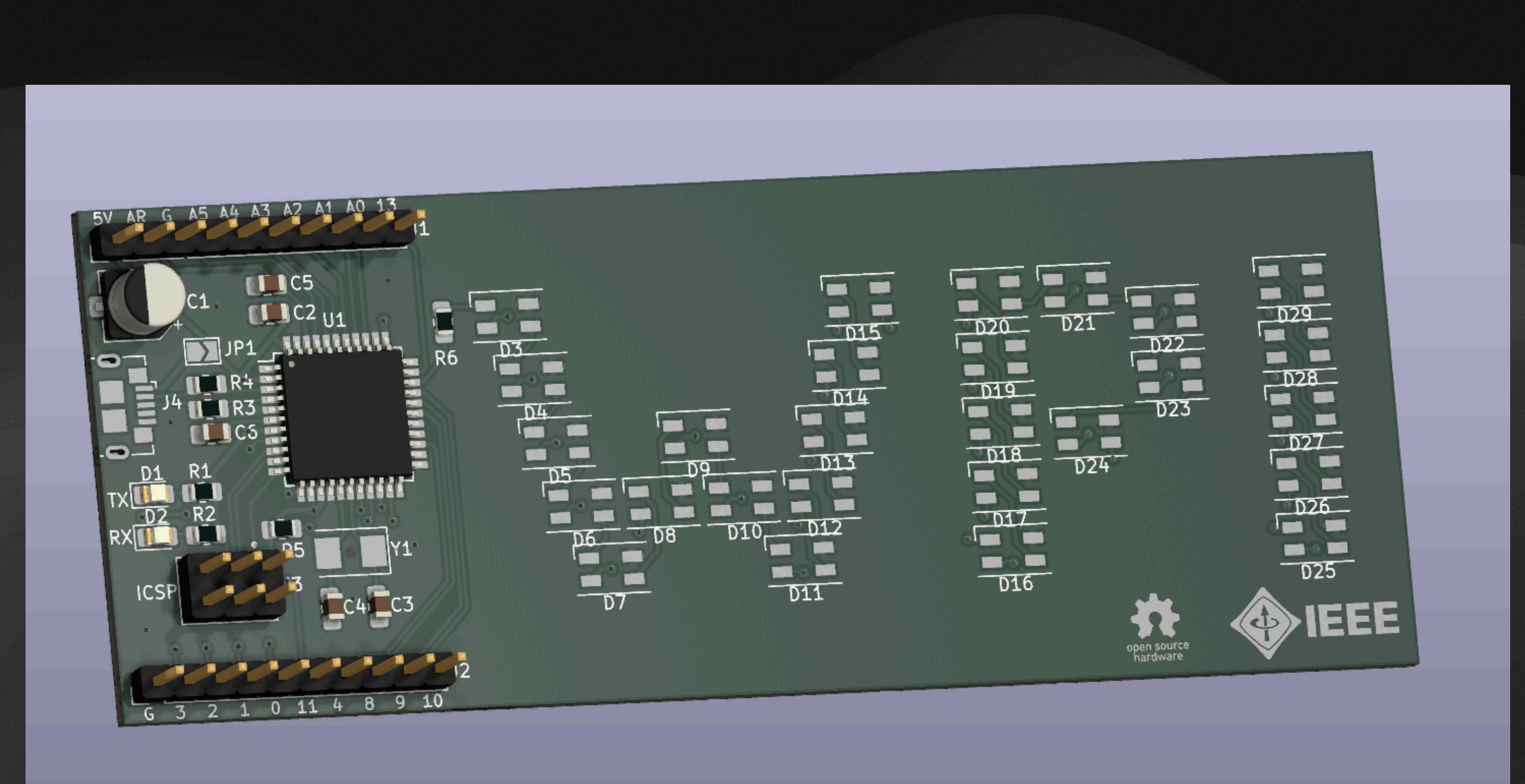
J@LC JLCPCB



# hardware design process

## walkthrough

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# assembly process

- Most SMT designs can most easily be soldered using a stencil
- Stencil has holes where component pads are
- Solder paste spread over stencil
- Components placed on solder paste
- Board place in reflow oven
- Yay it's finished!

