

## Chapter 5 General Register Files (GRF)

### 5.1 Overview

The general register file will be used to do static set by software, which is composed of many registers for system control. The GRF is divided into two sections,

- GRF, used for general non-secure system,
- PMUGRF, used for always on sysyem

### 5.2 Function Description

The function of general register file is:

- IOMUX control
- Control the state of GPIO in power-down mode
- GPIO PAD pull down and pull up control
- Used for common system control
- Used to record the system state

### 5.3 GRF Register Description

#### 5.3.1 Register Summary

Name	Offset	Size	Reset Value	Description
GRF_GPIO1A_IOMUX	0x00000	W	0x00000000	GPIO1A iomux control
GRF_GPIO1B_IOMUX	0x00004	W	0x00000000	GPIO1B iomux control
GRF_GPIO1C_IOMUX	0x00008	W	0x00000000	GPIO1C iomux control
GRF_GPIO1D_IOMUX	0x0000c	W	0x00000000	GPIO1D iomux control
GRF_GPIO2A_IOMUX	0x00010	W	0x00000000	GPIO2A iomux control
GRF_GPIO2B_IOMUX	0x00014	W	0x00000040	GPIO2B iomux control
GRF_GPIO2C_IOMUX	0x00018	W	0x00000000	GPIO2C iomux control
GRF_GPIO2D_IOMUX	0x0001c	W	0x00000000	GPIO2D iomux control
GRF_GPIO3A_IOMUX	0x00020	W	0x00000000	GPIO3A iomux control
GRF_GPIO3B_IOMUX	0x00024	W	0x00000000	GPIO3B iomux control
GRF_GPIO3C_IOMUX	0x00028	W	0x00000000	GPIO3C iomux control
GRF_GPIO3D_IOMUX	0x0002c	W	0x00000000	GPIO3D iomux control
GRF_GPIO1A_P	0x00100	W	0x0000aaaa	GPIO1A PU/PD control
GRF_GPIO1B_P	0x00104	W	0x0000aaaa	GPIO1B PU/PD control
GRF_GPIO1C_P	0x00108	W	0x00005555	GPIO1C PU/PD control
GRF_GPIO1D_P	0x0010c	W	0x00006995	GPIO1D PU/PD control
GRF_GPIO2A_P	0x00110	W	0x00005555	GPIO2A PU/PD control
GRF_GPIO2B_P	0x00114	W	0x0000aa59	GPIO2B PU/PD control
GRF_GPIO2C_P	0x00118	W	0x000096aa	GPIO2C PU/PD control

Name	Offset	Size	Reset Value	Description
GRF_GPIO2D_P	0x0011c	W	0x00005559	GPIO2D PU/PD control
GRF_GPIO3A_P	0x00120	W	0x00005a99	GPIO3A PU/PD control
GRF_GPIO3B_P	0x00124	W	0x000099aa	GPIO3B PU/PD control
GRF_GPIO3C_P	0x00128	W	0x000069a5	GPIO3C PU/PD control
GRF_GPIO3D_P	0x0012c	W	0x00005655	GPIO3D PU/PD control
GRF_GPIO1A_E	0x00200	W	0x00000000	GPIO1A drive strength control
GRF_GPIO1B_E	0x00204	W	0x00000800	GPIO1B drive strength control
GRF_GPIO1C_E	0x00208	W	0x0000aaa0	GPIO1C drive strength control
GRF_GPIO1D_E	0x0020c	W	0x00000002	GPIO1D drive strength control
GRF_GPIO2A_E	0x00210	W	0x00005655	GPIO2A drive strength control
GRF_GPIO2B_E	0x00214	W	0x00000119	GPIO2B drive strength control
GRF_GPIO2C_E	0x00218	W	0x00000000	GPIO2C drive strength control
GRF_GPIO2D_E	0x0021c	W	0x00005500	GPIO2D drive strength control
GRF_GPIO3A_E	0x00220	W	0x00000009	GPIO3A drive strength control
GRF_GPIO3B_E	0x00224	W	0x0000682a	GPIO3B drive strength control
GRF_GPIO3C_E	0x00228	W	0x00003115	GPIO3C drive strength control
GRF_GPIO3D_E	0x0022c	W	0x00000304	GPIO3D drive strength control
GRF_GPIO1L_SR	0x00300	W	0x00000800	GPIO1A/B SR control
GRF_GPIO1H_SR	0x00304	W	0x00000000	GPIO1C/D SR control
GRF_GPIO2L_SR	0x00308	W	0x00000200	GPIO2A/B SR control
GRF_GPIO2H_SR	0x0030c	W	0x00000000	GPIO2C/D SR control
GRF_GPIO3L_SR	0x00310	W	0x00004702	GPIO3A/B SR control
GRF_GPIO3H_SR	0x00314	W	0x00000040	GPIO3C/D SR control
GRF_GPIO_SMT	0x00380	W	0x00000315	GPIO smitter control register
GRF_SOC_CON0	0x00400	W	0x00000038	SoC control register 0
GRF_SOC_CON1	0x00404	W	0x000001c0	SoC control register 1
GRF_SOC_CON2	0x00408	W	0x000007f0	SoC control register 2
GRF_SOC_CON3	0x0040c	W	0x00002020	SoC control register 3

Name	Offset	Size	Reset Value	Description
GRF_SOC_CON4	0x00410	W	0x00002001	SoC control register 4
GRF_SOC_CON5	0x00414	W	0x00000000	SoC control register 5
GRF_SOC_CON6	0x00418	W	0x00000000	SoC control register 6
GRF_SOC_CON7	0x0041c	W	0x00000000	SoC control register 7
GRF_SOC_CON8	0x00420	W	0x00007538	SoC control register 8
GRF_SOC_CON9	0x00424	W	0x00000100	SoC control register 9
GRF_SOC_CON10	0x00428	W	0x00000000	SoC control register 10
GRF_SOC_CON11	0x0042c	W	0x00002000	SoC control register 11
GRF_SOC_CON12	0x00430	W	0x00006000	SoC control register 12
GRF_SOC_CON13	0x00434	W	0x00000000	SoC control register 13
GRF_SOC_CON14	0x00438	W	0x00000000	SoC control register 14
GRF_SOC_CON15	0x0043c	W	0x00002000	SoC control register 15
GRF_SOC_CON16	0x00440	W	0x00000000	SoC control register 16
GRF_SOC_CON17	0x00444	W	0x00000000	SoC control register 17
GRF_SOC_STATUS0	0x00480	W	0x00000000	SoC status register 0
GRF_SOC_STATUS1	0x00484	W	0x00000000	SoC status register 1
GRF_SOC_STATUS2	0x00488	W	0x00000000	SoC status register 2
GRF_SOC_STATUS3	0x0048c	W	0x00000000	SoC status register 3
GRF_SOC_STATUS4	0x00490	W	0x00000000	SoC status register 4
GRF_SOC_STATUS5	0x00494	W	0x00000000	SoC status register 5
GRF_SOC_STATUS6	0x00498	W	0x00000000	SoC status register 6
GRF_SOC_STATUS7	0x0049c	W	0x00000000	SoC status register 7
GRF_SOC_STATUS8	0x004a0	W	0x00000000	SoC status register 8
GRF_SOC_STATUS9	0x004a4	W	0x00000000	SoC status register 9
GRF_SOC_STATUS10	0x004a8	W	0x00000000	SoC status register 10
GRF_SOC_STATUS11	0x004ac	W	0x00000000	SoC status register 11
GRF_SOC_STATUS12	0x004b0	W	0x00000000	SoC status register 12
GRF_SOC_STATUS13	0x004b4	W	0x00000000	SoC status register 13
GRF_SOC_STATUS14	0x004b8	W	0x00000000	SoC status register 14
GRF_SOC_STATUS15	0x004bc	W	0x00000000	SoC status register 15
GRF_CPU_CON0	0x00500	W	0x0000000b	CPU little cluster control register 0
GRF_CPU_CON1	0x00504	W	0x00000000	CPU little cluster control register 1
GRF_CPU_CON2	0x00508	W	0x0000000b	CPU big cluster control register 2
GRF_CPU_CON3	0x0050c	W	0x00000000	CPU big cluster control register 1
GRF_CPU_STATUS0	0x00520	W	0x00000000	CPU status register 0
GRF_CPU_STATUS1	0x00524	W	0x00000000	CPU status register 1

Name	Offset	Size	Reset Value	Description
GRF_CCI_STATUS0	0x00540	W	0x00000000	CCI status register 0
GRF_CCI_STATUS1	0x00544	W	0x00000000	CCI status register 1
GRF_CCI_STATUS2	0x00548	W	0x00000000	CCI status register 2
GRF_CCI_STATUS3	0x0054c	W	0x00000000	CCI status register 3
GRF_CCI_STATUS4	0x00550	W	0x00000000	CCI status register 4
GRF_CCI_STATUS5	0x00554	W	0x00000000	CCI status register 5
GRF_CCI_STATUS6	0x00558	W	0x00000000	CCI status register 6
GRF_CCI_STATUS7	0x0055c	W	0x00000000	CCI status register 7
GRF_CCI_STATUS8	0x00560	W	0x00000000	CCI status register 8
GRF_CCI_STATUS9	0x00564	W	0x00000000	CCI status register 9
GRF_CCI_STATUS10	0x00568	W	0x00000000	CCI status register 10
GRF_CCI_STATUS11	0x0056c	W	0x00000000	CCI status register 11
GRF_CCI_STATUS12	0x00570	W	0x00000000	CCI status register 12
GRF_CCI_STATUS13	0x00574	W	0x00000000	CCI status register 13
GRF_CCI_STATUS14	0x00578	W	0x00000000	CCI status register 14
GRF_CCI_STATUS15	0x0057c	W	0x00000000	CCI status register 15
GRF_DDRC0_CON0	0x00600	W	0x00000000	DDRC0 control register 0
GRF_SIG_DETECT_CON	0x00680	W	0x00000000	external signal detect configue register
GRF_SIG_DETECT_STATUS	0x00690	W	0x00000000	external signal detect configue register
GRF_SIG_DETECT_CLR	0x006a0	W	0x00000000	external signal detect configue register
GRF_UOC0_CON0	0x00700	W	0x00000000	OTG control register
GRF_UOC1_CON1	0x00718	W	0x00000000	usb host control register
GRF_UOC1_CON2	0x0071c	W	0x0000c820	UOC1 control register 2
GRF_UOC1_CON3	0x00720	W	0x00000b40	UOC1 control register 3
GRF_UOC1_CON4	0x00724	W	0x0000001c	USB HOST 2.0 control register
GRF_UOC1_CON5	0x00728	W	0x00000000	USB HOST 2.0 control register
GRF_UOC3_CON0	0x00738	W	0x000030eb	UOC3 control register 0
GRF_UOC3_CON1	0x0073c	W	0x00000003	UOC3 control register 1
GRF_UOC4_CON0	0x00740	W	0x00000080	UOC4 control register 0
GRF_UOC4_CON1	0x00744	W	0x00000820	UOC4 control register 1
GRF_USBPHY_CON0	0x00780	W	0x00008518	USB PHY control register
GRF_USBPHY_CON1	0x00784	W	0x0000e007	USB PHY control register
GRF_USBPHY_CON2	0x00788	W	0x000002e7	USB PHY control register
GRF_USBPHY_CON3	0x0078c	W	0x00000200	USB PHY control register
GRF_USBPHY_CON4	0x00790	W	0x00005556	USB PHY control register

Name	Offset	Size	Reset Value	Description
GRF_USBPHY_CON5	0x00794	W	0x00004555	USB PHY control register
GRF_USBPHY_CON6	0x00798	W	0x00000005	USB PHY control register
GRF_USBPHY_CON7	0x0079c	W	0x000068c0	USB PHY control register
GRF_USBPHY_CON8	0x007a0	W	0x00008518	USB PHY control register
GRF_USBPHY_CON9	0x007a4	W	0x0000e007	USB PHY control register
GRF_USBPHY_CON10	0x007a8	W	0x000002e7	USB PHY control register
GRF_USBPHY_CON11	0x007ac	W	0x00000200	USB PHY control register
GRF_USBPHY_CON12	0x007b0	W	0x00005556	USB PHY control register
GRF_USBPHY_CON13	0x007b4	W	0x00004555	USB PHY control register
GRF_USBPHY_CON14	0x007b8	W	0x00000005	USB PHY control register
GRF_USBPHY_CON15	0x007bc	W	0x000068c0	USB PHY control register
GRF_PVTM_CON0	0x00800	W	0x00000000	PVT monitor control register 0
GRF_PVTM_CON1	0x00804	W	0x016e3600	PVT monitor control register 1
GRF_PVTM_CON2	0x00808	W	0x016e3600	PVT monitor control register 2
GRF_PVTM_STATUS0	0x0080c	W	0x00000000	PVT monitor status register 0
GRF_PVTM_STATUS1	0x00810	W	0x00000000	PVT monitor status register 1
GRF_PVTM_STATUS2	0x00814	W	0x00000000	PVT monitor status register 2
GRF_IO_VSEL	0x00900	W	0x00000004	IO voltage select
GRF_SARADC_TESTBIT	0x00904	W	0x00000000	SARADC Test bit register
GRF_FAST_BOOT_ADDRESS	0x00f80	W	0x00000000	Fast boot address

Notes: **Size** : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

### 5.3.2 Detail Register Description

#### GRF\_GPIO1A\_IOMUX

Address: Operational Base + offset (0x000000)  
GPIO1A iomux control

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1a7_sel GPIO1A[7] iomux select 2'b00: gpio 2'b01: cif_data9 2'b10: ts_data7 2'b11: reserved
13:12	RW	0x0	gpio1a6_sel GPIO1A[6] iomux select 2'b00: gpio 2'b01: cif_data8 2'b10: ts_data6 2'b11: reserved
11:10	RW	0x0	gpio1a5_sel GPIO1A[5] iomux select 2'b00: gpio 2'b01: cif_data7 2'b10: ts_data5 2'b11: reserved
9:8	RW	0x0	gpio1a4_sel GPIO1A[4] iomux select 2'b00: gpio 2'b01: cif_data6 2'b10: ts_data4 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio1a3_sel GPIO1A[3] iomux select 2'b00: gpio 2'b01: cif_data5 2'b10: ts_data3 2'b11: reserved
5:4	RW	0x0	gpio1a2_sel GPIO1A[2] iomux select 2'b00: gpio 2'b01: cif_data4 2'b10: ts_data2 2'b11: reserved
3:2	RW	0x0	gpio1a1_sel GPIO1A[1] iomux select 2'b00: gpio 2'b01: cif_data3 2'b10: ts_data1 2'b11: reserved
1:0	RW	0x0	gpio1a0_sel GPIO1A[0] iomux select 2'b00: gpio 2'b01: cif_data2 2'b10: ts_data0 2'b11: reserved

**GRF\_GPIO1B\_IOMUX**

Address: Operational Base + offset (0x00004)

GPIO1B iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1b7_sel GPIO1B[7] iomux select 2'b00: gpio 2'b01: cif_data11 2'b10: spi1_csn0 2'b11: reserved
13:12	RW	0x0	gpio1b6_sel GPIO1B[6] iomux select 2'b00: gpio 2'b01: cif_data10 2'b10: spi1_clk 2'b11: reserved
11:10	RW	0x0	gpio1b5_sel GPIO1B[5] iomux select 2'b00: gpio 2'b01: cif_data1 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio1b4_sel GPIO1B4] iomux select 2'b00: gpio 2'b01: cif_data0 2'b10: reserved 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio1b3_sel GPIO1B[3] iomux select 2'b00: gpio 2'b01: cif_clkout 2'b10: ts_fail 2'b11: reserved
5:4	RW	0x0	gpio1b2_sel GPIO1B[2] iomux select 2'b00: gpio 2'b01: cif_clkin 2'b10: ts_clk 2'b11: reserved
3:2	RW	0x0	gpio1b1_sel GPIO1B[1] iomux select 2'b00: gpio 2'b01: cif_href 2'b10: ts_valid 2'b11: reserved
1:0	RW	0x0	gpio1b0_sel GPIO1B[0] iomux select 2'b00: gpio 2'b01: cif_vsync 2'b10: ts_sync 2'b11: reserved

**GRF\_GPIO1C\_IOMUX**

Address: Operational Base + offset (0x00008)

GPIO1C iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1c7_sel GPIO1C[7] iomux select 2'b00: gpio 2'b01: flash_data5 2'b10: emmc_data5 2'b11: spi0_txd
13:12	RW	0x0	gpio1c6_sel GPIO1C[6] iomux select 2'b00: gpio 2'b01: flash_data4 2'b10: emmc_data4 2'b11: spi0_rxd
11:10	RW	0x0	gpio1c5_sel GPIO1C[5] iomux select 2'b00: gpio 2'b01: flash_data3 2'b10: emmc_data3 2'b11: sfc_sio3
9:8	RW	0x0	gpio1c4_sel GPIO1C4] iomux select 2'b00: gpio 2'b01: flash_data2 2'b10: emmc_data2 2'b11: sfc_sio2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio1c3_sel GPIO1C[3] iomux select 2'b00: gpio 2'b01: flash_data1 2'b10: emmc_data1 2'b11: sfc_sio1
5:4	RW	0x0	gpio1c2_sel GPIO1C[2] iomux select 2'b00: gpio 2'b01: flash_data0 2'b10: emmc_data0 2'b11: sfc_sio0
3:2	RW	0x0	gpio1c1_sel GPIO1C[1] iomux select 2'b00: gpio 2'b01: i2c3cam_sda 2'b10: spi1_txd 2'b11: reserved
1:0	RW	0x0	gpio1c0_sel GPIO1C[0] iomux select 2'b00: gpio 2'b01: i2c3cam_scl 2'b10: spi1_rxd 2'b11: reserved

**GRF\_GPIO1D\_IOMUX**

Address: Operational Base + offset (0x0000c)

GPIO1D iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio1d7_sel GPIO1D[7] iomux select 2'b00: gpio 2'b01: flash_wrn 2'b10: sfc_csn0 2'b11: reserved
13:12	RW	0x0	gpio1d6_sel GPIO1D[6] iomux select 2'b00: gpio 2'b01: flash_cle 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio1d5_sel GPIO1D[5] iomux select 2'b00: gpio 2'b01: flash_ale 2'b10: spi0_clk 2'b11: reserved
9:8	RW	0x0	gpio1d4_sel GPIO1D[4] iomux select 2'b00: gpio 2'b01: flash_rdn 2'b10: sfc_csn1 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio1d3_sel GPIO1D[3] iomux select 2'b00: gpio 2'b01: flash_wp 2'b10: emmc_pwren 2'b11: reserved
5:4	RW	0x0	gpio1d2_sel GPIO1D[2] iomux select 2'b00: gpio 2'b01: flash_rdy 2'b10: emmc_cmd 2'b11: sfc_clk
3:2	RW	0x0	gpio1d1_sel GPIO1D[1] iomux select 2'b00: gpio 2'b01: flash_data7 2'b10: emmc_data7 2'b11: spi0_csn1
1:0	RW	0x0	gpio1d0_sel GPIO1D[0] iomux select 2'b00: gpio 2'b01: flash_data6 2'b10: emmc_data6 2'b11: spi0_csn0

**GRF\_GPIO2A\_IOMUX**

Address: Operational Base + offset (0x00010)

GPIO2A iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:14	RW	0x0	<p>gpio2a7_sel</p> <p>GPIO2A[7] iomux select</p> <p>2'b00: gpio</p> <p>2'b01: sdmmc0_data2</p> <p>2'b10: jtag_tck</p> <p>2'b11: reserved</p>
13:12	RW	0x0	<p>gpio2a6_sel</p> <p>GPIO2A[6] iomux select</p> <p>2'b00: gpio</p> <p>2'b01: sdmmc0_data1</p> <p>2'b10: uart2dbg_sin</p> <p>2'b11: reserved</p>
11:10	RW	0x0	<p>gpio2a5_sel</p> <p>GPIO2A[5] iomux select</p> <p>2'b00: gpio</p> <p>2'b01: sdmmc0_data0</p> <p>2'b10: uart2dbg_sout</p> <p>2'b11: reserved</p>
9:8	RW	0x0	<p>gpio2a4_sel</p> <p>GPIO2A[4] iomux select</p> <p>2'b00: gpio</p> <p>2'b01: flash_dqs</p> <p>2'b10: emmc_clkout</p> <p>2'b11: reserved</p>

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2a3_sel GPIO2A[3] iomux select 2'b00: gpio 2'b01: flash_csn3 2'b10: emmc_rstnout 2'b11: reserved
5:4	RW	0x0	gpio2a2_sel GPIO2A[2] iomux select 2'b00: gpio 2'b01: flash_csn2 2'b10: reserved 2'b11: reserved
3:2	RW	0x0	gpio2a1_sel GPIO2A[1] iomux select 2'b00: gpio 2'b01: flash_csn1 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio2a0_sel GPIO2A[0] iomux select 2'b00: gpio 2'b01: flash_csn0 2'b10: reserved 2'b11: reserved

**GRF\_GPIO2B\_IOMUX**

Address: Operational Base + offset (0x00014)

GPIO2B iomux control

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2b7_sel GPIO2B[7] iomux select 2'b00: gpio 2'b01: i2s_sdi 1'b10: reserved 1'b11: reserved
13:12	RW	0x0	gpio2b6_sel GPIO2B[6] iomux select 2'b00: gpio 2'b01: i2s_lrcktx 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio2b5_sel GPIO2B[5] iomux select 2'b00: gpio 2'b01: i2s_lrckrx 2'b10: pcm_sync 2'b11: reserved
9:8	RW	0x0	gpio2b4_sel GPIO2B[4] iomux select 2'b00: gpio 2'b01: i2s_sclk 2'b10: reserved 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x1	gpio2b3_sel GPIO2B[3] iomux select 2'b00: gpio 2'b01: sdmmc0_dtectrn 2'b10: reserved 2'b11: reserved
5:4	RW	0x0	gpio2b2_sel GPIO2B[2] iomux select 2'b00: gpio 2'b01: sdmmc0_cmd 2'b10: mcujtag_tms 2'b11: reserved
3:2	RW	0x0	gpio2b1_sel GPIO2B[1] iomux select 2'b00: gpio 2'b01: sdmmc0_clkout 2'b10: mcujtag_tck 2'b11: reserved
1:0	RW	0x0	gpio2b0_sel GPIO2B[0] iomux select 2'b00: gpio 2'b01: sdmmc0_data3 2'b10: jtag_tms 2'b11: reserved

**GRF\_GPIO2C\_IOMUX**

Address: Operational Base + offset (0x00018)

GPIO2C iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2c7_sel GPIO2C[7] iomux select 2'b00: gpio 2'b01: spdif_tx 2'b10: edp_hpd 2'b11: reserved
13:12	RW	0x0	gpio2c6_sel GPIO2C[6] iomux select 2'b00: gpio 2'b01: i2c1audio_scl 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio2c5_sel GPIO2C[5] iomux select 2'b00: gpio 2'b01: i2c1audio_sda 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio2c4_sel GPIO2C[4] iomux select 2'b00: gpio 2'b01: i2s_clk 2'b10: reserved 2'b11: reserved

Bit	Attr	Reset Value	Description
7:6	RW	0x0	gpio2c3_sel GPIO2C[3] iomux select 2'b00: gpio 2'b01: i2s_sdo3 2'b10: pcm_in 2'b11: reserved
5:4	RW	0x0	gpio2c2_sel GPIO2C[2] iomux select 2'b00: gpio 2'b01: i2s_sdo2 2'b10: pcm_clk 2'b11: reserved
3:2	RW	0x0	gpio2c1_sel GPIO2C[1] iomux select 2'b00: gpio 2'b01: i2s_sdo1 2'b10: pcm_out 2'b11: reserved
1:0	RW	0x0	gpio2c0_sel GPIO2C[0] iomux select 2'b00: gpio 2'b01: i2s_sdo0 2'b10: reserved 2'b11: reserved

**GRF\_GPIO2D\_IOMUX**

Address: Operational Base + offset (0x0001c)

GPIO2D iomux control

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio2d7_sel GPIO2D[7] iomux select 2'b00: gpio 2'b01: sdio0_data3 2'b10: reserved 2'b11: reserved
13:12	RW	0x0	gpio2d6_sel GPIO2D[6] iomux select 2'b00: gpio 2'b01: sdio0_data2 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio2d5_sel GPIO2D[5] iomux select 2'b00: gpio 2'b01: sdio0_data1 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio2d4_sel GPIO2D[4] iomux select 2'b00: gpio 2'b01: sdio0_data0 2'b10: reserved 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio2d3_sel GPIO2D[3] iomux select 2'b00: gpio 2'b01: uart0bt_rtsn 2'b10: reserved 2'b11: reserved
5:4	RW	0x0	gpio2d2_sel GPIO2D[2] iomux select 2'b00: gpio 2'b01: uart0bt_ctsn 2'b10: reserved 2'b11: reserved
3:2	RW	0x0	gpio2d1_sel GPIO2D[1] iomux select 2'b00: gpio 2'b01:uart0bt_sout 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio2d0_sel GPIO2D[0] iomux select 2'b00: gpio 2'b01: uart0bt_sin 2'b10: reserved 2'b11: reserved

**GRF\_GPIO3A\_IOMUX**

Address: Operational Base + offset (0x00020)

GPIO3A iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio3a7_sel GPIO3A[7] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
13:12	RW	0x0	gpio3a6_sel GPIO3A[6] iomux select 2'b00: gpio 2'b01: sdio0_intn 2'b10: reserved 2'b11: reserved
11:10	RW	0x0	gpio3a5_sel GPIO3A[5] iomux select 2'b00: gpio 2'b01: sdio0_bkpwr 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio3a4_sel GPIO3A[4] iomux select 2'b00: gpio 2'b01: sdio0_pwren 2'b10: reserved 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio3a3_sel GPIO3A[3] iomux select 2'b00: gpio 2'b01: sdio0_wrprt 2'b10: reserved 2'b11: reserved
5:4	RW	0x0	gpio3a2_sel GPIO3A[2] iomux select 2'b00: gpio 2'b01: sdio0_detectn 2'b10: reserved 2'b11: reserved
3:2	RW	0x0	gpio3a1_sel GPIO3A[1] iomux select 2'b00: gpio 2'b01: sdio0_clkout 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio3a0_sel GPIO3A[0] iomux select 2'b00: gpio 2'b01: sdio0_cmd 2'b10: reserved 2'b11: reserved

**GRF\_GPIO3B\_IOMUX**

Address: Operational Base + offset (0x00024)

GPIO3B iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio3b7_sel GPIO3B[7] iomux select 2'b00: gpio 2'b01: max_rxd0 2'b10: gps_sig 2'b11: reserved
13:12	RW	0x0	gpio3b6_sel GPIO3B[6] iomux select 2'b00: gpio 2'b01: mac_txd3 2'b10: gps_mag 2'b11: reserved
11:10	RW	0x0	gpio3b5_sel GPIO3B[5] iomux select 2'b00: gpio 2'b01: mac_txen 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio3b4_sel GPIO3B[4] iomux select 2'b00: gpio 2'b01: mac_col 2'b10: reserved 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio3b3_sel GPIO3B[3] iomux select 2'b00: gpio 2'b01: mac_crs 2'b10: reserved 2'b11: reserved
5:4	RW	0x0	gpio3b2_sel GPIO3B[2] iomux select 2'b00: gpio 2'b01: mac_txd2 2'b10: reserved 2'b11: reserved
3:2	RW	0x0	gpio3b1_sel GPIO3B[1] iomux select 2'b00: gpio 2'b01: mac_txd1 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio3b0_sel GPIO3B[0] iomux select 2'b00: gpio 2'b01: mac_txd0 2'b10: pwm_0 2'b11: vop_pwm

**GRF\_GPIO3C\_IOMUX**

Address: Operational Base + offset (0x00028)

GPIO3C iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio3c7_sel GPIO3C[7] iomux select 2'b00: gpio 2'b01: edphdmi_cecinout 2'b10: isp_flashtrigin 2'b11: reserved
13:12	RW	0x0	gpio3c6_sel GPIO3C[6] iomux select 2'b00: gpio 2'b01: mac_clk 2'b10: isp_shuttertrig 2'b11: reserved
11:10	RW	0x0	gpio3c5_sel GPIO3C[5] iomux select 2'b00: gpio 2'b01: mac_rxer 2'b10: isp_prelighttrig 2'b11: reserved
9:8	RW	0x0	gpio3c4_sel GPIO3C[4] iomux select 2'b00: gpio 2'b01: mac_rxdv 2'b10: isp_flashtrigout 2'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio3c3_sel GPIO3C[3] iomux select 2'b00: gpio 2'b01: mac_mdc 2'b10: isp_shutteren 2'b11: reserved
5:4	RW	0x0	gpio3c2_sel GPIO3C[2] iomux select 2'b00: gpio 2'b01: mac_rxd3 2'b10: usb_drvvbus1 2'b11: reserved
3:2	RW	0x0	gpio3c1_sel GPIO3C[1] iomux select 2'b00: gpio 2'b01: mac_rxd2 2'b10: uart3gps_rtsn 2'b11: usb_drvvbus0
1:0	RW	0x0	gpio3c0_sel GPIO3C[0] iomux select 2'b00: gpio 2'b01: mac_rxd1 2'b10: uart3gps_ctsn 2'b11: gps_rfclk

**GRF\_GPIO3D\_IOMUX**

Address: Operational Base + offset (0x0002c)

GPIO3D iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio3d7_sel GPIO3D[7] iomux select 2'b00: gpio 2'b01: sc_vcc18v 2'b10: i2c2sensor_sda 2'b11: gpusjtag_tck
13:12	RW	0x0	gpio3d6_sel GPIO3D[6] iomux select 2'b00: gpio 3'b01: ir_tx 3'b10: uart3gps_sout 3'b11: pwm3
11:10	RW	0x0	gpio3d5_sel GPIO3D[5] iomux select 2'b00: gpio 3'b01: ir_rx 3'b10: uart3gsp_sin 3'b11: reserved
9:8	RW	0x0	gpio3d4_sel GPIO3D[4] iomux select 2'b00: gpio 3'b01: mac_txclkout 3'b10: spi1_csn1 3'b11: reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio3d3_sel GPIO3D[3] iomux select 2'b00: gpio 3'b01: hdmi2c_scl 3'b10: i2c5hdmi_scl 3'b11: reserved
5:4	RW	0x0	gpio3d2_sel GPIO3D[2] iomux select 2'b00: gpio 3'b01: hdmi2c_sda 3'b10: i2c5hdmi_sda 3'b11: reserved
3:2	RW	0x0	gpio3d1_sel GPIO3D[1] iomux select 2'b00: gpio 3'b01: mac_rxclkin 3'b10: i2c4tp_scl 3'b11: reserved
1:0	RW	0x0	gpio3d0_sel GPIO3D[0] iomux select 2'b00: gpio 3'b01: mac_mdio 3'b10: i2c4tp_sda 3'b11: reserved

**GRF\_GPIO1A\_P**

Address: Operational Base + offset (0x00100)

GPIO1A PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0xaaaa	<p>gpio1a_p</p> <p>GPIO1A PU/PD programmation section, every GPIO bit corresponding to 2bits</p> <p>2'b00: Z(Noraml operaton);</p> <p>2'b01: weak 1(pull-up);</p> <p>2'b10: weak 0(pull-down);</p> <p>2'b11: Repeater(Bus keeper)</p>

**GRF\_GPIO1B\_P**

Address: Operational Base + offset (0x00104)

GPIO1B PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0xaaaa	gpio1b_p GPIO1B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO1C\_P**

Address: Operational Base + offset (0x00108)

GPIO1C PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5555	gpio1c_p GPIO1C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO1D\_P**

Address: Operational Base + offset (0x0010c)

GPIO1D PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x6995	<p>gpio1d_p</p> <p>GPIO1D PU/PD programmation section, every GPIO bit corresponding to 2bits</p> <p>2'b00: Z(Noraml operaton);</p> <p>2'b01: weak 1(pull-up);</p> <p>2'b10: weak 0(pull-down);</p> <p>2'b11: Repeater(Bus keeper)</p>

**GRF\_GPIO2A\_P**

Address: Operational Base + offset (0x00110)

GPIO2A PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

Bit	Attr	Reset Value	Description
15:0	RW	0x5555	gpio2a_p GPIO2A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO2B\_P**

Address: Operational Base + offset (0x00114)

GPIO2B PU/PD control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaa59	gpio2b_p GPIO2B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO2C\_P**

Address: Operational Base + offset (0x00118)

GPIO2C PU/PD control

Bit	Attr	Reset Value	Description
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x96aa	<p>gpio2c_p</p> <p>GPIO2C PU/PD programmation section, every GPIO bit corresponding to 2bits</p> <p>2'b00: Z(Noraml operaton);</p> <p>2'b01: weak 1(pull-up);</p> <p>2'b10: weak 0(pull-down);</p> <p>2'b11: Repeater(Bus keeper)</p>

**GRF\_GPIO2D\_P**

Address: Operational Base + offset (0x0011c)

GPIO2D PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x5559	gpio2d_p GPIO2D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO3A\_P**

Address: Operational Base + offset (0x00120)

GPIO3A PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5a99	gpio3a_p GPIO3A PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO3B\_P**

Address: Operational Base + offset (0x00124)

GPIO3B PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x99aa	<p>gpio3b_p</p> <p>GPIO3B PU/PD programmation section, every GPIO bit corresponding to 2bits</p> <p>2'b00: Z(Noraml operaton);</p> <p>2'b01: weak 1(pull-up);</p> <p>2'b10: weak 0(pull-down);</p> <p>2'b11: Repeater(Bus keeper)</p>

**GRF\_GPIO3C\_P**

Address: Operational Base + offset (0x00128)

GPIO3C PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x69a5	gpio3c_p GPIO3C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO3D\_P**

Address: Operational Base + offset (0x0012c)

GPIO3D PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x5655	gpio3d_p GPIO3D PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**GRF\_GPIO1A\_E**

Address: Operational Base + offset (0x00200)

GPIO1A drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0000	<p>gpio1a_e</p> <p>GPIO1D drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO1B\_E**

Address: Operational Base + offset (0x00204)

GPIO1B drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x0800	<p>gpio1b_e</p> <p>GPIO1B drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO1C\_E**

Address: Operational Base + offset (0x00208)

GPIO1C drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0xa0aa	<p>gpio1c_e</p> <p>GPIO1C drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO1D\_E**

Address: Operational Base + offset (0x0020c)

GPIO1D drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:14	RW	0x0	<p>gpio1d7_e</p> <p>GPIO1D_7 drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>
13:12	RW	0x0	<p>gpio1d6_e</p> <p>GPIO1D_6 drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>
11:10	RW	0x0	<p>gpio1d5_e</p> <p>GPIO1D_5 drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>
9:8	RW	0x0	<p>gpio1d4_e</p> <p>GPIO1D_4 drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio1d3_e GPIO1D_3 drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
5:4	RW	0x0	gpio1d2_e GPIO1D_2 drive strength control, every GPIO bit corresponding to 2bits 2'b00: 12mA 2'b01: 8mA 2'b10: 4mA 2'b11: 2mA
3:2	RW	0x0	gpio1d1_e GPIO1D_1 drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA
1:0	RW	0x2	gpio1d0_e GPIO1D_0 drive strength control, every GPIO bit corresponding to 2bits 2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA

**GRF\_GPIO2A\_E**

Address: Operational Base + offset (0x00210)

GPIO2A drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x5655	<p>gpio2a_e</p> <p>GPIO2A drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO2B\_E**

Address: Operational Base + offset (0x00214)

GPIO2B drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x0119	<p>gpio2b_e</p> <p>GPIO2B drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO2C\_E**

Address: Operational Base + offset (0x00218)

GPIO2C drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0000	<p>gpio2c_e</p> <p>GPIO2C drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO2D\_E**

Address: Operational Base + offset (0x0021c)

GPIO2D drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x5500	<p>gpio2d_e</p> <p>GPIO2D drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO3A\_E**

Address: Operational Base + offset (0x00220)

GPIO3A drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x0009	<p>gpio3a_e</p> <p>GPIO3A drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA</p>

**GRF\_GPIO3B\_E**

Address: Operational Base + offset (0x00224)

GPIO3B drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x682a	<p>gpio3b_e</p> <p>GPIO3B drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA</p>

**GRF\_GPIO3C\_E**

Address: Operational Base + offset (0x00228)

GPIO3C drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x3115	<p>gpio3c_e</p> <p>GPIO3C drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO3D\_E**

Address: Operational Base + offset (0x0022c)

GPIO3D drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x0304	<p>gpio3d_e</p> <p>GPIO3D drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**GRF\_GPIO1L\_SR**

Address: Operational Base + offset (0x00300)

GPIO1A/B SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:8	RW	0x08	<p>gpio1b_sr</p> <p>GPIO1B slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>
7:0	RW	0x00	<p>gpio1a_sr</p> <p>GPIO1A slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>

**GRF\_GPIO1H\_SR**

Address: Operational Base + offset (0x00304)

GPIO1C/D SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:8	RW	0x00	<p>gpio1d_sr</p> <p>GPIO1D slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>
7:0	RW	0x00	<p>gpio1c_sr</p> <p>GPIO1C slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>

**GRF\_GPIO2L\_SR**

Address: Operational Base + offset (0x00308)

GPIO2A/B SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:8	RW	0x02	gpio2b_sr GPIO2B slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio2a_sr GPIO2A slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

**GRF\_GPIO2H\_SR**

Address: Operational Base + offset (0x0030c)

GPIO2C/D SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RW	0x00	gpio2d_sr GPIO2D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x00	gpio2c_sr GPIO2C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

**GRF\_GPIO3L\_SR**

Address: Operational Base + offset (0x00310)

GPIO3A/B SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:8	RW	0x47	<p>gpio3b_sr</p> <p>GPIO3B slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>
7:0	RW	0x02	<p>gpio3a_sr</p> <p>GPIO3A slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>

**GRF\_GPIO3H\_SR**

Address: Operational Base + offset (0x00314)

GPIO3C/D SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:8	RW	0x00	gpio3d_sr GPIO3D slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast
7:0	RW	0x40	gpio3c_sr GPIO3C slew rate control for each bit 1'b0: slow (half frequency) 1'b1: fast

**GRF\_GPIO\_SMT**

Address: Operational Base + offset (0x00380)

GPIO smitter control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x1	gpio0b_smt_ctrl GPIO0B1 Schmitt trigger control. 0: No hysteresis 1: Schmitt trigger enabled.
8	RW	0x1	gpio3d7_smt_ctrl GPIO3D7 Schmitt trigger control. 0: No hysteresis 1: Schmitt trigger enabled.
7:4	RW	0x1	gpio3d_smt_ctrl GPIO3D[3:0] Schmitt trigger control. 0: No hysteresis 1: Schmitt trigger enabled.

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3:2	RW	0x1	gpio2c_smt_ctrl GPIO2C[6:5] Schmitt trigger control. 0: No hysteresis 1: Schmitt trigger enabled.
1:0	RW	0x1	gpio1c_smt_ctrl GPIO1C[1:0] Schmitt trigger control. 0: No hysteresis 1: Schmitt trigger enabled.

**GRF\_SOC\_CON0**

Address: Operational Base + offset (0x00400)

SoC control register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RO	0x0	reserved
13:9	RW	0x00	cci_qosoverride CCI400 QOSOVERRIDE input control. If HIGH, internally generated values override the ARQOS and AWQOS inputs. One bit exists for each slave interface.
8:6	RW	0x0	cci_bufferableoverride CCI400 BUFFERABLE OVERRIDE input control. If HIGH, then all transactions from a master interface are made non-bufferable by modifying AWCACHE[0] and ARCACHE[0]. One bit exists for each master interface.

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
5:3	RW	0x7	cc_i_barrierterminate CCI BARRIERTERMINAGE input control. If HIGH, then barriers are terminated in the master interface and not propagated downstream. Set this HIGH if the downstream slave does not support barriers. One bit exists for each master interface.
2:0	RW	0x0	cc_i_broadcastcachemaint CCI400 BROADCASTCACHEMINT input control. If HIGH, then cache maintenance operations are sent downstream. Only set if there is a downstream cache with an ACE-Lite interface. One bit exists for each master interface.

**GRF\_SOC\_CON1**

Address: Operational Base + offset (0x00404)

SoC control register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x0	reserved
8:4	RW	0x1c	cc_i_acchannelen CCI400 ACCHANELEN input control. Slave interface supports DVM messages. This is overridden to 0x0 if you set the Control Override Register[1].

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3:0	RW	0x0	cc1_ecorevnum CC1400 ECOREVNUM input control. Used to ease the update of the revision field register in case of an ECO.

**GRF\_SOC\_CON2**

Address: Operational Base + offset (0x00408)

SoC control register 2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11	RW	0x0	gpu_timer_en SoC timer input enable for GPU. 0: tie TSVVALUE of GPU to low. 1: use system timer for TSVVALUE of GPU.
10	RW	0x1	gpu_resetn_jtag gpu jtag port resetn control
9	RW	0x1	gpu_jtag_sys_power_ctrl gpu system jtag power control
8	RW	0x1	gpu_aclk_mem_en gpu aclk master clock enable
7	RW	0x1	gpu_aclk_cfg_en gpu axi slave clock enable
6	RW	0x1	gpu_clk_core_en gpu core clock enable
5	RW	0x1	gpu_dxt_bc_enable gpu dxt_bc_enable port control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
4	RW	0x1	gpu_dusts_enable gpu dusts_enable port control
3:2	RW	0x0	gpu_mem_aw_qos GPU AXI master write channel QoS control.
1:0	RW	0x0	gpu_mem_ar_qos GPU AXI master read channel QoS control.

**GRF\_SOC\_CON3**

Address: Operational Base + offset (0x0040c)

SoC control register 3

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	saradc_tsen_pd_1 GPU TSADC temperature sensor output buffer power down 0: enable buffer 1: power down
14	RW	0x0	saradc_tsen_buf_pd_1 GPU TSADC temperature sensor output buffer power down 0: enable buffer 1: power down
13:8	RW	0x20	saradc_tsen_cal_1 GPU TSADC calibration control for temperature sensor output, increase register value to shift down temperature sensor output.

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7	RW	0x0	saradc_tsen_pd_0 Core TSADC temperature sensor power down 0: enable sensor 1: power down
6	RW	0x0	saradc_tsen_buf_pd_0 Core TSADC temperature sensor output buffer power down 0: enable buffer 1: power down
5:0	RW	0x20	saradc_tsen_cal_0 Core TSADC calibration control for temperature sensor output, increase register value to shift down temperature sensor output.

**GRF\_SOC\_CON4**

Address: Operational Base + offset (0x00410)

SoC control register 4

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
14:13	RW	0x1	drtype_dmac_peri peri dma drtype bit control, indicates the type of acknowledgement, or request, that the peripheral signals: b00 = single level request b01 = burst level request b10 = acknowledging a flush request that the DMAC requested b11 = reserved.
12	RW	0x0	edp_dc_tp_i eDP PHY analog DC test point input
11:3	RW	0x000	edp_frq_vid_ck_in eDP PHY frequency information of vid_ck_in frq_vid_ck_in<8:0>/8 = freq(vid_ck_in)/10
2	RW	0x0	edp_vid_lock eDP PHY input video PLL stable indicator 1'b1: stable 1'b0: unstable
1	RW	0x0	edp_iddq_en eDP PHY IDDDQ enable 1'b0: disable 1'b1: enable, all circuits are power down, all IO are high-z
0	RW	0x1	edp_ref_clk_sel eDP PHY reference clock source selection 1'b0: from PAD(IO_EDP_OSC_CLK_24M) 1'b1: from internal 24MHz or 27MHz clock

**GRF\_SOC\_CON5**

Address: Operational Base + offset (0x00414)

SoC control register 5

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7	RW	0x0	edp_mem_ctrl_sel eDP memory control selection 1'b1: controlled by eDP controller internal logic 1'b0: controlled by APB BUS
6	RW	0x0	edp_bist_en eDP memory control selection 1'b1: controlled by eDP controller internal logic 1'b0: controlled by APB BUS
5	RW	0x0	edp_hdcp_protect eDP HDCP function protection 1'b1: protect 1'b0: not protect
4	RW	0x0	edp_tx_bscan_en DP TX boundary enable 1'b0: disable 1'b1: enable

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3:0	RW	0x0	dp_tx_bscan_data eDP TX boundary data bit0: boundary data to ch0 bit1: boundary data to ch1 bit2: boundary data to ch2 bit3: boundary data to ch3

**GRF\_SOC\_CON6**

Address: Operational Base + offset (0x00418)

SoC control register 6

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x0	hevc_vcodec_sel hevc_vcodec_sel bit select 0: vcodec 1: hevc
11:8	RW	0x0	dphy_rx_forcerxmode MIPI DPHY RX force lane into receive mode/wait for stop stat. Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.
7	RW	0x0	dsi0_dpiupdatecfg DSI host0 dpiupdatecfg bit control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
6	RW	0x0	dphy_rx_clk_inv_sel dphy_rx clock invertor select 1'b0: with invertor 1'b1: without invertor
5	RW	0x0	clk0_lvds_inv_sel Inversion of VOP dclk for LVDS selection 1'b1: invert 1'b0: not invert
4	RW	0x0	dclk_lvds_div2_sel 2 divide frequency of VOP dclk for LVDS selection 1'b1: 2 divide frequency 1'b0: no divide frequency
3	RW	0x0	dsi_dpicolorm DSI dpicolorm bit control
2	RW	0x0	dsi0_dpishutd DSI host dpishutdn bit control
1	RW	0x0	isp_mipi_csi_host_sel ISP or MIPI_CSI host select 1'b0: mipi csi host 1'b1: ISP
0	RW	0x0	disable_isp ISP disable bit control

**GRF\_SOC\_CON7**

Address: Operational Base + offset (0x0041c)

SoC control register 7

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15	RW	0x0	<p>mipi_phy_ttl_mode</p> <p>mipi_phy_ttl_mode bit control</p> <p>0: dsi/lvds mode</p> <p>1: ttl mode</p>
14:13	RW	0x0	<p>lvds_select</p> <p>lvds_select control bit</p>
12	RW	0x0	<p>lvds_mode</p> <p>lvds_mode bit control</p>
11	RW	0x0	<p>lvds_msbsel</p> <p>LVDS controller msbsel signal control</p>
10:7	RW	0x0	<p>forcetxstopmode</p> <p>MIPI DPHY TX force lane into transmit mode and generate stop state.</p> <p>Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.</p>
6	RW	0x0	<p>dphy_tx0_forcerxmode</p> <p>MIPI DPHY TX force lane into receive mode/wait for stop stat.</p> <p>Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.</p>
5	RW	0x0	<p>lane0_turndisable</p> <p>MIPI DPHY TX0 disable turn around control</p> <p>Every bit for one lane, bit3 is for lane3, bit2 is for lane2, bit1 is for lane1, bit0 is for lane0.</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
4:1	RO	0x0	reserved
0	RW	0x0	vcodec_sel vdpu vepu clock select 1'b0: select vepu aclk as vcodec main clock 1'b1: select vdpu aclk as vcodec main clock

**GRF\_SOC\_CON8**

Address: Operational Base + offset (0x00420)

SoC control register 8

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x7538	mcu_stcalib_0 mcu_stcalib[15:0] bit control

**GRF\_SOC\_CON9**

Address: Operational Base + offset (0x00424)

SoC control register 9

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:10	RO	0x0	reserved
9:0	RW	0x100	mcu_stcalib_1 mcu_stcalib[25:16] bit control

**GRF\_SOC\_CON10**

Address: Operational Base + offset (0x00428)  
 SoC control register 10

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0000	mcu_code_addr_start MCU Code address start bit27 ~ bit12

**GRF\_SOC\_CON11**

Address: Operational Base + offset (0x0042c)  
 SoC control register 11

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x2000	mcu_sram_addr_start MCU SRAM address start bit27 ~ bit12

### **GRF\_SOC\_CON12**

Address: Operational Base + offset (0x00430)  
 SoC control register 12

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x6000	mcu_exsram_addr_start MCU external sram start address bit27 ~ bit12

**GRF\_SOC\_CON13**

Address: Operational Base + offset (0x00434)  
 SoC control register 13

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0000	<p>mcu_experi_addr_start</p> <p>MCU external periphral start address bit27 ~ bit12</p>

**GRF\_SOC\_CON14**

Address: Operational Base + offset (0x00438)  
 SoC control register 14

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:12	RW	0x0	experi_addr_start experi_addr_start bit31~bit28
11:8	RW	0x0	exsram_addr_start exsram_addr_start bit31~bit28
7:4	RW	0x0	sram_addr_start sram_addr_start bit31~bit28
3:0	RW	0x0	code_addr_start code_addr_start bit31~bit28

**GRF\_SOC\_CON15**

Address: Operational Base + offset (0x0043c)

SoC control register 15

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RO	0x0	reserved
14	RW	0x0	flash_poc_ctrl flash IO domain poc control selection 0: controled by gpio_0b5 pad 1: controled by bit 2 of IO_VSEL
13	RW	0x1	force_jtag Force select jtag function from sdmmc0 IO
12	RW	0x0	pwm_sel PWM solution selection 1'b1: RK design PWM 1'b0: DW PWM

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:9	RW	0x0	gmac_phy_intf_sel PHY interface select 3'b001: RGMII 3'b100: RMII All others: Reserved
8	RW	0x0	gmac_flowctrl GMAC transmit flow control When set high, instructs the GMAC to transmit PAUSE Control frames in Full-duplex mode. In Half-duplex mode, the GMAC enables the Back-pressure function until this signal is made low again
7	RW	0x0	gmac_speed MAC speed 1'b1: 100-Mbps 1'b0: 10-Mbps
6	RW	0x0	rmii_mode RMII mode selection 1'b1: RMII mode
5:4	RW	0x0	gmac_clk_sel RGMII clock selection 2'b00: 125MHz 2'b11: 25MHz 2'b10: 2.5MHz
3	RW	0x0	rmii_clk_sel RMII clock selection 1'b1: 25MHz 1'b0: 2.5MHz
2	RW	0x0	pause_mmc_peri PERI MMC AHB bus arbiter pause control
1	RW	0x0	pause_emem_peri PERI EMEM AHB bus arbiter pause control
0	RW	0x0	pause_usb_peri PERI USB AHB bus arbiter pause control

**GRF\_SOC\_CON16**

Address: Operational Base + offset (0x00440)  
 SoC control register 16

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	rxclk_dly_ena_gmac RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
14:8	RW	0x00	clk_rx_dl_cfg_gmac RGMII RX clock delayline value
7	RW	0x0	txclk_dly_ena_gmac RGMII TX clock delayline enable 1'b1: enable 1'b0: disable
6:0	RW	0x00	clk_tx_dl_cfg_gmac RGMII TX clock delayline value

### **GRF\_SOC\_CON17**

Address: Operational Base + offset (0x00444)  
 SoC control register 17

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:10	RO	0x0	reserved
9:5	RW	0x00	<p>uart_rts_sel</p> <p>uart_rts_sel bit control</p>
4	RW	0x0	<p>uart4_cts_sel</p> <p>UART polarity selection for cts port</p> <p>Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT.</p> <p>1'b1: high asserted</p> <p>1'b0: low asserted</p>
3	RW	0x0	<p>uart3_cts_sel</p> <p>UART polarity selection for cts port</p> <p>Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT.</p> <p>1'b1: high asserted</p> <p>1'b0: low asserted</p>
2	RW	0x0	<p>hsadc_clk_sel</p> <p>hsadc_clk source select</p> <p>1'b0: with clock inveror</p> <p>1'b1: without clock inveror</p>
1	RW	0x0	<p>uart1_cts_sel</p> <p>UART polarity selection for cts port</p> <p>Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT.</p> <p>1'b1: high asserted</p> <p>1'b0: low asserted</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
0	RW	0x0	uart0_cts_sel UART polarity selection for cts port Every bit for one UART, bit4 is for UART_EXP, bit3 is for UART_GPS, bit2 is for UART_DBG, bit1 is for UART_BB, bit0 is for UART_BT. 1'b1: high asserted 1'b0: low asserted

**GRF\_SOC\_STATUS0**

Address: Operational Base + offset (0x00480)

SoC status register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RO	0x0	reserved
15	RW	0x0	ddrphy_lock
14	RW	0x0	sdmmc_idle sdmmc_idle status
13	RW	0x0	gpu_idle gpu idle status
12	RO	0x0	gmac_portselect gmac_portselect status
11	RO	0x0	newpll_clk NEW PLL clock status
10	RO	0x0	generalpll_clk GENERAL PLL clock output
9	RO	0x0	codecpll_clk CODEC PLL clock output
8	RO	0x0	ddrpll_clk DDR PLL clock output
7	RO	0x0	arm_b_pll_clk ARM_B PLL clock output
6	RO	0x0	arm_l_pll_clk ARM_L PLL clock output
5	RO	0x0	newpll_lock NEW PLL lock
4	RO	0x0	general_pll_lock General PLL lock
3	RO	0x0	codecpll_lock CODEC PLL lock status
2	RO	0x0	ddrpll_lock DDR PLL lock status

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
1	RO	0x0	arm_b_pll_lock ARM_B PLL lock status
0	RO	0x0	arm_l_pll_lock ARM_L PLL lock status

**GRF\_SOC\_STATUS1**

Address: Operational Base + offset (0x00484)

SoC status register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	nif0_fifo0 DDR channel0 NIF interface FIFO0 status

**GRF\_SOC\_STATUS2**

Address: Operational Base + offset (0x00488)

SoC status register 2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	nif0_fifo1 DDR channel0 NIF interface FIFO1 status

**GRF\_SOC\_STATUS3**

Address: Operational Base + offset (0x0048c)

SoC status register 3

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	nif0_fifo2 DDR channel0 NIF interface FIFO2 status

**GRF\_SOC\_STATUS4**

Address: Operational Base + offset (0x00490)

SoC status register 4

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	nif0_fifo3 DDR channel0 NIF interface FIFO3 status

**GRF\_SOC\_STATUS5**

Address: Operational Base + offset (0x00494)

SoC status register 5

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi0_eff_wr_num DDR channel 0 DFI interface write command number

**GRF\_SOC\_STATUS6**

Address: Operational Base + offset (0x00498)

SoC status register 6

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi0_eff_rd_num DDR channel 0 DFI interface read command number

**GRF\_SOC\_STATUS7**

Address: Operational Base + offset (0x0049c)

SoC status register 7

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi0_eff_act_num DDR channel 0 DFI interface active command number

**GRF\_SOC\_STATUS8**

Address: Operational Base + offset (0x004a0)

SoC status register 8

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi0_timer_val DDR channel 0 DFI interface timer value

**GRF\_SOC\_STATUS9**

Address: Operational Base + offset (0x004a4)

SoC status register 9

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi1_eff_wr_num DDR channel 1 DFI interface write command number

**GRF\_SOC\_STATUS10**

Address: Operational Base + offset (0x004a8)

SoC status register 10

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi1_eff_rd_num DDR channel 1 DFI interface read command number

**GRF\_SOC\_STATUS11**

Address: Operational Base + offset (0x004ac)

SoC status register 11

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi1_eff_act_num DDR channel 1 DFI interface active command number

**GRF\_SOC\_STATUS12**

Address: Operational Base + offset (0x004b0)

SoC status register 12

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	dfi1_timer_val DDR channel 1 DFI interface timer value

**GRF\_SOC\_STATUS13**

Address: Operational Base + offset (0x004b4)

SoC status register 13

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:25	RO	0x0	reserved
24	RO	0x0	dphy_rx_rxclkactivehs dphy_rx_rxclkactivehs bit status
23	RO	0x0	dphy_rx_direction dphy_rx_direction bit status
22	RO	0x0	dphy_rx_ulpsactivenot_0 dphy_rx_ulpsactivenot_0 bit status
21	RO	0x0	dphy_rx_ulpsactivenot_1 dphy_rx_ulpsactivenot_1 bit status
20	RO	0x0	dphy_rx_ulpsactivenot_2 dphy_rx_ulpsactivenot_2 bit status
19	RO	0x0	dphy_rx_ulpsactivenot_3 dphy_rx_ulpsactivenot3 bit status
18:16	RO	0x0	ddrupctl0_stat ddrupctl0 stat status bit
15:0	RO	0x0000	ddrupctl0_bbflags ddrupctl0 bbflags status bit

**GRF\_SOC\_STATUS14**

Address: Operational Base + offset (0x004b8)

SoC status register 14

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31	RW	0x0	dp_detected_usbphy usb phy dp_detected_usbphy status bit status
30	RW	0x0	cp_detected_usbphy usb phy cp_detected_usbphy status bit status

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
29	RW	0x0	dcp_detected_usbphy usb phy dcp_detected_usbphy status bit status
28:23	RO	0x00	ehci_usbsts_host0 usb host 0 ehci_usbsts_host0 bit status
22:12	RO	0x000	ehci_xfer_cnt_host0 usb host 0 ehci_xfer_cnt_host0 bit status
11:8	RO	0x0	ehci_lpsmc_state_host0 usb host 0 ehci_lpsmc_state_host0 bit status
7	RO	0x0	ehci_xfer_prdc_host0 usb host 0 ehci_xfer_prdc_host0 bit status
6	RO	0x0	ehci_bufacc_host0 usb host 0 ehci_bufacc_host0 bit status
5	RO	0x0	ohci_globalsuspend_host0 usb host 0 ohci_globalsuspend_host0 bit status
4	RO	0x0	ohci_drwe_host0 usb host 0 ohci_drwe_host0 bit status
3	RO	0x0	ohci_rwe_host0 usb host 0 ohci_rwe_host0 bit status
2	RO	0x0	ohci_ccs_host0 usb host 0 ohci_ccs_host0 bit status
1	RO	0x0	ohci_bufacc_host0 usb host 0 ohci_bufacc bit status
0	RO	0x0	ohci_rmtwkp_host0 usb host 0 ohci_rmtwkp_host0 bit status

**GRF\_SOC\_STATUS15**

Address: Operational Base + offset (0x004bc)

SoC status register 15

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:27	RO	0x0	reserved
26	RO	0x0	otg0_utmiotg_iddig usb otg utmiotg_iddig bit status
25:24	RO	0x0	otg0_utmi_linestate usb otg utmi_linestate bit status
23	RO	0x0	otg0_utmisrp_bvalid usb otg utmisrp_bvalid bit status
22	RO	0x0	otg0_utmiotg_vbusvalid usb otg utmiotg_vbusvalid bit status
21:16	RO	0x00	grf_stat_ehci_usbsts hsic ehci_usbsts bit status bit status

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:5	RO	0x000	grf_stat_ehci_xfer_cnt hsic ehci_xfer_cnt bit status
4	RO	0x0	grf_stat_ehci_xfer_prdc hsic ehci_xfer_prdc bit status
3:0	RO	0x0	grf_stat_ehci_lpsmc_state hsic ehci_lpsmc_state bit status

**GRF\_CPU\_CON0**

Address: Operational Base + offset (0x00500)

CPU little cluster control register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	cfgte pd_core_l ca53 cpu cfgte bit control
11:8	RW	0x0	cfgend Field0008 Abstract pd_core_l ca53 cpu cfgend bit control
7	RW	0x0	I2rstdisable Field0007 Abstract pd_core_l ca53 I2rstdisable
6	RW	0x0	dbgI1rstdisable Field0006 Abstract pd_core_l ca53 cpu dbgI1rstdisable
5	RO	0x0	reserved
4	RW	0x0	clrexmonreq_pd_core_l pd_core_l ca53 cpu clrexmonreq_pd_core_l bit control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3	RW	0x1	sysbardisable pd_core_l ca53 cpu sysbardisable bit control 0: disable 1: enable
2	RW	0x0	broadcastcachemaint Field0002 Abstract pd_core_l ca53 cpu broadcastcachemaint bit control 0: disable 1: enable
1	RW	0x1	broadcastouter pd_core_l ca53 cpu broadcastouter bit control 0: disable 1: enable
0	RW	0x1	broadcastinner pd_core_l ca53 cpu broadcastinner bit control 1: enable 0: disable

**GRF\_CPU\_CON1**

Address: Operational Base + offset (0x00504)

CPU little cluster control register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x0	clusteridaff1 pd_core_l ca53 cpu clusteridaff1 bit control
7:4	RW	0x0	pd_core_arqos pd_core_l pd_core_arqos bit control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
3:0	RW	0x0	pd_core_awqos pd_core_l pd_core_awqos bit control

**GRF\_CPU\_CON2**

Address: Operational Base + offset (0x00508)

CPU big cluster control register 2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RW	0x0	cfgte pd_core_b ca53 cpu cfgte bit control
11:8	RW	0x0	cfgend Field0008 Abstract pd_core_b ca53 cpu cfgend bit control
7	RW	0x0	l2rstdisable pd_core_b ca53 cpu l2rstdisable bit control
6	RW	0x0	dbg1rst disable Field0006 Abstract pd_core_b ca53 cpu dbg1rst disable bit control
5	RO	0x0	reserved
4	RW	0x0	clrexmonreq_pd_core_b pd_core_b clrexmonreq_pd_core_b bit control
3	RW	0x1	sysbardisable Field0003 Abstract pd_core_b ca53 cpu sysbardisable bit control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
2	RW	0x0	broadcastcachemaint pd_core_b ca53 cpu broadcastcachemaint bit control
1	RW	0x1	broadcastouter Field0001 Abstract pd_core_b ca53 cpu broadcastouter bit control
0	RW	0x1	broadcastinner pd_core_b ca53 cpu broadcastinner bit control

**GRF\_CPU\_CON3**

Address: Operational Base + offset (0x0050c)

CPU big cluster control register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9:8	RW	0x0	clusteridaff1 Field0000 Abstract clusteridaff1 bit control
7:4	RW	0x0	pd_core_arqos pd_core_b_arqos bit control
3:0	RW	0x0	pd_core_awqos pd_core_b_awqos bit control

**GRF\_CPU\_STATUS0**

Address: Operational Base + offset (0x00520)

CPU status register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:28	RO	0x0	reserved
27:24	RO	0x0	ncorereset_pd_core_b ncorereset_pd_core_b status
23:20	RO	0x0	ncorereset_pd_core_l ncorereset_pd_core_l status
19	RO	0x0	mcu_sleeping mcu_sleeping status
18	RO	0x0	mcu_sleepdeep mcu_sleepdeep status
17	RO	0x0	mcu_core_halted mcu_core_halted status
16	RO	0x0	mcu_core_lockup mcu_core_lockup status
15:13	RO	0x0	reserved
12	RO	0x0	clrexnonack_pd_core_b clrexnonack_pd_core_b status
11:8	RO	0x0	smpen_pd_core_b smpen_pd_core_b status
7:5	RO	0x0	reserved
4	RO	0x0	clrextmonack_pd_core_l clrextmonack_pd_core_l status
3:0	RO	0x0	smpen_pd_core_l smpen_pd_core_l status

**GRF\_CPU\_STATUS1**

Address: Operational Base + offset (0x00524)

CPU status register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:24	RO	0x00	wrmemattr_pd_core_b wrmemattr of pd_core_b status
23:16	RO	0x00	rdmemattr_pd_core_b rdmemattr of pd_core_b status
15:8	RO	0x00	wrmemattr_pd_core_l wrmemattr of pd_core_l status
7:0	RO	0x00	rdmemattr_pd_core_l rdmemattr of pd_core_l status

**GRF\_CCI\_STATUS0**

Address: Operational Base + offset (0x00540)

CCI status register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:19	RO	0x0	reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
18	RO	0x0	cci400_activem0 Indicates that the master interface has active transactions. You can use it to gate the clock to downstream components.
17	RO	0x0	cci400_activem1 Indicates that the master interface has active transactions. You can use it to gate the clock to downstream components.
16	RO	0x0	cci400_activem2 Indicates that the master interface has active transactions. You can use it to gate the clock to downstream components.
15:12	RO	0x0	evntawqos4 Value of the QoS value regulator of slave interface 4 last applied to AWQOS.
11:8	RO	0x0	evntarqos4 Value of the QoS value regulator of slave interface 4 last applied to ARQOS.
7:4	RO	0x0	evntawqos3 Value of the QoS value regulator of slave interface 3 last applied to AWQOS.
3:0	RO	0x0	evntarqos3 Value of the QoS value regulator of slave interface 3 last applied to ARQOS.

**GRF\_CCI\_STATUS1**

Address: Operational Base + offset (0x00544)

CCI status register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	evntbus Bits 31~0 of CCI400 EVNTBUS output. CCI-400 events, exported if enabled in the PMCR.

**GRF\_CCI\_STATUS2**

Address: Operational Base + offset (0x00548)

CCI status register 2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	evntbus Bits 63~32 of CCI400 EVNTBUS output. CCI-400 events, exported if enabled in the PMCR.

**GRF\_CCI\_STATUS3**

Address: Operational Base + offset (0x0054c)

CCI status register 3

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	evntbus Bits 95~64 of CCI400 EVNTBUS output. CCI-400 events, exported if enabled in the PMCR.

**GRF\_CCI\_STATUS4**

Address: Operational Base + offset (0x00550)

CCI status register 4

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RO	0x00000000	evntbus Bits 127~96 of CCI400 EVNTBUS output. CCI-400 events, exported if enabled in the PMCR.

**GRF\_CCI\_STATUS5**

Address: Operational Base + offset (0x00554)

CCI status register 5

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31	RO	0x0	reserved
30:0	RO	0x00000000	evntbus Bits 158~128 of CCI400 EVNTBUS output. CCI-400 events, exported if enabled in the PMCR.

**GRF\_CCI\_STATUS6**

Address: Operational Base + offset (0x00558)

CCI status register 6

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:24	RO	0x00	arcnt_m0 The counter value of CCI 400 master 0 port AR channel.

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
23:16	RO	0x00	rcount_m0 The counter value of CCI 400 master 0 port R channel.
15:8	RO	0x00	awcount_m0 The counter value of CCI 400 master 0 interface AW channel.
7:0	RO	0x00	bcount_m0 The counter value of CCI 400 master 0 interface B channel.

**GRF\_CCI\_STATUS7**

Address: Operational Base + offset (0x0055c)

CCI status register 7

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:8	RO	0x0	reserved
7:4	RO	0x0	arcnt_m0 The difference between AR channel and R channel of CCI 400 master 0 interface.
3:0	RO	0x0	awdiff_m0 The difference between AW channel and B channel of CCI 400 master 0 interface.

**GRF\_CCI\_STATUS8**

Address: Operational Base + offset (0x00560)

CCI status register 8

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:24	RO	0x00	arcnt_m2 The counter value of CCI 400 master 2 port AR channel.
23:16	RO	0x00	rcount_m2 The counter value of CCI 400 master 2 port R channel.
15:8	RO	0x00	awcount_m2 The counter value of CCI 400 master 2 interface AW channel.
7:0	RO	0x00	bcount_m2 The counter value of CCI 400 master 2 interface B channel.

**GRF\_CCI\_STATUS9**

Address: Operational Base + offset (0x00564)

CCI status register 9

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:8	RO	0x0	reserved
7:4	RO	0x0	arcnt_m2 The difference between AR channel and R channel of CCI 400 master 2 interface.
3:0	RO	0x0	awdiff_m2 The difference between AW channel and B channel of CCI 400 master 2 interface.

**GRF\_CCI\_STATUS10**

Address: Operational Base + offset (0x00568)

CCI status register 10

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:24	RO	0x00	arcnt_s2 The counter value of CCI 400 slave 2 port AR channel.
23:16	RO	0x00	rcnt_s2 The counter value of CCI 400 slave 2 port R channel.
15:8	RO	0x00	awcnt_s2 The counter value of CCI 400 slave 2 interface AW channel.
7:0	RO	0x00	bcount_s2 The counter value of CCI 400 slave 2 interface B channel.

**GRF\_CCI\_STATUS11**

Address: Operational Base + offset (0x0056c)

CCI status register 11

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:8	RO	0x0	reserved
7:4	RO	0x0	arcnt_s2 The difference between AR channel and R channel of CCI 400 slave 2 interface.
3:0	RO	0x0	awdiff_s2 The difference between AW channel and B channel of CCI 400 slave 2 interface.

**GRF\_CCI\_STATUS12**

Address: Operational Base + offset (0x00570)

CCI status register 12

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:24	RO	0x00	arcount_s3 The counter value of CCI 400 slave 3 port AR channel.
23:16	RO	0x00	rcount_s3 The counter value of CCI 400 slave 3 port R channel.
15:8	RO	0x00	awcount_s3 The counter value of CCI 400 slave 3 interface AW channel.
7:0	RO	0x00	bcount_s3 The counter value of CCI 400 slave 3 interface B channel.

**GRF\_CCI\_STATUS13**

Address: Operational Base + offset (0x00574)

CCI status register 13

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:28	RO	0x0	reserved
27:20	RO	0x00	account_s3 The counter value of CCI 400 slave 3 interface AC channel.
19:12	RO	0x00	crcount_s3 The counter value of CCI 400 slave 3 interface CR channel.
11:8	RO	0x0	arcount_s3 The difference between AR channel and R channel of CCI 400 slave 3 interface.
7:4	RO	0x0	awdiff_s3 The difference between AW channel and B channel of CCI 400 slave 3 interface.
3:0	RO	0x0	acdiff_s3 The difference between AC channel and CR channel of CCI 400 slave 3 interface.

**GRF\_CCI\_STATUS14**

Address: Operational Base + offset (0x00578)

CCI status register 14

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:24	RO	0x00	arcount_s4 The counter value of CCI 400 slave 4 port AR channel.

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
23:16	RO	0x00	rcount_s4 The counter value of CCI 400 slave 4 port R channel.
15:8	RO	0x00	awcount_s4 The counter value of CCI 400 slave 4 interface AW channel.
7:0	RO	0x00	bcount_s4 The counter value of CCI 400 slave 4 interface B channel.

**GRF\_CCI\_STATUS15**

Address: Operational Base + offset (0x0057c)

CCI status register 15

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:28	RO	0x0	reserved
27:20	RO	0x00	account_s4 The counter value of CCI 400 slave 4 interface AC channel.
19:12	RO	0x00	crcount_s4 The counter value of CCI 400 slave 4 interface CR channel.
11:8	RO	0x0	arcount_s4 The difference between AR channel and R channel of CCI 400 slave 4 interface.
7:4	RO	0x0	awdiff_s4 The difference between AW channel and B channel of CCI 400 slave 4 interface.
3:0	RO	0x0	acdiff_s4 The difference between AC channel and CR channel of CCI 400 slave 4 interface.

**GRF\_DDRC0\_CON0**

Address: Operational Base + offset (0x00600)

DDRC0 control register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11	RW	0x0	upctl_lp_reset_mode upctl_lp_reset_mode bit control
10	RO	0x0	reserved
9	RW	0x0	noc_rsp_err_stall noc_rsp_err_stall bit control 0: stall response 1: error response
8	RW	0x0	upctl_anfifo upctl_anfifo bit control
7	RW	0x0	upctl_aburstint upctl_aburstint bit control
6	RW	0x0	dfi_eff_stat_en1 dfi_eff_stat_en1 bit control
5	RW	0x0	dfi_eff_stat_en0 dfi_eff_stat_en0 bit control
4	RW	0x0	mobile_ddr_sel mobile_ddr_sel bit control
3	RW	0x0	ddr0_16bit_en ddr0_16bit_en bit control
2	RW	0x0	mash_mainddr3 mash_mainddr3 bit control
1	RW	0x0	msch0_mainpartialpop msch0_mainpartialpop bit control
0	RW	0x0	upctl_c_active_in upctl_c_active_in bit control

**GRF\_SIG\_DETECT\_CON**

Address: Operational Base + offset (0x00680)

external signal detect configue register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	sd_detect_filter_time_sel Field0000 Abstract sd_detect_filter time sel 00: 5ms 01: 15ms 10: 35ms 11: 50ms
13:12	RW	0x0	host_ls_filter_time_sel Field0000 Abstract host_ls_filter time select 00: 100us 01: 500us 10: 1ms 11:10ms
11:10	RW	0x0	otg_ls_filter_time_sel otg_ls_filter time select 00: 100us 01: 500us 10: 1ms 11:10ms

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
9:8	RW	0x0	otg_id_filter_time_sel otg_id_filter time select 00: 5ms 01:15ms 10: 35ms
7	RO	0x0	reserved
6	RW	0x0	otg_id_fall_edge_detect_en otg_id_fall_edge_detect enable 0: disable 1: enable
5	RW	0x0	otg_id_rise_edge_detect_en otg_id_detect enable 0: disable 1: enable
4	RW	0x0	host_line_state_detect_en host_line_state_detect enable 0: disable 1: enable
3	RW	0x0	otg_bvalid_detect_en otg_bvalid detect enable 0: disable 1: enable
2	RW	0x0	otg_linenstate_detect_en otg_linenstate_detect enable 0: disable 1: enable
1	RW	0x0	sd_detect_fall_edge_detect_en Field0000 Abstract sd_detect_falling_edge enable 0: disable 1: enable
0	RW	0x0	sd_detect_rising_edge_dectect_en sd_detect_rising_edge enable 0: disable 1:enable

**GRF\_SIG\_DETECT\_STATUS**

Address: Operational Base + offset (0x00690)  
 external signal detect configue register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6	RO	0x0	otg_id_fall_edge_detect_status otg_id_fall_edge_detect status 0: disable 1: enable
5	RO	0x0	otg_id_rise_edge_detect_status otg_id_detect status 0: disable 1: enable
4	RO	0x0	host_line_state_detect_status host_line_state_detect status 0: disable 1: enable
3	RO	0x0	otg_bvalid_detect_status otg_bvalid detect status 0: disable 1: enable
2	RO	0x0	otg_linenstate_detect_status otg_linenstate_detect status 0: disable 1: enable
1	RO	0x0	sd_detect_fall_edge_detect_status sd_detect_falling_edge status 0: disable 1: enable

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
0	RO	0x0	sd_detect_rising_edge_dectect_status sd_detect_rising_edge status 0: disable 1:enable

**GRF\_SIG\_DETECT\_CLR**

Address: Operational Base + offset (0x006a0)  
external signal detect configue register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6	WO	0x0	otg_id_fall_edge_detect_clr otg_id_fall_edge_detect enable 0: disable 1: enable
5	WO	0x0	otg_id_rise_edge_detect_clr otg_id_detect enable 0: disable 1: enable
4	WO	0x0	host_line_state_detect_clr host_line_state_detect enable 0: disable 1: enable
3	WO	0x0	otg_bvalid_detect_clr otg_bvalid detect enable 0: disable 1: enable

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
2	WO	0x0	otg_linestate_detect_clr otg_linestate_detect enable 0: disable 1: enable
1	WO	0x0	sd_detect_fall_edge_detect_clr Field0000 Abstract sd_detect_falling_edge enable 0: disable 1: enable
0	WO	0x0	sd_detect_rising_edge_dectect_clr sd_detect_rising_edge enable 0: disable 1:enable

**GRF\_UOC0\_CON0**

Address: Operational Base + offset (0x00700)

OTG control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit 0 ~ bit 15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usb0tg_dbnce_filt_bypass USB OTG debounce filter for input signals bypass enable. This bit is only used in simulation mode.
14:11	RO	0x0	reserved
10	RW	0x0	iddig_status control software iddig value 0:host 1:device

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
9	RW	0x0	iddig_sft_sel 0 : iddig to otg controller select usbphy output 1: iddig to otg controller select grf_uoc0_con0[10]
8	RW	0x0	utmi_dmpulldown 0: DM 15 KOhm pull down disabled 1: DM 15 Kohm pull down enable
7	RW	0x0	utmi_dppulldown 0: DP 15 KOhm pull down disabled 1: DP 15 Kohm pull down enable
6	RW	0x0	utmi_termselect USB Termination Select 1: Full-speed terminations are enabled. 0: High-speed terminations are enabled.
5:4	RW	0x0	utmi_xcvrselect Transceiver Select 11: Sends an LS packet on an FS bus or receives an LS packet. 10: LS Transceiver 01: FS Transceiver 00: HS Transceiver
3:2	RW	0x0	utmi_opmode UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 11: Normal operation without SYNC or EOP generation. If the XCVRSEL bus is not set to 00 while OPMODE[1:0] is set to 11, USB PHY behavior is undefined. 10: Disable bit stuffing and NRZI encoding 01: Non-Driving 00: Normal
1	RW	0x0	utmi_suspend_n Suspend Assertion 1: Normal operating mode 0: Suspend mode
0	RW	0x0	usbphy_soft_con_sel 0: software control usb phy disable 1 : software control usb phy enable

**GRF\_UOC1\_CON1**

Address: Operational Base + offset (0x00718)  
 usb host control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:13	RO	0x0	reserved
12	RW	0x0	usbphy1_vdm_src_en open dm voltage source
11	RW	0x0	usbphy1_vdp_src_en open dp voltage source
10	RW	0x0	usbphy1_rdm_pdwn_en open dm pull down resistor
9	RW	0x0	usbphy1_idp_src_en open dp source current
8	RW	0x0	usbphy1_idm_sink_en open dm sink current enable
7	RW	0x0	usbphy1_idp_sink_en open dp sink current enable
6:0	RO	0x0	reserved

**GRF\_UOC1\_CON2**

Address: Operational Base + offset (0x0071c)  
 UOC1 control register 2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15	RW	0x1	usbhost0_incr4_en USB HOST0 incr4_en bit control
14	RW	0x1	usbhost0_incr16_en USB HOST0 incr16_en bit control
13	RW	0x0	usbhost0_hubsetup_min USB HOST0 hubsetup_min bit control
12	RW	0x0	usbhost0_app_start_clk USB HOST0 app_start_clk bit control
11:6	RW	0x20	usbhost0_fadj_val_common USB HOST0 fadj_val_common bit control
5:0	RW	0x20	usbhost0_fadj USB HOST0 fadj bit control

**GRF\_UOC1\_CON3**

Address: Operational Base + offset (0x00720)

UOC1 control register 3

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15	RW	0x0	usbhost0_ohci_susp_lgcy USB HOST0 ohci_susp_lgcy bit control
14	RW	0x0	usbhost0_ohci_cntsel USB HOST0 ohci_cntsel bit control
13	RW	0x0	usbhost0_app_prt_ovrcur USB HOST0 app_prt_ovrcur bit control
12	RO	0x0	reserved
11	RW	0x1	usbhost0_word_if USB HOST0 word_if bit control
10	RW	0x0	usbhost0_sim_mode USB HOST0 sim_mode bit control
9	RW	0x1	usbhost0_incrx_en USB HOST0 incr_x_en bit control
8	RW	0x1	usbhost0_incr8_en USB HOST0 incr8_en bit control
7	RO	0x0	reserved
6	RW	0x1	usbhost0_ohci_clkcktrst USB HOST0 ohci_clkcktrst bit control
5:2	RO	0x0	reserved
1	RW	0x0	<p>usbhost_sel</p> <p>usb host controller select</p> <p>1: choose old usb controller.</p> <p>0: choose EHCI controller.</p>
0	RW	0x0	usbhost0_autoppd_on_overcur USB HOST0 autoppd_on_overcur bit control

**GRF\_UOC1\_CON4**

Address: Operational Base + offset (0x00724)

USB HOST 2.0 control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable bit0~bit15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15	RW	0x0	usbphy_commonon USBPHY common on
14	RO	0x0	reserved
13	RW	0x0	reserved
12	RW	0x0	reserved
11	RW	0x0	reserved
10	RW	0x0	otgphydisable when 1, otgphy is disabled.
9:8	RW	0x0	utmiotg_scaledown_mode OTG controller scaledown mode. This bit is used only in simulation mode.
7:6	RW	0x0	utmihost_scaledown_mode utmihost scaledown mode. This bit is used only in simulation mode.
5	RW	0x0	utmiotg_idpullup Analog ID Input Sample Enable Function: This controller signal controls ID line sampling. 1: ID pin sampling is enabled, and the IDDIG output is valid. 0: ID pin sampling is disabled, and the IDDIG output is not valid.
4	RW	0x1	utmiotg_dppulldown D+ Pull-Down Resistor Enable
3	RW	0x1	utmiotg_dmpulldown D- Pull-Down Resistor Enable

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
2	RW	0x1	utmiotg_drvvbus Drive VBUS 1: The VBUS Valid comparator is enabled. 0: The VBUS Valid comparator is disabled.
1	RW	0x0	utmisrp_chrgvbus VBUS Input Charge Enable
0	RW	0x0	utmisrp_dischrgvbus VBUS Input Discharge Enable

**GRF\_UOC1\_CON5**

Address: Operational Base + offset (0x00728)

USB HOST 2.0 control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit 0 ~ bit 15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x0	reserved
8	RW	0x0	utmi_dmpulldown 0: DM 15 KOhm pull down disabled 1: DM 15 Kohm pull down enable
7	RW	0x0	utmi_dppulldown 0: DP 15 KOhm pull down disabled 1: DP 15 Kohm pull down enable
6	RW	0x0	utmi_termselect USB Termination Select 1: Full-speed terminations are enabled. 0: High-speed terminations are enabled.

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
5:4	RW	0x0	utmi_xcvrselect Transceiver Select 11: Sends an LS packet on an FS bus or receives an LS packet. 10: LS Transceiver 01: FS Transceiver 00: HS Transceiver
3:2	RW	0x0	utmi_opmode UTMI+ Operational Mode Function: This controller bus selects the UTMI+ operational mode. 11: Normal operation without SYNC or EOP generation. If the XCVRSEL bus is not set to 00 while OPMODE[1:0] is set to 11, USB PHY behavior is undefined. 10: Disable bit stuffing and NRZI encoding 01: Non-Driving 00: Normal
1	RW	0x0	utmi_suspend_n Suspend Assertion 1: Normal operating mode 0: Suspend mode
0	RW	0x0	usbphy_soft_con_sel 0: software control usb phy disable 1 : software control usb phy enable

**GRF\_UOC3\_CON0**

Address: Operational Base + offset (0x00738)

UOC3 control register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15	RO	0x0	reserved
14	RW	0x0	<p>hsicphy_soft_con_sel</p> <p>HSIC PHY software control enale</p>
13	RW	0x1	<p>hsicphy_txbitstuffenh</p> <p>HSIC high byte transmit bit-stuffing enable</p> <p>this controller signal controls biy stuffing on DATAIN[15:8] when OPMODE[1:0]=2'b11</p> <p>1'b1: bit stuffing is enabled</p> <p>1'b0: bit stuffing is disabled</p>
12	RW	0x1	<p>hsicphy_txbitstuffen</p> <p>HSIC low byte transmit bit-stuffing enable</p> <p>this controller signal controls biy stuffing on DATAIN[7:0] when OPMODE[1:0]=2'b11</p> <p>1'b1: bit stuffing is enabled</p> <p>1'b0: bit stuffing is disabled</p>
11	RW	0x0	<p>hsichhy_siddq</p> <p>HSIC SIDDQ test enable</p> <p>1'b1: the analog blocks are power down</p> <p>1'b0: the analog blocks are power up</p>
10	RW	0x0	<p>hsicphy_port_reset</p> <p>HSIC per-port reset</p> <p>when asserted, this customer-specific signal reset the corresponding prot's transmit and receive logic without disabling the clocks within the HSIC PHY</p> <p>1'b1: the transmit and receive FSMs are reset</p> <p>1'b0: tje transmit and receive FSMs are operational</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
9:6	RW	0x3	hsicphy_txsrtune drive slew rate adjustment 4'b1111: +20% 4'b0111: +10% 4'b0011: design default 4'b0001: -10% 4'b0000: -20%
5:4	RW	0x2	hsicphy_txrpdtune HSIC driver pull-down impedance adjustment 2'b11: -5% 2'b10: design default 2'b01: +5% 2'b00: +11%
3:2	RW	0x2	hsicphy_txrputune HSIC driver pull-up impedance adjustment 2'b11: -5% 2'b10: design default 2'b01: +5% 2'b00: +11%
1	RW	0x1	hsicphy_dmpulldown HSIC bus keepers resistor enable This control signal selects the HSIC PHY to operate as a host or device.
0	RW	0x1	hsicphy_dppulldown HSIC bus keepers resistor enable This control signal detects that the HSIC PHY is being used as a host.

**GRF\_UOC3\_CON1**

Address: Operational Base + offset (0x0073c)

UOC3 control register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:5	RO	0x0	reserved
4	RW	0x0	<p>hsic_utmi_xcvrselect</p> <p>HSIC PHY transceiver select</p> <p>1'b1: transceiver is in suspend, resume or connect mode</p> <p>1'b0: transceiver is in HS mode</p>
3:2	RW	0x0	<p>hsic_utmi_opmode</p> <p>HSIC PHY operation mode</p> <p>2'b11: normal mode without SYNC or EOP generation</p> <p>2'b10: disable bit stuffing and NRZI encodeing</p> <p>2'b01: Non-driving</p> <p>2'b00: normal</p>
1	RW	0x1	<p>hsic_utmi_suspend_n</p> <p>HSIC PHY suspend mode enable</p> <p>Asserting this signal places the HSIC PHY in suspend mode.</p> <p>1'b1: normal mode</p> <p>1'b0: suspend mode</p>
0	RW	0x1	<p>hsic_utmi_sleep_n</p> <p>HSIC PHY sleep mode enable</p> <p>Asserting this signal places the HSIC PHY in sleep mode.</p> <p>1'b1: normal mode</p> <p>1'b0: sleep mode</p>

**GRF\_UOC4\_CON0**

Address: Operational Base + offset (0x00740)

## UOC4 control register 0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:10	RO	0x0	reserved
9	RW	0x0	hsic_app_prt_ovrcur HSIC app_prt_ovrcur bit control
8	RW	0x0	hsic_autoppd_on_overcur HSIC autoppd_on_overcur bit control
7	RW	0x1	hsic_word_if HSIC word_if bit control
6	RW	0x0	hsic_sim_mode HSIC sim_mode bit control
5	RW	0x0	hsic_incrx_en HSIC incr_x_en bit control
4	RW	0x0	hsic_incr8_en HSIC incr8_en bit control
3	RW	0x0	hsic_incr4_en HSIC incr4_en bit control
2	RW	0x0	hsic_incr16_en HSIC incr16_en bit control
1	RW	0x0	hsic_hubsetup_min HSIC hubsetup_min bit control
0	RW	0x0	hsic_app_start_clk HSIC app_start_clk bit control

**GRF\_UOC4\_CON1**

Address: Operational Base + offset (0x00744)

UOC4 control register 1

Bit	Attr	Reset Value	Description
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:12	RO	0x0	reserved
11:6	RW	0x20	hsic_fladj_val_common HSIC fladj_val_common bit control
5:0	RW	0x20	hsic_fladj HSIC fladj bit control

**GRF\_USBPHY\_CON0**

Address: Operational Base + offset (0x00780)

USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0x8518	usbphy_con usbphy control register bit 15~0

**GRF\_USBPHY\_CON1**

Address: Operational Base + offset (0x00784)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0xe007	usbphy_con usbphy control register bit 31~16

**GRF\_USBPHY\_CON2**

Address: Operational Base + offset (0x00788)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x02e7	usbphy_con usbphy control register bit 47~32

**GRF\_USBPHY\_CON3**

Address: Operational Base + offset (0x0078c)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0200	usbphy_con usbphy control register bit 63~48

**GRF\_USBPHY\_CON4**

Address: Operational Base + offset (0x00790)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x5556	usbphy_con usbphy control register bit 79~64

**GRF\_USBPHY\_CON5**

Address: Operational Base + offset (0x00794)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x4555	usbphy_con usbphy control register bit 95~80

**GRF\_USBPHY\_CON6**

Address: Operational Base + offset (0x00798)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0005	usbphy_con usbphy control register bit 111~96

**GRF\_USBPHY\_CON7**

Address: Operational Base + offset (0x0079c)

USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x68c0	usbphy_con usbphy control register bit 127~112

**GRF\_USBPHY\_CON8**

Address: Operational Base + offset (0x007a0)

USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x8518	usbphy_con usbphy control register bit 143~128

**GRF\_USBPHY\_CON9**

Address: Operational Base + offset (0x007a4)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0xe007	usbphy_con usbphy control register bit 159~144

**GRF\_USBPHY\_CON10**

Address: Operational Base + offset (0x007a8)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x02e7	usbphy_con usbphy control register bit 175~160

**GRF\_USBPHY\_CON11**

Address: Operational Base + offset (0x007ac)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0200	usbphy_con usbphy control register bit 191~176

**GRF\_USBPHY\_CON12**

Address: Operational Base + offset (0x007b0)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x5556	usbphy_con usbphy control register bit 207~192

**GRF\_USBPHY\_CON13**

Address: Operational Base + offset (0x007b4)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x4555	usbphy_con usbphy control register bit 223~208

**GRF\_USBPHY\_CON14**

Address: Operational Base + offset (0x007b8)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0005	usbphy_con usbphy control register bit 239~224

**GRF\_USBPHY\_CON15**

Address: Operational Base + offset (0x007bc)  
 USB PHY control register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x68c0	usbphy_con usbphy control register bit 255~240

**GRF\_PVTM\_CON0**

Address: Operational Base + offset (0x00800)  
 PVT monitor control register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:10	RO	0x0	reserved

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
9	RW	0x0	pvtm_gpu_osc_en pd_gpu PVT monitor oscillator enable 1'b1: enable 1'b0: disable
8	RW	0x0	pvtm_gpu_start pd_gpu PVT monitor start control
7:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_osc_en pd_core PVT monitor oscillator enable 1'b1: enable 1'b0: disable
0	RW	0x0	pvtm_core_start pd_core PVT monitor start control

**GRF\_PVTM\_CON1**

Address: Operational Base + offset (0x00804)

PVT monitor control register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x016e3600	pvtm_core_cal_cnt pd_core pvtm calculator counter

**GRF\_PVTM\_CON2**

Address: Operational Base + offset (0x00808)

PVT monitor control register 2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x016e3600	pvtm_gpu_cal_cnt pd_gpu pvtm calculator counter

**GRF\_PVTM\_STATUS0**

Address: Operational Base + offset (0x0080c)

PVT monitor status register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:2	RO	0x0	reserved
1	RW	0x0	pvtm_gpu_freq_done pd_gpu pvtm frequency calculate done status
0	RW	0x0	pvtm_core_freq_done pd_core pvtm frequency calculate done status

**GRF\_PVTM\_STATUS1**

Address: Operational Base + offset (0x00810)

PVT monitor status register 1

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	pvtm_core_freq_cnt pd_core pvtm frequency count

**GRF\_PVTM\_STATUS2**

Address: Operational Base + offset (0x00814)

PVT monitor status register 2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	pvtm_gpu_freq_cnt pd_gpu pvtm frequency count

**GRF\_IO\_VSEL**

Address: Operational Base + offset (0x00900)

IO voltage select

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x0	reserved
8	RW	0x0	gpio1830_v18sel GPIO1830 IO domain 1.8V voltage selection 1'b0: 3.3V/2.5V 1'b1: 1.8V
7	RW	0x0	gpio30_v18sel GPIO30 IO domain 1.8V voltage selection 1'b0: 3.3V/2.5V 1'b1: 1.8V
6	RW	0x0	sdcard_v18sel SDCARD IO domain 1.8V voltage selection 1'b0: 3.3V/2.5V 1'b1: 1.8V

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
5	RW	0x0	audio_v18sel AUDIO IO domain 1.8V voltage selection 1'b0: 3.3V/2.5V 1'b1: 1.8V
4	RO	0x0	reserved
3	RW	0x0	wifi_v18sel WIFI IO domain 1.8V voltage selection 1'b0: 3.3V/2.5V 1'b1: 1.8V
2	RW	0x1	flash0_v18sel FLASH0 IO domain 1.8V voltage selection 1'b0: 3.3V/2.5V 1'b1: 1.8V
1	RW	0x0	dvp_v18sel DVP IO domain 1.8V voltage selection 1'b0: 3.3V/2.5V 1'b1: 1.8V
0	RO	0x0	reserved

**GRF\_SARADC\_TESTBIT**

Address: Operational Base + offset (0x00904)

SARADC Test bit register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:8	RO	0x0	reserved
7:0	RW	0x00	saradc_testbit SARADC test bit

**GRF\_FAST\_BOOT\_ADDR**

Address: Operational Base + offset (0x00f80)

Fast boot address

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	fast_boot_addr fast boot address control

**5.4 PMUGRF Register Description****5.4.1 Register Summary**

<b>Name</b>	<b>Offset</b>	<b>Size</b>	<b>Reset Value</b>	<b>Description</b>
PMUGRF_GPIO0A_IO_MUX	0x00000	W	0x00000000	GPIO0A iomux control
PMUGRF_GPIO0B_IO_MUX	0x00004	W	0x00000000	GPIO0B iomux control
PMUGRF_GPIO0C_IO_MUX	0x00008	W	0x00000000	GPIO0B iomux control
PMUGRF_GPIO0D_IO_MUX	0x0000c	W	0x00000000	GPIO0D iomux control
PMUGRF_GPIO0A_P	0x00010	W	0x0000aaaa	GPIO0A PU/PD control
PMUGRF_GPIO0B_P	0x00014	W	0x0000aaaa	GPIO0B PU/PD control
PMUGRF_GPIO0C_P	0x00018	W	0x0000aaaa	GPIO0C PU/PD control
PMUGRF_GPIO0D_P	0x0001c	W	0x0000aaaa	GPIO0D PU/PD control
PMUGRF_GPIO0A_E	0x00020	W	0x00005555	GPIO0A drive strength control
PMUGRF_GPIO0B_E	0x00024	W	0x00005555	GPIO0D drive strength control
PMUGRF_GPIO0C_E	0x00028	W	0x00000009	GPIO0C drive strength control
PMUGRF_GPIO0D_E	0x0002c	W	0x00000400	GPIO0D drive strength control
PMUGRF_GPIO0L_SR	0x00030	W	0x00000000	GPIO0 A/B SR control
PMUGRF_GPIO0H_SR	0x00034	W	0x0000000f	GPIO0C/D SR control
PMUGRF_SOC_CON0	0x00100	W	0x00000380	SoC control register 0
PMUGRF_PMUPVTM_CON0	0x00180	W	0x00000000	pmu pvtm configuration register
PMUGRF_PMUPVTM_CON1	0x00184	W	0x00000000	pmu pvtm configuration register
PMUGRF_PMUPVTM_STATUS0	0x00190	W	0x00000000	pmu pvtm status register

Name	Offset	Size	Reset Value	Description
PMUGRF_PMUPVTM_STATUS1	0x00194	W	0x00000000	pmu pvtm status register
PMUGRF_OS_REG0	0x00200	W	0x00000000	os register
PMUGRF_OS_REG1	0x00204	W	0x00000000	os register
PMUGRF_OS_REG2	0x00208	W	0x00000000	os register
PMUGRF_OS_REG3	0x0020c	W	0x00000000	os register

Notes: **Size** : **B** - Byte (8 bits) access, **HW** - Half WORD (16 bits) access, **W** -WORD (32 bits) access

## 5.4.2 Detail Register Description

### PMUGRF\_GPIO0A\_IOMUX

Address: Operational Base + offset (0x00000)

GPIO0A iomux control

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:14	RW	0x0	<p>gpio0a7_sel</p> <p>GPIO0A[7] iomux select</p> <p>2'b00: gpio</p> <p>2'b01: i2c0pmu_scl</p> <p>2'b10: reserved</p> <p>2'b11: reserved</p>
13:12	RW	0x0	<p>gpio0a6_sel</p> <p>GPIO0A[6] iomux select</p> <p>2'b00: gpio</p> <p>2'b01: i2c0pmu_sda</p> <p>2'b10: reserved</p> <p>2'b11: reserved</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
11:10	RW	0x0	gpio0a5_sel GPIO0A[5] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
9:8	RW	0x0	gpio0a4_sel GPIO0A[4] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
7:6	RW	0x0	gpio0a3_sel GPIO0A[3] iomux select 2'b00: gpio 2'b01: tsadc_int 2'b10: pmu_debug0 2'b11: reserved
5:4	RW	0x0	gpio0a2_sel GPIO0A[2] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
3:2	RW	0x0	gpio0a1_sel GPIO0A[1] iomux select 2'b00: gpio 2'b01: reserved 2'b10: reserved 2'b11: reserved
1:0	RW	0x0	gpio0a0_sel GPIO0A[0] iomux select 2'b00: gpio 2'b01: global_pwroff 2'b10: pmic_sleep 2'b11: reserved

**PMUGRF\_GPIO0B\_IOMUX**

Address: Operational Base + offset (0x00004)

GPIO0B iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio0b7_sel GPIO0B[7] iomux select 2'b00: gpio 2'b01: lcdc_data11 2'b10: trace_data1 2'b11: jtag_tdi
13:12	RW	0x0	gpio0b6_sel GPIO0B[6] iomux select 2'b00: gpio 2'b01: lcdcdata10 2'b10: trace_data0 2'b11 :jtag_trstn
11:10	RW	0x0	gpio0b5_sel GPIO0B[5] iomux select 2'b00: gpio 2'b01: sc_detect 2'b10: spi2_csn0 2'b11: reserved
9:8	RW	0x0	gpio0b4_sel GPIO0B4] iomux select 2'b00: gpio 2'b01: sc_io 2'b10: spi2_clk 2'b11: gpujtag_tdo

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio0b3_sel GPIO0B[3] iomux select 2'b00: gpio 2'b01: sc_clk 2'b10: spi2_txd 2'b11: gputag_tdi
5:4	RW	0x0	gpio0b2_sel GPIO0B[2] iomux select 2'b00: gpio 2'b01: sc_rst 2'b10: spi2_rxd 2'b11: gputag_tms
3:2	RW	0x0	gpio0b1_sel GPIO0B[1] iomux select 2'b00: gpio 2'b01: sc_vcc33v 2'b10: i2c2sensor_scl 2'b11: gputag_trstn
1:0	RW	0x0	gpio0b0_sel GPIO0B[0] iomux select 2'b00: gpio 2'b01: test_clkout 2'b10: pwm_1 2'b11: pmu_debug_1

**PMUGRF\_GPIO0C\_IOMUX**

Address: Operational Base + offset (0x00008)

GPIO0B iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio0c7_sel GPIO0C[7] iomux select 2'b00: gpio 2'b01: lcdc_data19 2'b10: trace_data9 2'b11: uart1bb_rtsn
13:12	RW	0x0	gpio0c6_sel GPIO0C[6] iomux select 2'b00: gpio 2'b01: lcdc_data18 2'b10: trace_data8 2'b11: uart1bb_ctsn
11:10	RW	0x0	gpio0c5_sel GPIO0C[5] iomux select 2'b00: gpio 2'b01: lcdc_data17 2'b10: trace_data7 2'b11: uart1bb_sout
9:8	RW	0x0	gpio0c4_sel GPIO0C[4] iomux select 2'b00: gpio 2'b01: lcdc_data16 2'b10: trace_data6 2'b11: uart1bb_sin

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio0c3_sel GPIO0C[3] iomux select 2'b00: gpio 2'b01: lcdc_data15 2'b10: trace_data5 2'b11: mcujtag_tdo
5:4	RW	0x0	gpio0c2_sel GPIO0C[2] iomux select 2'b00: gpio 2'b01: lcdc_data14 2'b10: trace_data4 2'b11: mcujtag_tdi
3:2	RW	0x0	gpio0c1_sel GPIO0C[1] iomux select 2'b00: gpio 2'b01: lcdc_data13 2'b10: trace_data3 2'b11: mcujtag_trstn
1:0	RW	0x0	gpio0c0_sel GPIO0C[0] iomux select 2'b00: gpio 2'b01: lcdc_data12 2'b10: trace_data2 2'b11: jtag_tdo

**PMUGRF\_GPIOOD\_IOMUX**

Address: Operational Base + offset (0x0000c)

GPIOOD iomux control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:14	RW	0x0	gpio0d7_sel GPIO0D[7] iomux select 2'b00: gpio 2'b01: lcdc_dclk 2'b10: trace_ctl 2'b11: pmu_debug5
13:12	RW	0x0	gpio0d6_sel GPIO0D[6] iomux select 2'b00: gpio 2'b01: lcdc_den 2'b10: trace_clk 2'b11: pmu_debug4
11:10	RW	0x0	gpio0d5_sel GPIO0D[5] iomux select 2'b00: gpio 2'b01: lcdc_vsync 2'b10: trace_data15 2'b11: pmu_debug3
9:8	RW	0x0	gpio0d4_sel GPIO0D[4] iomux select 2'b00: gpio 2'b01: lcdc_hsync 2'b10: trace_data14 2'b11: pmu_debug2

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
7:6	RW	0x0	gpio0d3_sel GPIO0D[3] iomux select 2'b00: gpio 2'b01: lcdc_data23 2'b10: trace_data13 2'b11: uart4exp_sin
5:4	RW	0x0	gpio0d2_sel GPIO0D[2] iomux select 2'b00: gpio 2'b01: lcdc_data22 2'b10: trace_data12 2'b11: uart4exp_sout
3:2	RW	0x0	gpio0d1_sel GPIO0D[1] iomux select 2'b00: gpio 2'b01: lcdc_data21 2'b10: trace_data11 2'b11: uart4exp_rtsn
1:0	RW	0x0	gpio0d0_sel GPIO0D[0] iomux select 2'b00: gpio 2'b01: lcdc_data20 2'b10: trace_data10 2'b11: uart4exp_ctsn

**PMUGRF\_GPIO0A\_P**

Address: Operational Base + offset (0x00010)

GPIO0A PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0xaaaa	<p>gpio0a_p</p> <p>GPIO0A PU/PD programmation section, every GPIO bit corresponding to 2bits</p> <p>2'b00: Z(Noraml operaton);</p> <p>2'b01: weak 1(pull-up);</p> <p>2'b10: weak 0(pull-down);</p> <p>2'b11: Repeater(Bus keeper)</p>

**PMUGRF\_GPIOOB\_P**

Address: Operational Base + offset (0x00014)

GPIOOB PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0xaaaa	gpio0b_p GPIO0B PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**PMUGRF\_GPIO0C\_P**

Address: Operational Base + offset (0x00018)

GPIO0C PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software . When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software . When bit 17=0, bit 1 cannot be written by software; ..... When bit 31=1, bit 15 can be written by software . When bit 31=0, bit 15 cannot be written by software;
15:0	RW	0xaaaa	gpio0c_p GPIO0C PU/PD programmation section, every GPIO bit corresponding to 2bits 2'b00: Z(Noraml operaton); 2'b01: weak 1(pull-up); 2'b10: weak 0(pull-down); 2'b11: Repeater(Bus keeper)

**PMUGRF\_GPIO0D\_P**

Address: Operational Base + offset (0x0001c)

GPIO0D PU/PD control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0xaaaa	<p>gpio0d_p</p> <p>GPIO0D PU/PD programmation section, every GPIO bit corresponding to 2bits</p> <p>2'b00: Z(Noraml operaton);</p> <p>2'b01: weak 1(pull-up);</p> <p>2'b10: weak 0(pull-down);</p> <p>2'b11: Repeater(Bus keeper)</p>

**PMUGRF\_GPIO0A\_E**

Address: Operational Base + offset (0x00020)

GPIO0A drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x5555	<p>gpio0a_e</p> <p>GPIO0A drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA</p>

**PMUGRF\_GPIO0B\_E**

Address: Operational Base + offset (0x00024)

GPIO0D drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x5555	<p>gpio0b_e</p> <p>GPIO0B drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA 2'b01: 4mA 2'b10: 8mA 2'b11: 12mA</p>

**PMUGRF\_GPIO0C\_E**

Address: Operational Base + offset (0x00028)

GPIO0C drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:0	RW	0x0009	<p>gpio0c_e</p> <p>GPIO0C drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**PMUGRF\_GPIOOD\_E**

Address: Operational Base + offset (0x0002c)

GPIOOD drive strength control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
15:0	RW	0x0400	<p>gpio0d_e</p> <p>GPIO0D drive strength control, every GPIO bit corresponding to 2bits</p> <p>2'b00: 2mA</p> <p>2'b01: 4mA</p> <p>2'b10: 8mA</p> <p>2'b11: 12mA</p>

**PMUGRF\_GPIO0L\_SR**

Address: Operational Base + offset (0x00030)

GPIO0 A/B SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:8	RW	0x00	<p>gpio0b_sr</p> <p>GPIO0B slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>
7:0	RW	0x00	<p>gpio0a_sr</p> <p>GPIO0A slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>

**PMUGRF\_GPIO0H\_SR**

Address: Operational Base + offset (0x00034)

GPIO0C/D SR control

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
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<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	WO	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>
15:8	RW	0x00	<p>gpio0d_sr</p> <p>GPIO0D slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>
7:0	RW	0x0f	<p>gpio0c_sr</p> <p>GPIO0C slew rate control for each bit</p> <p>1'b0: slow (half frequency)</p> <p>1'b1: fast</p>

**PMUGRF\_SOC\_CON0**

Address: Operational Base + offset (0x00100)

SoC control register 0

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:16	RW	0x0000	<p>write_enable</p> <p>bit0~15 write enable</p> <p>When bit 16=1, bit 0 can be written by software .</p> <p>When bit 16=0, bit 0 cannot be written by software;</p> <p>When bit 17=1, bit 1 can be written by software .</p> <p>When bit 17=0, bit 1 cannot be written by software;</p> <p>.....</p> <p>When bit 31=1, bit 15 can be written by software .</p> <p>When bit 31=0, bit 15 cannot be written by software;</p>

Bit	Attr	Reset Value	Description
15:11	RO	0x0	reserved
10	RW	0x0	pd_pmu_RST_HOLD pd_pmu IP reset hold control, including gpio0, pmu_grf, secure_grf block. 1'b0: don't hold the reset 1'b1: keep the reset as de-asserted even if the reset source is asserted
9	RW	0x1	ddrphy_bufferen_io_en ddr phy bufferen controlled by IO 0: enable 1: disable
8	RW	0x1	ddrphy_bufferen_core_en ddr phy bufferen controlled by core 0: enable 1: disable
7	RW	0x1	pwm2_sel 0: 32K clock source 1: pwm2
6	RW	0x0	chip_32k_src chip 32K clock source select 0: from external 1: from internal, pvtm
5	RW	0x0	poc_vop_sel18 VOP IO domain 1.8V voltage selection 0:3.3V/2.5V 1:1.8V
4	RW	0x0	poc_pmu_sel18 PMU IO domain 1.8V voltage selection 0:3.3V/2.5V 1:1.8V
3	RW	0x0	gpio_0a7_smt gpio_0b7 schmitt trigger control. 0: No hysteresis 1: Schmitt trigger enabled.
2	RW	0x0	gpio_0a6_smt Field0002 Abstract gpio_0a6 schmitt trigger control. 0: No hysteresis 1: Schmitt trigger enabled.

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
1:0	RW	0x0	x32k_crnt_ctrl x32k pad drive strength control bit 00: 2mA 01: 4mA 10: 8mA 11: 12mA

**PMUGRF\_PMUPVTM\_CON0**

Address: Operational Base + offset (0x00180)

pmu pvtm configuration register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:2	RO	0x0	reserved
1	RW	0x0	pvtm_core_osc_en pd_core PVT monitor oscillator enable 1'b1: enable 1'b0: disable
0	RW	0x0	pvtm_core_start pd_core PVT monitor start control

**PMUGRF\_PMUPVTM\_CON1**

Address: Operational Base + offset (0x00184)

pmu pvtm configuration register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	pvtm_core_cal_cnt pd_core pvtm calculator counter

**PMUGRF\_PMUPVTM\_STATUS0**

Address: Operational Base + offset (0x00190)

pmu pvtm status register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:1	RO	0x0	reserved
0	RW	0x0	pvtm_freq_done pvtm frequency calculate done status

**PMUGRF\_PMUPVTM\_STATUS1**

Address: Operational Base + offset (0x00194)

pmu pvtm status register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	pvtm_freq_cnt pvtm frequency count

**PMUGRF\_OS\_REG0**

Address: Operational Base + offset (0x00200)  
os register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	os_reg0 os register

### **PMUGRF\_OS\_REG1**

Address: Operational Base + offset (0x00204)  
os register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	os_reg1 os register

### **PMUGRF\_OS\_REG2**

Address: Operational Base + offset (0x00208)  
os register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	os_reg2 os register

### **PMUGRF\_OS\_REG3**

Address: Operational Base + offset (0x0020c)  
os register

<b>Bit</b>	<b>Attr</b>	<b>Reset Value</b>	<b>Description</b>
31:0	RW	0x00000000	os_reg3 os register