Lab 1 - Student Work Distribution

- MUX 64x1 - Isaac E.
  - Designed the overall schematic and outline for the 64x1 MUX
  - Designed the Vivado implementation of the 64x1 MUX using 2x1 MUX generic design from Jacob
  - Completed the first portion(s) of the report (not significant work)
- Testbench - Jacob S.
  - Non-txtio simulation (to verify functionality of MUX - commented out in final code)
  - Txtio simulation testbench to show functionality of the mux when taking in data stream and outputting results to a .txt
- MUX 16x1 Demo - Adrian A.
  - Modified the 64x1 MUX code to fit the 16x1 MUX specifications for the DEMO.
  - Edited constraint file to work with the NEXYS 4DDR development board and tested code on the board.
  - Reviewed and made minor modifications to the report.