California Polytechnic State University, Pomona

ECE 4304.01
Lab 4

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Architecture

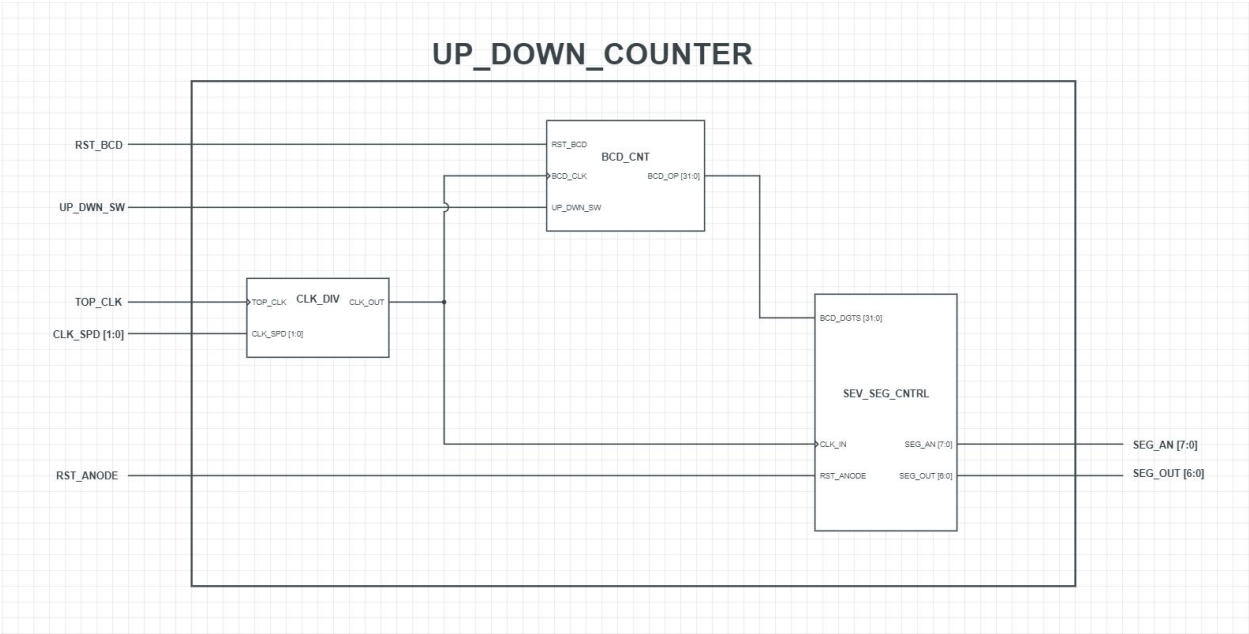

Fig. 4.1 - Initial Design

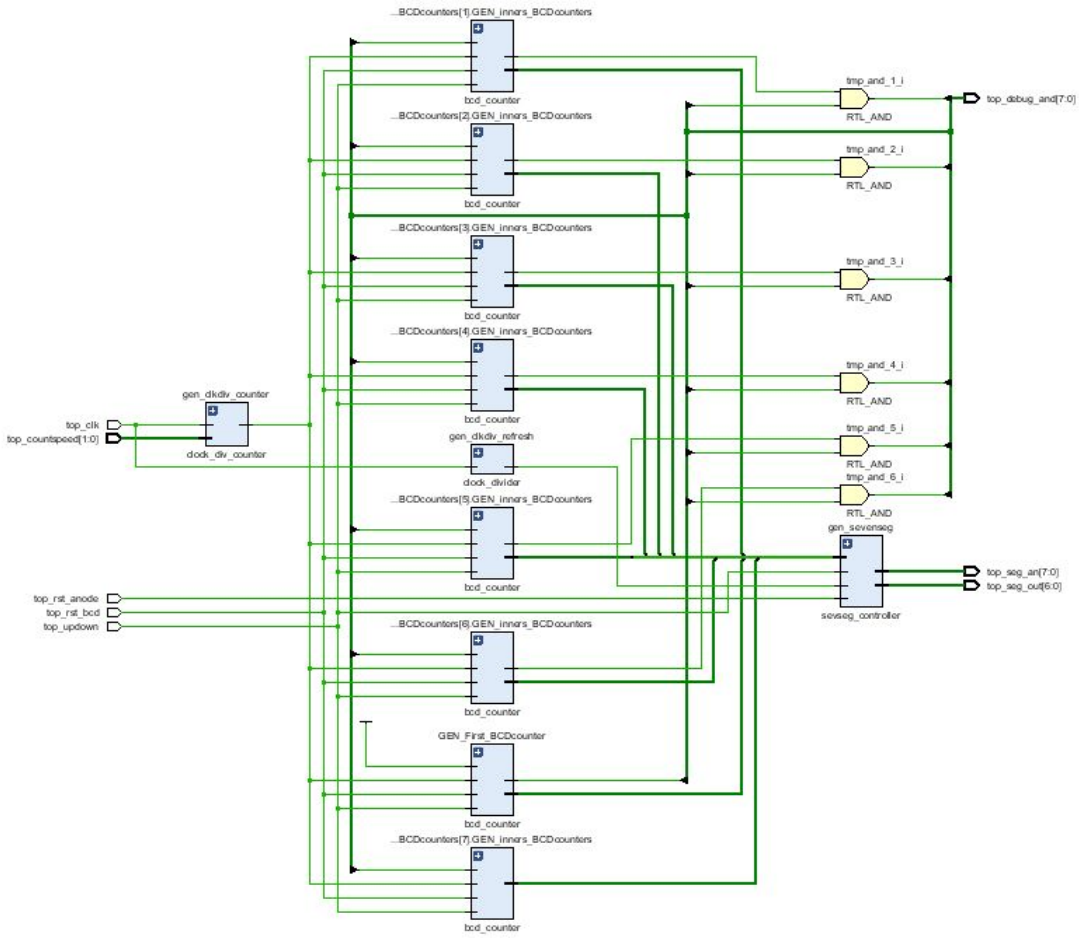

Fig 4.2 - Implemented Design

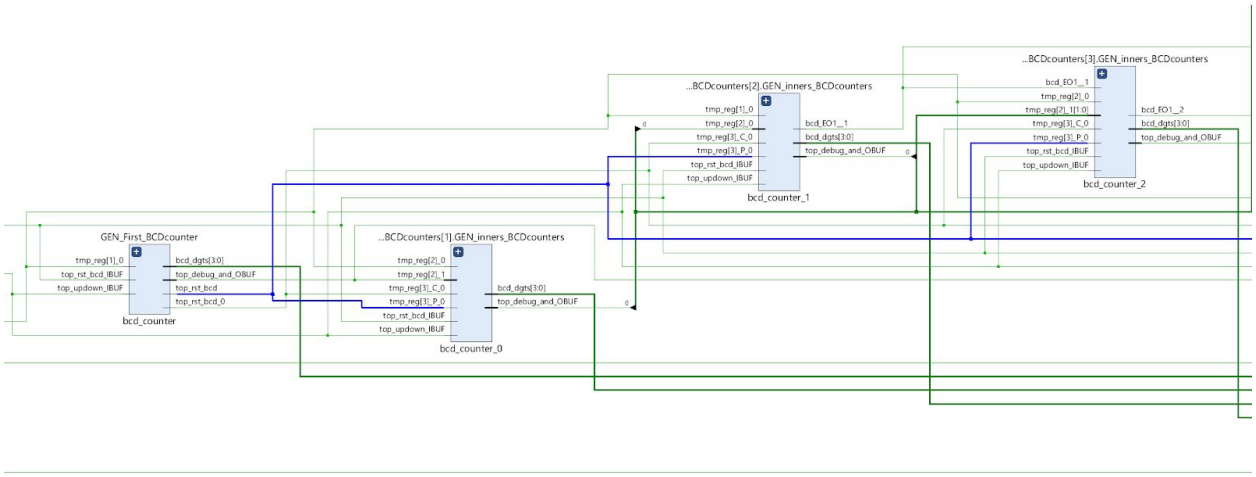

Fig. 4.3 - Cascaded Counter in Synthesis Design

Trick of the Codes

When creating the design for the project we tried to figure out how to make the BCD Counter work for all the individual digits on the seven segment display, what we came up with were cascaded BCD counters that feeded into each other with the use of carry-in enables. In **Figure 4.3** the cascaded counters can be seen in the synthesis design given in Vivado. In addition to the cascaded BCD Counters, the Inner BCD Counters had an enable which were ANDed so that each counter in the line of cascaded counters will only increment when *all* of the previous counters have reached the reset (9 for up count, 0 for down count). We also made the outputs of the AND gates a top output in order to observe on the LEDs when each counter was getting a signal to increment (this was used for debugging purposes).

In order to have the display and the counter have separate resets we had to include a top reset for the BCD counter module and the another reset for the seven segment display. The results were a display that was turned off while the button is being pressed and the counter continuing to count. And if resetting the counter, if the UP_DWN_SW is high it will reset it to all zeroes to begin counting up; if UP_DWN_SW is low, the reset will reset to all nines so that the counter will begin to count down.

Corner Cases

- N/A

Pick the area/resources information from the tool

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM
✓ synth_1	constrs_1	synth_design Complete!								210	117	0.0
✓ impl_1	constrs_1	write_bitstream Complete!	4.304	0.000	0.263	0.000	0.000	0.128	0	207	117	0.0

Figure 4.4 - Design Runs

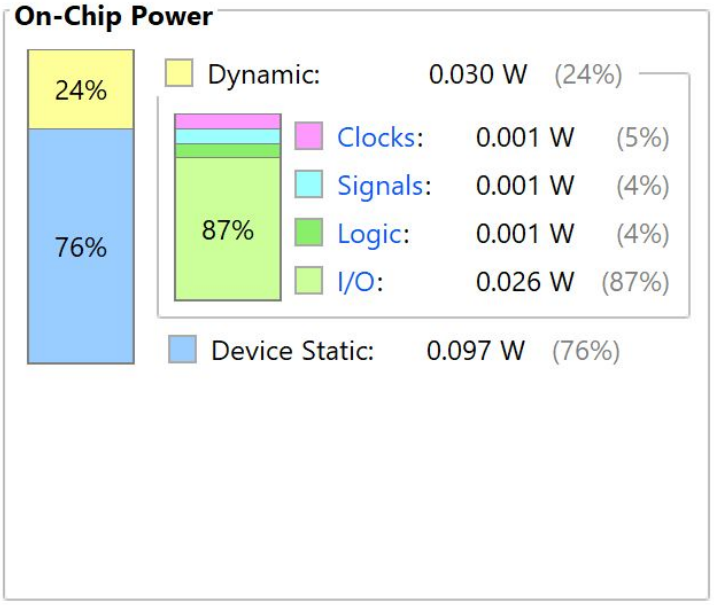

Fig. 4.5 - On-Chip Power