California Polytechnic State University, Pomona

ECE 4304.01
Lab 8

Adrian Alarcon
Isaac Elizarraz
Jacob Swenke

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Architecture

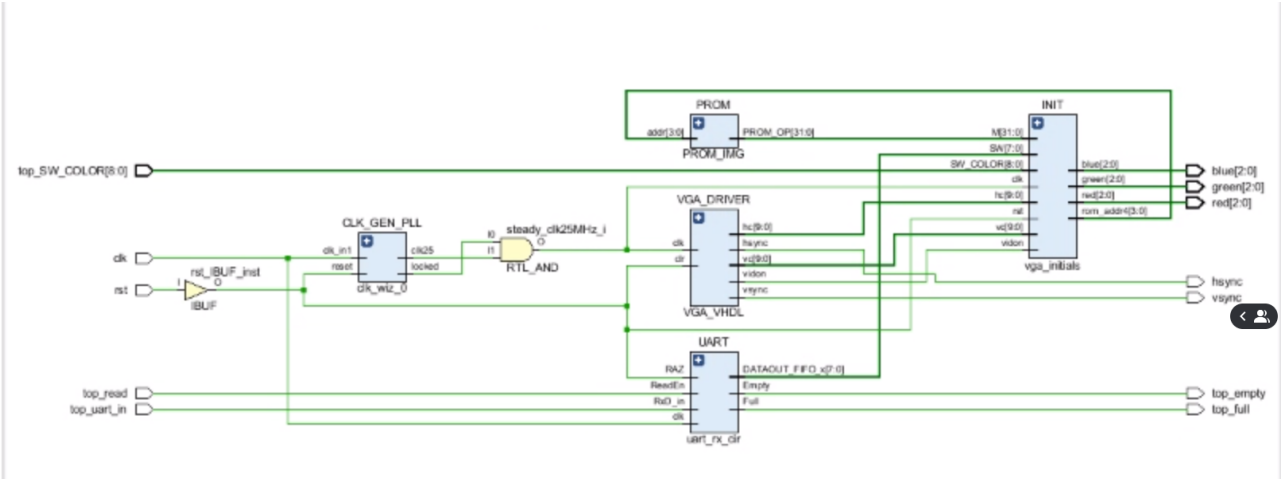

Fig. 8.1 - Elaborated Design

Trick of the Code

The primary focus of this lab was on the VGA module; there were some workarounds to getting the colors to display. In order to make the colored pixels we made a conditional statement that would determine whether the individual pixel would be on or off. For our purposes, we used and statements to set our pix_rom selected bits colored portions. In lecture, Professor Aly mentioned that we needed 3 separate pix_rom's in order to control the color scheme of the VGA with switches. We found this to be overly complicated, and a much simpler implementation can be done by simply forcing the pixel color scheme to be low in certain areas whenever a pixel is determined to be on. For example, if you have a rom_pix selection in our 32 bit array of say pixel 7, and it is determined that this pixel will be ON at the time of display, we can set the ON state to be colored by forcing the high bits of 111, 111 , 111 (RGB) to be 110,101,100 for instance. This is a very simple trick that allows us to perform the exact thing the Professor asked for with the lowest power and highest efficiency.

The outputs front the UART are loaded into a register which contains the data sent from Real Term. When we load the values from the register to the VGA module, it is like we are flipping any of the 8 switches that we used to control the position of the image on the screen before, it's just that we sent it through UART from a PC instead.

Resource Information

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
synth_1 (active)	**constrs_1**	**synth_design Complete!**								**105**	**83**	**0.0**	**0**	**0**
impl_1	constrs_1	write_bitstream Complete!	2.151	0.000	0.179	0.000	0.000	0.302	0	103	83	0.0	0	0
Out-of-Context Module Runs														
clk_wiz_1_synth_1	clk_wiz_1	synth_design Complete!								0	0	0.0	0	0
clk_wiz_0		Using cached IP results												

Fig. 8.3 - Design Runs

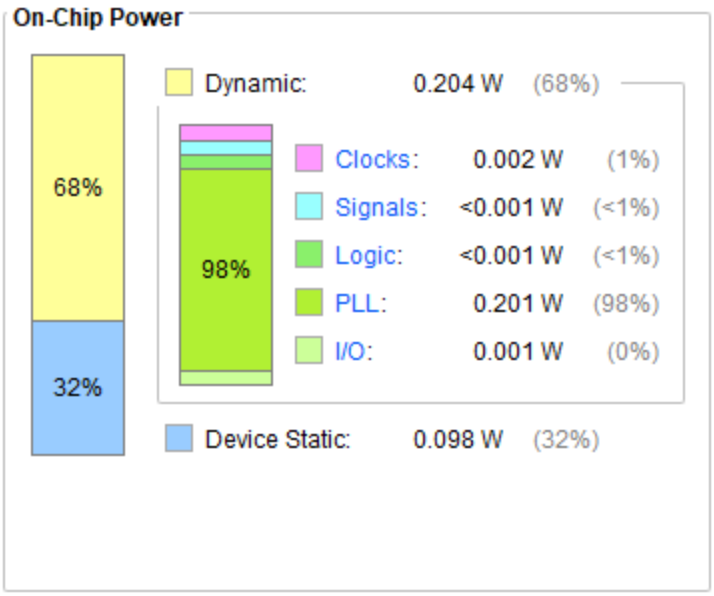

Fig. 8.4 - On-Chip Power