California Polytechnic State University, Pomona

ECE 4304.01
Lab 7

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Architecture

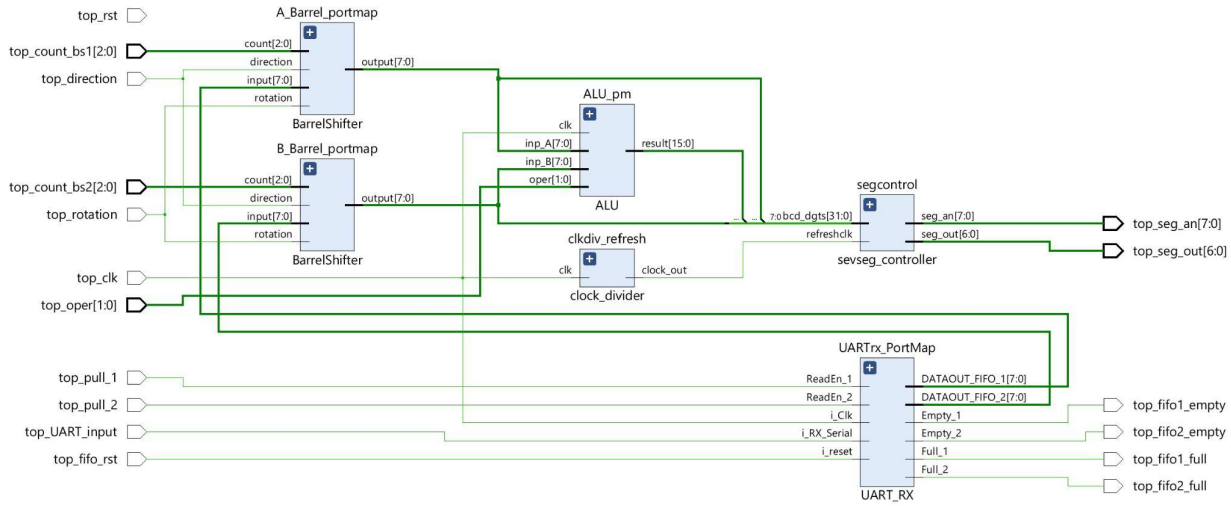

Fig. 7.1 - Elaborated Design

Trick of the Code

This lab was a combination of all of the prior labs with the exception of the UART and FIFO modules. The majority of the time was invested in implementing the UART and FIFO modules; secondary to that, the Top_File wired all of the different modules from before together. In figure 7.1 the schematic retrieved from the elaborated design matches the requested design from the lab session.

We used the Real Term serial terminal as our way of communicating with the ports. Normally Tera Term is used, it excels with ASCII characters, however, in this case we would like to use binary. And Real Term gives us the option to do so.

In order to make the UART and FIFO work in the way we need for this lab, we needed to tweak the existing files a little bit. We had to add another input and output for the UART module so that we can pull data from each of the fifos with a button push, and another output so that we can get the data sent out of each FIFO into their respective barrel shifters. This wasn't too bad to implement and only required a little bit of wiring and patience.

Resource Information

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP
✓ synth_1	constrs_1	synth_design Complete!								303	119	0.0	0	0
✓ impl_1	constrs_1	write_bitstream Complete!	5.414	0.000	0.154	0.000	0.000	0.134	0	288	119	0.0	0	0

Fig. 7.3 - Design Runs

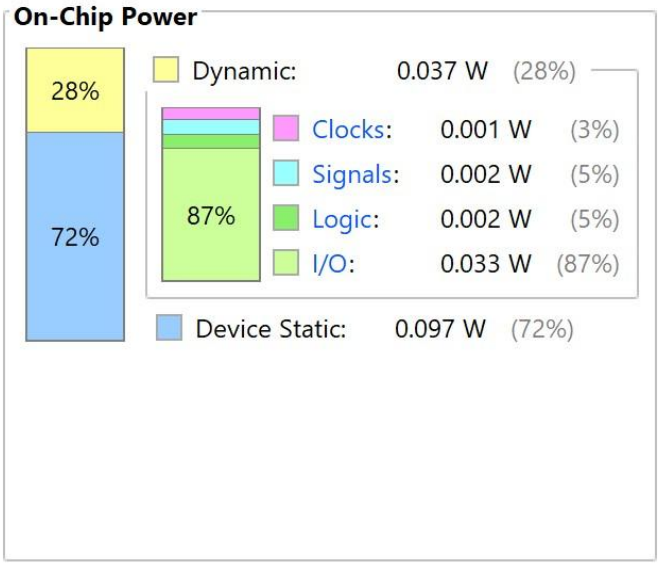

Fig. 7.4 - On-Chip Power