California Polytechnic State University, Pomona
ECE 4304.01
Lab 2
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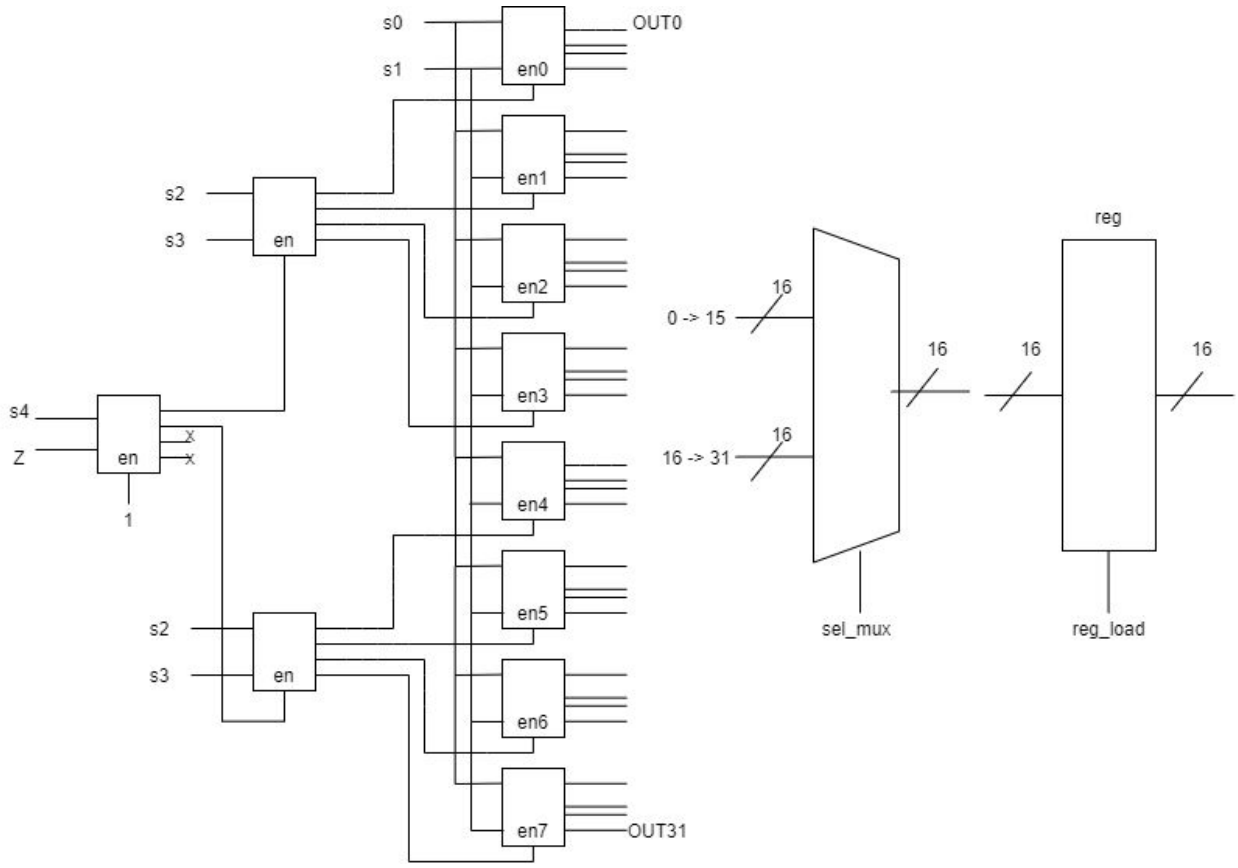
2/17/21

Architecture



Trick of the Codes

Initially, we aimed to implement a generic 5x32 decoder using a network of 2x4 decoders, but faced many issues along the way. One of the main things blocking us from making progress in the initial phases was the generation pattern of the decoders. After we determined the pattern for the generation, which gave us a little trouble at first, we were getting a lot of syntax errors trying to generate port maps inside processes, among other things. After figuring out some of the minor syntax errors that were actually more difficult to solve than anticipated, we hit another wall in the case of the wiring. I think our understanding of how wiring works in VHDL and what syntax goes along with it wasn't fully up to par in the beginning of the lab and it only served to make everything more confusing. Although we weren't able to complete the generic model in the end, we feel that what we learned from our mistakes throughout this lab were invaluable to gaining a better understanding of how hardware design in VHDL works and it will help us reach better solutions to the problems proposed in our future labs in the class.

Corner Cases

During the development of the generic code, we encountered many issues. Primarily how to distinguish when an input was odd or even and how to implement it so that a fully generic code was realized. If an input was even, it would be easier to implement, but covering an odd input brought issues as the basis for this generic circuit was made from 2x4 decoders.

Pick the area/resources information from the tool

N/A