California Polytechnic State University, Pomona
ECE 4304.01
Lab 1
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Architecture

The design before we started coding in VHDL is shown below. The selects connect to all corresponding brackets of 2x1 Mux, with each set of outputs connecting to the next brackets inputs. In order to implement 64x1, we needed 32 2x1 MUX (2^6 inputs), cascading down by powers of 2 until we reached 2 final inputs with 1 output.

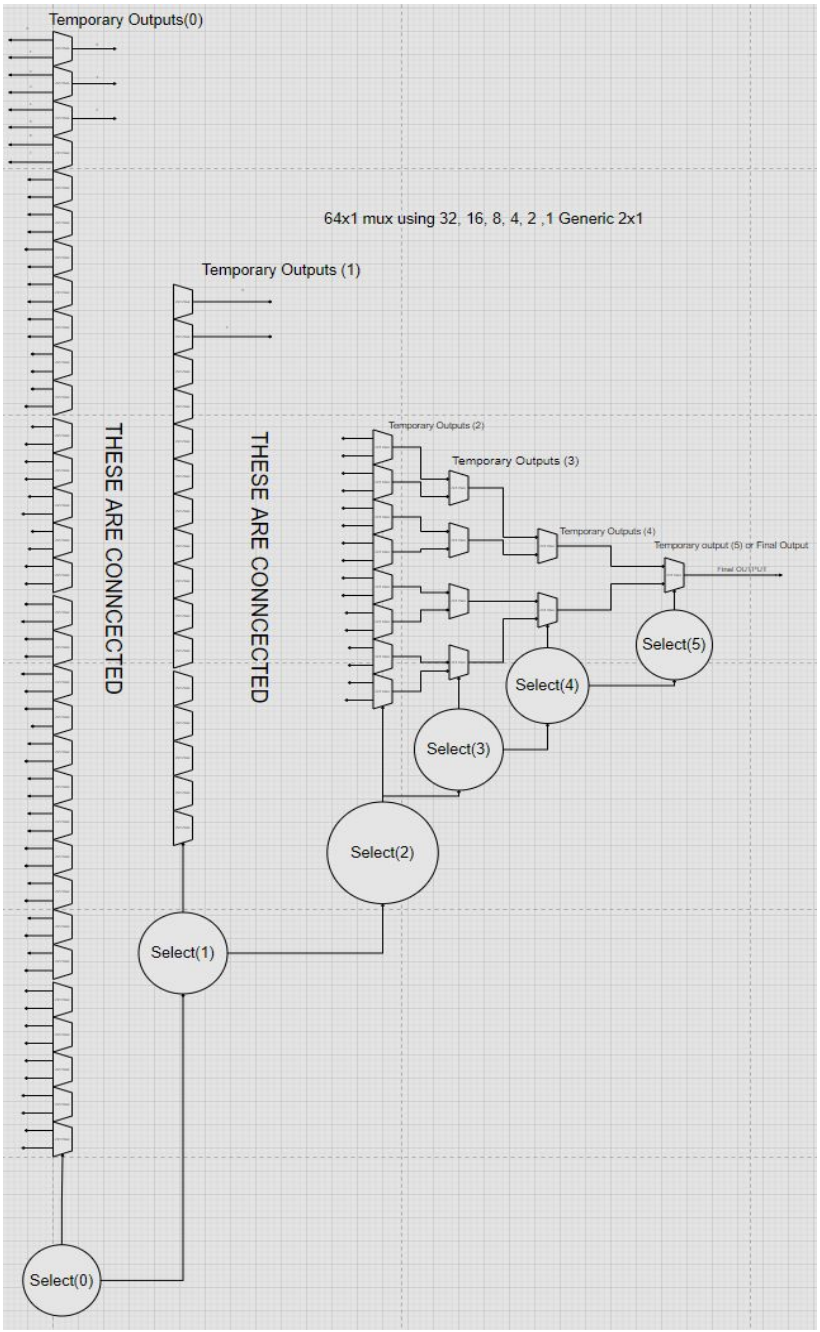


Fig 1.1 - Sketch/Schematic used to design system for lab

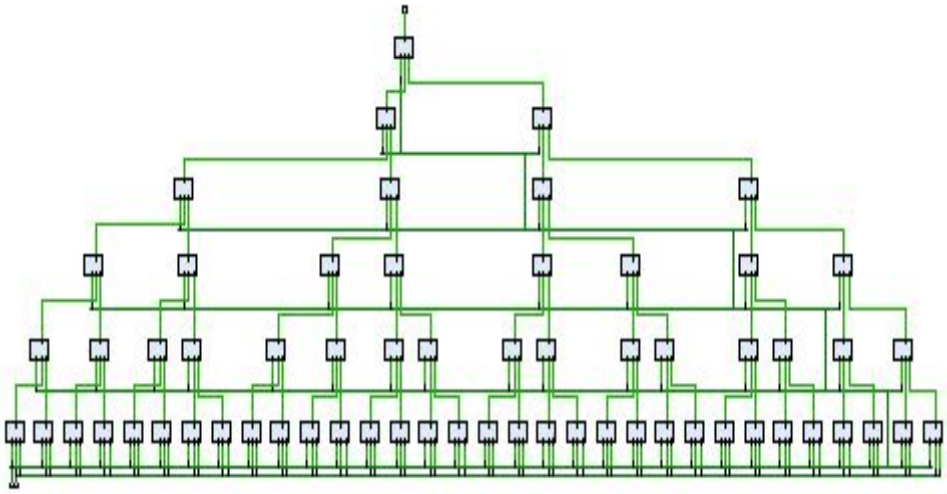


Fig. 1.2 - Vivado Elaborated Design

Trick of the Codes

The trick of the codes for the design implementation was to ensure that we used for-generate loops in order to produce our sets of generic 2x1 mux in order to create our 64x1 mux. To do this, we used a for loop for each power of 2 in the cascading mux's. For each bracket: 32, 16, 8, 4, 2, 1, we needed to use a for-generate loop and port map so we could utilize and create many sets of generic 2x1 mux. This implementation was super simple as we only needed to change minimal values in each for loop to correctly connect and implement each level of mux's. Overall the most difficult part of the code for our team was more so the syntax rather than the actual implementation of the design.

The testbench was also relatively simple to write after figuring out how to format txtio functions in VHDL. After specifying the variables for storing the lines, vectors, characters, and file paths, a simple while loop was written to take in the values from a file titled "input.txt", match them to the inputs on our 64x1 mux, and output the results to a file "output.txt". We formatted the input file to work so that if you wanted to turn on x1_0 you would type "00000001 00000000 000001" where the first 8 bits are x1(7 downto 0), the second are x0(7 downto 0), and the last digits are select(5 downto 0). The first two digits are input as hexadecimal and the last digit is input as binary since it is the select and 6 bits would allow us to choose from 1 to 64 (or 0 to 63).

Corner Cases

N/A

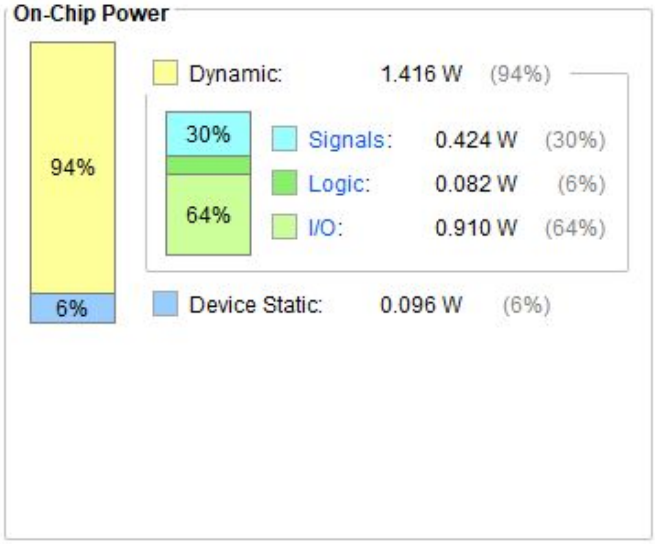
Pick the area/resources information from the tool

WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAM	URAM	DSP	Start	Elapsed
							4	0	0.0	0	0	2/8/21, 9:07 PM	00:00:29
NA	NA	NA	NA	NA	1.961	0	4	0	0.0	0	0	2/8/21, 9:08 PM	00:01:03

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**1.512 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**31.9°C**
Thermal Margin:	53.1°C (11.5 W)
Effective ϑJA:	4.6°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity



Hierarchical

Utilization	Name	Signals (W)	Data (W)	Logic (W)	I/O (W)
1.416 W (94% of total)	N_MUX2x1				
1.416 W (94% of total)	Leaf Cells (100)				

Data

Utilization	Name	Signal Rate (Mtr/s)	% High	Fanout	Slice Fanout	Clock	Logic Type
0.424 W (28% of total)	N_MUX2x1						
0.024 W (2% of total)	N2x1MUX_OUT_OBUF	49563.598	50.000	1	1	Dummy	N/A
0.009 W (1% of total)	N2x1MUX_SEL_IBUF[2]	12500.000	50.000	8	4	Dummy	N/A
0.009 W (1% of total)	N2x1MUX_X1_IBUF[30]	12500.000	50.000	1	1	Dummy	N/A
0.008 W (1% of total)	N2x1MUX_X1_IBUF[31]	12500.000	50.000	1	1	Dummy	N/A
0.008 W (1% of total)	N2x1MUX_X0_IBUF[0]	12500.000	50.000	1	1	Dummy	N/A
0.008 W (1% of total)	N2x1MUX_X1_IBUF[21]	12500.000	50.000	1	1	Dummy	N/A
0.008 W (1% of total)	N2x1MUX_SEL_IBUF[1]	12500.000	50.000	16	4	Dummy	N/A
0.008 W (1% of total)	N2x1MUX_X1_IBUF[27]	12500.000	50.000	1	1	Dummy	N/A

Logic

Utilization	Name	Type	Clock (MHz)	Clock Name	Signal Rate (Mtr/s)	% High
0.082 W (5% of total)	N_MUX2x1					
0.009 W (1% of total)	N2x1MUX_OUT_OBUF_inst_i_1 (LUT6)	LUT	N/A	Async	49563.598	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_21 (LUT6)	LUT	N/A	Async	25000.000	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_22 (LUT6)	LUT	N/A	Async	25000.000	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_23 (LUT6)	LUT	N/A	Async	25000.000	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_24 (LUT6)	LUT	N/A	Async	25000.000	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_25 (LUT6)	LUT	N/A	Async	25000.000	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_29 (LUT6)	LUT	N/A	Async	25000.000	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_14 (LUT6)	LUT	N/A	Async	24609.375	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_18 (LUT6)	LUT	N/A	Async	24609.375	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_19 (LUT6)	LUT	N/A	Async	24609.375	50.000
0.004 W (<1% of total)	N2x1MUX_OUT_OBUF_inst_i_28 (LUT6)	LUT	N/A	Async	24609.375	50.000

I/O

Estimated Calculated

Utilization	Name	I/O Type	I/O Standard	Drive Strength	Input Pins	Output Pins	Bidir Pins	IO LOGIC SERDES	IO DELAY	IBUF LOW PWR	Input Term	Output Impedance	Clock
0.91 W (60% of total)	N_MUX2x1												
0.63 W (42% of total)	N2x1MUX_OUT	HR	LVCMOS18	12.000	0	1	0	No	Off	No	NONE	RDRV_NONE_NONE	N/A
0.128 W (8% of total)	N2x1MUX_X0	HR	LVCMOS18	N/A	32	0	0	No	Off	No	RTT_NONE	NONE	N/A
0.128 W (8% of total)	N2x1MUX_X1	HR	LVCMOS18	N/A	32	0	0	No	Off	No	RTT_NONE	NONE	N/A
0.024 W (2% of total)	N2x1MUX_SEL	HR	LVCMOS18	N/A	6	0	0	No	Off	No	RTT_NONE	NONE	N/A