California Polytechnic State University, Pomona

ECE 4304.01
Lab 3

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2/24/21

Architecture

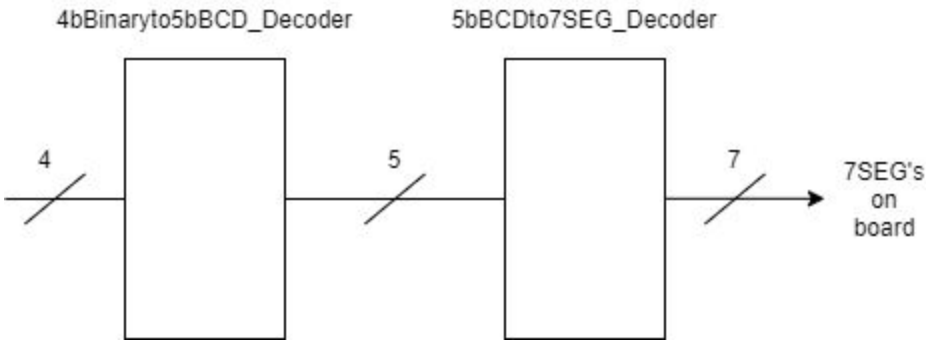

Fig. 3.1 - Initial Design

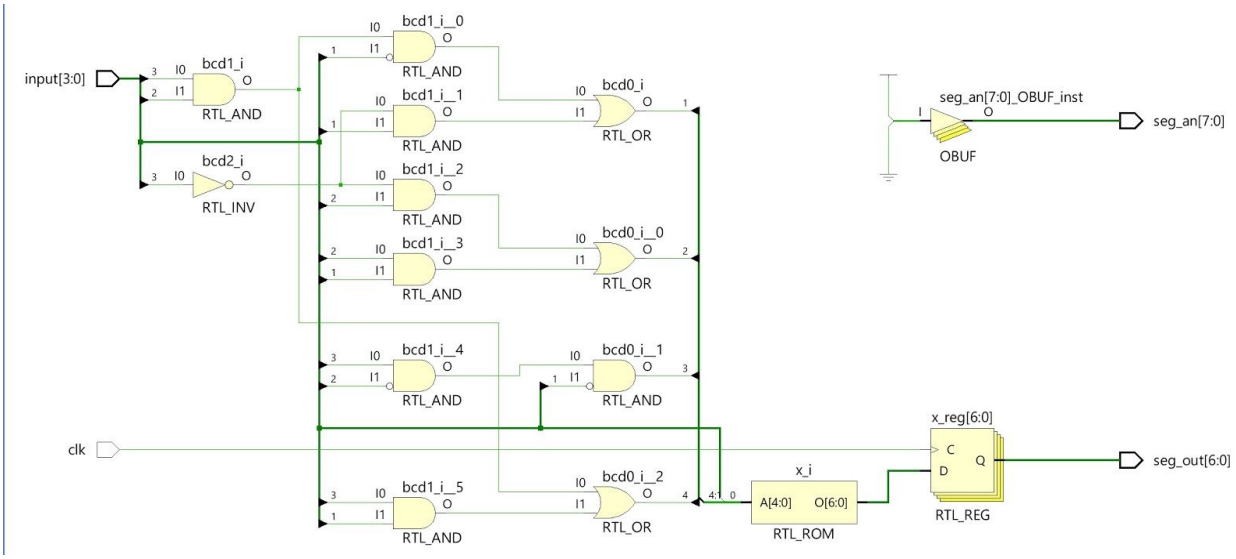

Fig 3.2 - Elaborated Design

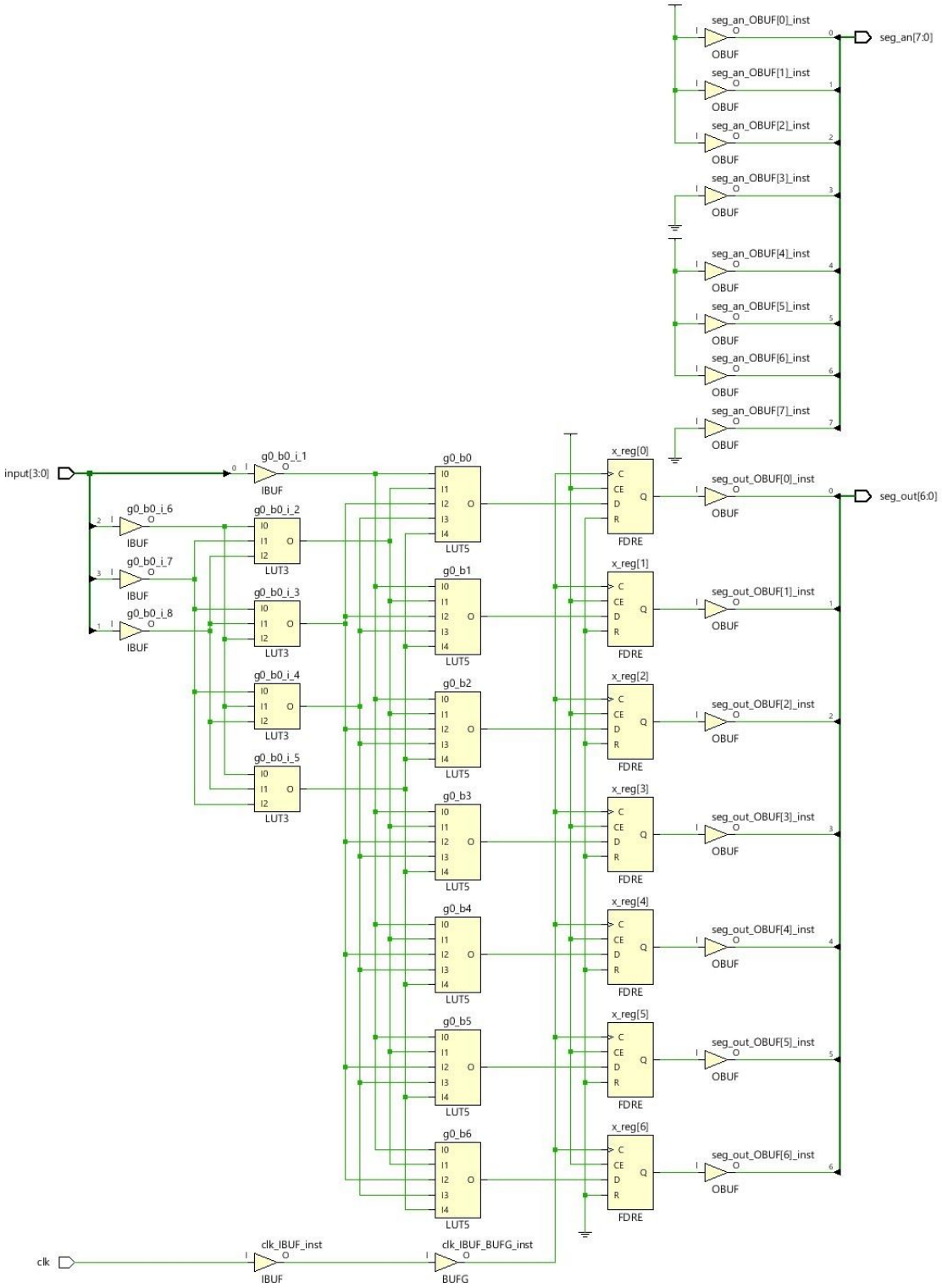

Fig. 3.3 - Implemented Design

Trick of the Codes

There wasn't really anything too tricky about the code for this lab. The only parts that took some thought were the derivation of the logic equations for the 4 bit binary to 5 bit BCD decoder as well as the "pinout" for the seven segment. After figuring those two things out, we simply implemented them as processes in VHDL and wrote the testbench to verify that our code worked as intended. A new addition to the labs included the usage of the clock to verify our input processes, but this was derived from previous 3300 experience so this was not of much difficulty aside from small syntax changes. Aside from that, everything is previous knowledge being applied in the new language/syntax of VHDL which is a trick in itself.

Corner Cases

N/A

Pick the area/resources information from the tool

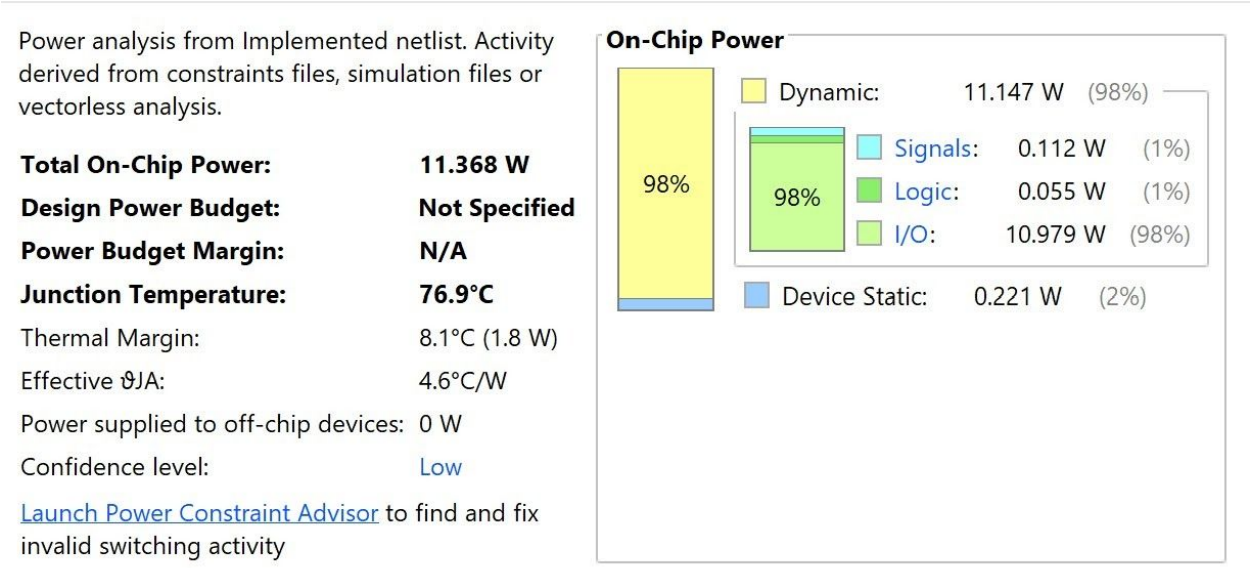

Figure 3.4 - On-Chip Power