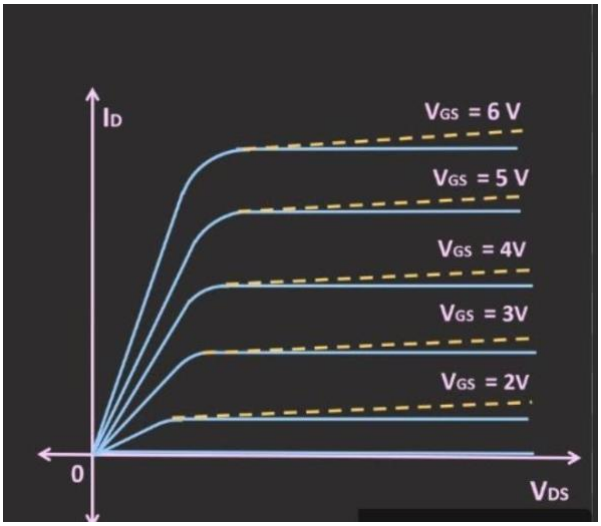
1. **How do wet oxidation and dry oxidation differ from each other, including their respective chemical equations- 3 marks** 1. **Oxidizing Agent**:
    - **Dry Oxidation**: Uses pure oxygen (O_2) as the oxidizing agent. **Chemical Equation**: Si+O2→SiO2
    - **Wet Oxidation**: Uses water vapor (H_2O) as the oxidizing agent. **Chemical Equation**: Si+2H2O→SiO2 + 2H2
2. **Oxidation Rate**:
    - Wet oxidation is **faster** because H_2O diffuses more readily through SiO_2 than O_2.
    - Dry oxidation is **slower** but produces higher-quality oxide with better electrical properties.
3. **Applications**:
    - **Dry Oxidation**: Used for thin, high-quality oxide layers (e.g., gate oxides in MOSFETs).
    - **Wet Oxidation**: Used for thicker oxide layers (e.g., masking layers or field oxides).
4. **Temperature Dependence:**
    - Wet oxidation can achieve usable growth rates at lower temperatures compared to dry oxidation.
    - Dry oxidation typically requires higher temperatures for reasonable growth rates.

2.How does channel length modulation influence the saturation drain current? 2 marks

Reduction in Effective Channel Length:

- In saturation, the channel pinches off near the drain, but the depletion region extends further with increasing V_DS, effectively shortening the channel (ΔL).
- This reduces the resistance of the channel, causing I_Dsat to **increase slightly with V_DS** instead of remaining constant.



3.describe the photolithography process flow with reference to various types of photoresists. 5 marks

1. **Substrate Preparation & Photoresist Coating**

- Wafer cleaning followed by spin-coating of **positive resist** (solubilizes on exposure) or **negative resist** (hardens on exposure).

2. **Soft Baking & UV Exposure**
    - Pre-bake (~100°C) removes solvents; UV light exposes resist through a photomask (positive: exposed areas dissolve, negative: unexposed dissolve).
3. **Development**
    - Chemical developer removes soluble regions, transferring mask pattern to resist (positive: exposed removed, negative: unexposed removed).
4. **Hard Baking & Pattern Transfer**
    - Post-bake (~120°C) strengthens resist for etching/doping; resist acts as a protective mask.
5. **Resist Stripping**
    - Removal of resist using solvents/plasma, completing the lithography cycle.

Photoresist Types:

- **Positive** (e.g., DNQ-Novolac): High resolution for ICs.
- **Negative** (e.g., SU-8): Thick films for MEMS.

4. describe the voltage transfer characteristics of a cmos inverter circuit. 5 marks

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$> (V_{DD} + V_{T0,p})$	V_{OL}	linear	cut-off

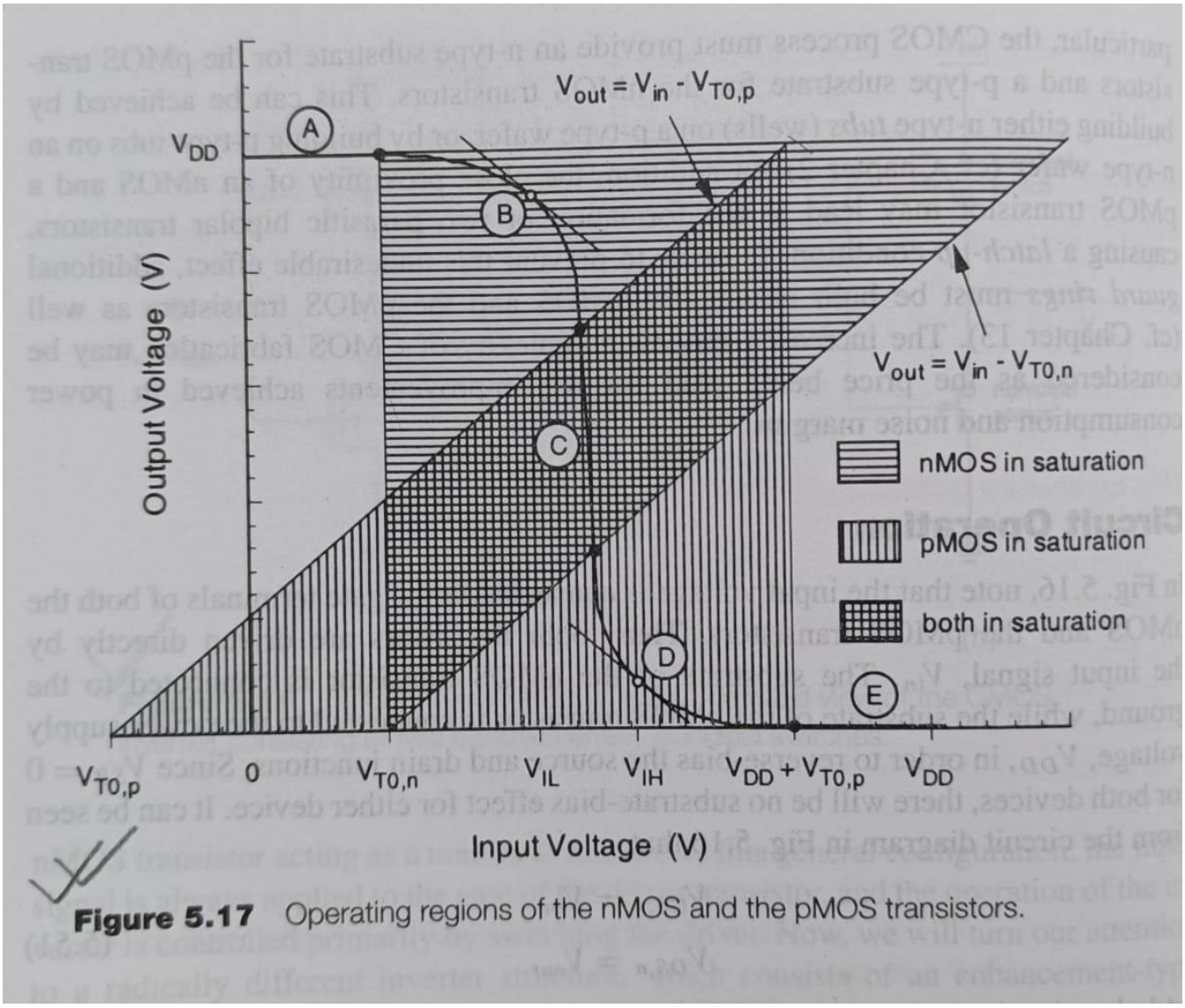


Figure 5.17 Operating regions of the nMOS and the pMOS transistors.

6. Discuss the y chart along with the overall vlsi design flow. 10 marks

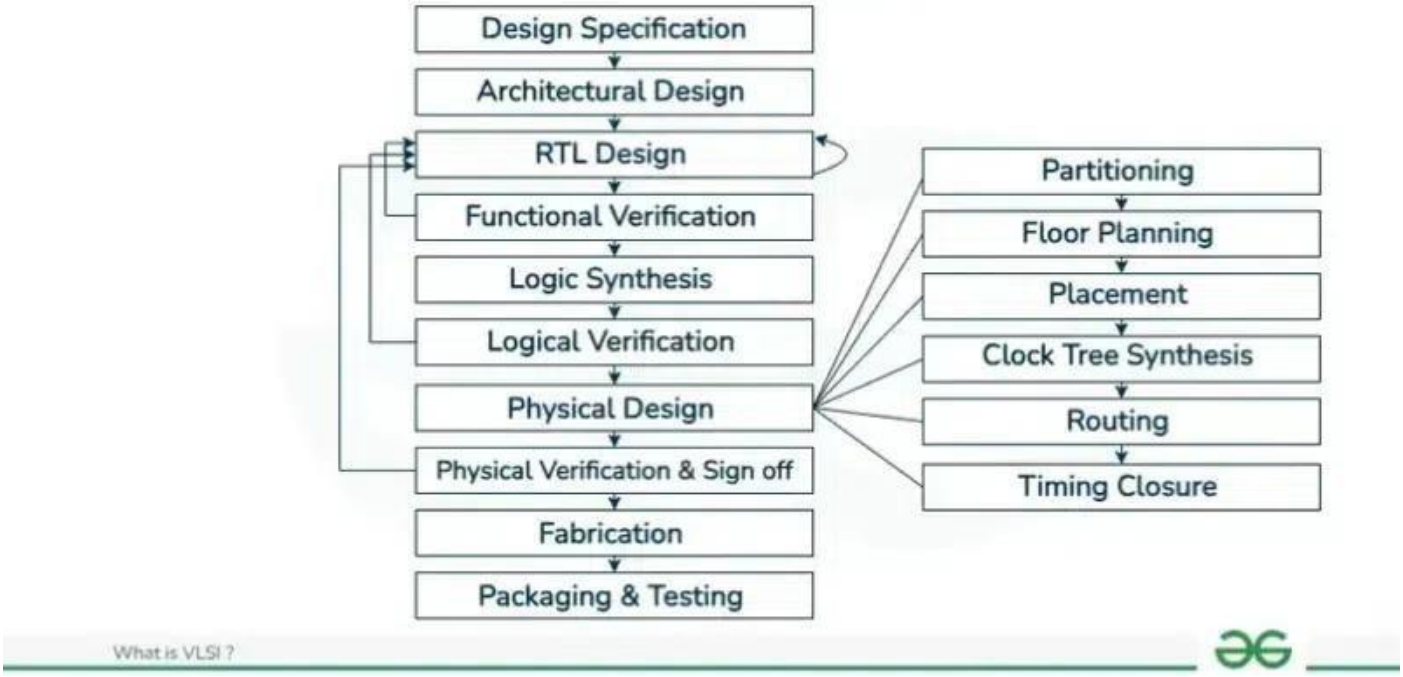
Y-Chart (Gajski–Kuhn Y-Chart):

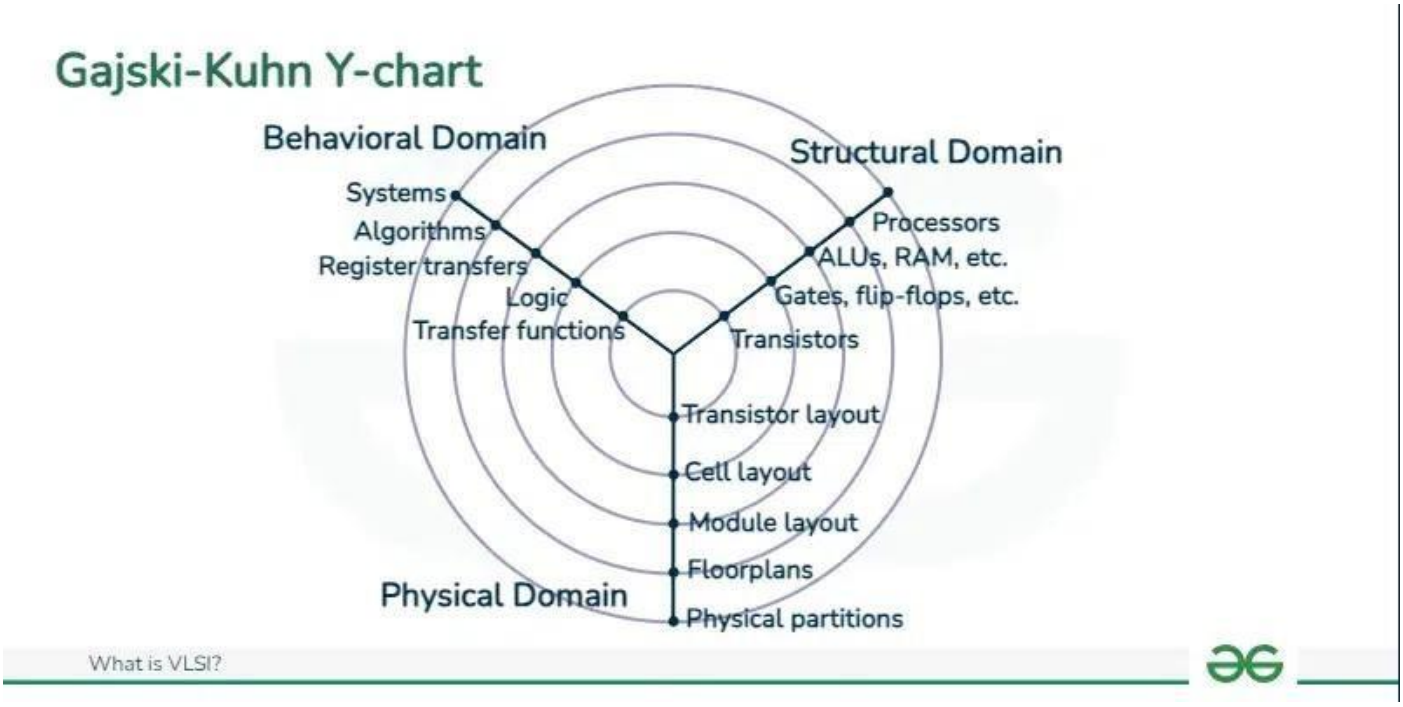
- The Y-Chart is a model for VLSI design representation.
- It has three axes representing different domains of design:
    1. Behavioural Domain: Describes *what the system does* (functions, algorithms, HDL code).
    2. Structural Domain: Describes *how the system is built* (logic gates, modules, interconnections).
    3. Physical Domain: Describes the *geometric layout* (placement, routing, masks).
- Each axis has levels of abstraction: system → logic → circuit → layout.
- Designers move around the Y to refine from high-level description down to the physical chip.

Overall VLSI Design Flow:

1. Specification: Define system requirements (function, performance, cost).
2. Behavioural/RTL Design: Describe functionality in HDL (VHDL/Verilog).
3. Functional Verification: Check correctness via simulation.

4. Logic Synthesis: Convert RTL into gate-level netlist.
5. Design for Testability (DFT): Add scan chains, BIST, etc.
6. Floorplanning & Placement: Decide chip area and block positions.
7. Routing: Connect components physically.
8. Timing Analysis & Optimization: Ensure performance, remove violations.
9. Physical Verification: DRC (Design Rule Check), LVS (Layout vs Schematic).
10. Fabrication & Testing: Send final layout (GDSII) to foundry → manufactured chip → tested.





7.Obtain the expression for the resistance of a mosfet in the deep trode region. 10 marks

Expression for MOSFET Resistance in the Triode (Linear) Region (10 Marks)

1. Assumptions & Operating Conditions

- **Triode (Linear) Region Condition:**
  $V_{DS} < V_{GS} - V_{th}$ (Drain-Source voltage is small).
- **MOSFET acts as a voltage-controlled resistor.**
- **Channel is fully formed** (no pinch-off).

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2. Drain Current (I_D) in Triode Region

The drain current in the triode region is given by:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Where:

- μ_n = Electron mobility
- C_{ox} = Oxide capacitance per unit area
- W/L = Width-to-length ratio
- V_{GS} = Gate-Source voltage
- V_{th} = Threshold voltage
- V_{DS} = Drain-Source voltage

---

3. Small-Signal Resistance Approximation

For **very small V_{DS} (Deep Triode Region)**, the quadratic term $\frac{V_{DS}^2}{2}$ becomes negligible. Thus:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS}$$

4. MOSFET Resistance (R_{on})

The **on-resistance** (R_{on}) is defined as:

$$R_{on} = \frac{V_{DS}}{I_D}$$

Substituting I_D from the simplified triode equation:

$$R_{on} = \frac{V_{DS}}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) V_{DS}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})}$$

Final Expression:

$$\boxed{R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})}}$$