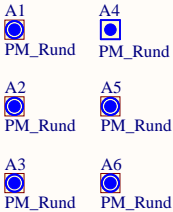
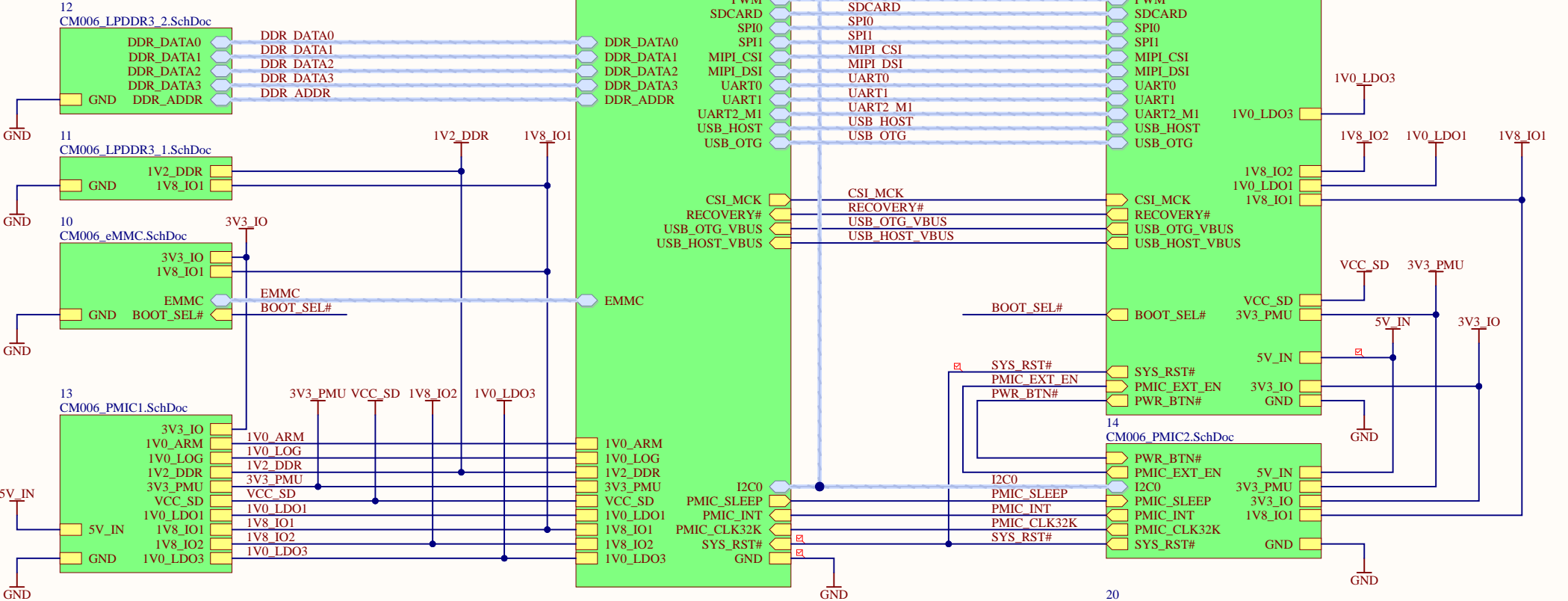



OSM Module Size-S

SOC: Rockchip PX30(K)  
OSM Interface based on Spec. REV1.0  
<https://sget.org/>



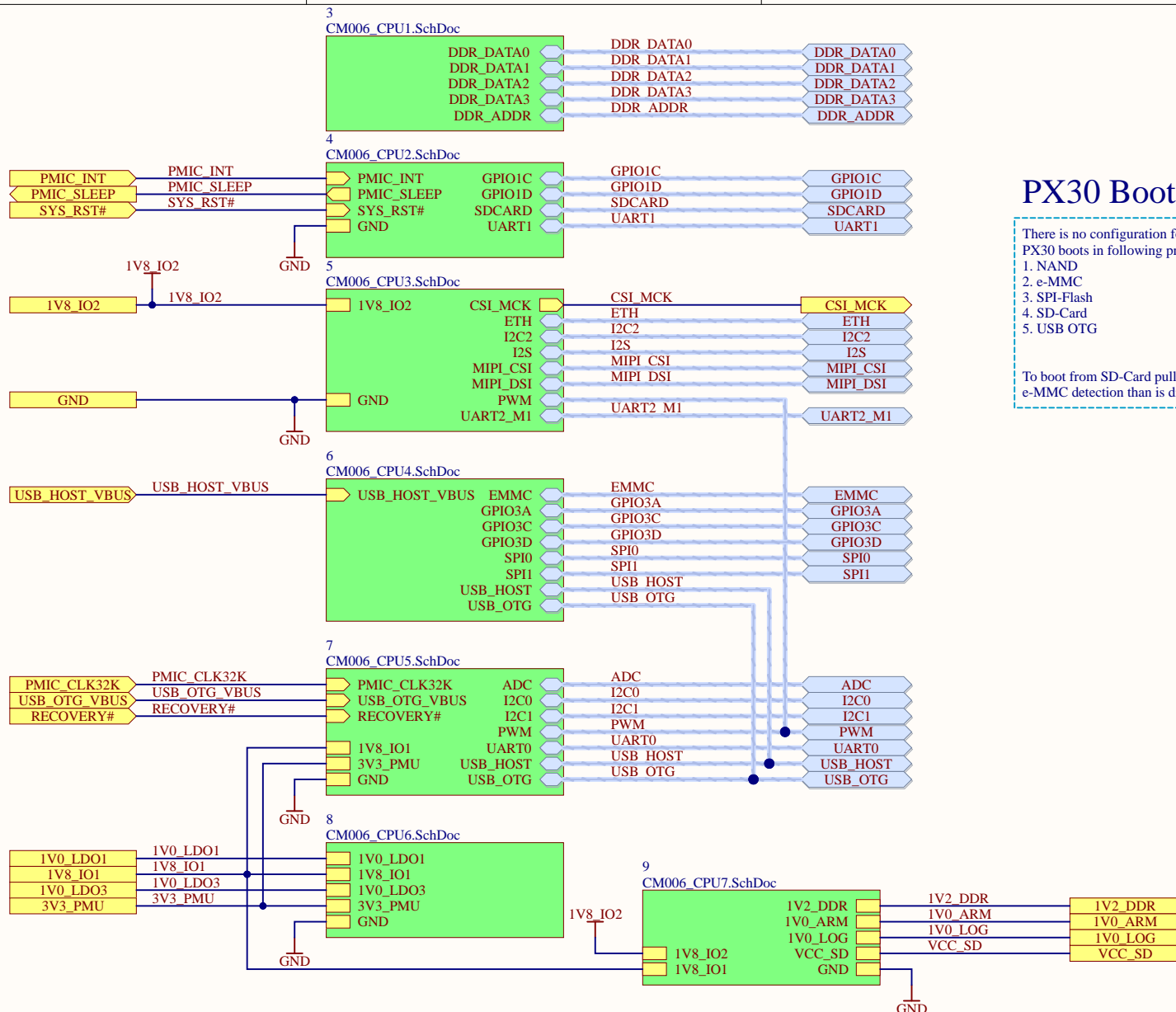
	Datum	Name	Art. Nr. 20.0010.1208	<div><i>CM006 (iesy PX30 OSM-SF)</i></div> <div><i>CM006a</i></div> <div><i>CM006_TOP.SchDoc</i></div>	17.09.2021	REV.: 1.00
Bearb.	11.12.2020	MAS			<div><i>88892 - SL (4)</i></div> <div><i>TOP Sheet</i></div>	LK: 02.0500.0759
CAD:	13.08.2021	FIN				Blatt-Nr: 1
Prüfer:	09.07.2021	YAG				von: 20

A

B

C

D



## PX30 Boot Priority

There is no configuration for boot selection of PX30.  
PX30 boots in following priority depending on connected device:

1. NAND
2. e-MMC
3. SPI-Flash
4. SD-Card
5. USB OTG

To boot from SD-Card pull BOOT\_SEL# low on carrier.  
e-MMC detection than is disabled by pulling low DATA0.

	Datum	Name	Art. Nr.
	11.12.2020	MAS	20.0010.1208
Bearb.	13.08.2021	FIN	
CAD:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)  
CM006a  
CM006\_CPU\_TOP.SchDoc

16.09.2021

REV.: 1.00

88892 - SL (4)  
PX30 TOP Sheet

LK: 02.0500.0759  
Blatt-Nr: 2  
von: 20

IC1A

DDR\_IO

DDR\_DQS0\_P  
DDR\_DQS0\_N

DDR\_DM0

DDR\_DQ0  
DDR\_DQ1  
DDR\_DQ2  
DDR\_DQ3  
DDR\_DQ4  
DDR\_DQ5  
DDR\_DQ6  
DDR\_DQ7DDR\_DQS1\_P  
DDR\_DQS1\_N

DDR\_DM1

DDR\_DQ8  
DDR\_DQ9  
DDR\_DQ10  
DDR\_DQ11  
DDR\_DQ12  
DDR\_DQ13  
DDR\_DQ14  
DDR\_DQ15DDR\_DQS2\_P  
DDR\_DQS2\_N

DDR\_DM2

DDR\_DQ16  
DDR\_DQ17  
DDR\_DQ18  
DDR\_DQ19  
DDR\_DQ20  
DDR\_DQ21  
DDR\_DQ22  
DDR\_DQ23DDR\_DQS3\_P  
DDR\_DQS3\_N

DDR\_DM3

DDR\_DQ24  
DDR\_DQ25  
DDR\_DQ26  
DDR\_DQ27  
DDR\_DQ28  
DDR\_DQ29  
DDR\_DQ30  
DDR\_DQ31W2 DDR\_DATA0.DQS\_P DIFF 100  
W1 DDR\_DATA0.DQS\_N DIFF 100T2 SINGLE\_50  
△DDR\_DATA0.DMR4 DDR\_DATA0.DQ0  
R1 DDR\_DATA0.DQ1  
U3 DDR\_DATA0.DQ2  
Y2 DDR\_DATA0.DQ3  
N2 DDR\_DATA0.DQ4  
R3 DDR\_DATA0.DQ5  
R2 DDR\_DATA0.DQ6  
Y1 DDR\_DATA0.DQ7

DDR\_DATA0

U2 DDR\_DATA1.DQS\_P DIFF 100  
U1 DDR\_DATA1.DQS\_N DIFF 100U4 SINGLE\_50  
△DDR\_DATA1.DMAA2 DDR\_DATA1.DQ0  
P3 DDR\_DATA1.DQ1  
Y3 DDR\_DATA1.DQ2  
M2 DDR\_DATA1.DQ3  
V4 DDR\_DATA1.DQ4  
M3 DDR\_DATA1.DQ5  
V3 DDR\_DATA1.DQ6  
N4 DDR\_DATA1.DQ7

DDR\_DATA1

J2 DDR\_DATA2.DQS\_P DIFF 100  
J1 DDR\_DATA2.DQS\_N DIFF 100G4 SINGLE\_50  
△DDR\_DATA2.DMF4 DDR\_DATA2.DQ0  
G3 DDR\_DATA2.DQ1  
F3 DDR\_DATA2.DQ2  
K2 DDR\_DATA2.DQ3  
L2 DDR\_DATA2.DQ4  
M1 DDR\_DATA2.DQ5  
E2 DDR\_DATA2.DQ6  
L1 DDR\_DATA2.DQ7

DDR\_DATA2

G2 DDR\_DATA3.DQS\_P DIFF 100  
G1 DDR\_DATA3.DQS\_N DIFF 100M4 SINGLE\_50  
△DDR\_DATA3.DMK3 DDR\_DATA3.DQ0  
J4 DDR\_DATA3.DQ1  
C2 DDR\_DATA3.DQ2  
D2 DDR\_DATA3.DQ3  
K4 DDR\_DATA3.DQ4  
J3 DDR\_DATA3.DQ5  
D1 DDR\_DATA3.DQ6  
E1 DDR\_DATA3.DQ7

DDR\_DATA3

PX30K

IC1B

DDR\_IO

DDR3\_A0/DDR4\_A10  
DDR3\_A1/DDR4\_A9  
DDR3\_A2/DDR4\_A4  
DDR3\_A3/DDR4\_A6  
DDR3\_A4/DDR4\_A5  
DDR3\_A5/DDR4\_A8  
DDR3\_A6/DDR4\_A7  
DDR3\_A7/DDR4\_A11  
DDR3\_A8/DDR4\_A13  
DDR3\_A9/DDR4\_A0  
DDR3\_A10/DDR4\_CS0n  
DDR3\_A11/DDR4\_A3  
DDR3\_A12/DDR4\_BA1  
DDR3\_A13/DDR4\_A2  
DDR3\_A14/DDR4\_A1  
DDR3\_A15/DDR4\_ODT0DDR3\_BA0/DDR4\_BG0  
DDR3\_BA1/DDR4\_CASn/DDR4\_A15  
DDR3\_BA2/DDR4\_BA0  
DDR3\_CASn/DDR4\_A12  
DDR3\_RASn/DDR4\_CKE  
DDR3\_CKE/DDR4\_RASn/DDR4\_A16  
DDR3\_CSN0/DDR4\_ACTn  
DDR3\_CSN1/DDR4\_CS1N  
DDR3\_ODT0/DDR4\_WEn/DDR4\_A14  
DDR3\_ODT1/DDR4\_ODT1  
DDR3\_WEn/DDR4\_BG1DDR3\_CLKN/DDR4\_CLKN  
DDR3\_CLKP/DDR4\_CLKP

DDR3\_RESEtN/DDR4\_RESEtN

PX30K

C7 SINGLE\_50  
△DDR\_ADDR.CA0  
D10 DDR\_ADDR.CA1  
D8 DDR\_ADDR.CA2  
B5 DDR\_ADDR.CA3  
A8 DDR\_ADDR.CA4  
A4 DDR\_ADDR.CA5  
B8 DDR\_ADDR.CA6  
B4 DDR\_ADDR.CA7  
C10 DDR\_ADDR.CA8  
C6 DDR\_ADDR.CA9A10  
B7  
A9  
D6  
A7  
C9A3  
B10  
A5  
D9  
C4B11 SINGLE\_50  
△DDR\_ADDR.CKE0  
B3 DDR\_ADDR.CS0#  
D11 DDR\_ADDR.CS1#  
D5 DDR\_ADDR.ODTC11  
C8B1 DDR\_ADDR.CK\_N DIFF 100  
B2 DDR\_ADDR.CK\_P DIFF 100

A2

DDR\_ADDR

Datum Name Art. Nr. 20.0010.1208

Bearb. 11.12.2020 MAS

CAD: 13.08.2021 FIN

Prüfer: 09.07.2021 YAG



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_CPU1.SchDoc

16.09.2021

REV.: 1.00

88892 - SL (4)

PX30 Sheet 1

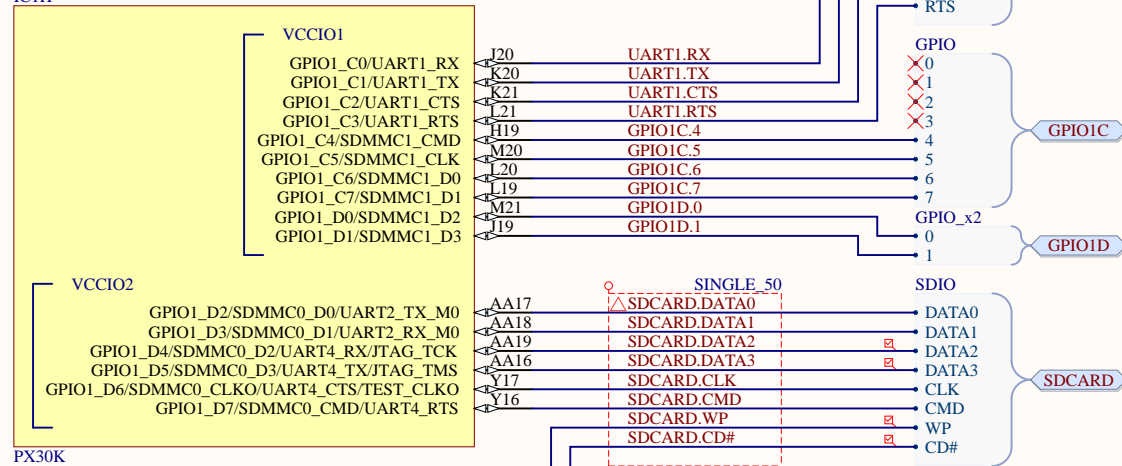
LK: 02.0500.0759

Blatt-Nr: 3

von: 20

A

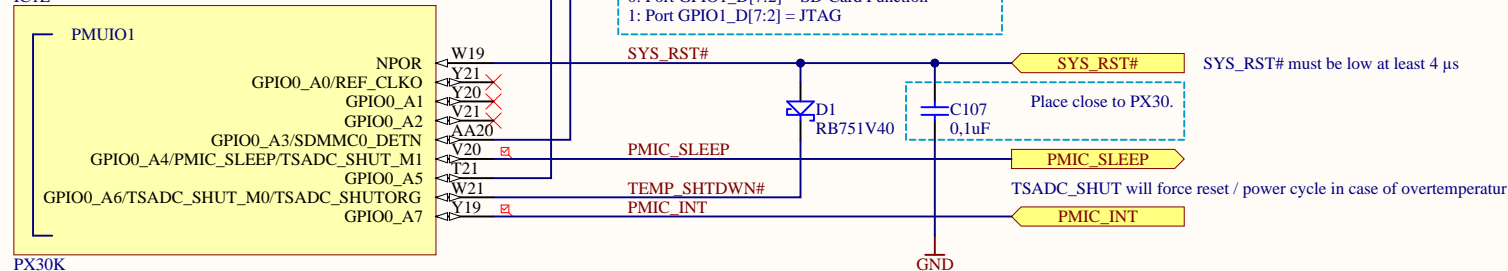
IC1H



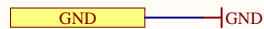
B

C

IC1E



D



	Datum	Name	Art. Nr.
			20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_CPU2.SchDoc

16.09.2021

REV.: 1.00

88892 - SL (4)

PX30 Sheet 2

LK: 02.0500.0759

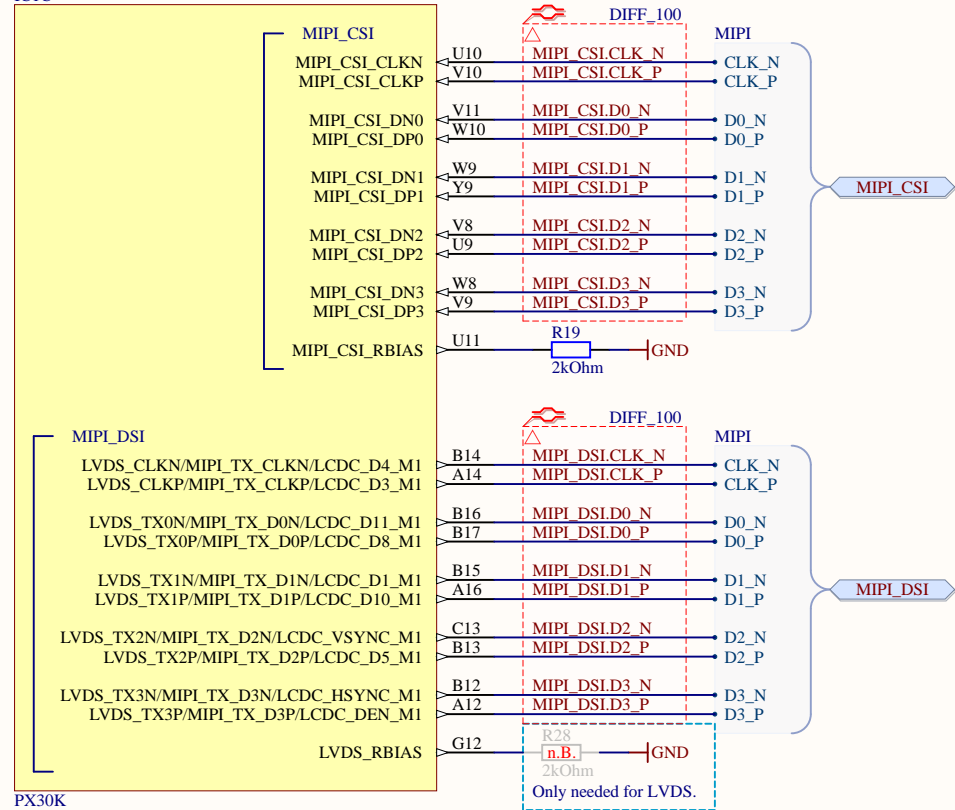
Blatt-Nr: 4

von: 20

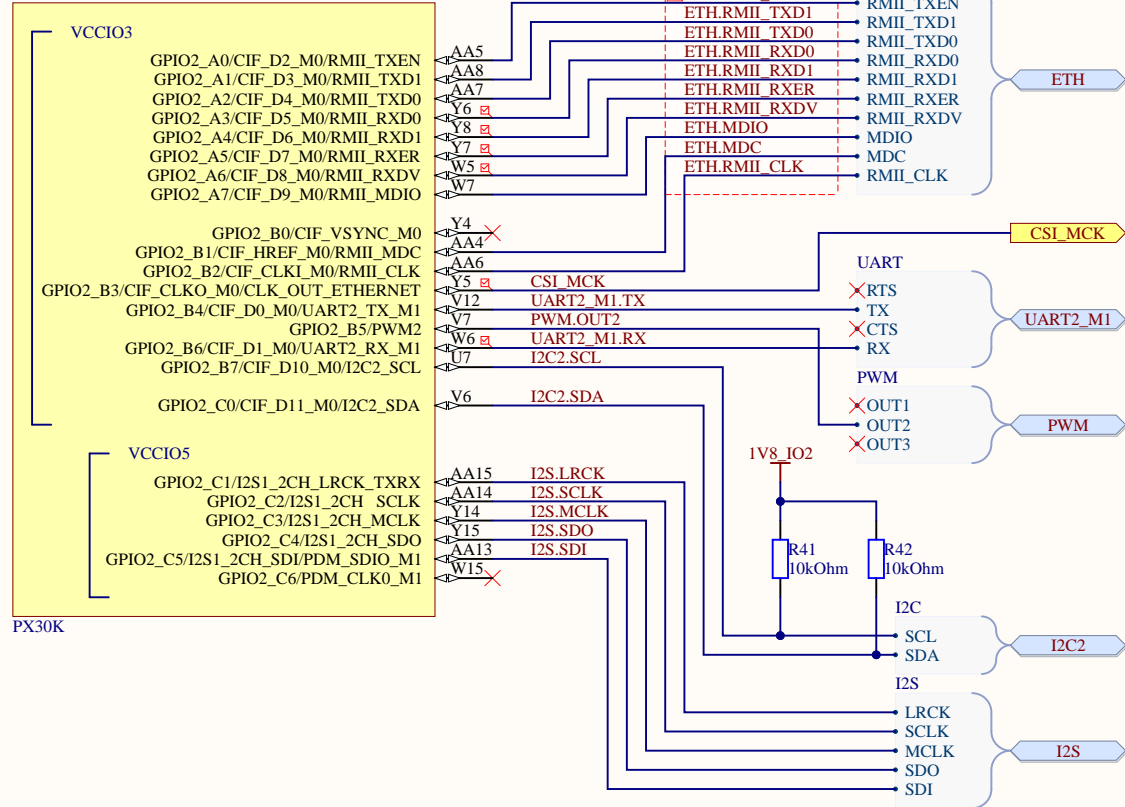
A

A

ICIC

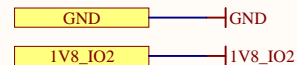


ICII



D

D



	Datum	Name	Art. Nr.
			20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)  
 CM006a  
 CM006\_CPU3.SchDoc

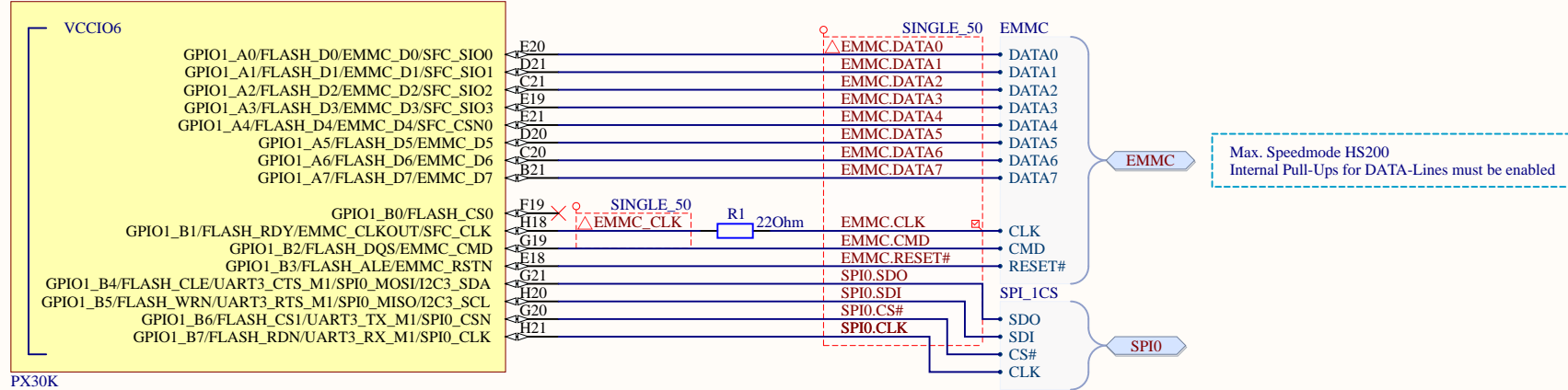
16.09.2021

REV.: 1.00

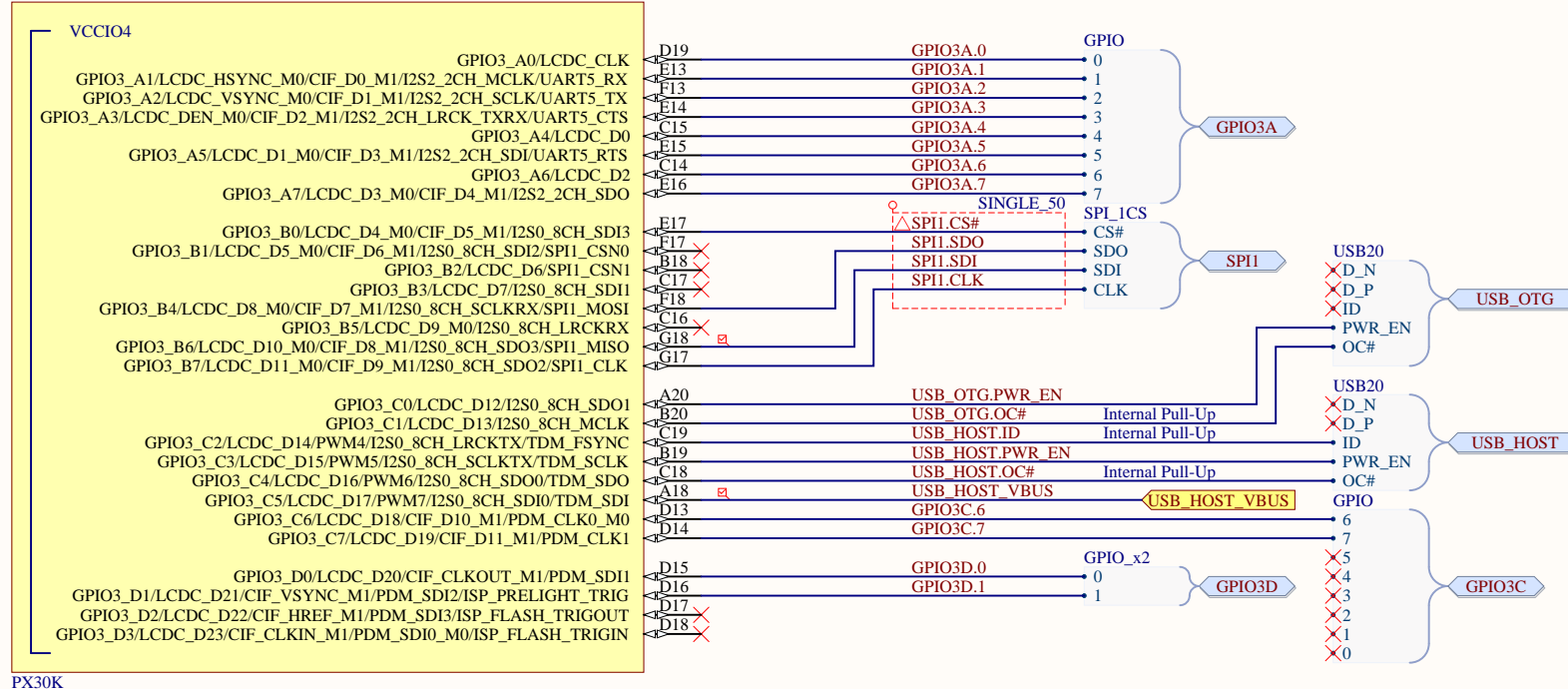
88892 - SL (4)  
 PX30 Sheet 3

LK: 02.0500.0759  
 Blatt-Nr: 5  
 von: 20

## IC1G



## IC1J



Datum	Name	Art. Nr.
Bearb.	11.12.2020	MAS
CAD:	13.08.2021	FIN
Prüfer:	09.07.2021	YAG



CM006 (iesy PX30 OSM-SF)  
CM006a  
CM006\_CPU4.SchDoc

16.09.2021

REV.: 1.00

88892 - SL (4)  
PX30 Sheet 4

LK: 02.0500.0759  
Blatt-Nr: 6  
von: 20

A

A

B

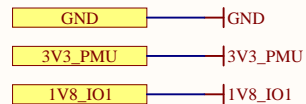
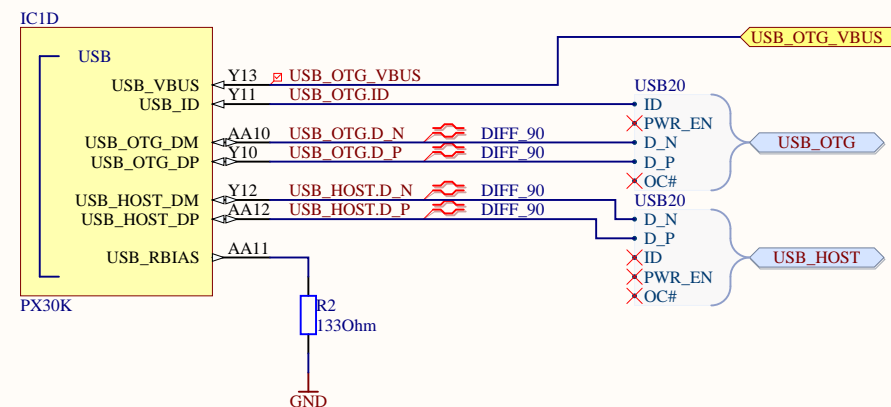
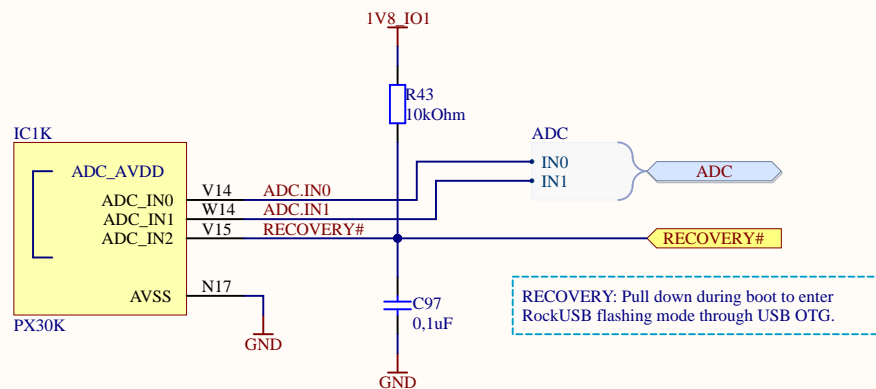
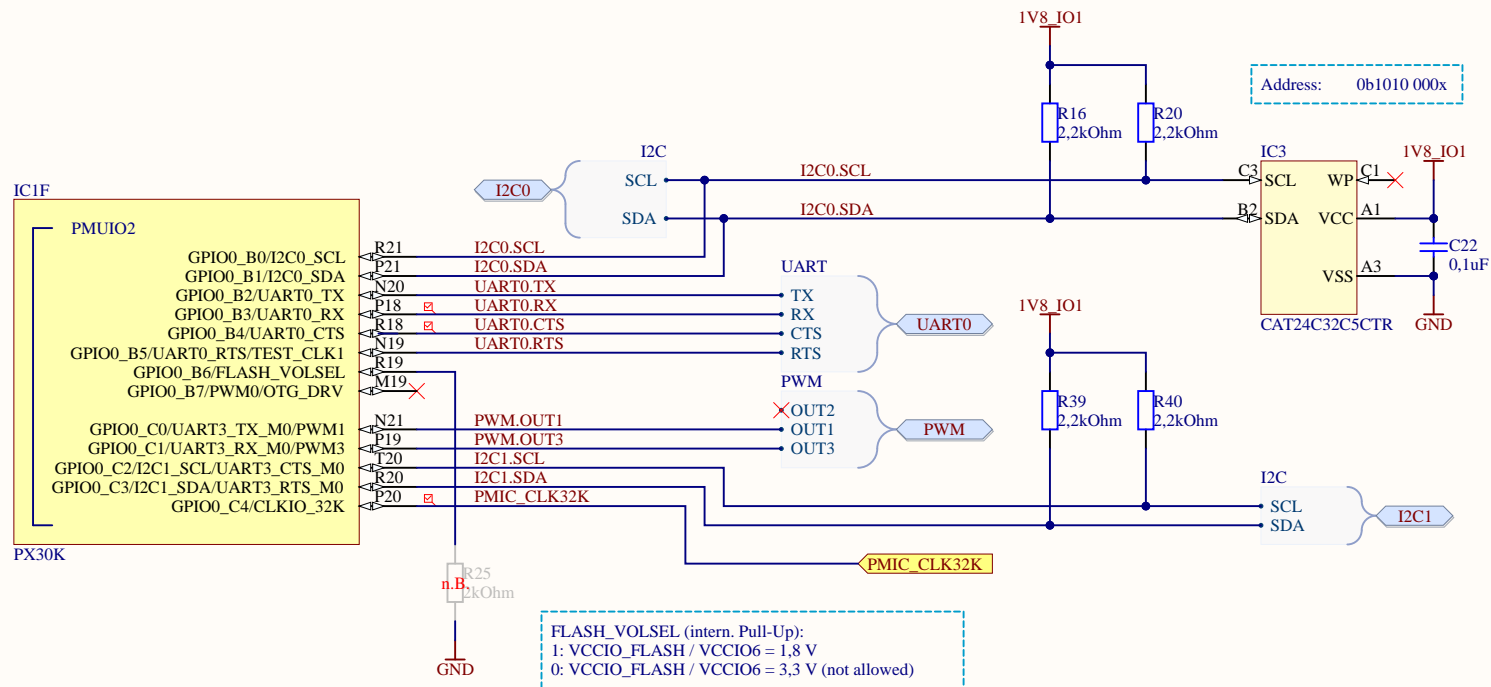
B

C

C

D

D



	Datum	Name	Art. Nr.
			20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)

**CM006a**

CM006\_CPU5.SchDoc

16.09.2021

REV.: 1.00

**88892 - SL (4)**

PX30 Sheet 5

LK: 02.0500.0759

Blatt-Nr: 7

von: 20



A

A

B

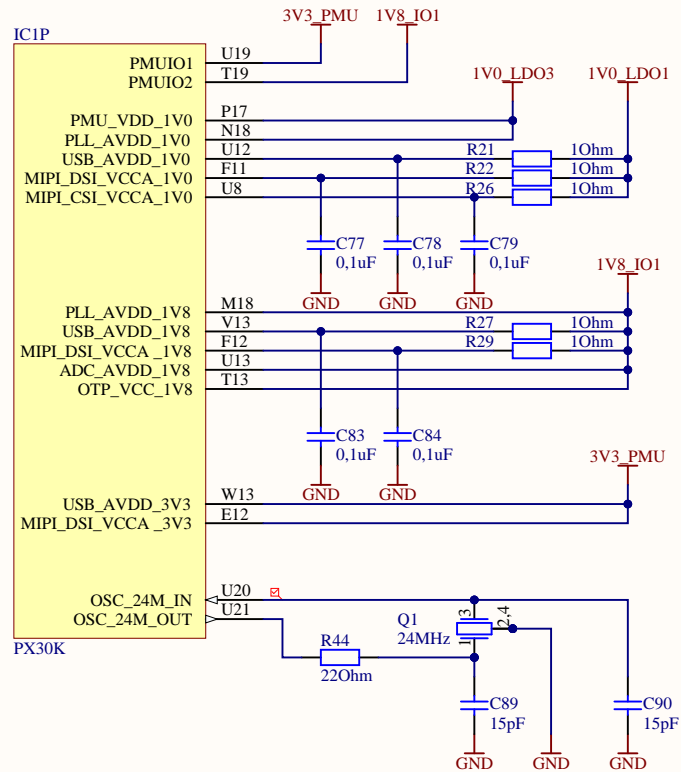
B

C

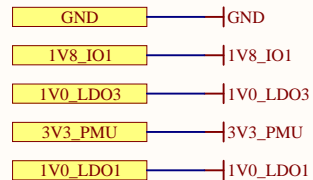
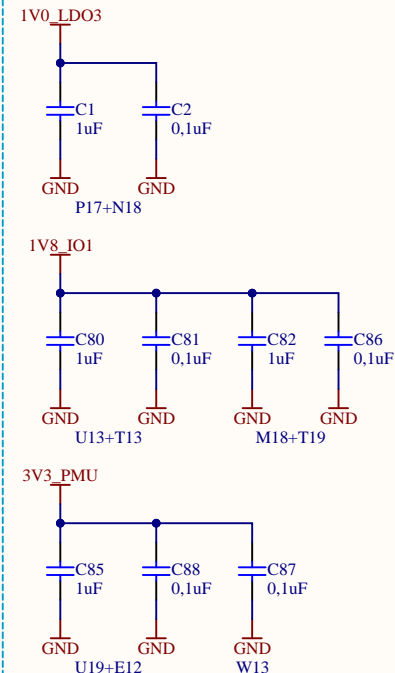
C

D

D



Place close to PX30.



	Datum	Name	Art. Nr. 20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_CPU6.SchDoc

17.09.2021

REV.: 1.00

88892 - SL (4)

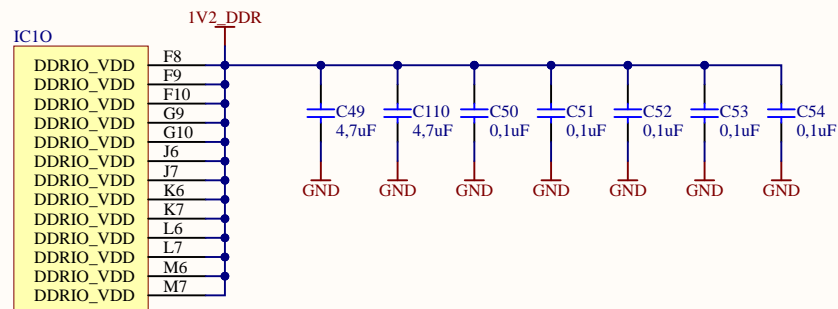
PX30 Sheet 6

LK: 02.0500.0759

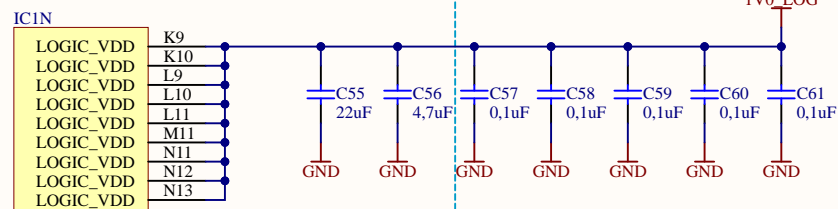
Blatt-Nr: 8

von: 20

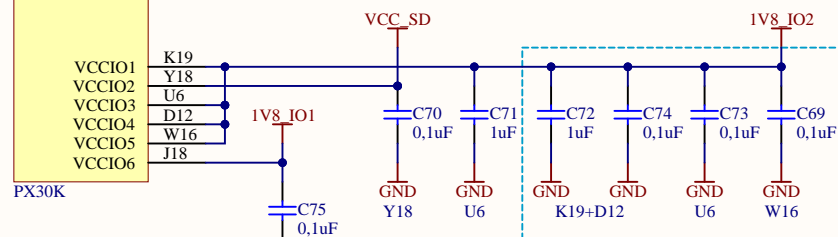
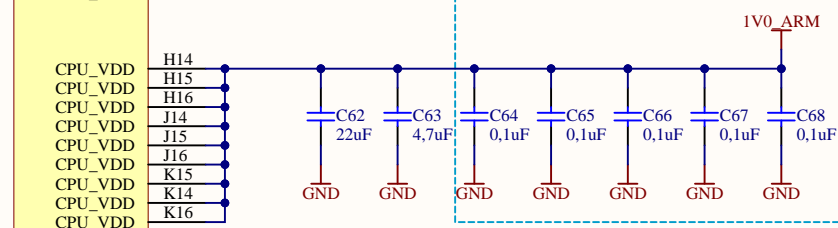




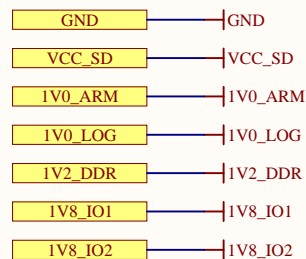
PX30K




Place close to PX30.



Place close to PX30.



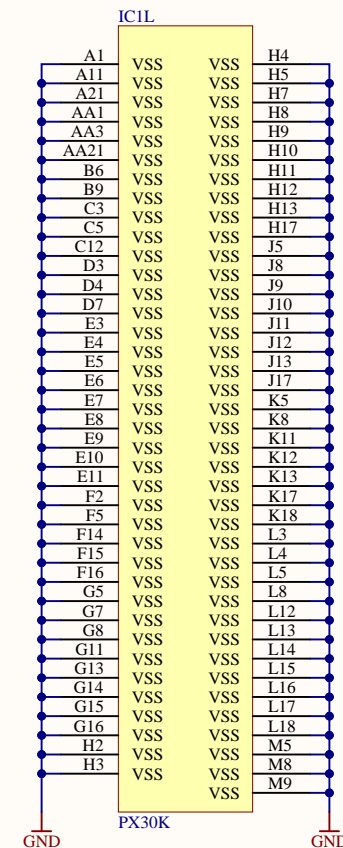
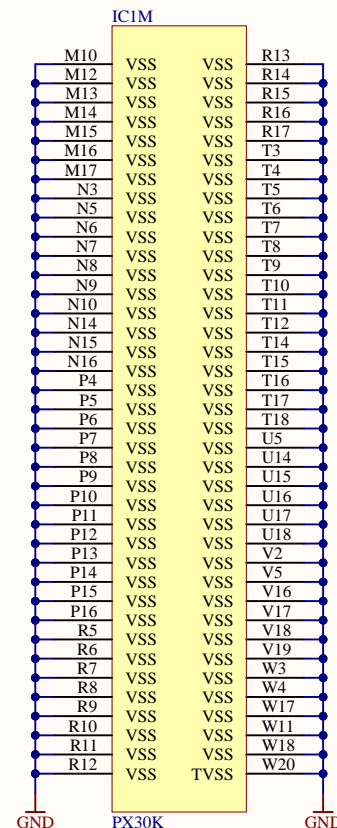
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Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_CPU7.SchDoc



16.09.2021	REV.: 1.00
<div> <div>88892 - SL (4)</div> <div>PX30 Sheet 7</div> </div>	LK: 02.0500.0759
	Blatt-Nr: 9
	von: 20

A

A

B

B

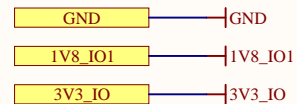
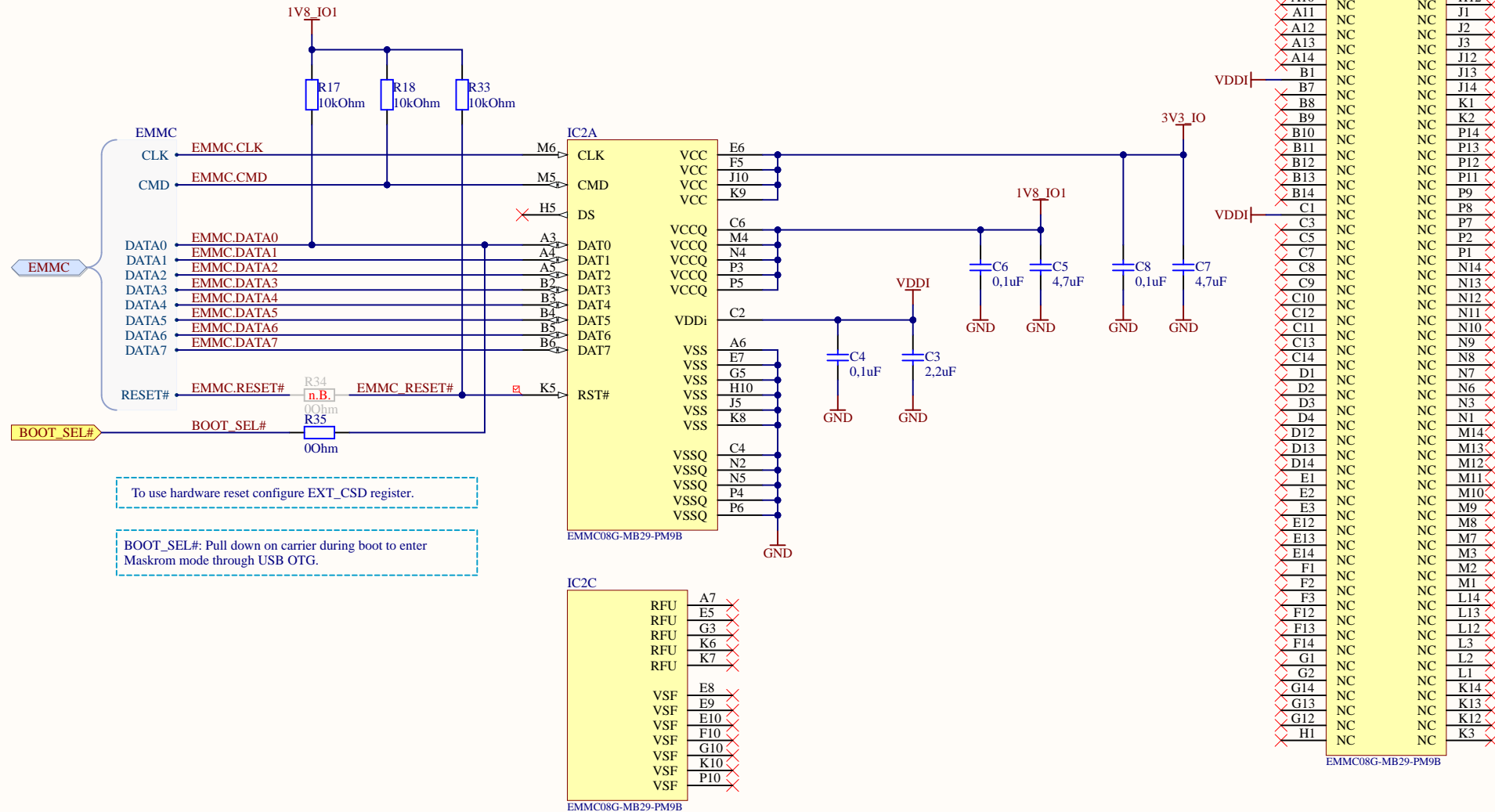
C

C

D

D

Usage of NC balls for easier routing is allowed for e-MMC.



	Datum	Name	Art. Nr.
			20.0010.1208
Bearb.	11.12.2020	MAS	
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Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_eMMC.SchDoc

16.09.2021

REV.: 1.00

88892 - SL (4)

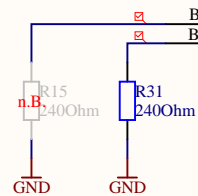
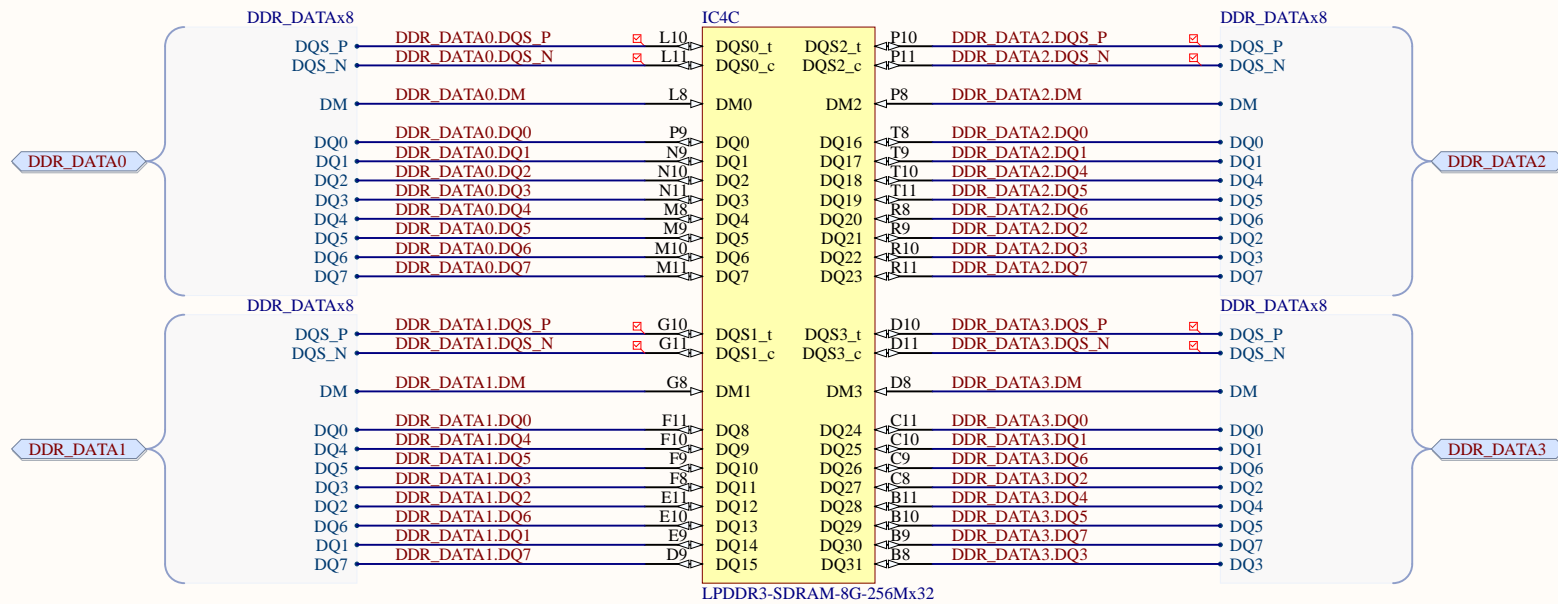
e-MMC 5.1 HS200

LK: 02.0500.0759

Blatt-Nr: 10

von: 20





GND

	Datum	Name	Art. Nr.
	11.12.2020	MAS	20.0010.1208
Bearb.	13.08.2021	FIN	
CAD:	09.07.2021	YAG	
Prüfer:			



CM006 (iesy PX30 OSM-SF)  
CM006a  
CM006\_LPDDR3\_2.SchDoc

16.09.2021

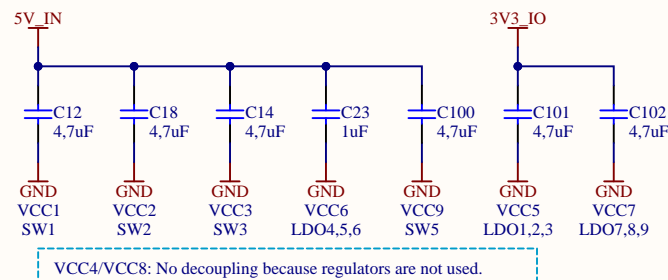
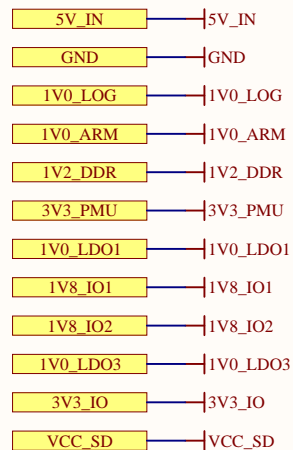
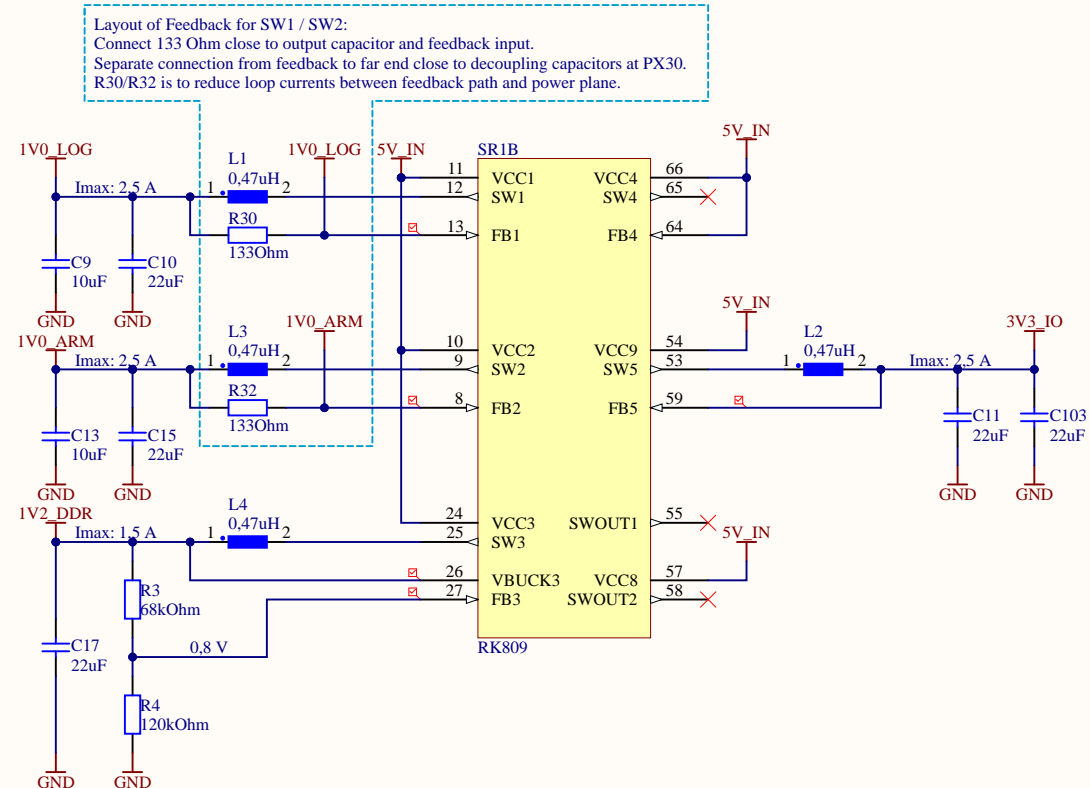
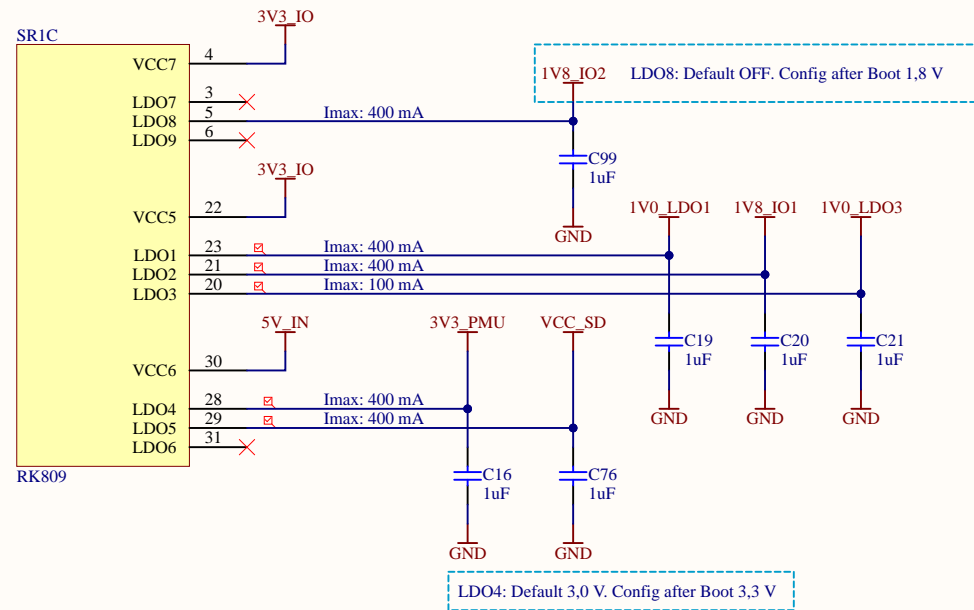
REV.: 1.00

88892 - SL (4)  
LPDDR3 Interface

LK: 02.0500.0759

Blatt-Nr: 12

von: 20



	Datum	Name	Art. Nr.
	11.12.2020	MAS	20.0010.1208
Bearb.	13.08.2021	FIN	
CAD:	09.07.2021	YAG	
Prüfer:			



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_PMIC1.SchDoc

16.09.2021

REV.: 1.00

88892 - SL (4)

PMIC Sheet 1

LK: 02.0500.0759

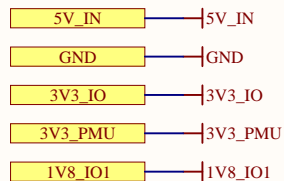
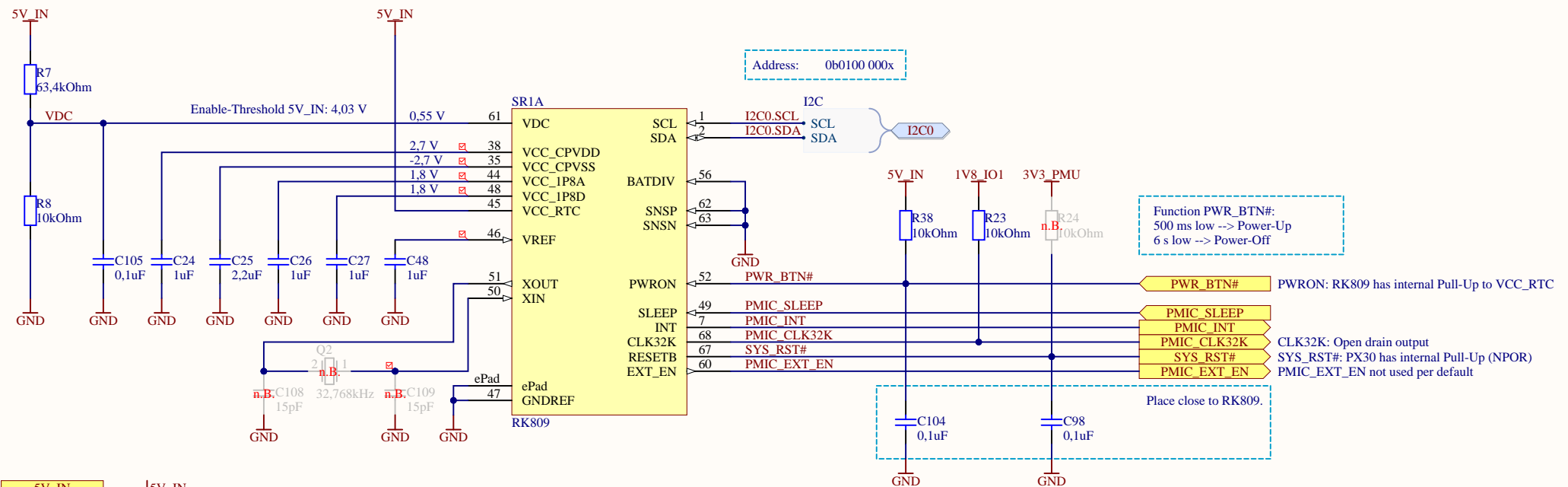
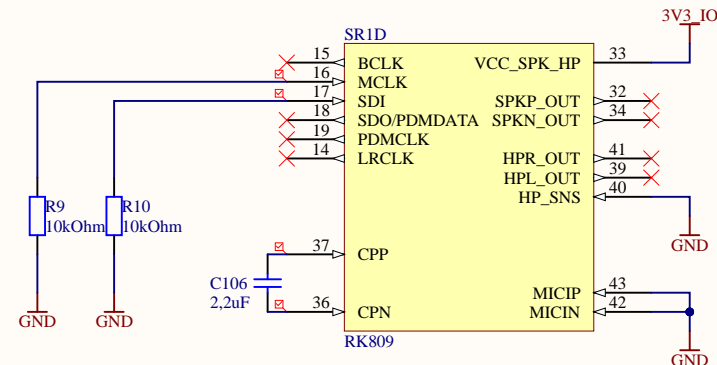
Blatt-Nr: 13


von: 20

## Power-Sequence

Trigger of sequene is PWRON button or rising edge of 5V\_IN (VDC)

SEQ n x 2 ms	Name	Startup- Voltage	Regulator	iesy Boot configuration
1	3V3_IO	3,3 V	BUCK5	Configured to 3,3 V during boot 1,8 V / 3,3 V depending on SD-Card not used; Switched off during boot not used; Switched off during boot
2	1V0_LOG	1,0 V	BUCK1	
2	1V0_ARM	1,0 V	BUCK2	
2	1V0_LDO3	1,0 V	LDO3	
3	1V0_LDO1	1,0 V	LDO1	
3	1V8_IO1	1,8 V	LDO2	
4	1V2_DDR	1,25 V	BUCK3	
5	3V3_PMU	3,0 V	LDO4	
5	VCC_SD	3,0 V	LDO5	
5	-	3,0 V	LDO6	
5	-	3,0 V	BUCK4	
11	SYS_RST#	-	-	Configured to 1,8 V during boot not used not used
SW	1V8_IO2	0 V	LDO8	
-	-	0 V	LDO7	
-	-	0 V	LDO9	



	Datum	Name	
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	

CM006 (*iesy* PX30 OSM-SF)

CM006a

CM006\_PMIC2.SchDoc

16.09.2021

REV.: 1.00

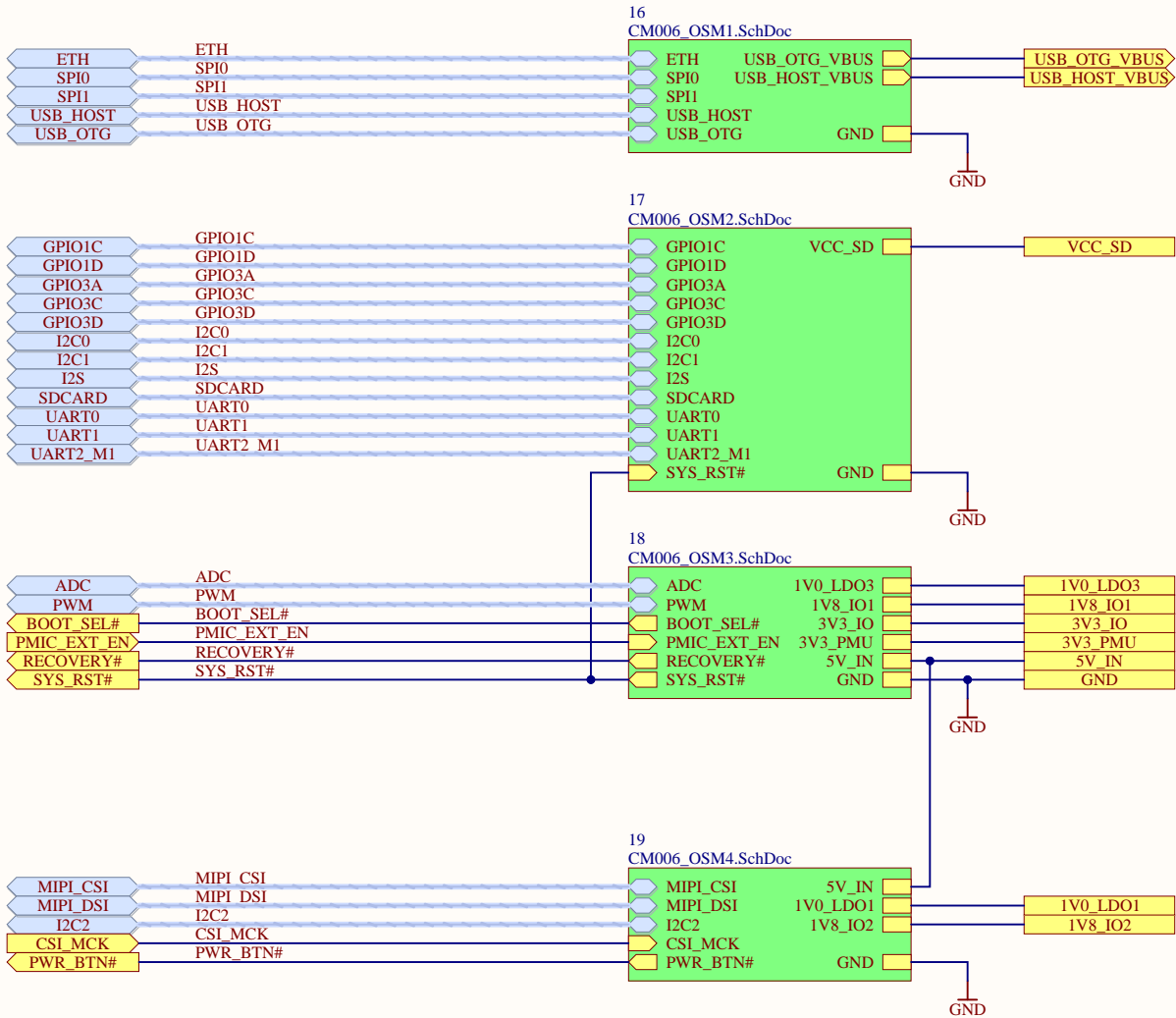
88892 - SL (4)


LK: 02.0500.0759

*PMIC Sheet 2*

Blatt-Nr: 14

von: 20



	Datum	Name	Art. Nr. 20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	

CM006 (iesy PX30 OSM-SF)  
CM006a  
CM006\_OSM\_Top.SchDoc

16.09.2021

REV.: 1.00

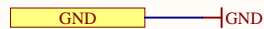
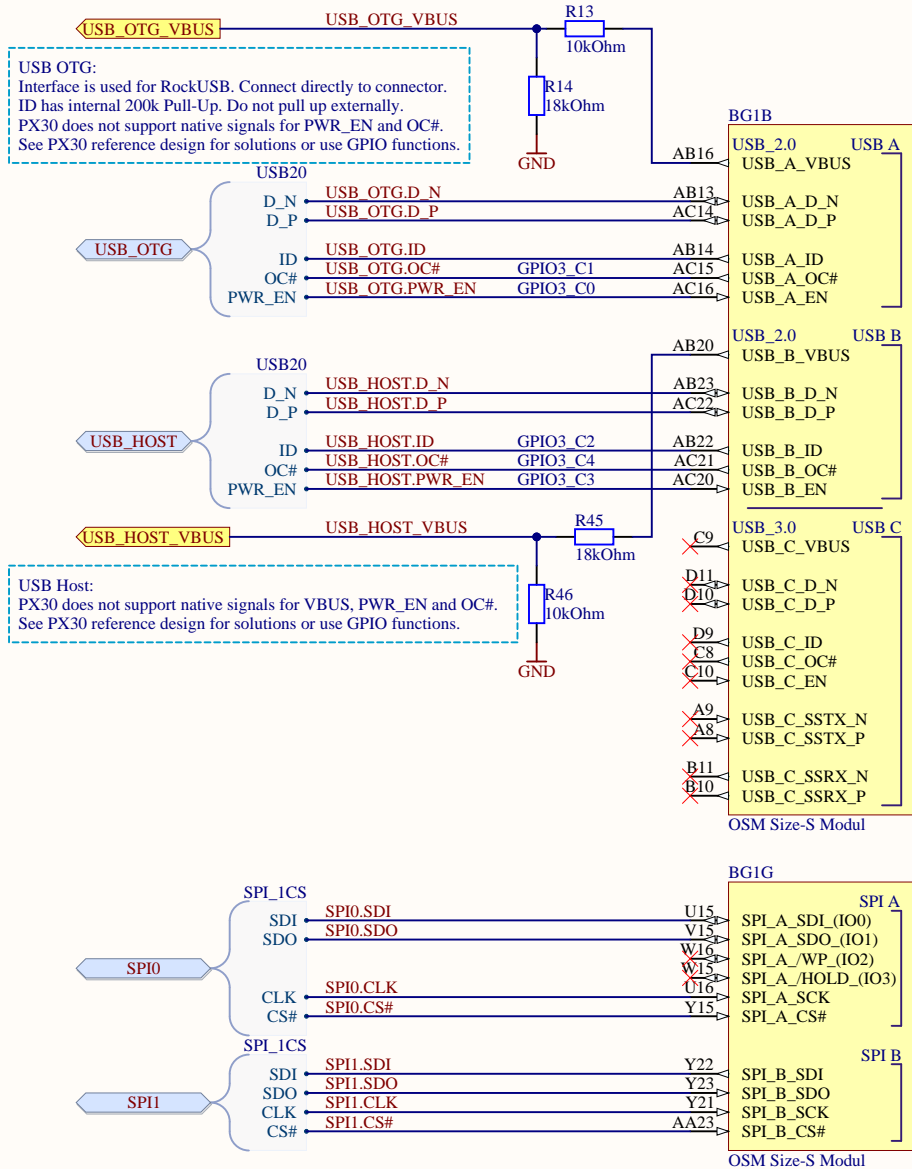
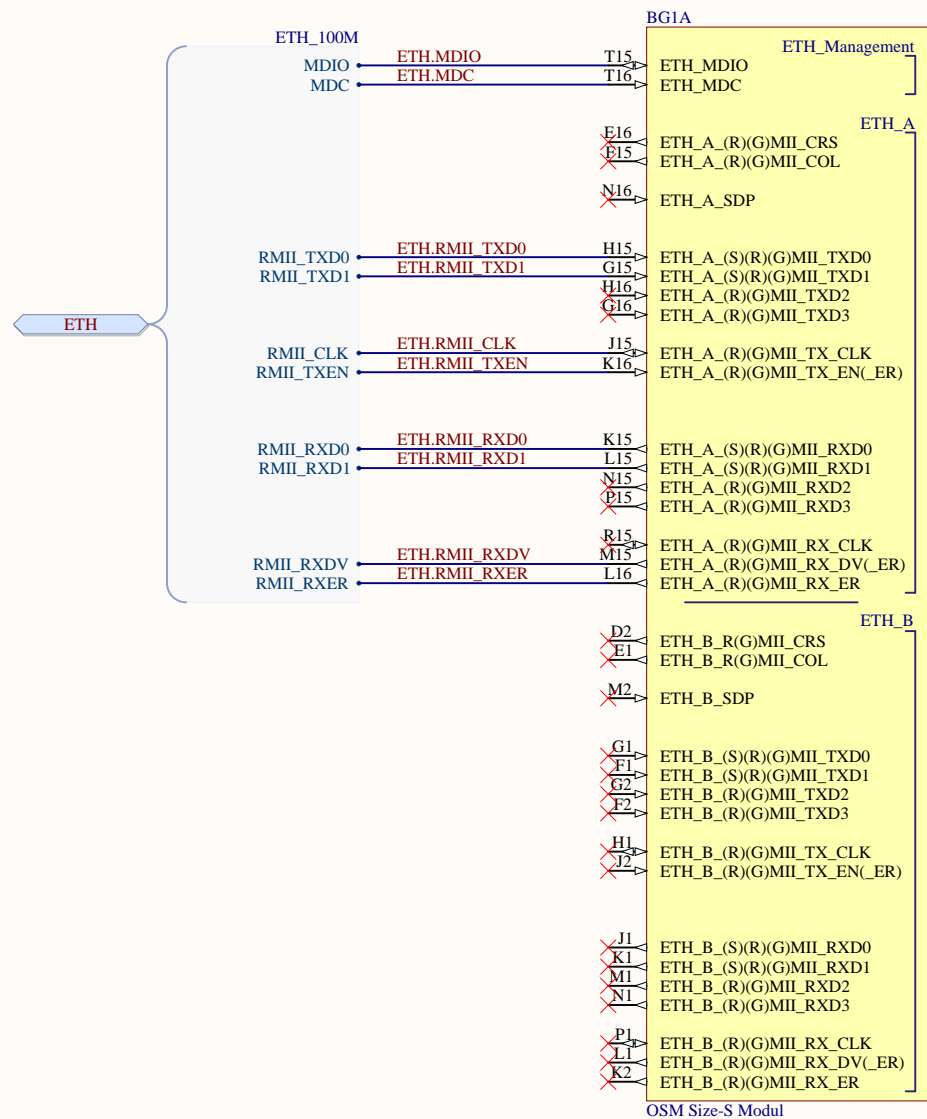
88892 - SL (4)  
OSM TOP Sheet

LK: 02.0500.0759

Blatt-Nr: 15

von: 20





	Datum	Name	Art. Nr. 20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)  
CM006a  
CM006\_OSM1.SchDoc

17.09.2021

REV.: 1.00

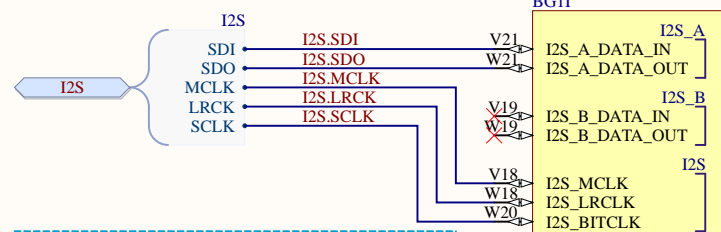
88892 - SL (4)  
OSM Sheet 1

LK: 02.0500.0759

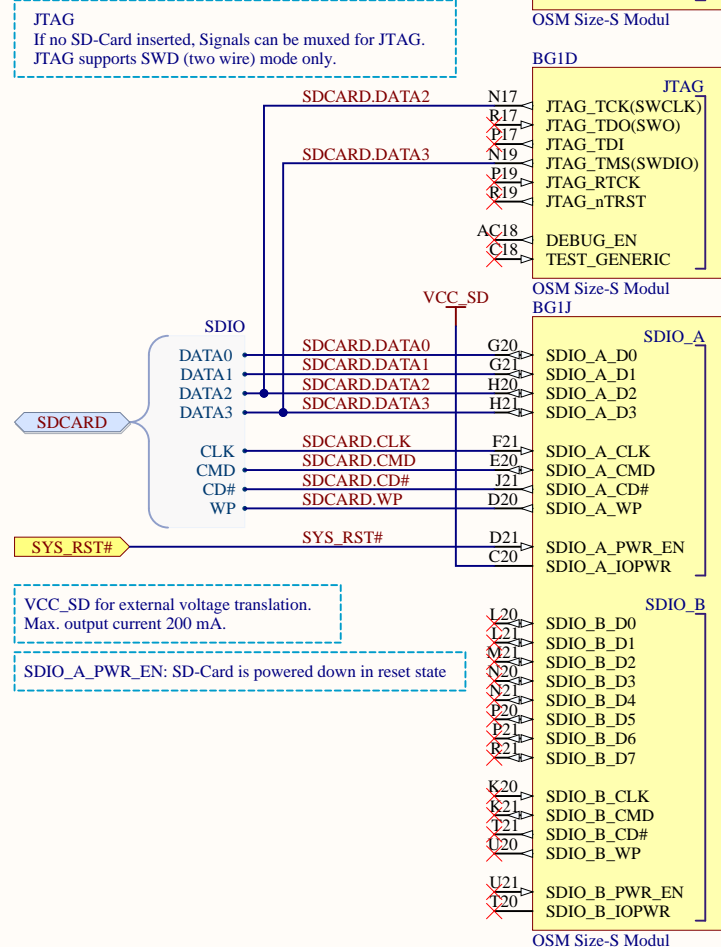
Blatt-Nr: 16

von: 20

A



B



D



	Datum	Name	Art. Nr.
	11.12.2020	MAS	20.0010.1208
Bearb.	13.08.2021	FIN	
CAD:	09.07.2021	YAG	
Prüfer:			



CM006 (iesy PX30 OSM-SF)  
 CM006a  
 CM006\_OSM2.SchDoc

17.09.2021

88892 - SL (4)  
 OSM Sheet 2

REV.: 1.00

LK: 02.0500.0759

Blatt-Nr: 17

von: 20

A

A

B

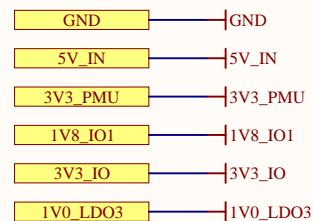
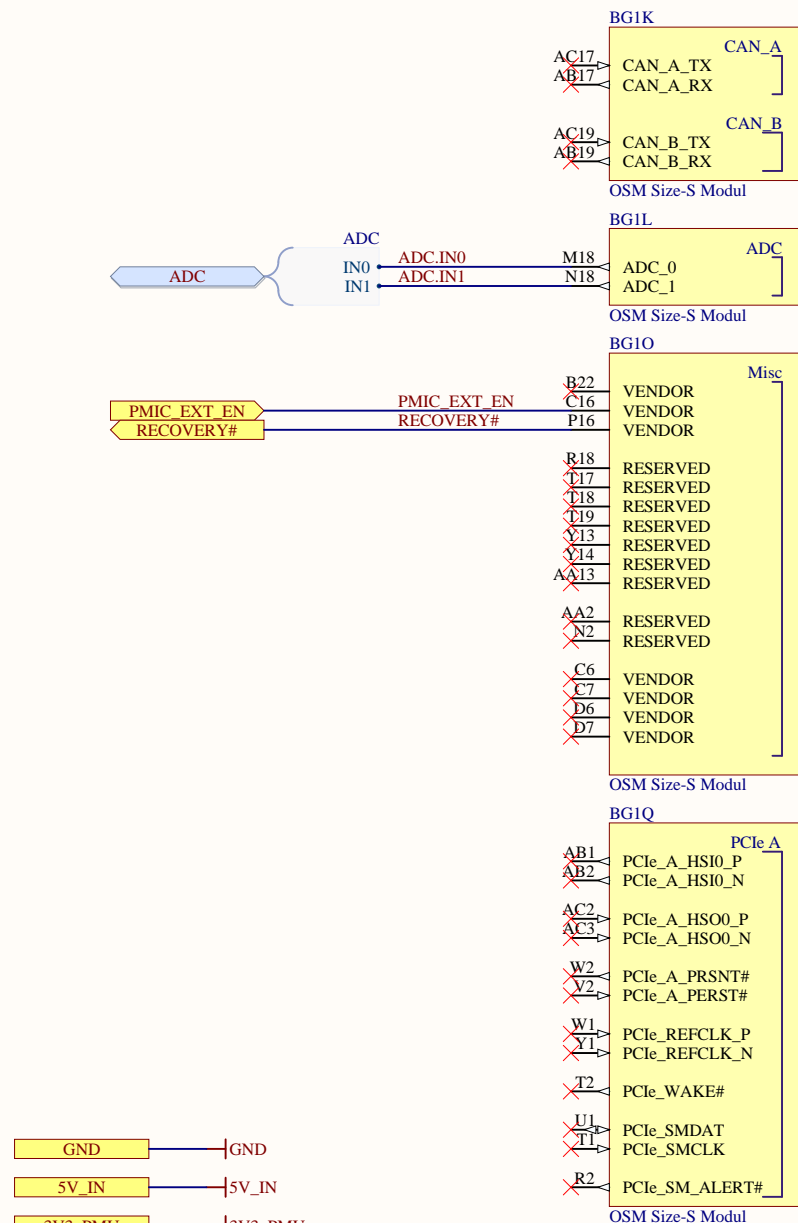
B

C

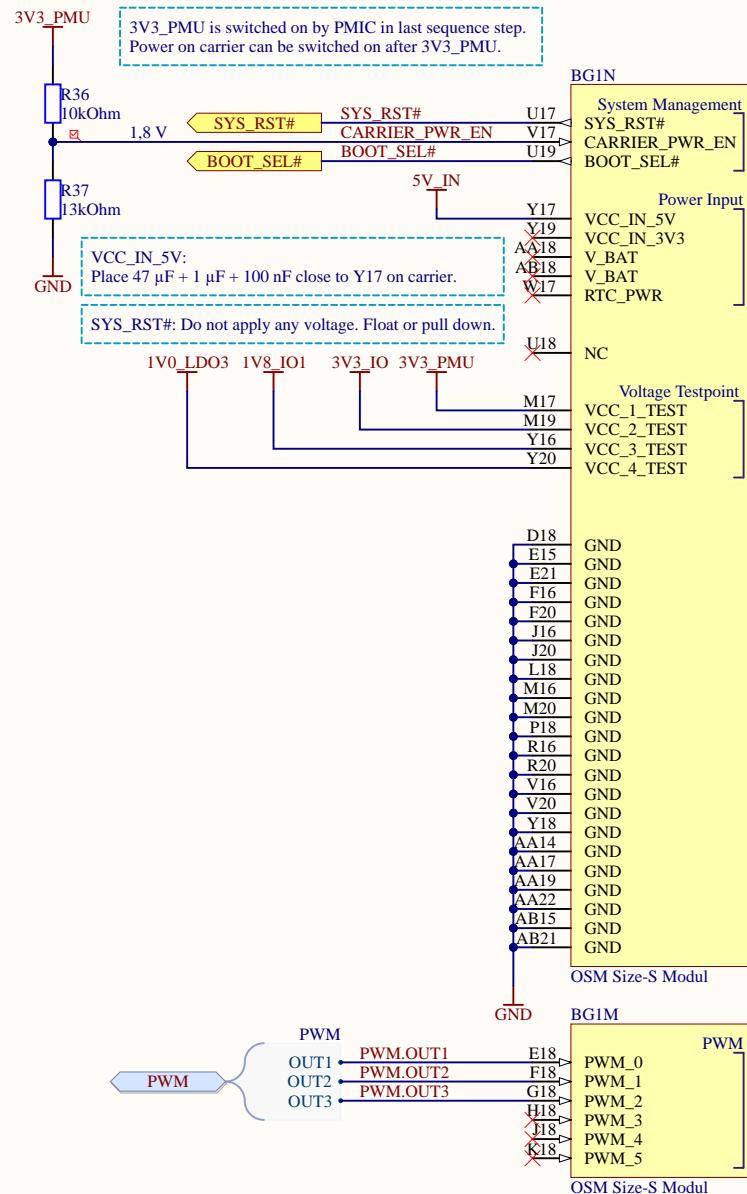
C

D

D



	Datum	Name	Art. Nr.
			20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_OSM3.SchDoc

17.09.2021

REV.: 1.00

88892 - SL (4)

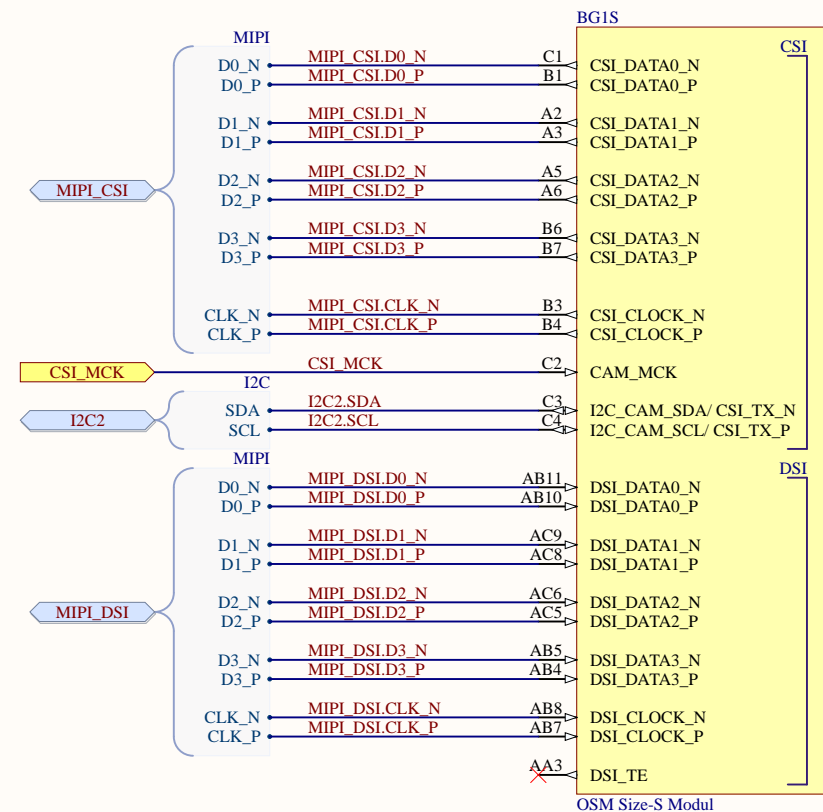
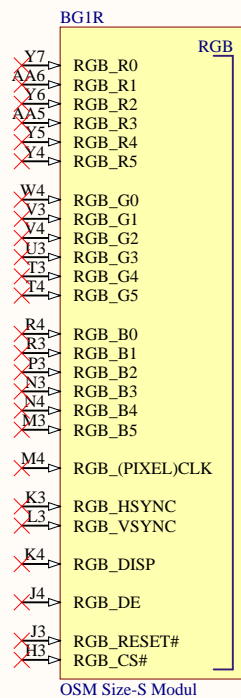
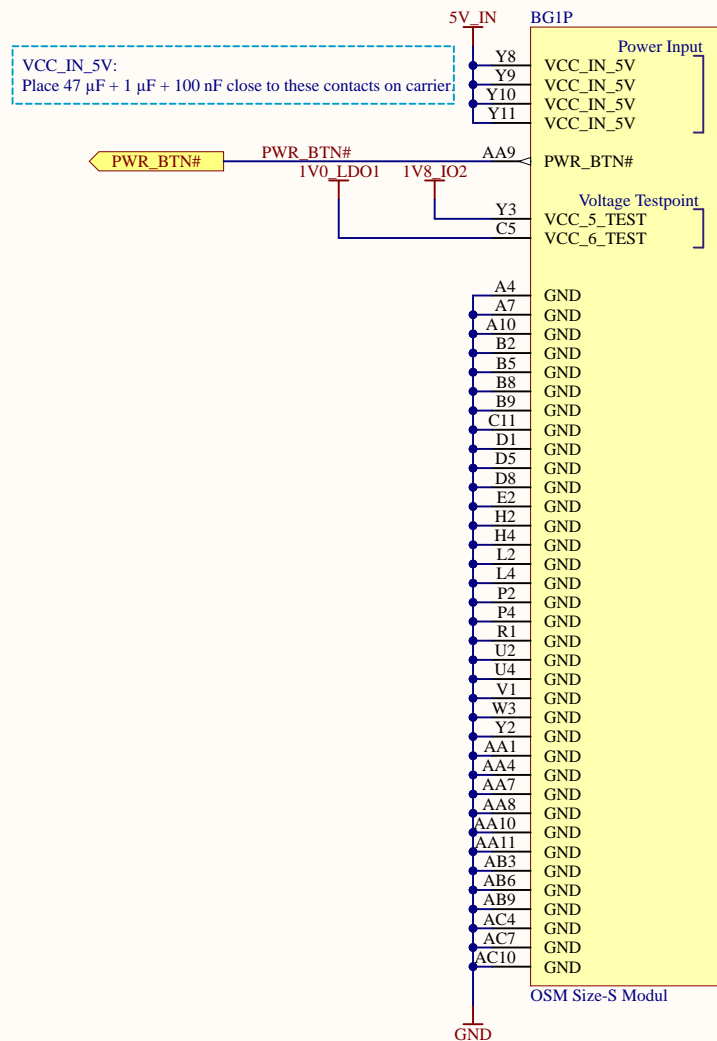
OSM Sheet 3

LK: 02.0500.0759

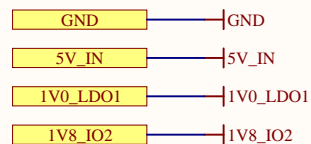
Blatt-Nr: 18

von: 20

A



D



	Datum	Name	Art. Nr.
			20.0010.1208
Bearb.	11.12.2020	MAS	
CAD:	13.08.2021	FIN	
Prüfer:	09.07.2021	YAG	



CM006 (iesy PX30 OSM-SF)

CM006a

CM006\_OSM4.SchDoc

17.09.2021

REV.: 1.00

88892 - SL (4)

OSM Sheet 4

LK: 02.0500.0759

Blatt-Nr: 19

von: 20

A

B

C

D

A

B

C

D


Board 30 mm x 30 mm  
88891: CM006 (blank PCB)  
88892: CM006a (PX30K, 8GB e-MMC, 1GB LPDDR3, 32kb EEPROM)

Revision History

Revision	Sheet	Component	Description	Date	Name
REV 1.00	All	All	First release	17.09.2021	MAS

I2C adresses

Interface I2C0 (OSM I2C\_A)  
SR1A RK809 0b0100 000x  
IC3 CAT24C32 0b1010 000x

	Datum	Name	Art. Nr. 20.0010.1208	<div><i>CM006 (iesy PX30 OSM-SF)</i></div> <div><i>CM006a</i></div> <div><i>CM006_History.SchDoc</i></div>	17.09.2021	REV.: 1.00
Bearb.	11.12.2020	MAS			<div><i>88892 - SL (4)</i></div> <div><i>History</i></div>	LK: 02.0500.0759
CAD:	13.08.2021	FIN				Blatt-Nr: 20
Prüfer:	09.07.2021	YAG				von: 20