INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

Session (2020-21)

4-Bit Right-Shift Register

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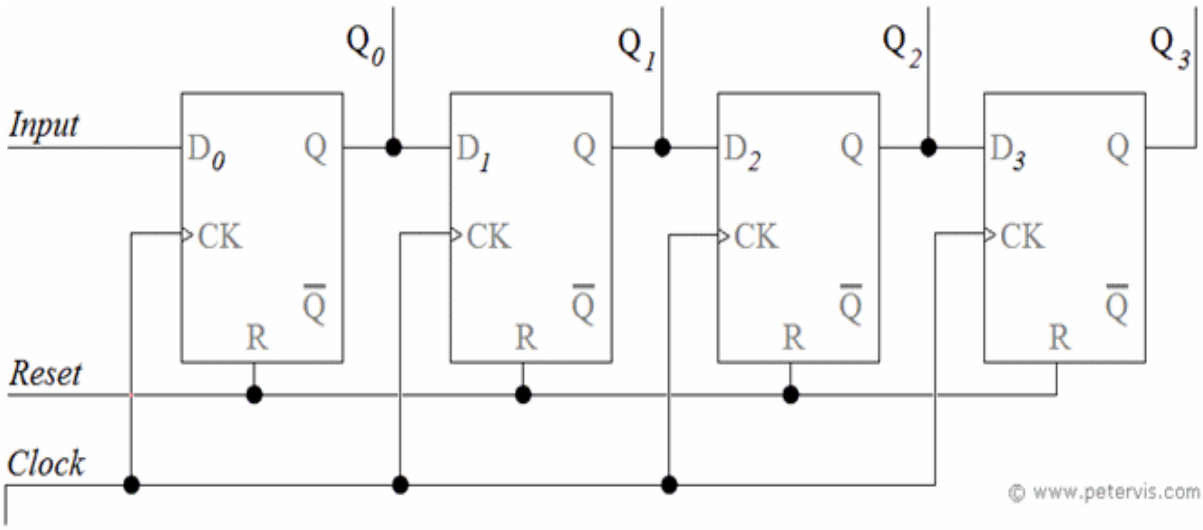
4Bit-RightShift-Register



VHDL CODE-

design.vhd

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity sreg4dflw is

 port(
        serial_in   : in    std_logic;
        clk : in    std_logic;
        q   : out   std_logic_vector(3 downto 0));

end sreg4dflw;

architecture right_shift of sreg4dflw is
begin

  process (clk)
  begin

    q(3) <= serial_in;
    q(2) <= q(3);
    q(1) <= q(2);
    q(0) <= q(1);

  end process;
  end right_shift;
```

Testbench Code-

testbench.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity sreg4dflw_tb is
end sreg4dflw_tb;

architecture right_shift of sreg4dflw_tb is
 component sreg4dflw is

 port(serial_in,clk : in std_logic;
 q : OUT std_logic_vector(3 downto 0));
 end component;
 --Inputs
 signal serial_in : std_logic := '0';
 signal clk : std_logic := '0';

 --Outputs
 signal q : std_logic_vector(3 downto 0);
 begin
 uut: sreg4dflw port map (serial_in,clk,q);
 clk_process :process
 begin
clk <= '0';
wait for 200ns;
clk <= '1';
wait for 200ns;
 end process;
 stim_proc: process
 begin
  serial_in<='1';
 wait for 400ns;
 wait;
 end process;
end;
```

EP Wave-