

# **INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE**



## **CIRCUIT DESIGN USING HDL (EIR7C4)**

**(Lab Assignment)**

**Session (2020-21)**

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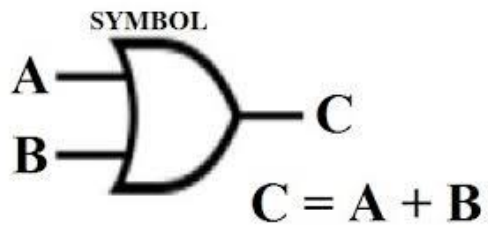
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**Q. Design OR code using VHDL language?**

**Ans.**

Circuit of OR Gate

## OR Gate



TRUTH TABLE

INPUT		OUTPUT
A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

## Design code for OR gate :

design.vhd



```
1  -- Simple OR gate VHDL Design
2  library IEEE;
3  use IEEE.std_logic_1164.all;
4
5  entity or_gate is
6  port(
7      a: in std_logic;
8      b: in std_logic;
9      q: out std_logic);
10 end or_gate;
11
12 architecture rtl of or_gate
13 is
14 begin
15     process(a, b) is
16     begin
17         q <= a or b;
18     end process;
19 end rtl;
```

## Testbench code for OR gate :

testbench.vhd



```
1  -- Testbench for VHDL Testbench
2  library IEEE;
3  use IEEE.std_logic_1164.all;
4
5  entity testbench is
6  -- empty
7  end testbench;
8
9  architecture tb of testbench
10 is
11 -- DUT component
12 component or_gate is
13 port(
14   a: in std_logic;
15   b: in std_logic;
16   q: out std_logic);
17 end component;
18
19 signal a_in, b_in, q_out:
20 std_logic;
21
22 begin
23   -- Connect DUT
24   DUT: or_gate port map(a_in,
25   b_in, q_out);
26
27   process
28   begin
29     a_in <= '0';
30     b_in <= '0';
31     wait for 1 ns;
32     assert(q_out='0') report
33     "Fail 0/0" severity error;
34
35     a_in <= '0';
36     b_in <= '1';
37     wait for 1 ns;
38     assert(q_out='1') report
39     "Fail 0/1" severity error;
40
41     a_in <= '1';
42     b_in <= 'X';
43     wait for 1 ns;
44     assert(q_out='1') report
45     "Fail 1/X" severity error;
46
47     a_in <= '1';
48     b_in <= '1';
49     wait for 1 ns;
50     assert(q_out='1') report
51     "Fail 1/1" severity error;
52
53     -- Clear inputs
54     a_in <= '0';
55     b_in <= '0';
56
57     assert false report "Test
58 done." severity note;
59     wait;
60   end process;
61 end tb;
```

## EP waveform for OR gate :

