INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV

INDORE

ELECTRONICS & INSTUMENTATION ENGINEERING

CIRCUIT DESIGN USING HDL(EIR7E1)

LAB VIVA

Session: 2020-21

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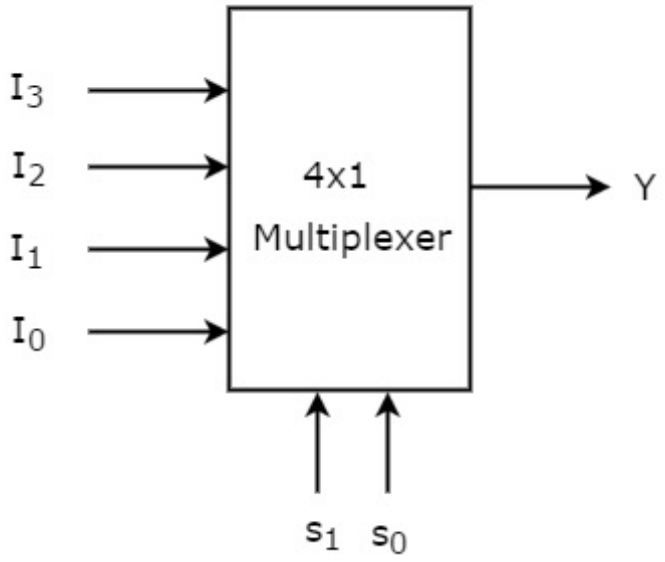
4x1 Multiplexer



Truth table of a 4:1 Mux

Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Design code

VHDL Testbench

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MUX41_IMPL_SIMBOX is
end MUX41_IMPL_SIMBOX;

architecture TEST_MUX41_IMPL
of MUX41_IMPL_SIMBOX is

component MUX41_IMPL is
    port (
          D0, D1, D2, D3, S0,
S1: in STD_LOGIC;
          mux_out : out
STD_LOGIC
    );
end component;

signal D0_test : STD_LOGIC :=
'1';
signal D1_test : STD_LOGIC :=
'0';
signal D2_test : STD_LOGIC :=
'1';
signal D3_test : STD_LOGIC :=
'1';
signal S0_test, S1_test :
STD_LOGIC := '0';
signal mux_out_test :
STD_LOGIC;

for my_MUX41_IMPL :
MUX41_IMPL use entity
work.MUX41_IMPL_top(structure
);

begin
    my_MUX41_IMPL :
MUX41_IMPL
    port map (
    D0 => D0_test,
    D1 => D1_test,
    D2 => D2_test,
    D3 => D3_test,
    S0 => S0_test,
    S1 => S1_test,
    mux_out => mux_out_test
    );

    S0_test <= not S0_test
after 2 ns;
    S1_test <= not S1_test
after 4 ns;

end TEST_MUX41_IMPL;
```

VHDL Design

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MUX41_IMPL_top is
port (
    D0, D1, D2, D3, S0, S1:
in STD_LOGIC;
    mux_out : out STD_LOGIC
);
end MUX41_IMPL_top;

architecture structure of
MUX41_IMPL_top is

component MUX41_IMPL
    port (
          D0, D1, D2, D3, S0,
S1: in STD_LOGIC;
          mux_out : out
STD_LOGIC
    );
end component;

begin

u1: MUX41_IMPL port map (D0,
D1, D2, D3, S0, S1,
mux_out);
end structure;
```

Output Waveform: