INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL

(Lab Assignment)

Session (2020-2021)

8:1 MUX

Submitted to:

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Submitted by

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E&I(7th sem)

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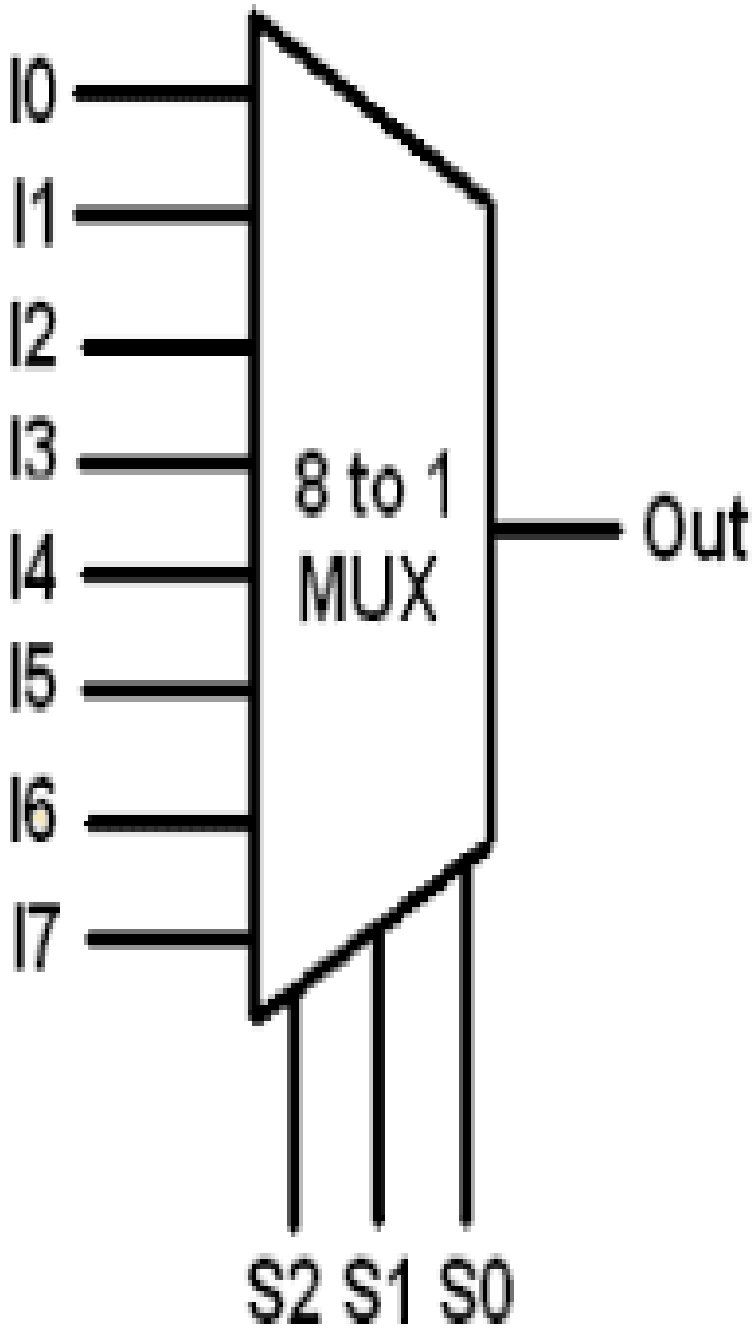
Design of 8:1 MUX

Block Diagram:



Truth Table:

Select Data Inputs			Output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

Design Code:

design.vhd

```
1
2  library IEEE;
3  use IEEE.STD_LOGIC_1164.ALL;
4  use IEEE.STD_LOGIC_ARITH.ALL;
5  use IEEE.STD_LOGIC_UNSIGNED.ALL;
6
7  entity MUX8_1 is
8      Port ( i : in  STD_LOGIC_VECTOR (7 downto 0);
9             s : in  STD_LOGIC_VECTOR (2 downto 0);
10            y : out  STD_LOGIC);
11 end MUX8_1;
12
13 architecture dataflow of MUX8_1 is
14
15 begin
16
17 with s select
18 y <=     i(0) when "000",
19           i(1) when "001",
20           i(2) when "010",
21           i(3) when "011",
22           i(4) when "100",
23           i(5) when "101",
24           i(6) when "110",
25
26           i(7) when others;
27
28 end dataflow;
```

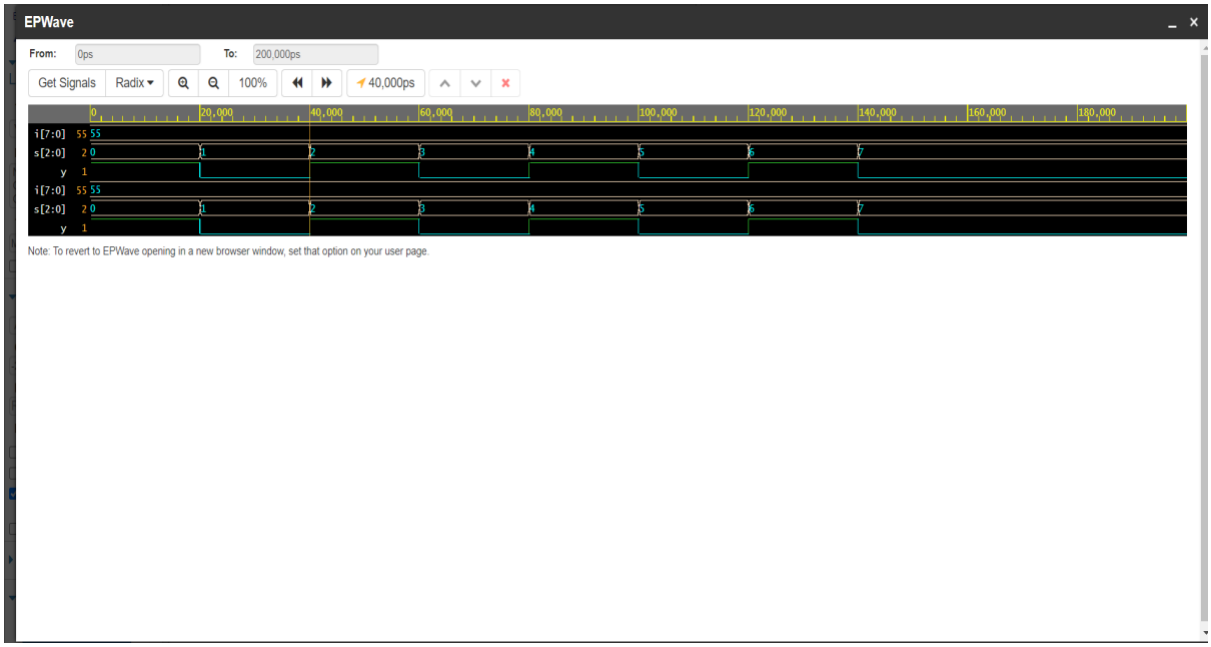
Testbench code:

testbench.vhd

VHDL Testbench

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity Mux8_1_tb is
end entity;
architecture tb of Mux8_1_tb is
component MUX8_1 is
Port ( i : in STD_LOGIC_VECTOR downto 0);
s : in STD_LOGIC_VECTOR (2 downto 0);
y : out STD_LOGIC);
end component;

signal i : STD_LOGIC_VECTOR (7 downto 0);
signal s : STD_LOGIC_VECTOR (2 downto 0);
signal y : STD_LOGIC;

begin

uut: MUX8_1 port map(
i => i,
s => s,
y => y);

stim: process
begin

i <= "01010101";
s <= "000";
wait for 20 ns;
s <= "001";
wait for 20 ns;
s <= "010";
wait for 20 ns;
s <= "011";
wait for 20 ns;
s <= "100";
wait for 20 ns;
s <= "101";
wait for 20 ns;
s <= "110";
wait for 20 ns;
s <= "111";
wait for 20 ns;
wait;

end process;
end tb;
```

Waveform:


EPWave
From:
0ps
To:
200,000ps
Get Signals
Radix
100%
40,000ps
0
20,000
40,000
60,000
80,000
100,000
120,000
140,000
160,000
180,000
i[7:0]
55
s[2:0]
2
0
1
2
3
4
5
6
7
y
1
i[7:0]
55
s[2:0]
2
0
1
2
3
4
5
6
7
y
1
Note: To revert to EPWave opening in a new browser window, set that option on your user page.