

INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE



Circuit Design using HDL (EIR7C4)

SESSION (2020-21)

Lab Assignment

Topic: Design of Negative Edge DFF
(using data flow modelling)

SUBMITTED TO :

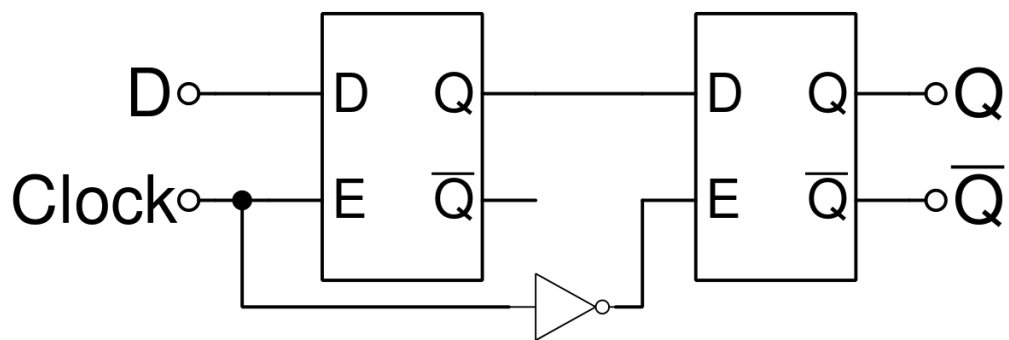
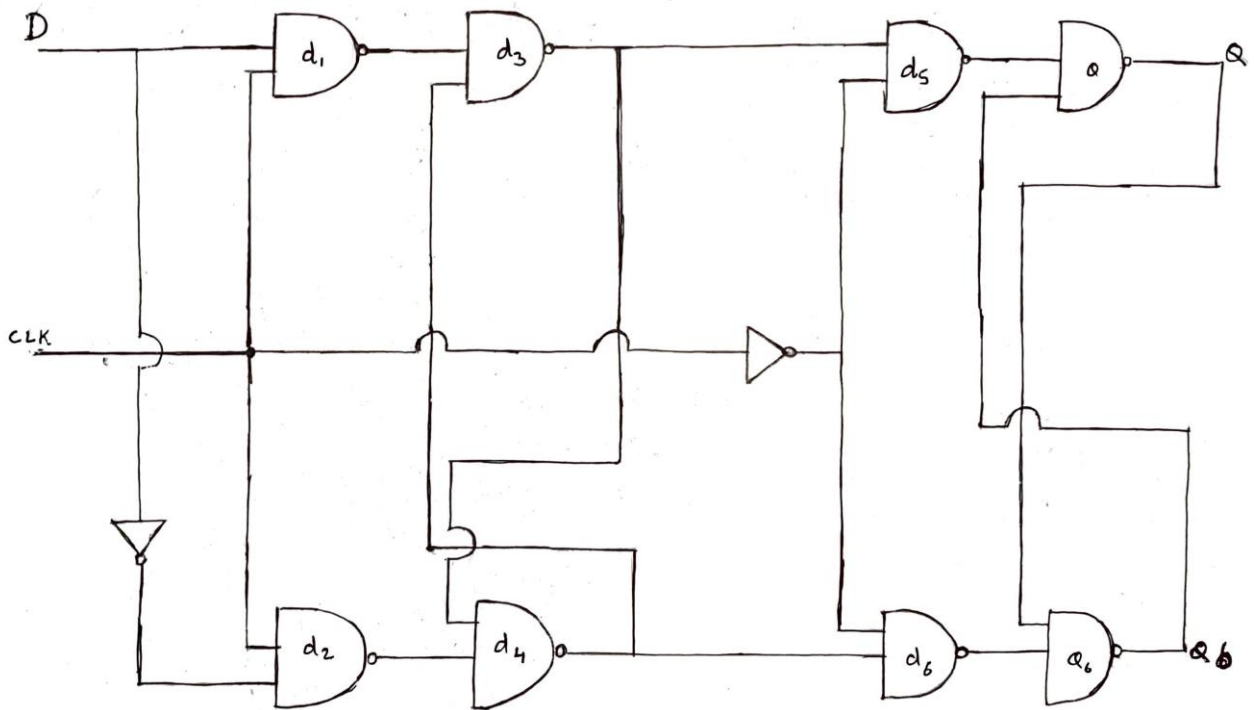
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SUBMITTED BY :

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E&I(IV yr) 7th Sem

Negative Edge Triggered D Flip Flop



Negative Edge triggered D Flip Flop

CLK	D	Q	Q _b (Q bar)
0	X	No change	No change
1	0	0	1
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	1

Table 1: negative edge triggered d flip flop

Test Bench

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DFF_tb is

end entity;

architecture tb of DFF_tb is

component DFF is

Port (D, CLK, RST : in STD_LOGIC;

Q, Qb : out STD_LOGIC);

end component ;

signal D, CLK, RST, Q, Qb : STD_LOGIC;

begin

```
 uut: DFF port map(
```

```
  D => D,
```

```
  CLK => CLK,
```

```
  RST => RST,
```

```
  Q => Q,
```

```
  Qb => Qb);
```

```
 Clock : process
```

```
begin
```

```
  CLK <= '0';
```

```
  wait for 10 ns;
```

```
  CLK <= '1';
```

```
  wait for 10 ns;
```

```
end process;
```

```
stim : process
```

```
begin
```

```
  RST <= '0';
```

```
  D <= '0';
```

```
  wait for 40 ns;
```

```
  D <= '1';
```

```
  wait for 40 ns;
```

```
end process;
```

```
end tb;
```

Design Code

```
library IEEE;
```

```
use IEEE.STD_LOGIC_1164.ALL;
```

```
use IEEE.STD_LOGIC_ARITH.ALL;
```

```
use IEEE.STD_LOGIC_UNSIGNED.ALL;
```

```
entity DFF is
```

```
Port ( d,clk : in  STD_LOGIC;
```

```
q,qb : inout STD_LOGIC);
```

```
end DFF;
```

```
architecture dataflow of DFF is
```

```
signal d1,d2,d3,d4,d5,d6:STD_LOGIC;
```

```
begin
```

```
d1 <= d nand d2;
```

```
d2 <= not d nand clk;
```

```
d3 <= d1 nand d4;
```

```
d4 <= d2 nand d3;
```

```
d5 <= d3 nand not clk;
```

```
d6 <= d4 nand not clk;
```

q <= d5 nand qb;

qb <= d6 nand q;

end dataflow;

EDAplayground

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PlaygroundsProfile

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Languages & Libraries

Testbench + Design

VHDL

Libraries

None

OVLL 2.8.1

OSVVM

Top entity

DFF_tb

Enable VUnit

Tools & Simulators

Aldec Riviera Pro 2020.04

Compile Options

-2008 -o

Run Options

Run Options

Run Time: 100 ns

Use run.do Tcl file

Use run.bash shell script

Open EPWave after run if not

downloading files after run

Examples

Community

Collaborate

Forum

testbench.vhd

VHDL Testbench

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_ARITH.ALL;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5
6 entity DFF_tb is
7 end entity;
8
9 architecture tb of DFF_tb is
10
11 component DFF is
12 Port ( D, CLK, RST : in STD_LOGIC;
13 Q, Qb : out STD_LOGIC);
14 end component ;
15
16 signal D, CLK, RST, Q, Qb : STD_LOGIC;
17
18 begin
19 uut: DFF port map(
20 D => D,
21 CLK => CLK,
22 RST => RST,
23 Q => Q,
24 Qb => Qb);
25
26 Clock : process
27 begin
28 CLK <= '0';
29 wait for 10 ns;
30 CLK <= '1';
31 wait for 10 ns;
32 end process;
33
34 stim : process
35 begin
36
37 RST <= '0';
38 D <= '0';
39 wait for 40 ns;
40 D <= '1';
41 wait for 40 ns;
42
43 end process;
44 end tb;
```

design.vhd

VHDL Design

```
1 library IEEE;
2
3 use IEEE.STD_LOGIC_1164.ALL;
4
5 use IEEE.STD_LOGIC_ARITH.ALL;
6
7 use IEEE.STD_LOGIC_UNSIGNED.ALL;
8
9 entity DFF is
10
11 Port ( d,clk : in STD_LOGIC;
12 q,qb : inout STD_LOGIC);
13
14 end DFF;
15
16
17 architecture dataflow of DFF is
18
19 signal d1,d2,d3,d4,d5,d6:STD_LOGIC;
20
21 begin
22
23 d1 <= d nand d2;
24
25 d2 <= not d nand clk;
26 d3 <= d1 nand d4;
27 d4 <= d2 nand d3;
28 d5 <= d3 nand not clk;
29 d6 <= d4 nand not clk;
30 q <= d5 nand qb;
31
32 qb <= d6 nand q;
33
34 end dataflow;
```

EDAplayground

RunSave*Copy*ASU students: please log on using the Google button.

PlaygroundsProfile

EPWave

From: 0psTo: 100,000ps

Get SignalsRadixSearch100%Navigation

CLK

D

Q

Qb

RST

CLK

D

Q

Qb

RST

Note: To revert to EPWave opening in a new browser window, set that option on your user page.