INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV

INDORE

ELECTRONICS & INSTUMENTATION ENGINEERING

CIRCUIT DESIGN USING HDL(EIR7E1)

LAB VIVA

Session: 2020-21

SUBMITTED TO:

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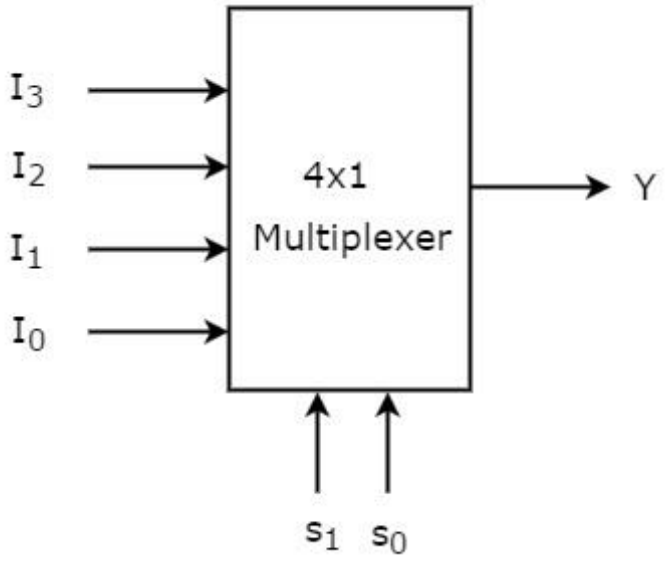
4x1 Multiplexer



Truth table of a 4:1 Mux

Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

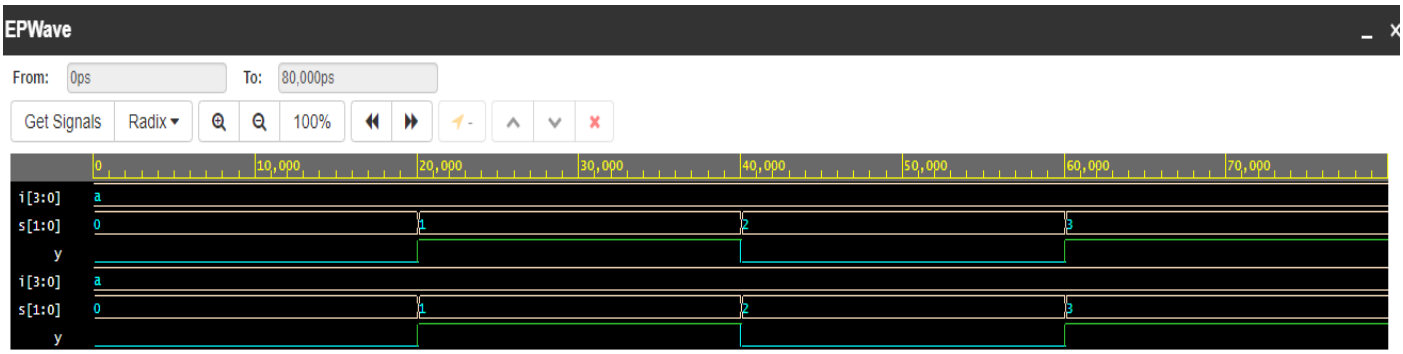
Design code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity MUX4_1 is
    Port ( i : in  STD_LOGIC_VECTOR (3 downto 0);
           s : in  STD_LOGIC_VECTOR (1 downto 0);
           y : out  STD_LOGIC);
end MUX4_1;

architecture dataflow of MUX4_1 is

begin

with s select
y <=     i(0) when "00",
         i(1) when "01",
         i(2) when "10",
         i(3) when others;

end dataflow;
```

Test-bench code

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Mux4_1_tb is
end entity;

architecture tb of Mux4_1_tb is
component MUX4_1 is
Port ( i : in STD_LOGIC_VECTOR (3 downto 0);
s : in STD_LOGIC_VECTOR (1 downto 0);
y : out STD_LOGIC);
end component;

signal i : STD_LOGIC_VECTOR (3 downto 0);
signal s : STD_LOGIC_VECTOR (1 downto 0);
signal y : STD_LOGIC;

begin

uut: MUX4_1 port map(
i => i,
s => s,
y => y);

stim: process
begin

i <= "1010";

s <= "00";
wait for 20 ns;

s <= "01";
wait for 20 ns;

s <= "10";
wait for 20 ns;

s <= "11";
wait for 20 ns;
wait;

end process;
end tb;
```

Output Waveform:



Eda playground link:

https://www.edaplayground.com/x/H25z