INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV , INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

LAB ASSIGNMENT

4 Bit Right Shift Register- Structural

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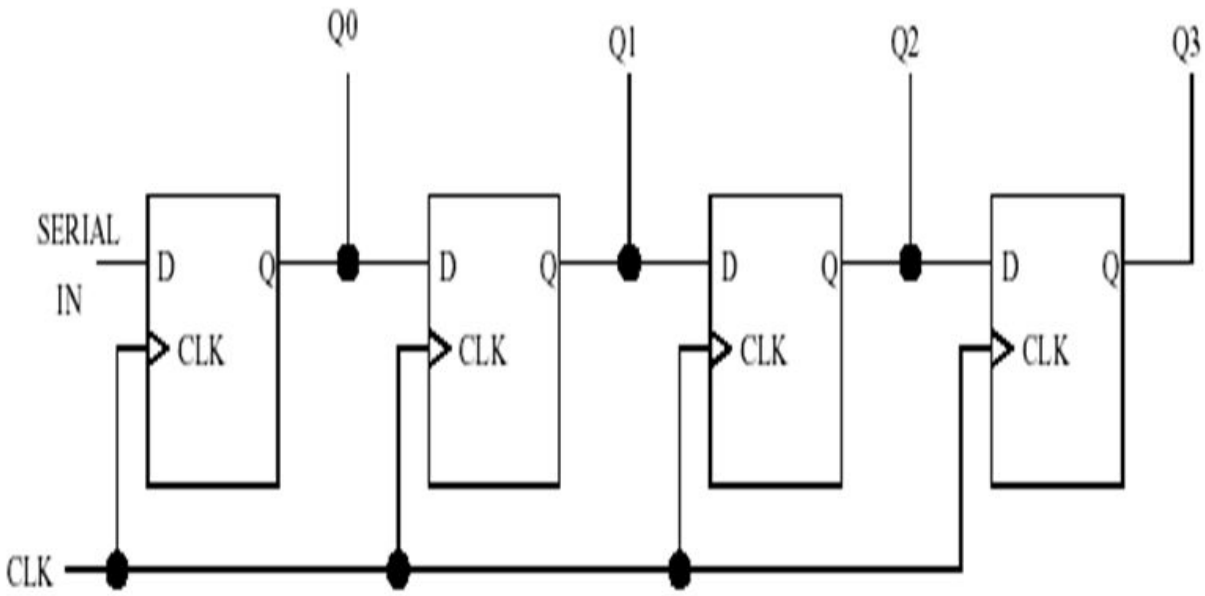
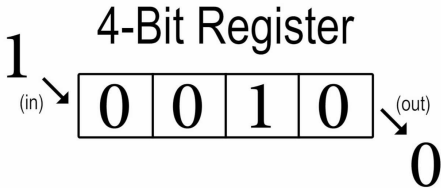
Structural Equation Modeling

Structural equation modeling is a multivariate statistical analysis technique that is used to analyze structural relationships. This technique is the combination of factor analysis and multiple regression analysis, and it is used to analyze the structural relationship between measured variables and latent constructs.

4 BIT RIGHT SHIFT USING D FLIP FLOP





VHDL Design Code

design.vhd

```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity SHIFT is
Port ( Din,clk,reset : in STD_LOGIC;
 Q : out STD_LOGIC_VECTOR (3 downto 0));
end SHIFT;

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity D_FFP is
port( clk, reset,D: in std_logic;
Q: out std_logic);
end D_FFP;
architecture Behavioral of D_FFP is
begin
process(clk,reset)
begin
if(reset='1')then
 Q <='0';
elsif(clk='1' and clk'event)then
 Q <= D;
end if;
end process;
end Behavioral;

architecture Structural of SHIFT is
component D_FFP is
port( clk, reset,D: in std_logic;
Q: out std_logic);
end component;

signal Q_temp: std_logic_vector(3 downto 1);
begin
DFF3: D_FFP port map (clk, reset, Din, Q_temp(3));
DFF2: D_FFP port map (clk, reset, Q_temp(3), Q_temp(2));
DFF1: D_FFP port map (clk, reset, Q_temp(2), Q_temp(1));
DFF0: D_FFP port map (clk, reset, Q_temp(1), Q(0));
Q(3 downto 1)<= Q_temp;
end Structural;
```

Testbench Code

testbench.vhd

```
1  -- Code your testbench here
2  library IEEE;
3  use IEEE.std_logic_1164.all;
4  use IEEE.STD_LOGIC_ARITH.ALL;
5  use IEEE.STD_LOGIC_UNSIGNED.ALL;
6
7  ENTITY TB IS
8  END ENTITY;
9  ARCHITECTURE TB OF TB IS
10  COMPONENT SHIFT IS
11  PORT(din,clk,reset : IN std_logic;
12  Q : OUT std_logic_vector(3 downto 0));
13  END COMPONENT;
14  --Inputs
15  signal din : std_logic := '0';
16  signal clk : std_logic := '0';
17  signal reset : std_logic := '0';
18  --Outputs
19  signal Q : std_logic_vector(3 downto 0);
20 BEGIN
21  uut: SHIFT PORT MAP (din,clk,reset,Q);
22  clk_process :process
23  begin
24 clk <= '0';
25 wait for 100ns;
26 clk <= '1';
27 wait for 100ns;
28  end process;
29  stim_proc: process
30  begin
31  Reset <= '1'; Din<='1';
32  wait for 200ns;
33  Reset <= '0';
34  wait;
35  end process;
36 END;
```

EP Wave