SUBJECT: CIRCUIT DESIGN USING HDL LAB

TOPIC: POSITIVE EDGE TRIGGERED D FLIP FLOP USING BEHAVIORAL STYLE OF MODELLING

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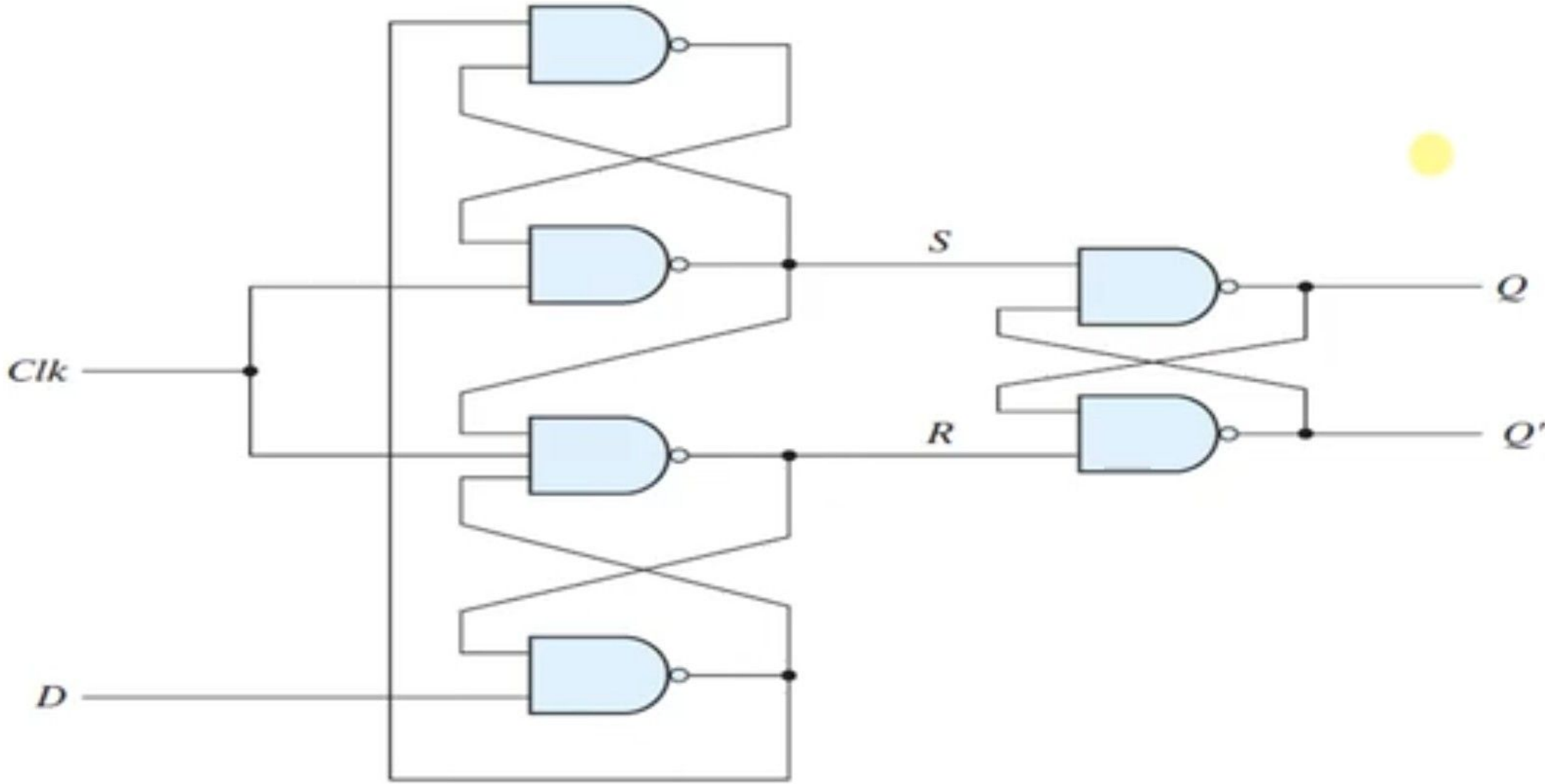
D-FLIP-FLOP (POSITIVE EDGE TRIGGERED)



TRUTH TABLE

Clk	D	Q_{t+1}	$\overline{Q_{t+1}}$
0	X	Q_T	$\overline{Q_T}$
1	X	Q_T	$\overline{Q_T}$
↑	0	0	1
↑	1	1	0

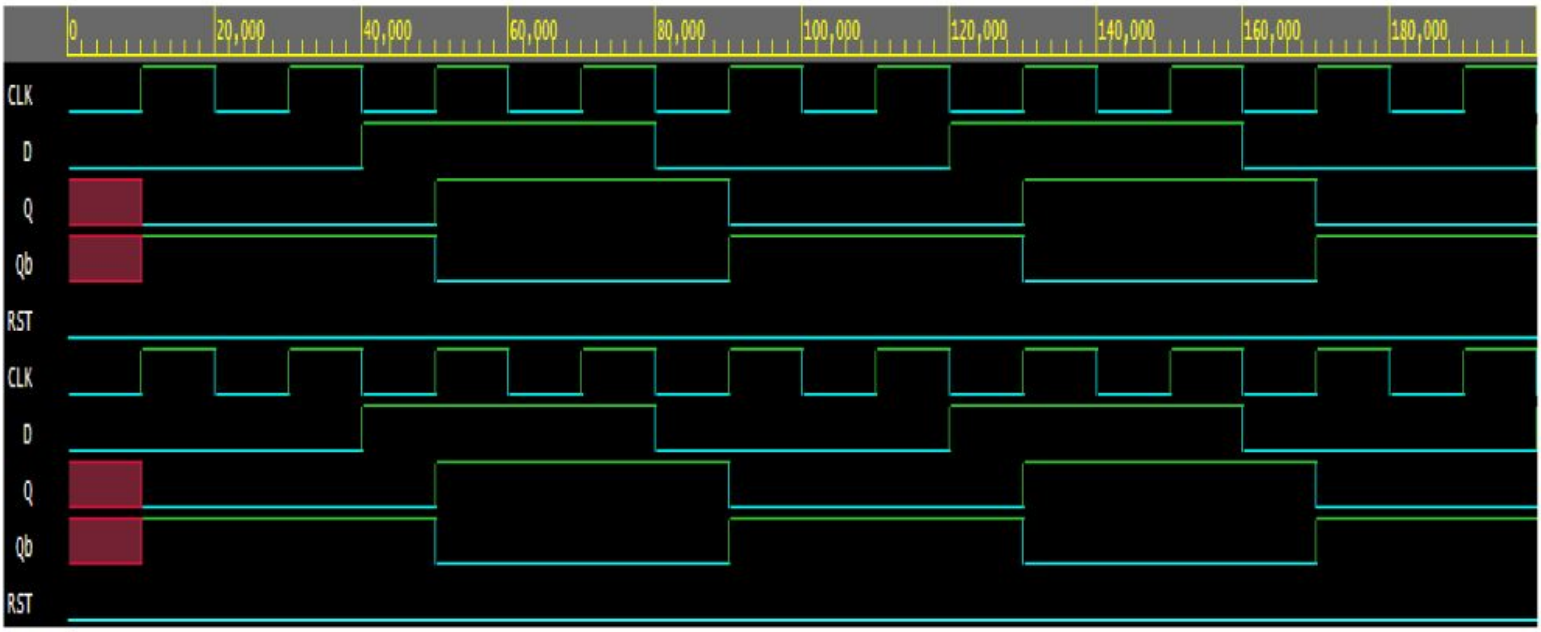
VHDL CODE FOR POSITIVE EDGE TRIGGERED D FLIP FLOP USING BEHAVIORAL STYLE OF MODELLING:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity D_FLIPFLOP_SOURCE is
Port ( D, CLK, RST : in  STD_LOGIC;
Q, Qb : out  STD_LOGIC);
end D_FLIPFLOP_SOURCE;

architecture Behavioral of D_FLIPFLOP_SOURCE is

begin
process (D, CLK, RST)
begin

if (RST = '1') then
Q <= '0';
elsif (rising_edge(CLK)) then ---this is for data flip-flop, for delay flip-flop use negative edge
Q <= D;
Qb <= not D;

end if;
end process;
end Behavioral;
```

TEST BENCH CODE

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity D_FLIPFLOP_SOURCE_tb is
end entity;

architecture tb of D_FLIPFLOP_SOURCE_tb is

component D_FLIPFLOP_SOURCE is
Port ( D, CLK, RST : in STD_LOGIC;
Q, Qb : out STD_LOGIC);
end component ;

signal D, CLK, RST, Q, Qb : STD_LOGIC;

begin
uut: D_FLIPFLOP_SOURCE port map(
D => D,
CLK => CLK,
RST => RST,
Q => Q,
Qb => Qb);

Clock : process
```

```
begin
CLK <= '0';
wait for 10 ns;
CLK <= '1';
wait for 10 ns;
end process;

stim : process
begin

RST <= '0';
D <= '0';
wait for 40 ns;
D <= '1';
wait for 40 ns;

end process;
end tb;
```


0
20,000
40,000
60,000
80,000
100,000
120,000
140,000
160,000
180,000
CLK
D
Q
Qb
RST
CLK
D
Q
Qb
RST