

# **INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV INDORE**



## **ELECTRONICS & INSTRUMENTATION ENGINEERING**

**VHDL (EIR7E1)**

**LAB VIVA**

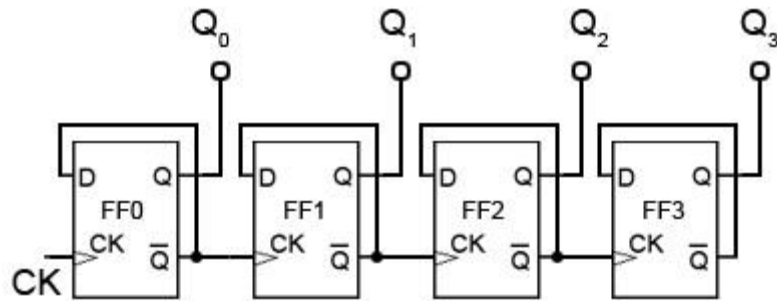
**Session: 2020-21**

**SUBMITTED TO:  
VAIBHAV NEEMA**

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## Asynchronous 4-bit UP counter



State	$Q_D$	$Q_C$	$Q_B$	$Q_A$
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

counter\_4 - EDA Playground

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Languages & Libraries

Testbench + Design

VHDL

Libraries

None OVL 2.8.1 OSVVM

Top entity

counter\_tb

Enable VUnit

Tools & Simulators

Aldec Riviera Pro 2020.04

Compile Options

-2008 -o

Run Options

Run Options

Run Time: 10 ms

Use run.do Tcd file

Use run.bash shell script

Open EPWave after run if not

downloading files after run

Examples

Community

Collaborate

testbench.vhd

```

1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 entity counter_tb is
4 end counter_tb;
5 architecture Behavioral of counter_tb is
6
7 component counter is
8 port (clk : in bit;
9       D : buffer bit_vector(3 downto 0);
10      Q : buffer bit_vector(3 downto 0) );
11 end component;
12 --Inputs
13 signal D : bit_vector(3 downto 0);
14 signal Q : bit_vector(3 downto 0);
15
16 signal clk: bit;
17
18
19
20 begin
21 uut: counter PORT MAP(c1k,D,Q);
22 --Stimulus Process
23 stim_proc:process
24 begin
25   wait for 10ns;
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40

```

design.vhd

```

1 library IEEE;
2 use IEEE.std_logic_1164.all;
3
4 entity counter is
5
6
7 port( clk : in bit;
8       D : buffer bit_vector(3 downto 0);
9       Q : buffer bit_vector(3 downto 0) );
10
11
12 end counter;
13
14
15 architecture Behavioral of counter is
16 begin
17 process(clk)
18 begin
19   if clk'event and clk='1' then
20     D(0) <= NOT(Q(0));
21     D(1) <= (NOT(Q(3))) AND (NOT(Q(1))) AND Q(0) OR (Q(1) AND (NOT(Q(0))));
22     D(2) <= (Q(2) AND (NOT(Q(1)))) OR (Q(2) AND (NOT(Q(0))) )OR ((NOT(Q(2))) AND
23     Q(1) AND Q(0));
24     D(3) <= (Q(3) AND (NOT(Q(1))) AND ( NOT(Q(0)))) OR ( Q(0) AND Q(1) AND Q(2) );

```

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Examples

Community

Collaborate

testbench.vhd

```

15
16 signal clk: bit;
17
18
19
20 begin
21 uut: counter PORT MAP(c1k,D,Q);
22 --Stimulus Process
23 stim_proc:process
24 begin
25   wait for 10ns;
26   clk <= '0';
27
28   wait for 12ns;
29   clk <= '1';
30
31   wait for 18ns;
32   clk <= '0';
33
34   wait for 20ns;
35   clk <= '1';
36
37   wait for 22ns;
38   clk <= '0';
39
40

```

design.vhd

```

1 library IEEE;
2 use IEEE.std_logic_1164.all;
3
4 entity counter is
5
6
7 port( clk : in bit;
8       D : buffer bit_vector(3 downto 0);
9       Q : buffer bit_vector(3 downto 0) );
10
11
12 end counter;
13
14
15 architecture Behavioral of counter is
16 begin
17 process(clk)
18 begin
19   if clk'event and clk='1' then
20     D(0) <= NOT(Q(0));
21     D(1) <= (NOT(Q(3))) AND (NOT(Q(1))) AND Q(0) OR (Q(1) AND (NOT(Q(0))));
22     D(2) <= (Q(2) AND (NOT(Q(1)))) OR (Q(2) AND (NOT(Q(0))) )OR ((NOT(Q(2))) AND
23     Q(1) AND Q(0));
24     D(3) <= (Q(3) AND (NOT(Q(1))) AND ( NOT(Q(0)))) OR ( Q(0) AND Q(1) AND Q(2) );

```

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testbench.vhd

```

29 clk<='1';
30
31 wait for 18ns;
32 clk<='0';
33
34 wait for 20ns;
35 clk<='1';
36
37
38 wait for 22ns;
39 clk<='0';
40
41
42 wait for 24ns;
43 clk<='1';
44
45
46 wait for 25ns;
47 clk<='0';
48
49
50 wait ;
51 end process;
52 end Behavioral;
53
54

```

VHDL Testbench

design.vhd

```

10
11
12 end counter;
13
14
15 architecture Behavioral of counter is
16 begin
17 process(clk)
18 begin
19 if clk'event and clk='1' then
20 D(0)<= NOT(Q(0));
21 D(1)<= (NOT(Q(3)) AND (NOT(Q(1))) AND Q(0)) OR (Q(1) AND (NOT(Q(0)))));
22 D(2)<= (Q(2) AND (NOT(Q(1))) OR (Q(2) AND (NOT(Q(0))) )OR ((NOT(Q(2))) AND
Q(1) AND Q(0));
23 D(3)<= (Q(3) AND (NOT(Q(1))) AND ( NOT(Q(0)))) OR ( Q(0) AND Q(1) AND Q(2) );
24
25
26 end if;
27 end process;
28 Q<=D;
29
30
31 end Behavioral;
32

```

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Examples Community

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EPWave

From: 0ps To: 131,000ps

Get Signals Radix 100%

clk  
p(3:0)  
q(3:0)  
clk  
p(3:0)  
q(3:0)

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

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