SUBJECT:CIRCUIT DESIGN USING HDL LAB

TOPIC: 4 BIT SYNCHRONOUS COUNTER USING BEHAVIORAL STYLE OF MODELLING

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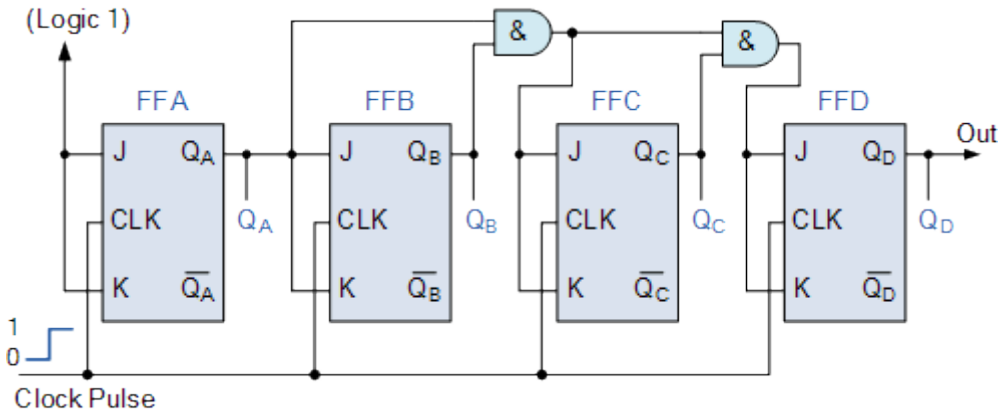
4 BIT SYNCHRONOUS COUNTER



TRUTH TABLE

Table 5.6.2

CK	Q_3	Q_2	Q_1	Q_0	$\overline{Q_3}$	$\overline{Q_2}$	$\overline{Q_1}$	$\overline{Q_0}$
0	0	0	0	0	1	1	1	1
1	0	0	0	1	1	1	1	0
2	0	0	1	0	1	1	0	1
3	0	0	1	1	1	1	0	0
4	0	1	0	0	1	0	1	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	0	0
8	1	0	0	0	0	1	1	1
9	1	0	0	1	0	1	1	0
10	1	0	1	0	0	1	0	1
11	1	0	1	1	0	1	0	0
12	1	1	0	0	0	0	1	1
13	1	1	0	1	0	0	1	0
14	1	1	1	0	0	0	0	1
15	1	1	1	1	0	0	0	0

Vhdl code for synchronous counter using behavioral style of modelling:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity SOURCE is
    Port ( CLK,RST : in  STD_LOGIC;
COUNT :inout  STD_LOGIC_VECTOR (3 downto 0));
end SOURCE;

architecture Behavioral of SOURCE is

begin
process (CLK,RST)
begin

if (RST = '1')then
COUNT <= "0000";
elsif(rising_edge(CLK))then
COUNT <= COUNT+1;

end if;
end process;
end Behavioral;
```

Testbench:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity SOURCE_tb is
end entity;
architecture tb of SOURCE_tb is
component SOURCE is
Port ( CLK,RST : in STD_LOGIC;
COUNT :inout STD_LOGIC_VECTOR (3 downto 0));
end component;
signal CLK,RST : STD_LOGIC := '1';
signal COUNT : STD_LOGIC_VECTOR(3 downto 0);
begin
uut: SOURCE port map(
CLK => CLK,
RST => RST,
COUNT => COUNT);
clock: process
begin
RST <= '0';
CLK <= '0';
wait for 20 ns;
CLK <= '1';
wait for 20 ns;
end process;
end tb;
```

OUTPUT WAVEFORM;