INSTITUTE OF ENGINEERING AND TECHNOLOGY

DAVV , INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

Session (2020-21)

Submitted to:-

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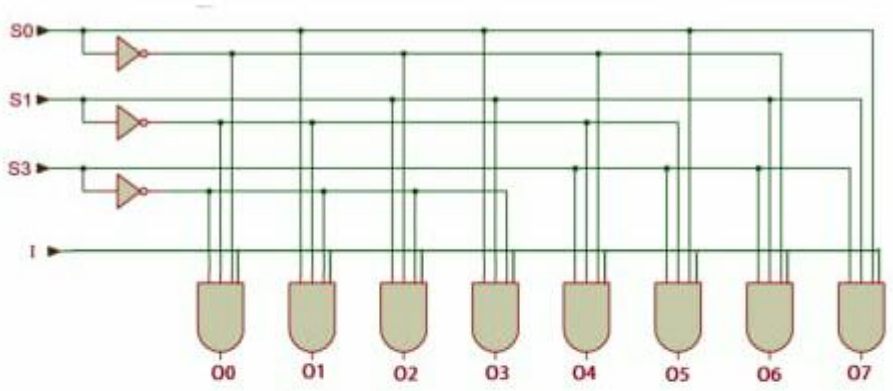
ROLL NUMBER 17E7036

1×8 Demultiplexer circuit



Truth Table

S2	S1	S0	O0	O1	O2	O3	O4	O5	O6	O7
0	0	0	I	0	0	0	0	0	0	0
0	0	1	0	I	0	0	0	0	0	0
0	1	0	0	0	I	0	0	0	0	0
0	1	1	0	0	0	I	0	0	0	0
1	0	0	0	0	0	0	I	0	0	0
1	0	1	0	0	0	0	0	I	0	0
1	1	0	0	0	0	0	0	0	I	0
1	1	1	0	0	0	0	0	0	0	I

VHDL CODE

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DEMUXSOURCE is

Port ( i : in  STD_LOGIC;

s : in STD_LOGIC_VECTOR (2 downto 0);

y : out STD_LOGIC_VECTOR (7 downto 0));

end DEMUXSOURCE;

architecture Behavioral of DEMUXSOURCE is

begin

process (i, s) is

begin

if (s <= "000") then
```

```
y(0 ) <=i ;

elsif (s <= " 0 0 1") then

y(1) <=i ;

elsif (s <= " 0 10 ") then

y(2 ) <=i ;

elsif (s<=" 0 11") then

y(3 ) <=i ;

elsif (s<=" 10 0 ") then

y(4) <=i ;

elsif (s<=" 10 1") then

y(5 ) <=i ;

elsif (s<=" 110 ") then

y(6 ) <=i ;

elsif (s<=" 111") then

y(7) <=i ;
```

```
end if;

end process;

end Behavioral;
```

TEST BENCH

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity demuxtb is
end demuxtb;
architecture tb of demuxtb is
component DEMUXSOURCE is
Port( i : in STD_LOGIC;
s : in STD_LOGIC_VECTOR (2 downto 0);
y : out STD_LOGIC_VECTOR (7 downto 0));
end component;
signal i: STD_LOGIC;
signal s: STD_LOGIC_VECTOR (2 downto 0);
signal y: STD_LOGIC_VECTOR (7 downto 0);
begin
uut: DEMUXSOURCE port map(
i => i,
s => s,
y => y);
```

```
stim: process
begin
i <= '1';
s <= "000";
wait for 10 ns;
s <= "001";
wait for 10 ns;
s <= "010";
wait for 10 ns;
s <= "011";
wait for 10 ns;
s <="100";
wait for 10 ns;
s <="101";
wait for 10 ns;
s <="110";
wait for 10 ns;
s <="111";
wait;
end process;
end tb;
```

waveform