INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

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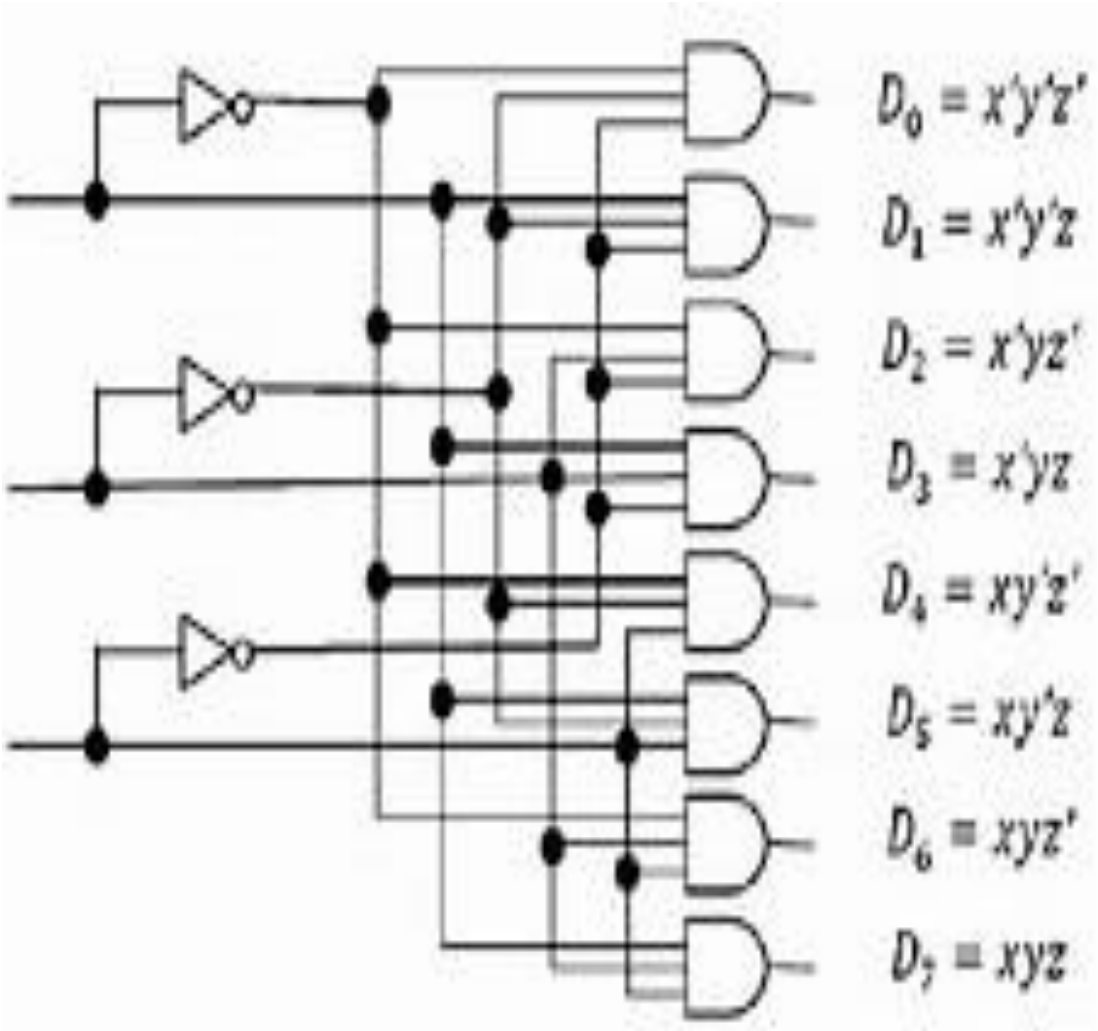
DESIGN 3:8 DECODER USING BEHAVIOURAL MODELLING.

Ans.



1)VHDL TEST BENCH CODE FOR 3:8 DECODER using BEHAVIOURAL MODELLING.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity decoder_tb is end entity;
architecture tb of decoder_tb is
component DECODER_SOURCE is
Port ( A,B,C : in STD_LOGIC;Y7,Y6,Y5,Y4,Y3,Y2,Y1,Y0 : out STD_LOGIC);
end component;
signal A, B, C, Y7, Y6, Y5, Y4, Y3, Y2, Y1, Y0 : STD_LOGIC;
begin
uut: DECODER_SOURCE port map(
A => A, B => B, C=> C,
Y7 => Y7, Y6 => Y6, Y5 => Y5, Y4 => Y4, Y3 => Y3, Y2 => Y2, Y1 => Y1, Y0 => Y0);
stim: process
begin
A <= '0';
B <= '0';
C <= '0';wait for 10 ms;
A <= '0';
B <= '0';
C <= '1';wait for 10 ms;
A <= '0';
B <= '1';
C <= '0';wait for 10 ms;
A <= '0';
B <= '1';
C <= '1';wait for 10 ms;
A <= '1';
B <= '0';
C <= '0';wait for 10 ms;
A <= '1';
B <= '0';
C <= '1';wait for 10 ms;
A <= '1';
B <= '1';
C <= '0';wait for 10 ms;
A <= '1';
B <= '1';
C <= '1';wait for 10 ms;
wait;
end process;end tb;
```

2) VHDL SOURCE CODE FOR 3:8 DECODER:

```
-- Code your design here
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity DECODER_SOURCE is
   port ( A,B,C : in STD_LOGIC;
Y7,Y6,Y5,Y4,Y3,Y2,Y1,Y0 : out STD_LOGIC);
end DECODER_SOURCE;
architecture dataflow of DECODER_SOURCE is
begin
Y0 <= ((not A)and(not B)and(not C));
Y1 <= ((not A)and(not B)and C);
Y2 <= ((not A)and B and(not C));
Y3 <= ((not A)and B and C);
Y4 <= ( A and(not B)and(not C));
Y5 <= ( A and(not B)and C);
Y6 <= ( A and B and(not C));
Y7 <= ( A and B and C);

end dataflow;

```

3) Output Waveform: