

INSTITUTE OF ENGINEERING AND TECHNOLOGY

DAVV ,INDORE



CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

Session (2020-21)

Submitted to:-

Dr. Vaibhav Nema

Submitted by :-

Manjeet Narwariya

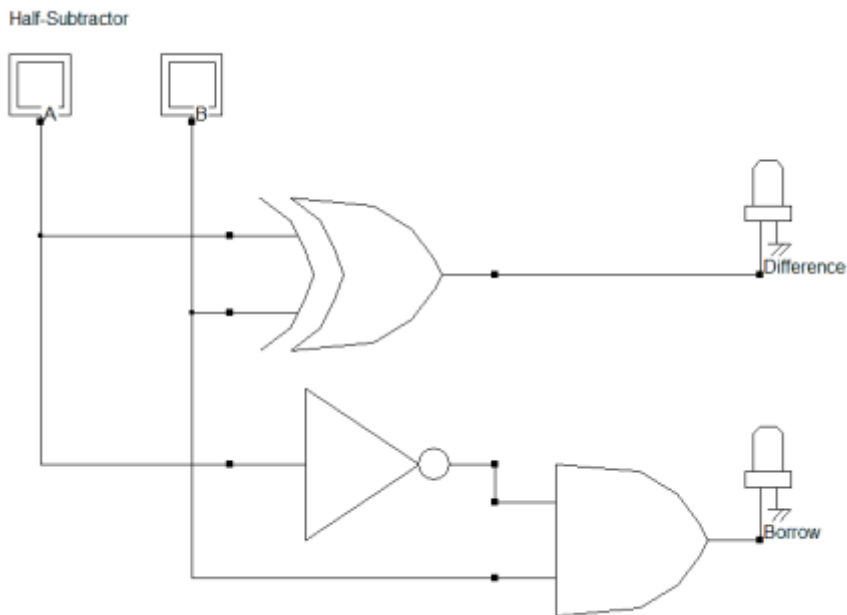
E&I (7th Sem)

Roll no – 17E7024

Enroll no. – DE17216

URL to see my Practical Code and wave - <https://www.edaplayground.com/x/b6cL>

Q- Design of 2 bit Subtractor using Behavioral Method?



Truth table of the half Subtractor-

A	B	DIFFERENCE	BORROW
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

TEST BENCH-

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity half_sub_tb is

end entity;

architecture tb of half_sub_tb is

component HS is

Port ( A : in STD_LOGIC;

B : in STD_LOGIC;

Diff : out STD_LOGIC;

Borrow : out STD_LOGIC);

end component;

signal A,B: STD_LOGIC;

signal Diff : STD_LOGIC;

signal Borrow : STD_LOGIC;

begin

uut: HS port map(

A => A, Diff => Diff,B => B,Borrow => Borrow);

stim: process

begin

    A <= '0'; B <= '0';
```

```

        wait for 20 ns;

A <= '1'; B <= '0';

        wait for 20 ns;

A <= '0'; B <= '1';

        wait for 20 ns;

A <= '1'; B <= '1';

        wait for 20 ns;

end process;

end tb;

```

DESIGN CODE-

```

library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

entity HS is

Port (

A : in STD_LOGIC;

B : in STD_LOGIC;

Diff : out STD_LOGIC;

Borrow : out STD_LOGIC

);

end HS;

architecture Behavioral of HS is

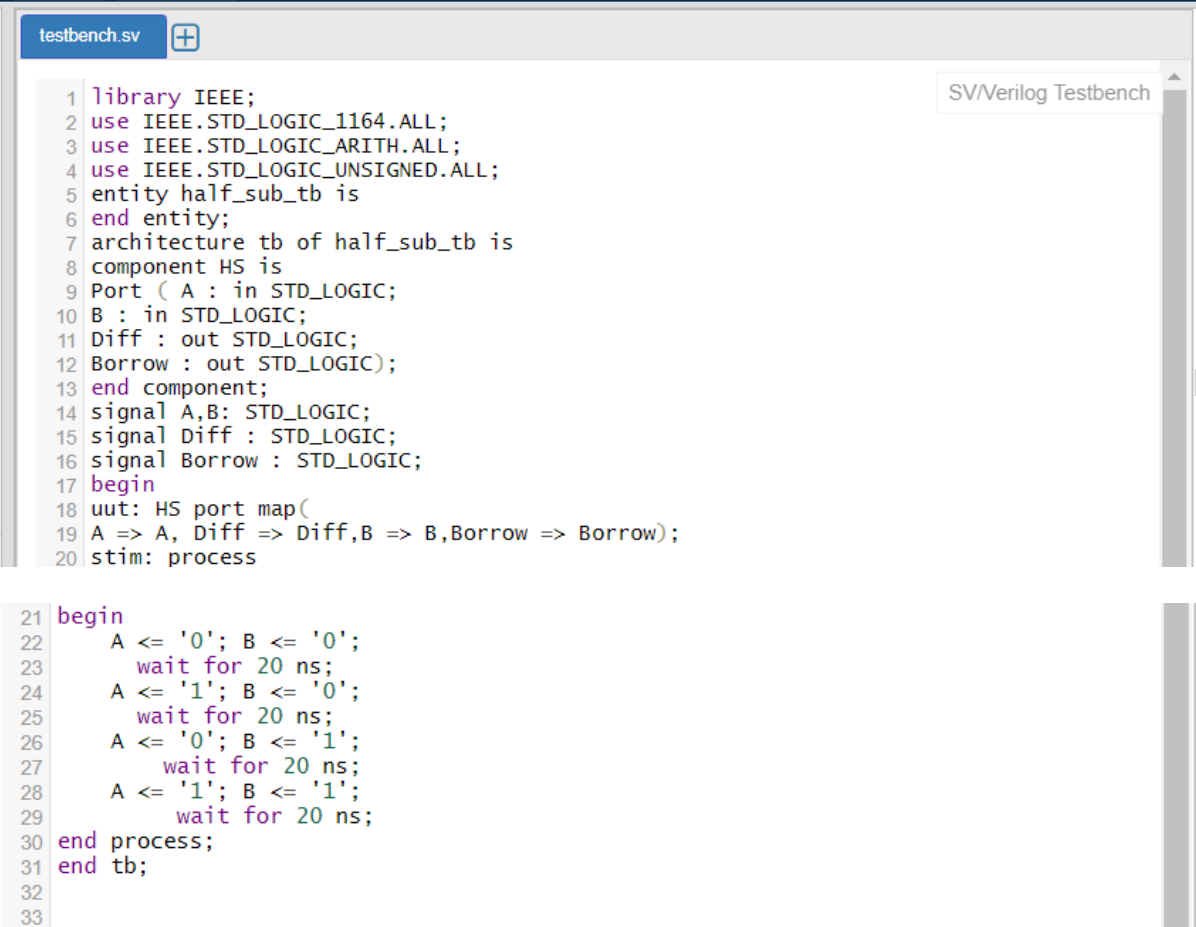
begin

process(A,B)

```

```
begin
if (A ='0' and B='0') THEN
Diff <= '0';
Borrow <= '0';
elsif (A = '0' and B='1') THEN
Diff <= '1';
Borrow <= '1';
elsif (A ='1' and B='0') THEN
Diff <= '1';
Borrow <= '0';
elsif (A = '1' and B='1') THEN
Diff <= '0';
Borrow <= '0';
else
Diff <= 'Z';
Borrow <='Z';
end if;
end process;
end Behavioral;
```

EDA Playground Test bench-



The screenshot shows the EDA Playground interface. At the top, there is a tab labeled 'testbench.sv' with a plus icon to its right. On the right side, there is a button labeled 'SV/Verilog Testbench'. The main area contains Verilog code for a testbench. The code defines an entity 'half_sub_tb' and its architecture 'tb'. It includes a component 'HS' (half-subtractor) and a process 'stim' that applies test vectors to the component's ports 'A' and 'B', and monitors the outputs 'Diff' and 'Borrow'.

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.STD_LOGIC_ARITH.ALL;
4 use IEEE.STD_LOGIC_UNSIGNED.ALL;
5 entity half_sub_tb is
6 end entity;
7 architecture tb of half_sub_tb is
8 component HS is
9 Port ( A : in STD_LOGIC;
10 B : in STD_LOGIC;
11 Diff : out STD_LOGIC;
12 Borrow : out STD_LOGIC);
13 end component;
14 signal A,B: STD_LOGIC;
15 signal Diff : STD_LOGIC;
16 signal Borrow : STD_LOGIC;
17 begin
18 uut: HS port map(
19 A => A, Diff => Diff,B => B,Borrow => Borrow);
20 stim: process
21 begin
22     A <= '0'; B <= '0';
23     wait for 20 ns;
24     A <= '1'; B <= '0';
25     wait for 20 ns;
26     A <= '0'; B <= '1';
27     wait for 20 ns;
28     A <= '1'; B <= '1';
29     wait for 20 ns;
30 end process;
31 end tb;
32
33
```

Design code -

```

design.sv
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 entity HS is
4 Port (
5 A : in STD_LOGIC;
6 B : in STD_LOGIC;
7 Diff : out STD_LOGIC;
8 Borrow : out STD_LOGIC
9 );
10 end HS;
11 architecture Behavioral of HS is
12 begin
13 process(A,B)
14 begin
15 if (A = '0' and B='0') THEN
16 Diff <= '0';
17 Borrow <= '0';
18 elsif (A = '0' and B='1') THEN
19 Diff <= '1';
20 Borrow <= '1';
21 elsif (A = '1' and B='0') THEN
22 Diff <= '1';
23 Borrow <= '0';
24 elsif (A = '1' and B='1') THEN
25 Diff <= '0';
26 Borrow <= '0';
27 else
28 Diff <= 'Z';
29 Borrow <= 'Z';
30 end if;
31 end process;
32 end Behavioral;
33
34

```

EP Waveform-

