INSTITUTE OF ENGINEERING AND TECHNOLOGY

DAVV , INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

Session (2020-21)

Submitted to:-

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Submitted by :-

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ROLL NUMBER 17E7047

Table 1				
OPERATION OF SHIFT-LEFT REGISTER				
Shift Pulse	**D**	**C**	**B**	**A**
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1
4	1	1	1	1

testbench.vhd

VHDL Testbench

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY TB IS
END ENTITY;
ARCHITECTURE TB OF TB IS
 COMPONENT SHIFT IS
 PORT(din,clk,reset : IN std_logic;
 Q : OUT std_logic_vector(3 downto 0));
 END COMPONENT;
 --Inputs
 signal din : std_logic := '0';
 signal clk : std_logic := '0';
 signal reset : std_logic := '0';
 --Outputs
 signal Q : std_logic_vector(3 downto 0);
BEGIN
 uut: SHIFT PORT MAP (din,clk,reset,Q);
 clk_process :process
 begin
clk <= '0';
wait for 100ns;
clk <= '1';
wait for 100ns;
 end process;
 stim_proc: process
 begin
 Reset <= '1'; Din<='1';
 wait for 200ns;
 Reset <= '0';
 wait;
 end process;
END;
```

design.vhd

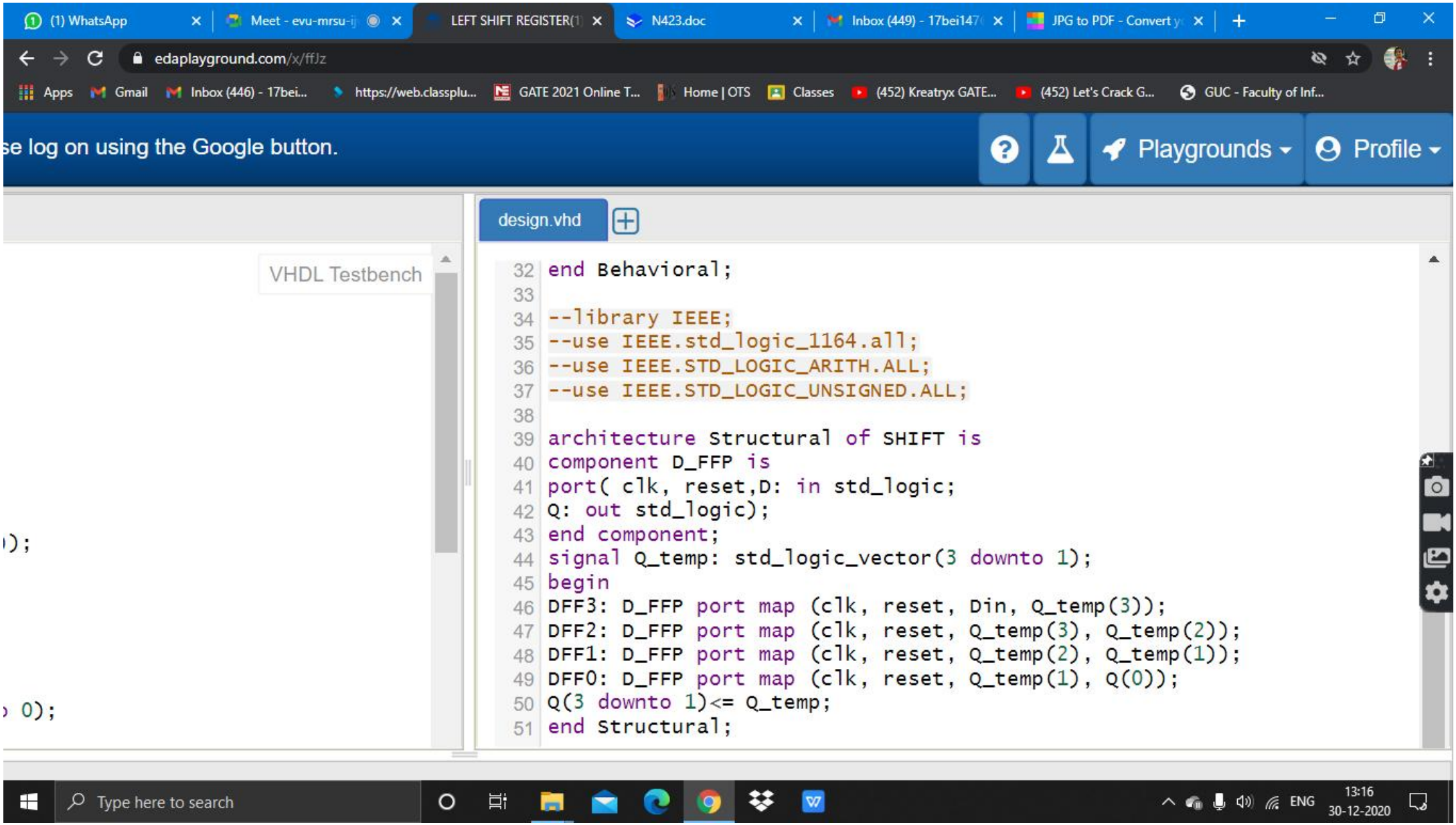
```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity SHIFT is
Port ( Din,clk,reset : in STD_LOGIC;
 Q : out STD_LOGIC_VECTOR (3 downto 0));
end SHIFT;

library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity D_FFP is
port( clk, reset,D: in std_logic;
Q: out std_logic);
end D_FFP;
architecture Behavioral of D_FFP is
begin
process(clk,reset)
begin
if(reset='1')then
 Q <='0';
elsif(clk='1' and clk'event)then
 Q <= D;
end if;
end process;
end Behavioral;

architecture Structural of SHIFT is
component D_FFP is
port( clk, reset,D: in std_logic;
Q: out std_logic);
```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Playgrounds
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VHDL Testbench
design.vhd
end Behavioral;
--library IEEE;
--use IEEE.std_logic_1164.all;
--use IEEE.STD_LOGIC_ARITH.ALL;
--use IEEE.STD_LOGIC_UNSIGNED.ALL;
architecture Structural of SHIFT is
component D_FFP is
port(clk, reset,D: in std_logic;
Q: out std_logic);
end component;
signal Q_temp: std_logic_vector(3 downto 1);
begin
DFF3: D_FFP port map (clk, reset, Din, Q_temp(3));
DFF2: D_FFP port map (clk, reset, Q_temp(3), Q_temp(2));
DFF1: D_FFP port map (clk, reset, Q_temp(2), Q_temp(1));
DFF0: D_FFP port map (clk, reset, Q_temp(1), Q(0));
Q(3 downto 1)<= Q_temp;
end Structural;
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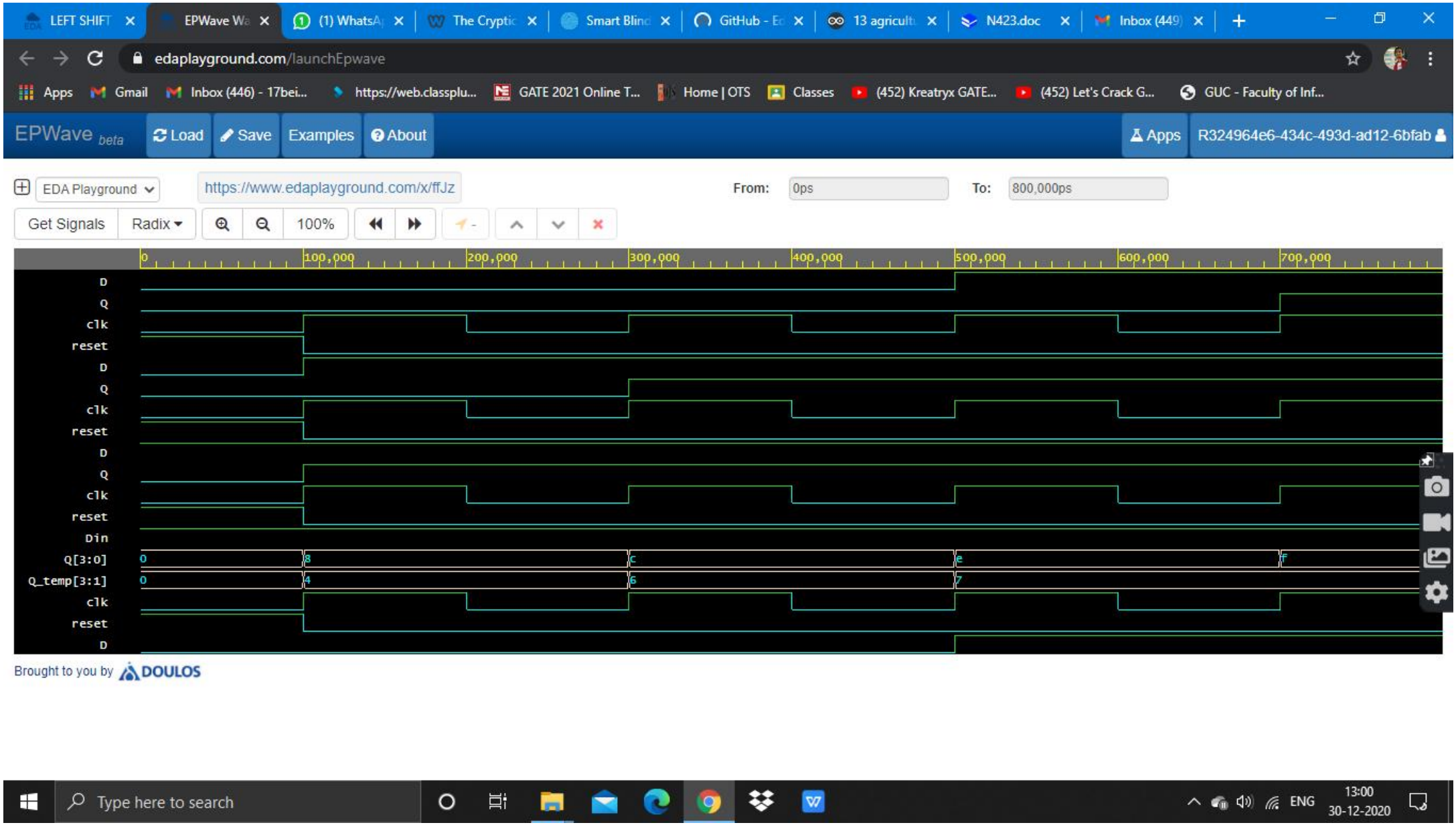
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EPWave beta
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Save
Examples
About
Apps
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EDA Playground
https://www.edaplayground.com/x/ffJz
From:
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To:
800,000ps
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100%
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700,000
D
Q
clk
reset
D
Q
clk
reset
D
Q
clk
reset
Din
Q[3:0]
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c
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f
Q_temp[3:1]
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7
clk
reset
D
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