INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV INDORE

ELECTRONICS & INSTUMENTATION ENGINEERING

VHDL (EIR7E1)

LAB VIVA

Session: 2020-21

SUBMITTED TO:
VAIBHAV NEEMA

SUBMITTED BY :

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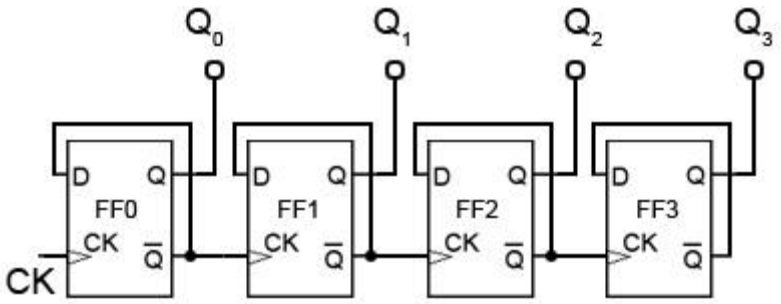
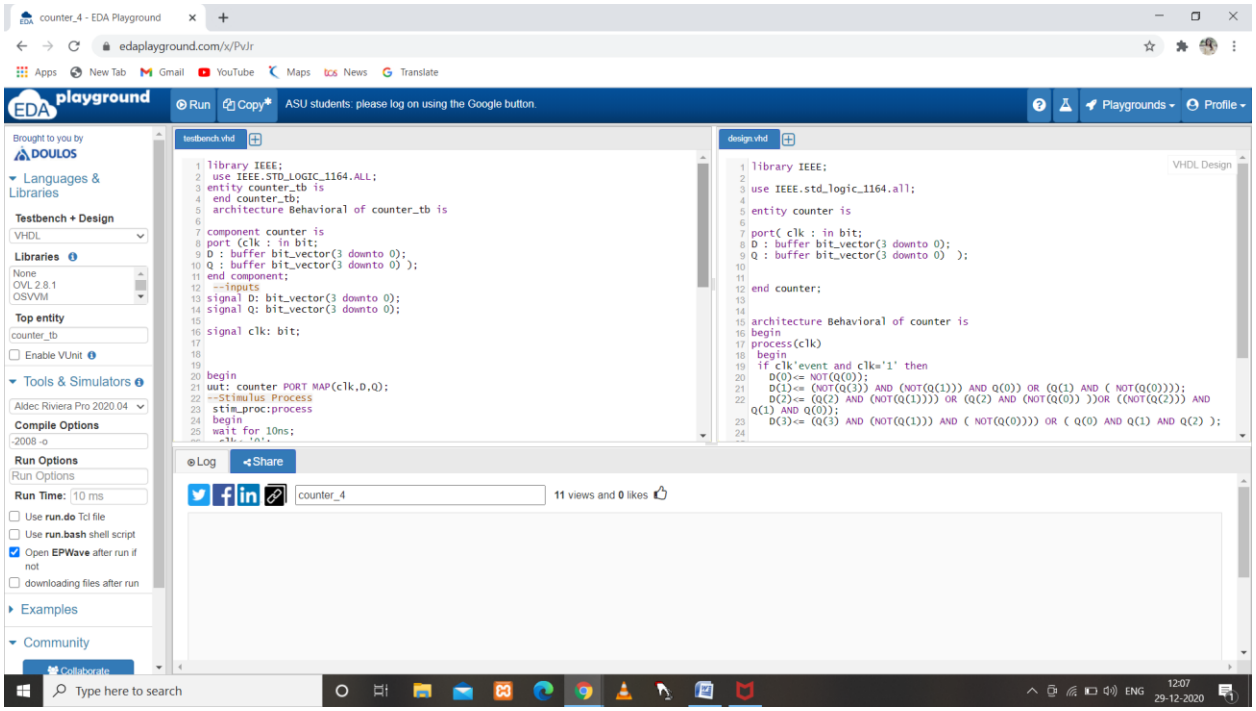
Asynchronous 4-bit UP counter



State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0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Languages & Libraries
Testbench + Design
VHDL
Libraries
None OVL 2.8.1 OSVVM
Top entity
counter_tb
Enable VUnit
Tools & Simulators
Aldec Riviera Pro 2020.04
Compile Options
-2008 -o
Run Options
Run Options
Run Time: 10 ms
Use run.do Tcl file
Use run.bash shell script
Open EPWave after run if not
downloading files after run
Examples
Community
Collaborate
testbench.vhd
design.vhd
VHDL Design
Log Share
counter_4
11 views and 0 likes
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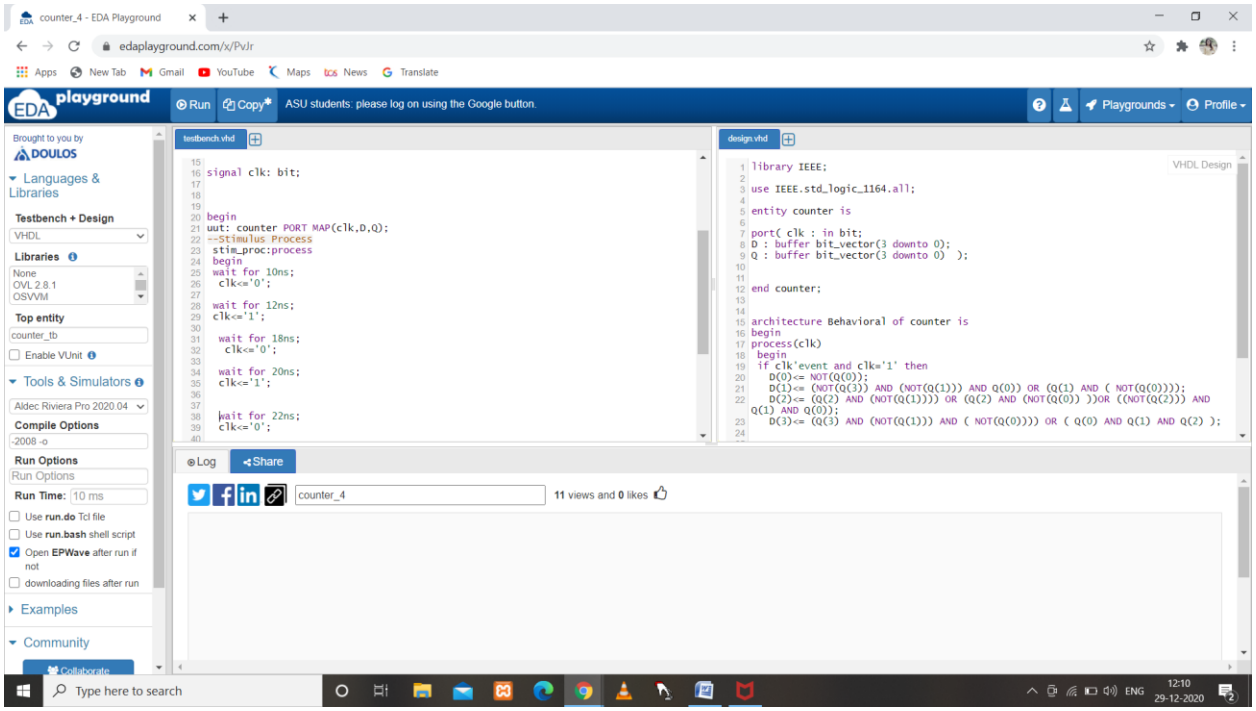
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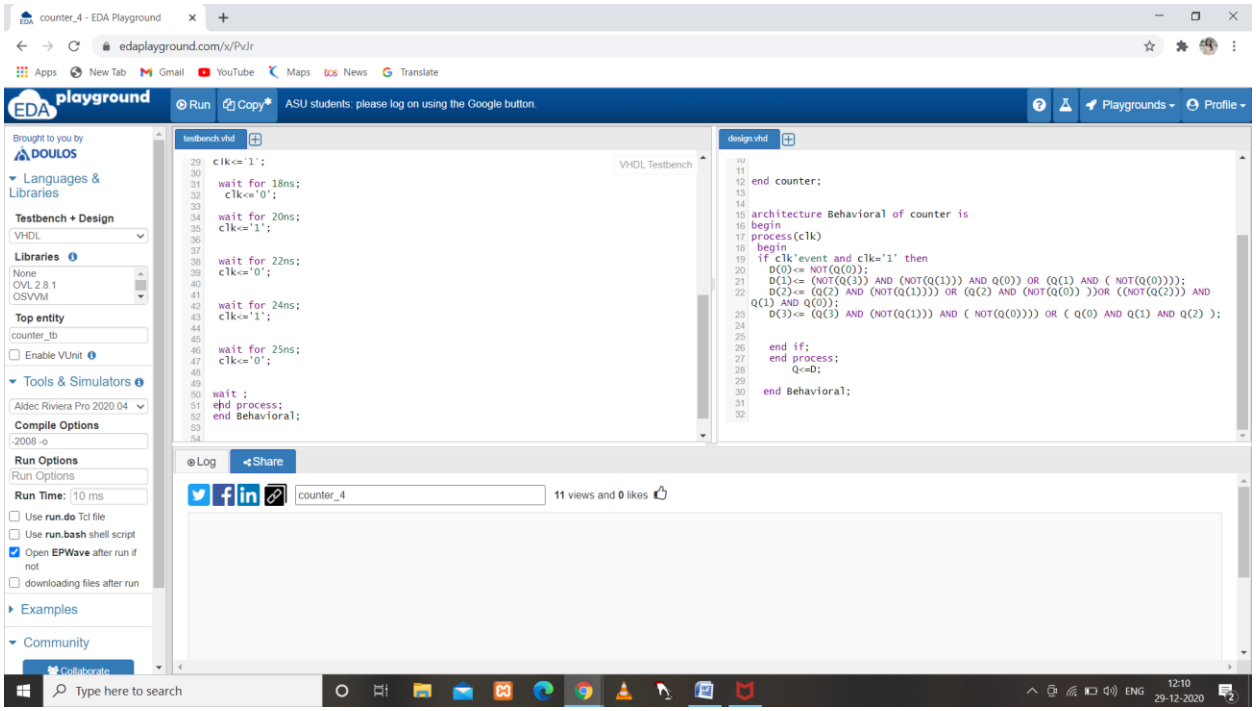
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testbench.vhd
VHDL Testbench
clk<='1';
wait for 18ns;
clk<='0';
wait for 20ns;
clk<='1';
wait for 22ns;
clk<='0';
wait for 24ns;
clk<='1';
wait for 25ns;
clk<='0';
wait ;
end process;
end Behavioral;
design.vhd
end counter;
architecture Behavioral of counter is
begin
process(clk)
begin
if clk'event and clk='1' then
D(0)<= NOT(Q(0));
D(1)<= (NOT(Q(3)) AND (NOT(Q(1))) AND Q(0)) OR (Q(1) AND (NOT(Q(0))));
D(2)<= (Q(2) AND (NOT(Q(1)))) OR (Q(2) AND (NOT(Q(0))))OR ((NOT(Q(2))) AND Q(1) AND Q(0));
D(3)<= (Q(3) AND (NOT(Q(1))) AND (NOT(Q(0)))) OR (Q(0) AND Q(1) AND Q(2));
end if;
end process;
Q<=D;
end Behavioral;
Log
Share
counter_4
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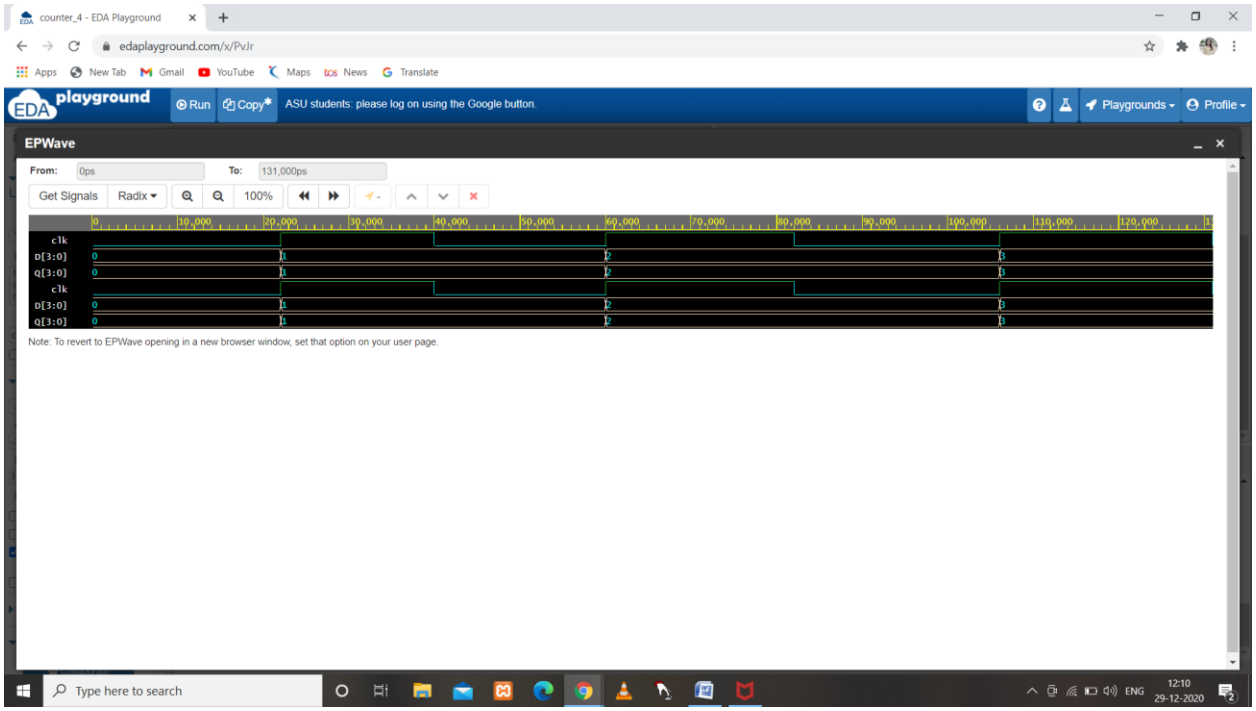
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Playgrounds
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EPWave
From: 0ps
To: 131,000ps
Get Signals
Radix
100%
0
10,000
20,000
30,000
40,000
50,000
60,000
70,000
80,000
90,000
100,000
110,000
120,000
clk
D[3:0]
Q[3:0]
clk
D[3:0]
Q[3:0]
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
Type here to search
ENG
12:10
29-12-2020