INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV

INDORE

ELECTRONICS & INSTUMENTATION ENGINEERING

VHDL (EIR7E1)

LAB VIVA

Session: 2020-21

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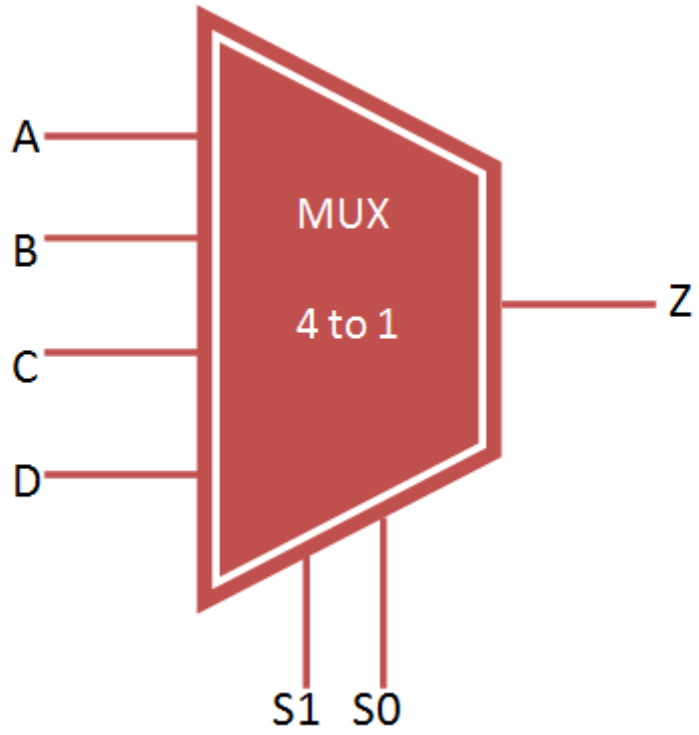
4 :1 multiplexer using Behavioural modelling



Input		output
S1	S0	Z
0	0	A
0	1	B
1	0	C
1	1	D

Design Code:

design.vhd

VHDL Design

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity mux_4to1 is
 port(

     A,B,C,D : in STD_LOGIC;
     S0,S1: in STD_LOGIC;
     Z: out STD_LOGIC
  );
end mux_4to1;

architecture bhv of mux_4to1 is
begin
process (A,B,C,D,S0,S1) is
begin
  if (S0 ='0' and S1 = '0') then
      Z <= A;
  elsif (S0 ='1' and S1 = '0') then
      Z <= B;
  elsif (S0 ='0' and S1 = '1') then
      Z <= C;
  else
      Z <= D;
  end if;

end process;
end bhv;

```

TestBench Code:

testbench.vhd

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY tb_mux IS
END tb_mux;

ARCHITECTURE behavior OF tb_mux IS


    COMPONENT mux_4to1
    PORT(
         A : IN  std_logic;
         B : IN  std_logic;
         C : IN  std_logic;
         D : IN  std_logic;
         S0 : IN  std_logic;
         S1 : IN  std_logic;
         Z : OUT  std_logic
        );
    END COMPONENT;


   signal A : std_logic := '0';
   signal B : std_logic := '0';
   signal C : std_logic := '0';
   signal D : std_logic := '0';
   signal S0 : std_logic := '0';
   signal S1 : std_logic := '0';


   signal Z : std_logic;

BEGIN


   uut: mux_4to1 PORT MAP (
          A => A,
          B => B,
          C => C,
          D => D,
          S0 => S0,
          S1 => S1,
          Z => Z
        );


   stim_proc: process
   begin

      wait for 20 ns;

    A <= '1';
    B <= '0';
    C <= '1';
    D <= '0';

    S0 <= '0'; S1 <= '0';

      wait for 20 ns;

    S0 <= '1'; S1 <= '0';

      wait for 20 ns;

    S0 <= '0'; S1 <= '1';

        wait for 20 ns;

    S0 <= '1'; S1 <= '1';

        wait for 20 ns;

    end process;

END;
```

Output:

EPWave beta
Load
Save
Examples
About
Apps
R153c656e-a03d-4727-b5b2-a8cae
EDA Playground
https://www.edaplayground.com/x/7mrN
From:
0ps
To:
200,000ps
Get Signals
Radix
100%
0
20,000
40,000
60,000
80,000
100,000
120,000
140,000
160,000
180,000
A
B
C
D
S0
S1
Z

Link to EDA playground:

https://www.edaplayground.com/x/7nrN