INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

Session (2020-21)

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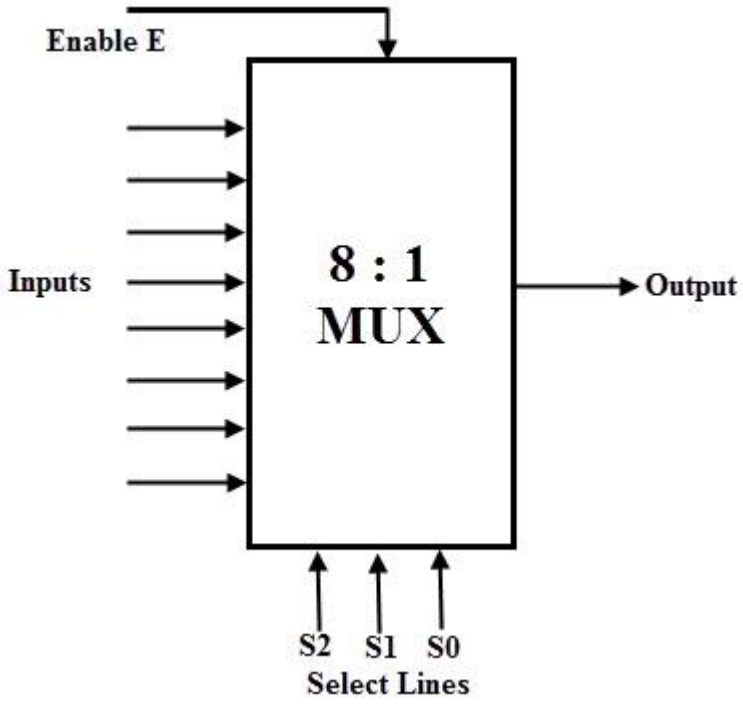
Q. Design Of 8:1 MUX.
Ans.



Truth Table of 8:1 MUX

S1	S2	S3	O
0	0	0	I1
0	0	1	I2
0	1	0	I3
0	1	1	I4
1	0	0	I5
1	0	1	I6
1	1	0	I7
1	1	1	I8

Testbench code of 8:1 MUX

testbench.vhd

VHDL Testbench

```
-- Code your testbench here
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.all;
USE ieee.numeric_std.ALL;

ENTITY tb_multiplexer_vhd IS
END tb_multiplexer_vhd;

ARCHITECTURE behavior OF tb_multiplexer_vhd IS

-- Component Declaration for the Unit Under Test (UUT)
COMPONENT multiplexer
PORT(
x:IN std_logic_vector(7 downto 0);
sel:IN std_logic_vector(2 downto 0);
y:OUT std_logic
);
END COMPONENT;

--Inputs
SIGNAL x : std_logic_vector(7 downto 0) := (others=>'0');
SIGNAL sel : std_logic_vector(2 downto 0) := (others=>'0');

--Outputs
```

testbench.vhd

VHDL Testbench

```
20
21 --Inputs
22 SIGNAL x : std_logic_vector(7 downto 0) := (others=>'0');
23 SIGNAL sel : std_logic_vector(2 downto 0) := (others=>'0');
24
25 --Outputs
26 SIGNAL y : std_logic;
27
28 BEGIN
29
30 -- Instantiate the Unit Under Test (UUT)
31 uut: multiplexer PORT MAP(x => x,
32 sel => sel,
33 y => y
34 );
35 x<= "01010101" after 10ns;
36 sel<= "001" after 10ns,"010" after 20ns,"011" after 30ns,"100" after 40ns,"101" after 50ns,"110"
   after 60ns, "111" after 70ns;
37
38 END;
39
40
```

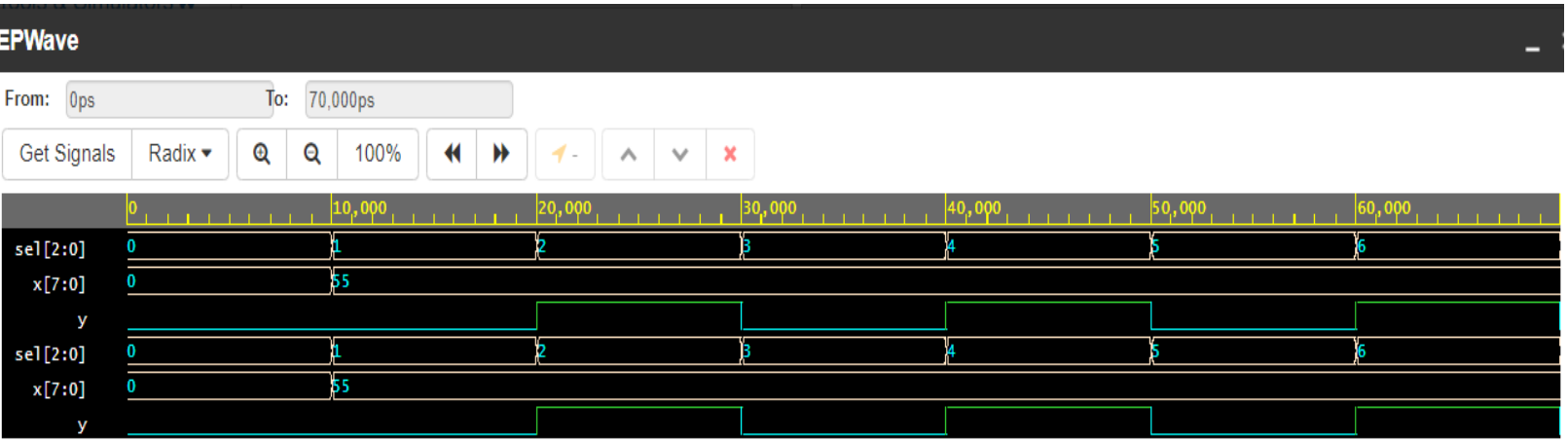
Design code of 8:1 MUX

design.vhd

VHDL Design

```
1  -- Code your design herelibrary IEEE;
2  library IEEE;
3  use IEEE.STD_LOGIC_1164.ALL;
4  use IEEE.STD_LOGIC_ARITH.ALL;
5  use IEEE.STD_LOGIC_UNSIGNED.ALL;
6  entity multiplexer is
7  Port ( x:in STD_LOGIC_VECTOR (7 downto 0);
8  sel:in STD_LOGIC_VECTOR (2 downto 0);
9  y : out STD_LOGIC);
10 end multiplexer;
11 architecture Behavioral of multiplexer is
12 begin
13 process (x,sel)
14 begin
15 case sel is
16 when "000"=>y<=x(0);
17 when "001"=>y<=x(1);
18 when "010"=>y<=x(2);
19 when "011"=>y<=x(3);
20 when "100"=>y<=x(4);
21 when "101"=>y<=x(5);
22 when "110"=>y<=x(6);
23 when "111"=>y<=x(
24 end Behavioral;7);
25 when others=> null;
26 end case;
27 end process;
```

Output of 8:1 MUX



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