INSTITUTE OF ENGINEERING & TECHNOLOGY
INDORE

ELECTRONICS AND INSTRUMENTATION
(2017-2021)

CIRCUIT DESIGN USING VHDL :

VHDL code for 4-bit Synchronous counter using data flow style of modelling

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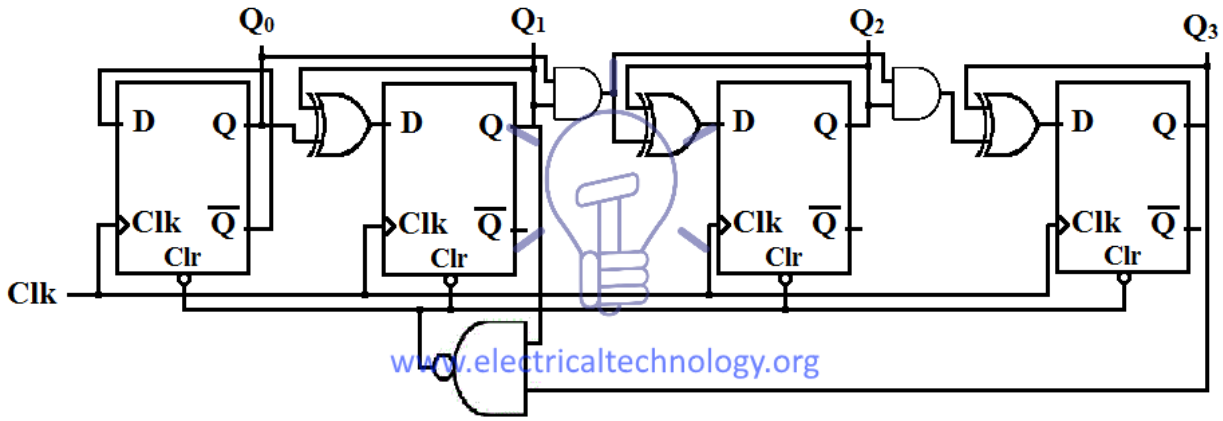
4 bit Synchronous counter



VHDL Code for 4 –bit synchronous counter:

Testbench code :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
entity sync_counter_tb is
end entity;

architecture tb of sync_counter_tb is
component updown_count is
Port ( clk,rst,updown : in STD_LOGIC;
count : out STD_LOGIC_VECTOR (3 downto 0));
end component;

signal clk, rst, updown : STD_LOGIC := '0';
signal count : STD_LOGIC_VECTOR (3 downto 0);
constant num_of_clocks : integer := 20;
signal i : integer := 0;
constant T : time := 20 ns;
begin
uut: updown_count port map(
clk => clk,
rst => rst,
updown => updown,
```

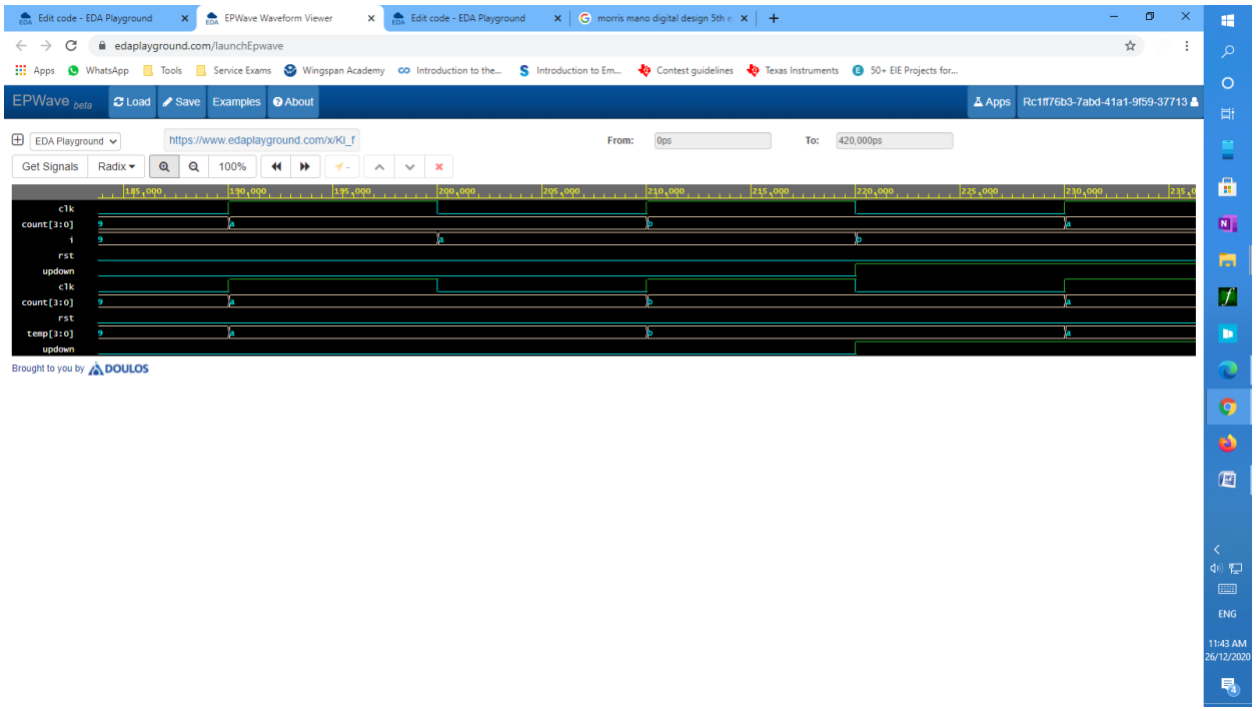
```
count => count);

process

begin

rst <= '0';

clk <= '0';

wait for T/2;

clk <= '1';

wait for T/2;

if (i = num_of_clocks) then

wait;

else

i <= i + 1;

end if;

if (i < 10) then

updown <= '0';

else

updown <= '1';

end if;

end process;

end tb;
```

Design code :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;
```

```
entity updown_count is
   Port ( clk,rst,updown : in  STD_LOGIC;
          count : out  STD_LOGIC_VECTOR (3 downto 0));
end updown_count;

architecture Behavioral of updown_count is

signal temp:std_logic_vector(3 downto 0):="0000";

begin
process(clk,rst)
begin

if(rst='1')then
temp<="0000";
elsif(rising_edge(clk))then
if(updown='0')then
temp<=temp+1;
else
temp<=temp-1;
end if;
end if;
end process;

count<=temp;
end Behavioral;
```

Waveform :



The above VHDL can be viewed here: https://www.edaplayground.com/x/Ki_f