INSTITUTE OF ENGINEERING AND TECHNOLOGY,INDORE

Circuit Design using HDL (EIR7C4)

SESSION (2020-21)

Lab Assignment

Topic: Design of Negative Edge DFF

(using data flow modelling)

SUBMITTED TO :

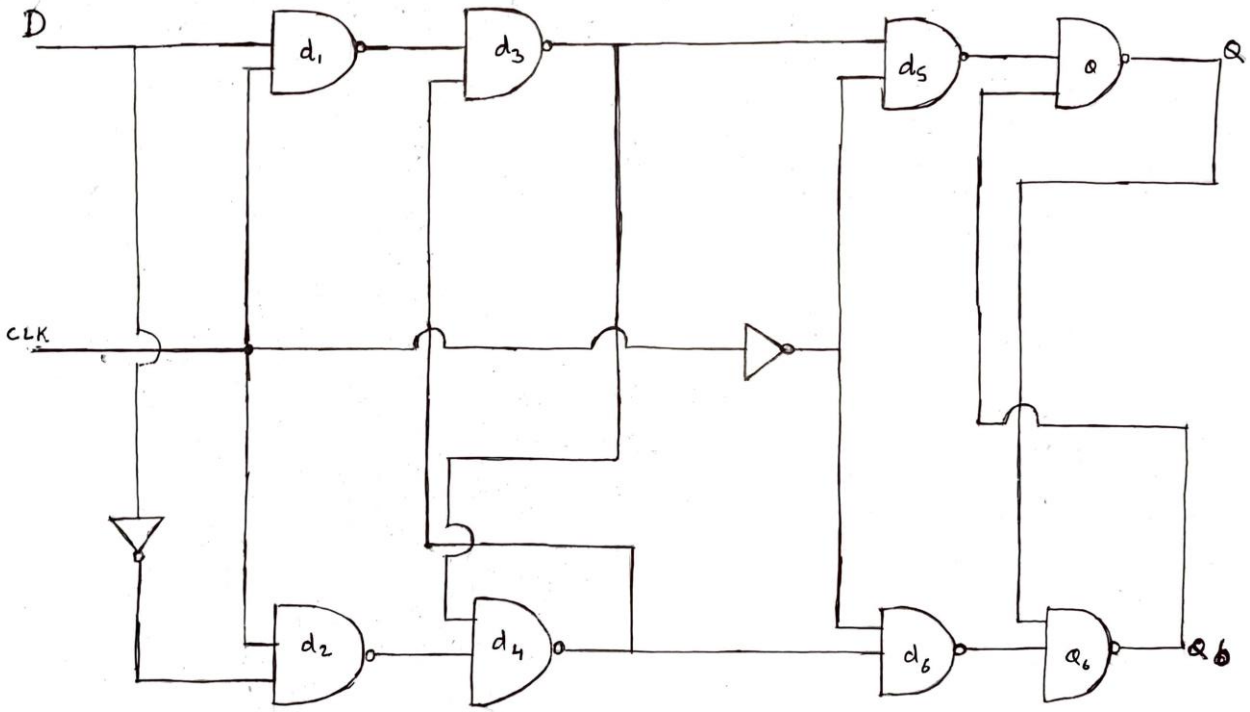
Dr. Vaibhav Neema

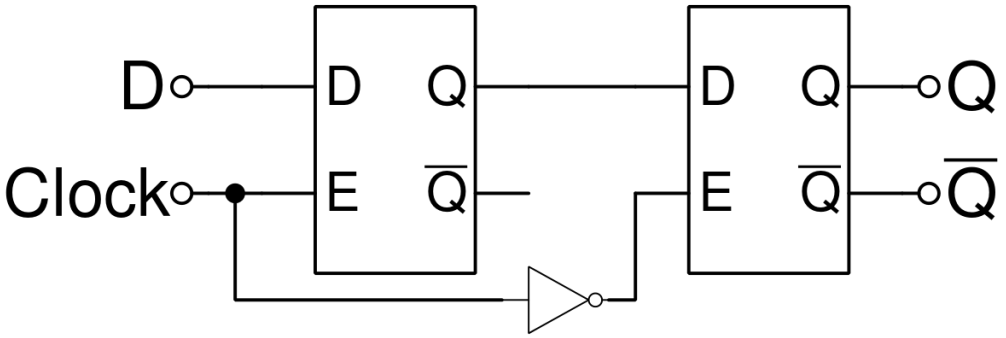
SUBMITTED BY :

Kshitij Chaturvedi (17E7021)

E&I(IV yr) 7th Sem

Negative Edge Triggered D Flip Flop





Negative Edge triggered D Flip Flop

CLK	D	Q	Q_b (Q bar)
0	X	No change	No change
1	0	0	1
1	1	0	1
0	1	1	0
1	0	1	0
0	0	0	1

Table 1: negative edge triggered d flip flop

Test_Bench

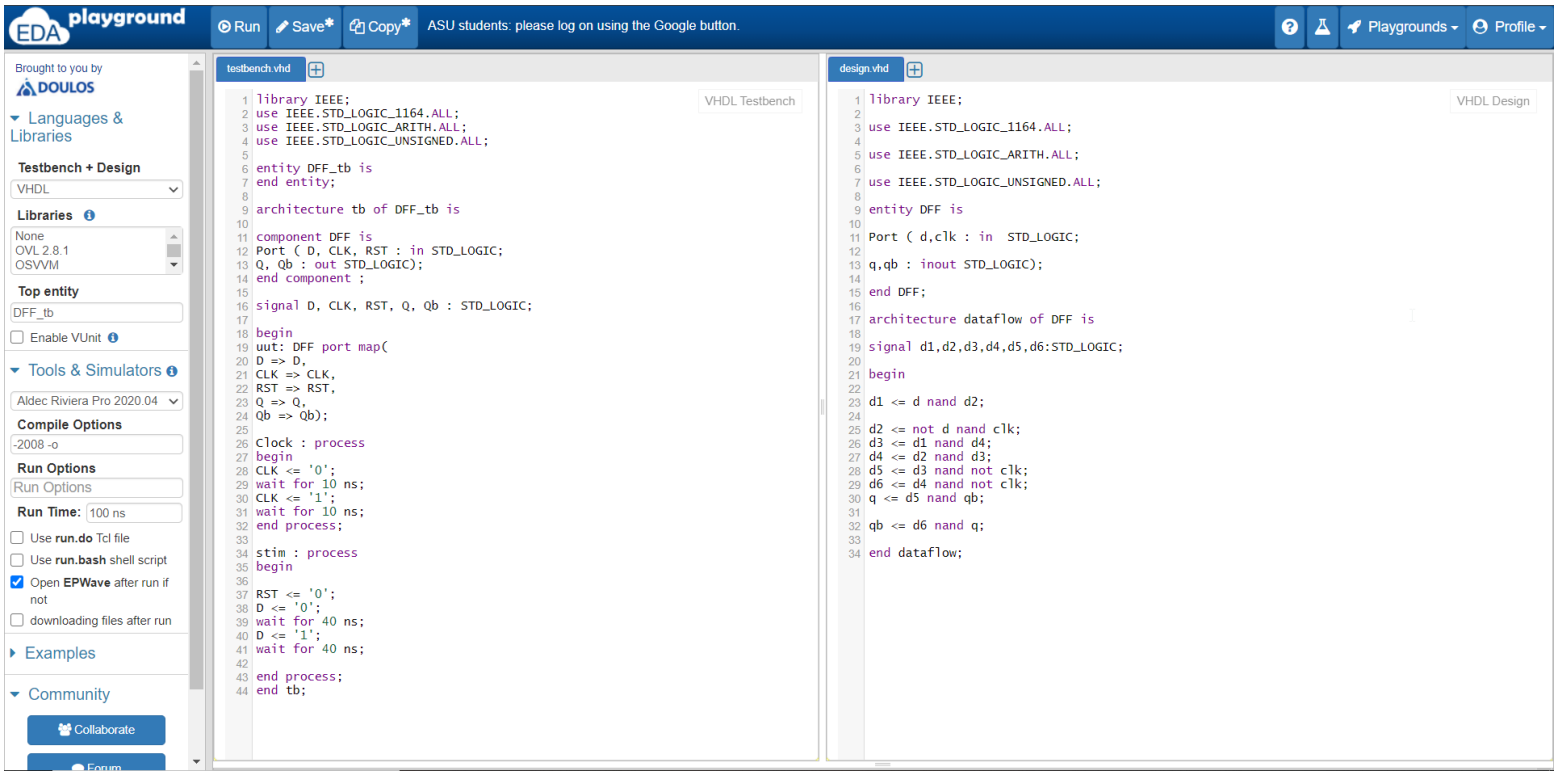
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DFF_tb is
end entity;

architecture tb of DFF_tb is

component DFF is
Port ( D, CLK, RST : in STD_LOGIC;
Q, Qb : out STD_LOGIC);
end component ;

signal D, CLK, RST, Q, Qb : STD_LOGIC;

begin
```

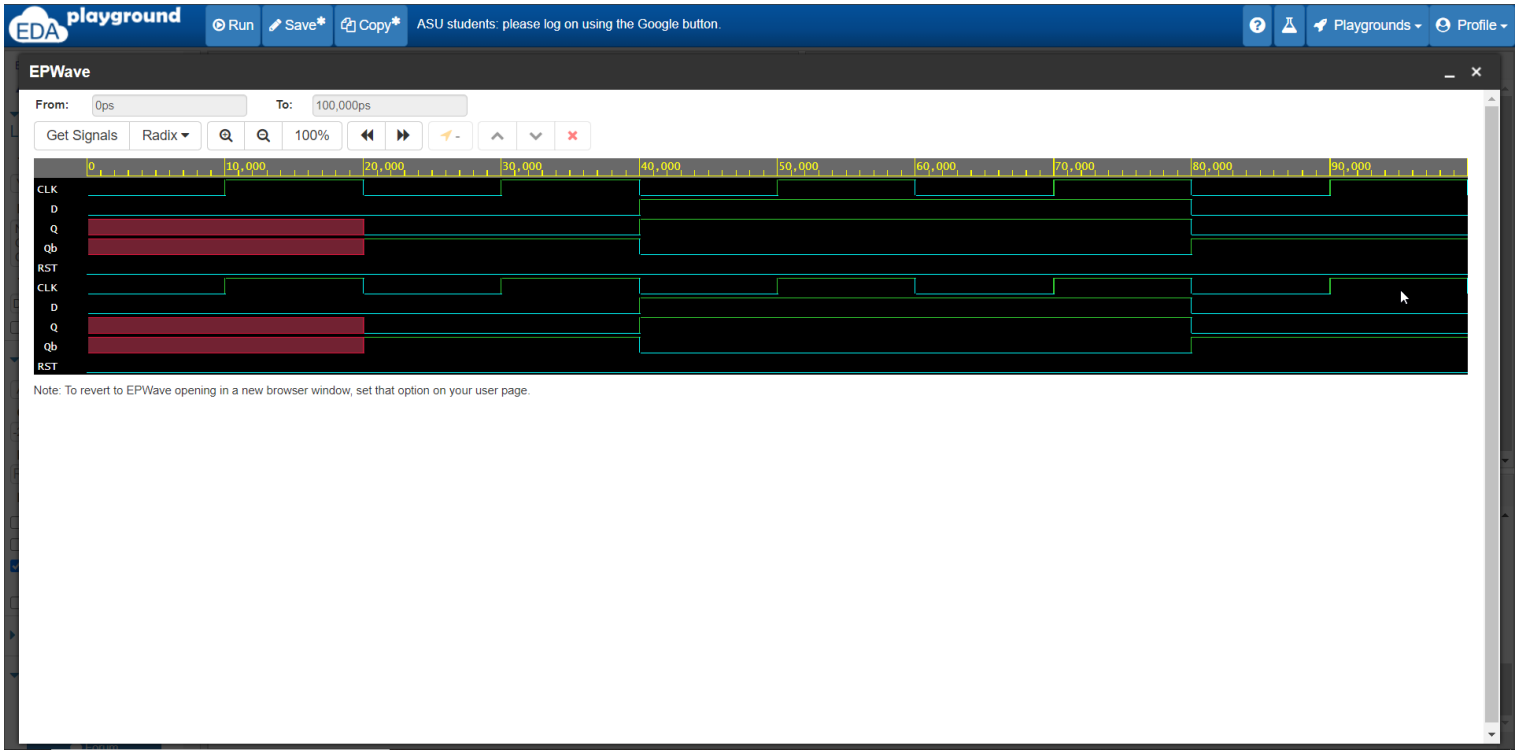
```
uut: DFF port map(
D => D,
CLK => CLK,
RST => RST,
Q => Q,
Qb => Qb);

Clock : process
begin
CLK <= '0';
wait for 10 ns;
CLK <= '1';
wait for 10 ns;
end process;

stim : process
begin

RST <= '0';
D <= '0';
wait for 40 ns;
D <= '1';
wait for 40 ns;

end process;
end tb;
```

Design Code

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DFF is

Port ( d,clk : in  STD_LOGIC;

q,qb : inout STD_LOGIC);

end DFF;

architecture dataflow of DFF is

signal d1,d2,d3,d4,d5,d6:STD_LOGIC;

begin

d1 <= d nand d2;
d2 <= not d nand clk;
d3 <= d1 nand d4;
d4 <= d2 nand d3;
d5 <= d3 nand not clk;
d6 <= d4 nand not clk;
```

```
q <= d5 nand qb;

qb <= d6 nand q;


end dataflow;
```




EDA playground
Run
Save*
Copy*
ASU students: please log on using the Google button.
Playgrounds
Profile
EPWave
From:
0ps
To:
100,000ps
Get Signals
Radix
100%
0
10,000
20,000
30,000
40,000
50,000
60,000
70,000
80,000
90,000
CLK
D
Q
Qb
RST
CLK
D
Q
Qb
RST
Note: To revert to EPWave opening in a new browser window, set that option on your user page.