INSTITUTE OF ENGINEERING AND TECHNOLOGY

CIRCUIT DESIGN USING HDL (EIR7C4)

LAB ASSIGNMENT

SESSION: 2020-2021

TOPIC: 3X8 DECODER USING BEHAVIOURAL MODELLING.

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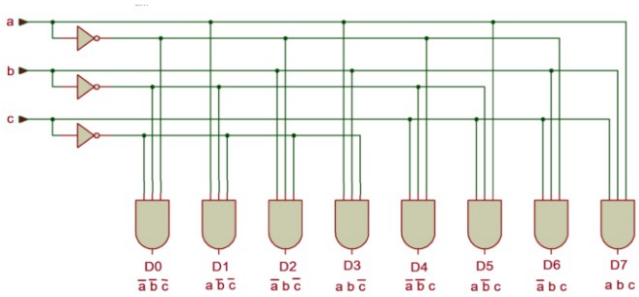
1) 3X8DECODER CIRCUIT DIAGRAM AND TRUTH TABLE:

3×8 Decoder circuit



Truth Table

c	b	a	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

2) SOURCE CODE:

design.vhd

VHDL Design

```
-- Code your design here
library IEEE;
use IEEE.std_logic_1164.all;
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DECODER_SOURCE is

    Port ( I : in  STD_LOGIC_VECTOR (2 downto 0);

           Y : out STD_LOGIC_VECTOR (7 downto 0));

end DECODER_SOURCE;


architecture Behavioral of DECODER_SOURCE is


begin


process (I)


begin


case I is
when "111" => Y<="00000001";
when "110" => Y<="00000010";
when "101" => Y<="00000100";
when "100" => Y<="00001000";
when "011" => Y<="00010000";
when "010" => Y<="00100000";
when "001" => Y<="01000000";

when "000" => Y<="10000000";
when others => null;
end case;
end process;
end Behavioral;
```

3) TEST BENCH:

testbench.vhd

```
-- Code your testbench here
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity decoder_tb is
end entity;

architecture tb of decoder_tb is
component DECODER_SOURCE is
Port ( I : in STD_LOGIC_VECTOR (2 downto 0);
Y : out STD_LOGIC_VECTOR (7 downto 0));
end component;

signal I: STD_LOGIC_VECTOR(2 downto 0);
signal Y: STD_LOGIC_VECTOR(7 downto 0);

begin

uut: DECODER_SOURCE port map(
I => I, Y => Y);

stim: process
begin
I<="111";
wait for 10ms;
I<="110";
wait for 10ms;
I<="101";
wait for 10ms;
I<="100";
wait for 10ms;
I<="011";
wait for 10ms;
I<="010";
wait for 10ms;
I<="001";
wait for 10ms;
I<="000";
wait for 10ms;
wait;
end process;
end tb;
```

4) OUTPUT WAVEFORM: