INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV INDORE

VHDL (EIR7E1)

Lab Viva

SESSION (2020-2021)

SUBMITTED TO-

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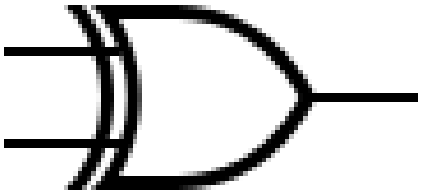
XOR gate



Symbol of xor gate

The Exclusive OR (or XOR) relationship
$F=A \oplus B$ is defined by the truth tables shown below:-

Input		**Output**
A	B	F
0	0	0
0	1	1
1	0	1
1	1	0

Design Code:-

design.vhd

```
1  LIBRARY IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3
4  entity xorgate is
5    PORT (
6       a : in STD_LOGIC;
7        b : in STD_LOGIC;
8        f : out STD_LOGIC);
9  end xorgate;
10
11 architecture dataflow of xorgate is
12 begin
13 f <= a xor b;
14 end dataflow;
15
```

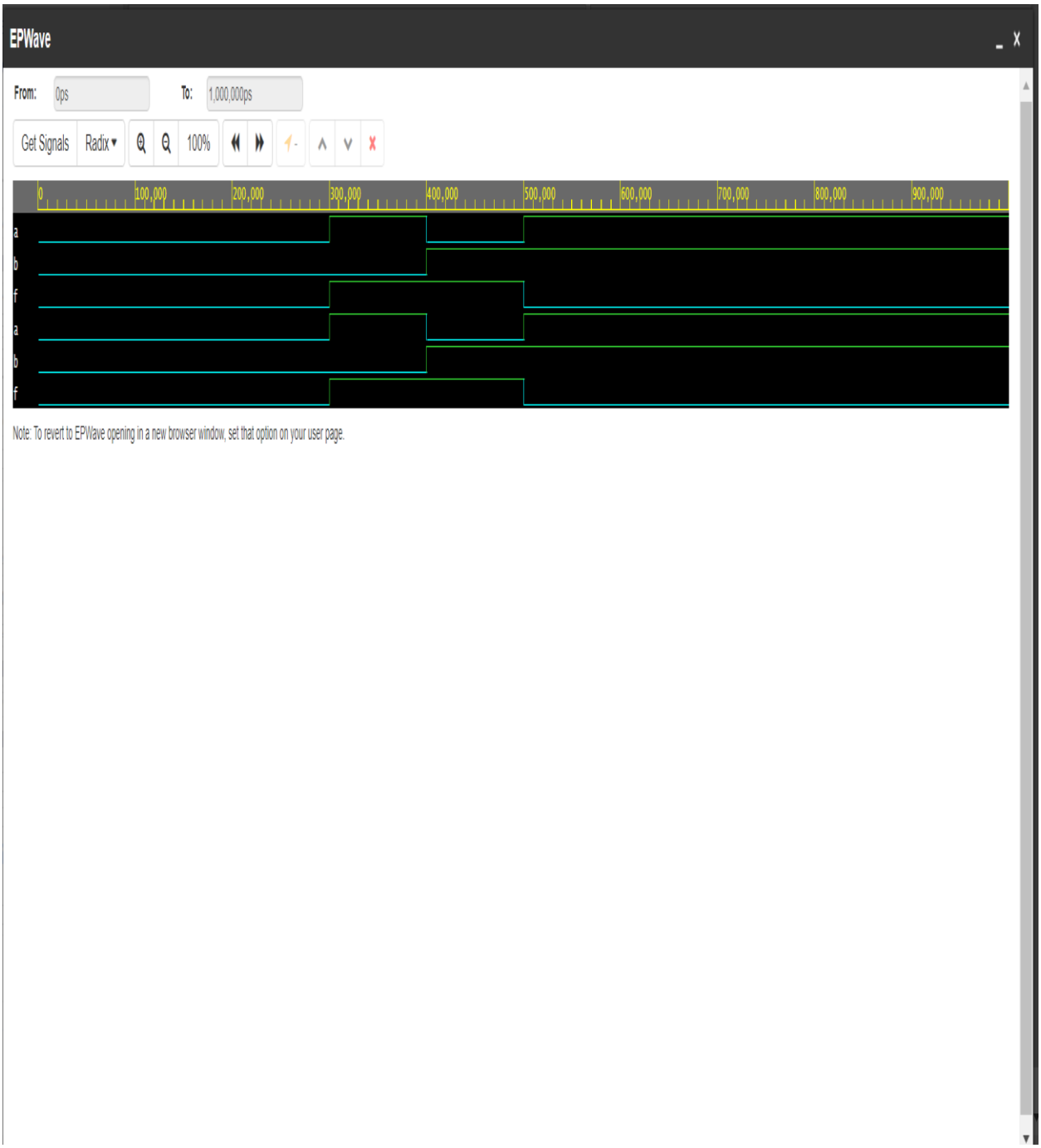
EPWave

Testbench Code:-

testbench.vhd

```
LIBRARY ieee;
 USE ieee.std_logic_1164.ALL;

 ENTITY xor_gate_test IS
 END xor_gate_test;

 ARCHITECTURE dataflow OF xor_gate_test IS

   COMPONENT xorgate
   PORT(
      a : IN std_logic;
      b : IN std_logic;
      f : OUT std_logic
     );
   END COMPONENT;

   signal a : std_logic := '0';
   signal b : std_logic := '0';
   signal f : std_logic;



 BEGIN

   uut: xorgate PORT MAP (
      a => a,
      b => b,
      f => f
     );


   stim_proc: process
       begin

         wait for 100 ns;
               wait for 100 ns;
               a <= '0';
               b <= '0';
               wait for 100 ns;
               a <= '1';
               b <= '0';
               wait for 100 ns;
               a <= '0';
               b <= '1';
               wait for 100 ns;
               a <= '1';
               b <= '1';
         wait;
    end process;
 END dataflow;
```

Output Waveform:-



Link of code:- https://www.edaplayground.com/x/j9p2