INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

Session (2020-21)

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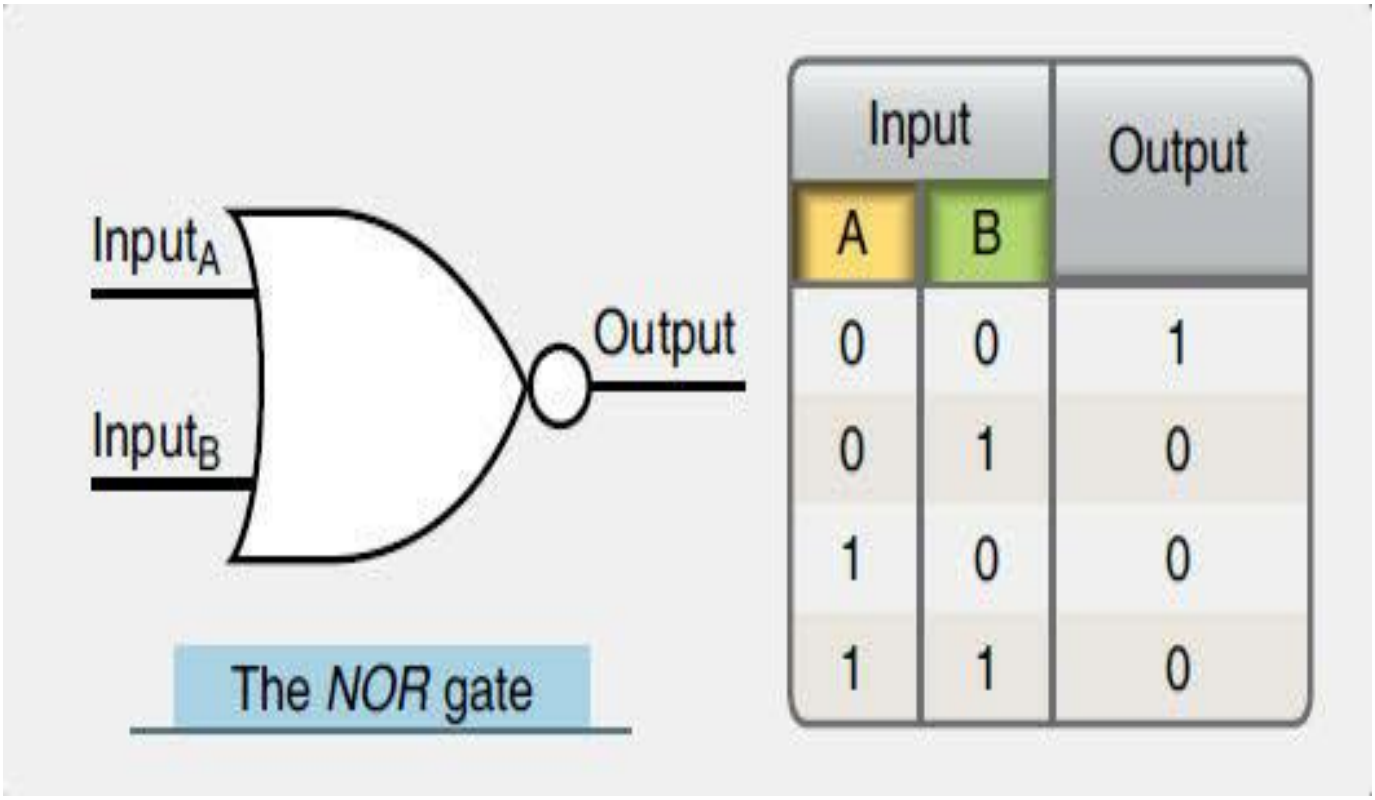
Q. Design NOR code using VHDL language?

Ans.

Circuit of NOR Gate



Input		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	0

Design code for NOR gate :

design.vhd

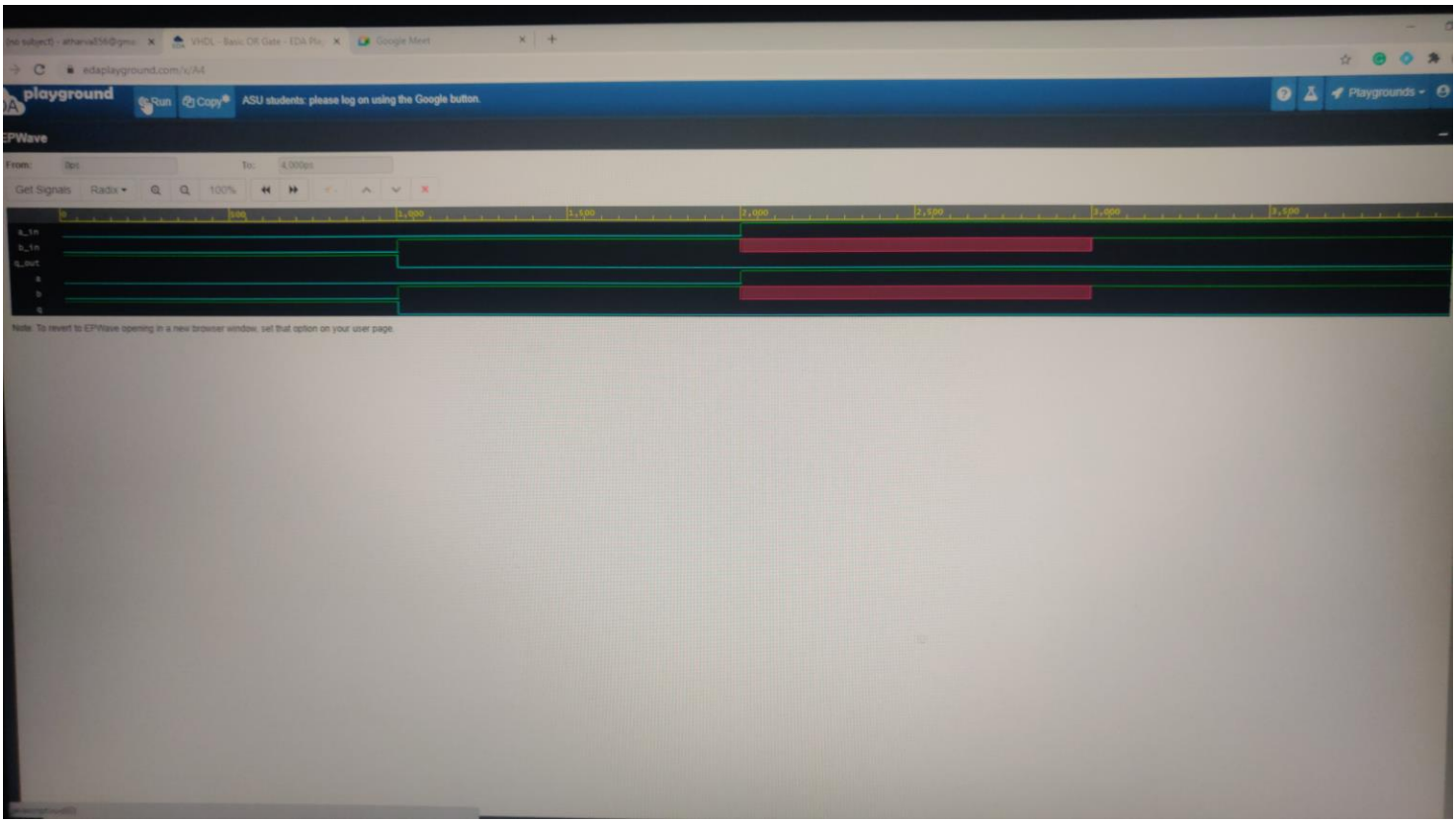
```vhdl
-- Simple OR gate design
library IEEE;
use IEEE.std_logic_1164.all;

entity or_gate is
port(
  a: in std_logic;
  b: in std_logic;
  q: out std_logic);
end or_gate;

architecture rtl of or_gate
is
begin
  process(a, b) is
  begin
    q <= not(a or b);
  end process;
end rtl;

```

Testbench code for NOR gate :

testbench.vhd

```vhdl
-- Testbench for OR gate
library IEEE;
use IEEE.std_logic_1164.all;

entity testbench is
-- empty
end testbench;

architecture tb of testbench
is

-- DUT component
component or_gate is
port(
   a: in std_logic;
   b: in std_logic;
   q: out std_logic);
end component;

signal a_in, b_in, q_out:
std_logic;

begin

   -- Connect DUT
   DUT: or_gate port map(a_in,
b_in, q_out);

   process
   begin
      a_in <= '0';
      b_in <= '0';
      wait for 1 ns;
      assert(q_out='0') report
"Fail 0/0" severity error;

      a_in <= '0';
      b_in <= '1';
      wait for 1 ns;
      assert(q_out='1') report
"Fail 0/1" severity error;

      a_in <= '1';
      b_in <= 'X';
      wait for 1 ns;
      assert(q_out='1') report
"Fail 1/X" severity error;

      a_in <= '1';
      b_in <= '1';
      wait for 1 ns;
      assert(q_out='1') report
"Fail 1/1" severity error;

      -- Clear inputs
      a_in <= '0';
      b_in <= '0';

      assert false report "Test
done." severity note;
      wait;
   end process;
end tb;
```

EP waveform for OR gate :


playground
Run
Copy
ASU students: please log on using the Google button.
Playgrounds
EPWave
From:
To:
Get Signals
Radix
100%
a_in
b_in
q_out
a
b
q
Note: To revert to EPWave opening in a new browser window, set that option on your user page.