INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

Session (2020-21)

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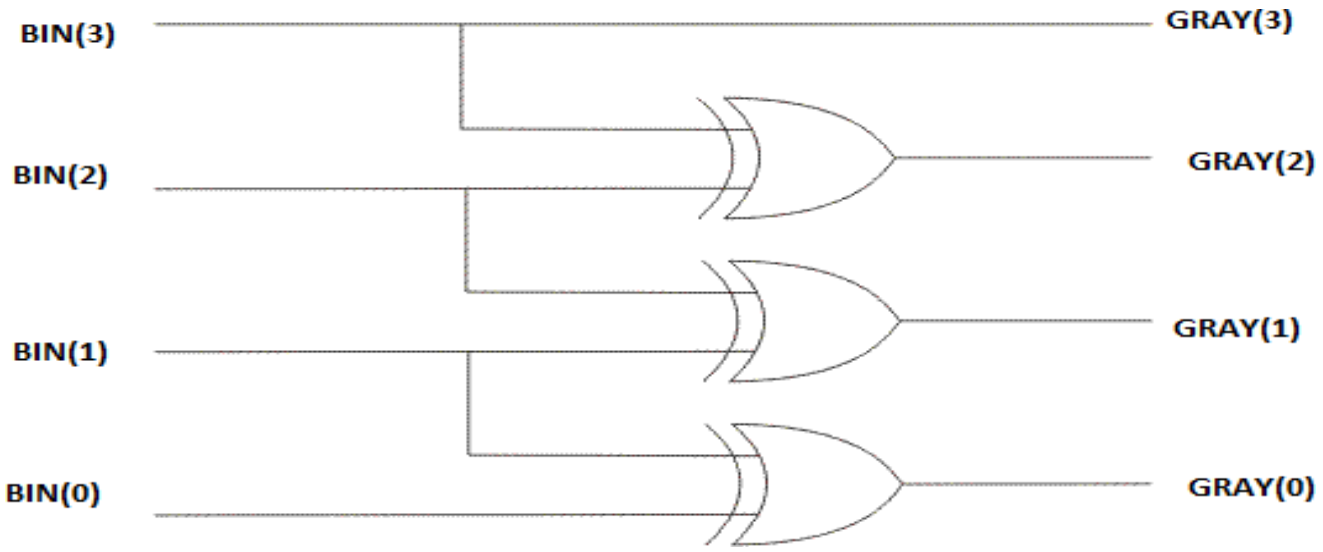
Q. Design of Binary to gray code converter using structure modelling.
Ans.

Circuit of 4 bit binary to gray code converter



Logic used -

GRAY (3) = BIN (3)

GRAY (2) = BIN (3) **XOR** BIN (2)

GRAY (1) = BIN (2) **XOR** BIN (1)

GRAY (0) = BIN (1) **XOR** BIN (0)

Component-

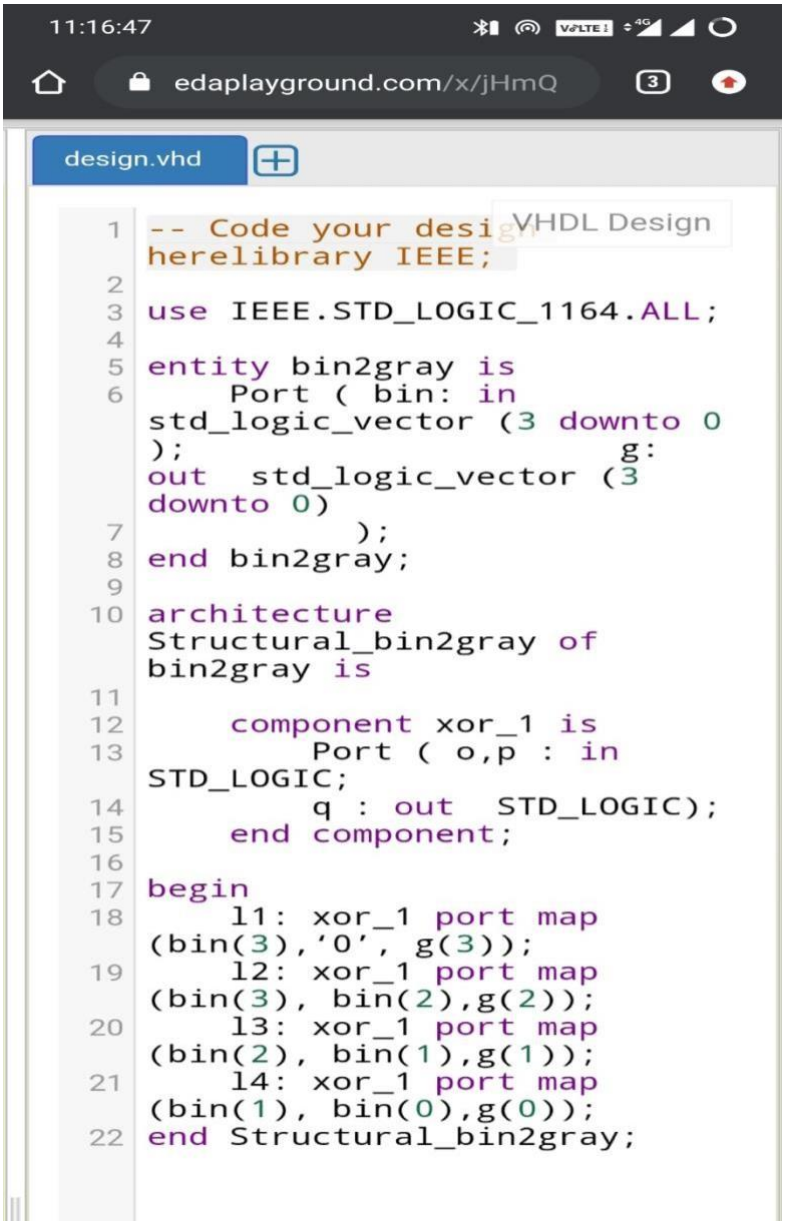
3 XOR gates

Truth Table of Binary to Gray code

BINARY INPUT				*GRAY CODE INPUT*			
B3	*B2*	*B1*	*B0*	*G3*	*G2*	*G1*	*G0*
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Binary to gray code converter in vhdl using structural modelling:

Design code:

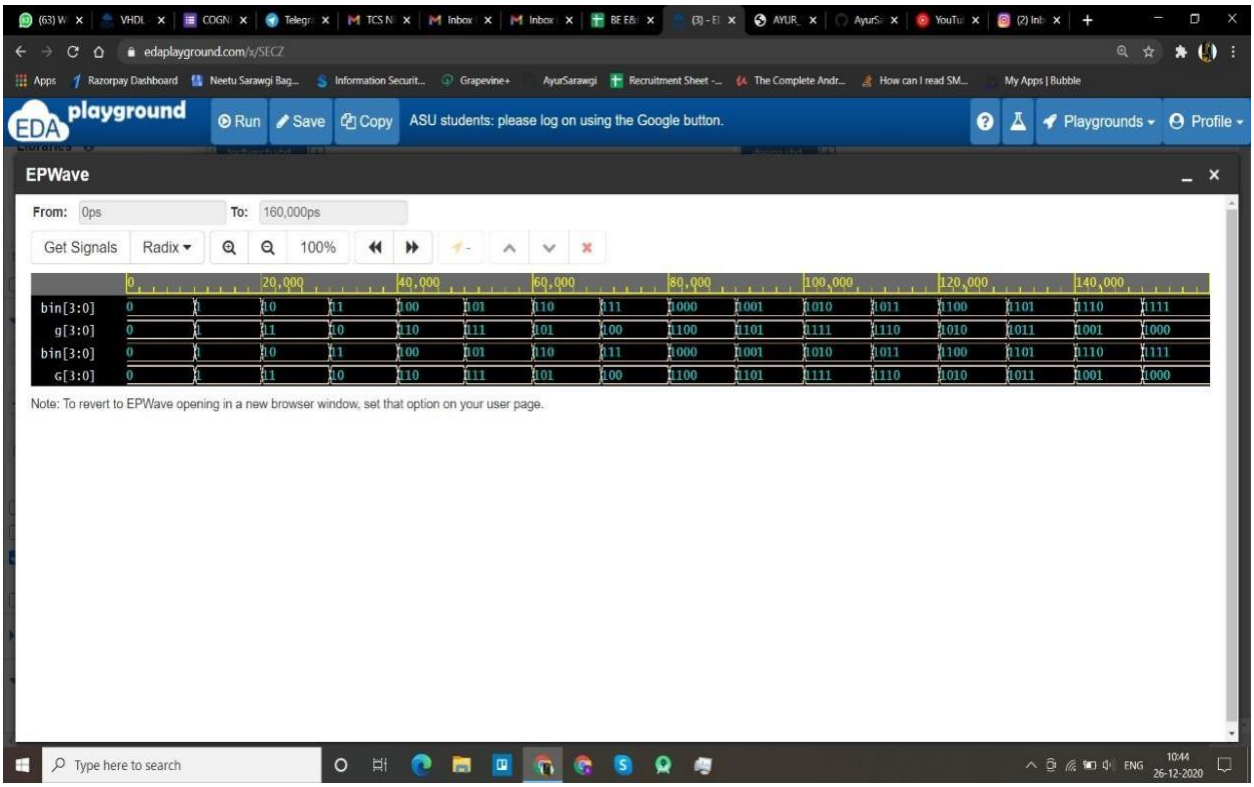


Testbench code:

testbench.vhd

```
-- Code your te VHDL Testbench
library ieee;
use ieee.std_logic_1164.all;

entity tb is
end tb;

architecture behavior of tb
is

    -- component declaration
for the unit under test's
(uut)
component bin2gray is
    port(   bin : in
std_logic_vector(3 downto 0);
            g : out
std_logic_vector(3 downto 0)
            );
end component;

signal bin,g:
std_logic_vector(3 downto 0)
:= (others=>'0');

begin
    -- instantiate the unit
under test's (uut)
   uut1: bin2gray port map (
          bin => bin,
          g => g
        );


   -- stimulus process
   stim_proc: process
   begin
        bin <= "0000";
wait for 10 ns;
        bin <= "0001";  wait
for 10 ns;
        bin <= "0010";  wait
for 10 ns;
        bin <= "0011";  wait
for 10 ns;
        bin <= "0100";
wait for 10 ns;
        bin <= "0101";  wait
for 10 ns;
        bin <= "0110";  wait
for 10 ns;
        bin <= "0111";  wait
for 10 ns;
        bin <= "1000";
wait for 10 ns;
        bin <= "1001";  wait
for 10 ns;
        bin <= "1010";  wait
for 10 ns;
        bin <= "1011";  wait
for 10 ns;
        bin <= "1100";
wait for 10 ns;
        bin <= "1101";  wait
for 10 ns;
        bin <= "1110";  wait
for 10 ns;
        bin <= "1111";  wait
for 10 ns;
      wait;
   end process;

end;
```

EP waveform:


edaplayground.com/x/5ECZ
playground
Run
Save
Copy
ASU students: please log on using the Google button.
Playgrounds
Profile
EPWave
From: 0ps
To: 160,000ps
Get Signals
Radix
100%
0
20,000
40,000
60,000
80,000
100,000
120,000
140,000
bin[3:0]
g[3:0]
bin[3:0]
G[3:0]
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
Type here to search
ENG
10:44
26-12-2020