INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

(Lab Assignment)

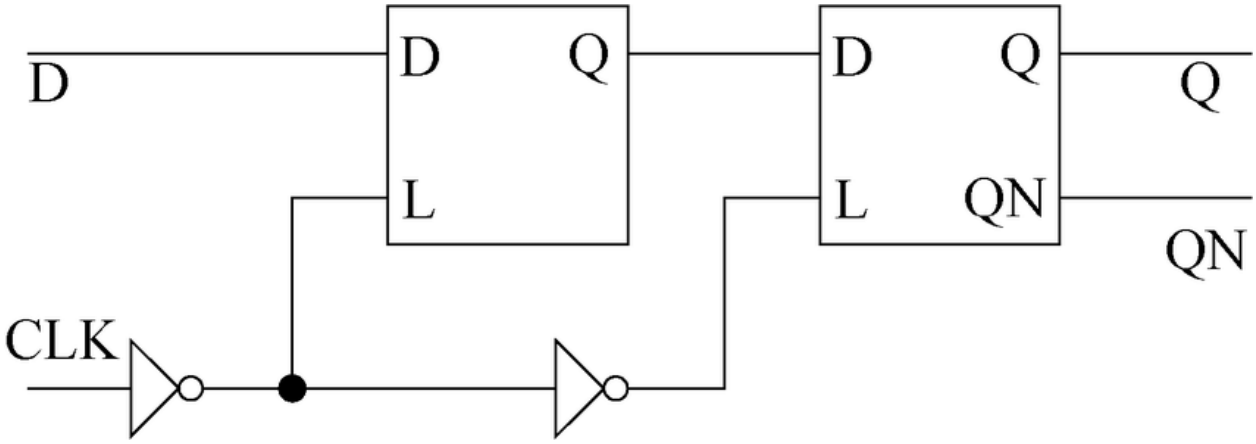
Session (2020-21)

Submitted to:
Dr. Vaibhav Neema

Submitted by
VIDHI SHARMA
E&I (7th Sem)
Roll no. 17E7056
Enroll no. DE17247

DESIGN OF POSITIVE EDGE TRIGGERED D FLIP FLOP (DATAFLOW MODELLING)

Circuit Diagram



Truth Table

Clk	Q(t-1)	D	Q(t)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Testbench Code

testbench.vhd

VHDL Testbench

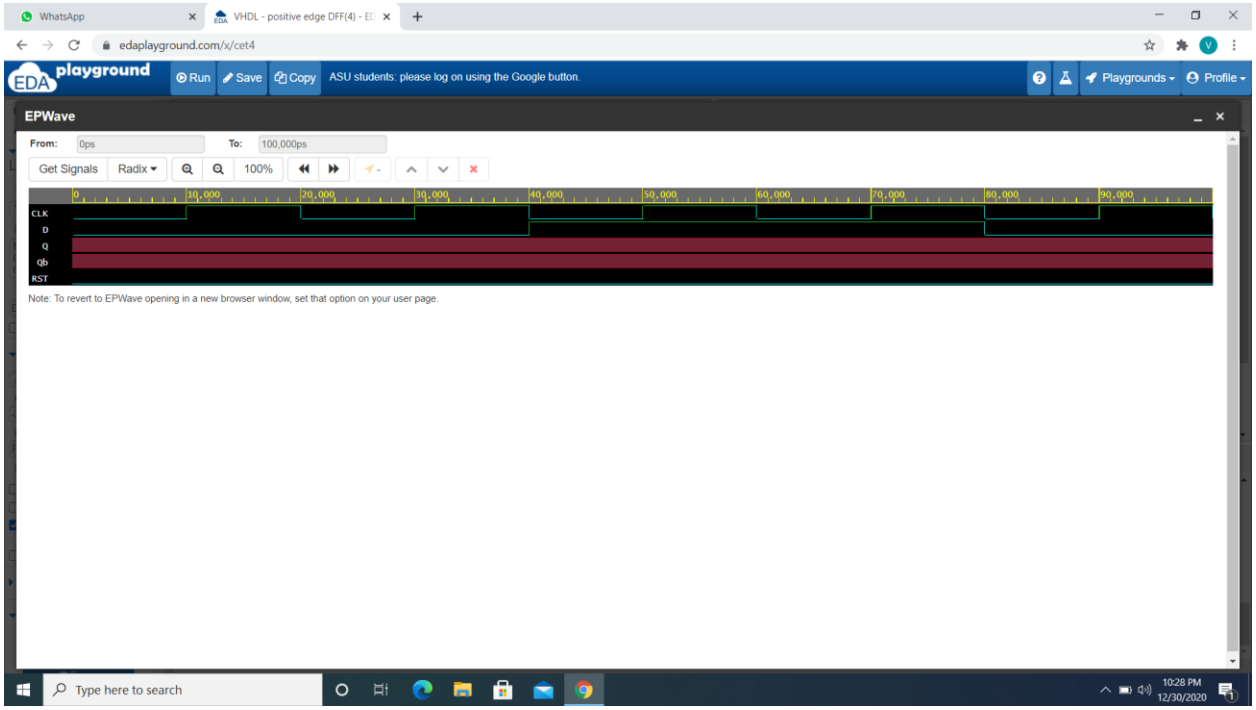
```
-- Testbench for OR gate
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DFF_tb is
end entity;

architecture tb of DFF_tb is

component DFF is
Port ( D, CLK, RST : in STD_LOGIC;
Q, Qb : out STD_LOGIC);
end component ;

signal D, CLK, RST, Q, Qb : STD_LOGIC;

begin
uut: DFF port map(
D => D,
CLK => CLK,
RST => RST,
Q => Q,
Qb => Qb);

Clock : process
begin
CLK <= '0';
wait for 10 ns;
CLK <= '1';
wait for 10 ns;
end process;

stim : process
begin

RST <= '0';
D <= '0';
wait for 40 ns;
D <= '1';
wait for 40 ns;

end process;
end tb;
```

Source Code

design.vhd

```
-- Simple OR gate design
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.STD_LOGIC_ARITH.ALL;

use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity DFF is

Port ( d,clk : in  STD_LOGIC;

q,qb : inout STD_LOGIC);

end DFF;

architecture dataflow of DFF is

signal d1,s1,r1:STD_LOGIC;

begin

s1 <= d nand clk;

d1 <= d nand d;

r1 <= d1 nand clk;

q <= s1 nand qb;

qb <= r1 nand q;

end dataflow;
```

Waveform


WhatsApp
VHDL - positive edge DFF(4) - ED
edaplayground.com/x/cet4
EDA playground
Run
Save
Copy
ASU students: please log on using the Google button.
Playgrounds
Profile
EPWave
From:
0ps
To:
100,000ps
Get Signals
Radix
100%
0
10,000
20,000
30,000
40,000
50,000
60,000
70,000
80,000
90,000
CLK
D
Q
Qb
RST
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
Type here to search
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12/30/2020