INSTITUTE OF ENGINEERING & TECHNOLOGY

Devi Ahilya Vishwavidyalaya

INDORE

Department of E&I ENGINEERING

SESSION: 2017-2021

Subject: VLSI

17E7053

SUBMITTED TO:	SUBMITTED BY:
Vaibhav Neema sir	Tanay Paliwal

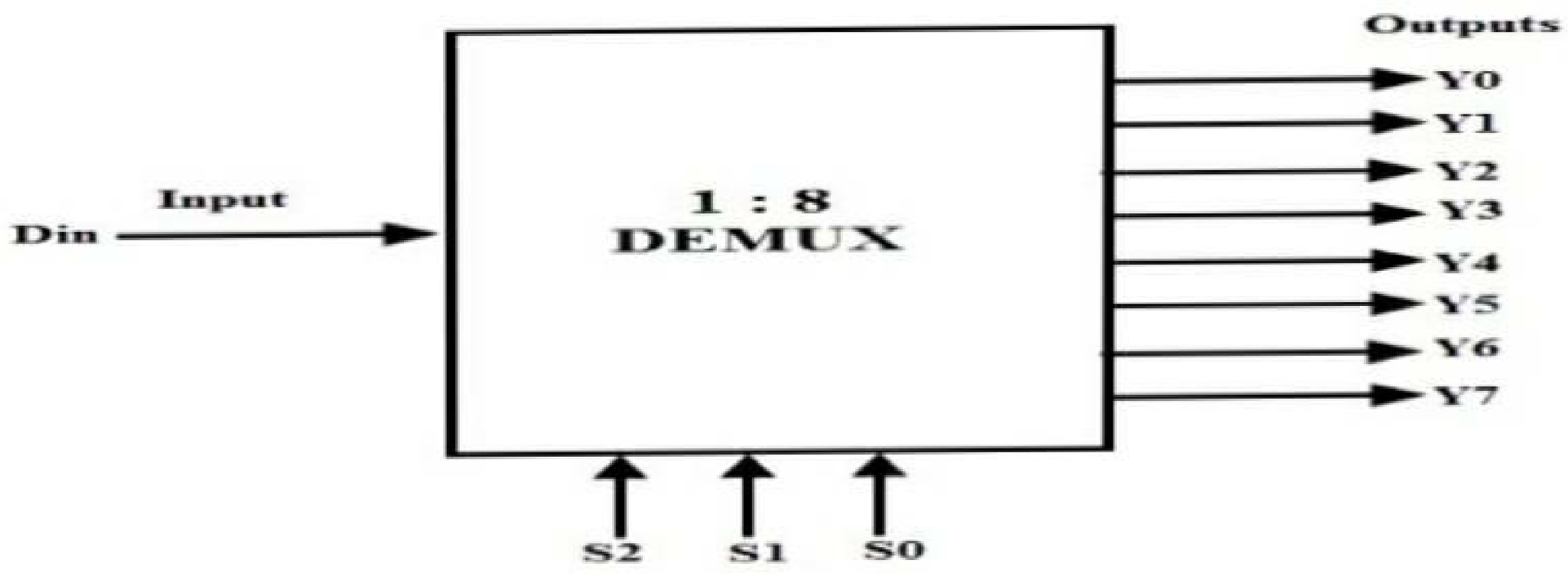
1-8 DEMUX

The process of getting information from one input and transmitting the same over one of many outputs is called demultiplexing. A demultiplexer is a combinational logic circuit that receives the information on a single input and transmits the same information over one of 2n possible output lines.

Demultiplexers are also called as data distributors, since they transmit the same data which is received at the input to different destinations.

The below figure shows the block diagram of a 1-to-8 demultiplexer that consists of single input D, three select inputs S2, S1 and S0 and eight outputs from Y0 to Y7.

It is also called as 3-to-8 demultiplexer due to three select input lines. It distributes one input line to one of 8 output lines depending on the combination of select inputs.



The truth table for this type of demultiplexer is shown below. The input D is connected with one of the eight outputs from Y0 to Y7 based on the select lines S2, S1 and S0.

Data Input	Select Inputs			Outputs							
D	S_2	S_1	S_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
D	0	0	0	0	0	0	0	0	0	0	D
D	0	0	1	0	0	0	0	0	0	D	0
D	0	1	0	0	0	0	0	0	D	0	0
D	0	1	1	0	0	0	0	D	0	0	0
D	1	0	0	0	0	0	D	0	0	0	0
D	1	0	1	0	0	D	0	0	0	0	0
D	1	1	0	0	D	0	0	0	0	0	0
D	1	1	1	D	0	0	0	0	0	0	0

Boolean expressions for all the outputs can be written as follows.

$$Y0 = D\ \overline{S2}\ \overline{S1}\ \overline{S0}$$

$$Y1 = D\ \overline{S2}\ \overline{S1}\ S0$$

$$Y2 = D\ \overline{S2}\ S1\ \overline{S0}$$

$$Y3 = D\ \overline{S2}\ S1\ S0$$

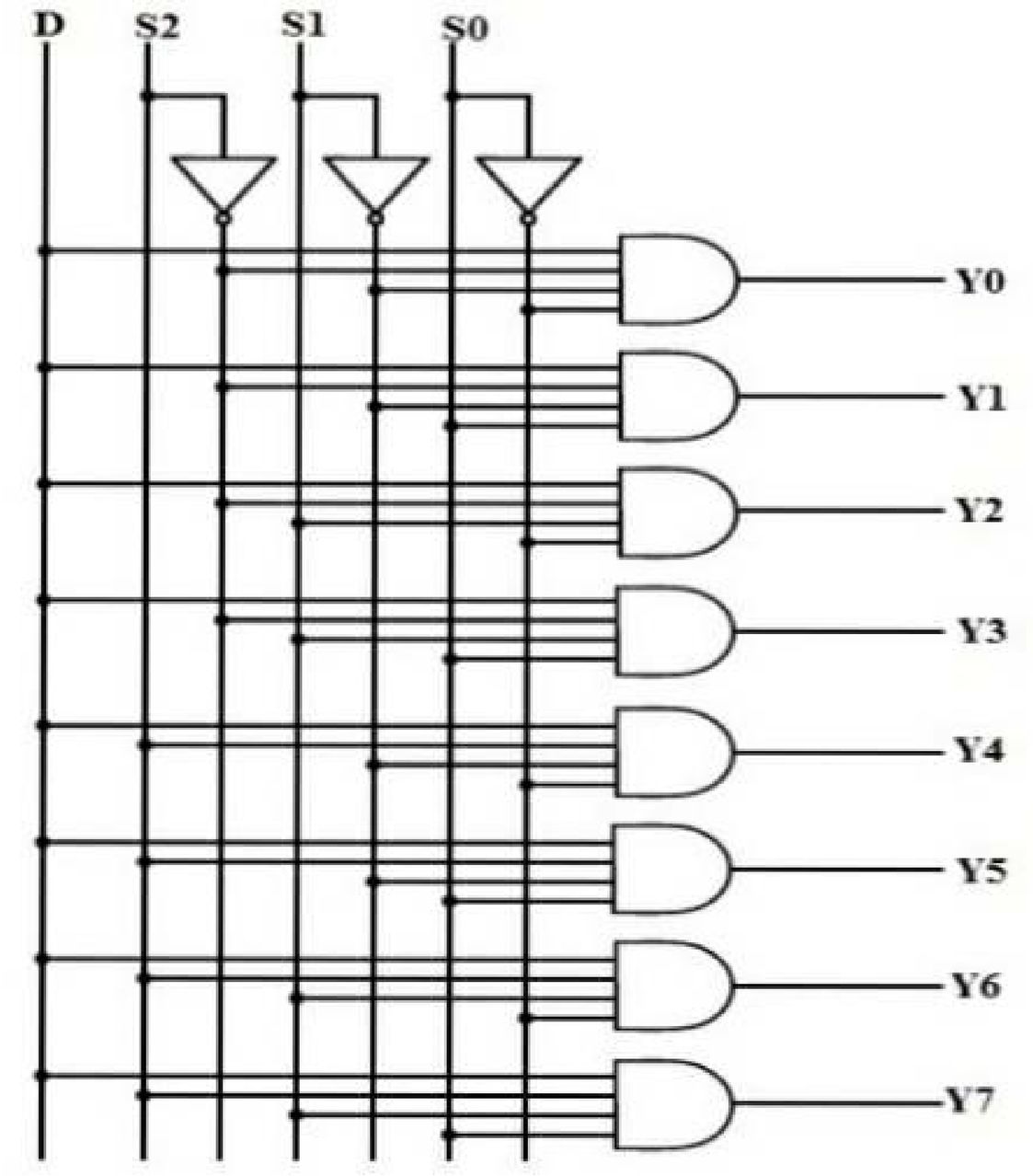
$$Y4 = D\ S2\ \overline{S1}\ \overline{S0}$$

$$Y5 = D\ S2\ \overline{S1}\ S0$$

$$Y6 = D\ S2\ S1\ \overline{S0}$$

$$Y7 = D\ S2\ S1\ S0$$

From these obtained equations, the logic diagram of this demultiplexer can be implemented by using eight AND gates and three NOT gates as shown in below figure. The different combinations of the select lines , select one AND gate at given time , such that data input will appear at a particular output.



None
OVL 2.8.1
OSVVM

Top entity

demux_tb

Enable VUnit

Tools & Simulators

Aldec Riviera Pro 2020.04

Compile Options

-2008 -o

Run Options

Run Options

Run Time: 200ns

Use run.do Tcl file

Use run.bash shell script

Open EPWave after run if not

downloading files after run

Examples

Community

Collaborate

Forum

Follow @edaplayground

testbench.vhd

VHDL Testbench

```
1  library IEEE;
2  use IEEE.std_logic_1164.all;
3  entity demux_tb is
4  end entity;
5  architecture demux1_8 of demux_tb is
6  component dmux1_8 is
7  port( din : in STD_LOGIC;
8        s : in STD_LOGIC_VECTOR (2 downto 0);
9        y : out STD_LOGIC_VECTOR (7 downto 0));
10 end component;
11 signal din : STD_LOGIC;
12 signal s: STD_LOGIC_VECTOR (2 downto 0);
13 signal y: STD_LOGIC_VECTOR (7 downto 0);
14 begin
15 uut: dmux1_8 port map(         din => din,
16 s => s,
17 y => y);
18 stim: process
19 begin
20
```

design.vhd

```
1  library IEEE;
2
3  use IEEE.STD_LOGIC_1164.ALL;
4
5  use IEEE.STD_LOGIC_ARITH.ALL;
6
7  use IEEE.STD_LOGIC_UNSIGNED.ALL;
8
9  entity demux1_8 is
10
11 port( f : in std_logic;
12
13       s: in std_logic_vector(2 downto 0);
14
15       y: out std_logic_vector(7 downto 0));
16
17 end demux1_8;
18
19 architecture demux1_8 of demux1_8 is
20 begin
```

Log | Share

```
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 5399 kB (elbread=427 elab2=4829 kernel=142 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: stopped at time: 200 ns
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2020-12-28 11:55:52 EST] Opening EPWave...
Done
```

EPWave

playground

Run | Save* | Copy* | ASU students: please log on using the Google button. | Playgrounds | Profile

None
OVL 2.8.1
OSVVM

Top entity

demux_tb

Enable VUnit

Tools & Simulators

Aldec Riviera Pro 2020.04

Compile Options

2008 -o

Run Options

Run Options

Run Time: 200ns

Use run.do Tcl file

Use run.bash shell script

Open EPWave after run if not

downloading files after run

Examples

Community

Collaborate

Forum

Follow @edaplayground

testbench.vhd

VHDL Testbench

```
signal y: STD_LOGIC_VECTOR (7 downto 0);
begin
uut: dmux1_8 port map(         din => din,
s => s,
y => y);
stim: process
begin

 din <= '1';
s <= "000"; wait for 20 ns;
s <= "001"; wait for 20 ns;
s <= "010"; wait for 20 ns;
s <= "011"; wait for 20 ns;
s <= "100"; wait for 20 ns;
s <= "101"; wait for 20 ns;
s <= "110"; wait for 20 ns;
s <= "111"; wait for 20 ns;
wait;
end process;
end demux1_8;
```

design.vhd

```

port( f : in std_logic;

      s: in std_logic_vector(2 downto 0);

      y: out std_logic_vector(7 downto 0));

end demux1_8;

architecture demux1_8 of demux1_8 is
begin
     y(0)<=f when s="000"else'0';
     y(1)<=f when s="001"else'0';
     y(2)<=f when s="010"else'0';
     y(3)<=f when s="011"else'0';
     y(4)<=f when s="100"else'0';
     y(5)<=f when s="101"else'0';
     y(6)<=f when s="110"else'0';
     y(7)<=f when s="111"else'0';
end demux1_8;
```

Log | Share

```
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 5399 kB (elbread=427 elab2=4829 kernel=142 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# KERNEL: stopped at time: 200 ns
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2020-12-28 11:55:52 EST] Opening EPWave...
Done
```