INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV

INDORE

ELECTRONICS & INSTRUMENTATION ENGINEERING

CIRCUIT DESIGN USING HDL(EIR7E1)

LAB VIVA

Session: 2020-21

SUBMITTED TO:

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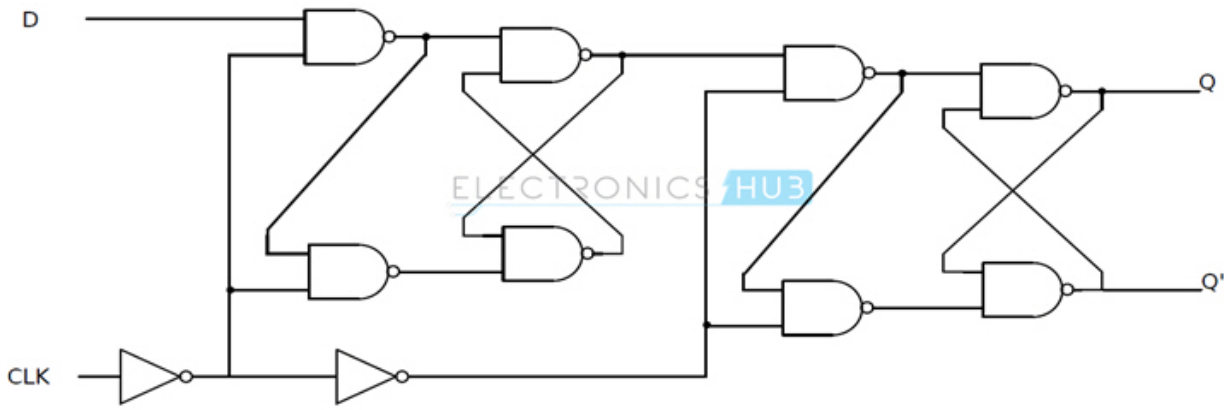
Positive Edge D Flip Flop

The Master slave D flip flop shown below is a positive edge triggered device that means it will operate when clock input has raising edge. The first flip flop (master flip – flop) is connected with a negative clock signal i.e. Inverted and the second flip – flop (slave flip – flop) is connected with double inverse of clock signal i.e. normal clock signal.



Truth Table:

Functional Table

D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

Design Code

Run | Save | Copy | ASU students: please log on using the Google button.

design.vhd

```
Library ieee;
use ieee.std_logic_1164.all;

Entity ip2_nand is
Port ( a,b:in std_logic;
       op:out std_logic);
End entity;

Architecture da of ip2_nand is
begin
      Op<=a nand b;
End architecture;

Library ieee;
use ieee.std_logic_1164.all;

entity d_latch is
Port(clk,d:in std_logic;
     q,qbar:out std_logic);
End entity;

Architecture rch of d_latch is
signal p1,p2,p3,q1,q2:std_logic;

component ip2_nand is
Port ( a,b:in std_logic;
       op:out std_logic);
End component;
Begin
U1: ip2_nand port map (clk,d,p1);
U2: ip2_nand port map (d,d,p3);
U3: ip2_nand port map (clk,p3,p2);
U4: ip2_nand port map (p1,q2,q1);
U5: ip2_nand port map (q1,p2,q2);
q<=q1;
qbar<=q2;
```

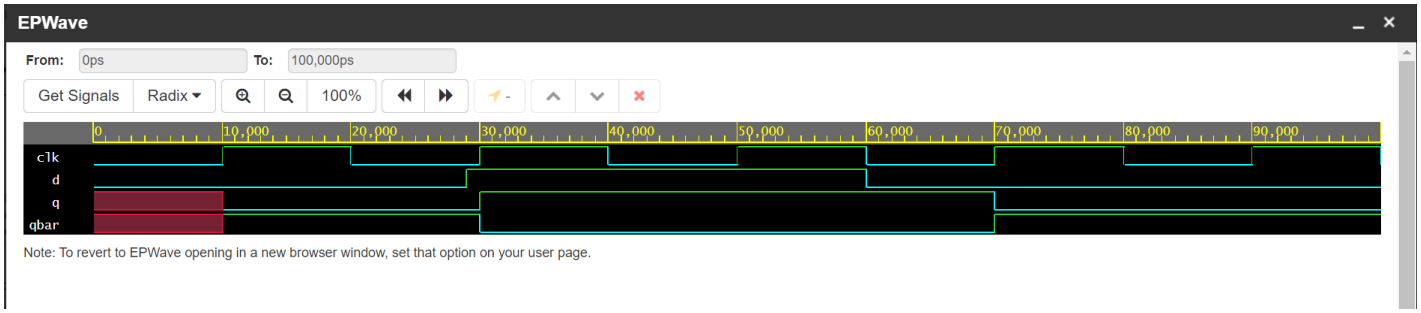
```
Library ieee;
use ieee.std_logic_1164.all;

entity my_dff is
Port (clk,d:in std_logic;
     q,qbar:out std_logic);
End entity;

Architecture rch of my_dff is
Signal q1,q2,q3:std_logic;

component ip2_nand is
Port ( a,b:in std_logic;
       op:out std_logic);
End component;

component d_latch is
Port(clk,d:in std_logic;
     q,qbar:out std_logic);
End component;

Begin
master   : d_latch port map (q3,d,q1,q2);
nand4not : ip2_nand port map (clk,clk,q3);
slave    : d_latch port map (clk,q1,q,qbar);
End rch;
```

Test-Bench Code

testbench.vhd

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity dff_tb is
5  end entity;
6
7  architecture tb of dff_tb is
8
9  component my_dff is
10 Port (clk,d : in std_logic;
11     q, qbar : out std_logic);
12 end component ;
13
14 signal d, clk,q, qbar : std_logic;
15
16 begin
17 dut: my_dff port map (clk,d,q,qbar);
18 Clock : process
19 begin
20 clk <= '0';
21 wait for 10 ns;
22 clk <= '1';
23 wait for 10 ns;
24 end process;
25
26 stim : process
27 begin
28
29 d <= '0';
30 wait for 29 ns;
31 d <= '1';
32 wait for 31 ns;
33 d <= '0';
34 wait for 42 ns;
35 d <= '1';
36 wait for 23 ns;
37
38 end process;
39 end tb;
```

OUTPUT Waveform



EDA Playground link:

https://www.edaplayground.com/x/B4yA