INSTITUTE OF ENGINEERING AND TECHNOLOGY, INDORE

CIRCUIT DESIGN USING HDL (EIR7C4)

Session (2020-21)

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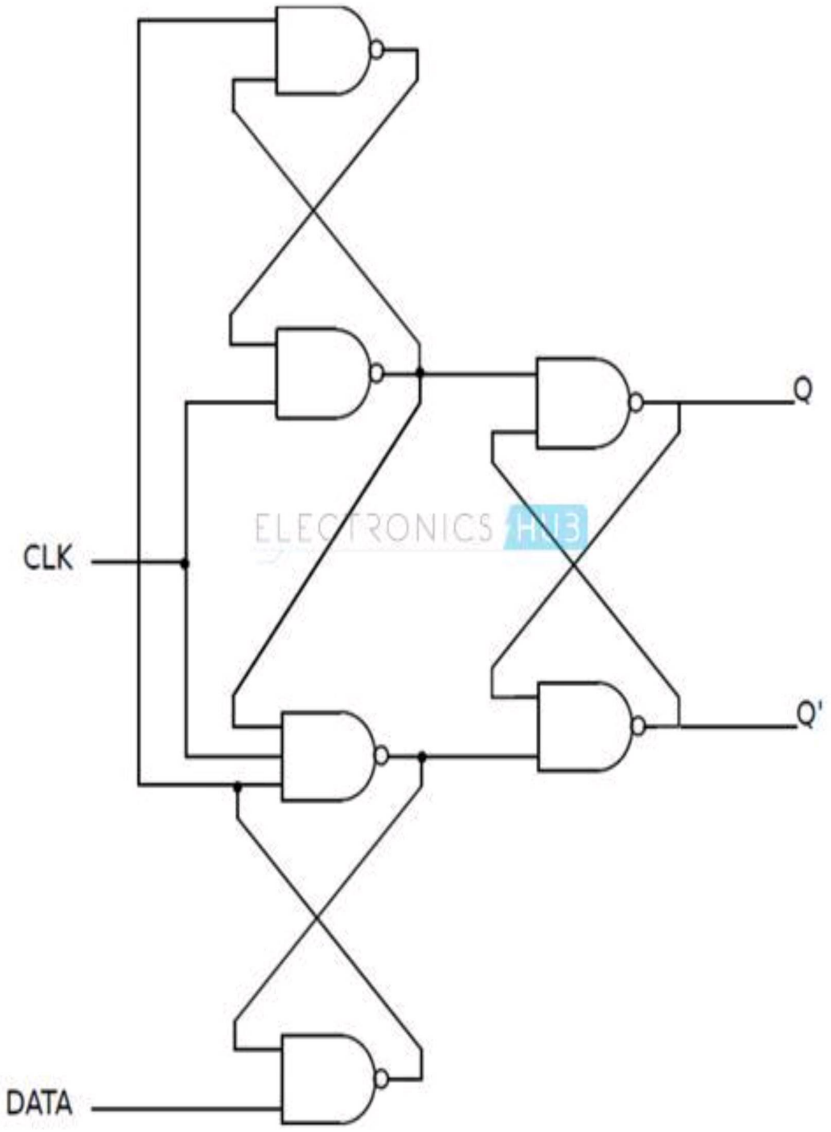
Q. Design of negative edge DFF using behavioral modelling.
Ans.

Circuit of negative edge DFF



Truth Table of negative edge DFF

clk	D	Q	Q̄
↑	0	0	1
↑	1	0	1
↑	0	0	1
↓	1	1	0
↓	0	0	1

Testbench code of negative edge DFF

testbench.vhd

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY DFF_tb IS
END DFF_tb;

ARCHITECTURE behavior OF DFF_tb IS
 COMPONENT DFF
 PORT(
 din : IN std_logic;
 clk : IN std_logic;
 rst : IN std_logic;
 dout : OUT std_logic
 );
 END COMPONENT;

 signal din : std_logic := '0';
 signal clk : std_logic := '0';
 signal rst : std_logic := '1';
 signal dout : std_logic;
 constant clk_period : time := 10 ns;

BEGIN
 uut: DFF PORT MAP (
 din => din,
 clk => clk,
 rst => rst,
 dout => dout
 );

 clk_process :process
 begin
```

testbench.vhd

```
    for i in 1 to 24 loop
     clk <= '0';
     wait for 1.25 ns;
     clk <= '1';
     wait for 1.25 ns;

     end loop;
     wait;
end process;

stim_proc: process
begin
    rst <= '1';
    din <= '0';
    wait for 10 ns;

    rst <= '1';
    din <= '1';
    wait for 10 ns;

    rst <= '0';
    din <= '0';
    wait for 10 ns;

    rst <= '0';
    din <= '1';
    wait for 10 ns;

    rst <= '1';
    din <= '1';
    wait for 10 ns;

```

testbench.vhd

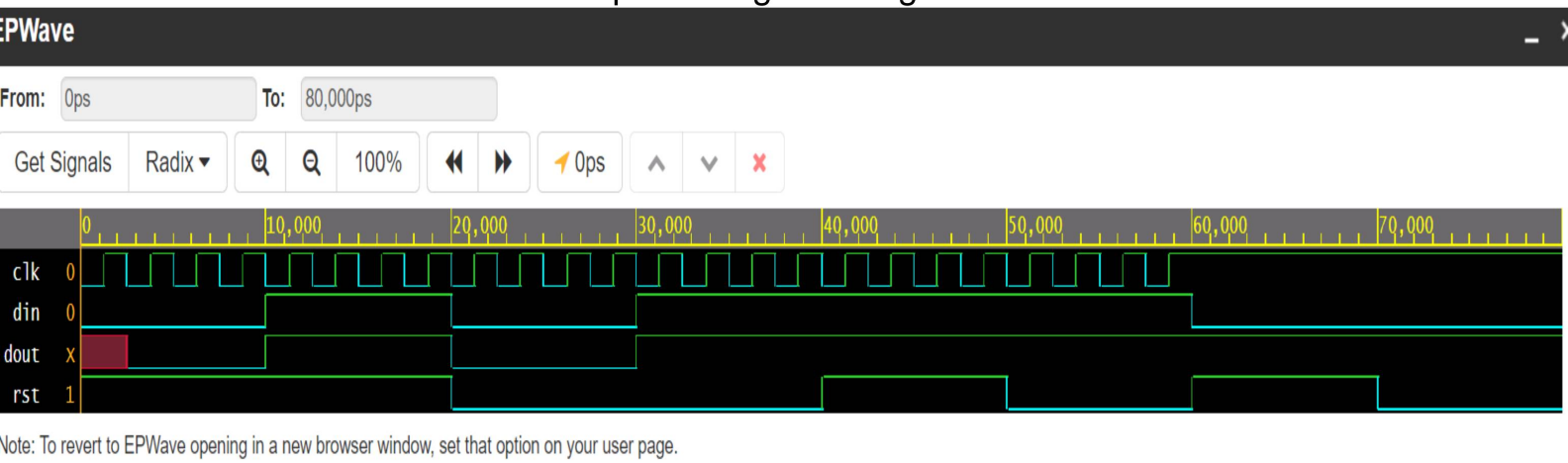
```
    wait for 10 ns;

    rst <= '1';
    din <= '1';
    wait for 10 ns;

    rst <= '0';
    din <= '1';
    wait for 10 ns;

    rst <= '1';
    din <= '0';
    wait for 10 ns;

    rst <= '1';
    din <= '1';
    wait for 10 ns;

    rst <= '0';
    din <= '0';
    wait for 10 ns;

    rst <= '0';
    din <= '0';
    wait for 10 ns;

wait;

end process;
END;

```

Design code of negative edge DFF

design.vhd

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity DFF is
5  port(
6      din: in std_logic;
7      clk: in std_logic;
8      rst: in std_logic;
9      dout: out std_logic
10     );
11 end DFF;
12
13 architecture behavioral of DFF is
14 begin
15
16 process(rst,clk,din)
17 begin
18
19     if(falling_edge(clk)) then
20     dout<= din;
21     end if;
22
23 end process;
24 end behavioral;
```

Output of negative edge DFF



Note: To revert to EPWave opening in a new browser window, set that option on your user page.