

**INSTITUTE OF ENGINEERING AND TECHNOLOGY, DAVV
INDORE**



**ELECTRONICS & INSTRUMENTATION ENGINEERING
CIRCUIT DESIGN USING HDL(EIR7E1)**

LAB VIVA

Session: 2020-21

SUBMITTED TO:

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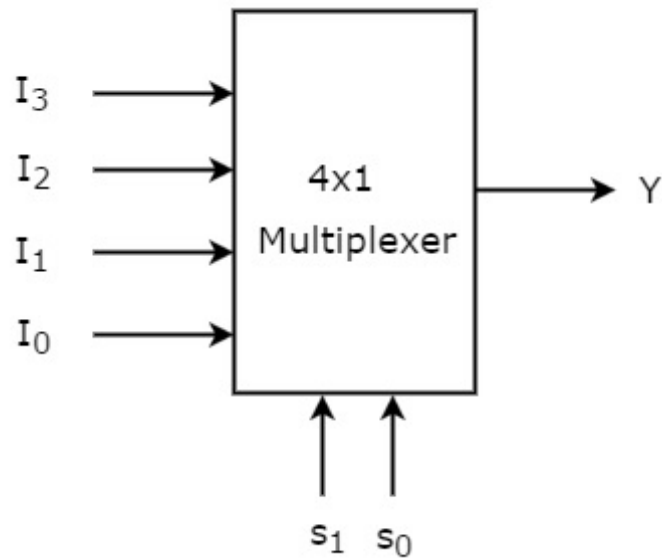
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4x1 Multiplexer



Truth table of a 4:1 Mux

Selection Lines		Output
s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Design code

```
1 library IEEE;          VHDL Testbench
2 use IEEE.STD_LOGIC_1164.ALL;
3
4 entity MUX41_IMPL_SIMBOX is
5 end MUX41_IMPL_SIMBOX;
6
7 architecture TEST_MUX41_IMPL
  of MUX41_IMPL_SIMBOX is
8
9   component MUX41_IMPL is
10     port (
11       D0, D1, D2, D3, S0,
12       S1: in STD_LOGIC;
13       mux_out : out
14         STD_LOGIC
15     );
16   end component;
17
18   signal D0_test : STD_LOGIC :=
19     '1';
20   signal D1_test : STD_LOGIC :=
21     '0';
22   signal D2_test : STD_LOGIC :=
23     '1';
24   signal D3_test : STD_LOGIC :=
25     '1';
26   signal S0_test, S1_test :
27     STD_LOGIC := '0';
28   signal mux_out_test :
29     STD_LOGIC;
30
31   for my_MUX41_IMPL :
32     MUX41_IMPL use entity
33     work.MUX41_IMPL_top(structure
34     );
35
36   begin
37     my_MUX41_IMPL :
38       MUX41_IMPL
39       port map (
40         D0 => D0_test,
41         D1 => D1_test,
42         D2 => D2_test,
43         D3 => D3_test,
44         S0 => S0_test,
45         S1 => S1_test,
46         mux_out => mux_out_test
47       );
48
49     S0_test <= not S0_test
50     after 2 ns;
51     S1_test <= not S1_test
52     after 4 ns;
53
54   end TEST_MUX41_IMPL;
```

```
1 library IEEE;          VHDL Design
2 use IEEE.STD_LOGIC_1164.ALL;
3
4 entity MUX41_IMPL_top is
5   port (
6     D0, D1, D2, D3, S0, S1:
7     in STD_LOGIC;
8     mux_out : out STD_LOGIC
9   );
10 end MUX41_IMPL_top;
11
12 architecture structure of
13   MUX41_IMPL_top is
14
15   component MUX41_IMPL
16     port (
17       D0, D1, D2, D3, S0,
18       S1: in STD_LOGIC;
19       mux_out : out
20         STD_LOGIC
21     );
22   end component;
23
24   begin
25     u1: MUX41_IMPL port map (D0,
26       D1, D2, D3, S0, S1,
27       mux_out);
28
29   end structure;
```

Output Waveform:

