INSTITUTE OF ENGINEERING & TECHNOLOGY

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Department of electronics and instrumentation

SESSION: 2017-2021

Subject: circuit design using HDL(EIR7C4)

4 bit left shift register

Roll no. : 17E7051

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E&I(7th sem)

4-BIT LEFT SHIFT REGISTER

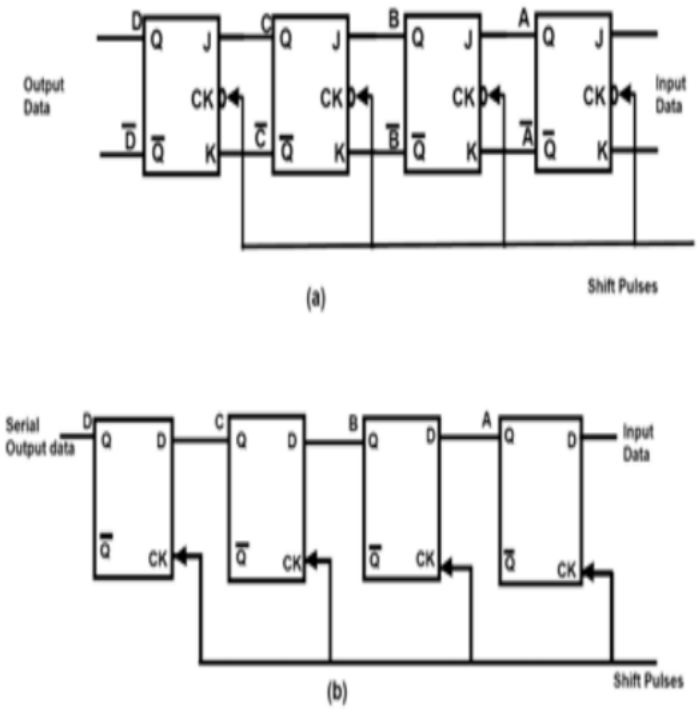

Figure 1: Shift Registers (a) JK (b) D-type

Design code

design.vhd

VHDL Design

```
1  -- Code your design code
2  library IEEE;
3  use IEEE.std_logic_1164.all;
4  use IEEE.numeric_std.all;
5
6  entity bitreg is
7
8   port(
9            serial_in    : in
   std_logic;
10           clk : in
   std_logic;
11           temp : in
   std_logic_vector;
12           q    : out
   std_logic_vector(3 downto
   0));
13
14 end bitreg;
15
16
17 architecture dataflow of
   bitreg is
18
19 begin
20   process (clk)
21   begin
22     -- q(3) <= temp(3);
23     -- q(2) <= temp(2);
24     -- q(1) <= temp(1);
25      q(0) <= serial_in;
26      q <= temp;
27   end process;

28 end dataflow;
```

Testbench code

testbench.vhd

```
-- code your testbench here
library IEEE;
use IEEE.std_logic_1164.all;

entity d_bitreg is
end d_bitreg;

architecture dataflow of d_bitreg is
  component bitreg is

  port(
        serial_in,clk : in std_logic;
        temp : in std_logic_vector;
        q : OUT std_logic_vector(3 downto 0));
  end component;

  --Inputs

  signal serial_in : std_logic := '0';
  signal clk : std_logic := '0';
  signal temp : std_logic_vector(3 downto 0) := "0101";

  --Outputs
  signal q : std_logic_vector(3 downto 0);

  begin
     uut: bitreg port map(
     serial_in => serial_in ,
     temp => temp,
     clk => clk,
     q => q);
         clk_process :process

         begin
             clk <= '0';
             wait for 10ns;
             clk <= '1';
             wait for 10ns;
         end process;
         stim : process
         begin
             serial_in <= '1';
             wait for 20ns;
             wait;
        end process;
end;
```

EPwave