Implementation Agreement 400ZR

OIF-400ZR-01.0

March 10, 2020

Implementation Agreement created and approved

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ABSTRACT: Implementation Agreement created and approved by the Optical Internetworking Forum for a 400ZR Coherent Optical interface. The project start was approved at the Q3 Technical Meeting, October 2016 (San Jose CA, USA). OIF2016.400.04 is the original project start document for this project

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4 Document Revision History

Table 1 provides the 400ZR Implementation Agreement revision history.

Document	Date	Revisions/Comments
OIF-400ZR-01.0	March 10, 2020	Initial release

Table 1: 400ZR IA document revision history

5 Introduction

This Implementation Agreement (IA) specifies a Digital Coherent 400ZR interface for two applications:

- 120 km or less, amplified, point-to-point, DWDM noise limited links.
- Unamplified, single wavelength, loss limited links.

The IA aims to enable interoperable, cost-effective, 400Gb/s implementations based on single-carrier coherent DP-16QAM modulation, low power DSP supporting absolute (Non-Differential) phase encoding/decoding, and a Concatenated FEC (C-FEC) with a post-FEC error floor <1.0E-15. 400ZR operates as a 400GBASE-R PHY.

Figure 1 shows the scope of this IA.

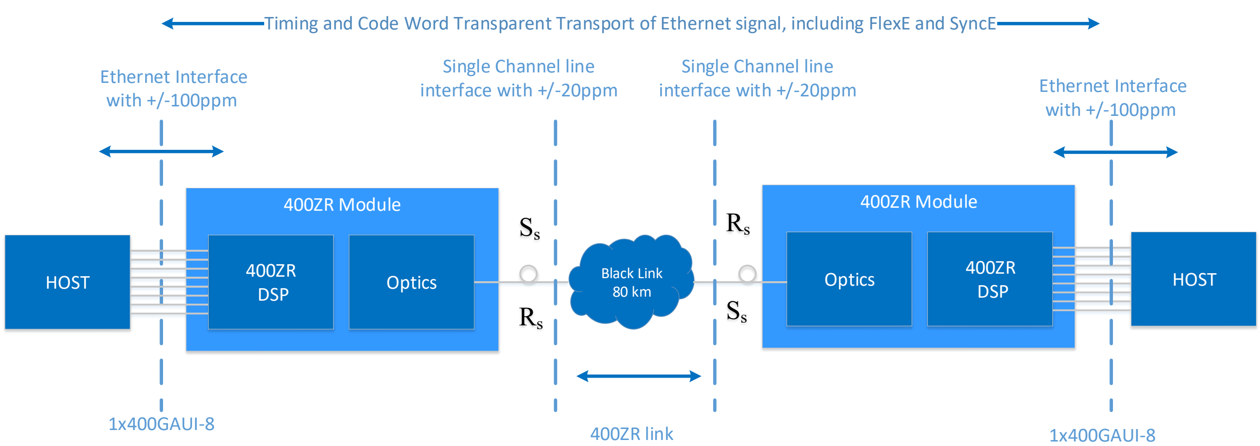


Figure 1: 400ZR reference diagram

No restriction on the physical form factor is implied by this IA (QSFP-DD, OSFP, COBO, CFP2, CFP8), but the specifications target a pluggable DCO architecture with port densities equivalent to grey client optics.

400ZR builds upon the work of other standards bodies including IEEE 802.3TM-2018 and ITU-T SG-15.

6 400ZR interfaces

The 400ZR IA supports the following host interface functions.

Host protocol support	Sublayer	Capabilities
IEEE Std 802.3™-2018 400GBASE-R	PCS	FEC coding RS(544,514), lane distribution, AM lock and deskew, per clause 119.1, Extender sublayer.
	PMA	Mux'ing, clock and data recovery, clock generation, modulation.
	AUI	Optionally physically instantiated as 400GAUI-8 C2M; 8 x CEI-56G-VSR PAM-4.

Table 2: 400ZR host interface

This IA does NOT define support of other host interfaces, nor the aggregation of multiple host interfaces. This IA, however, should not limit the ability to extend the host interfaces in the future.

6.1 400ZR Clocking Modes

The 400ZR data path is mapped asynchronously using a local clock reference. Simplified GMP mapping per ITU-T G.709.1 Annex D is used to rate-adapt the payload to the local reference, supporting data and timing transparency. The local clock tolerance is +/- 20ppm.

For timing transparent applications digital phase-interpolation is used to recover the timing information from the GMP mapped C_m bytes.

6.2 Media Interface - Black Link

400ZR provides timing and codeword transparent transmission of a 400GBASE-R interface. 400ZR uses a "black link" approach, to define the optical interface parameters for a (single-channel) optical tributary as shown in Figure 1.

The black link may contain neighboring channels and optical amplifiers in the optical path. Black link specifications are provided in Sections 13.1.1 and 13.2.1. The black link methodology enables longitudinal mode compatibility at the single-channel points (S_s, R_s), however, it does not enable longitudinal mode compatibility at multichannel points.

7 400ZR use cases

400ZR is intended for the use cases summarized here. The different 400ZR use cases can be addressed with different 400ZR DCO module implementations.

7.1 120 km or less, amplified, point-to-point, DWDM noise limited link

There are 3 use cases of amplified point-to-point links (no OADM) identified for 400ZR in Figure 2 through Figure 4. For amplified links the reach is dependent on the OSNR at the receiver (noise limited). The 400ZR targeted reach for these applications is 80km or more. These use cases are covered by Application Code ***0x01*** in this IA.

Figure 2: Transceiver line card with 400ZR amplified point-to-point interface

Figure 3: Router switch line card with 400ZR DWDM Interfaces

Figure 4: Transceiver line card with 400ZR DWDM interfaces

7.2 Unamplified, single wavelength, loss limited link

For an unamplified link as shown in Figure 5**,** the reach is dependent on the transmit output power, input receive sensitivity, and the channel's loss characteristics. This use case is covered by Application Code ***0x02*** in this IA.

Figure 5: Router/Switch line card with 400ZR unamplified point-to-point Interface

8 Host to 400ZR data path

Figure 6 shows the functional blocks in the Tx and Rx data path.

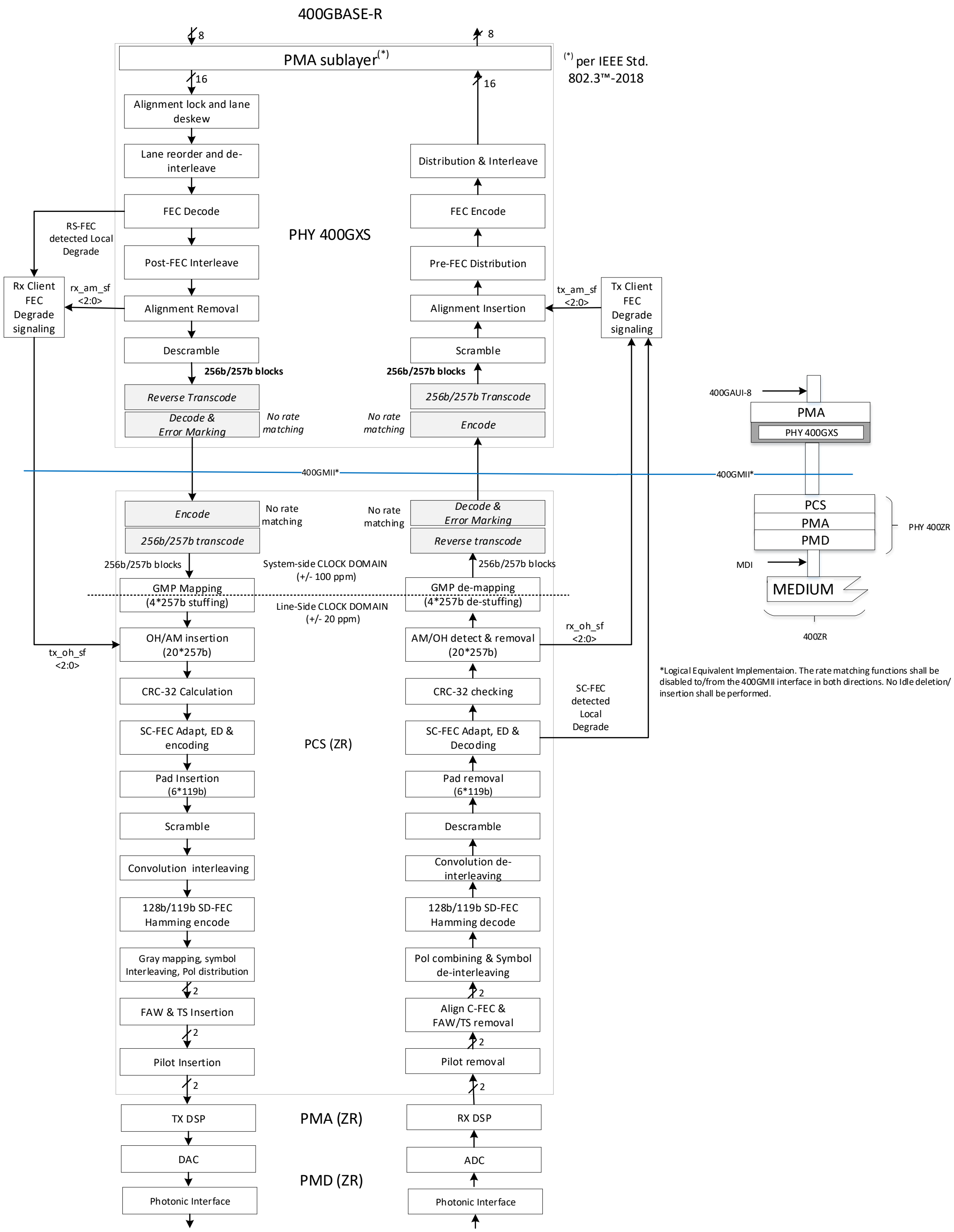


Figure 6: Data path detail

8.1 400G Host Side Interface

The 400GbE data enters the transceiver using the 400GBASE-R PMA sublayer, where the electrical interface, for example, may be 400GAUI-8 C2M. The characteristic information of the adapted and mapped 400GBASE-R host interface signal consists of a scrambled sequence of 256b/257b encoded blocks with a nominal bit-rate of 425 000 000 kbit/s, ±100 ppm.

NOTE – 425 000 000 kbit/s is the nominal bit-rate of the aggregate 400GBASE-R PCS signal consisting of 16 PCS lanes with 256b/257b encoding and FEC at the PMA service interface.

8.2 PMA

The PMA provides a medium-independent means for the PCS to support the use of a range of physical media. The 400GBASE-R PMA performs the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface. In addition, the PMA performs retiming of the received data stream when appropriate. The 400GBASE-R PMA service interface is defined in IEEE Std 802.3™-2018 Clause 120.3 as an instance of the inter-sublayer service interface definition in clause 116.3.

8.3 PCS (partial processes)

The 400ZR application implements only a portion of the full PCS processes defined in IEEE Std 802.3™-2018 clause 119.

8.3.1 PCS Rx direction (400ZR Tx datapath)

The 400GBASE-R PCS Rx direction (400ZR Tx data path) is defined for 400ZR to include the following services:

- Alignment lock and lane de-skew (reference IEEE Std 802.3™-2018 119.2.5.1).
- Lane reorder and de-interleave (reference IEEE Std 802.3™-2018 119.2.5.2).
- Reed-Solomon FEC decoding the 257-bit blocks and signaling of RS-FEC (544,514) detected local degrade (Reference IEEE Std 802.3™-2018 119.2.5.3).
- Post FEC interleave (Reference IEEE Std 802.3™-2018 119.2.5.4).
- Alignment Marker removal and signaling of Alignment Marker Signal Fail *(rx_am_sf<2:0>)*. Reference IEEE Std 802.3™-2018 119.2.5.5.
- Descramble (Reference IEEE Std 802.3™-2018 119.2.5.5).
- Error Marking – Signaling Tx link degrade (Reference ITU-T G.709/Y.1331 Amendment 2 (06/2018) Annex K and Section 8.8.4).

The RS-FEC decoder may provide the option to perform error detection without error correction to reduce the latency contributed by the RS-FEC sublayer.

8.3.2 PCS Tx direction (400ZR Rx datapath)

The 400GBASE-R PCSs Tx direction (400ZR Rx data path) defined for 400ZR include the following services:

- Scramble (Reference IEEE Std 802.3™-2018 Clause 119.2.4.3).
- Alignment Marker Insertion and signaling of Alignment Marker Signal Fail (*tx_am_sf<2:0>)*. (Reference IEEE Std 802.3™-2018 Clause 119.2.4.4).
- Pre-FEC distribution (Reference IEEE Std 802.3™-2018 Clause 119.2.4.5).
- Reed-Solomon FEC encoding the 257-bit blocks (reference IEEE Std 802.3™-2018 Clause 119.2.4.6).
- Distribution and interleave (Reference IEEE Std 802.3™-2018 Clause 119.2.4.6).
- Error Marking – Signaling Rx link degrade (Reference ITU-T G.709/Y.1331 Amendment 2 (06/2018) Annex K and Section 8.8.4).

8.4 400ZR frame structure

400GBASE-R, FlexO-4-DSH, and 400ZR frames have similar structures. They are all block formats, 10280 columns×4096 rows (1×4096 or 16×256). The 400ZR frame OH area is the same as the FlexO-4-DSH, however, fewer OH fields are defined as required for 400ZR than for FlexO-4-DSH. Bonding across multiple PHY's is not supported by the 400ZR frame structure. Figure 7 shows the 400ZR frame structure.

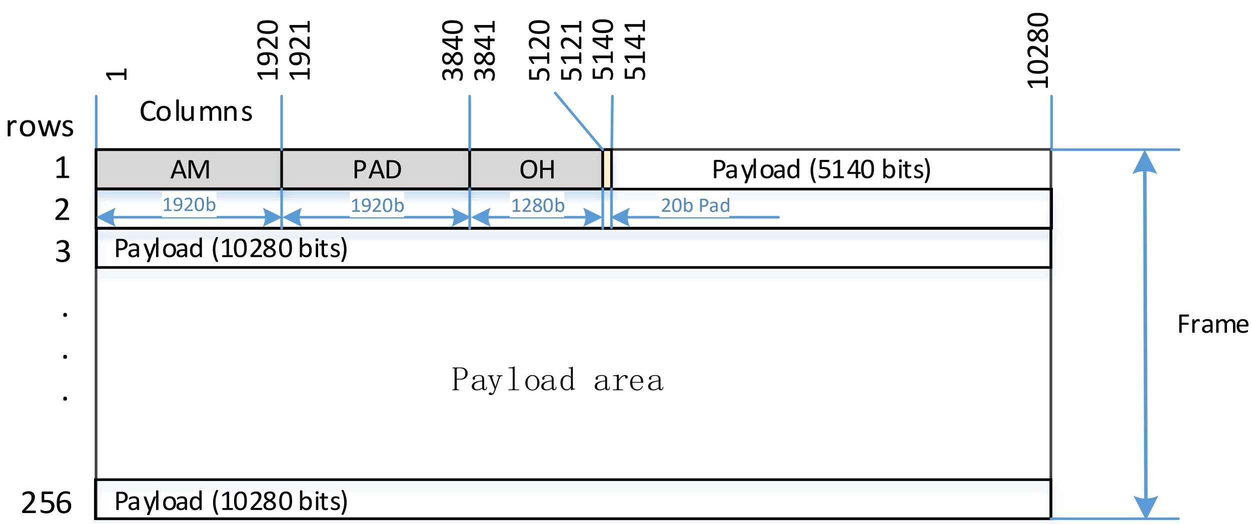


Figure 7: 400ZR frame structure without parity bits

8.4.1 400ZR Multi-Frame

The 400ZR multi-frame structure with FEC parity field (columns 10281 to 10970) is shown in Figure 8 and contains a frame Alignment Marker (AM) sequence every 256 rows. Columns are defined as 1-bit wide and a frame consists of 10970 columns. This results in a bit-oriented structure. The 400ZR multi-frame can be viewed as a binary matrix with n×256 rows of 10970 bits.

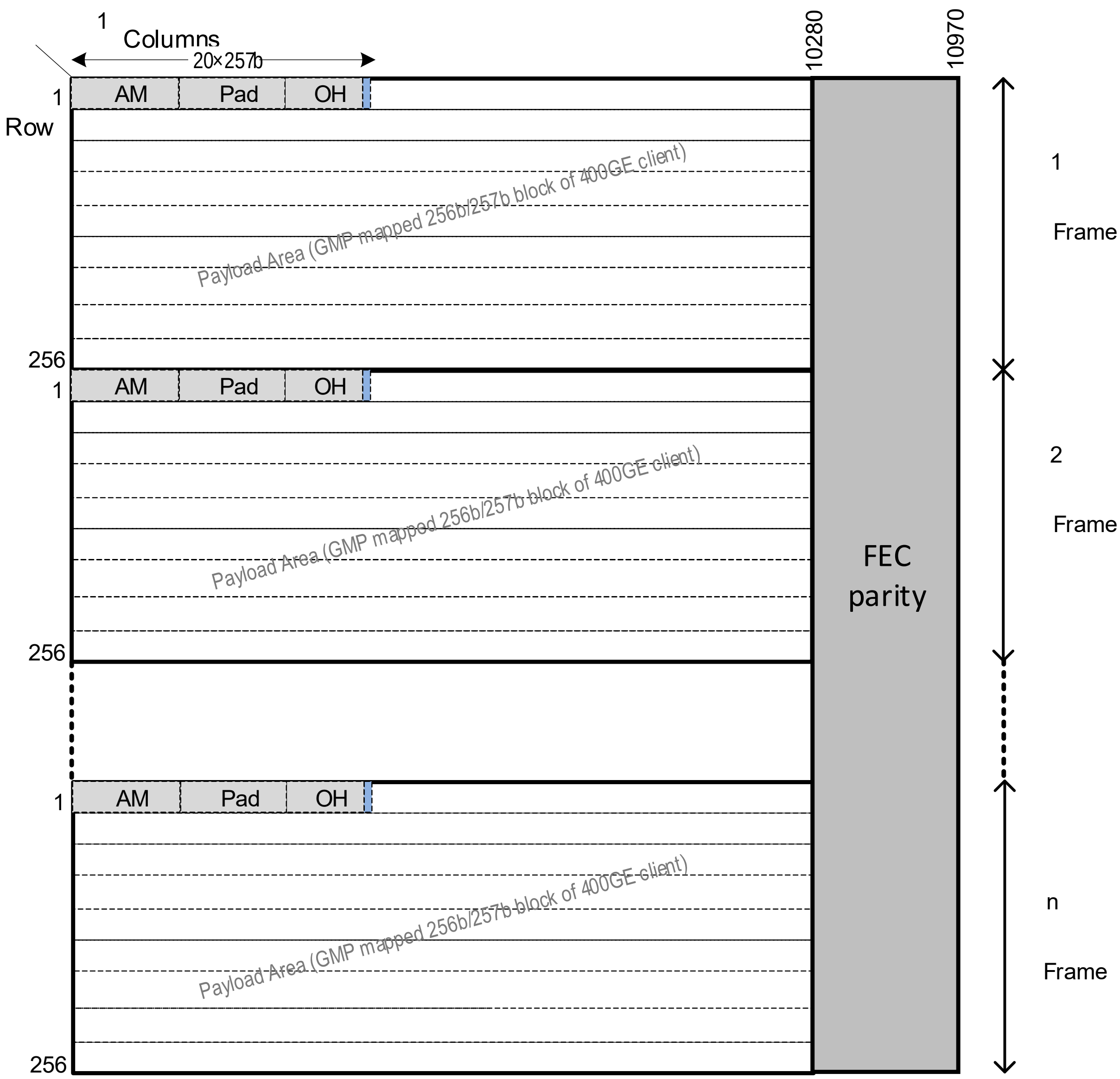


Figure 8: 400ZR multi-frame structure with parity bits

8.5 AM/PAD/OH insertion

5120-bits of AM/PAD/OH, plus 20-bits of additional pad for 257b alignment, are inserted in columns 1 to 5140 of the first row of each 400ZR frame. This leaves 10220 × 257b of additional payload area in the frame. See Figure 9 below.

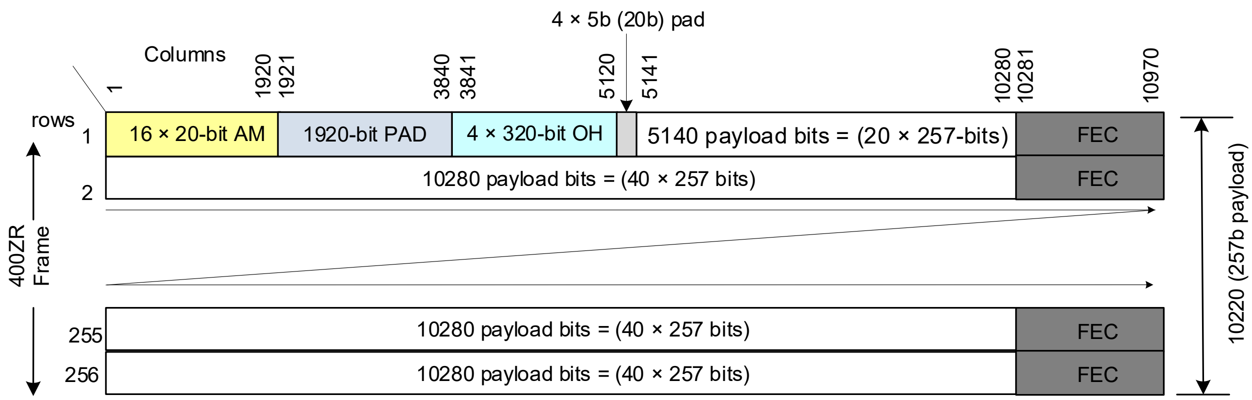


Figure 9: 400ZR Frame overhead

The AM field is a set of 16×120-bit blocks that are 10-bit interleaved. PAD is a 1920-bit all-zeros field. The 400ZR OH consists of 4×320b blocks (1280-bits) that are 10b interleaved and transmitted immediately after the 1920-bits of PAD. Figure 10 details the first 320-bit OH block. The remaining 3×320-bit 400ZR OH blocks are reserved for future standardization (transmitted as all-zeros and ignored on receipt).

The required 400ZR OH fields are highlighted in black text; the optional fields, in gray text. The 400ZR OH area includes GMP mapping control bytes (JC*x* Bytes). See section 8.9 for GMP processing details. The undefined 400ZR frame OH can provide additional OAM fields, or be set to zero and ignored at the 400ZR receiver.

8.5.1 400ZR AM/PAD/OH Transmission order

The 400ZR frame structure carries 514 blocks of 10-bit interleaved (5140 bits) of AM/PAD/OH + 20-bits of additional PAD. The transmission order for each of these fields is defined in Section 8.6 through Section 8.8 and is the same as IEEE Std 802.3™-2018 and 400G FlexO.

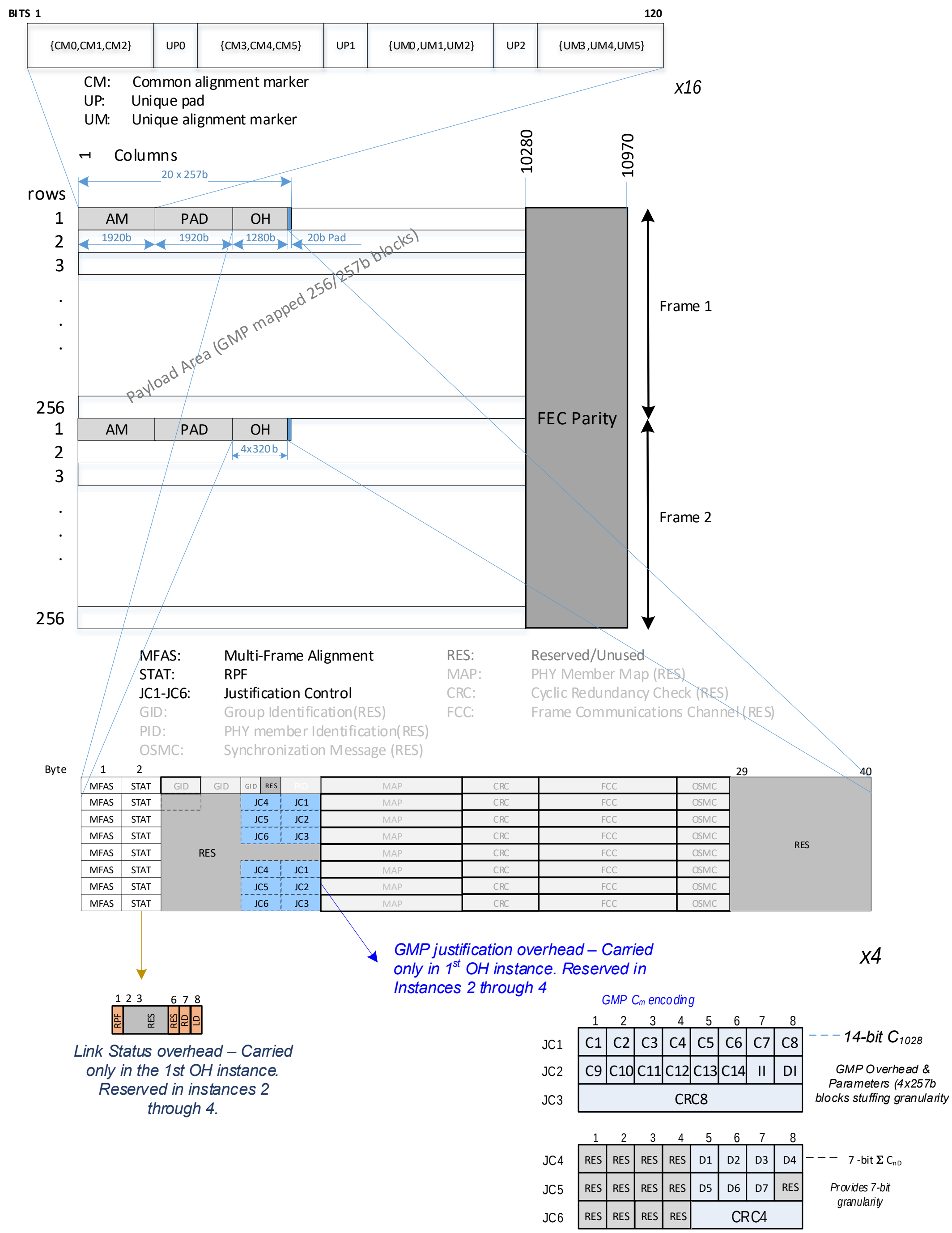


Figure 10: 400ZR overhead

8.6 400ZR Alignment Markers (AM)

The role of AM is to find the FEC block boundary. Alignment markers are inserted before FEC encoding and removed after FEC decoding. The 400ZR modem operates across two domains. IEEE Std 802.3™-2018 clause 119 defines the AM requirements at the 400GBASE-R interface. This IA defines the 400ZR frame AM requirements for the coherent single-carrier media interface.

400ZR frame defines a 16×120 = 1920 bits AM field which contains the 10-bit interleaving result of 16 lane alignment markers of 120-bits each. Frame alignment, however, can be done across a subset of these fields. The alignment marker field is carried at the beginning of each frame (1st row). 400ZR AM is protected by the SC-FEC and its value is scrambled. AM alignment is processed post FEC decode (after descrambling) to locate the row number corresponding to the start of the 400ZR frame (SC-FEC being already 10970b row aligned).

Figure 11 illustrates the AM transmission order. The 192×10b (1920 bits total) blocks are transmitted left to right starting with the 1st 10-bits of am0, followed by the 1st 10-bits of am1, etc.., until the 12th 10-bits of am14 (1920 bits total).

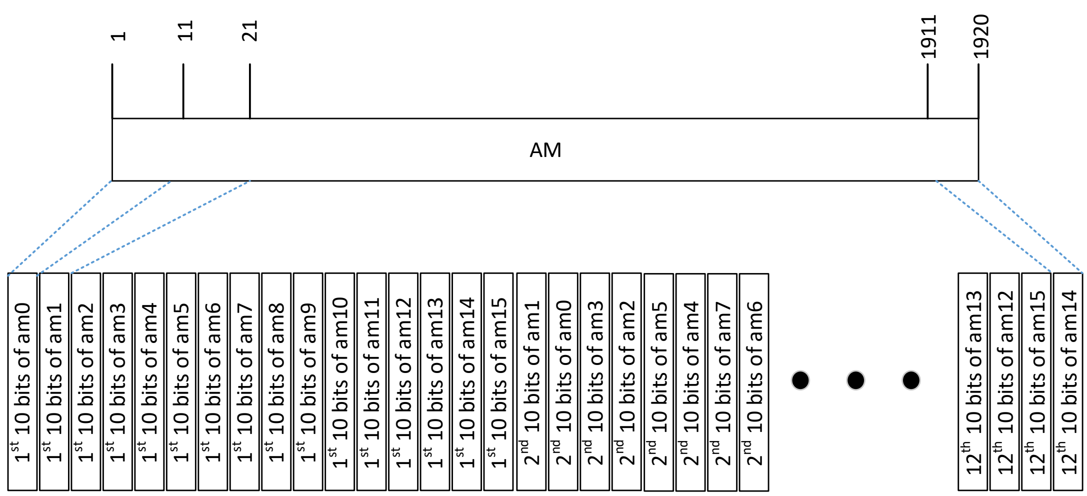


Figure 11: Alignment Marker transmission order – 10b interleaved

The 400ZR AM field consists of 16 logical lane alignment marker indicators (am<i>, where <i> = 0,1...15). Each lane carries a 120-bit lane alignment marker. Figure 12, and rows of Table 3 give the values of am<i> transmitted over lane <i>.

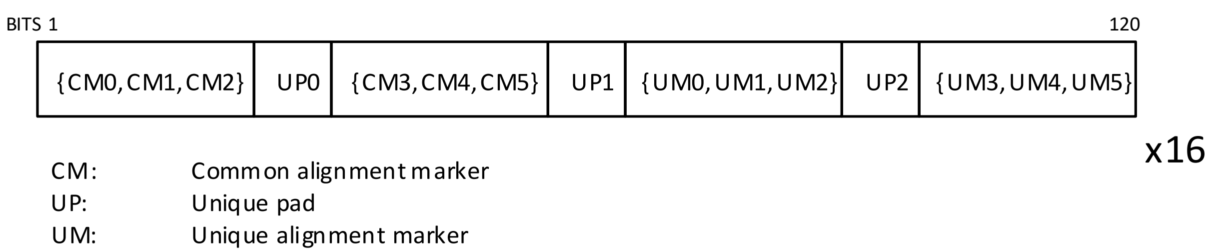


Figure 12: Alignment Marker format

The alignment marker encoding is shown in Table 3.

Logical Lane am<i>	Encoding {CM_0, CM_1, CM_2, UP_0, CM_3, CM_4, CM_5, UP_1, UM_0, UM_1, UM_2, UP_2, UM_3, UM_4, UM_5}
0	0x59,0x52,0x64,0x6D,0xA6,0xAD,0x9B,0x9B,0x80,0x8E,0xCF,0x64,0x7F,0x71,0x30
1	0x59,0x52,0x64,0x20,0xA6,0xAD,0x9B,0xE6,0x5A,0x7B,0x7E,0x19,0xA5,0x84,0x81
2	0x59,0x52,0x64,0x62,0xA6,0xAD,0x9B,0x7F,0x7C,0xCF,0x6A,0x80,0x83,0x30,0x95
3	0x59,0x52,0x64,0x5A,0xA6,0xAD,0x9B,0x21,0x61,0x01,0x0B,0xDE,0x9E,0xFE,0xF4
4	0x59,0x52,0x64,0x87,0xA6,0xAD,0x9B,0x98,0x54,0x8A,0x4F,0x67,0xAB,0x75,0xB0
5	0x59,0x52,0x64,0x4F,0xA6,0xAD,0x9B,0x72,0x48,0xF2,0x8B,0x8D,0xB7,0x0D,0x74
6	0x59,0x52,0x64,0xBC,0xA6,0xAD,0x9B,0x77,0x42,0x39,0x85,0x88,0xDB,0xC6,0x7A
7	0x59,0x52,0x64,0x44,0xA6,0xAD,0x9B,0x4C,0x6B,0x6E,0xDA,0xB3,0x94,0x91,0x25
8	0x59,0x52,0x64,0x06,0xA6,0xAD,0x9B,0xF9,0x87,0xCE,0xAE,0x06,0x78,0x31,0x51
9	0x59,0x52,0x64,0xD6,0xA6,0xAD,0x9B,0x45,0x8E,0x23,0x3C,0xBA,0x71,0xDC,0xC3
10	0x59,0x52,0x64,0x5F,0xA6,0xAD,0x9B,0x20,0xA9,0xD7,0x1B,0xDF,0x56,0x28,0xE4
11	0x59,0x52,0x64,0x36,0xA6,0xAD,0x9B,0x8E,0x44,0x66,0x1C,0x71,0xBB,0x99,0xE3
12	0x59,0x52,0x64,0x81,0xA6,0xAD,0x9B,0xDA,0x45,0x6F,0xA9,0x25,0xBA,0x90,0x56
13	0x59,0x52,0x64,0x28,0xA6,0xAD,0x9B,0x33,0x8C,0xE9,0xC3,0xCC,0x73,0x16,0x3C
14	0x59,0x52,0x64,0x0B,0xA6,0xAD,0x9B,0x8D,0x53,0xDF,0x65,0x72,0xAC,0x20,0x9A
15	0x59,0x52,0x64,0x2D,0xA6,0xAD,0x9B,0x6A,0x65,0x5D,0x9E,0x95,0x9A,0xA2,0x61
NOTE – The value in each byte of this table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of AM values found in [IEEE Std 802.3™-2018], which uses an LSB-first bit transmission format.	

Table 3: 400ZR Alignment Marker encodings

8.7 400ZR PAD

Immediately following the 1920-bit AM is a 1920-bit field of PAD, transmitted as all-zeros and ignored on receipt.

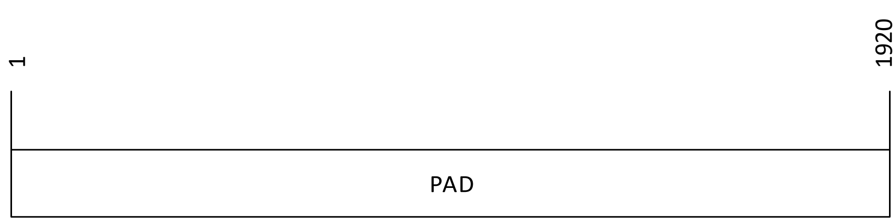


Figure 13: PAD transmission order – 10b interleaved

8.8 400ZR OH

Four 320-bit blocks of overhead are transmitted immediately after the 1920 bit of PAD. These are 10-bit interleaved.

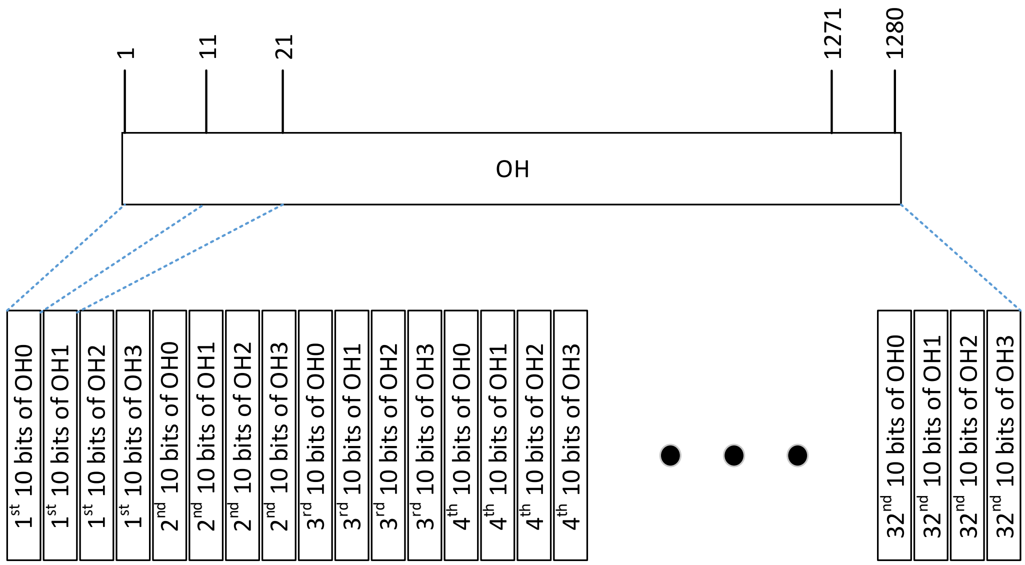


Figure 14: Over Head transmission order – 10b interleaved

8.8.1 Multi-Frame Alignment Signal (MFAS)

The Multi-frame alignment signal (MFAS) is in the first of the four 320-bit OH instances. It is present and incremented in every 400ZR frame. It counts from 0x00 to 0xFF and provides a 256-frame multi-frame sequence following [ITU-T G.709.1] Clause 9.2.1 definition.

8.8.2 Link error and Link degrade detection and marking

Table 4 specifies the replacement signal to the host interface in the event of DSP framing or ZR frame/multi-frame loss.

Host interface signal	Replacement signal	Bit-rate tolerance (ppm)
400GBASE-R	Continuous 400GBASE-R local fault sequence ordered sets as 256b/257b encoded blocks	+/- 100

Table 4: Replacement signal

The FEC decoder can also detect a degrading link and signal Link Degrade (LD). A degraded link condition data may be passing data without error, however, the BER may be high and approaching FEC exhaust. Causes of link degrade may be component wear-out due to aging or stress. A user may want to take pre-emptive actions based on programmable BER thresholds. Consequent actions can include re-routing traffic away from the impaired link.

8.8.3 Link status monitoring and signaling (STAT)

The status (STAT) overhead byte is present in every 400ZR frame, but only carried in the first of the four 320-bit OH instances. It includes the 1-bit RPF and 3-bit LDI fields:

- The Remote PHY Fault (RPF) bit indicates signal fail status detected at the remote 400ZR sink function in the upstream direction and follows the definition in [ITU-T G.709.1] Clause 9.2.5.1. RPF is set to "1" to indicate a remote 400ZR PHY defect indication; otherwise, it is set to "0'. The RPF field is in bit 1 of the STAT field as per Figure 15.
- The 3-bit host Link Degrade Indication (LDI) field is defined to indicate to the downstream device the quality of the host interface signal or the media interface signal.

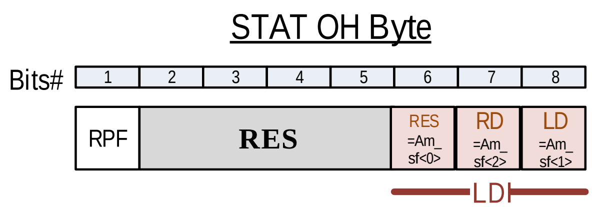


Figure 15: STAT Over Head byte definitions

The 400ZR link shall provide detection and signaling of Link Degrade (LD) for use by switch/routers with soft reroute capabilities. Figure 16 illustrates the bidirectional signaling between a 400ZR transceiver and two Routers (A and B). Pre-FEC BER monitors are used to detect and insert link degrade at both the 400ZR optical link and the 400GBASE-R interface.

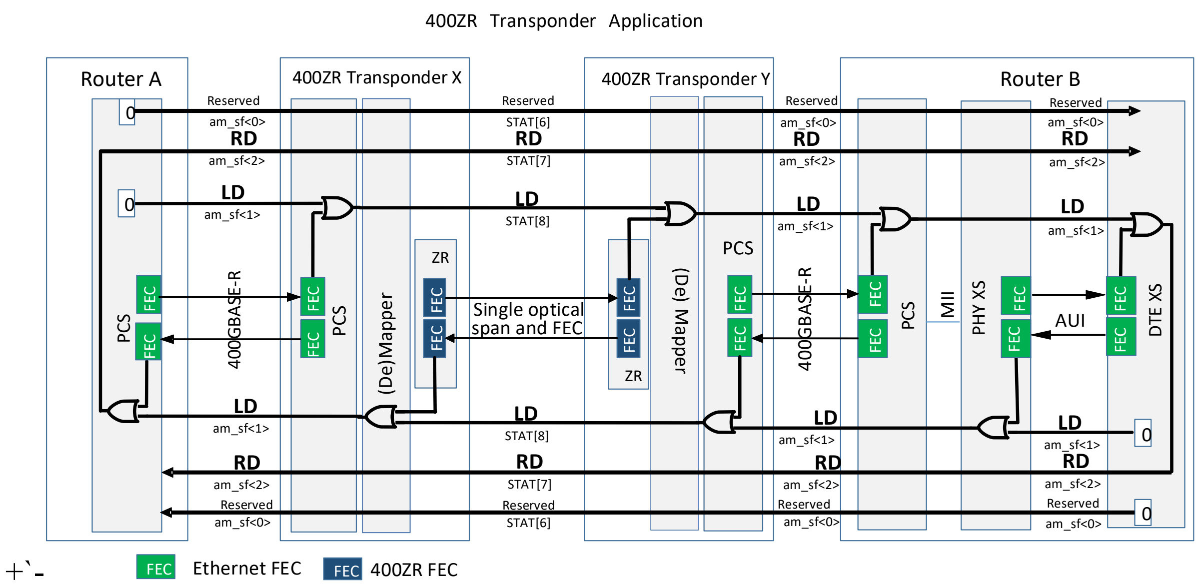


Figure 16: Local/Remote Degrade interworking between Switch/Router and 400ZR transceiver

8.8.4 Link Degrade Indication (LDI)

[IEEE 802.3] has specified three bits in the AM field (am_sf<2:0>) to carry Link Degrade Indication (LDI). Bit am sf<2> is defined as a Remote Degrade (RD) signal, bit am_sf<1> is defined as a Local Degrade (LD) signal and bit am_sf<0> is reserved.

The 400ZR transceiver X and Y shall forward the information in the Reserved (am_sf<0>) and RD (am_sf<2>) bits between transceivers as illustrated in Figure 16. The information in am_sf<0> shall be carried in 400ZR STAT overhead bit 6. The status information in am_sf<2> shall be carried in 400ZR STAT overhead bit 7. The status information in the LD (am_sf<1>) bit shall be carried after some additional processing in the 400ZR STAT overhead, bit 8 to the downstream device.

In the host-to-media datapath, the additional processing consists of ORing the ingress LD status in the am_sf<1> bit of the 400GBASE-R signal with the local host interface RS(544,514) FEC degrade status and signaling LD in STAT[8] to the media interface. In the media-to-host datapath, the STAT<8> bit from the media interface is ORed with the 400ZR FEC degrade status and signaled on the am_sf<1> bit to the local host.

8.8.5 Link Degrade Warning and Alarming.

FEC Detected Degrade (FDD) and FEC Excessive Degrade (FED) is an optional [*user configurable*] link monitoring feature, indicating a link degrade condition to the local host and remote transmitter. It can be used, for example, to pre-emptively move traffic away from a degraded link (e.g. traffic re-route). This feature requires capturing the pre-FEC BER from the FEC decoder block over a Performance Monitor (PM) interval. Statistics are gathered by HW and reported by SW. FED and FDD are determined by comparing the HW BER reported statistics against [user configurable] thresholds.

Link Degrade (LD) signaling shall be based on the FEC decoder statistics (number of corrected errored bits, and uncorrectable blocks). Fault detection calculation and threshold settings may be implementation dependent (e.g. based on FEC decoder pre-FEC BER detection capabilities).

The following Performance Monitoring (PM) parameters are defined for determining a Link Degrade (LD) condition over a PM interval. The PM interval and the collection of the statistics to determine LD is defined by the Management Interface Spec specific to the module which this IA is implemented.

FEC decoder block, bit counters:

- *pFECblkcount* = FEC blocks counted over PM interval
- *pFECbitcount* = total number of bits counted over PM interval = (*pFECblkcount* × bits per FEC block), 64-bit value
- *pFECcorrbitblk* = FEC corrected bits per block (min., avg., max.) over PM interval
- *pFECcorrbit* = total number of FEC corrected bits over PM interval = ∑*pFECcorrbitblk* over PM interval. (64-bit value).

Pre-FEC BER block, bit counters:

- *pFECblkBER* = FEC block BER (min., avg., max.) over PM interval = (*pFECcorrbitblk*/*pFECblkcount*)
- *pFECBER* = FEC BER over PM interval = (*pFECcorrbit* / *pFECbitcount*)

Pre-FEC threshold settings:

- *FEC_excessive_BER_activate_threshold* (programmable)
- *FEC_excessive_BER_deactivate_threshold* (programmable)
- *FEC_degraded_BER_activate_threshold* (programmable)
- *FEC_degraded_BER_deactivate threshold* (programmable)

FEC degrade settings:

- *FECdetectdegraded =* FEC degraded status condition over PM interval.
- *FECexcessdegraded =* FEC excessively degraded status condition over PM interval.

Each of the above registers shall have a corresponding enable, status, and latch bit settings. *FECdetectdegraded* and *FECexcessdegraded* shall also be a maskable interrupt.

PM interval:

- *PM_Interval* = (programmable); default = 1 second*.*

The FEC decoder counts and reports the number of bits detected in error over the PM interval per FEC block (min., max., avg.).

- When the (avg) number of bit errors exceeds the threshold set in *FEC_degraded_BER_activate_threshold, FECdetectdegraded* is set and latched.
- When the (avg) number of bit errors falls below the threshold *FEC_degraded_BER_deactivate_threshold*, *FECdetectdegraded* is cleared.
- When the (avg) number of bit errors exceeds the threshold set in *FEC_excessive_BER_activate_threshold, FECexcessdegraded* is set and latched.
- When the (avg) number of bit errors falls below the threshold *FEC_excessive_BER_deactivate_threshold*, *FECexcessdegraded* is cleared.

When errors are detected after C-FEC error correction in the Rx data path (e.g. uncorrected block status from the C-FEC decoder or CRC32 checking), the entire base block of 30592×8 bits is considered corrupted and all 952×257-bits of information must be marked as being in error using transcoded error control blocks.

If the link input BER is much lower than C-FEC limit under normal operational conditions, error marking using post-FEC statistics (i.e. CRC32 checking) could be turned-off to lower Rx latency. In this case, a programmable pre-FEC excessive error threshold status could be used for error marking at the FEC decoder output.

Per 802.3™-2018 Clause 119.2.5.3, if bypass error indication is not supported or not enabled, when the Reed-Solomon decoder determines that a codeword contains errors that were not corrected, it shall cause the PCS receive function to set every 66-bit block within the two associated codewords to an error block (EBLOCK_R) as in Figure 17.

The encoding of a 64b/66b error control block is: [sync="10", control block type=0x1e, and eight 7-bit /E/control characters.

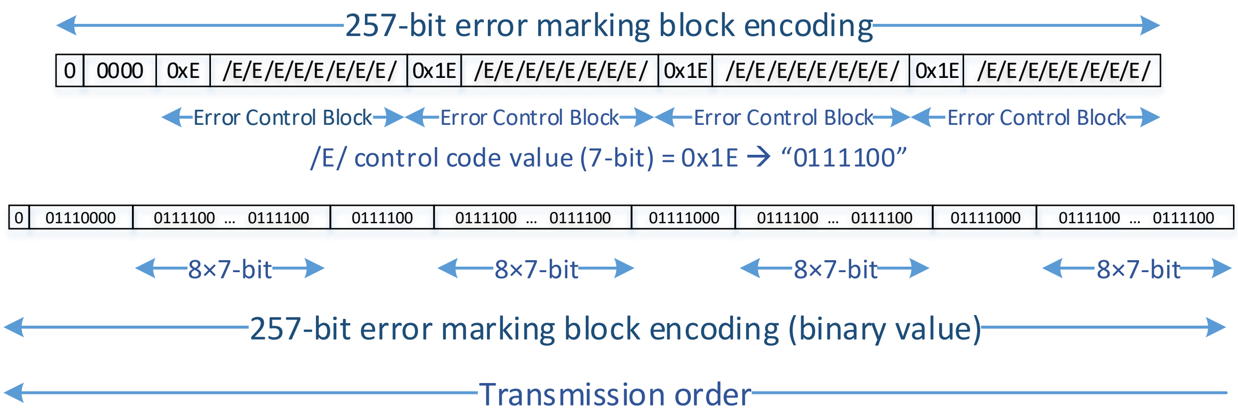


Figure 17: Error marking

8.9 GMP mapping processes

The 400GBASE-R is asynchronously mapped into a 400ZR container using GMP. The timing is de-correlated from the 400GBASE-R host clock to simplify ASIC design. Even though the mapping is asynchronous, the 400GBASE-R stream is treated as CBR data (including preamble, and IPG). Data and timing transparency shall be supported using information fields which are inserted by the GMP process for use upon de-mapping.

The GMP Justification Control bytes (JC1-6) are carried in the first of the four 320-bit OH instances, and present in the 2nd, 3rd, and 4th frames of a 400ZR 4-frame multi-frame to signal the GMP parameters C_m and $\sum C_{nD}$ from mapper to de-mapper. The 4 frames are identified by MFAS bits 7 and 8 being 00, 01, 10 and 11.

Reference ITU-T G.709 annex D for the general principles of the Generic Mapping Procedure (GMP).

For the purpose of 400ZR the GMP parameters shall be defined as:

- m = GMP data/stuff granularity = 4 × 257 = 1028 bit;
- n = 1028/128 = 8.03125-bit unit and represents the timing granularity of the GMP mapping present in C_n and $\sum C_{nD}$ parameters;
- $P_{m,server}$ = maximum number of m-bit data entities in 4-frame multi-frame server payload = 10220.
- C_m = number of client m-bit data entities in 4-frame multi-frame server payload. It is encoded with 14 bits and carried in JC1 and JC2 control OH bytes.
- C_n = number of equivalent client n-bit data entities in 4-frame multi-frame server payload. This value provides additional 'n'-bit timing information.
- $\sum C_{nD}$ = accumulated value of the remainder of C_n and C_m. It is encoded with 7-bits and carried in JC4 and JC5 control OH bytes.
- C_n and C_m being integer values, then:

$$C_n(t) = 128 \times C_m(t) + (\sum C_{nD}(t) - \sum C_{nD}(t-1))$$

The support for n-bit timing information ($\sum C_{nD}$) in the JC4/JC5/JC6 OH is required.

The mapper shall first recover the 400GBASE-R stream. The 400GBASE-R is a sequence of 256b/257b encoded blocks as per IEEE Std 802.3™-2018 after the partial PCS processing defined in Figure 6 and Section 8.3. The 400ZR frame payload area is a direct multiple of 257 bits (10220×257b).

The 400GBASE-R signal is mapped to the 400ZR frame as a 257b block stream, with 20 blocks of AM/PAD/OH every 10240 blocks. The payload area for this mapping consists of the payload of a 4-frame 400ZR multi-frame (40880 257b blocks) for host interface data. Groups of 1028 successive bits (4×257b), of the client signal are mapped into a group of 4 successive 257b blocks of the 4-frame 400ZR multi-frame payload area under control of the GMP data/stuff control mechanism. Each group of 4×257b in the 4-frame 400ZR multi-frame payload area may either carry 1028 host interface bits or carry 1028 stuff bits. The stuff bits shall be set to zero.

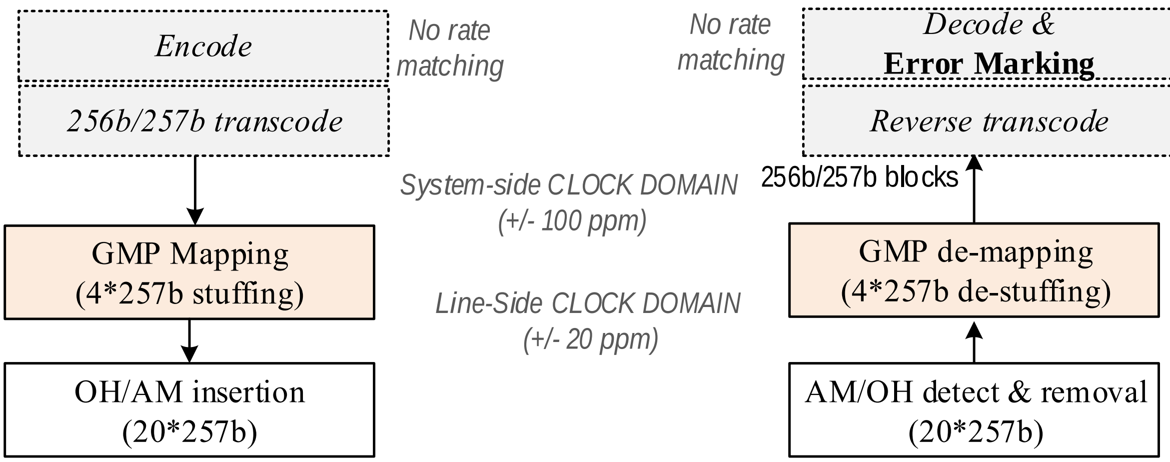


Figure 18: GMP mapping/de-mapping process

Table 5 specifies the host interface and its GMP m, n and C_{nD} parameter values.

Host nominal bit rate (kbits/s)	Nominal information bit rate (kbits/s) after FEC and AM removal	Bit-rate tolerance (ppm)	m	n	C_{nD}
425 000 000	401 542 892	+/- 100	1028	8.03125	Yes

Table 5: Host interface and its GMP parameter values

The server input nominal bit rate of 401 542 892 kbit/s equals the 400GBASE-R interface signal after RS(544/514) FEC decode and AM removal.

The de-mapping process decodes $C_m(t)$ and $C_{nD}(t)$ from JC1/JC2/JC3 and JC4/JC5/JC6 and interprets $C_m(t)$ and $C_{nD}(t)$ according to ITU-T G.709 Annex D. CRC8 shall be used to protect against an error in JC1/JC2/JC3 and CRC4 protect against an error in the JC4/JC5/JC6 signals.

Ref	GMP Parameter	Formula	Value	Units
f_{client}	nominal client information bit rate	425.00 Gbit/s × 514/544 × 20479/20480	401,542,892,456.055	bit/s
Δf_{client}	client bit rate tolerance		100	ppm
f_{server}	server nominal bit rate f		402,489,753,309.729	bit/s
Δf_{server}	server bit rate tolerance		20	ppm
T_{server}	period of the server multi-frame,	425.00 Gbit/s × 514/544 × 20479/20480	26.154	µs
B_{server}	number of bits per server multi-frame		10,526,720	bits
O_{server}	number of overhead bits per server multi-frame		20,560	bits
P_{server}	maximum number of bits in the server payload area		10,506,160	bits
$f_{p,server}$	nominal server payload bit rate	B_{server} / f_{server}	401,703,640,510.296	bits/s
m	GMP data/stuff granularity		(4×257 =) 1,028	bits
M	m and n ratio		128	
$P_{m,server}$	maximum number of (m bits) data entities in the server payload area	B_{server} - O_{server}	10220	
C_m	number of client m-bit data entities per server multi-frame	f_{server} × P_{server} / B_{server} = 478.75 × 28/29 × 119/128 × 5140/5488 × 511/512		
$C_{m,nom}$	c_m value at nominal client and server bit rates	m bit data entity	10,215.910	1028b blocks
$C_{m,min}$	c_m value at minimum client and maximum server bit rates	m / n	10,214.684	
$C_{m,max}$	c_m value at maximum client and minimum server bit rates	P_{server} / m	10,217.136	
$C_{m,min}$	integer value of $c_{m,min}$		10,214	
$C_{m,max}$	rounded up value of $c_{m,max}$	(f_{client} / $f_{p,server}$) × $P_{m,server}$	10,218	
n	GMP justification accuracy, n bit data entity	$C_{m,nom}$ × (1 - Δf_{client}) / (1 + Δf_{server})	8.03125	bits
$P_{n,server}$	maximum number of (n bits) data entities in the server payload area	$C_{m,nom}$ × (1 + Δf_{client}) / (1 - Δf_{server})	1,308,160.000	8.03125b blocks

Ref	GMP Parameter	Formula	Value	Units
C_n	number of client n-bit data entities per server multi-frame	$\lfloor C_{,min} \rfloor$		
$C_{n,nom}$	C_n value at nominal client and server bit rates	$\lceil C_{m,max} \rceil$	1,307,636.519	
$C_{n,min}$	C_n value at minimum client and maximum server bit rates		1,307,479.603	
$C_{n,max}$	C_n value at maximum client and minimum server bit rates	P_{server} / n	1,307,793.436	
C_{nD}	remainder of C_n and C_m		0.910305637	
C_{nD}	integer value of c_{nD}	$(f_{client} / f_{p,server}) \times P_{n,server}$		
ΣC_{nD}	accumulated value of C_{nD}	$C_{n,nom} \times (1 - \Delta f_{client}) / (1 + \Delta f_{server})$	127	

Table 6: GMP parameter values

Where,

- Client information rate is 400GBASE-R after RS(544,514) FEC and AM removal with f_{client} nominal bit rate and Δf_{client} bit rate tolerance.
- Server is 400ZR 4-frame multi-frame (both payload and overhead) with f_{server} nominal bit rate Δf_{server} bit rate tolerance and B_{server} number of bits per server 4-frame multi-frame.
- Server payload is 400ZR 4-frame multi-frame payload (before AM/PAD/OH insert) with $f_{p,server}$ nominal bit rate, Δf_{server} bit rate tolerance and P_{server} number of bits per server 4-frame multi-frame payload area.
- The maximum number_of_m [=1028] bit GMP data entities per 4-frame multi-frame payload is $P_{m,server}$ [=10220].
- For 400ZR, we use n = [m / 128] = [4×257-bit]/128 = 8.03125 UI that is used as a phase unit "n-bit equivalent" for C_n parameter. C_n indicates the number of "n-bit equivalent" of the 400GBASE-R client per 400ZR 4-frame multi-frame server payload. It can be used as a finer phase indicator to encode the client clock at the GMP mapper.
- So, $C_{n, nom} = 128 \times C_{m, nom}$; $C_{n, min} = 128 \times C_{m, min}$; $C_{n, max} = 128 \times C_{m, max}$
- $C_m = P_{m,server} \times$ [client_bit_rate / Server_Payload_bit_rate].
- C_m is an integer value indicating to every 400ZR frame the number of m-bit client blocks carried [m = 4×257b = 1028b] in this 400ZR 4-frame server multi-frame payload = int($P_{m,server}$×[client_bit_rate/Server_Payload_bit_rate]).
- $C_m \leq P_{m,server}$ and is a value varying between $C_{m,min}$ and $C_{m,max}$ for the given client and payload type, due to client and payload bit rate tolerance range (+/- 100 ppm and +/-20 ppm).

8.9.1 Stuffing Locations

Stuff location determination for GMP uses a delta-sigma algorithm based on the Cm value over the total number of payload location. GMP is a positional mapping with non-fixed stuff. So, the stuff location will vary on a GMP payload-by-payload basis, based on the $C_m(t)$ value. In the case of 400ZR the GMP payload covers four 400ZR frames.

Table 7 shows the location of the "stuff" GMP blocks for a few specific C_m values.

C_m	GMP Blocks Number of Stuff Locations
10220	N/A
10219	1
10218	1, 5111
10217	1, 3407, 6814
10216	1, 2556, 5111, 7666
10215	1, 2045, 4089, 6133, 8177
10214	1, 1704, 3407, 5111, 6814, 8517

Table 7: GMP stuff locations of 400ZR

Figure 19 shows an example of GMP stuff opportunities over four 400ZR frames.

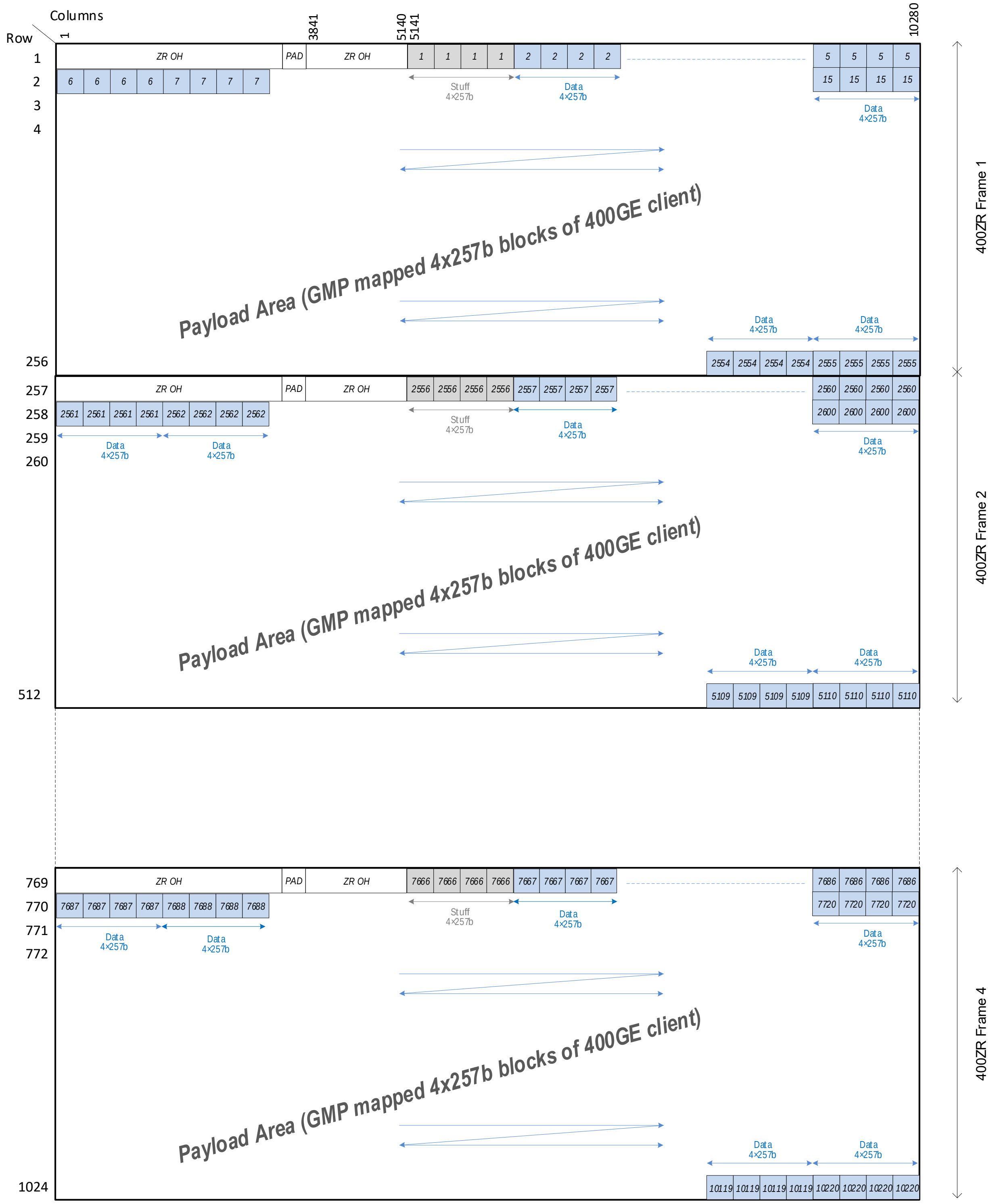


Figure 19: GMP mapping over four 400ZR frames with C_m=10216

8.9.2 GMP overhead Encoding

GMP overhead (JC Bytes OH) is carried once per GMP payload envelope (combining four consecutive 400ZR frame payloads), so once per 4-frame multi-frame. GMP overhead carries the encoded 14-bit Cm(t) (i.e. 4×257b block count value) in C1-14 bits of JC1 & JC2 (C1 = MSB, ..,C14= LSB) and the encoded 7-bit $\Sigma C_{nD}(t)$ (cumulative value of $C_{nD}(t)$) in D1-D7 bits of JC4 & JC5 (D1=MSB,.. , D7 = LSB) GMP parameters.

$C_m(t)$ is protected by a CRC8 (carried in JC3 OH byte) and $\Sigma C_{nD}(t)$ is protected by a CRC4 (carried in the four LSBs of JC6 OH byte).

The JC3 OH CRC8 calculation is described in ITU-T G.709 Annex D.3, and an example of a parallel implementation can be found in ITU-T G.709 Appendix VI.

8.9.3 GMP OH – CRC8 calculation

The CRC8 located in JC3 is calculated over the JC1 and JC2 bits. The CRC8 uses the generator polynomial:

$$g(x) = x^8 + x^3 + x^2 + 1$$

- The JC1 and JC2 octets are taken in order, most significant bit first, to form a 16-bit pattern representing the coefficients of a polynomial M(x) of degree 15.
- M(x) is multiplied by x^8 and divided (modulo 2) by G(x), producing a remainder R(x) of degree 7 or less.
- The coefficients of R(x) are considered to be an 8-bit sequence, where x^7 is the most significant bit.
- This 8-bit sequence is the CRC8 where the MSB of the CRC8 is the coefficient of x^7 and the LSB is the coefficient of x^0.

The de-mapper process performs steps 1-3 in the same manner as the mapper process, except that here, the M(x) polynomial of step 1 includes the CRC bits of JC3, resulting in M(x) having degree 23. In the absence of bit errors, the remainder shall be 0000 0000.

8.9.4 The JC6 OH CRC4 Calculation

The CRC4 located in JC6 uses the generator polynomial:

$$g(x) = x^4 + x + 1.$$

- The four least significant bits of the JC4 and JC5 octets (JC4 D1-D4 and JC5 D5-D7 + RES) are taken in order, most significant bit first, to form an 8-bit pattern representing the coefficients of a polynomial M(x) of degree 7.
- M(x) is multiplied by x^4 and divided (modulo 2) by G(x), producing a remainder R(x) of degree 4 or less.
- The coefficients of R(x) are considered to be a 4-bit sequence, where x^3 is the most significant bit.
- This 4-bit sequence is the CRC4 where the MSB of the CRC4 is the coefficient of x^3 and the LSB is the coefficient of x^0.

The de-mapper process performs steps 1-3 in the same manner as the mapper process, except that here, the M(x) polynomial of step 1 includes the CRC bits of JC6, resulting in M(x) having degree 11. In the absence of bit errors, the remainder shall be 0000.

9 400ZR frame to SC adaptation

Figure 20 and Figure 24 show the relationship of the 400ZR frame mapping to the SC-FEC block.

- 119 rows×[2×5140-bit] of information (1223320 bits) + 119×[2×345 bit] of FEC parity (81920 bits) and pad (190 bits) is mapped to 5×SC-FEC Blocks.
- One SC-FEC frame [510b×512b] carries 952×257-bit blocks of information + CRC32 + 6-bit MBAS + 34-bit zero stuff (261120 bits).

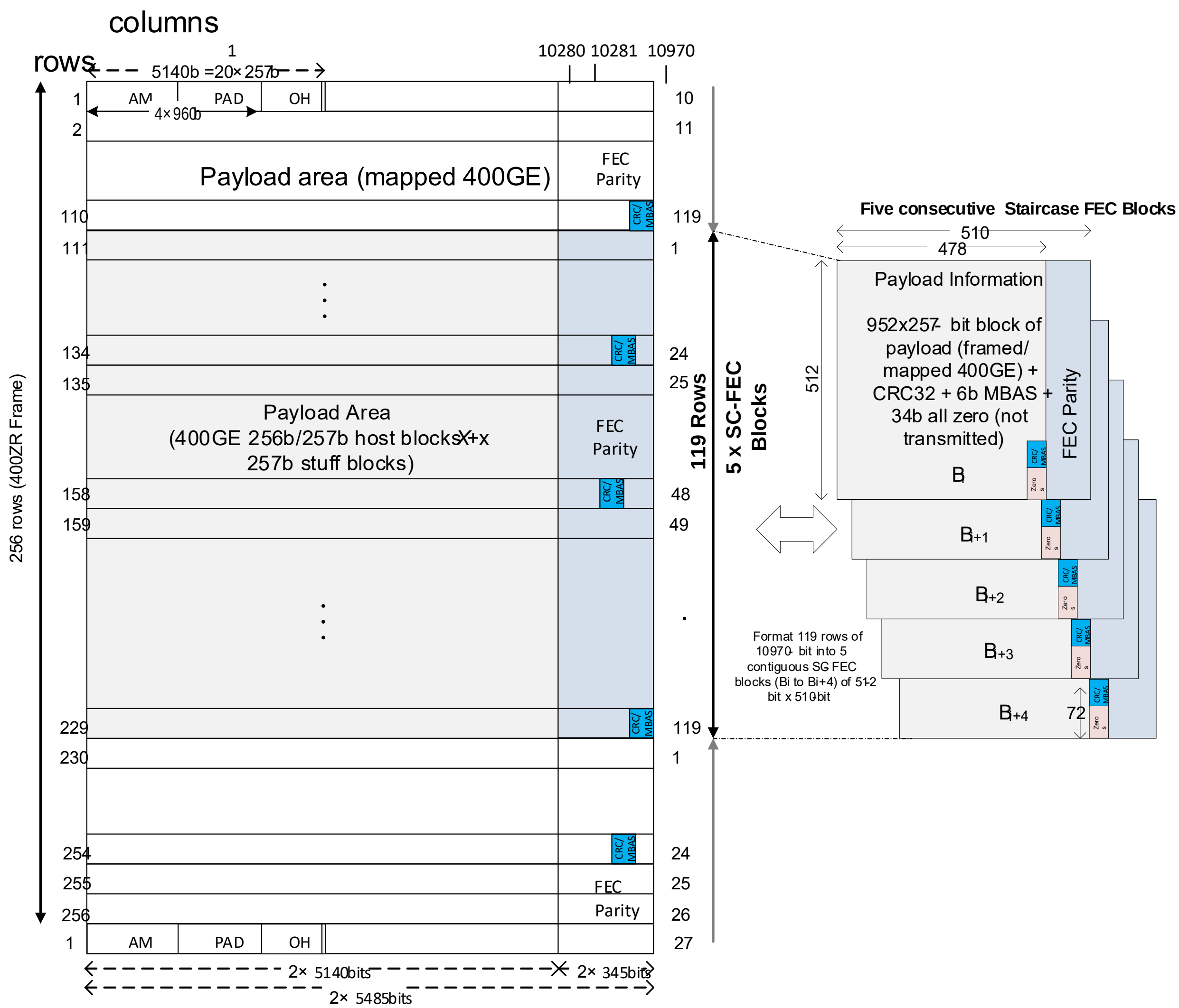


Figure 20: 400ZR frame to SC-FEC relationship

9.1 Mapping 400ZR Frame Payload to Staircase FEC Blocks

The payload of a 400ZR frame is mapped into units of 244,664 bits, where 244,664 = 512×478-72 consecutive bits. For every 244,664 consecutive bits a 32-bit CRC (ref. section 9.2) is calculated, plus a 6-bit Multi-Block Alignment Signal (MBAS) is added forming the CRC(32B)+MBAS(6b) block. The CRC+MBAS (38b) block is inserted at the end of each parity block (ref. Figure 21).

Each SC-FEC frame contains 261120 bits (244664b of payload + 16384b of FEC parity bits + 32 bits of CRC + 6b of MBAS + 34b of pad). The 34b of additional pad is not transmitted. In the Figure 23, the 38-bit CRC+MBAS is shown located at the end of each parity block.

Information and parity bits in 119 400ZR frame rows (119×10970 bits) or (1305430 bits), can be represented in 5 SC blocks organized as 5×32640x8 bits – 34 bits of pad that is not transmitted). See Figure 24 left and right side.

- 400ZR Information block boundaries are thus located at the 23.8th, 47.6th, 71.4th, 95.2th and 119th rows and at columns 8224, 6184, 4112, 2056 and 10280.
- Parity block boundaries are thus at parity columns 138, 276, 414, 552 and 690 (or columns 10418, 10556, 10694, 10832 and 10970).

9.2 400ZR CRC+MBAS Bit Insertion Block

A 32-bit CRC is calculated over the 244,664 input bits with the generator polynomial IEEE 802.3 (Hammond, et.al. [1]).

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x + 1,$$

appended to the end of the sequence.

Mathematically, the CRC value corresponding to the 244,664 input bits is defined by the following procedures:

- The first 32 bits of the frame are complemented.
- The 244,664 bits of the protected fields are the coefficients of a polynomial $M(x)$ of degree 244,663. (The first bit of the 244,664 input bits corresponds to the $x^{244,663}$ term and the last bit of the 244,664 input bits corresponds to the x^0 term).
- $M(x)$ is multiplied by x^{32} and divided (modulo 2) by $G(x)$, producing a remainder *R*(x) of degree $\le$ 31.
- The coefficients of *R*(x) are a 32-bit sequence.
- The bit sequence is complemented, and the result is the CRC.

The 32 bits of the CRC value are placed with the x^{31} term as the left-most bit of the CRC32 field and the x^0 term as the right-most bit of the CRC32 field. (The bits of the CRC are thus transmitted in the order: $x^{31}, x^{30}, \dots, x^1, x^0$). The 6-bit MBAS is appended after the 32-bit CRC

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32	33 34 35 36 37 38
CRC32	MBAS

Figure 21: CRC32 + MBAS

9.2.1 400ZR Multi Block Alignment Signal (MBAS)

To synchronize the state of the Error De-correlator (ED) controllers between the receiver and the transmitter, the Staircase FEC scheme uses a 7-bit SC FEC Multi Block Alignment Signal (MBAS) which provides a 128-block sequence.

The six most significant bits of the 7-bit MBAS are transferred between source and sink in the 6-bit MBAS overhead, which is located in bits 33 to 38 in Figure 21.

The numerical value represented in the six MBAS overhead bits will be incremented every two SC FEC blocks and provides as such a 128-block multi-block as illustrated in Figure 22.

	7-bit Multi-Block Alignment Signal						
	1	2	3	4	5	6	7
	6-bit MBAS OH						
	33	34	35	36	37	38	
			:				
0	0	0	0	0	0	0	*0*
1	0	0	0	0	0	0	*1*
2	0	0	0	0	0	1	*0*
3	0	0	0	0	0	1	*1*
4	0	0	0	0	1	0	*0*
5	0	0	0	0	1	0	*1*
6	0	0	0	0	1	1	*0*
7	0	0	0	0	1	1	*1*
			:				:
			:				:
125	1	1	1	1	1	0	*1*
126	1	1	1	1	1	1	*0*
127	1	1	1	1	1	1	*1*
0	0	0	0	0	0	0	*0*
1	0	0	0	0	0	0	*1*
2	0	0	0	0	0	1	*0*
			:				:

Figure 22: Multi-block alignment signal overhead

Figure 23 shows the location and transmission order of the CRC32 and MBAS.

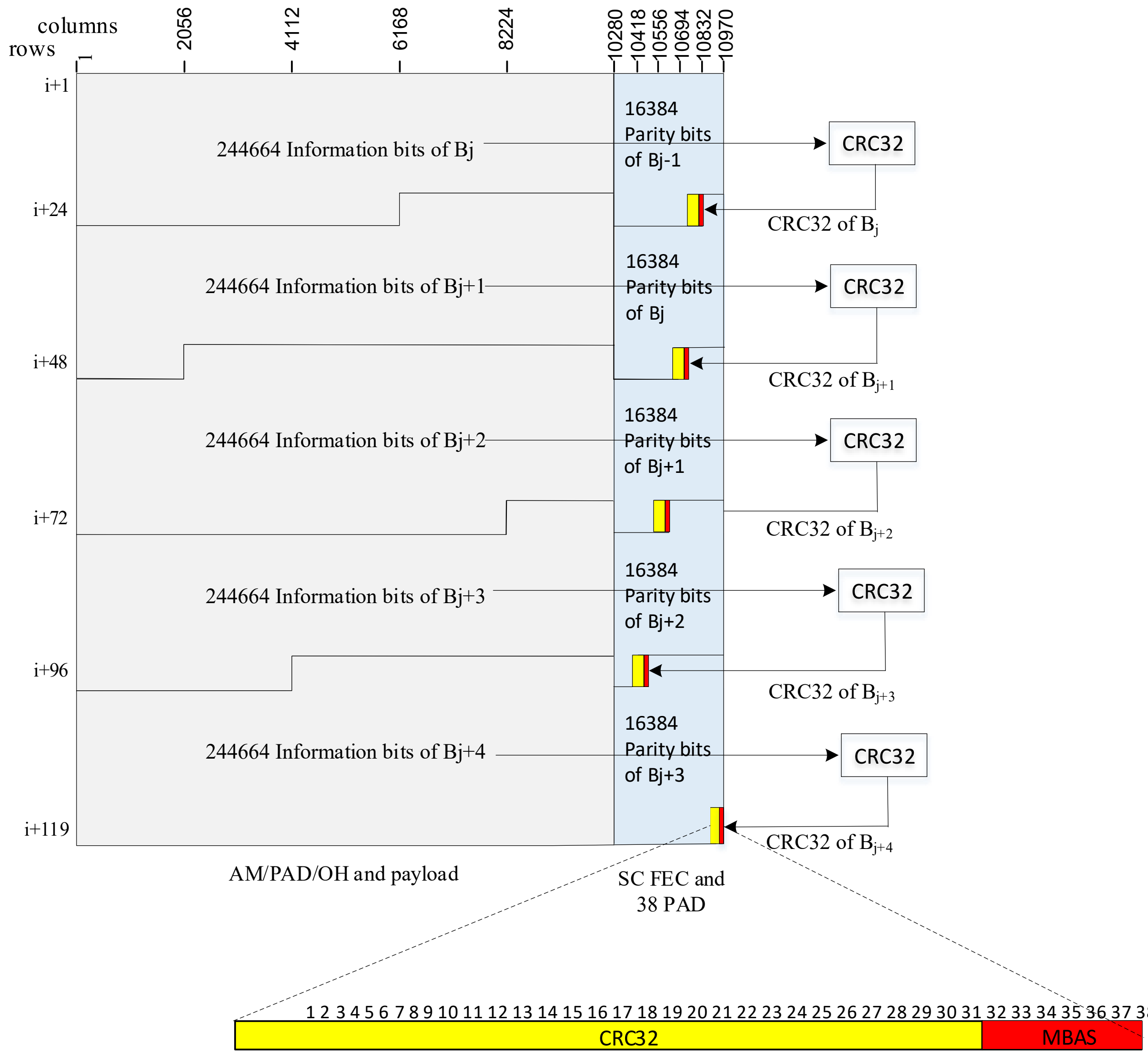


Figure 23: CRC32 + MBAS transmission order

Figure 24 details the 400ZR frame to SC-FEC adaptation.

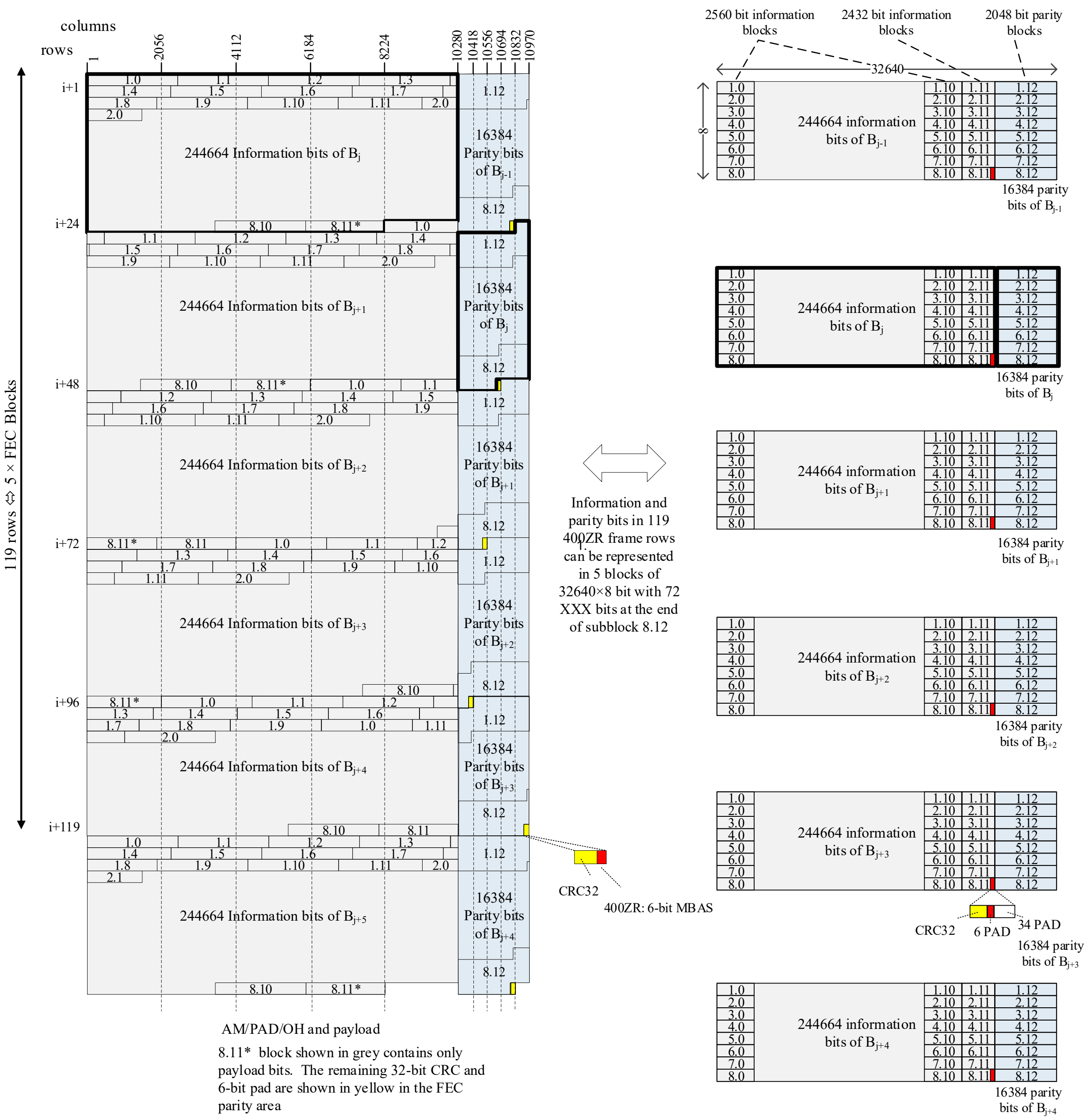


Figure 24: 400ZR frame adaptation SC FEC block

10 400ZR Forward Error Correction (FEC)

The 400ZR Forward Error Correction (FEC) algorithm is a Concatenated FEC (C-FEC) that combines a HD-FEC (255,239) outer code and an inner double-extended SD-FEC (128,119) Hamming code resulting in ~10.8dB of NCG with ~14.8% overhead (e.g. BER_in = 1.25E-2 results in BER_out = 1.0E-15).

The HD-FEC is a (512-bit × 510-bit) generalized staircase code that works in conjunction with an error de-correlator. The error de-correlator function randomizes the position of the symbols to reduce the impact of correlated errors on the FEC performance.

10.1 SC-FEC

For the purposes of this IA and to minimize the possibility of misinterpretation that might deviate from a common implementation the SC-FEC, Adapt, ED and Encoding/Decoding processes shown in Figure 25 are defined by reference [5] Annex A.

Figure 25: 400ZR HD-FEC processes

10.2 Sync Pad Insertion

For the purpose of alignment and synchronization 6×119 bits are appended/removed from the tail end of the 5xSC-FEC block.

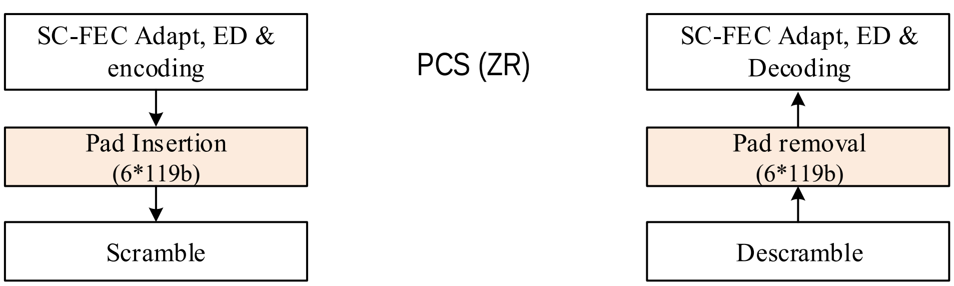


Figure 26: Pad insertion/removal

Figure 27 shows the location of 6 ×119b pad relative to the 400ZR Frame.

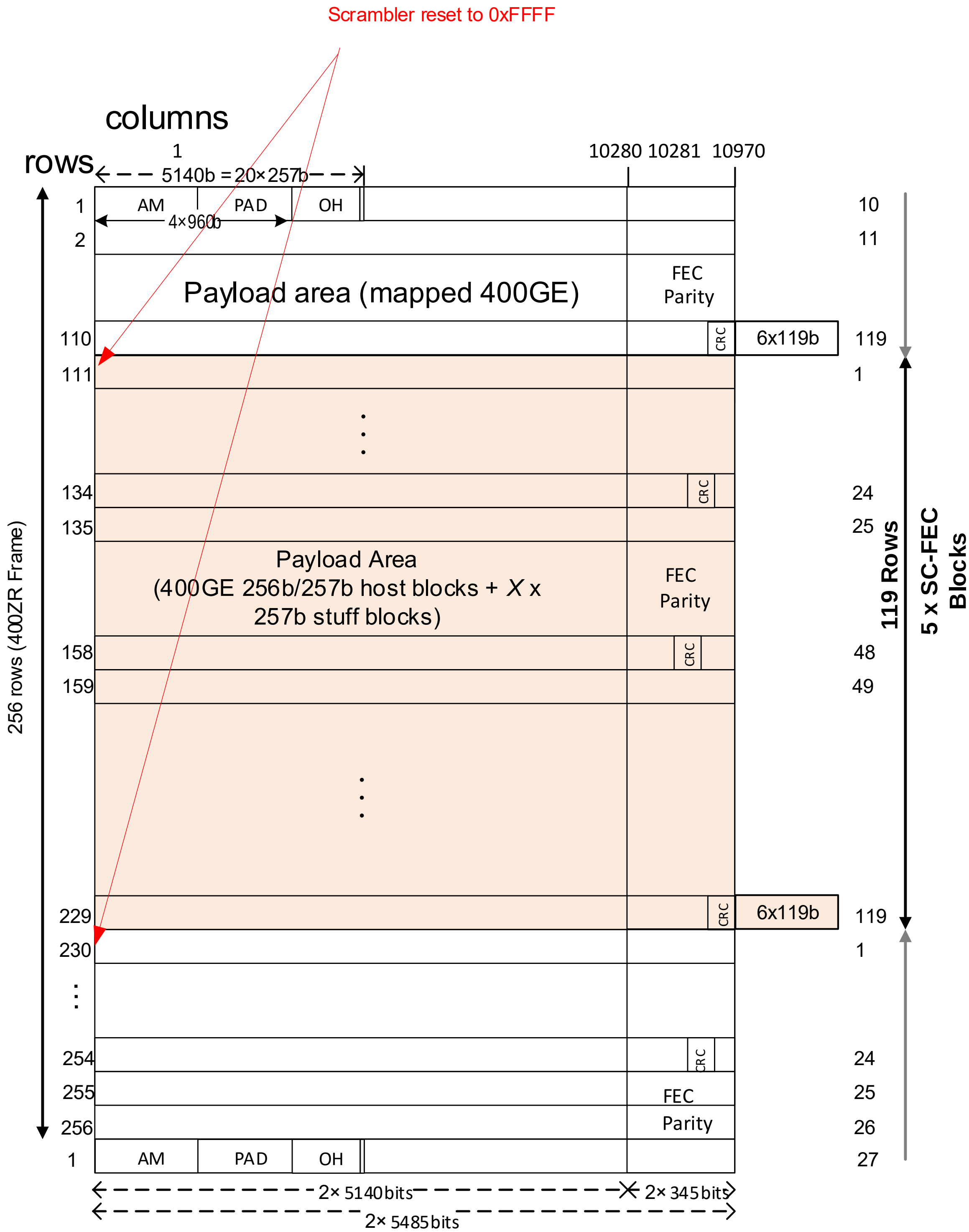


Figure 27: 6 × 119 Pad Insertion

10.3 Frame Synchronous Scrambling

The scrambler/descrambler is located after/before the SC-FEC encoding and 6 ×119b pad insertion.

Figure 28: Frame synchronous scrambler

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous scrambler of sequence 65535 and the generating polynomial shall be:

$$x^{16} + x^{12} + x^{3} + x + 1.$$

The scrambler/descrambler resets to 0xFFFF on row 1, column 1 of the five SC-FEC block structure and subsequent 714-bit (6 x 119b) pad insertion and the scrambler state advances during each bit of the 5xSC-FEC blocks. In the source function, all payload bits (included SC-FEC parity) are scrambled. At the sink the scrambler is synchronized (initialized) at the start of each payload.

10.4 Convolutional Interleave

The staircase encoded frame + 6 Sync/Pad, which consists of 10976×119 bits, is first interleaved (in units of 119 bits) by a convolutional interleave (CI). The CI serves to spread out the transmission order of consecutive units of 119 bits from the staircase encoded frame, which increases the resilience of the system to bursts of errors.

Figure 29: Convolution interleave

The CI is of depth 16, that is, it consists of 16 parallel delay lines, as illustrated in Figure 30.

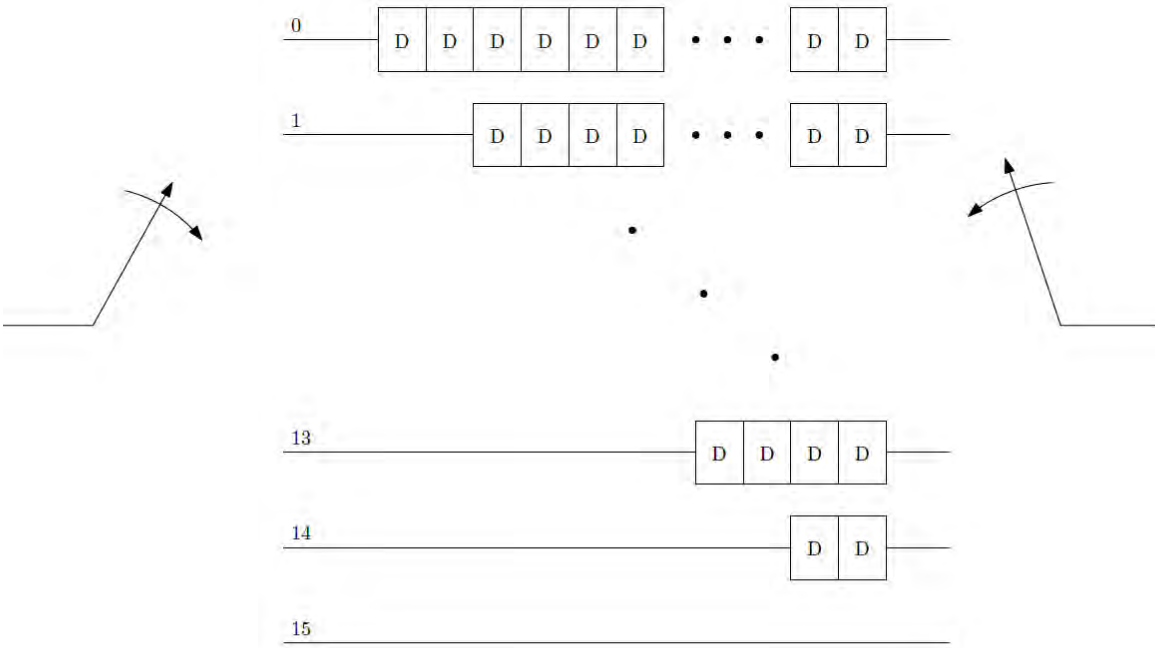


Figure 30: Convolution interleave

Each delay operator "D" represents a storage element of 119b. From one row to the next lower row, two delays operators are deleted.

At time i, the input and output switches are aligned at row b_i:

- A block of 119b is read from row b_i
- The contents of row b_i are shifted to the right by 119b
- A block of 119b is written to row b_i
- The switch position is updated to $b_{i+1} = b_i + 1\ (mod\ 16)$

Initialization of the convolutional interleave switches (to their topmost positions) is defined to occur at the start of every DSP super frame, which contains 5 SC-FEC blocks (i.e. immediately prior to processing the first row in Figure 27). Since 10976 is evenly divisible by the depth of the CI (i.e. 16), the switches will wrap around to this position at the start of every ZR frame. The start of the DSP super frame emitted from the CI will align with the first block of data emitted following a re-initialization of the interleaving switches.

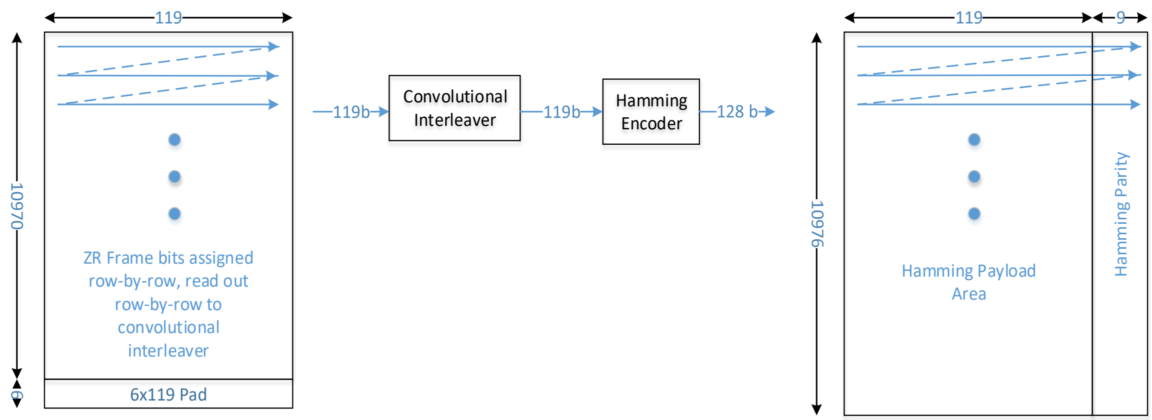


Figure 31: Hamming FEC frame format

The 119b outputs of the convolutional interleave are encoded by a systematic (128,119) double-extended Hamming code.

10.5 Inner Hamming Code

The inner FEC of C-FEC is a double-extended Hamming Code SD-FEC (128,119), increasing NCG from 9.4 dB to ~10.8 dB with ~7.56% added overhead.

Figure 32: Hamming code

The systematic double-extended Hamming code is most naturally defined in terms of its parity-check matrix. Consider the function g which maps an integer $i, 0 \le i \le 127$, to the column vector:

$$g(i) = \begin{bmatrix} s_{0,i} \\ s_{1,i} \\ \vdots \\ s_{6,i} \\ s_{7,i} \\ 1 \end{bmatrix},$$

where,

$$i = 64s_{6,i} + 32s_{5,i} + \cdots + 2s_{1,i} + s_{0,i},$$

and,

$$s_{7,i} = (s_{0,i} \wedge s_{2,i}) \vee (\overline{s_{0,i}} \wedge \overline{s_{1,i}} \wedge \overline{s_{2,i}}) \vee (s_{0,i} \wedge s_{1,i} \wedge \overline{s_{2,i}}).$$

The parity-check matrix is then a 9×128 binary matrix:

$$H = [g(0)\colon g(62), g(64)\colon g(94), g(96)\colon g(110), g(112)\colon g(118), g(120), g(122), g(124),$$
$$g(63), g(95), g(111), g(119), g(121), g(123), g(125)\colon g(127)]$$

where g(a):g(b) represents:

$$[g(a), g(a+1), g(a+2), \ldots, g(b)]$$

To obtain the encoder matrix G, we calculate

$$P = B[g(0)\colon g(62), g(64)\colon g(94), g(96)\colon g(110), g(112)\colon g(118), g(120), g(122), g(124)]$$

where,

$$B = [\, g(63), g(95), g(111), g(119), g(121), g(123), g(125)\colon g(127)]^{-1}$$

Finally, the generator matrix of the Hamming code is,

$$G = [I; P^T],$$

and a 119-bit message,

$$b = [b_0, b_1, \ldots, b_{118}]$$

is encoded to the 128-bit code word.

$$c = [c_0, c_1, \ldots, c_{127}] = bG$$

11 DP-16QAM Symbol mapping and polarization distribution

Each 128-bit code word is mapped to 16 DP-16QAM symbols (S),

$$S = [s_0, s_1, \dots, s_{15}],$$

where,

- (c_{8i}, c_{8i+1}) maps to the in-phase (I) component of the X-pol of s_i
- (c_{8i+2}, c_{8i+3}) maps to the quadrature-phase (Q) component of the X-pol of s_i
- (c_{8i+4}, c_{8i+5}) maps to the I component of the Y-pol of s_i
- (c_{8i+6}, c_{8i+7}) maps to the Q component of the Y-pol of s_i

In each signaling dimension, we define the following mapping from binary label to symbol amplitude:

(0,0)→−3,(0,1)→−1,(1,1)→+1,(1,0)→+3

This mapping is further detailed in Table 8 below:

$(c_{8i}, c_{8i+1,} c_{8i+2,} c_{8i+3})$ or $(c_{8i+4}, c_{8i+5,} c_{8i+6,} c_{8i+7})$	I	Q
(0,0,0,0)	-3	-3
(0,0,0,1)	-3	-1
(0,0,1,0)	-3	3
(0,0,1,1)	-3	1
(0,1,0,0)	-1	-3
(0,1,0,1)	-1	-1
(0,1,1,0)	-1	3
(0,1,1,1)	-1	1
(1,0,0,0)	3	-3
(1,0,0,1)	3	-1
(1,0,1,0)	3	3
(1,0,1,1)	3	1
(1,1,0,0)	1	-3
(1,1,0,1)	1	-1
(1,1,1,0)	1	3
(1,1,1,1)	1	1

Table 8: In-phase (I) and quadrature phase (Q) symbol amplitude

11.1 Interleaving DP-16QAM Symbols

The DP-16QAM symbols are time-interleaved, to de-correlate the noise between consecutively received symbols, as well as to uniformly distribute the symbols (mapped from a single Hamming code word) between pilot symbols.

Prior to Fame Alignment Word (FAW) and pilot insertion, each frame consists of 10976×16 DP-16QAM symbols. The symbol interleave performs an 8-way interleaving of symbols from Hamming code words.

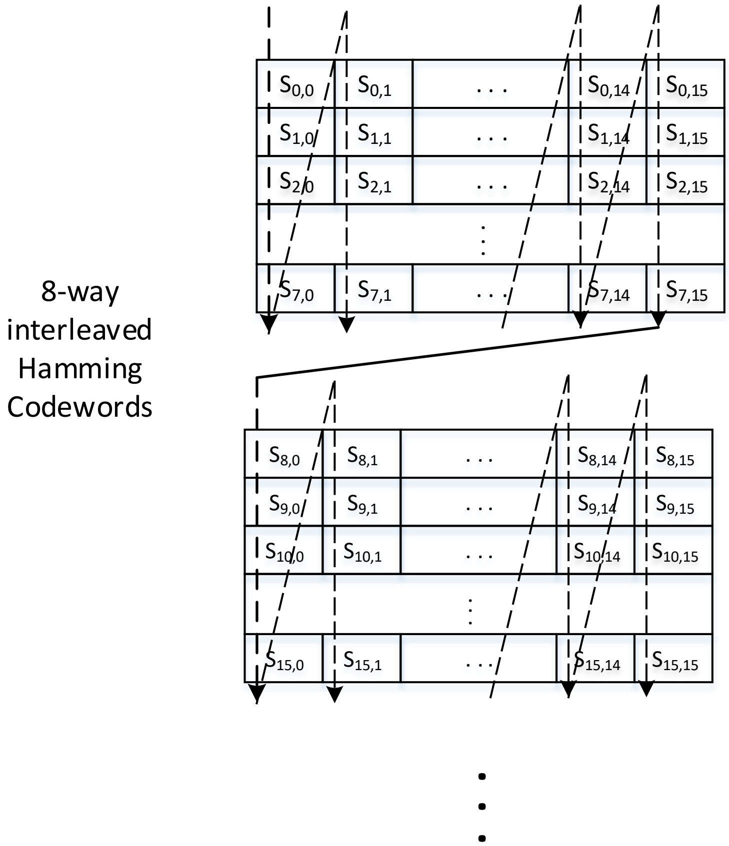


Figure 33: Hamming code 8-way interleave

12 DSP framing

A DSP super-frame is defined as a set of 181888 symbols in each of the X/Y polarization. A DSP sub-frame consists of 3712 symbols. A DSP super-frame thus consists of 49 DSP sub-frames.

Pilot symbols are inserted every 32 symbols, starting with the first symbol of each DSP super-frame. The first 11 symbols of the DSP sub-frame can also be used for training (e.g. frame acquisition). The first symbol of the Training Sequence (TS) is a Pilot Symbol (PS).

- Every DSP subframe has the same structure based on a fixed TS with the first symbol processed as a pilot.
- The TS includes 11 QPSK symbols for each polarization. The TS is different between X and Y polarizations
- The PS sequence includes (1+115) QPSK symbols based on PRBS. The first TS symbol is also the first symbol of the PS sequence.

12.1 First DSP sub-Frame

The first DSP sub-frame of the super-frame includes a 22 symbol Frame Alignment Word (FAW) used to align to the 5 SC-FEC Frames. 76 additional symbols are reserved for future use/innovation.

The First DSP sub-frame includes:

- 22 symbols used as the Super Frame Alignment Word (FAW). The FAW is different between X and Y polarizations.
- 76 symbols are reserved to be used for future proofing and for innovation. These symbols should be randomized to avoid strong tones. These symbols should be selected from 16QAM modulation.

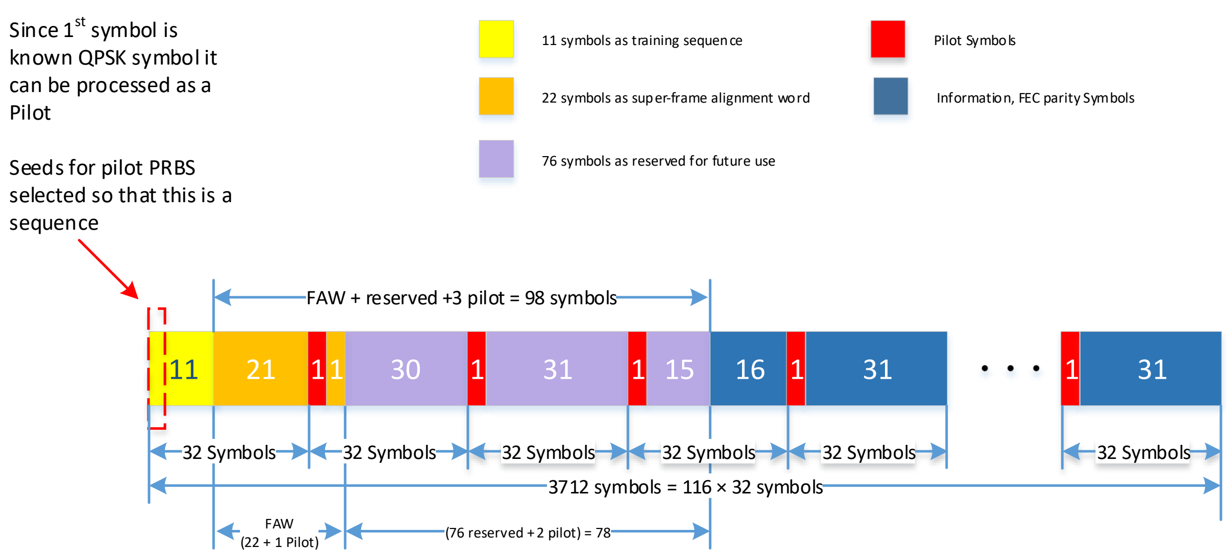


Figure 34: First DSP sub-frame of super-frame

12.1.1 FAW Sequence

Index	FAW X	FAW Y	Index	FAW X	FAW Y
1	3 - 3j	3 + 3j	**12**	3 - 3j	-3 + 3j
2	3 + 3j	-3 + 3j	**13**	-3 - 3j	-3 + 3j
3	3 + 3j	-3 - 3j	**14**	-3 - 3j	3 + 3j
4	3 + 3j	-3 + 3j	**15**	-3 + 3j	-3 - 3j
5	3 - 3j	3 - 3j	**16**	3 + 3j	3 + 3j
6	3 - 3j	3 + 3j	**17**	-3 - 3j	-3 - 3j
7	-3 - 3j	3 - 3j	**18**	3 - 3j	-3 + 3j
8	3 + 3j	3 - 3j	**19**	-3 + 3j	3 - 3j
9	-3 - 3j	-3 - 3j	**20**	3 + 3j	-3 - 3j
10	-3 + 3j	3 - 3j	**21**	-3 - 3j	3 - 3j
11	-3 + 3j	3 + 3j	**22**	-3 + 3j	-3 + 3j

Table 9: FAW sequence

12.2 Subsequent DSP sub-frames.

Each subsequent DSP sub-frame after the first includes an 11 symbol TS, the first symbol of which is a PS.

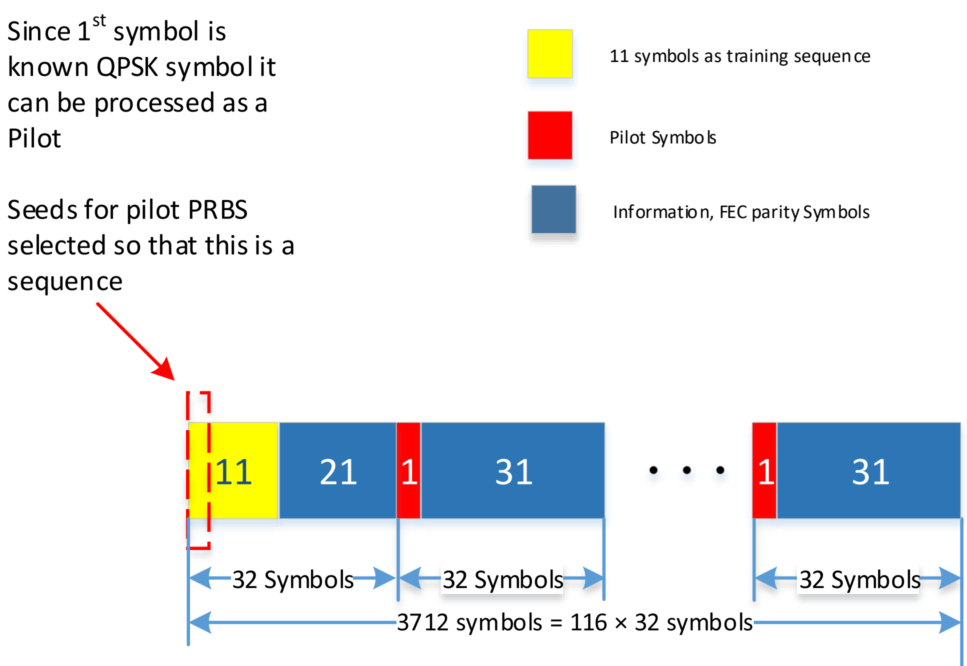


Figure 35: DSP sub-frames 2-49 of the DSP super-frame

12.2.1 Training Sequence

The TS is defined by the following table:

Index	Training X	Training Y
1*	-3 + 3j	-3 - 3j
2	3 + 3j	-3 - 3j
3	-3 + 3j	3 - 3j
4	3 + 3j	-3 + 3j
5	-3 - 3j	-3 + 3j
6	3 + 3j	3 + 3j
7	-3 - 3j	-3 - 3j
8	-3 - 3j	-3 + 3j
9	3 + 3j	3 -3j
10	3 - 3j	3 + 3j
11	3 - 3j	3 - 3j

Table 10: Training symbol sequence

*The first symbol of the TS is processed as a pilot

12.3 Pilot Sequence

Training symbols and pilot symbols shall be set at the outer 4 points of the 16QAM constellation. See Figure 36.

The PS is a fixed PRBS10 sequence mapped to QPSK with different seed values for X/Y.

- Seeds are selected so that the pilot and training sequence combined are DC balanced
- Seeds are selected so that the first symbol in the training sequence is also the first symbol in the pilot sequence
- The seed is reset at the start of every DSP sub-frame

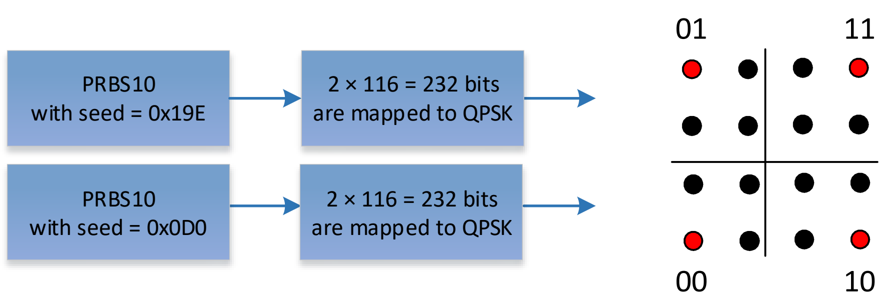


Figure 36: QPSK mapped Pilot Sequence

Table 11 shows the pilot generator polynomial and seed values.

Generator polynomial	Seed X	Seed Y
$x^{10} + x^8 + x^4 + x^3 + 1$	0x19E	0x0D0

Table 11: Pilot polynomial and seed

Figure 37 shows the sequencing.

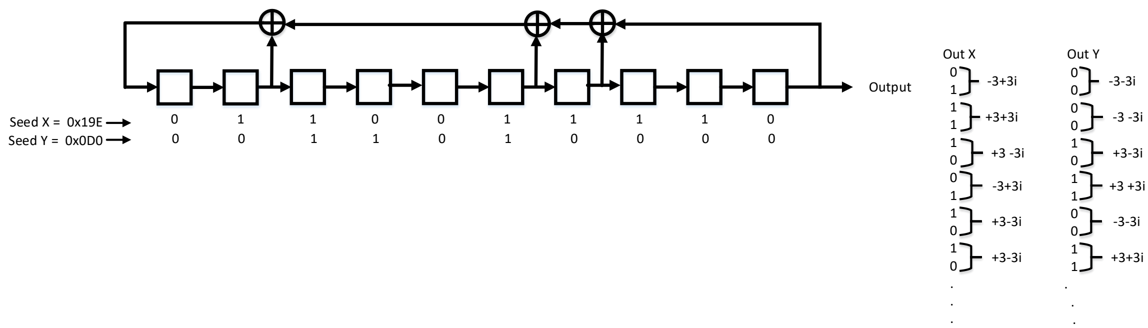


Figure 37: Pilot seed and sequence

The complete table is shown below:

Index	Pilot X	Pilot Y	Index	Pilot X	Pilot Y	Index	Pilot X	Pilot Y	Index	Pilot X	Pilot Y
1	-3 + 3j	-3-3j	**30**	3 - 3j	3-3j	**59**	3 - 3j	3-3j	**88**	3 - 3j	-3+3j
2	3 + 3j	-3-3j	**31**	-3 - 3j	-3+3j	**60**	3 + 3j	-3+3j	**89**	-3 - 3j	-3+3j
3	3 - 3j	3-3j	**32**	3 + 3j	-3-3j	**61**	3 - 3j	3+3j	**90**	3 - 3j	3-3j
4	-3 + 3j	3+3j	**33**	-3 + 3j	3-3j	**62**	-3 - 3j	-3-3j	**91**	3 - 3j	3+3j
5	3 - 3j	-3-3j	**34**	-3 + 3j	-3-3j	**63**	3 - 3j	3+3j	**92**	-3 + 3j	3-3j
6	3 - 3j	3+3j	**35**	-3 + 3j	-3-3j	**64**	-3 + 3j	-3+3j	**93**	-3 - 3j	3-3j
7	-3 - 3j	-3+3j	**36**	3 - 3j	3-3j	**65**	3 - 3j	3-3j	**94**	3 + 3j	-3+3j
8	3 + 3j	-3+3j	**37**	3 - 3j	3-3j	**66**	3 + 3j	3+3j	**95**	-3 - 3j	3-3j
9	-3 + 3j	-3-3j	**38**	-3 - 3j	-3-3j	**67**	3 - 3j	-3-3j	**96**	-3 - 3j	3-3j
10	3 + 3j	3+3j	**39**	-3 - 3j	3+3j	**68**	-3 + 3j	3-3j	**97**	3 + 3j	-3+3j
11	3 + 3j	3+3j	**40**	3 - 3j	-3-3j	**69**	3 - 3j	-3+3j	**98**	-3 + 3j	3-3j
12	-3 - 3j	-3-3j	**41**	-3 - 3j	3-3j	**70**	-3 + 3j	-3+3j	**99**	3 - 3j	-3-3j
13	3 + 3j	3+3j	**42**	3 - 3j	3-3j	**71**	3 + 3j	-3+3j	**100**	-3 - 3j	3+3j
14	3 - 3j	3+3j	**43**	-3 + 3j	-3-3j	**72**	-3 - 3j	-3-3j	**101**	3 + 3j	-3-3j
15	3 + 3j	3-3j	**44**	-3 + 3j	-3-3j	**73**	-3 - 3j	-3+3j	**102**	-3 + 3j	-3+3j
16	3 - 3j	3+3j	**45**	-3 - 3j	3+3j	**74**	3 - 3j	3+3j	**103**	-3 - 3j	-3+3j
17	3 + 3j	3+3j	**46**	-3 + 3j	-3+3j	**75**	-3 + 3j	-3-3j	**104**	-3 - 3j	3+3j
18	3 - 3j	-3+3j	**47**	-3 - 3j	3+3j	**76**	3 - 3j	-3-3j	**105**	3 + 3j	-3+3j
19	-3 + 3j	-3-3j	**48**	3 + 3j	-3+3j	**77**	-3 + 3j	-3-3j	**106**	3 - 3j	3-3j
20	-3 - 3j	3-3j	**49**	3 + 3j	3-3j	**78**	-3 - 3j	3+3j	**107**	3 + 3j	3+3j
21	3 + 3j	3-3j	**50**	-3 + 3j	-3+3j	**79**	3 + 3j	-3-3j	**108**	-3 + 3j	-3+3j
22	-3 + 3j	3+3j	**51**	3 - 3j	3+3j	**80**	3 + 3j	-3-3j	**109**	-3 - 3j	3+3j
23	-3 + 3j	-3+3j	**52**	3 - 3j	-3+3j	**81**	3 + 3j	3-3j	**110**	-3 + 3j	-3-3j
24	3 - 3j	3-3j	**53**	3 - 3j	-3+3j	**82**	-3 - 3j	-3-3j	**111**	-3 - 3j	-3+3j
25	-3 + 3j	3-3j	**54**	-3 - 3j	3+3j	**83**	-3 - 3j	3+3j	**112**	-3 + 3j	3-3j
26	-3 + 3j	3+3j	**55**	3 - 3j	-3+3j	**84**	3 + 3j	-3-3j	**113**	-3 + 3j	-3+3j
27	-3 + 3j	-3+3j	**56**	3 + 3j	-3+3j	**85**	3 - 3j	-3-3j	**114**	3 + 3j	3+3j
28	-3 + 3j	3+3j	**57**	-3 + 3j	-3-3j	**86**	-3 + 3j	-3-3j	**115**	3 + 3j	3-3j
29	-3 - 3j	3+3j	**58**	-3 - 3j	3-3j	**87**	3 + 3j	3-3j	**116**	-3 - 3j	3-3j

Table 12: Pilot Sequence

12.4 Channel Mappings

X and Y indicate a pair of mutually orthogonal polarizations of any orientation and I and Q are mutually orthogonal phase channels in each polarization. The four data path channels are therefore labeled XI, XQ, YI, and YQ.

All coherent channel mappings provided in Table 13 are allowed for the Tx signal. The Rx should work in all cases because the Rx can unambiguously identify the signals polarization and phase, based on the FAW.

The Tx mapping is specified in Table 13 by two designations: [X:Y ; I,Q], where a ":" is used to separate X & Y, a "," is used to separate I & Q.

Table 13 *does not* allow interleaving of the channels by polarization since this would add a non-essential level of complexity to the Rx digital processing.

Mapping	X:Y	I,Q	Notes
[0,x]	**X:Y**		Pol. cannot be interleaved
[1,x]	**Y:X**		
[x,0]		**I,Q:I,Q**	Same across Pol.
[x,1]		**Q,I:Q,I**	
[x,2]		**I,Q:Q,I**	Flip across Pol.
[x,3]		**Q,I:I,Q**	

Table 13: Channel mappings

12.5 Frame Expansion Rate

The 400ZR optical signal is DP-16QAM with a symbol rate of 59.843750000 Gbaud (478.750 Gbps) per polarization. Figure 38 and Table 14 provide details on expansion for each functional block.

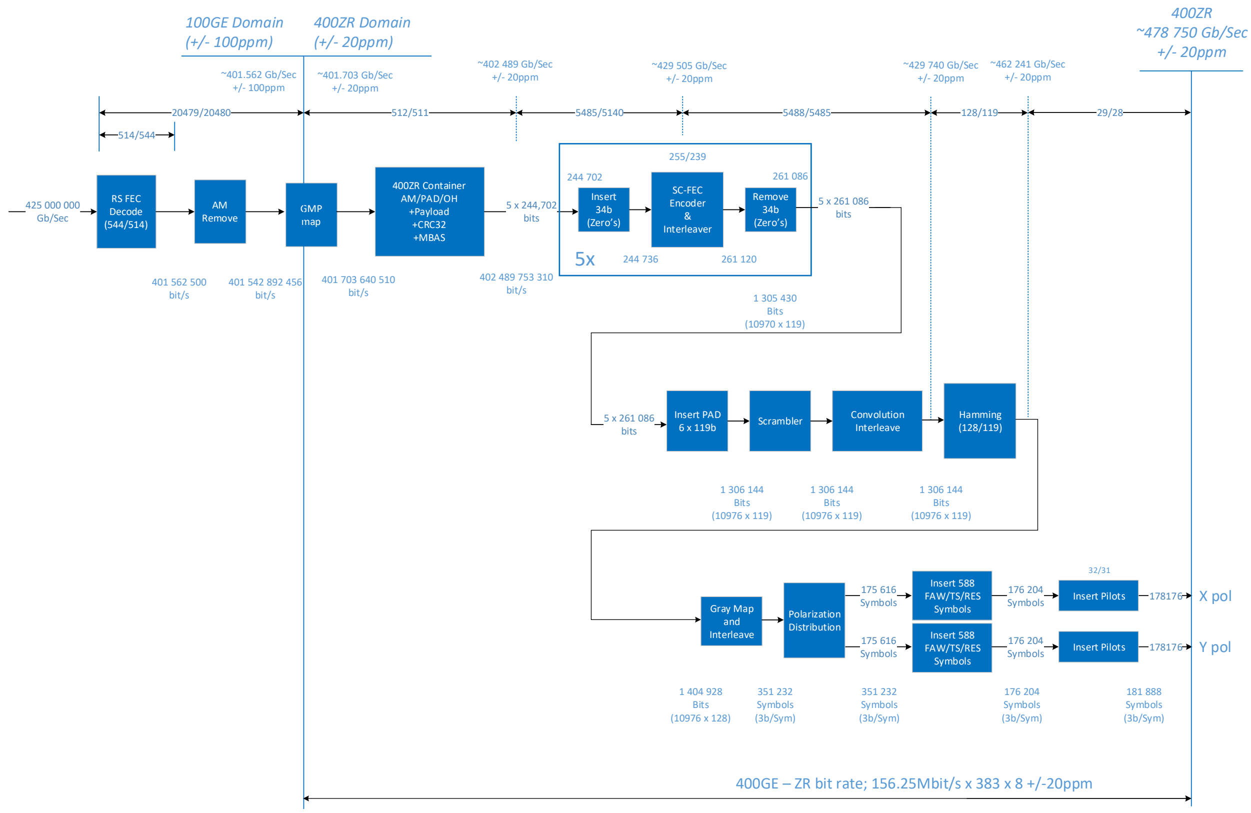


Figure 38: 400ZR expansion rates

Table 14 details the bit level expansion.

GMP

FlexO/400ZR frame

	400GBASE-R Client -rate [bps]	After Client FEC Termination [bps]	After 400GE AM Removal [bps]	Before 400ZR AM/PAD/OH insert [bps]	Before SC-FEC + MBAS + CRC32 [bps]	Before *[6 x 119b*] pad insert [bps]	Before Hamming [bps]	Before FAW/TS/RES [bps]	Before Pilot Symbol insertion [bps]	400ZR Bit rate [bps]	400ZR Baud rate [bps]	
+100ppm	425 042 500 000	401 602 656 250	401 583 046 745	401 711 674 583	402 497 803 105	429 513 706 231	429 748 627 128	462 250 624 138	463 798 338 281	478 759 575 000	059 844 946 875	+20ppm
Nominal	425 000 000 000	401 562 500 000	401 542 892 456	401 703 640 510	402 489 753 310	429 505 116 129	429 740 032 328	462 241 379 310	463 789 062 500	478 750 000 000	059 843 750 000	Nominal
-100ppm	424 957 500 000	401 522 343 750	401 502 738 167	401 695 606 437	402 481 703 515	429 496 526 027	429 731 437 527	462 232 134 483	463 779 786 719	478 740 425 000	059 842 553 125	-20ppm

Table 14: 400ZR expansion rate table

13 Optical Specifications

The 400ZR optical parameters are organized by Application Code (defined in Table 15) for Tx, Rx, and the Optical Channel (black link).

Ref.	Application Description	Minimum Reach	Application Code - Name
13.0.100	120 km or less, amplified, point-to-point, DWDM noise limited links.	80 km	***0x01*** – 400ZR, DWDM amplified
13.0.110	Unamplified, single wavelength, loss limited links.	11dB loss budget minus link impairments	***0x02*** – 400ZR, Single wavelength, Unamplified

Table 15: 400ZR application codes

Note: All specifications are defined after calibration and compensation, at EOL over temperature and wavelength. All specifications are based on default grid spacing (defined in 13.1.110).

Bold italicized items found in tables indicate a reference to a Coherent Management Interface Spec[1] (CMIS) defined function, state, or status condition.

13.1 400ZR, DWDM amplified - Application Code (0x01):

This section defines the optical parameters for the DWDM amplified application code (**0x01**).

13.1.1 Optical channel specifications – Black Link

Ref.	Parameter	Default	Min	Max	Unit	Conditions/Comments
13.1.100	Channel frequency	193.7	191.3	196.1	THz	
13.1.110	Channel spacing†		100		GHz	See Section 15.1
13.1.111 (optional)			75		GHz	See Section 15.2
13.1.112 (optional)			75		GHz	See Section 15.3
13.1.120	Post FEC BER			10^{-15}		Pre-FEC BER 1.25E-2 or lower.
13.1.130	Fiber type	G.652				Single mode fiber. Specified for link budgeting purposes only.
13.1.140	Target reach		80	-	km	Amplified Link – Noise limited

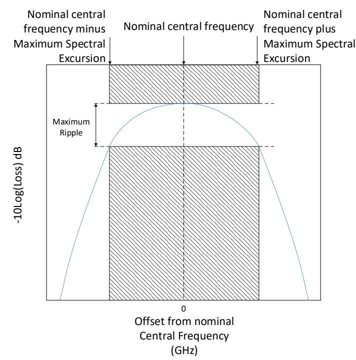
Ref.	Parameter	Default	Min	Max	Unit	Conditions/Comments
13.1.150	Ripple			2.0	dB	 (See definition 13.3.4)
13.1.160	Chromatic Dispersion		0	2400	ps/nm	Frequency dependent change in phase velocity due to fiber.
13.1.161	Optical Return Loss at S_s			24	dB	(See definition 13.3.5)
13.1.162	Discrete Reflectance between S_s and R_s			-27	dB	(See definition 13.3.6)
13.1.170	Maximum Instantaneous Differential Group Delay (DGD)			28	ps	(See definition 13.3.7)
13.1.171	Polarization Dependent Loss (PDL)			2	dB	(See definition 13.3.8)
13.1.172	Polarization Rotation Speed			50	krad/s	(See definition 13.3.9)
13.1.180	Inter-channel Crosstalk at R_s			-8	dB	(See definition 13.3.10) Ref. Clause 9.6 and Fig 9-17 in ITU-T G.sup39.
13.1.181	Interferometric Crosstalk			-35	dB	(See definition 13.3.11)

Table 16: Optical channel specifications

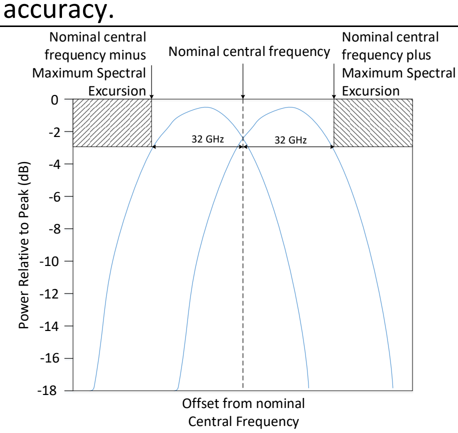
†For channel spacing of 100 GHz on a fiber, the allowed channel frequencies (in THz) are defined by 193.1 + *n* × 0.1 where *n* is a positive or negative integer including 0. For 400ZR modules, *n* = 30 to -17 in steps of 1. The specified 48 × 100GHz DWDM application channels are as defined in Section 15.1.

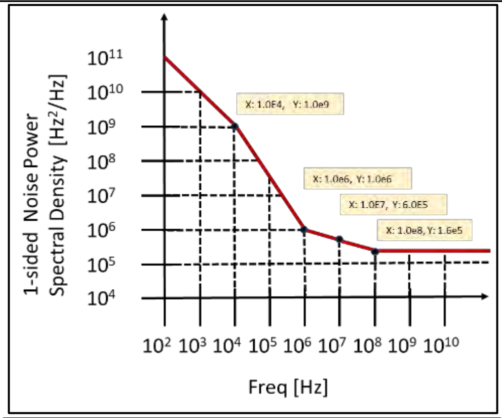
†For channel spacing of 75 GHz or more on a fiber, the allowed channel frequencies (in THz) are defined by 193.1 + 3*n* × 0.025 where *n* is a positive or negative integer including 0. For 400ZR modules, 3*n* = 120 to -69. The reference 64 × 75 GHz DWDM application channels are as defined in Section 15.2.

†For the flexible DWDM grid, the allowed frequency slots have a nominal central frequency (in THz) defined by 193.1 + $n \times 0.00625$ where n is a positive or negative integer including 0 and 0.00625 is the nominal central frequency granularity in THz. Slot width is defined by $12.5 \times m$ where m is a positive integer and 12.5 is the slot width granularity in GHz. Any combination of frequency slots is allowed if no two frequency slots overlap. Example 100 GHz and 75 GHz DWDM applications with offset grid channels are defined in Section 15.3.

13.1.2 Transmitter Optical Specifications

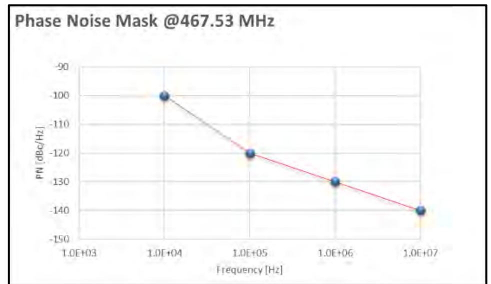
Note: All Tx optical specifications are based on default grid spacing of 100GHz (see 13.1.110). For this grid spacing no Tx shaping is required. If optical shaping is applied on Tx (e.g. for operation at other grid settings) a matched Rx equalizer setting must also be applied on Rx or additional OSNR penalty may be incurred.

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.200	Laser frequency accuracy	-1.8	1.8	GHz	Offset from channel frequency set point. The receiver LO has the same frequency accuracy.
13.1.201	Tx Spectral Excursion		32	GHz	 (See definition 13.3.2) Measured between the nominal central frequency of the channel and the -3.0dB points of the transmitter spectrum furthest from the nominal central frequency measured at point Ss. Includes Laser frequency accuracy (13.1.200) error value from nominal center frequency.

<table>
<tr><th>Ref.</th><th>Parameter</th><th>Min</th><th>Max</th><th>Unit</th><th>Conditions/Comments</th></tr>
<tr><td>13.1.210</td><td>Laser frequency noise</td><td></td><td>See Mask</td><td></td><td>


<table>
<tr><th>Frequency [Hz]</th><th>1- sided Noise power spectral density [Hz²/Hz]</th></tr>
<tr><td>1.0e+02</td><td>1.0e+11</td></tr>
<tr><td>1.0e+04</td><td>1.0e+09</td></tr>
<tr><td>1.0e+06</td><td>1.0e+06</td></tr>
<tr><td>1.0e+07</td><td>6.0e+05</td></tr>
<tr><td>1.0e+08</td><td>1.6e+05</td></tr>
<tr><td>1.0e+09</td><td>1.6e+05</td></tr>
</table>
Mask does not apply to spurs. Measurement Resolution BW shall be between 10^{-1} and 10^{-6} of the frequency of interest.

High frequency component of the phase noise (100MHz and above) is consistent with a 500 kHz laser line width. The receiver LO has the same linewidth.</td></tr>
<tr><td rowspan="2">13.1.212</td><td rowspan="2">Laser RIN</td><td></td><td>-145</td><td rowspan="2">dB/Hz</td><td>0.2GHz $\leq f \leq$ 10GHz Avg</td></tr>
<tr><td></td><td>-140</td><td>0.2GHz $\leq f \leq$ 10GHz Peak</td></tr>
</table>

<table>
<tr><th>Ref.</th><th>Parameter</th><th>Min</th><th>Max</th><th>Unit</th><th>Conditions/Comments</th></tr>
<tr><td>13.2.213a</td><td>Tx clock phase noise (PN): Maximum PN mask for low frequency PN</td><td></td><td>See mask</td><td>dBc/Hz</td><td>


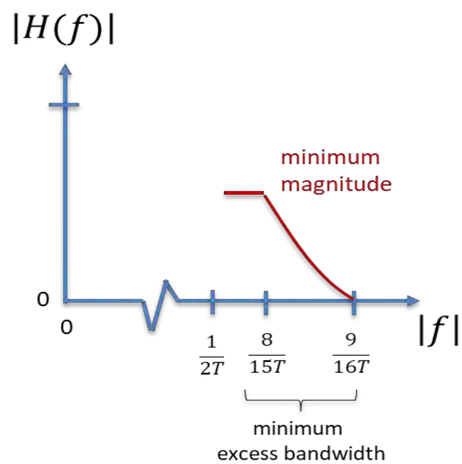
<table>
<tr><th>PN [dBc/Hz]</th><th>Frequency [Hz]</th></tr>
<tr><td>-100</td><td>1.00E+04</td></tr>
<tr><td>-120</td><td>1.00E+05</td></tr>
<tr><td>-130</td><td>1.00E+06</td></tr>
<tr><td>-140</td><td>1.00E+07</td></tr>
</table>
Phase noise, $\mathcal{L}(f)$,

$$f_c = \frac{f_{baud}}{128} = \sim 467.53\ \text{MHz}$$

Mask does not apply to spurs, broadband phase noise only. Spurs are considered separately as per 13.1.213b and 13.1.213c
</td></tr>
</table>

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.213b	Tx clock phase noise (PN); Maximum total integrated RMS phase jitter between 10kHz and 10MHz		600	fs	rms random jitter: $$\sigma_{rj} = \frac{1}{2\pi f_c}\sqrt{2 \cdot \int_{f_1}^{f_2} 10^{\frac{\mathcal{L}(f)}{10}} df}$$ rms periodic jitter (spurs): $$\sigma_{pj,i} = \frac{1}{\sqrt{2}\pi f_c} \cdot 10^{\frac{s_i}{20}}$$ where, $\mathrm{f_1} = 10\mathrm{kHz}$, $\mathrm{f_2} = 10\mathrm{MHz}$, $\mathrm{f_c} = \frac{\mathrm{f_{baud}}}{128} = \sim 467.53\mathrm{MHz}$ $\mathcal{L}(\mathrm{f}) = \text{phase noise (PN)}$ $s_i = \text{individual spur in [dBc]}$ rms total jitter: $$\sigma_{tj} = \sqrt{\sigma_{rj}{}^2 + \sum_{i=1}^{N} \sigma_{pj,i}{}^2}$$ where, $\mathrm{N} = \text{total number of spurs.}$

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.213c	Tx clock phase noise (PN): Maximum total integrated RMS phase jitter between 1MHz and 200MHz		250	fs	rms random jitter: $\sigma_{rj} = \frac{1}{2\pi f_c}\sqrt{2 \cdot \int_{f_1}^{f_2} 10^{\frac{\mathcal{L}(f)}{10}} df}$ rms periodic jitter (spurs): $\sigma_{pj,i} = \frac{1}{\sqrt{2}\pi f_c} \cdot 10^{\frac{s_i}{20}}$ where, $\mathrm{f}_1 = 1\mathrm{MHz}$, $\mathrm{f}_2 = 200\mathrm{MHz}$, $\mathrm{f}_c = \frac{f_{baud}}{128} = 467.53MHz$, $\mathcal{L}(\mathrm{f}) = \text{phase noise (PN)}$, $s_i = \text{individual spur in [dBc]}$ rms total jitter: $\sigma_{tj} = \sqrt{\sigma_{rj}{}^2 + \sum_{i=1}^{N} \sigma_{pj,i}{}^2}$ where, $\mathrm{N} = \text{total number of spurs.}$

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.215	Minimum Excess Bandwidth[1] (See Mask)	12.5		%	The baseband Tx spectral shape in this excess bandwidth shall meet or exceed the following conditions: The magnitude of the spectrum in the frequency range: $\frac{1}{2T} \leq f \leq \frac{9}{16T}$ shall meet $|H(f)| \geq H(0)\sqrt{\frac{1}{2}\left\{1 + \cos\left[8\pi T\left(\left(\frac{8}{15T}\right) - \frac{7}{16T}\right)\right]\right\}},$ $\frac{1}{2T} \leq |f| \leq \frac{8}{15T}$ $|H(f)| \geq H(0)\sqrt{\frac{1}{2}\left\{1 + \cos\left[8\pi T\left(|f| - \frac{7}{16T}\right)\right]\right\}},$ $\frac{8}{15T} \leq |f| \leq \frac{9}{16T}$ where T denotes the symbol period of the signal. 
13.1.220	Allowable output signal power window	-10	-6	dBm	Measured at optical connector.
13.1.221	Total output power with Tx disabled		-20	dBm	*Tx Disable* == false
13.1.222	Total output power during wavelength switching		-20	dBm	Applicable to modules with tunable optics.

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.230	Inband (IB) OSNR	34		dB/0.1nm	Inband OSNR is defined within the bandwidth of the Tx spectral excursion given in (13.1.201) The IB OSNR is referenced to an optical bandwidth of 0.1nm @ 193.7 THz or 12.5 GHz.
13.1.231	Out-of-band (OOB) OSNR	23		dB/0.1nm	Channel total power over peak noise power in the whole frequency range measured with 0.1 nm resolution bandwidth. The OOB OSNR is referenced to an optical bandwidth of 0.1nm @ 193.7 THz or 12.5 GHz.
13.1.240	Transmitter reflectance		-20	dB	Looking into the Tx
13.1.241	Transmitter back reflection tolerance		-24	dB	Light reflected relative to Tx output power back to transmitter while still meeting Tx optical performance requirements.
13.1.250	Transmitter polarization dependent power		1.5	dB	Power difference between X and Y polarization.
13.1.260	X-Y Skew		5	ps	
13.1.270a	DC I-Q offset (mean per polarization)		-26	dB	$P_{excess} = \frac{\mathbf{I}^2_{\mathbf{mean}} + \mathbf{Q}^2_{\mathbf{mean}}}{\mathbf{P}_{\mathbf{Signal}}}$ $IQ_{offset} = \mathbf{10}\,\mathbf{log}_{\mathbf{10}}(\mathbf{P}_{\mathbf{excess}})$
13.1.270b	I-Q instantaneous offset		-20	dB	Same formula definition as 13.1.270a, however, any averaging period shall be ≤ 1us to be consistent with the timescales of Rx DSP operations. Specification applies at any point in time. Allows for modulator bias controls/errors.
13.1.271	Mean I-Q amplitude imbalance		1	dB	
13.1.272	I-Q phase imbalance	-5	+5	degrees	
13.1.273	I-Q Skew		0.75	ps	

Table 17: Tx optical specifications

[1]The minimum excess bandwidth is specified to guarantee multi-vendor clock recovery interoperability. It is required because the Tx spectrum mask is not defined by this IA. For operation on a 75 GHz grid this specification will be modified or removed and replaced by a Tx spectrum mask.

13.1.3 Receiver Optical Specifications

The receiver optical tolerance specifications include margin for Tx and line impairments.

Note: All Rx optical specifications are based on default grid spacing of 100GHz (see 13.1.110). When operating at other grid settings additional compensation may be required or additional penalties may be incurred.

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.300	Frequency offset between received carrier and LO	-3.6	+3.6	GHz	Acquisition Range.
13.1.310	Input power range	-12	0	dBm	Signal power of the channel at the OSNR performance defined in (13.1.330).
13.1.320	Input sensitivity	-12		dBm	Input power needed to achieve post FEC BER per (13.1.120) when OSNR Tolerance > (13.1.330).
13.1.330	OSNR Tolerance		26	dB/0.1nm	At C-FEC threshold (ref. Section 10). See Definition in Section 13.3.2 The OSNR tolerance is referenced to an optical bandwidth of 0.1nm @ 193.7 THz or 12.5 GHz.
13.1.340	Optical return loss	20		dB	Optical reflectance at Rx connector input.
13.1.341	CD Tolerance	2400		ps/nm	Tolerance to Chromatic Dispersion.
13.1.342	Optical path OSNR penalty tolerance		0.5	dB	OSNR penalty tolerance over (13.1.330) due to interferometric crosstalk (13.1.181) and chromatic dispersion (13.1.160).

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.350	PMD tolerance (DGD, SOPMD)	10	-	ps	Tolerance to PMD with $\leq$ 0.5 dB penalty to OSNR sensitivity (13.1.330). when change in SP is $\leq$ 1 rad/ms. 10 ps of average PMD (DGD, SOPMD) corresponds to: • 33 ps of DGDmax when SOPMD = 0 ps^2. • 272 ps^2 of SOPMD when DGD = 23.3 ps. Due to the statistical nature of PMD the DGDmax to DGDmean Ratio is calculated at 3.3 (4.1 x 10^{-6} probability that DGDmean being greater than DGDmax).
13.1.351	Peak PDL tolerance	3.5	-	dB	Tolerance to peak PDL with $\leq$ 1.3 dB penalty to OSNR sensitivity (13.1.330) when change in SOP is < =1 rad/ms. Test configuration - PDL emulator applied before noise loading.
13.1.352	Tolerance to change in SOP	50	-	krad/s	Tolerance to change in SOP with $\leq$0.5 dB additional OSNR penalty over all PMD and PDL values defined in (13.1.350) and (13.1.351).
13.1.353	Optical input power transient tolerance	+/-2	-	dB	Tolerance to change in input power with $\leq$ 0.5 dB penalty to OSNR sensitivity (13.1.330). When transient received power is within range defined by input power range (13.1.310). Rise/fall times of power change defined by 20-80% of 50 us or slower.

Table 18: Rx optical specifications

[1]*Italicized* items indicate a reference to a Coherent Management Interface Spec [1] (CMIS) defined function, state, or status condition.

13.1.4 Module Requirements Tx - (Informative)

The following specifications provide guidance for modules based on the 400ZR IA.

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.1.400	Transmitter laser disable time		100	ms	The maximum transmitter turn-off time from any condition that results in *Tx_Disable==true* to reach the Tx output power given by (13.1.221). Rx shall remain locked and thus LO must remain enabled.
13.1.410	Transmitter turn-up time from warm start		180	s	The maximum time from *ModuleLowPwr* to *DataPathActivated* state.
13.1.411	Transmitter turn-up time from cold start		200	s	The maximum time from de-assertion of *ResetS* == false to *DataPathActivated* state while LoPwrS == false.
13.1.420	Transmitter wavelength switching time		180	s	The maximum time to change wavelengths including turn-up time. Applicable to modules with tunable optics.
13.1.430	Output power monitor - Accuracy	-2.0	2.0	dB	Total output power measurement including all ASE contribution. Measurement accuracy does not contribute to allowable output power signal window.

Table 19: 400ZR module – Tx specifications

13.1.5 Module Requirements Rx - (Informative)

The following specifications provide guidance for modules based on the 400ZR IA.

Ref.	Parameter	Default	Min	Max	Unit	Conditions/Comments
13.1.510	Receiver turn-up time from warm start			10	s	Upon ***Rx_LOS*** de-assert, Receiver has been turned up previously.
13.1.511	Receiver turn-up time from cold start			200	s	From module reset, with valid optical input signal present.
13.1.530	Input total power monitor - Accuracy		-4.0	4.0	dB	Over the superset of input power range (13.1.310), receiver sensitivity 13.1.320) and the optical ***Rx_LOS*** Assert threshold range (13.1.532 assuming Min accuracy – i.e. Real input total power range of 0dBm to -14dBm at the default Optical ***Rx_LOS*** Assert Threshold.
13.1.531	Input Channel power monitor - Accuracy		-4.0	4.0	dB	The module reports the channel power as received by the module.
13.1.532	Optical ***Rx_LOS*** Assert Threshold†	-18	-20	-16	dBm	Channel Power.
13.1.533	Optical ***Rx_LOS*** Hysteresis		1.0	2.5	dBm	***Rx_LOS*** cleared.

Table 20: 400ZR module – Rx specifications

† If a module supports both amplified and unamplified use cases, Optical ***Rx_LOS*** thresholds must be programmable to support different ranges for each application.

13.2 400ZR, Single wavelength, Unamplified - Application Code (0x02):

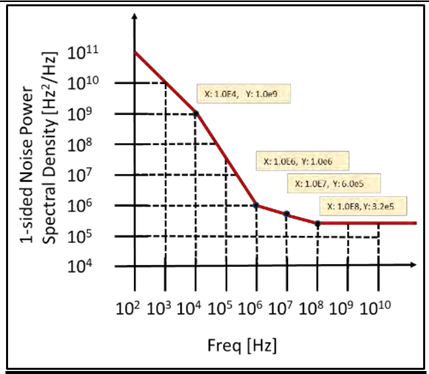
This section defines the optical parameters for application code ***0x02***.

13.2.1 Optical channel specifications

Ref.	Parameter	Default	Min	Max	Unit	Conditions/Comments
13.2.100	Channel frequency	193.7			THz	
13.2.120	Post FEC BER			10^{-15}		Pre-FEC BER 1.25E-2 or lower.
13.2.130	Fiber type	G.652				Single mode fiber.
13.2.160	Chromatic Dispersion		0	1200	ps/nm	Frequency dependent change in phase velocity due to fiber
13.2.161	Optical Return Loss at S_s			24	dB	(See definition 13.3.5)
13.2.162	Discrete Reflectance between S_s and R_s			-27	dB	(See definition 13.3.6)
13.2.170	Maximum Instantaneous Differential Group Delay (DGD)			16	ps	(See definition 13.3.7)
13.2.172	Polarization Rotation Speed			50	krad/s	(See definition 13.3.9)

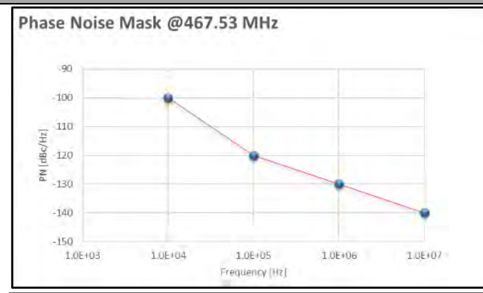
Table 21: Optical channel specifications

13.2.2 Transmitter Optical Specifications

<table>
<tr><th>Ref.</th><th>Parameter</th><th>Min</th><th>Max</th><th>Unit</th><th>Conditions/Comments</th></tr>
<tr><td>13.2.200</td><td>Laser frequency accuracy</td><td>-1.8</td><td>1.8</td><td>GHz</td><td>Offset from channel frequency set point. The receiver LO has the same frequency accuracy</td></tr>
<tr><td>13.2.210</td><td>Laser frequency noise</td><td></td><td>See Mask</td><td></td><td>

<table>
<tr><th>Frequency [Hz]</th><th>Frequency Noise [Hz2/Hz]</th></tr>
<tr><td>1.0e+02</td><td>1.0e+11</td></tr>
<tr><td>1.0e+04</td><td>1.0e+09</td></tr>
<tr><td>1.0e+06</td><td>1.0e+06</td></tr>
<tr><td>1.0e+07</td><td>6.0e+05</td></tr>
<tr><td>1.0e+08</td><td>3.2e+05</td></tr>
<tr><td>1.0e+09</td><td>3.2e+05</td></tr>
</table>
Mask does not apply to spurs. Measurement Resolution BW shall be between 10^{-1} and 10^{-6} of the frequency of interest.

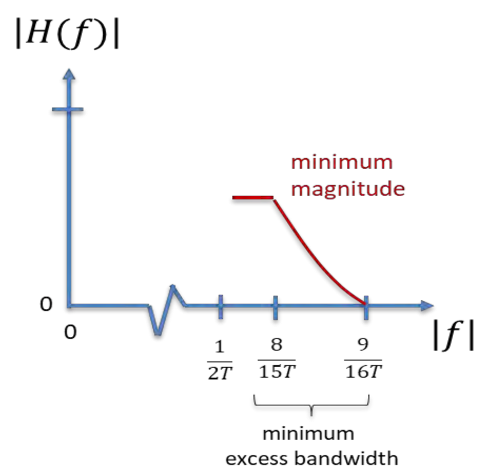
High frequency component of the phase noise (100MHz and above) is consistent with a 1 MHz laser line width. The receiver LO has the same linewidth.</td></tr>
<tr><td rowspan="2">13.2.212</td><td rowspan="2">Laser RIN</td><td></td><td>-145</td><td rowspan="2">dBc/Hz</td><td>0.2GHz $\leq f \leq$ 10GHz - Avg</td></tr>
<tr><td></td><td>-140</td><td>0.2GHz $\leq f \leq$ 10GHz - Peak</td></tr>
</table>

<table>
<tr><th>Ref.</th><th>Parameter</th><th>Min</th><th>Max</th><th>Unit</th><th>Conditions/Comments</th></tr>
<tr><td>13.2.213a</td><td>Tx clock phase noise (PN): Maximum PN mask for low frequency PN</td><td></td><td>See mask</td><td>dBc/Hz</td><td>


<table>
<tr><th>PN [dBc/Hz]</th><th>Frequency [Hz]</th></tr>
<tr><td>-100</td><td>1.00E+04</td></tr>
<tr><td>-120</td><td>1.00E+05</td></tr>
<tr><td>-130</td><td>1.00E+06</td></tr>
<tr><td>-140</td><td>1.00E+07</td></tr>
</table>
Phase noise, $\mathcal{L}(f)$,
$$f_c = \frac{f_{baud}}{128} = \sim 467.53\ \text{MHz}$$
Mask does not apply to spurs, broadband phase noise only. Spurs are considered separately as per 13.2.213b and 13.2.213c</td></tr>
</table>

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.2.213b	Tx clock phase noise (PN); Maximum total integrated RMS phase jitter between 10kHz and 10MHz		600	fs	rms random jitter: $\sigma_{rj} = \frac{1}{2\pi f_c}\sqrt{2 \cdot \int_{f_1}^{f_2} 10^{\frac{\mathcal{L}(f)}{10}} df}$ rms periodic jitter (spurs): $\sigma_{pj,i} = \frac{1}{\sqrt{2}\pi f_c} \cdot 10^{\frac{s_i}{20}}$ where, $\mathrm{f_1} = 10\mathrm{kHz}$, $\mathrm{f_2} = 10\mathrm{MHz}$, $\mathrm{f_c} = \frac{\mathrm{f_{baud}}}{128} = \sim 467.53\mathrm{MHz}$ $\mathcal{L}(\mathrm{f}) = \text{phase noise (PN)}$ $s_i = \text{individual spur in [dBc]}$ rms total jitter: $\sigma_{tj} = \sqrt{{\sigma_{rj}}^2 + \sum_{i=1}^{N} {\sigma_{pj,i}}^2}$ where, $\mathrm{N} = \text{total number of spurs.}$

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.2.213c	Tx clock phase noise (PN): Maximum total integrated RMS phase jitter between 1MHz and 200MHz		250	fs	rms random jitter: $\sigma_{rj} = \frac{1}{2\pi f_c}\sqrt{2 \cdot \int_{f_1}^{f_2} 10^{\frac{\mathcal{L}(f)}{10}} df}$ rms periodic jitter (spurs): $\sigma_{pj,i} = \frac{1}{\sqrt{2}\pi f_c} \cdot 10^{\frac{s_i}{20}}$ where, $\mathrm{f_1} = 1\mathrm{MHz},$ $\mathrm{f_2} = 200\mathrm{MHz},$ $\mathrm{f_c} = \frac{f_{baud}}{128} = 467.53MHz,$ $\mathcal{L}(\mathrm{f}) = \text{phase noise (PN)},$ $s_i = \text{individual spur in [dBc]}$ rms total jitter: $\sigma_{tj} = \sqrt{{\sigma_{rj}}^2 + \sum_{i=1}^{N} {\sigma_{pj,i}}^2}$ where, $\mathrm{N} = \text{total number of spurs.}$

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.2.215	Minimum Excess Bandwidth[1] (See Mask)	12.5		%	The baseband Tx spectral shape in this excess bandwidth shall meet or exceed the following conditions: The magnitude of the spectrum in the frequency range: $\frac{1}{2T} \le f \le \frac{9}{16T}$ shall meet $|H(f)| \ge H(0)\sqrt{\frac{1}{2}\left\{1+\cos\left[8\pi T\left(\left(\frac{8}{15T}\right)-\frac{7}{16T}\right)\right]\right\}},$ $\frac{1}{2T} \le |f| \le \frac{8}{15T}$ $|H(f)| \ge H(0)\sqrt{\frac{1}{2}\left\{1+\cos\left[8\pi T\left(|f|-\frac{7}{16T}\right)\right]\right\}},$ $\frac{8}{15T} \le |f| \le \frac{9}{16T}$ where T denotes the symbol period of the signal. 
13.2.220	Allowable output signal power window	-9	0	dBm	Measured at optical connector.
13.2.221	Total output power with Tx disabled		-20	dBm	*Tx Disable* == false
13.2.230	Inband (IB) OSNR	34		dB/0.1nm	The 0.1nm bandwidth for the IB OSNR refers to 193.7 THz or 12.5 GHz optical bandwidth.
13.2.240	Transmitter reflectance		-20	dB	Looking into the Tx

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.2.241	Transmitter back reflection tolerance		-24	dB	Light reflected relative to Tx output power to transmitter while still meeting Tx optical performance requirements.
13.2.250	Transmitter polarization dependent power		1.5	dB	Power difference between X and Y polarization.
13.2.260	X-Y Skew		5	ps	
13.2.270a	DC I-Q offset (mean per polarization)		-26	dB	$P_{excess} = \frac{\mathbf{I}^2_{\mathbf{mean}} + \mathbf{Q}^2_{\mathbf{mean}}}{\mathbf{P}_{\mathbf{Signal}}}$ $IQ_{offset} = \mathbf{10}\log_{\mathbf{10}}(\mathbf{P}_{\mathbf{excess}})$
13.2.270b	I-Q instantaneous offset		-20	dB	Same formula definition as 13.2.270a, however, any averaging period shall be < 1us to be consistent with the timescales of Rx DSP operations. Specification applies at any point in time. Allows for modulator bias controls/errors.
13.2.271	I-Q amplitude imbalance		1	dB	
13.2.272	I-Q phase imbalance	-5	+5	degrees	
13.2.273	I-Q Skew		0.75	ps	

Table 22: Tx Optical specifications

[1]The minimum excess bandwidth is specified to guarantee multi-vendor clock recovery interoperability. It is required because the Tx spectrum mask is not defined by this IA.

13.2.3 Receiver Optical Specifications

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.2.300	Frequency offset between received carrier and LO	-3.6	+3.6	GHz	Acquisition Range.
13.2.310	Input power range	-20	0	dBm	Signal power of the channel.
13.2.320	Input sensitivity	-20		dBm	Input power needed to achieve post FEC BER per (13.2.120) when Inband (IB) OSNR ≥ (13.2.230).
13.2.340	Optical return loss	20		dB	Optical reflectance at connector input.
13.2.341	CD Tolerance	1200		ps/nm	Tolerance to Chromatic Dispersion.
13.2.342	Optical path power penalty		0.5	dB	Rx Sensitivity penalty over (13.2.320) due to reflections and the combined effects of dispersion (13.2.341).
13.2.350	Average PMD (DGD, SOPMD) tolerance	7	-	ps	Tolerance to PMD with ≤ 0.5dB Rx sensitivity penalty (13.2.320) when change in SOP is ≤= 1 rad/ms. 7 ps of average PMD (DGD, SOPMD) corresponds to: • 23 ps of DGDmax when SOPMD = 0 ps^2. • 132 ps^2 of SOPMD when DGD = 16.3 ps. Due to the statistical nature of PMD the DGDmax to DGDmean Ratio is calculated at 3.3 (4.1×10^{-6} probability that DGDmean being greater than DGDmax).
13.2.351	Peak PDL tolerance	1.5	-	dB	Tolerance to change in peak PDL with ≤ 0.4dB Rx sensitivity penalty (13.2.320) when change in SOP is <= 1 rad/ms.
13.2.352	Tolerance to change in SOP	50	-	krad/s	Tolerance to change in SOP with ≤0.3 dB additional power penalty over all PMD and PDL values defined in (13.2.350) and (13.2.351).

Table 23: Rx Optical specifications

13.2.4 Module Requirements Tx - (Informative)

The following specifications provide guidance for modules based on the 400ZR IA.

Ref.	Parameter	Min	Max	Unit	Conditions/Comments
13.2.400	Transmitter laser disable time		100	ms	The maximum transmitter turn-off time from any condition that results in *Tx_Disable==true* to reach the Tx output power given by (13.2.221). Rx shall remain locked and thus LO must remain enabled.
13.2.410	Transmitter turn-up time from warm start		180	s	The maximum time from *ModuleLowPwr* to *DataPathActivated* state.
13.2.411	Transmitter turn-up time from cold start		200	s	The maximum time from de-assertion of *ResetS* == false to *DataPathActivated* state while LoPwrS == false.
13.2.430	Output power monitor - Accuracy	-2.0	2.0	dB	Total output power measurement including all ASE contribution. Measurement accuracy does not contribute to allowable output power signal window.

Table 24: 400ZR module – Tx specifications

13.2.5 Module Requirements Rx - (Informative)

The following specifications provide guidance for modules based on the 400ZR IA.

Ref.	Parameter	Default	Min	Max	Unit	Conditions/Comments
13.2.510	Receiver turn-up time from warm start			10	s	Upon ***Rx_LOS*** de-assert, Receiver has been turned up previously.
13.2.511	Receiver turn-up time from cold start			200	s	From module reset, with valid optical input signal present.
13.2.531	Input Channel or Total power monitor - Accuracy		-4.0	4.0	dB	Over the superset of input power range (13.2.310), receiver sensitivity (13.2.320), and the optical ***Rx_LOS*** Assert threshold range (13.2.532) assuming Min accuracy (i.e. real input total power range of 0dbm to -22dBm at the default Optical ***Rx_LOS*** Assert Threshold).
13.2.532	Optical ***Rx_LOS*** Assert Threshold†	-26	-28	-24	dBm	Channel or Total Input Power.
13.2.533	Optical ***Rx_LOS*** Hysteresis		1.0	2.5	dBm	***Rx_LOS*** cleared.

Table 25: 400ZR module – Rx specifications

† If a module supports both amplified and unamplified use cases, Optical ***Rx_LOS*** thresholds must be programmable to support different ranges for each application.

13.3 Optical Parameter Definitions

13.3.1 The Receiver Optical Signal-to-noise Ratio Tolerance

The receiver OSNR tolerance is defined as the minimum value of OSNR (referred to 0.1 nm @193.7 THz or 12.5 GHz) that can be tolerated while maintaining the maximum BER of the application. This must be met for all powers between the maximum and minimum mean input power with a transmitter with worst-case values of:

- Transmitter optical return loss,
- Receiver connector degradations
- Measurement tolerances

The receiver OSNR tolerance does not have to be met in the presence of chromatic dispersion, non-linear effects, reflections from the optical path, PMD, and PDL or optical crosstalk. These effects are specified separately but contribute to total optical path OSNR penalty.

System integrators need to account for these path penalties when evaluating network performance.

13.3.2 Spectral excursion

Spectral excursion is defined as the difference between the nominal central frequency of the channel and the -3.0 dB points of the transmitter spectrum furthest from the nominal central frequency measured at point S_s.

13.3.3 Out-of-Band OSNR (OOB OSNR)

Out-of-Band OSNR (OOB OSNR) is the ratio of the peak transmitter power to the integrated power outside the transmitter spectral excursion. The spectral resolution of the measurement shall be better than the maximum spectral width of the peak.

13.3.4 Ripple

Ripple is defined as the peak-to-peak difference in insertion loss between the input and output ports of the black link over that channel in the frequency (or wavelength) range of the channel +/- the maximum spectral excursion.

13.3.5 Optical return loss at S_S

Reflections are caused by refractive index discontinuities along the optical path. If not controlled, they can degrade system performance through their disturbing effect on the operation of the optical source, or through multiple reflections which lead to interferometric noise at the receiver. Reflections from the optical path are controlled by specifying the:

- minimum optical return loss of the cable plant at the source reference point (S_S), including any connectors; and
- maximum discrete reflectance between source reference point (S_S) and receive reference point (R_S)

Reflectance denotes the reflection from any single discrete reflection point, whereas the optical return loss is the ratio of the incident optical power to the total returned optical power from the entire fiber including both discrete reflections and distributed backscattering such as Rayleigh scattering.

13.3.6 Discrete reflectance between S_S and R_S

Optical reflectance is defined to be the ratio of the reflected optical power present at a point, to the optical power incident to that point. The maximum number of connectors or other discrete reflection points which may be included in the optical path must be such as to allow the specified overall optical return loss to be achieved.

13.3.7 Differential Group Delay (DGD)

Differential group delay (DGD) is the time difference between the fractions of an optical signal transmitted in the two principal states of polarization. For distances greater than several kilometers, and assuming random (strong) polarization mode coupling, DGD in a fiber can be statistically modelled as having a Maxwellian distribution.

Due to the statistical nature of polarization mode dispersion (PMD), the relationship between maximum instantaneous DGD and mean DGD can only be defined probabilistically. The probability of the instantaneous DGD exceeding any given value can be inferred from its Maxwellian statistics.

For purposes of this IA the ratio of maximum instantaneous DGD to mean DGD is defined as 3.3, corresponding to the probability of exceeding the maximum DGD 4.1×10^{-6}.

13.3.8 Polarization Dependent Loss (PDL)

The polarization dependent loss (PDL) is the difference (in dB) between the maximum and minimum values of the channel insertion loss (or gain) of the black link from point S_s to R_s due to a variation of the State Of Polarization (SOP) over all state of polarizations.

13.3.9 Polarization rotation speed

The polarization rotation speed is the rate of rotation in Stokes space of the two polarizations of the optical signal at point R_s measured in krad/s.

13.3.10 Inter-channel crosstalk

Inter-channel crosstalk is defined as the ratio of total power in all the disturbing channels to that in the wanted channel, where the wanted and disturbing channels are at different wavelengths.

Specifically, the isolation of the link shall be greater than the amount required to ensure that when any channel is operating at the minimum mean output power at point S_s and all of the others are at the maximum mean output power, then the inter-channel crosstalk at the corresponding point R_s is less than the maximum inter-channel crosstalk value.

13.3.11 Interferometric crosstalk

Interferometric crosstalk is defined as the ratio of the disturbing power to the wanted power within a single channel, where the disturbing power is the power (not including ASE) within the optical channel that would remain if the wanted signal were removed from the link while leaving all of the other link conditions the same.

Specifically, the isolation of the link shall be greater than the amount required to ensure that when any channel is operating at the minimum mean output power at point S_s and all of the others are at the maximum mean output power, then the interferometric crosstalk at the corresponding point R_s is less than the maximum interferometric crosstalk value.

14 Interoperability Test Methodology, Definitions

Interoperability is achievable by complying with all required aspects of this IA. Digital datapath verification is measured through a combination of interoperability Test Vectors and the use of common sets of test generators and checkers. The generators and checkers can be configure using looped back pairs for self-testing or in a cross-linked configuration.

Optical interworking is achieved through strict adherence to the discrete Tx/Rx optical specifications over a compliant channel (ref Section 13). Error Vector Magnitude Testing (Section 20, Appendix C) is intended for future integration to the normative sections of this IA.

14.1 400ZR Test Features

To verify the design for interoperability, a full set of test vectors is made available to OIF member companies. Lower level diagnostic capabilities in the form of loopbacks and insertion points for test generators/checkers is also described in Section 14.2.

14.2 Loopback features, Test Generators and Checkers

Figure 39 shows the various diagnostic and test capabilities overlaid on the data path. Generators and checkers are provided and can be used in conjunction with the loopbacks for self-diagnostic, or they can be used in conjunction with external test equipment to verify the data path.

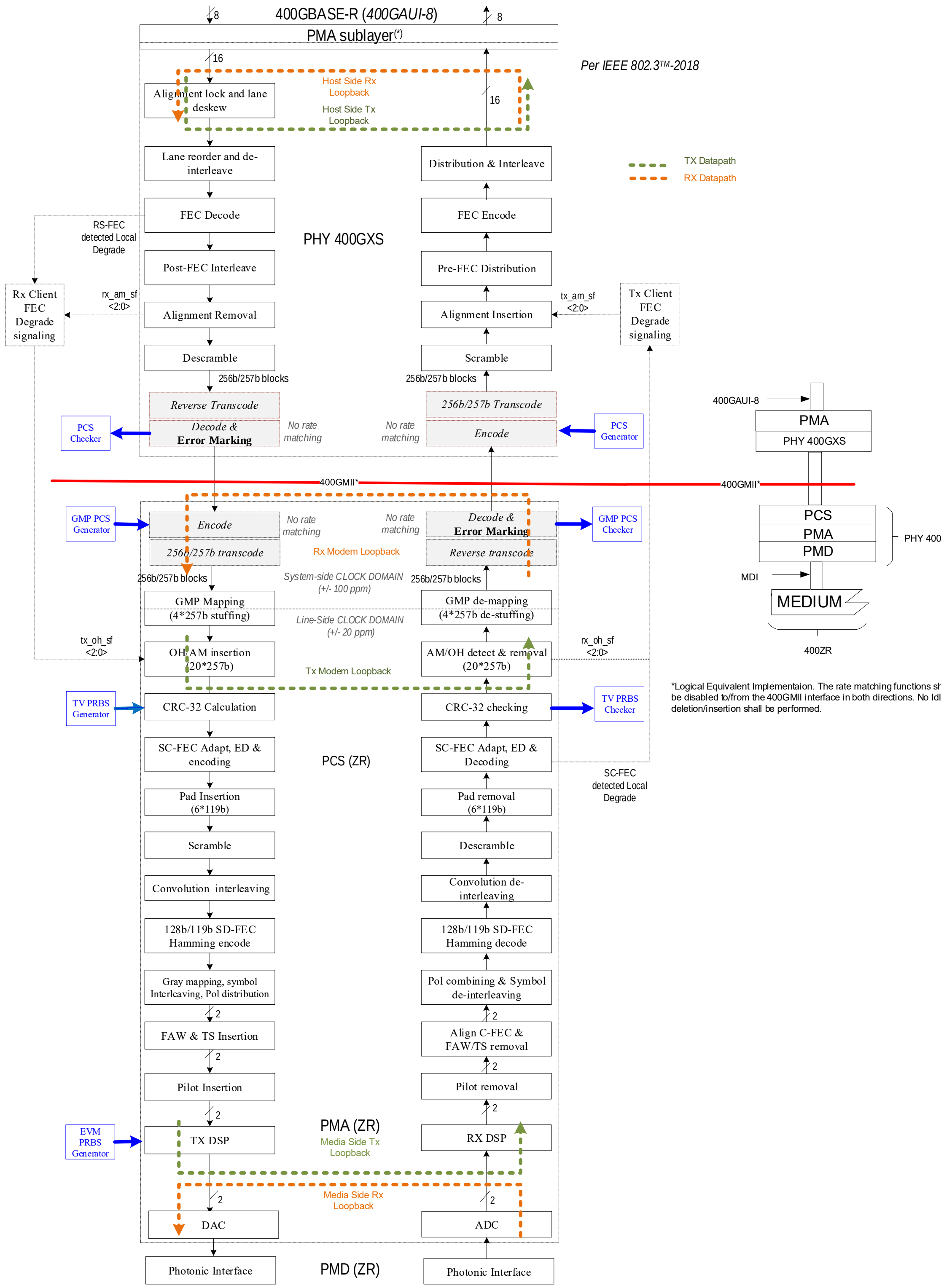


Figure 39: 400ZR test features

14.2.1 Loopbacks

A 400ZR module must be capable to minimally support one of the following loopback sets. The sets are defined such that when two 400ZR modules are cross-connected over a black link a near-end and a far-end loopback path exists across the black link. The CMIS supported loopback modes are shown in ***Italic***. Each set has 1 Rx path and 1 Tx path.

- Modem Tx loopback + Modem Rx Loopback
- Modem Tx loopback + ***Host Side Rx Loopback***
- ***Media Side Tx loopback*** + Modem Rx Loopback
- ***Host Side Tx loopback*** + ***Host Side Rx Loopback***

The specific loopback mode enabled must be coordinated at each end of the link by each host.

The following loopback modes are defined:

Loopback Name	Description
Host Side Tx Loopback	Loopback after Alignment lock and lane De-skew → PMA sublayer. Host loop timed.
Modem Tx Loopback	Loopback after GMP mapping → GMP De-mapping. Data re-transmitted relative to local clock
Media Side Tx Loopback	Loopback after Tx DSP processing blocks and before Rx DSP processing blocks
Media Side Rx Loopback	Loopback in DSP. After polarity split and symbol de-interleave → Grey mapper, symbol Interleave. Media loop timed.
Modem Rx Loopback	Loopback after GMP De-mapping → GMP mapping. Data retransmitted relative to local clock.
Host Side Rx Loopback	Loopback after distribution/interleaving block on host ingress path, and before lane reorder and interleave

Table 26: Loopbacks

14.2.2 Test Generators/Checkers

The test generators and checker requirements are described below: Required modes are highlighted with **Bold** text.

Generator/Checker Type	Description
EVM PRBS	Tx Generator only - Used for EVM • PRBS-7 - Optional • PRBS-11 - Optional • PRBS-15 - Optional • PRBS-23 - Optional • PRBS-31 - Optional
TV PRBS	Tx Generator, Rx Checker, ZR Frame replacement to/from SC-FEC, Used for Test Vectors, and FEC characterization. • PRBS-7 - Optional • PRBS-11 - Optional • PRBS-15 - Optional • PRBS-23 - Optional • **PRBS-31 - Required**
GMP PCS	Tx Generator, Rx Checker. PCS Test pattern. Data retransmitted relative to local clock.
PCS	Rx Generator, Tx Checker. PCS Test pattern: IEEE Std 802.3™-2018 Clause 119.2.4.9 idle control blocks (block type 0x1E)

Table 27: Test generator/checker descriptions

14.3 Interoperability Test Vectors

The Interoperability generators/checkers are primarily used during design development (e.g. simulation). Test vectors are used to guarantee the design integrity and the datapath interoperability.

14.3.1 EVM PRBS

The EVM PRBS is intended for EVM measurements. The EVM PRBS will overwrite all transmit symbols. No specific algorithm, synchronization or seed is required.

14.3.2 TV PRBS

The TV PRBS is used for validating C-FEC/DSP framing, symbol mapping, and FAW/TS/PS insertion. The required PRBS31 is per IEEE 802.3 with initial state being all 1's.

- Generation/checking is to/from the media interface (see Figure 39).
- The PRBS test vector generator is inserted in the Tx data path after the GMP mapper. Test vector generation data is a PRBS31 sequence replacing the entire 400ZR frame.
- The TV PRBS test vector checker is inserted in the Rx data path before the GMP de-mapper. The TV PRBS checker shall recover and verify the PRBS31 sequence.
- The TV PRBS test vector generator can be looped back to the TV PRBS test vector checker as a self-test.

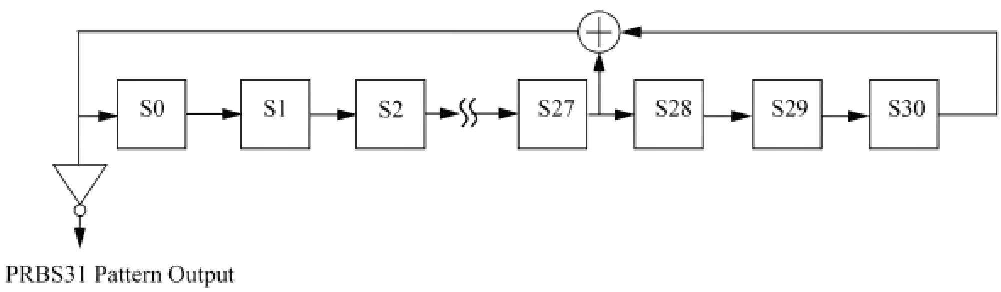


Figure 40: Test vector PRBS31 generator

The TV PRBS test vector files are attached in Table 28.

Order	Polynomial	Seed value	Test Vector File
31	$Z^{31}+Z^{28}+1$	No seed value required.	testVector.txt

Table 28: Test vector PRBS files

14.3.3 GMP PCS test vectors

The GMP PCS Test Vectors are used for validating the PCS (ZR) datapath. This includes the GMP mapping process, C-FEC generation and DSP framing. The GMP PCS generator inserts a continuous stream of Idle control characters /I/ per IEEE Std 802.3™-2018 Clause 119.2.3.5 prior to GMP mapping on the Tx datapath. The checker is after the GMP de-mapper on the Rx datapath. See Figure 39.

GMP PCS Test vectors should be longer than 26 super frames. The test vector attached in this document have a length of 52 super frames. However, 52 super frames may not be enough length to find GMP stuffing event. The vector of 256 400ZR frames (as input of C-FEC) is also included.

C_m OH value may be mismatched due to C_m fluctuation (between 10215 min. and 10216 max.) depending on the ppm offset and the initialization process of the C_m calculation.

Reserved symbols in the super frame are set to (0,0) for the test vectors. Although these symbols are permitted for the proprietary usage, these symbols must be mapped with the following considerations:

- Randomized,
- DC Balanced,
- Low cross correlation on the symbol stream of TS, FAW and RES

The GMP PCS test vector files are attached in Table 29.

Description	Test Vector File
Readme	Readme.txt
Idle test pattern into 400ZR frame	400ZR_PCS_test_FlexO_out.txt
Test Pattern into DSP	400ZR_PCS_test_symbol_out.txt

Table 29: GMP PCS test vector files

14.3.1 PCS test vectors

Generation/checking is to/from host interface (see Figure 39).

The PCS test vector generator is inserted in the Rx data path after the GMP de-mapper. The test pattern is based on IEEE Std 802.3™-2018 Clause 119.2.4.9 (Idle Insert). Downstream logic in the 400ZR data path shall support transcoding, scrambling, PCS alignment marker insertion and RS(544,514) FEC encapsulation. The host loop Rx data path vector check monitor point is at the 400GBASE-R PMA sublayer.

The PCS test vector checker is inserted in the Tx data path before the GMP mapper. The test pattern used within the 400GBASE-R PCS sublayer is IEEE Std 802.3™-2018 Clause 119.2.4.9 idle control blocks (block type 0x1E). Downstream logic in the 400ZR data path shall support RS(544,514) FEC termination, PCS de-skew, descrambling. The host loop Tx data path vector check monitor is pre GMP mapping. The expected string is per IEEE Std 802.3™-2018 Clause 119.2.3.5 (Idle Insert).

Once the host loop Rx and Tx data path are confirmed the PCS test vector generator can be looped back to the PCS test vector checker as a self-test.

14.3.1 Media loop testing

Test vector generation/checking shall be run on the complete data path bypassing the on-board test vector generators/checkers to verify end-to-end interoperability. Test vector generation/checking in this case is done at both the media and host interfaces.

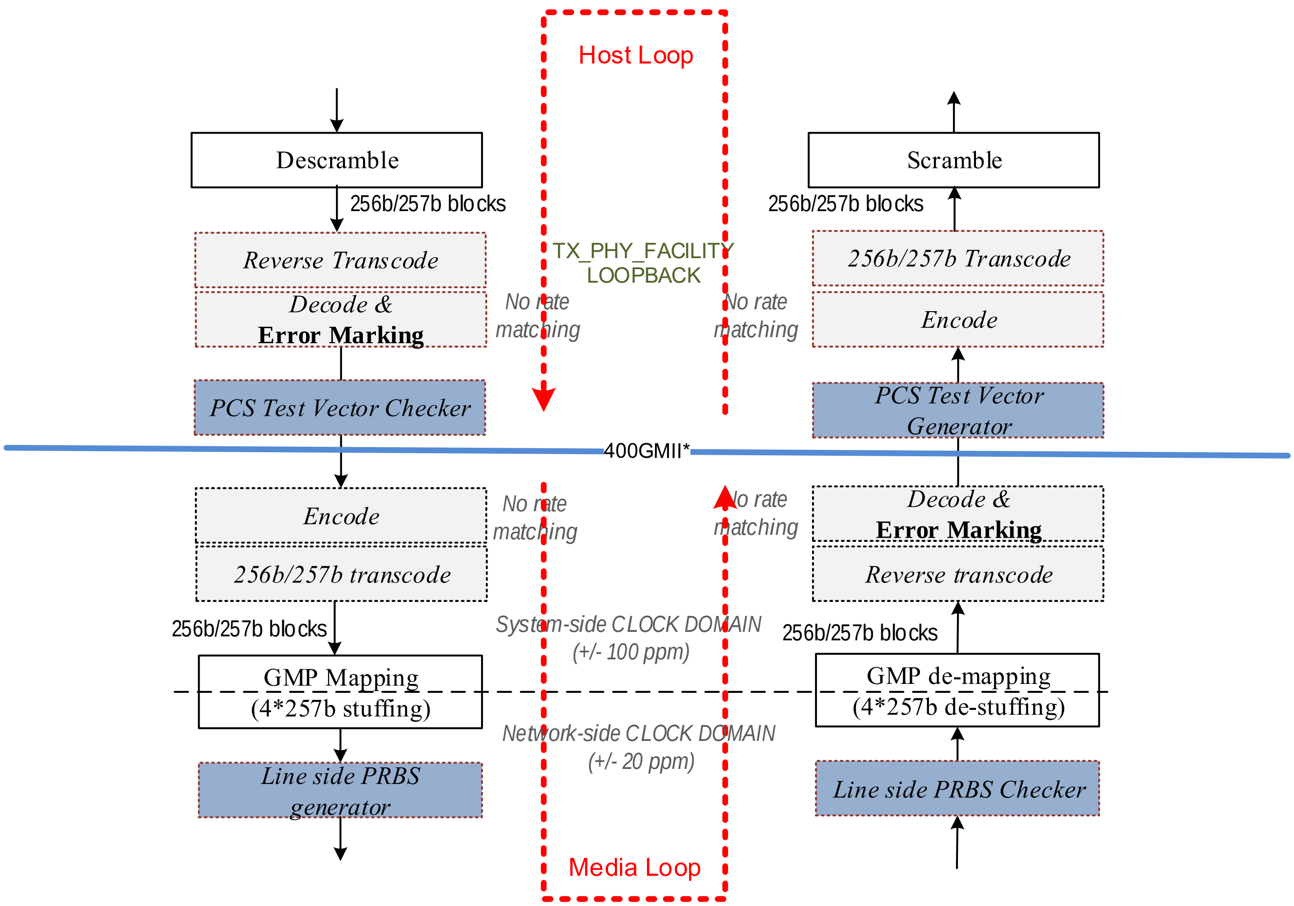


Figure 41: Test vector detail

15 Operating frequency channel definitions

15.1 Normative 48 x 100 GHz DWDM Application Channels.

Application Code (***0x1)*** requires 400ZR modules at the 48 frequencies provided in Table 30. The Channel spacing in Table 30 is based on ITU-T G.694.1 Section 6 “Fixed grid nominal central frequencies for dense WDM systems”.

index	*n* (from ITU-T G.694.1)	freq. [THz]
1	30	196.100
2	29	196.000
3	28	195.900
…	…	…
46	-15	191.600
47	-16	191.500
48	-17	191.400

Table 30: 100GHz channel spacing

15.2 Optional 64 x 75 GHz DWDM Application Channels

The preferred optional Application Code (***0x1)*** 75 GHz Channel spacing in Table 31 is based on ITU-T G.694.1 Section 6 “Fixed grid nominal central frequencies for Dense WDM systems.”

index	*n* (from ITU-T G.694.1)	freq. [THz]
1	120	196.100
2	117	196.025
3	114	195.950
…	…	…
62	-63	191.525
63	-66	191.450
64	-69	191.375

Table 31: 75GHz channel spacing

15.3 Optional Flexible DWDM Grid

Flexible DWDM grids are defined in ITU-T G.694.1 Section 7 "Flexible DWDM grid definition", where center frequencies are determined by,

$$(193.1 + n \times 0.00625) \text{ THz}$$

and each channel occupies a slot width,

$$12.5 \text{ GHz} \times m$$

Such that adjacent channel's frequency slots differ in n by,

$$\Delta n = 2 \text{ x } m$$

There are two example grids in Section 15.3.1 and 15.3.2 that allow the maximum channel fill with 100 GHz and 75 GHz spaced channels on a previously defined spectrum of 96 50 GHz spaced channels. This allows the re-use of previously designed and deployed DWDM hardware such as WSS and amplifier components without wasting spectrum.

The offset in the grids in Table 32 and Table 33 relative to Table 30 and Table 31 allow for channel plans (e.g. 48 channels spaced at 100 GHz or 64 Channels spaced at 75 GHz), which are edge-aligned to the band of 96 channels spaced at 50 GHz where the center frequencies are not offset.

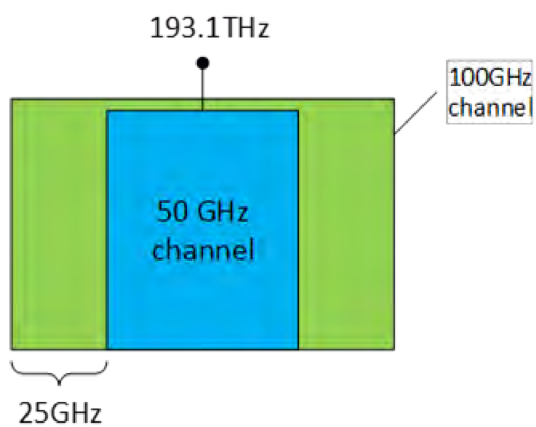


Figure 42: Flexible grid provisioning example

15.3.1 Example 100GHz Flexible Grid Offset

This 48-channel grid has 100 GHz frequency slots corresponding to *m* = 8. The grid is offset by 25 GHz from the normative fixed 100 GHz grid defined in Section 15.1. The following table shows the values of *n* in steps of Δ*n* = 16, and an offset at 193.1 THz of *n* = -4 which corresponds to -25 GHz.

n (from ITU-T G.694.1 Sect. 7)	center freq. [THz]
476	196.075
460	195.975
444	195.875
…	…
12	193.175
-4	193.075
-20	193.975

Table 32: Example 100GHz flexible grid

15.3.2 Example 75GHz Flexible Grid Offset

This 64-channel grid has 75 GHz frequency slots corresponding to *m* = 6. The grid is offset by 12.5 GHz from fixed 75 GHz grid defined in Section 15.2. The following table shows the values of *n* in steps of Δ*n* = 12, and an offset at 193.1 THz of *n* = -2 which corresponds to -12.5 GHz.

n (from ITU-T G.694.1 Sect. 7)	center freq. [THz]
478	196.0875
466	196.0125
454	195.9375
…	…
10	193.1625
-2	193.0875
-14	193.0125
…	…
-254	191.5125
-266	191.4375
-278	191.3625

Table 33: Example 75GHz flexible grid

15.3.3 Flexible Grid Provisioning

The 400ZR coherent MIS IA [1] defines an alternate frequency provisioning model to allow a provisioning method for flexible DWDM grid systems. This alternative frequency provisioning model allows a direct setting of the frequency (i.e. no grid limitations) once enabled by a control register. The grid provisioning model remains the default model.

16 Summary

This 400ZR IA specifies the requirements of a 400GBASE-R PHY. The 400ZR PHY provides timing and code-word transparent transmission of a 400GBASE-R host signal over a single carrier optical interface (Black Link) with less than 1.0E-15 bit-errors. This coherent interface uses DP-16QAM, non-differential phase encoding/decoding, and a Concatenated FEC (C-FEC). The two application codes defined for this IA are:

- 120 km or less, amplified, point-to-point, DWDM noise limited links.
- Unamplified, single wavelength, loss limited links.

No restrictions are placed on the physical form factor by this IA. This 400ZR IA builds upon the work of other standards bodies including IEEE 802.3™-2018 and ITU-T SG-15.

17 References

17.1 Normative references

[1] Implementation Agreement for Coherent CMIS, IA # oif2019.015.06
[2] Standard for Ethernet: IEEE Std 802.3TM-2018
[3] ITU-T G.709/Y.1331 (2019), Amendment 3, Interfaces for the optical transport network.
[4] ITU-T G.709.1/Y.1331.1 (2018), Flexible OTN short-reach interfaces.
[5] ITU-T G.709.2/Y.1331.2 (2018), OTU4 long-reach interfaces.
[6] ITU-T G.709.3/Y.1331.3 (2018), Flexible OTN long-reach interfaces.
[7] ITU-T G.sup39 (02/2016), Optical system design and engineering considerations.

17.2 Informative references

[8] ITU-T G.694.1 (2012): Spectral grids for WDM applications: DWDM Frequency grid.
[9] EIC/TR 61282-10, Ed. 1.0, 201: Fibre optic communication system design guides- Part 10: Characterization of the quality of optical vector-modulated signals with the error vector magnitude.”

18 Appendix A: Glossary

Acronym	Definition	Acronym	Definition
AM	Alignment Marker	**NA**	Not Applicable
BER	Bit Error Ratio	**NCG**	Net Coding Gain
CD	Chromatic Dispersion	**OADM**	Optical Add/Drop Multiplexer
C-FEC	Concatenated FEC (Staircase FEC + Hamming)	**OSNR**	Optical Signal-to-Noise Ratio
DGD	Differential Group Delay	**PDL**	Polarization Dependent Loss
DP-*m*QAM	Dual Polarization – *m state* Quadrature Amplitude Modulation	**PMD**	Polarization Mode Dispersion
DSP	Digital Signal Processing	**QAM**	Quadrature Amplitude Modulation
DWDM	Dense Wavelength-Division Multiplexing	**R_s**	Single-Channel Reference point at the DWDM network element tributary output
EOL	End of Life	**SC-FEC**	StairCase FEC
EVM	Error Vector Magnitude	**SD-FEC**	Soft-Decision FEC
FEC	Forward Error Correction	**S_s**	Single-Channel Reference point at the DWDM network element tributary input
FFS	For Further Study	**SNR**	Signal-to-Noise Ratio
GMP	Generic Mapping Procedure	**SOP**	State of Polarization
HD-FEC	Hard-Decision FEC	**SOPMD**	Second Order Polarization Mode Dispersion
IA	Implementation Agreement	**TBD**	To Be Decided
LD	Local Degrade	**WDM**	Wavelength-Division Multiplexing
LO	Local Oscillator	**WSS**	Wavelength Selective Switching
LOS	Loss of Signal		

Table 34: Acronyms

19 Appendix B: Future work items

These items below will be considered as part of a maintenance update. Additional contributions are required to define these items.

1. EVM specifications
2. 75 GHz grid operation
    a. Once the Transmit Spectrum is defined it can replace Minimum Excess Bandwidth.
3. ZR+ definitions and specifications

20 Appendix C: Error Vector Magnitude

20.1 Maximum error vector magnitude

The Error vector magnitude is measured using a reference receiver as defined in Section 20.3. EVM_{rms} uses the **peak ref. vector** (not average) for normalization.

20.2 Maximum I-Q DC offset

The I-Q DC offset of a modulated signal relates to the average signal amplitudes in the I and Q phases of that signal. The relative excess (unmodulated) power, P_{excess}, is a measure of this impairment and is obtained from the parameters I_{mean} and Q_{mean} and P_{signal}, which are intermediate results during the evaluation of the Error Vector Magnitude:

$$P_{excess} = \frac{\mathrm{I}_{\mathrm{mean}}^2 + \mathrm{Q}_{\mathrm{mean}}^2}{\mathrm{P}_{\mathrm{Signal}}}$$

$$IQ_{offset} = 10\log_{10}(\mathrm{P}_{\mathrm{excess}})$$

20.3 Reference receiver for EVM and I-Q DC offset

The reference receiver includes the following hardware characteristics and processing steps:

20.3.1 Hardware characteristics:

- Dual-polarization coherent receiver. Ideally, the receiver should be calibrated over wavelength for:
  - Frequency response
  - Channel imbalances
  - IQ phase angle error
  - Timing skew
- Real-time Nyquist sampler with sampling rate equal to or larger than the 400ZR symbol rate.

20.3.2 Processing steps[1]:

- Polarization demultiplex.
- Retime and resample to one sample per symbol using a Gaussian-shaped low pass filter anti-aliasing filter with a 3-dB bandwidth of 0.5 times the symbol rate.
- Clock phase recovery.
- Frequency offset estimation and removal assuming a constant frequency offset over the given block size *N.*
- Carrier phase recovery.
- IQ-offset evaluation and compensation.
- Noise loading for EQ training and EVM evaluation.

  The amplitude A_{RMS} of the noise for each quadrature is calculated from the following equation:

[1] The processing is done block wise with block size $N = 1000$. It is possible to group multiple blocks for some of the processing steps. The processing steps should perform only the tasks mentioned in the description. Processing steps can be consolidated and changed in order but not perform any additional signal processing with the purpose of compensating for signal distortions resulting for example from CD, PMD, skews, crosstalk, etc.

$$A_{RMS} = \sqrt{\frac{0.814 \cdot R_{symbol}}{10^{\frac{OSNR}{10}} \cdot \Delta f_{ref}}}$$

where OSNR is 26 dB and,

$$\Delta f_{ref} = \frac{c}{\lambda^2} \cdot RB$$

where c is the velocity of light in vacuum, λ is the optical wavelength and RB is the resolution bandwidth that is 0.1 nm.

- Apply a 7-tap T-spaced FIR filter with the tap coefficients optimized for BER

  The sum of all filter tap coefficients is equal to one, and the largest coefficient can be for any of the 7 taps. The individual filter taps are found by minimizing the EVM_{RMS} value.

20.4 EVM evaluation

Find the peak vector normalization scaling factor[2]:

$$\alpha = \sqrt{\frac{\max\limits_{0\le k<K} \left(I_{\text{ref}}(k)^2 + Q_{\text{ref}}(k)^2\right)^2}{\frac{1}{K}\sum_{k=0}^{K-1}\left(I_{\text{ref}}(k)^2 + Q_{\text{ref}}(k)^2\right)}}$$

- Normalize the sample pairs I_δ and Q_δ in each of the polarizations using the average power multiplied by the peak vector constellation scaling factor[3]:

$$\alpha_{\text{peak}} = \alpha \sqrt{\frac{1}{N}\sum_{n=0}^{N-1}\left(I_\delta(n)^2 + Q_\delta(n)^2\right)}$$

- Find the nearest constellation pair $I_{\text{ref}}(n)$ and $Q_{\text{ref}}(n)$ for each normalized sample pair I_δ and Q_δ in each of the polarizations.
- Calculate the error vector magnitude for each normalized sample pair I_δ and Q_δ in each of the polarizations:

$$\text{EVM}(n) = \sqrt{\left(I_\delta(n) - I_{\text{ref}}(n)\right)^2 + \left(Q_\delta(n) - Q_{\text{ref}}(n)\right)^2}$$

  where n is the symbol number within the block starting at 0

- Using all the N samples from the x-polarization calculate $\text{EVM}_{\text{RMS},x}$:

$$\text{EVM}_{\text{RMS},x} = \sqrt{\frac{1}{N}\sum_{n=0}^{N-1}\text{EVM}(n)^2}$$

- Using all the N samples from the y-polarization and calculate $\text{EVM}_{\text{RMS},y}$:

[2] k runs over all points in the constellation
[3] This assumes that all constellation points have equal probability in the sample pairs

$$\mathrm{EVM}_{\mathrm{RMS},y} = \sqrt{\frac{1}{N}\sum_{n=0}^{N-1}\mathrm{EVM}(n)^2}$$

- Then calculate $\mathrm{EVM}_{\mathrm{RMS}}$ in percent from:

$$\mathrm{EVM}_{\mathrm{RMS}} = \sqrt{\frac{\left(\mathrm{EVM}_{\mathrm{RMS},x}^2 + \mathrm{EVM}_{\mathrm{RMS},y}^2\right)}{2}} \times 100\%$$

20.5 Reference Algorithms for EVM Test of 400ZR transmitters.

The EVM algorithms are attached in Table 35.

Description	Test Vector File
Error Vector Magnitude Algorithms[1]	400ZR EVM Test Vectors

Table 35: EVM algorithms

[1]Only available to OIF members at this time.

21 Appendix D: List of companies belonging to OIF when document is approved

Acacia Communications	Google
ADVA Optical Networking	Hewlett Packard Enterprise (HPE)
Alibaba	IBM Corporation
Alphawave IP Inc.	Idea Sistemas Electronicos S.A.
Amphenol Corp.	II-VI Incorporated
AnalogX Inc.	Infinera
Applied Optoelectronics, Inc.	InnoLight Technology Limited
Arista Networks	Innovium
BizLink Technology Inc.	Inphi
Broadcom Inc.	Integrated Device Technology
Cadence Design Systems	Intel
China information and communication technology Group Corporation	IPG Photonics Corporation
China Telecom Global Limited	Juniper Networks
Ciena Corporation	Kandou Bus
Cisco Systems	KDDI Research, Inc.
Corning	Keysight Technologies, Inc.
Credo Semiconductor (HK) LTD	Lumentum
Dell, Inc.	MACOM Technology Solutions
EFFECT Photonics B.V.	Marvell Semiconductor, Inc.
Elenion Technologies, LLC	Maxim Integrated Inc.
Epson Electronics America, Inc.	MaxLinear Inc.
eSilicon Corporation	MediaTek
Facebook	Mellanox Technologies
Foxconn Interconnect Technology, Ltd.	Microsemi Inc.
Fujikura	Microsoft Corporation
Fujitsu	Mitsubishi Electric Corporation
Furukawa Electric Japan	Molex
Global Foundries	Multilane SAL Offshore

NEC Corporation	SiFotonics Technologies Co., Ltd.
NeoPhotonics	Socionext Inc.
Nokia	Spirent Communications
NTT Corporation	Sumitomo Electric Industries, Ltd.
O-Net Communications (HK) Limited	Sumitomo Osaka Cement
Open Silicon Inc.	Synopsys, Inc.
Optomind Inc.	TE Connectivity
Orange	Tektronix
PETRA	Telefonica SA
Precise-ITC, Inc.	TELUS Communications, Inc.
Rambus Inc.	UNH InterOperability Laboratory (UNH-IOL)
Ranovus	Verizon
Rianta Solutions, Inc.	Viavi Solutions Deutschland GmbH
Rosenberger Hochfrequenztechnik GmbH & Co. KG	Xelic
Samsung Electronics Co. Ltd.	Xilinx
Samtec Inc.	Yamaichi Electronics Ltd.
Semtech Canada Corporation	ZTE Corporation

[EOD] End of Document