Keystone Architecture
DDR3 Memory Controller

User's Guide

Literature Number: SPRUGV8E
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About This Manual

The DDR3 memory controller is used to interface with JESD79-3C standard compliant SDRAM devices. Memory types such as DDR1 SDRAM, DDR2 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR3 memory controller SDRAM can be used for program and data storage.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

NOTE: Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION

Indicates the possibility of service interruption if precautions are not taken.

WARNING

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

C66x CorePac User Guide	SPRUGW0
C66x CPU and Instruction Set Reference Guide	SPRUGH7
Enhanced Direct Memory Access 3 (EDMA3) for KeyStone Devices User Guide	SPRUGS5
External Memory Interface (EMIF16) for KeyStone Devices User Guide	SPRUGZ3
Interrupt Controller (INTC) for KeyStone Devices User Guide	SPRUGW4

Introduction

This document describes the operation of the DDR3 module in the KeyStone II devices. (Refer to the device-specific data manual for exact device applicability.) The DDR3 module is accessible across all the cores and all system masters that are not cores.

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1.1 Purpose of the Peripheral

The DDR3 memory controller is used to interface with JESD79-3C standard compliant SDRAM devices. Memory types such as DDR1 SDRAM, DDR2 SDRAM, SDR SDRAM, SBSRAM, and asynchronous memories are not supported. The DDR3 memory controller SDRAM can be used for program and data storage. The KeyStone device has one instance.

1.2 Features

The DDR3 controller supports the following features:

- Supports JEDEC standard JESD79-3C – DDR3 compliant devices
- 33-bit address for 8 GB of address space
- 16/32/64-bit data bus width support
- CAS latencies: 5, 6, 7, 8, 9, 10, and 11
- 1, 2, 4, and 8 internal banks
- Burst Length: 8
- Burst Type: sequential
- 8GB address space available over one or two chip selects
- Page sizes: 256, 512, 1024, and 2048-word
- SDRAM auto initialization from reset or configuration change
- Self-refresh mode
- Prioritized refresh scheduling
- Programmable SDRAM refresh rate and backlog counter
- Programmable SDRAM timing parameters
- Big and little endian modes
- ECC on SDRAM data bus
- 8-bit ECC per 64-bit data quanta without additional cycle latency
- Two latency classes supported
- UDIMM Address mirroring is not supported

1.3 Industry Standard(s) Compliance Statement

The DDR3 controller is compliant with the JESD79-3C DDR3 SDRAM standard.

Peripheral Architecture

The DDR3 controller interfaces with most standard DDR3 SDRAM devices. It supports self-refresh mode and prioritized refresh. In addition, it provides flexibility through programmable parameters such as the refresh rate, CAS latency, and many SDRAM timing parameters. The following sections describe the architecture of the DDR3 controller as well as how to interface and configure it to perform read and write operations to DDR3 SDRAM devices. Examples for interfacing the DDR3 controller to a common DDR3 SDRAM device are shown in Section 3.1.

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2.1 Clock Interface

There are two clocking schemes in the DDR3 controller - the clocking scheme used to drive the DDR3 controller and the clocking scheme used to drive the DDR3 I/O interface. The DDR3 controller is clocked by the DSP/2 clock domain. The I/O interface is driven by the DDR3 memory clock (half the data rate).

2.2 SDRAM Memory Map

For information describing the DDR3 memory map, see the device-specific data manual.

2.3 Signal Descriptions

The DDR3 memory controller signals are shown in Figure 2-1 and described in Figure 2-1.

- The maximum data bus is 64-bits wide.
- The address bus is 33-bits wide.
- Two differential output clocks driven by internal clock sources.
- Command signals: Row and column address strobe, write enable strobe, data strobe, and data mask.
- Two chip selects and two clock enable signals.

Figure 2-1. DDR3 Memory Control Signals

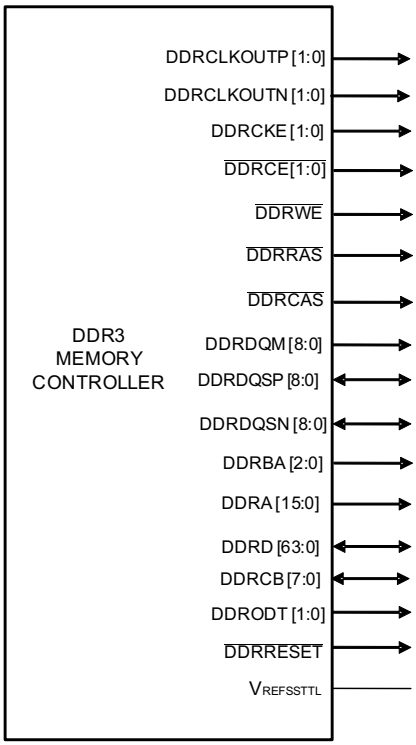


Table 2-1. DDR3 Memory Controller Signal Descriptions

Pin	Description
DDRD [63:0]	Bidirectional data bus. Input for data reads and output for data writes.
DDRCB [7:0]	Bidirectional data bus (check bits) for ECC byte lane. Input for data reads and output for data writes.
DDRA [15:0]	External address output.
DDRCE0	Active-low chip enable for memory space CE0. DDRCE0z is used to enable the DDR3 SDRAM memory device during external memory accesses.
DDRCE1	Active-low chip enable for memory space CE1. DDRCE1z is used to enable the DDR3 SDRAM memory device during external memory accesses.
DDRDQM [8:0]	Active-high output data mask.

Table 2-1. DDR3 Memory Controller Signal Descriptions (continued)

Pin	Description
DDR3CLKOUTP [1:0]/	Differential clock outputs.
DDR3CLKOUTN [1:0]	
DDRCKE [1:0]	Clock enable (used for self-refresh mode).
$\overline{\text{DDRCAS}}$	Active-low column address strobe.
$\overline{\text{DDRRAS}}$	Active-low row address strobe.
$\overline{\text{DDRWE}}$	Active-low write enable.
DDRDQSP [8:0]/	Differential data strobe bidirectional signals.
DDRDQSN [8:0]	
DDRODT [1:0]	On-die termination signal(s) to external DDR3 SDRAM
DDRBA [2:0]	Bank-address control outputs
VREFSSTTL	DDR3 Memory Controller reference voltage. This voltage must be supplied externally. For more details, see the device-specific data manual.
DDRSLRATE [1:0]	See the section on Slew Rate Control in the Hardware Design Guide for Keystone Devices (SPRABI2) for details.

2.4 Protocol Descriptions

The DDR3 memory controller supports the DDR3 SDRAM commands listed in Table 2-2.

Table 2-2. DDR3 SDRAM Commands

Command	Function
ACT	Activates the selected bank and row.
PREA	Precharge all command. Deactivates (precharges) all banks.
PRE	Precharge single command. Deactivates (precharges) a single bank.
DES	Device Deselect.
EMRS	Extended Mode Register set. Allows altering the contents of the mode register.
MRS	Mode register set. Allows altering the contents of the mode register.
NOP	No operation.
PDE	Power down entry
PDX	Power down exit
RD	Inputs the starting column address and begins the read operation.
REF	Autorefresh cycle
SRE	Self-refresh entry
SRX	Self-refresh exit
WR	Inputs the starting column address and begins the write operation.
ZQCS	ZQ Calibration short operation
ZQCL	ZQ Calibration long operation

Table 2-3 shows the signal truth table for the DDR3 SDRAM commands.

Table 2-3. Truth Table for DDR3 SDRAM Commands[1]

DDR3 SDRAM Signals	CKE		CS#	RAS#	CAS#	WE#	BA [2:0]	A [15:13]	A12	A10	A [9:0], A11
DDR3 Memory controller signals	DDRCKE		$\overline{DCE}$	$\overline{DDRRAS}$	$\overline{DDRCAS}$	$\overline{DDRWE}$	DDRBA [2:0]	DDRA [15:13]	DDRA [12]	DDRA [10]	DDRA [9:0],[11]
	Previous Cycle	Current Cycle									
ACT	H	H	L	L	H	H	BA	Row Address (RA)			
PREA	H	H	L	L	H	L	V	V	V	H	V
PRE	H	H	L	L	H	L	BA	V	V	L	V
MRS	H	H	L	L	L	L	BA	OP Code			
EMRS[2]	H	H	L	L	L	L	BA	OP Code			
RD (BL8)	H	H	L	H	L	H	BA	RFU	V	L	CA
WR (BL8)	H	H	L	H	L	L	BA	RFU	V	L	CA
REF	H	H	L	L	L	H	V	V	V	V	V
SRE[3]	H	L	L	L	L	H	V	V	V	V	V
SRX[3][4]	L	H	H	X	X	X	X	X	X	X	X
			L	H	H	H	V	X	V	V	V
NOP	H	H	L	H	H	H	V	V	V	V	V
DES[5]	H	H	H	X	X	X	X	X	X	X	X
PDE[6]	H	L	L	H	H	H	V	V	V	V	V
			X	X	X	X	X	X	X	X	X
PDX[6]	L	H	L	H	H	H	V	V	V	V	V
			X	X	X	X	X	X	X	X	X
ZQCL	H	H	L	H	H	L	X	X	X	H	X
ZQCS	H	H	L	H	H	L	X	X	X	L	X

(1) LEGEND: H = Logic High, L = Logic Low, X = Don't Care, RA = Row Address, CA = Column Address, RFU = Reserved for future use, V = Valid

(2) For extended mode register set (EMRS) command, bank address (BA) pins select an extended mode register (EMR).

(3) ODT function is not available during self-refresh.

(4) Self-refresh exit (SRE) is asynchronous.

(5) The Deselect (DES) command performs the same function as No Operation (NOP).

(6) The Power down mode does not perform any self-refresh operation.

2.4.1 Mode Register Set (MRS or EMRS)

DDR3 SDRAM contains mode and extended mode registers that configure the DDR3 memory for operation. These registers control burst type, burst length, CAS latency, DLL enable/disable, etc.

The DDR3 memory controller programs the mode and extended mode registers of the DDR3 memory by issuing MRS and EMRS commands. MRS and EMRS commands can be issued during DDR3 initialization as well as during normal operation as long as the external SDRAM is in idle state. When the MRS or EMRS command is executed, the value on DDRBA [1:0] selects the mode register to be written and the data on DDRA [12:0] is loaded into the register. DDRA [15:13] and DDRBA [2] are reserved and are programmed to 0 during MRS (or EMRS).

Each mode register allows programming of different sets of DDR3 SDRAM parameters. The DDR3 memory controller programs the mode registers in compliance with the JEDEC JESD79-3C spec. For more information about mode registers and how they are programmed, see the JEDEC spec.

2.4.2 Refresh Mode

The DDR3 memory controller issues refresh commands (REF) to the DDR3 SDRAM device. REF is automatically preceded by a Precharge-all (PREA) command, ensuring the deactivation of all CE spaces and banks selected.

Following the PREA command, the DDR3 memory controller begins performing refreshes at a rate defined by the refresh rate (REFRESH_RATE) field in the SDRAM refresh control register (SDRFC). In general, a refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for efficient operation, refresh commands can be postponed a maximum of 8 times. Also, at any given time a maximum of 16 refresh commands can issued within a 2 xtREFI interval. For more information on refresh command timing, see the JEDEC spec.

2.4.3 Activation

The ACTIVE command is used to open (or activate) a row in a specific bank for a subsequent access. DDRBA [2:0] select the bank, and the address provided on DDRA[15:0] selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

When the DDR3 memory controller issues an ACT command, a delay of tRCD is incurred before a read or write command is issued. Reads or writes to the currently active row and bank of memory can achieve much higher throughput than reads or writes to random areas because every time a new row is accessed, the ACT command must be issued and a delay of tRCD incurred.

2.4.4 Deactivation

The precharge command is used to deactivate the open row in a particular bank (PRE) or the open row in all banks (PREA). The bank(s) will be available for a subsequent row activation a specified time (tRP) after the precharge command is issued, except in the case of concurrent auto precharge, where a read or write command to a different bank is allowed as along as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. A PRE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. During a PREA command, DDRA [10] is driven high to ensure deactivation of all banks.

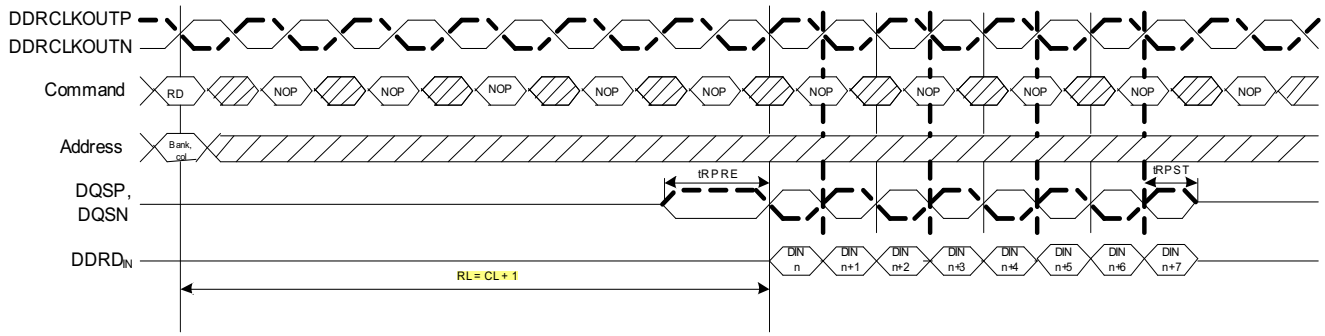
2.4.5 READ Command

Figure 2-2 shows the DDR3 memory controller performing a read burst from DDR3 SDRAM. The READ command initiates a burst read operation to an active row. The column address is driven on DDRA [15:0], and the bank address is driven on DDRBA [2:0].

The DDR3 memory controller uses a burst length of 8, and has a programmable CAS latency of 5, 6, 7, 8, 9, 10, or 11. The CAS latency is five cycles in Figure 2-2. Read latency can be programmed in the DDR PHY Control 1 register and can take integer values from CL+1 to CL+7. In this figure it has been programmed to CL + 1. Because the default burst size is 8, the DDR3 memory controller returns 8 words of data for every read command. Word size is nothing but the DDR3 interface bus width.

If additional accesses are not pending to the DDR3 memory controller, the read burst completes and the unneeded data is disregarded. If additional accesses are pending, based on the arbitration result, the DDR3 memory controller can terminate the read burst and start a new read burst.

Figure 2-2. READ Command



NOP commands are shown for ease of illustration ; other commands may be valid at these times

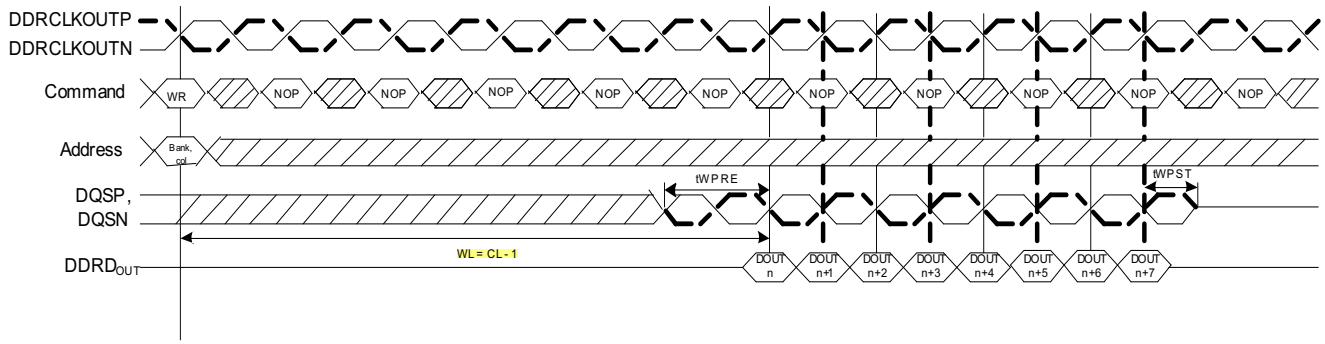
2.4.6 Write (WR) Command

Prior to a WRT command, the desired bank and row are activated by the ACT command. Following the WRT command, a write latency is incurred. Write latency is equal to CAS latency minus 1. All writes have a burst length of 8.

Figure 2-3 shows the timing for a write on the DDR3 memory controller. If the transfer request is for less than 8 words, depending on the scheduling result and the pending commands, the DDR3 memory controller can:

- Mask out the additional data using DDRDQM outputs
- Terminate the write burst and start a new write burst

Figure 2-3. WRITE Command



NOP commands are shown for ease of illustration; other commands may be valid at these times

2.5 Address Mapping

The DDR3 memory controller views external DDR3 SDRAM as one continuous block of memory across the two chip-selects. If smaller devices are used, the memory is seen to roll over. The DDR3 memory controller receives DDR3 memory access requests along with a 33-bit logical address from the rest of the system. The controller uses the logical address to generate a row/page, column, bank address, and chip selects for the DDR3 SDRAM. The number of bank and column address bits used is determined by the IBANK and PAGESIZE fields. The chip selection pins used are determined by the EBANK field (Table 2-4).

Table 2-4. Bank Configuration Register Fields for Address Mapping

Bit Field	Bit Value	Bit Description
IBANK		Defines the number of internal banks on external DDR3 memory
	0	1 bank
	1h	2 banks
	2h	4 banks
	3h	8 banks
PAGESIZE		Defines the page size of each page of the external DDR3 memory
	0	256 words (requires 8 column address bits)
	1h	512 words (requires 9 column address bits)
	2h	1024 words (requires 10 column address bits)
	3h	2048 words (requires 11 column address bits)
EBANK		External chip select setup. Defines whether SDRAM accesses use 1 or 2 chip select lines
	0	Use only chip enable 0 for all SDRAM accesses
	1	Use chip enables 0 and 1 for SDRAM accesses

NOTE: IBANK should always be programmed to 3h since DDR3 memory devices offer only 8-bank support unlike DDR2 with the option of 4-bank or 8-bank memory devices.

The IBANK_POS bit field in the SDRAM Config Register (SDCFG) determines how many banks the DDR3 controller can interleave amongst. For IBANK POS = 0, as source address increments across SDRAM page boundaries, the DDR3 controller moves to the same page in the next bank on current device (chip-select).

After the page has been accessed in all banks of the current device, the same page is accessed in all banks in the next device. This is followed by accessing the next page in the first device and the process continues. To the DDR3 SDRAM, this process looks as shown on Figure 2-5. Thus IBANK_POS = 0 serves to maximize number of open banks within overall SDRAM space. The ROWSIZE parameter is not used by the DDR3 controller if IBANK_POS = 0. See Figure 2-5.

Thus 16 banks (eight internal banks across two chip selects) can be kept open at a time, interleaving among all of them.

Table 2-5. Logical Address-to-SDRAM Address Mapping for IBANK_POS = 0

Logical Address [32:N]							
Row Address		Chip Select		Bank Address[2:0]		Column Address	
ROW SIZE	nrb	EBANK	ncs	IBANK	nbb	PAGE SIZE	ncb
Don't care	16 bits	0	0 bits	0	0 bits	0	8 bits
		1	1 bit	1	1 bit	1	9 bits
				2	2 bits	2	10 bits
				3	3 bits	3	11 bits
Logical address mapping for row address		Logical address mapping for chip select		Logical address mapping for bank address[1:0]		Logical address mapping for column address	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
M3+nrb-1	M3+1	M3=M2+ ncs-1	M2+1	M2=M1+ nbb-1	M1+1	M1=N+ ncb-1	N

NOTE: N=1 for 16-bit SDRAM, N=2 for 32-bit SDRAM and N=3 for 64-bit SDRAM. ROWSIZE is not used for IBANK_POS =0. nrb = Number of row bits. ncs = Number of chip select bits. nbb = Number of bank select bits determined by bank address [2:0].

For example, if IBANK = 3, PAGESIZE = 3 and EBANK = 1, the address mapping for a 64-bit SDRAMs would be as shown below in Table 2-6. For 64-bit, N = 3.

Table 2-6. Address Mapping Example (IBANK_POS=0, IBANK=3, PAGESIZE=3, EBANK=1, 64-bit SDRAM)

SDCFG bit			Logical Address			
IBANK	EBANK	PAGESIZE	33:18	17	16:14	13:3
3	1	3	Don't care	ncs=1	nbb=3	ncb=11

For IBANK_POS = 1, interleaving is the same as IBANK_POS = 0 but limited to 4 banks per device (per chip select). Thus 16 banks (8 internal banks across 2 chip selects) can be kept open at a time, but interleaving among only 8 of them. The address mapping is shown in Table 2-7.

Table 2-7. Logical Address-to-SDRAM Address Mapping for IBANK_POS = 1

Logical Address [32:N]									
Bank Address [2]		Row Address		Chip Select		Bank Address [1:0]		Column Address	
IBANK	nbb2	ROW SIZE	nrb	EBANK	ncs	IBANK	nbb10	PAGE SIZE	ncb
0	0 bits	0	9 bits	0	0 bits	0	0 bits	0	8 bits
1	0 bits	1	10 bits	1	1 bit	1	1 bit	1	9 bits
2	0 bits	2	11 bits			2	2 bits	2	10 bits
3	1 bit	3	12 bits			3	2 bits	3	11 bits
		4	13 bits						
		5	14 bits						
		6	15 bits						
		7	16 bits						
Logical address mapping for bank_address[2]		Logical address mapping for row address		Logical address mapping for chip select		Logical address mapping for bank address[1:0]		Logical address mapping for column address	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
M4+nbb2-1	M4+1	M4=M3+ nrb-1	M3+1	M3=M2+ ncs-1	M2+1	M2=M1+ nbb10-1	M1+1	M1=N+ ncb-1	N

NOTE: N=1 for 16-bit SDRAM; N=2 for 32-bit SDRAM; N=3 for 64-bit SDRAM. ncb = Number of column address bits. nrb = Number of row bits. ncs = Number of chip select bits. nbb10 = Number of bank select bits determined by bank address [1:0]. nbb2 = Number of bank select bits determined by bank address[2].

For IBANK_POS = 2, interleaving is the same as IBANK_POS = 0 but limited to 2 banks per device (per chip select). Thus 16 banks (8 internal banks across 2 chip selects) can be kept open at a time, but interleaving among only 4 of them. The address mapping is shown in Table 2-8. An address mapping table for the desired configuration can be generated on the lines of Table 2-6.

Table 2-8. Logical Address-to-SDRAM Address Mapping for IBANK_POS = 2

Logical Address [32:N]									
Bank Address [2:1]		**Row Address**		**Chip Select**		**Bank Address [0]**		**Column Address**	
IBANK	**nbb21**	**ROW SIZE**	**nrb**	**EBANK**	**ncs**	**IBANK**	**nbb0**	**PAGE SIZE**	**ncb**
0	0 bits	0	9 bits	0	0 bits	0	0 bits	0	8 bits
1	0 bits	1	10 bits	1	1 bit	1	1 bit	1	9 bits
2	1 bit	2	11 bits			2	1 bit	2	10 bits
3	2 bits	3	12 bits			3	1 bit	3	11 bits
		4	13 bits						
		5	14 bits						
		6	15 bits						
		7	16 bits						
Logical address mapping for bank_address[2:1]		Logical address mapping for row address		Logical address mapping for chip select		Logical address mapping for bank address[0]		Logical address mapping for column address	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
M4+ nbb21-1	M4+1	M4=M3+ nrb-1	M3+1	M3=M2+ ncs-1	M2+1	M2=M1+ nbb0-1	M1+1	M1=N+ ncb-1	N

NOTE: N=1 for 16-bit SDRAM; N=2 for 32-bit SDRAM; N=3 for 64-bit SDRAM. ncb = Number of column address bits. nrb = Number of row bits. ncs = Number of chip select bits. nbb0 = Number of bank select bits determined by bank address [0]. nbb21 = Number of bank select bits determined by bank address[2:1]

For IBANK_POS = 3, interleaving among banks within a device (per chip select) is not permitted. Thus, 16 banks (8 internal banks across 2 chip selects) can be kept open at a time, but interleaving among only 2 of them. Table 2-9 shows the address mapping. Address mapping for the desired configuration can be generated on the lines of Table 2-6.

Table 2-9. Logical Address-to-SDRAM Address Mapping for IBANK_POS = 3

Logical Address [32:N]							
Bank Address [2:0]		**Row Address**		**Chip Select**		**Column Address**	
IBANK	**nbb20**	**ROW SIZE**	**nrb**	**EBANK**	**ncs**	**PAGE SIZE**	**ncb**
0	0 bits	0	9 bits	0	0 bits	0	8 bits
1	1 bit	1	10 bits	1	1 bit	1	9 bits
2	2 bits	2	11 bits			2	10 bits
Logical address mapping for bank_address[2:0]		Logical address mapping for row address		Logical address mapping for chip select		Logical address mapping for column address	
MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB
M3+nbb20-1	M3+1	M3=M2+nrb-1	M2+1	M2=M1+ncs-1	M1+1	M1=N+ncb-1	N

The DDR3 memory controller never opens more than one page per bank. The active row is left open until it becomes necessary to close it, thus decreasing the deactivate-reactivate overhead.

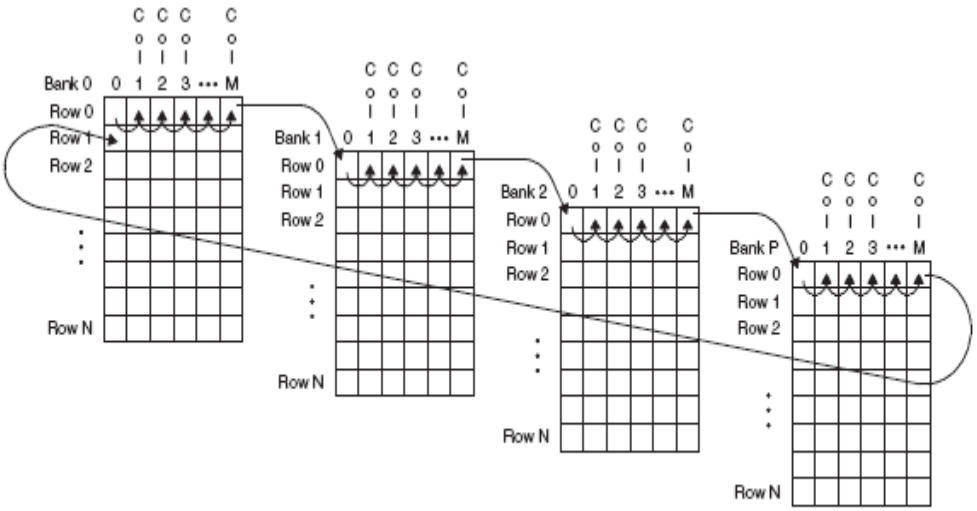
The number of banks between which the controller can interleave is maximum when IBANK_POS=0 and reduces progressively as IBANK_POS is increased from 1 to 3. Thus, maximum performance is obtained when IBANK_POS=0. However, to trade off performance for power savings, the application can program IBANK_POS to a non-zero value.

Figure 2-4. Logical Address-to-DDR3 SDRAM Address Map (EBANK=0)

Col. 0	Col. 1	Col. 2	Col. 3	Col. 4	• • •	Col. M–1	Col. M	
					• • •			Row 0, bank 0
					• • •			Row 0, bank 1
					• • •			Row 0, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row 0, bank P
					• • •			Row 1, bank 0
					• • •			Row 1, bank 1
					• • •			Row 1, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row 1, bank P
					• • •			•
					• • •			•
					• • •			•
					• • •			Row N, bank 0
					• • •			Row N, bank 1
					• • •			Row N, bank 2
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
•	•	•	•	•	• • •	•	•	•
					• • •			Row N, bank P

A M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.

Figure 2-5. DDR3 SDRAM Column, Row, and Bank Access (EBANK=0)



A M is number of columns (as determined by PAGESIZE) minus 1, P is number of banks (as determined by IBANK) minus 1, and N is number of rows (as determined by both PAGESIZE and IBANK) minus 1.

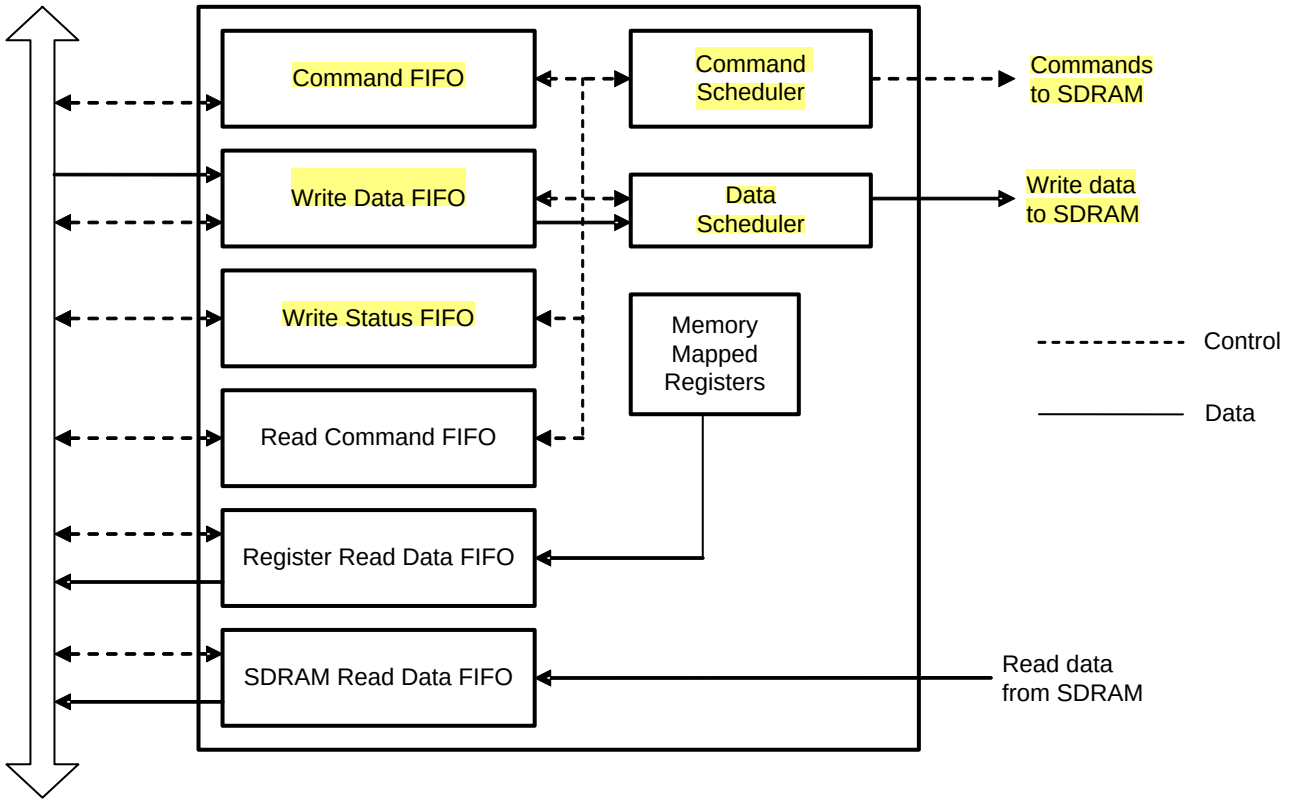
2.6 DDR3 Memory Controller Interface

To move data efficiently from on-chip resources to an external DDR3 SDRAM device, the DDR3 memory controller makes use of a Command FIFO, a Write Data FIFO, a Write Status FIFO, a Read Command FIFO, and two Read Data FIFOs and command and data schedulers. Table 2-10 describes the purpose of each FIFO. Figure 2-6 shows the block diagram of the DDR3 memory controller FIFOs. Commands, write data, and read data arrive at the DDR3 memory controller parallel to each other. The same peripheral bus is used to write and read data from external memory as well as internal memory-mapped registers (MMR).

Table 2-10. DDR3 Memory Controller FIFO Description

FIFO	Description	Depth
Command	Stores all commands coming from on-chip requestors	16
Write Data	Stores write data coming from on-chip requestors to memory	20 (512-bit wide)
Write Status	Stores the write status information for each write transaction	7
Read Command	Stores all read transactions that are to be issued to on-chip requestors	22
SDRAM Read Data	Stores read data coming from SDRAM memory to on-chip requestors	22 (256-bit wide)
Register Read Data	Stores read data coming from MMRs to on-chip requestors	2 (256-bit wide)

Figure 2-6. DDR3 Memory Controller FIFO Block Diagram



2.6.1 Arbitration

The DDR3 memory controller performs command reordering and scheduling in an attempt to achieve efficient transfers with maximum throughput. The goal is to maximize the utilization of the data, address, and command buses while hiding the overhead of opening and closing DDR3 SDRAM rows. Command reordering takes place within the command FIFO.

The DDR3 memory controller examines all the commands stored in the command FIFO to schedule commands to the external memory. For each master, the DDR3 memory controller reorders the commands based on the following rules:

- The DDR3 controller will advance a read command before an older write command from the same master if the read is to a different block address (2048 bytes) and the read priority is equal to or greater than the write priority.
- The DDR3 controller will block a read command, regardless of the master or priority if that read command is to the same block address (2048 bytes) as an older write command.

Thus, one pending read or write for a master might exist.

- Among all pending reads, the DDR3 controller selects all reads that have their corresponding SDRAM banks already open.
- Among all pending writes, the DDR3 controller selects all writes that have their corresponding SDRAM banks already open.

As a result of the above reordering, several pending reads and writes may exist that have their corresponding banks open. The highest priority read is selected from pending reads, and the highest priority write from pending writes. If two or more commands have the highest priority, the oldest command is selected. As a result, there might exist a final read and a final write command. Either the read or the write command will be selected depending on the value programmed in the Section 4.30.

The DDR3 controller supports interleaving of commands for maximum efficiency. In other words, the controller will partially execute one command and switch to executing another higher priority command before finishing the first command.

Apart from reads and writes the DDR3 controller also needs to open and close SDRAM banks, and maintain the refresh counts for an SDRAM. The priority of SDRAM commands with respect to refresh levels are as follows:

1. (Highest priority) SDRAM refresh request due to Refresh Must level of refresh urgency reached.
2. Read request without a higher priority write (from the reordering algorithm above)
3. Write request.
4. SDRAM Activate commands.
5. SDRAM Deactivate commands.
6. SDRAM Power-Down request.
7. SDRAM refresh request due to Refresh May or Release level of refresh urgency reached.
8. (Lowest priority) SDRAM self-refresh request.

2.6.2 Command Starvation

While running the scheduling algorithm described in Section 2.6.1, the DDR3 memory controller is subject to the following:

1. A continuous stream of high priority commands can block lower priority commands.
2. A continuous stream of SDRAM commands to a row in an open bank can block commands to another row in the same bank.

To avoid a continuous blocking effect, the priority of the oldest command is momentarily raised over all other commands when the latency counter for the oldest command expires. The latency counter for the oldest command (PR_OLD_COUNT) is configurable in the Latency Configuration Register. In addition to this, the order of command accesses can also be tailored by grouping commands into two categories or "classes" and assigning different latency expiration counters to each category. See Section 2.6.4 for more information.

On top of the above scheduling, the highest priority condition is a removal of hard or soft reset. If this occurs, the DDR3 controller abandons whatever it is currently doing and commences its startup sequence. In this case, commands and data stored in the FIFOs are lost. The startup sequence also commences whenever the SDRAM Config register is written and INITREF_DIS field in SDRAM Refresh Control register (SDRFC) is set to 0. In this case, commands and data stored in the FIFOs are not lost. The DDR3 controller will ensure that in-flight read or write transactions to the SDRAM are complete before starting the initialization sequence.

2.6.3 Possible Race Condition

A race condition may exist when certain masters write data to the DDR3 memory controller. For example, if master A passes a software message via a buffer in DDR3 memory and does not wait for indication that the write completes, when master B attempts to read the software message it may read stale data and therefore receive an incorrect message. In order to confirm that a write from master A has landed before a read from master B is performed, master A must wait for the write to complete before indicating to master B that the data is ready to be read. For example, an EDMA transfer controller should wait for the transfer completion event to occur before signaling a CorePac to read the message from DDR3.

If master A does not wait for indication that a write is complete, it must perform the following workaround:

1. Perform the required write.
2. Perform a dummy write to the DDR3 memory controller module ID and revision register.
3. Perform a dummy read to the DDR3 memory controller module ID and revision register.
4. Indicate to master B that the data is ready to be read after completion of the read in step 3. The completion of the read in step 3 ensures that the previous write was done.

2.6.4 Class of Service

The commands in the Command FIFO can be mapped to two classes of service: 1 and 2. The mapping of commands to a particular class of service can be done based on the priority or the master ID. The mapping based on priority can be done by setting the appropriate values in the Priority to Class of Service Mapping register. The mapping based on master ID can be done by setting the appropriate values of master ID and the masks in the Master ID to Class of Service Mapping registers.

There are three master ID and mask values that can be set for each class of service. In conjunction with the masks, each class of service can have a maximum of 144 master IDs mapped to it. For example, a master ID value of 0xFF along with a mask value of 0x3 will map all master IDs from 0xF8 to 0xFF to that particular class of service. By default all commands will be mapped to class of service 2.

Each class of service has an associated latency counter. The value of this counter can be set in the Latency Configuration register. When the latency counter for a command expires, i.e., reaches the value programmed for the class of service that the command belongs to, that command will be the one that is executed next. If there is more that one command that has expired latency counters, the command with the highest priority will be executed first. One exception to this rule is as follows: if any of the commands with the expired latency counters is also the oldest command in the queue, that command will be executed first irrespective of priority. This is done to prevent a continuous block effect as described in Section 2.6.1.

2.7 Refresh Scheduling

The DDR3 controller uses two counters to schedule AUTO REFRESH commands:

- a 13-bit decrementing refresh interval counter
- a four-bit refresh backlog counter

The interval counter is loaded with the REFRESH_RATE field value at reset. The interval counter decrements by one each cycle until it reaches zero at which point it reloads from REFRESH_RATE and restarts decrementing. The counter also reloads and restarts decrementing whenever the REFRESH_RATE field is updated.

The refresh backlog counter records the number of AUTO REFRESH commands that are currently outstanding. The backlog counter increments by one each time the interval counter reloads (unless it has reached its maximum value of 15). The backlog counter decrements by one each time the DDR3 controller issues an AUTO REFRESH command (unless it is already at zero). Following a refresh command, the DDR3 memory controller waits T_RFC cycles, defined in the SDRAM timing 3 register (SDTIM1), before rechecking the refresh urgency level.

For the range of values that the backlog counter can take, there are three levels of urgency with which the DDR3 controller should perform an auto refresh cycle (in which it issues AUTO REFRESH commands), as follows:

- Refresh May level is reached whenever the backlog count is greater than 0, to indicate that there is a refresh backlog, so if the DDR3 controller is not busy and none of the SDRAM banks are open, it should perform an auto refresh cycle.
- Refresh Release level is reached whenever the backlog count is greater than 4, to indicate that the refresh backlog is getting high, so if the DDR3 controller is not busy it should perform an auto refresh cycle even if any banks are open.
- Refresh Must level is reached whenever the backlog count is greater than 7, to indicate that the refresh backlog is getting excessive and the DDR3 controller should perform an auto refresh cycle before servicing any new memory access requests.

The DDR3 controller starts servicing new memory accesses after Refresh Release level is cleared. If any of the commands in the Command FIFO have class-of-service latency counters that are expired, the DDR3 controller will not wait for Refresh Release level to be cleared but will only perform one refresh command and exit the refresh state.

The refresh counters do not operate when SDRAM has been put into self-refresh mode. Also, the refresh counters start tracking the missed refreshes only after initialization is complete.

2.8 Self-Refresh Mode

The DDR3 memory controller supports self-refresh mode for low power. The controller maintains DDRCKE low to maintain the self-refresh state. In self-refresh, the memory maintains valid data while consuming a minimal amount of power.

Self-refresh mode is set by programming the LP_MODE in the Power Management Control register (PMCTL) to 2. The controller automatically puts the SDRAM into self-refresh after the controller is idle for SR_TIM DDR3CLKOUT cycles. (See Section 4.8 for more information.)

The memory is brought out of self-refresh under any of the following conditions:

- If the LP_MODE field is set not equal to 2
- A memory access is requested
- SR_TIM bit in PMCTL is cleared

In a situation where memory accesses and a self-refresh command are sent to the DDR3 memory controller, the controller always prioritizes the memory access. Thus, if a reset is triggered when memory accesses and a self-refresh command are queued in the controller, it is likely that self-refresh will not be entered.

The user must ensure that all memory accesses have been completed, and verify that self-refresh is set in the STATUS register before initiating a reset.

NOTE: The DDR3 memory controller completes all pending memory accesses and refreshes before it puts SDRAM into self-refresh. If a request for a memory access is received, the DDR3 memory controller services the memory access request then returns to the self-refresh state upon completion.

CAUTION

A special case may exist where the DDR3 controller violates the DDR3 JEDEC standard by issuing excessive refreshes (more than 16) within twice the tREFI interval when in self refresh mode. A workaround exists to conform to the JEDEC standard. Refer to the Errata document for your device for the advisory and workaround.

2.8.1 Extended Temperature Range

The normal operating temperature range for DDR3 SDRAMs is typically 0 to 85°C. When operating in self-refresh mode within the extended temperature range (85°C to 95°C), the memory device must be refreshed at 2× the normal refresh rate. For this purpose, either the auto self-refresh (ASR) or self-refresh temperature (SRT) feature should be used. Under normal operating conditions, both ASR and SRT should be disabled (equal to 0). When ASR is enabled, the internal refresh rate of the SDRAM automatically switches to 2× the refresh rate when the operating case temperature Tc is greater than 85°C when in Self-refresh mode. When SRT is enabled, the internal refresh rate of the SDRAM is forced to 2× the refresh rate regardless of Tc. Both SRT and ASR cannot be enabled at the same time. One must be disabled if the other is enabled.

NOTE: ASR and SRT are used only in self-refresh mode (LP_MODE=0×2). When operating in extended temperature range with LP_MODE = 0×0 (not in self-refresh), it is up to the user to program the manual refresh rate to 2× the normal refresh rate for proper operation. If it is guaranteed that Tc will exceed 85°C, it is recommended that SRT=1 to force the refresh rate to 2× regardless of operating temperature.

2.9 Reset Considerations

The DDR3 memory controller can be reset through a hard reset or a soft reset. A hard reset resets the state machine, the FIFOs, and the internal registers. A soft reset only resets the state machine and the FIFOs. A soft reset does not reset the internal registers except for the interrupt registers. Register accesses cannot be performed while either reset is asserted.

The DDR3 memory controller hard and soft reset are derived from device-level resets. Table 2-11 shows the relationship between the device-level resets and the DDR3 memory controller resets. For more information on the device-level resets, see the device-specific data manual.

Table 2-11. Device and DDR3 Memory Controller Reset Relationship

DDR3 Memory Controller	Reset Effect	Initiated by
Hard reset	Resets control logic and all DDR3 memory controller registers	• Please refer to the reset controller description in your device data manual
Soft reset	Resets control logic and interrupt registers	• Please refer to the reset controller description in your device data manual

2.10 Turnaround Time

Table 2-12 shows the turn around time that the DDR3 memory controller introduces on the data bus for various back-to-back accesses. Note that the DDR3 memory controller takes advantage of the CAS latencies and packs the commands as close as possible on the control bus to introduce the following turn around time on the data bus.

Table 2-12. Turnaround Time

Previous Access	Next Access	Turnaround Time (DDR3 memory clock cycles)
SDRAM Write	SDRAM Write to same chip select	0
SDRAM Write	SDRAM Write to different chip select	T CSTA + 1
SDRAM Read	SDRAM Read to same chip select	0
SDRAM Read	SDRAM Read to different chip select	T CSTA + 1
SDRAM Write	SDRAM Read	T WTR + 1 + CL
SDRAM Read	SDRAM Write	T_RTW + 1

2.11 DDR3 SDRAM Memory Initialization

DDR3 SDRAM initialization is achieved by programming memory mapped registers in the DDR3 controller configuration space and the Bootcfg space in a specific sequence. The software programming sequence is described in the Keystone I DDR3 Initialization Application Note. This sequence of software programming steps, causes the controller to issue MRS and EMRS commands to program mode and extended mode registers in the SDRAM device. These registers control parameters such as burst type, burst length, and CAS latency. The sequence of commands during the initialization sequence described in Section 2.11.1. The initialization sequence performed by the DDR3 memory controller is compliant with the JESD79-3C specification.

The DDR3 memory controller performs the initialization sequence under the following conditions:

- Automatically following a hard or soft reset (see Section 2.11.1)
- Following a write to the SDRAM configuration register (SDCFG) (see Section 2.11.1)

At the end of the initialization sequence, the DDR3 memory controller performs an auto-refresh cycle, leaving the DDR3 memory controller in an idle state with all banks deactivated.

During the initialization sequence, the DDR3 memory controller issues MRS and EMRS commands that configure the DDR3 SDRAM mode registers with the values described in Table 2-13 and Table 2-14.

When a reset occurs, the DDR3 memory controller immediately begins the initialization sequence. Under this condition, commands and data stored in the DDR3 memory controller FIFOs will be lost. However, when the initialization sequence is initiated by a write to the SDCFG Register, data and commands stored in the DDR3 memory controller FIFOs will not be lost and the DDR3 memory controller will ensure read and write commands are completed before starting the initialization sequence.

As the default values of the Mode Register (MR) and extended mode registers 1, 2, 3 are not defined, contents of Mode/Extended Mode Registers must be fully initialized and/or reinitialized, i.e., written, after power up and/or reset for proper operation. Also the contents of the Mode/Extended Mode Registers can be altered by re-executing the MRS/EMRS command during normal operation. The mode/extended mode registers are selected by varying the bank address bits BA [1:0]. BA [2] and A [15:13] are reserved for future use and must be programmed to zero.

The extended mode register 3 is configured with a value of 0h.

Table 2-13. DDR3 SDRAM Extended Mode Register 2 Configuration(1)

Mode Register Bit	Mode Register Field	Init Value	Description
15-11	Reserved	0x0	Reserved
10-9	Rtt_WR	SDCFG.DYN _ODT	Dynamic ODT value from SDRAM Config Register
8	Reserved	0x0	Reserved
7	SRT	SDRCR.SRT	Self-Refresh temperature range from SDRAM Refresh Control register
6	ASR	SDRCR.ASR	Auto self-refresh enable from SDRAM Refresh Control register
5-3	CWL	SDCFG.CWL	CAS write latency from SDRAM Config register
2-0	PASR	SDRCR.PASR	Partial array self-refresh from SDRAM Refresh Control register

(1) Bank Address bits to select EMR 2 are BA [1:0] = 0x2.

Table 2-14. DDR3 SDRAM Extended Mode Register 1 Configuration(1)

Mode Register Bit	Mode Register Field	Init Value	Description
12	Qoff	0x0	Output Buffer Enabled
11	TDQS	0x0	TDQS enable/disable
10	Reserved	0x0	Reserved
9	Rtt_nom	SDCFG.DDRTERM[2]	DDR3 termination resistor value from SDRAM Config register
8	Reserved	0x0	Reserved
7	Level	0x0	Write Leveling Disabled
6	Rtt_nom	SDCFG.DDRTERM[1]	DDR3 termination resistor value from SDRAM Config register
5	Output driver impedance	SDCFG.SDRAM _DRIVE[1]	SDRAM drive strength from SDRAM Config register
4-3	Additive Latency	0x0	Additive latency = 0
2	Rtt_nom	SDCFG.DDRTERM [0]	DDR3 termination resistor value from SDRAM Config register
1	Output driver impedance	SDCFG.SDRAM _DRIVE[0]	SDRAM drive strength from SDRAM Config register
0	DLL Enable	0x0	DLL enable/disable from SDRAM Config register

(1) Bank Address bits to select EMR 1 are BA [1:0] = 0x1.

Table 2-15. DDR3 SDRAM Mode Register 0 Configuration(1)

Mode Register Bit	Mode Register Field	Init Value	Description
12	DLL control for Precharge PD	0x0	Fast exit active powerdown exit time
11-9	Write Recovery	SDTIM1.T_WR	Write recovery for auto precharge from SDAM Timing 1 Register
8	DLL Reset	0x1	DLL Reset
7	Mode	0x0	Normal Mode from SDRAM Config Register
6-4	CAS Latency	SDCFG.CL[3:1]	CAS Latency from SDRAM Config Register
3	Read Burst Type	0x0	sequential/interleave burst type
2	CAS Latency	SDCFG.CL[0]	CAS Latency from SDRAM Config Register
1-0	Burst length	0x0	Burst length of 8

(1) Bank Address bits to select MR are BA [1:0] = 0x0.

2.11.1 DDR3 Initialization Sequence

On coming out of reset if the SDRAM_TYPE field in the SDRAM Config register is equal to 3 and the INITREF_DIS bit in the SDRAM Refresh Control register is set to 0, the DDR3 Controller performs a DDR3 SDRAM initialization sequence. The sequence follows the JEDEC standard. Please refer to the JEDEC spec for the initialization sequence.

The DDR3 memory controller also performs the initialization sequence whenever the SDRAM Config register is written. But in this case, the sequence starts at step 3. The DDR3 memory controller does not perform any transactions until the DDR3 initialization sequence is complete.

2.12 Dual Rank Support

The Keystone-I device also offers dual rank support. The device uses both chip selects (DCE0 and DCE1), with each chip select enabling access to one of the two SDRAM ranks. To enable dual rank access:

1. Set use_rank0_delays bit in the DDR3_CONFIG_12 register to 1. This directs the PHY leveling logic to use one set of optimal leveling values to access both ranks. This write must immediately follow the completion of the leveling process.
2. Set the EBANK bit in the SDCFG register to 1. This directs the controller to use both chip selects, one for each rank.

See the section on Dual Rank Support in the Keystone-I DDR3 Initialization App note for the proper sequence of initialization steps. Although dual rank access is supported, address mirroring is not.

2.13 Leveling

The DDR3 controller supports a new feature called leveling to compensate for the command and DQS skew as a result of the fly-by topology. Leveling compensates the skew for both reads and writes. Both full leveling and incremental leveling are supported. The controller does not perform full leveling after initialization. It must be first enabled by software after initialization.

2.13.1 Full Leveling (Auto Leveling)

Full leveling or auto leveling consists of write leveling, read data eye training and read DQS gate training. Write leveling is used to compensate for the command-to-DQS delay for writes. Read DQS gate training is used by the internal DDR3 controller logic before read data eye leveling to determine the most appropriate time to ensure a valid DQS coming into the DDR3 controller from the SDRAM. Read data eye training then tries to align the valid DQS to the center of the DQ line for reads by adjusting the DQS delay relative to DQ.

Leveling (both full and incremental) can be enabled by writing a '1' to the RDWRLVL_EN field in the Read-Write Leveling Ramp Control register (RDWR_LVL_RMP_CTRL). Once enabled, full leveling can be triggered by writing a ‘1’ to the RDWRLVLFULL_START bit in the Read-Write Leveling Control Register (RDWR_LVL_CTRL). Once triggered, all three full levelings (write leveling, read DQS gate training and read data eye training) will be performed. Thus there is no independent control over individual leveling types for full leveling.

NOTE: Full leveling violates the refresh interval; data inside DDR3 can be lost if full leveling is performed during normal operation. It is recommended that full leveling be performed after initialization and before any transactions to the DDR3 memory device are initiated. Any subsequent full leveling will not guarantee the data integrity inside the memory. During normal operation, temperature and voltage can be better tracked by incremental leveling.

2.13.2 Incremental Leveling

Incremental leveling is a feature that can be used to track voltage and temperature (V-T) changes over time as these can negatively impact the DQS de-skewing process that has occurred after full leveling. After performing full leveling once, incremental leveling can be performed periodically to more accurately track V-T drifts. Incremental leveling allows for greater control over the individual leveling types - write, read DQS gate and read data eye. Each of these levelings can be programmed to occur at a different rate. The rate is measured in terms of refresh periods. RDWRLVLINC_PRE is the base period defined in terms of number of refresh intervals. WRLVLINC_INT, RDLVLGATEINC_INT, and RDLVLINC_INT fields in the RDWR_LVL_CTRL register can be used to program independent leveling intervals (in number of the base period) for write leveling, gate training and read data eye leveling respectively. The respective leveling is triggered when its interval expires.

2.13.2.1 Ramp Incremental Leveling

What was described above can be referred to as standalone incremental leveling which is software-triggered. Ramp incremental leveling can only be used for DSPs that support Smart-reflex Class-3 (SR Class-3). Because SR Class-3 is not supported by Keystone-I devices, the ramp incremental leveling feature is also not supported.

2.13.3 Impact On Bandwidth

The DDR3 controller does not perform any reads/writes during incremental leveling. So a faster incremental leveling rate will have a larger impact on throughput than programming a smaller rate. Also, programming the intervals such that they all don't expire at the same time can minimize the impact on bandwidth.

NOTE: At this time there are no "best practices" recommendations for setting the incremental leveling intervals. The choice is entirely up to the application depending on the bandwidth tradeoff and environmental conditions expected.

2.13.4 Programming Full Leveling

Leveling (both full and incremental) is executed separately for each byte lane (clock-DQS pair). Therefore, the leveling process converges separately for each byte lane. To ensure that leveling converges correctly, the DDR3 controller must be given an initial set of values to use during leveling. The leveling process uses these initial values to arrive at a set of converged values for each byte lane. These initial values should be plugged into a set of memory-mapped registers in the Boot configuration section.

The user should note that the DATAx registers in steps 2 and 3 below map to specific byte lanes as follows (note the difference between C665x and other device variants). The mapping is consistent for write leveling and gate leveling initial values i.e. DATA *n*_PHY_WRLVL_INIT_RATIO and DATA *n*_PHY_GATELVL_INIT_RATIO map to the same byte lane. DATA *m*_PHY_WRLVL_INIT_RATIO and DATA *m*_PHY_GATELVL_INIT_RATIO map to the same byte lane.

Table 2-16. DATAx register to byte lane mapping

Register	C665x devices (36-bit)	All other Keystone-I devices (72-bit)
DATA0_*	Byte lane 3	Byte lane 7
DATA1_*	Byte lane 2	Byte lane 6
DATA2_*	Byte lane 1	Byte lane 5
DATA3_*	Byte lane 0	Byte lane 4
DATA4_*	NA	Byte lane 3
DATA5_*	NA	Byte lane 2
DATA6_*	NA	Byte lane 1
DATA7_*	NA	Byte lane 0
DATA8_*	ECC Byte lane	ECC Byte lane

The steps to program full leveling are as follows:

1. Unlock the Boot configuration module by writing 0x83E70B13 to the KICK0 and 0x95A4F1E0 to the KICK1 registers.
2. Program the write leveling initial values into the DATA0_PHY_WRLVL_INIT_RATIO to DATA8_PHY_WRLVL_INIT_RATIO fields of the DDR3_CONFIG_2 to DDR3_CONFIG_10 registers respectively. (See the tables in sections Section 4.33 to Section 4.41).

   NOTE: The values to enter into the registers depend on the board topology and the DDR3 clock frequency in use. The DDR3 clock frequency (half the data rate) and trace lengths for each byte lane (CK-DQS pair) should be plugged in the appropriate fields in the accompanying PHY calculation spreadsheet which generates the values to be programmed into the boot config registers mentioned above.

3. Program the gate leveling initial values into the DATA0_PHY_GATELVL_RATIO to DATA8_PHY_GATELVL_RATIO fields of the DDR3_CONFIG_14 to DDR3_CONFIG_22 registers respectively. (See the tables in sections Section 4.43 to Section 4.51.)

   NOTE: The values to enter into the registers depend on the board topology and the DDR3 clock frequency in use. The DDR3 clock frequency (half the data rate) and trace lengths for each byte lane (CK-DQS pair) should be plugged in the appropriate fields in the accompanying PHY calculation spreadsheet which generates the values to be programmed into the boot config registers mentioned above.

4. Program CMD_PHY_DLL_LOCK_DIFF field in DDR3_CONFIG_0 register to 0xF. (See Section 4.31.)
5. Enable global leveling (Set RDWRLVL_EN = 1 in RDWR_LVL_RMP_CTRL).
6. Trigger full leveling (Set RDWRLVLFULL_START = 1 in RDWR_LVL_CTRL).
7. Read back any of the DDR3 controller registers.
   This ensures full leveling is complete because this step is executed only after full leveling completes.

2.13.4.1 Leveling Timeout

The DDR3 controller attempts to converge to the correct leveling values within a reasonable time frame after full leveling is triggered. If a leveling type (write, gate or read data eye) does not converge within the time frame the controller will leave in the unconverged values for each byte lane which will affect DDR3 stability since the de-skew will not be accurate. In such a case, a timeout bit for that leveling will be set in the SDRAM Status Register (WRLVLTO, RDLVLGATETO, and RDLVLTO). The timeouts are global values for all byte lanes that will be set even if one of the byte lanes times out. Plugging in incorrect initial values for a byte lane can typically result in a timeout.

2.13.4.2 Read Data Eye Training Errata For Full Leveling

On certain KeyStone DSPs, the read data eye training has issues converging to the correct values during the full leveling process. See the device-specific Errata document for this and other advisories and usage notes.

2.13.5 Programming Incremental Leveling

This assumes that global leveling is enabled (RDWRLVL_EN=1) and full leveling has already been performed.

2.13.5.1 Standalone Incremental Leveling

Steps to program standalone incremental leveling are:

1. Program RDWRLVLINC_PRE to set the pre-scalar in terms of refresh intervals.
2. Program non-zero values for WRLVLINC_INT, RDLVLGATEINC_INT, and RDLVLINC_INT to decide each of the leveling intervals.
3. Step 2 will trigger incremental leveling. To disable a type of incremental leveling, just program its interval to zero.

2.13.6 Programming Ratio Forced Leveling

The user can disable auto leveling and instead use a set of ratio forced register values present in Section 4.52 and Section 4.53 for devices other than C665x and TCI6612/13/14. These values control the DQ and DQS delay for all byte lanes for write leveling, read DQS gate training and read data eye training. Similar to auto-leveling, these values also depend on board characteristics (trace lengths) and the DDR3 frequency of operation.

For devices other than C665x and TCI6612/13/14, independent control over each byte lane is not possible. A single value needs to be used for all byte lanes. Thus the DQ and DQS skews across byte lanes must be very small. The values to be programmed are WR_DATA_SLAVE_RATIO, WR_DQS_SLAVE_RATIO, RD_DQS_SLAVE_RATIO, and FIFO_WE_SLAVE_RATIO and can be found in the PHY calculation spreadsheet.

For C665x and TCI6612/13/14 devices, independent control is possible over each byte lane through registers DDR3_CONFIG_REG_25 through DDR3_CONFIG_REG_60.

2.13.7 Using Invert Clock Out

For write leveling (both full and incremental) to function correctly, the skew between command and data lines from DSP to an SDRAM should satisfy certain command-to-data skew requirements. The skew is defined as follows:

- $write\_leveling_{skew} = command_{delay} - data_{delay}$.

Both $command_{delay}$ and $data_{delay}$ are measured from the DSP to the SDRAM.

The JEDEC standard parameters tJIT (per, lck) and tWLS defined as the clock period jitter when DLL is locking and write leveling setup time respectively, demand a minimum $write\_leveling_{skew}$ that must be satisfied. The minimum skew is a function of the DDR3 speed bin that is being used. If $write\_leveling_{skew}$ is greater than the minimum skew, CMD_PHY_INVERT_CLKOUT in DDR3_CONFIG_12 register can be left to its default value of 0. If $write\_leveling_{skew}$ is smaller than the minimum required skew, CMD_PHY_INVERT_CLKOUT should be set to 1. This essentially adds a half-clock cycle delay to the $write\_leveling_{skew}$ and thus increases the skew above the minimum skew requirements.

Similar to the minimum skew requirements, there also exists a maximum skew that cannot be exceeded for the write leveling algorithm to function correctly. Maximum skew is also a function of the DDR3 speed bin in use. Both minimum and maximum skews have routing implications for command and data lines. For min/max routing limits with CMD_PHY_INVERT_CLKOUT = 0 or 1, refer to the DDR3 Design Guide (SPRABI1A).

NOTE: When setting CMD_PHY_INVERT_CLKOUT to 1, the CMD_PHY_CTRL_SLAVE_RATIO field in DDR3_CONFIG_0 should be programmed to 0x100. If set to 0, program the default value of 0x80.

NOTE: From the equation, if command lines are shorter than the data lines the resulting skew will be negative. There is a maximum negative skew that the write leveling algorithm can tolerate. For more information refer to the DDR3 Design Guide (SPRABI1A)

2.14 Interrupt Support

The DDR3 memory controller generates one error interrupt. Please check the section on interrupts in the device data manual for details on how the ECC error interrupt is routed. The source of the interrupt can be checked in the Interrupt Raw Status Register.

2.15 EDMA Event Support

The DDR3 memory controller is a DMA slave peripheral and therefore does not generate EDMA events. Data read and write requests may be made directly by masters including the EDMA controller.

2.16 Emulation Considerations

The DDR3 memory controller will remain fully functional during emulation halts to allow emulation access to external memory.

2.17 ECC

For data integrity, the DDR3 memory controller supports ECC on the data written to or read from the ECC protected address ranges in memory. The ECC algorithm is a single-error-correct-double-error-detect (SECDED) algorithm and uses the (72,64) Hamming code. Eight-bit ECC is calculated over 64-bit data quanta. ECC is enabled by setting ECC_EN = 1 in the ECC Control register. ECC is disabled by setting ECC_EN=0. By default, ECC_EN=0. The address ranges can be programmed in the ECC Address Range 1 and 2 register. The system must ensure that any bursts accesses starting in the ECC protected region must not cross over into the unprotected region and vice-versa.

NOTE: The ECC is stored inside the SDRAM during writes. After enabling ECC and before performing any functional reads or writes, all DDR3 memory space configured as ECC should be first written with known data that is 64-bit aligned and multiples of 64-bit. This is to ensure the correct ECC values are stored in the ECC SDRAM prior to functional use.

A write access with byte count that is not a multiple of 64-bit quanta, or with a non-64-bit-aligned address performed within the address range protected by ECC, will result in a write ECC error interrupt. In this case, the DDR3 memory controller writes to the SDRAM. However, the ECC value written to the SDRAM will be corrupted. The controller will NOT trigger a write ECC error if a write access with a multiple of 64-bit quanta and with 64-bit aligned address but with partial byte enables set, is performed within the address range protected by ECC (this can be the case if the Multicore Navigator PktDMA writes to a descriptor placed in DDR3). The data and corrupted ECC value will be written to the SDRAM, but will go undetected and may be detected as 1-bit or 2-bit errors when read back.

If there is a one-bit error, the DDR3 memory controller corrects the data and sends it on the read interface. For 2-bit errors, the DDR3 memory controller generates a read ECC error interrupt. Note that in both cases, the data in SDRAM is still corrupted. It is the responsibility of system software to go and correct the data in the SDRAM.

NOTE: The user should note that the single error correct, double error detect (SECDED) algorithm used by the ECC logic cannot detect more than 2-bit errors per 64-bit quanta. For these errors, the output of the algorithm is unknown i.e. it may erroneously detect as 1-bit, 2-bit or no errors. More than 2-bit errors are expected to be very rare in a well designed system.

See Section 4.27 through Section 4.29 for ECC-related registers.

NOTE: If ECC is disabled, the ECC byte lane is held in reset to save power. Hence, full-leveling must be triggered after enabling ECC to ensure that the ECC byte lane is leveled.

2.18 Power Management

2.18.1 SDRAM Self-Refresh Mode

(See Section 2.8.)

2.18.2 SDRAM Power-Down Mode

The DDR3 memory controller supports power-down mode. Automatic power-down is enabled by setting the LP_MODE field in the Power Management Control register (PMCTL) to 4. The memory is put into power-down after the controller is idle for PD_TIM number of DDR3CLKOUT cycles. In power-down mode, the DDR3 memory controller does not stop the clocks to the memory. The controller maintains DDRCKE low to maintain the power-down state. When the SDRAM is in power-down, the DDR3 memory controller services register accesses as normal.

The memory is brought out of power-down under any of the following conditions:

- If the LP_MODE field is set not equal to 4
- A memory access is requested
- Refresh Must level is reached

2.19 Performance Monitoring

The DDR3 controller provides a set of performance counter registers which can be used to monitor or calculate the bandwidth and efficiency of the DDR traffic. The counters can be configured to count events such as total number of SDAM accesses, SDRAM activates, reads, write and so on. The Performance Counter 1 and 2 Registers (PERF_CNT_1 and PERF_CNT_2) act as two 32-bit counters that are able to count events independent of each other. To provide more granularity the counters can also be configured to filter events originating from a particular master or address space. The events to be counted and filter enabled are programmed in the Performance Counter Config Register (PERF_CNT_CFG). The actual value of the filter is programmed in Performance Counter Master Region Select Register (PERF_CNT_SEL). The counters start counting the events independently when commands enter the Command FIFO.

The CNTRN_CFG (N=1,2) fields in the PERF_CNT_CFG register are used to select the event for the counter to count. The PERF_CNT_CFG also includes options to enable or disable the master (CNTRN_MSTID_EN) and address space (CNTRN_REGION_EN) filters for each counter. The filters are disabled by default. If the respective filters are enabled, the master ID value and region select options can be programmed in the PERF_CNT_SEL register. It should be noted that the master ID and region select filters apply only to a certain subset of events that can be counted. The table below shows the events for which the filters are applicable.

Table 2-17. Performance Counter Filter Configuration

PERF_CNT_CFG. [CNTR_CFG]	Event Selected for counting	PERF_CNT_CFG. [CTNR_REGION_EN]	PERF_CNT_CFG. [CNTR_MSTID_EN]
0x0	Total SDRAM accesses	NA	0 - Disable, 1 - Enable
0x1	Total SDRAM activates	NA	0 - Disable, 1 - Enable
0x2	Total Reads	0 - Disable, 1 - Enable	0 - Disable, 1 - Enable
0x3	Total Writes	0 - Disable, 1 - Enable	0 - Disable, 1 - Enable
0x4	Number of DDR/2 clock cycles Command FIFO is full	NA	NA
0x5	Number of DDR/2 clock cycles Write Data FIFO is full	NA	NA
0x6	Number of DDR/2 clock cycles Read Data FIFO is full	NA	NA
0x7	Number of DDR/2 clock cycles Write Status FIFO is full	NA	NA
0x8	Number of priority elevations	0 - Disable, 1 - Enable	0 - Disable, 1 - Enable
0x9	Number of DDR/2 clock cycles that a command was pending	NA	NA
0xA	Number of DDR/2 clock cycles for which DDR i/f was transferring data	NA	NA
0xB	Total number of 1-bit ECC errors	NA	NA
0x C - 0XF	Reserved		

See Chapter 4 for details on Performance counter registers.

Using the DDR3 Memory Controller

The following sections show various ways to connect the DDR3 memory controller to DDR3 memory devices. The steps required to configure the DDR3 memory controller for external memory access are also described.

Topic **Page**

3.1 Connecting the DDR3 Memory Controller to DDR3 SDRAM

The following figures show high-level views of the three memory topologies:

- Figure 3-1
- Figure 3-2
- Figure 3-3

All DDR3 SDRAM devices must comply with the JESD79-3C standard.

Not all of the memory topologies shown may be supported by your device. For more information, see the device-specific data manual.

The printed-circuit-board (PCB) layout rules and connection requirements between the DSP and the memory device are described in a separate document. For more information, see the device-specific data manual.

Figure 3-1. Connecting Two 16 MB x 16 x 8 Banks (4Gb Total) Devices

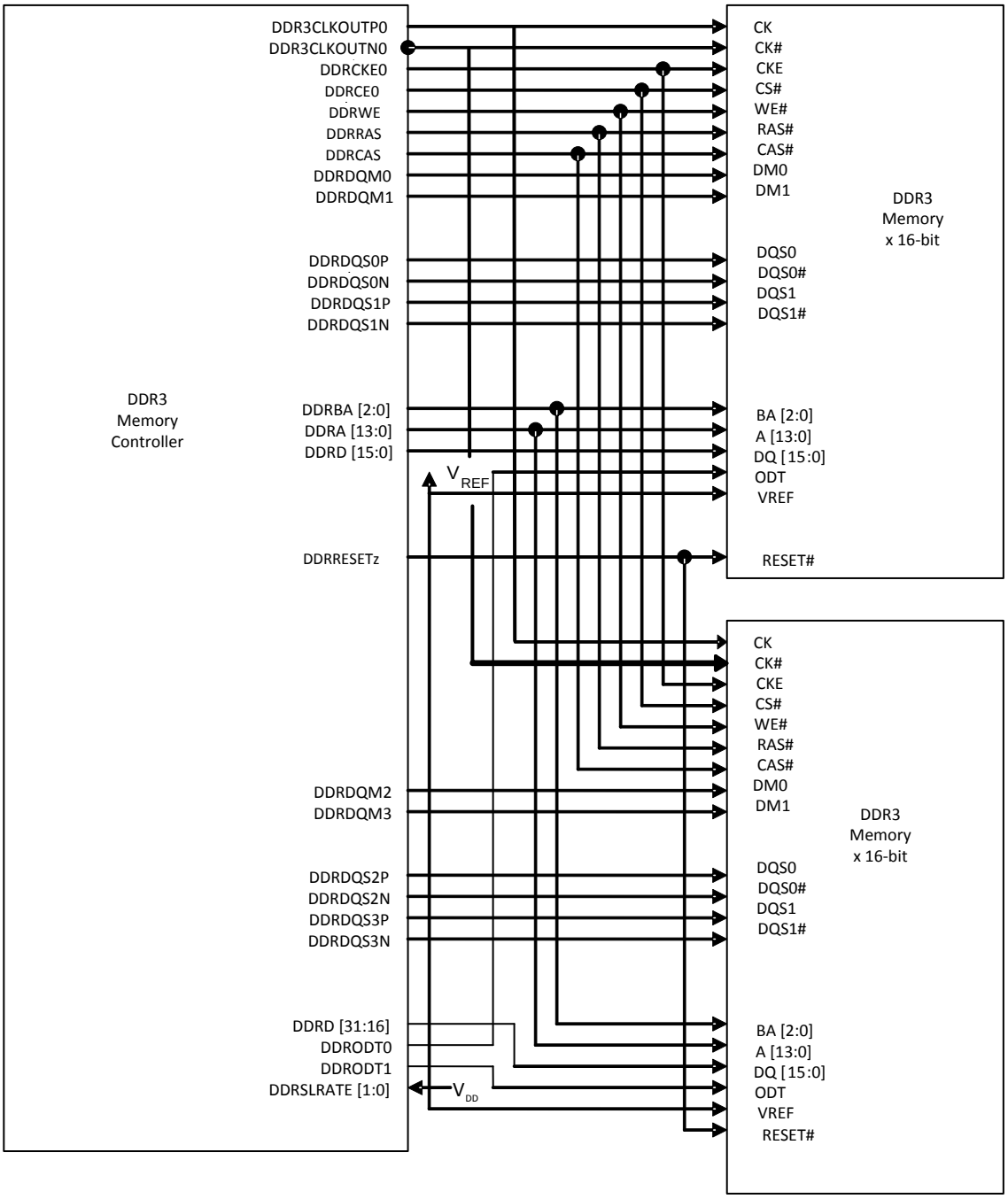


Figure 3-2. Connecting One 8 MB x 16 x 8 Banks (1Gb Total) Device

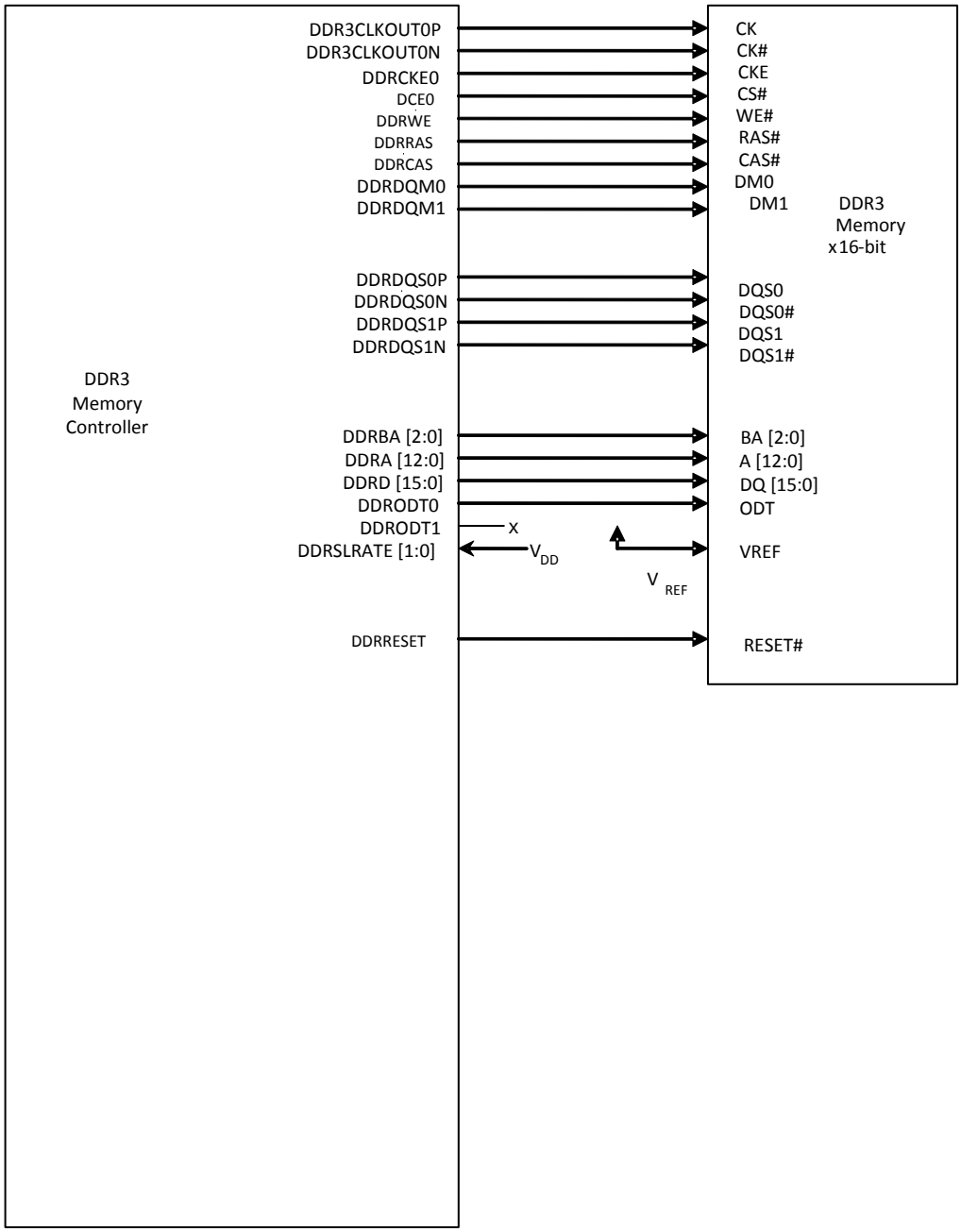
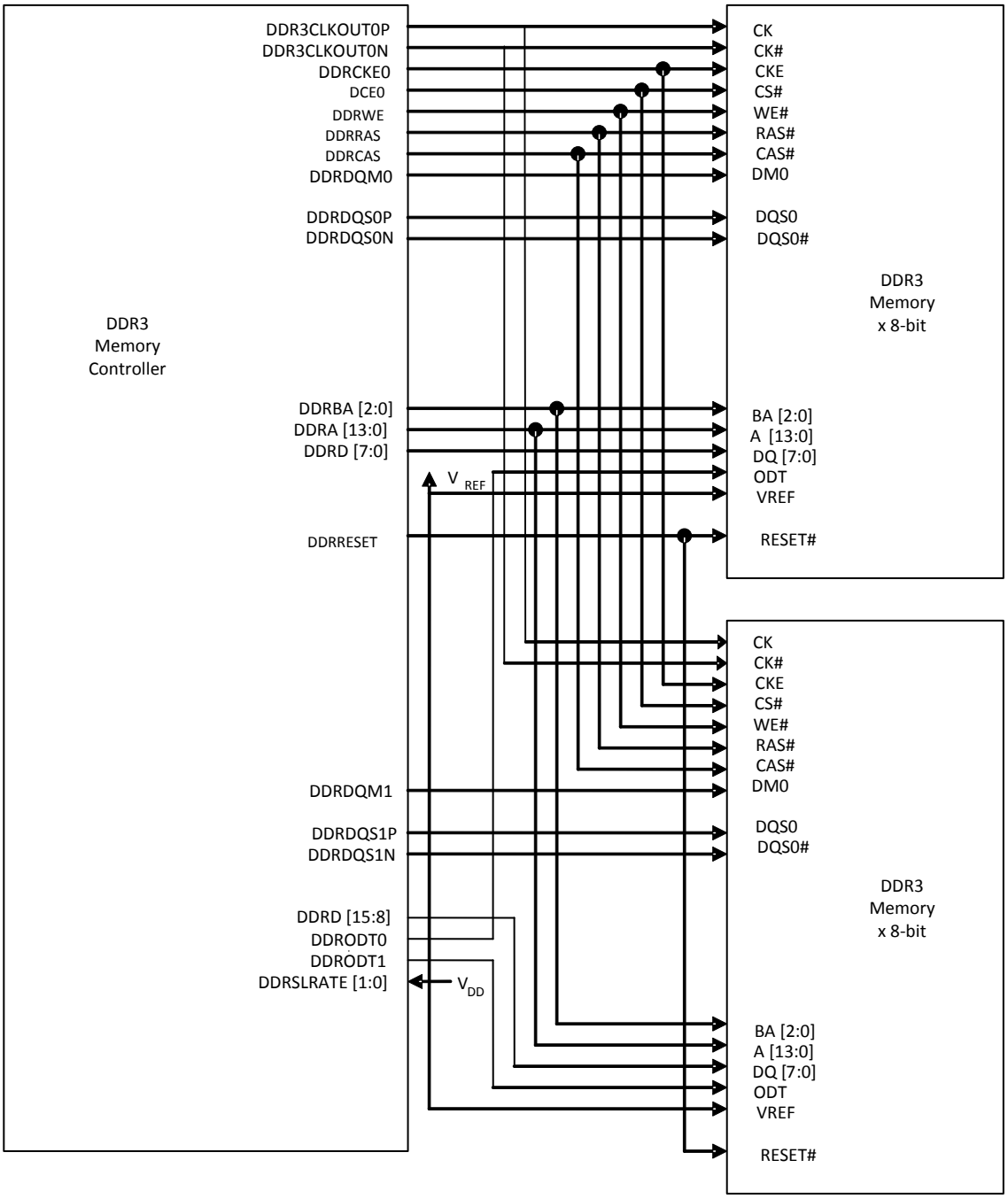


Figure 3-3. Connecting Two 16 MB x 8 x 8 Banks (2Gb Total) Devices



3.2 Configuring DDR3 Memory Controller Registers to Meet DDR3 SDRAM Specifications

The DDR3 memory controller allows a high degree of programmability for shaping DDR3 accesses. This provides the DDR3 memory controller with the flexibility to interface with a variety of DDR3 devices. By programming the SDRAM Configuration Register (SDCFG), SDRAM Refresh Control Register (SDRFC), SDRAM Timing 1 Register (SDTIM1), SDRAM Timing 2 Register (SDTIM2) and SDRAM Timing 3 Register (SDTIM3), the DDR3 memory controller can be configured to meet the data sheet specification for JESD79-3C compliant DDR3 SDRAM devices.

As an example, the following sections describe how to configure each of these registers for access to two 1 Gb, 16-bit wide DDR3 SDRAM devices connected as shown on Figure 3-2, where each device has the following configuration:

- Maximum data rate: 1333 MHz
- Number of banks: 8
- Page size: 1024 words
- CAS latency: 9

It is assumed that the frequency of the DDR3 memory controller clock (DDR3CLKOUT) is set to 666.5 MHz.

3.2.1 Programming the SDRAM Configuration Register (SDCFG)

The SDRAM configuration register (SDCFG) contains register fields that configure the DDR3 memory controller to match the data bus width, CAS latency, number of banks, and page size of the attached DDR3 memory.

Table 3-1 shows the resulting SDCFG configuration.

Table 3-1. SDCFG Configuration

Field	Value	Function Selection
SDRAM_TYPE	0x3h	SDRAM Type Select – DDR3
NM	1h	To configure the DDR3 memory controller for a 32-bit data bus width.
CL	10h	To select a CAS latency of 9.
IBANK	3h	To select 8 internal DDR3 banks.
EBANK	0	To select only DCE0z to be used.
PAGESIZE	2h	To select 1024-word page size.

3.2.2 Programming the SDRAM Refresh Control Register (SDRFC)

The SDRAM refresh control register (SDRFC) configures the DDR3 memory controller to meet the refresh requirements of the attached DDR3 device. SDRFC also allows the DDR3 memory controller to enter and exit self refresh.

The REFRESH_RATE field in SDRFC is defined as the rate at which the attached DDR3 device is refreshed in DDR3 cycles. The value of this field may be calculated using the following equation:

REFRESH_RATE = DDR3CLKOUT frequency × memory refresh period (1)

According to the DDR3 JEDEC standard, on reset de-assertion the DDRCKE pin must remain low for at least 500µs before becoming active during power-up initialization. This is achieved by programming a 500 µs refresh period in the SDRFC prior to initialization.

Table 3-2 shows the DDR3-1333 refresh rate specification.

Table 3-2. DDR3 Memory Refresh Specification

Symbol	Description	Value
t_{REFI}	Refresh interval to be programmed during power-up initialization	500 µs
t_{REFI}	Average Periodic Refresh Interval (after power-up initialization)	7.8 µs

The refresh rate of 500 µs to be programmed during power-up initialization should be calculated equal to a divide-by-16 value as follows. The DDR3 controller takes care of the divide-by-16 internal logic.

REFRESH_RATE = (666.5 MHz × 500 µs)/16 = 515Ch (2)

After power-up initialization, the refresh rate of 7.8 µs should be programmed as follows:

REFRESH_RATE = 666.5 MHz × 7.8 µs = 1450h (3)

Table 3-3 shows the resulting SDRFC configuration.

Table 3-3. SDRFC Configuration

Field	Value	Function Selection
SRT	0	Normal Operating Temperature Range
ASR	0	Manual Self-Refresh
REFRESH_RATE	515Ch 1450h	Set a divide-by-16 equivalent of 500 µs during power-up initialization. Set to 1450h DDR3 clock cycles to meet the DDR3 memory refresh rate requirement during normal opertion.

3.2.3 Configuring SDRAM Timing Registers (SDTIM1, SDTIM2, SDTIM3, SDTIM4)

The SDRAM timing 1 register (SDTIM1), SDRAM timing 2 register (SDTIM2), SDRAM timing 3 register (SDTIM3), SDRAM timing 4 register (SDTIM4) configure the DDR3 memory controller to meet the datasheet timing parameters of the attached DDR3 device. Each field in SDTIM1, SDTIM2, SDTIM3, SDTIM4 corresponds to a timing parameter in the DDR3 datasheet specification. Table 3-4, Table 3-5, and Table 3-6 show the register field name and corresponding DDR3 datasheet parameter name and value. These tables also provide a formula to calculate the register field value and show the resulting calculation. Each of the equations includes a minus 1 because the register fields are defined in terms of DDR3 clock cycles minus 1. (See Section 4.5- Section 4.7 for more information.). Some of these timing parameters will also have to be programmed in the DRAM Timing Parameter Registers (See Section 4.50 - Section 4.52)

The objective behind programming the timing values is to calculate them in terms of DRAM clock cycles and round off to the next highest integer value. For example, at 666.5 MHz, the clock period t_{CK} = 1.5 ns. So 13.5 ns will be programmed as (13.5/1.5)-1= 9 - 1 = 8 DDR3 clock cycles and 14ns will be 9 DDR3 clock cycles.

Table 3-4. See the register section for the SDTIM* register where the field exists

Register Field Name	DDR3 SDRAM Datasheet Parameter Name	Description	Datasheet Value (ns)	Formula (Register Field must be >=)	Field Value (h)
T_RP	t_{RP}	Precharge to Activate or Refresh command	13.5	(t_{RP}/t_{CK}) – 1	8
T_RCD	t_{RCD}	Activate command to Read/Write command	13.5	(t_{RCD}/t_{CK}) – 1	8
T_WR	t_{WR}	Write recovery time	6	(t_{WR}/t_{CK}) – 1	3
T_RAS	t_{RAS}	Active to precharge command	36	(t_{RAS}/t_{CK}) – 1	17
T_RC	t_{RC}	Activate to Activate command in same bank	49.5	(t_{RC}/t_{CK}) – 1	20
T_RRD	t_{RRD}	Activate to Activate in different bank	t_{FAW} = 30ns	($t_{FAW}/(4*t_{CK})$) – 1	4
T_WTR	t_{WTR}	Write to Read command delay	6	(t_{WTR}/t_{CK}) – 1	3

Table 3-5. See the register section for the SDTIM* register where the field exists

Register Field Name	DDR3 SDRAM Datasheet Parameter Name	Description	Datasheet Value (ns)	Formula (Register Field must be >=)	Field Value (h)
T_RTP	t_{RTP}	Read to precharge command delay	6	(t_{RTP}/t_{CK}) – 1	3
T_CKE	t_{CKE}	CKE minimum pulse width	3(t_{CK} cycles)	(t_{CKE}) – 1	2
T_XP	t_{XP}	Power-down exit to non-read command	5(t_{CK} cycles)	(t_{XP}) – 1	4

Table 3-6. See the register section for the SDTIM* register where the field exists

Register Field Name	DDR3 SDRAM Datasheet Parameter Name	Description	Datasheet Value (ns)	Formula (Register Field must be >=)	Field Value (h)
T_CSTA	DDR controller parameter	Refer to SDTIM 34 Register	—	—	5
T_RFC	t_{RFC}	Refresh cycle time	110	(t_{RFC}/t_{CK}) –1	49
T_ZQCS	t_{ZQcs}	ZQCS command time	64(t_{CK} cycles)	(t_{ZQcs}) –1	3F

3.2.4 Configuring Leveling Registers

The PHY registers in the Boot configuration section should be programmed according to the instructions in Section 2.13. Full leveling can be enabled by writing a 1 to bit 31 of the RDWR_LVL_RMP_CTRL register and then triggered by writing a 1 to bit 31 of the RDWR_LVL_CTRL register . For forced ratio leveling, program DDR3_CONFIG_23 and DDR3_CONFIG_24 with the effective slave ratio values for devices other than C665x or TCI6612/13/14. For C665x and TCI6612/13/14, program DDR3_CONFIG_REG_25 through DDR3_CONFIG_REG_60 with the effective slave ratio values.

3.2.5 Configuring Read Latency

The read latency can be programmed in the DDR PHY Control 1 Register [4:0]. Read latency can be programmed from a minimum of CAS latency +1 to CAS latency +7. The value programmed should be the required value minus one.

DDR3 Memory Controller Registers

Table 4-1 lists the memory-mapped registers for the DDR3 memory controller. For the memory address of these registers, see the device-specific data manual.

Table 4-1. DDR3 Memory Controller Registers (See datasheet memory map for base address)

Offset	Acronym	Register Description	Section
000h	MIDR	Module ID and Revision Register	Section 4.1
004h	STATUS	DDR3 Memory Controller Status Register	Section 4.2
008h	SDCFG	SDRAM Configuration Register	Section 4.3
010h	SDRFC	SDRAM Refresh Control Register	Section 4.4
018h	SDTIM1	SDRAM Timing 1 Register	Section 4.5
020h	SDTIM2	SDRAM Timing 2 Register	Section 4.6
028h	SDTIM3	SDRAM Timing 3 Register	Section 4.7
038h	PMCTL	Power Management Control Register	Section 4.8
0x54h	LAT_CONFIG	VBUSM Configuration Register	Section 4.9
0x80	PERF_CNT_1	Performance Counter 1 Register	Section 4.10
0x84	PERF_CNT_2	Performance Counter 2 Register	Section 4.11
0x88	PERF_CNT_CFG	Performance Counter Config Register	Section 4.12
0x8C	PERF_CNT_SEL	Performance Counter Master Region Select Register	Section 4.13
0x90	PERF_CNT_TIM	Performance Counter Time Register	Section 4.14
0A4h	IRQSTATUS_RAW_SYS	Interrupt Raw Status Register	Section 4.15
0ACh	IRQ_STATUS_SYS	Interrupt Status Register	Section 4.16
0B4h	IRQENABLE_SET_SYS	Interrupt Enable Set Register	Section 4.17
0BCh	IRQENABLE_CLR_SYS	Interrupt Enable Clear Register	Section 4.18
0C8h	ZQCONFIG	SDRAM Output Impedance Calibration Configuration Register	Section 4.19
0D4h	RDWR_LVL_RMP_WIN	Read-Write Leveling Ramp Window Register	Section 4.20
0D8h	RDWR_LVL_RMP_CTRL	Read-Write Leveling Ramp Control Register	Section 4.21
0DCh	RDWR_LVL_CTRL	Read-Write Leveling Control Register	Section 4.22
0E4h	DDR_PHY_CTRL_1	DDR PHY Control 1 Register	Section 4.23
100h	PRI_COS_MAP	Priority To Class-Of-Service Mapping Register	Section 4.24
104h	MSTID_COS_1_MAP	Master ID to Class-Of-Service 1 Mapping Register	Section 4.25
108h	MSTID_COS_2_MAP	Master ID to Class-Of-Service 2 Mapping Register	Section 4.26
110h	ECCCTL	ECC Control Register	Section 4.27
114h	ECCADDR1	ECC Address Range 1 Register	Section 4.28
118h	ECCADDR2	ECC Address Range 2 Register	Section 4.29
120h	RWTHRESH	Read Write Execution Threshold Register	Section 4.30

Table 4-2. DDR3 PHY Leveling Registers (See device datasheet for base address)

Offset	Acronym	Register Description	Section
404h	DDR3_CONFIG_0	DDR3 Configuration 0 Register	Section 4.31
408h	DDR3_CONFIG_1	DDR3 Configuration 1 Register	Section 4.32
40Ch	DDR3_CONFIG_2	DDR3 Configuration 2 Register	Section 4.33
410h	DDR3_CONFIG_3	DDR3 Configuration 3 Register	Section 4.34
414h	DDR3_CONFIG_4	DDR3 Configuration 4 Register	Section 4.35
418h	DDR3_CONFIG_5	DDR3 Configuration 5 Register	Section 4.36
41Ch	DDR3_CONFIG_6	DDR3 Configuration 6 Register	Section 4.37
420h	DDR3_CONFIG_7	DDR3 Configuration 7 Register	Section 4.38
424h	DDR3_CONFIG_8	DDR3 Configuration 8 Register	Section 4.39
428h	DDR3_CONFIG_9	DDR3 Configuration 9 Register	Section 4.40
42Ch	DDR3_CONFIG_10	DDR3 Configuration 10 Register	Section 4.41
434h	DDR3_CONFIG_12	DDR3 Configuration 12 Register	Section 4.42
43Ch	DDR3_CONFIG_14	DDR3 Configuration 14 Register	Section 4.43
440h	DDR3_CONFIG_15	DDR3 Configuration 15 Register	Section 4.44
444h	DDR3_CONFIG_16	DDR3 Configuration 16 Register	Section 4.45
448h	DDR3_CONFIG_17	DDR3 Configuration 17 Register	Section 4.46
44Ch	DDR3_CONFIG_18	DDR3 Configuration 18 Register	Section 4.47
450h	DDR3_CONFIG_19	DDR3 Configuration 19 Register	Section 4.48
454h	DDR3_CONFIG_20	DDR3 Configuration 20 Register	Section 4.49
458h	DDR3_CONFIG_21	DDR3 Configuration 21 Register	Section 4.50
45Ch	DDR3_CONFIG_22	DDR3 Configuration 22 Register	Section 4.51
460h	DDR3_CONFIG_23 (NA for TCI6612/13/14 and C665x devices)	DDR3 Configuration 23 Register	Section 4.52
464h	DDR3_CONFIG_24 (NA for TCI6612/13/14 and C665x devices)	DDR3 Configuration 24 Register	Section 4.53
The following registers are applicable only for C665x and TCI6612/13/14 (Reserved for all other devices). Registers that say 'TCI6612/13/14 only' do not apply to C665x devices.			
468h	DDR3_CONFIG_REG_25	DDR3 Configuration 25 Register	Section 4.54
46Ch	DDR3_CONFIG_REG_26	DDR3 Configuration 26 Register	Section 4.55
470h	DDR3_CONFIG_REG_27	DDR3 Configuration 27 Register	Section 4.56
474h	DDR3_CONFIG_REG_28	DDR3 Configuration 28 Register	Section 4.57
478h	DDR3_CONFIG_REG_29 (TCI6612/13/14 only)	DDR3 Configuration 29 Register	Section 4.58
47Ch	DDR3_CONFIG_REG_30 (TCI6612/13/14 only)	DDR3 Configuration 30 Register	Section 4.59
480h	DDR3_CONFIG_REG_31 (TCI6612/13/14 only)	DDR3 Configuration 31 Register	Section 4.60
484h	DDR3_CONFIG_REG_32 (TCI6612/13/14 only)	DDR3 Configuration 32 Register	Section 4.61
488h	DDR3_CONFIG_REG_33	DDR3 Configuration 33 Register	Section 4.62
48Ch	DDR3_CONFIG_REG_34	DDR3 Configuration 34 Register	Section 4.63
490h	DDR3_CONFIG_REG_35	DDR3 Configuration 35 Register	Section 4.64
494h	DDR3_CONFIG_REG_36	DDR3 Configuration 36 Register	Section 4.65
498h	DDR3_CONFIG_REG_37	DDR3 Configuration 37 Register	Section 4.66
49Ch	DDR3_CONFIG_REG_38 (TCI6612/13/14 only)	DDR3 Configuration 38 Register	Section 4.67
4A0h	DDR3_CONFIG_REG_39 (TCI6612/13/14 only)	DDR3 Configuration 39 Register	Section 4.68
4A4h	DDR3_CONFIG_REG_40 (TCI6612/13/14 only)	DDR3 Configuration 40 Register	Section 4.69
4A8h	DDR3_CONFIG_REG_41 (TCI6612/13/14 only)	DDR3 Configuration 41 Register	Section 4.70
4ACh	DDR3_CONFIG_REG_42	DDR3 Configuration 42 Register	Section 4.71
4B0h	DDR3_CONFIG_REG_43	DDR3 Configuration 43 Register	Section 4.72
4B4h	DDR3_CONFIG_REG_44	DDR3 Configuration 44 Register	Section 4.73
4B8h	DDR3_CONFIG_REG_45	DDR3 Configuration 45 Register	Section 4.74
4BCh	DDR3_CONFIG_REG_46	DDR3 Configuration 46 Register	Section 4.75

Table 4-2. DDR3 PHY Leveling Registers (See device datasheet for base address) (continued)

Offset	Acronym	Register Description	Section
4C0h	DDR3_CONFIG_REG_47 (TCI6612/13/14 only)	DDR3 Configuration 47 Register	Section 4.76
4C4h	DDR3_CONFIG_REG_48 (TCI6612/13/14 only)	DDR3 Configuration 48 Register	Section 4.77
4C8h	DDR3_CONFIG_REG_49 (TCI6612/13/14 only)	DDR3 Configuration 49 Register	Section 4.78
4CCh	DDR3_CONFIG_REG_50 (TCI6612/13/14 only)	DDR3 Configuration 50 Register	Section 4.79
4D0h	DDR3_CONFIG_REG_51	DDR3 Configuration 51 Register	Section 4.80
4D4h	DDR3_CONFIG_REG_52	DDR3 Configuration 52 Register	Section 4.81
4D8h	DDR3_CONFIG_REG_53	DDR3 Configuration 53 Register	Section 4.82
4DCh	DDR3_CONFIG_REG_54	DDR3 Configuration 54 Register	Section 4.83
4E0h	DDR3_CONFIG_REG_55	DDR3 Configuration 55 Register	Section 4.84
4E4h	DDR3_CONFIG_REG_56 (TCI6612/13/14 only)	DDR3 Configuration 56 Register	Section 4.85
4E8h	DDR3_CONFIG_REG_57 (TCI6612/13/14 only)	DDR3 Configuration 57 Register	Section 4.86
4ECh	DDR3_CONFIG_REG_58 (TCI6612/13/14 only)	DDR3 Configuration 58 Register	Section 4.87
4F0h	DDR3_CONFIG_REG_59 (TCI6612/13/14 only)	DDR3 Configuration 59 Register	Section 4.88
4F4h	DDR3_CONFIG_REG_60	DDR3 Configuration 60 Register	Section 4.89

4.1 Module ID and Revision Register (MIDR)

The Module ID and Revision register contains the revision number and identification data of the DDR3 peripheral, and is described in the following figure and table.

Figure 4-1. Module ID and Revision Register (MIDR)

31 28	27 16	15 8	7 6	5 0
Reserved	MOD_ID	MJ_REV	Reserved	MIN_REV
R=0x4	R=0x46	R=0x4	R=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-3. Module ID and Revision Register (MIDR) Field Descriptions

Bit	Field	Attribute	Description
31-28	Reserved	R	Value = 0x4 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
27-16	MOD_ID	R	Value = 0x46 Module ID Bits
15-8	MJ_REV	R	Value = 0x4 Major Revision
7-6	Reserved	R	Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
5-0	MIN_REV	R	Value = 0x0 Minor Revision

4.2 DDR3 Memory Controller Status Register (STATUS)

This register contains the status of the DDR3 module and is described in the following figure and table.

Figure 4-2. DDR3 Memory Controller Status Register (STATUS)

31	30 7	6	5	4	3	2	1 0
BE	Reserved	RDLVGATETO	RDLVLTO	WRLVLTO	Reserved	IFRDY	Reserved
R=0	R=0	R=0	R=0	R=0	R=0	R=0	R=0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-4. DDR3 Memory Controller Status Register (STATUS) Field Descriptions

Bit	Field	Attribute	Description
31	BE	R	Big Endian. Reflects the value on the BIG_ENDIAN port that defines whether the EMIF is in big or little-endian mode
30	Reserved	R	Value = 0 This field is tied off to 0x1.
29-7	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
6	RDLVGATETO	R	Read DQS Gate Training Timeout • 0 = Reset value • 1 = Indicates read DQS gate training has timed out
5	RDLVLTO	R	Read Data Eye Training Timeout • 0 = Reset value • 1 = Read data eye training has timed out
4	WRLVLTO	R	Write Leveling Timeout • 0 = Reset value • 1 = Write Leveling has timed out
3	Reserved	R	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
2	IFRDY	R	DDR3 memory controller interface logic ready bit. The interface logic controls the signals used to communicate with DDR3 SDRAM devices. This bit displays the status of the interface logic. • 0 = Interface logic is not ready; either powered down, not ready, or not locked. • 1 = Interface logic is powered up, locked and ready for operation.
1-0	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.

4.3 SDRAM Configuration Register (SDCFG)

The SDRAM Configuration Register (SDCFG) contains field that program the DDR3 memory controller to meet the specifications of the DDR3 memory. These fields configure the DDR3 memory controller to match the data bus width, CAS latency, number of internal banks, and page size of the external DDR3 memory. For more information on initializing the configuration registers of the DDR3 memory controller, see Section 3.2.

Figure 4-3. SDRAM Configuration Register (SDCFG)

31–29	28–27	26–24	23	22–21	20	19–18
SDRAM_TYPE	IBANK_POS	DDR_TERM	Reserved	DYN_ODT	DDR_DISABLE_DLL	SDRAM_DRIVE
RW=0x0	RW=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0	RW=0x0

17–16	15–14	13–10	9–7	6–4	3	2–0
CWL	NM	CL	ROWSIZE	IBANK	EBANK	PAGESIZE
RW=0x0	RW=0x0	RW=0x2	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-5. SDRAM Configuration Register (SDCFG) Field Descriptions

Bit	Field	Attribute	Description
31-29	SDRAM_TYPE	RW	Value = 3 SDRAM type selection. Set to 3 for DDR3. All other values reserved.
28-27	IBANK_POS	RW	Internal bank position. • 0 = Assigns internal bank address bits from address as shown in Table 2-5 • 1,2,3 = Assign internal bank address bits from address as shown in Table 2-6
26-24	DDR_TERM	RW	Defines termination resistor value. • 0 = Disables termination • 1 = RZQ/4 • 2 = RZQ/2 • 3 = RZQ/6 • 4 = RZQ/12 • 5 = RZQ/8
23	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
22-21	DYN_ODT	RW	Dynamic On-Die Termination • 0 = Turn off dynamic ODT. • 1 = RZQ/4 • 2 = RZQ/2 All other values reserved.
20	DDR_DISABLE_DLL	RW	Disable DLL select. • 0 = Normal Operation. • 1 = Disables DLL inside SDRAM.
19-18	SDRAM_DRIVE	RW	SDRAM drive strength. • 0 = RZQ/6 • 1 = RZQ/7 All other values reserved.
17-16	CWL	RW	CAS Write Latency. Lower value gives better performance. • 0 = CAS write latency of 5 • 1 = CAS write latency of 6 • 2 = CAS write latency of 7 • 3 = CAS write latency of 8

Table 4-5. SDRAM Configuration Register (SDCFG) Field Descriptions (continued)

Bit	Field	Attribute	Description
15-14	NM	RW	DDR3 data bus width. A write to this bit field will cause the memory controller to start SDRAM initialization sequence. • 0 = 64-bit bus width. • 1 = 32-bit bus width. • 2 = 16-bit bus width. All other values reserved.
13-10	CL	RW	CAS Latency. The value of this field defines the CAS latency, to be used when accessing connected SDRAM devices. A write to this field will cause the DDR3 memory controller to start the SDRAM initialization sequence. • 2 = CAS latency of 5. • 4 = CAS latency of 6. • 6 = CAS latency of 7. • 8 = CAS latency of 8. • 10 = CAS latency of 9. • 12 = CAS latency of 10. • 14 = CAS latency of 11. All other values are reserved.
9-7	ROWSIZE	RW	Row size. Defines the number of row address bits of connected SDRAM devices • 0 = 9 row bits. • 1 = 10 row bits. • 2 = 11 row bits. • 3 = 12 row bits. • 4 = 13 row bits. • 5 = 14 row bits. • 6 = 15 row bits. • 7 = 16 row bits.
6- 4	IBANK	RW	Internal SDRAM bank setup bits. Defines number of banks inside connected SDRAM devices. A write to this bit will cause the DDR3 memory controller to start SDRAM initialization sequence. Values 4-7 are reserved for this field. A word is equal to the bus width of the individual SDRAM devices used (example, 1 byte for x8 and 2bytes for x16 devices) • 0 = One bank SDRAM devices. • 1 = Two bank SDRAM devices. • 2 = Four bank SDRAM devices. • 3 = Eight bank SDRAM devices.
3	EBANK	RW	External chip select setup. Defines whether SDRAM accesses use 1 or 2 chip select lines as follows: • 0 = Use DCE0# for all SDRAM accesses. • 1 = Use DEC0# and DCE1# for SDRAM accesses.
2 -0	PAGESIZE	RW	Page size bits. Defines internal page size of the external DDR3 memory. A write to this bit will cause the DDR3 memory controller to start the SDRAM initialization sequence. Values 4-7 are reserved for this field. A word is equal to the bus width of the individual SDRAM devices used (example, 1 byte for x8 and 2bytes for x16 devices) • 0 = 256-word page requiring 8 column address bits. • 1 = 512-word page requiring 9 column address bits. • 2 = 1024-word page requiring 10 column address bits. • 3 = 2048-word page requiring 11 column address bits.

4.4 SDRAM Refresh Control Register (SDRFC)

The SDRAM Refresh Control Register (SDRFC) is used to configure the DDR3 memory controller to:

- Enter and Exit the self-refresh state.
- Meet the refresh requirements of the attached DDR3 device by programming a rate at which the DDR3 memory controller issues autorefresh commands.

The SDRFC register is described in the following figure and table.

Figure 4-4. SDRAM Refresh Control Register (SDRFC)

31	30	29	28	27	26 24	23 16	15 0
INITREF_DIS	Reserved	SRT	ASR	Reserved	PASR	Reserved	REFRESH _RATE
RW=0x1	R=0x0	RW=0x0	RW=0x0	R=0x0	RW=0x0	R=0x0	RW=0x61A8

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-6. SDRAM Refresh Control (SDRFC) Register Field Descriptions

Bit	Field	Attribute	Description
31	INITREF_DIS	RW	Initialization and Refresh Disable. • 0 = Normal operation • 1 = Disables SDRAM initialization and refreshes, but carries out SDRAM write/read transactions
30	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
29	SRT	RW	DDR3 self-refresh temperature range. A write to this bit will cause the DDR3 memory controller to start SDRAM initialization sequence. • 0 = Normal operating temperature range. This must be set to zero if ASR bit is set to 1. • 1 = Extended operating temperature range when ASR bit is set to zero.
28	ASR	RW	A write to this bit will cause the DDR3 memory controller to start SDRAM initialization sequence. • 0 = Use manual self-refresh • 1 = Auto self-refresh enable
27	Reserved	R	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
26-24	PASR	RW	Partial Array self-refresh. These bits get loaded into the extended mode register during initialization. A write to this bit will cause the DDR3 memory controller to start SDRAM initialization sequence. • 0 = Full-array. • 1 or 5 = ½ array. • 2 or 6 = ¼ array. • 3 or 7 = 1/8 array. • 4 = ¾ array.
23-16	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
15-0	REFRESH_RATE	RW	The value in this field is used to define the rate at which connected SDRAM devices will be refreshed. REFRESH_RATE = Refresh period * DDR3 clock frequency.

4.5 SDRAM Timing 1 (SDTIM1) Register

SDRAM Timing 1 register (SDTIM1) configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. Note that DDR3CLKOUT is equal to the period of the DDR3CLKOUT signal. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM1 register is described in the following figure and table.

Figure 4-5. SDRAM Timing 1 (SDTIM1) Register

31 29	28 25	24 21	20 17	16 12	11 6	5 3	2 0
Reserved	T_RP	T_RCD	T_WR	T_RAS	T_RC	T_RRD	T_WTR
R=0x0	RW=0xA	RW=0xA	RW=0xB	RW=0x1B	RW=0x26	RW=0x5	RW=0x4

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-7. SDRAM Timing 1 (SDTIM1) Register Field Descriptions

Bit	Field	Attribute	Description
31- 29	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
28-25	T_RP	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a precharge command to a refresh or activate command, minus 1. The value of this parameter can be derived from the t_{RP} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RP = (t_{RP}/t_{CK}) - 1$
24-21	T_RCD	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to a read or write command, minus 1. The value of this parameter can be derived from the t_{RCD} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RCD = (t_{RCD}/t_{CK}) - 1$
20-17	T_WR	RW	These bits specify the minimum number of DDR3CLKOUT cycles from the last write transfer to a precharge command, minus 1. The value of this parameter can be derived from the t_{WR} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_WR = (t_{WR}/t_{CK}) - 1$
16-12	T_RAS	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to precharge command, minus 1. The value of this parameter can be derived from the minimum value of the t_{RAS} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RAS = (t_{RAS}/t_{CK}) - 1$
11-6	T_RC	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate command to an activate command, minus 1. The value of this parameter can be derived from the t_{RC}AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RC = (t_{RC}/t_{CK}) - 1$
5-3	T_RRD	RW	These bits specify the minimum number of DDR3CLKOUT cycles from an activate to an activate in a different bank, minus 1. The value of this parameter can be derived from the t_{FAW} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_RRD = (t_{FAW}/(4*t_{CK})) - 1$
2-0	T_WTR	RW	These bits specify the minimum number of DDR3CLKOUT cycles from the last write to a read command, minus 1. The value of this parameter can be derived from the t_{WTR} AC timing parameter in the DDR3 memory data sheet. Convert the t_{WTR} value from the memory datasheet into ns before using the formula below. Calculate using the formula: $T\_WTR = (t_{WTR}/t_{CK}) - 1$

4.6 SDRAM Timing 2 (SDTIM2) Register

Like the SDRAM Timing 1 register (SDTIM1), the SDRAM Timing 2 register (SDTIM2) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM2 register is described in the following figure and table.

Figure 4-6. SDRAM Timing 2 (SDTIM2) Register

31	30 28	27 25	24 16	15 6	5 3	2 0
Reserved	T_XP	Reserved	T_XSNR	T_XSRD	T_RTP	T_CKE
R=0x0	RW=0x6	R=0x7	RW=0x5F	RW=0x1FF	RW=0x5	RW=0x5

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-8. SDRAM Timing 2 (SDTIM2) Register Field Descriptions

Bit	Field	Attribute	Description
31	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
30-28	T_XP	RW	These bits specify the minimum number of DDR3CLKOUT cycles from Power down exit to any command other than a read command, minus 1. The value of this parameter can be derived from the t_{XP} AC timing parameter in the DDR3 memory data sheet. Convert the t_{XP} datasheet parameter value into ns before using formula below. Calculate using the formula: $T\_XP = (t_{XP}/t_{CK}) - 1$
27-25	Reserved	R	Reserved. A value written to this field has no effect.
24-16	T_XSNR	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a self-refresh exit to a command that does not require a locked DLL, minus 1. The value of this parameter can be derived from the t_{XS} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_XSNR = (t_{XS}/t_{CK}) - 1$
15-6	T_XSRD	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a self-refresh exit to a command that requires a locked DLL, minus 1. The value of this parameter can be derived from the t_{XSDLL} AC timing parameter in the DDR3 memory data sheet. This parameter typically appears in the datasheet in terms of t_{CK} clock cycles. Calculate using the formula: $T\_XSRD = t_{XSDLL} - 1$
5-3	T_RTP	RW	These bits specify the minimum number of DDR3CLKOUT cycles from the last read to precharge command, minus 1. The value of this parameter can be derived from the t_{RTP} AC timing parameter in the DDR3 memory data sheet. Convert the t_{XP} datasheet parameter value into ns before using formula below. Calculate using the formula: $T\_RTP = (t_{RTP}/t_{CK}) - 1$
2-0	T_CKE	RW	These bits specify the minimum number of DDR3CLKOUT cycles between transitions on the DSDCKE pin, minus 1. The value of this parameter can be derived from the t_{CKE} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula: $T\_CKE = (t_{CKE}/t_{CK}) - 1$

4.7 SDRAM Timing 3 (SDTIM3) Register

Like the SDRAM Timing 1 and 2 registers (SDTIM1 & SDTIM2), the SDRAM Timing 3 register (SDTIM3) also configures the DDR3 memory controller to meet many of the AC timing specifications of the DDR3 memory. See the DDR3 memory datasheet for information on appropriate values to program each field. The SDTIM3 register is described in the following figure and table.

Figure 4-7. SDRAM Timing 3 (SDTIM3) Register

31 28	27 24	23 21	20 15	14 13	12 4	3 0
T_PDLL_UL	T_CSTA	T_CKESR	ZQ_ZQCS	Reserved	T_RFC	T_RAS_MAX
RW=0x0	RW=0x0	RW=0x3	RW=0x3F	R=0x3	RW=0x57	RW=0x6

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-9. SDRAM Timing 3 (SDTIM3) Register Field Descriptions

Bit	Field	Attribute	Description
31-28	T_PDLL_UL	RW	Value = 0 This field must always be programmed to 0x5.
27-24	T_CSTA	RW	Minimum DDR3CLKOUT cycles between write-to-write or read-to-read data phases to different chip selects, minus 1. This field should be set according to PHY requirements as 0x5.
23-21	T_CKESR	RW	Value = 0 Minimum DDR3CLKOUT cycles for which DDR3 should remain in self-refresh. This parameter typically appears as number of t_{CK} clock cycles. T_CKESR = (t_{CKESR}/t_{CK}) – 1
20-15	ZQ_ZQCS	RW	These bits specify the minimum number of DDR3CLKOUT cycles for a ZQCS command, minus 1. The value of this parameter can be derived from the t_{ZQCS} AC timing parameter in the DDR3 memory data sheet. This parameter typically appears as number of t_{CK} clock cycles. Calculate using the formula ZQ_ZQCS = t_{ZQCS} – 1
14-13	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
12-4	T_RFC	RW	These bits specify the minimum number of DDR3CLKOUT cycles from a refresh or load mode command to a refresh or activate command, minus 1. The value of this parameter can be derived from the t_{RFC} AC timing parameter in the DDR3 memory data sheet. Calculate using the formula T_RFC = (t_{RFC}/t_{CK}) – 1
3-0	T_RAS_MAX	RW	This field must always be programmed to 0xF.

4.8 Power Management Control Register (PMCTL)

The PMCTL register is described in the following figure and table.

Figure 4-8. Power Management Control Register (PMCTL)

31 16	15 12	11	10 8	7 4	3 0
Reserved	PD_TIM	Reserved	LP_MODE	SR_TIM	Reserved
R=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0	R=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-10. Power Management Control Register (PMCTL) Field Descriptions

Bit	Field	Attribute	Description
31-16	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
15-12	PD_TIM	RW	Power Management timer for power-down. The DDR3 memory controller will put the SDRAM in power-down mode after the DDR3 controller is idle for PD_TIM number of DDR3CLKOUT cycles and if LP_MODE is set to 4. • 0 = Immediately enter power-down • 1 = Enter power-down after 16 clocks • 2 = Enter power-down after 32 clocks • 3 = Enter power-down after 64 clocks • 4 = Enter power-down after 128 clocks • 5 = Enter power-down after 256 clocks • 6 = Enter power-down after 512 clocks • 7 = Enter power-down after 1024 clocks • 8 = Enter power-down after 2048 clocks • 9 = Enter power-down after 4096 clocks • 10 = Enter power-down after 8912 clocks • 11 = Enter power-down after 16384 clocks • 12 = Enter power-down after 32768 clocks • 13 = Enter power-down after 65536 clocks • 14 = Enter power-down after 131072 clocks • 15 = Enter power-down after 262144 clocks
11	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect
10-8	LP_MODE	RW	Automatic power management enable. • 2 = Self-refresh mode • 4 = Power-down mode All other values will disable automatic power management.

Table 4-10. Power Management Control Register (PMCTL) Field Descriptions (continued)

Bit	Field	Attribute	Description
7-4	SR_TIM	RW	Power management timer for self-refresh. The DDR3 memory controller will put the external SDRAM in self-refresh mode after DDR3 controller has been idle for these number of DDR3CLKOUT cycles and LP_MODE is set to 2. • 0 = Immediately enter self-refresh • 1 = Enter self-refresh after 16 clocks • 2 = Enter self-refresh after 32 clocks • 3 = Enter self-refresh after 64 clocks • 4 = Enter self-refresh after 128 clocks • 5 = Enter self-refresh after 256 clocks • 6 = Enter self-refresh after 512 clocks • 7 = Enter self-refresh after 1024 clocks • 8 = Enter self-refresh after 2048 clocks • 9 = Enter self-refresh after 4096 clocks • 10 = Enter self-refresh after 8912 clocks • 11 = Enter self-refresh after 16384 clocks • 12 = Enter self-refresh after 32768 clocks • 13 = Enter self-refresh after 65536 clocks • 14 = Enter self-refresh after 131072 clocks • 15 = Enter self-refresh after 262144 clocks
3-0	Reserved	R	Reserved

4.9 VBUSM Configuration Register (VBUSM_CONFIG)

The VBUSM_CONFIG register is described in the following figure and table.

Figure 4-9. VBUSM Configuration Register (VBUSM_CONFIG)

31 24	23 16	15 8	7 0
Reserved	COS_COUNT_1	COS_COUNT_2	PR_OLD_COUNT
R=0x0	RW=0xFF	RW=0xFF	RW=0xFF

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

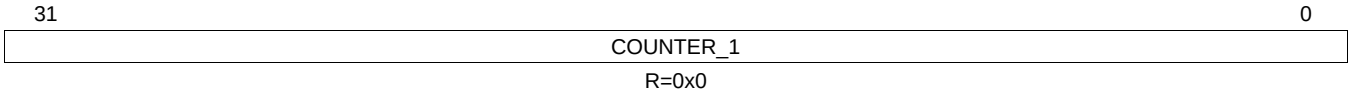
Table 4-11. VBUSM Configuration Register (VBUSM_CONFIG) Field Descriptions

Bit	Field	Attribute	Description
31-24	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
23-16	COS_COUNT_1	RW	Value = 0xFF Priority raise counter for Class of Service 1. Number of DDR3CLKOUT cycles after which the DDR3 controller momentarily raises the priority of Class of Service 1 commands in Command FIFO. Number of clock cycles = COS_COUNT_1 x 16 clocks
15-8	COS_COUNT_2	RW	Value = 0xFF Priority raise counter for Class of Service 2. Number of DDR3CLKOUT cycles after which the DDR3 controller momentarily raises the priority of Class of Service 2 commands in Command FIFO. Number of clock cycles = COS_COUNT_2 x 16 clocks
7-0	PR_OLD_COUNT	RW	Value = 0xFF Priority raise old counter. Number of DDR3CLKOUT cycles after which DDR3 controller momentarily raises the priority of the oldest command in Command FIFO. Number of clock cycles = PR_OLD_COUNT_2 x 16 clocks

4.10 Performance Counter 1 Register (PERF_CNT_1)

The PERF_CNT_1 register is described in the following figure and table.

Figure 4-10. Performance Counter 1 Register (PERF_CNT_1)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

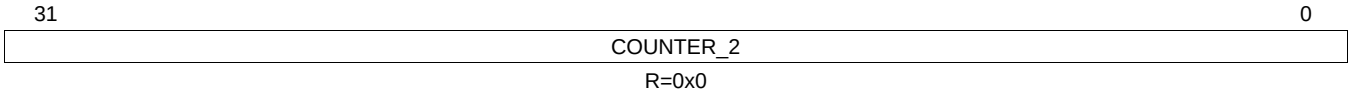
Table 4-12. Performance Counter 1 Register (PERF_CNT_1) Field Descriptions

Bit	Field	Attribute	Description
31-0	COUNTER_1	R	32-bit counter can be programmed as specified in the Performance Counter Config and Performance Counter Master Region Select registers.

4.11 Performance Counter 2 Register (PERF_CNT_2)

The PERF_CNT_2 register is described in the following figure and table.

Figure 4-11. Performance Counter 2 Register (PERF_CNT_2)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-13. Performance Counter 2 Register (PERF_CNT_2) Field Descriptions

Bit	Field	Attribute	Description
31-0	COUNTER_2	R	32-bit counter can be programmed as specified in the Performance Counter Config and Performance Counter Master Region Select registers.

4.12 Performance Counter Config Register (PERF_CNT_CFG)

The PERF_CNT_CFG register is described in the following figure and table.

Figure 4-12. Performance Counter Config Register (PERF_CNT_CFG)

31	30	29 20	19 16
CNTR2_MSTID_EN	CNTR2_REGION_EN	Reserved	CNTR2_CFG
RW=0x0	RW=0x0	R=0x0	RW=0x1
15	14	13 4	3 0
CNTR1_MSTID_EN	CNTR1_REGION_EN	Reserved	CNTR1_CFG
RW=0x0	RW=0x0	R=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-14. Performance Counter Config Register (PERF_CNT_CFG) Field Descriptions

Bit	Field	Attribute	Description
31	CNTR2_MSTID_EN	RW	Master ID filter enable for Performance Counter 2 Register. Set to 1 to enable filtering of events for counter 2 by Master ID. Refer to your device data manual for the master IDs of various masters.
30	CNTR2_REGION_EN	RW	Memory space region enable for Performance Counter 2 Register. Set to 1 to enable filtering of events for counter 2 by the accessed memory region.
29-20	Reserved	R	Value = 0x0 Reserved
19-16	CNTR2_CFG	RW	Filter configuration selected for Performance Counter 2. This field selects the type of event to count for Counter 2. Refer to Table 2-17 for various configuration options.
15	CNTR1_MSTID_EN	RW	Master ID filter enable for Performance Counter 1 Register. Set to 1 to enable filtering of events for counter 1 by Master ID. Refer to your device data manual for the master IDs of various masters.
14	CNTR1_REGION_EN	RW	Memory space region enable for Performance Counter 1 Register. Set to 1 to enable filtering of events for counter 1 by the accessed memory region.
13-4	Reserved	R	Value = 0x0 Reserved
3-0	CNTR1_CFG	RW	Filter configuration selected for Performance Counter 1. This field selects the type of event to count for Counter 1. Refer to Table 2-17 for various configuration options.

4.13 Performance Counter Master Region Select Register (PERF_CNT_SEL)

For events that can be configured to enable master ID and/or memory region filters, the value of the master ID and the region select options for the counters are programmed in the PERF_CNT_SEL register. The PERF_CNT_SEL register is described in the following figure and table.

Figure 4-13. Performance Counter Master Region Select Register (PERF_CNT_SEL)

31 24	23 20	19 16	15 8	7 4	3 0
MSTID2	Reserved	REGION_SEL2	MSTID1	Reserved	REGION_SEL1
RW=0x0	R=0x0	RW=0x0	RW=0x0	R=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

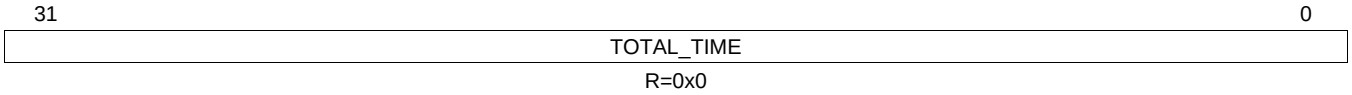
Table 4-15. Performance Counter Master Region Select Register (PERF_CNT_SEL) Field Descriptions

Bit	Field	Attribute	Description
31-24	MSTID2	RW	Master ID for Performance Counter 2 Register. Refer to your device data manual for the master IDs of various masters.
23-20	Reserved	R	Value = 0x0 Reserved
19-16	REGION_SEL2	RW	Region select for Performance Counter 2. • 0x0 - DDR3 memory space • 0x7 - DDR3 controller memory mapped registers All other values are reserved.
15-8	MSTID1	RW	Master ID for Performance Counter 1 Register. Refer to your device data manual for the master IDs of various masters.
7-4	Reserved	R	Value = 0x0 Reserved
3-0	REGION_SEL1	RW	Region select for Performance Counter 1. • 0x0 - DDR3 memory space • 0x7 - DDR3 controller memory mapped registers All other values are reserved.

4.14 Performance Counter Time Register (PERF_CNT_TIM)

The PERF_CNT_TIM register is described in the following figure and table.

Figure 4-14. Performance Counter Time Register (PERF_CNT_TIM)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-16. Performance Counter Time Register (PERF_CNT_TIM) Field Descriptions

Bit	Field	Attribute	Description
31-0	TOTAL_TIME	R	32-bit counter continuously counts number of DDR/2 clock cycles elapsed after the controller is brought out of reset.

4.15 Interrupt Raw Status Register (IRQSTATUS_RAW_SYS)

The IRQSTATUS_RAW_SYS register is described in the following figure and table.

Figure 4-15. Interrupt Raw Status Register (IRQSTATUS_RAW_SYS)

31	5	4	3	2	1	0
Reserved		RD_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved		ERR_SYS
R=0x0		WOS=0x0	WOS=0x0	R=0x0		WOS=0x0

Legend: R = Read only; WOS = Write one to set; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-17. Interrupt Raw Status Register (IRQSTATUS_RAW_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 5	Reserved	R	Value = 0x0 Reserved
4	RD_ECC_ERR_SYS	WOS	Value = 0x0 Raw status of read ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOS	Value = 0x0 Raw status of write ECC error interrupt. Writing a 1 sets the raw status. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved
0	ERR_SYS	WOS	Value = 0x0 Raw status of system VBUSM interrupt for command or address error. Writing a 1 sets the raw status. Writing a 0 has no effect.

4.16 Interrupt Status Register (IRQSTATUS_ SYS)

The IRQSTATUS_SYS register is described in the following figure and table.

Figure 4-16. Interrupt Status Register (IRQSTATUS_ SYS)

31 5	4	3	2 1	0
Reserved	RD_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved	ERR_SYS
R	WOC	WOC	R	WOC

Legend: R = Read only; WOC = write one to clear; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-18. Interrupt Status Register (IRQSTATUS_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 5	Reserved	R	Value = 0x0 Reserved.
4	RD_ECC_ERR_SYS	WOC	Value = 0x0 Enabled status of read ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOC	Value = 0x0 Enabled status of write ECC error interrupt. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved.
0	ERR_SYS	WOC	Value = 0x0 Enabled status of system VBUSM interrupt for command or address error. Writing a 1 clears the status as well the raw status. Writing a 0 has no effect.

4.17 Interrupt Enable Set Register (IRQSTATUS_ SET_SYS)

The IRQSTATUS_SET_SYS register is described in the following figure and table.

Figure 4-17. Interrupt Enable Set Register (IRQSTATUS_ SET_SYS)

31	5	4	3	2	1	0
Reserved		RD_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved		ERR_SYS
R=0x0		WOS=0x0	WOS=0x0	R=0x0		WOS=0x0

Legend: R = Read only; WOS = Write one to set; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-19. Interrupt Enable Set Register (IRQSTATUS_ SET_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 5	Reserved	R	Value = 0x0 Reserved.
4	RD_ECC_ERR_SYS	WOS	Value = 0x0 Enabled set for read ECC error interrupt. Writing a 1 will enable the read ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOS	Value = 0x0 Enabled set for write ECC error interrupt. Writing a 1 will enable the write ECC error interrupt, set this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved.
0	ERR_SYS	WOS	Value = 0x0 Enable set for system VBUSM interrupt for command or address error. Writing a 1 will enable the interrupt, and set this bit as well as the corresponding Interrupt Enable Clear Register. Writing a 0 has no effect.

4.18 Interrupt Enable Clear Register (IRQSTATUS_ CLR_SYS)

The IRQSTATUS_CLR_SYS register is described in the following figure and table.

Figure 4-18. Interrupt Enable Clear Register (IRQSTATUS_ CLR_SYS)

31	5	4	3	2	1	0
Reserved		RD_ECC_ERR_SYS	WR_ECC_ERR_SYS	Reserved		ERR_SYS
R		WOC=0x0	WOC=0x0	R		WOC=0x0

Legend: R = Read only; WOC = Write one to clear; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-20. Interrupt Enable Clear Register (IRQSTATUS_ CLR_SYS) Field Descriptions

Bit	Field	Attribute	Description
31- 5	Reserved	R	Value = 0x0 Reserved.
4	RD_ECC_ERR_SYS	WOC	Value = 0x0 Enabled clear for read ECC error interrupt. Writing a 1 will disable the read ECC error interrupt, clear this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
3	WR_ECC_ERR_SYS	WOC	Value = 0x0 Enabled clear for write ECC error interrupt. Writing a 1 will disable the write ECC error interrupt, clear this bit as well as the bit in Interrupt Enable Clear Register. Writing a 0 has no effect.
2-1	Reserved	R	Value = 0x0 Reserved.
0	ERR_SYS	WOC	Value = 0x0 Enable clear for system VBUSM interrupt for command or address error. Writing a 1 will disable the interrupt, and clear this bit as well as the corresponding Interrupt Enable Set Register. Writing a 0 has no effect.

4.19 SDRAM Output Impedance Calibration Configuration Register (ZQCFG)

The ZQCFG register is described in the following figure and table.

Figure 4-19. SDRAM Output Impedance Calibration Configuration Register (ZQCFG)

31	30	29	28
ZQ_CS1EN	ZQ_CS0EN	ZQ_DUALCALEN	ZQ_SFEXITEN
RW=0x1	RW=0x1	RW=0x0	RW=0x1

27 20	19 18	17 16	15 0
Reserved	ZQ_ZQINIT_MULT	ZQ_ZQCL_MULT	ZQ_REFINTERVAL
R	RW=0x1	RW=0x3	RW=0x4C1F

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-21. SDRAM Output Impedance Calibration Configuration Register (ZQCFG) Field Descriptions

Bit	Field	Attribute	Description
31	ZQ_CS1EN	RW	ZQ calibration for CS1 • 0 = Disable ZQ calibration for CS1 • 1 = Enable ZQ calibration for CS1
30	ZQ_CS0EN	RW	ZQ calibration for CS0 • 0 = Disable ZQ calibration for CS0 • 1 = Enable ZQ calibration for CS0
29	ZQ_DUALCALEN	RW	ZQ Dual Calibration enable. Allows both ranks to be calibrated simultaneously. • 0 = Dual ZQ calibration disable • 1 = Both chip selects have a separate calibration resistor per device. **This bit should always be set to 1** . See the Silicon Errata for your device for more details on this issue.
28	ZQ_SFEXITEN	RW	ZQCL on Self-refresh, Active power-down and precharge power-down exit enable. • 0 = Disable ZQCL on Self-refresh, Active power-down and precharge power-down exit enable • 1 = Enable ZQCL on Self-refresh, Active power-down and precharge power-down exit enable. Set this value to 1 to issue a ZQCL command upon self-refresh exit.
27- 20	Reserved	R	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
19-18	ZQ_ZQINIT_MULT	RW	Number of ZQCL intervals that make up a ZQINIT interval, minus one. The value of this parameter can be derived from the t_{ZQinit} and t_{ZQoper} AC timing parameters in the DDR3 memory data sheet. Calculate using the formula T_ZQ_ZQINIT_MULT = (t_{ZQinit}/t_{ZQoper} – 1)
17 -16	ZQ_ZQCL_MULT	RW	Number of ZQCS intervals that make up a ZQCL interval, minus one. ZQCS interval is defined by ZQ_ZQCS field in SDRAM Timing 3 (SDTIM3) register. The value of this parameter can be derived using the formula: T_ZQ_ZQCL_MULT = (t_{ZQoper}/t_{ZQCS} – 1)

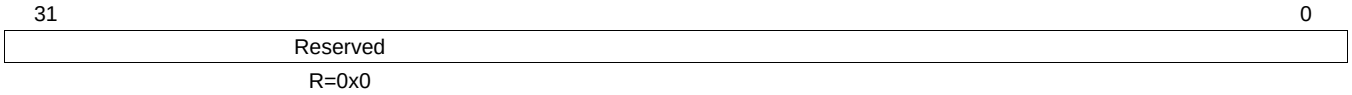
Table 4-21. SDRAM Output Impedance Calibration Configuration Register (ZQCFG) Field Descriptions (continued)

Bit	Field	Attribute	Description
15-0	ZQ_REFINTERVAL	RW	Number of refresh periods between ZQCS commands, minus one. This field supports between one refresh period to 256 ms between ZQCS calibration commands. Refresh period is defined by REFRESH_RATE field in SDRAM Refresh control (SDRFC) register. ZQ_REFINTERVAL = number of refresh periods between ZQCS commands. The interval is calculated as = 0.5% / [(Tsens x Tdriftrate) + (Vsens x Vdriftrate)]. Tsens = max (dRTTdT, dRONdTM) from the memory device datasheet. Vsens = max(dRTTdV, dRONdVM) from the memory device datasheet Tdriftrate = drift rate in ^{o} C/second. This is the temperature drift rate that the SDRAM is subject to in the application. Vdriftrate = drift rate in mV/second. This is the voltage drift rate that the SDRAM is subject to in the application. Example: If Tsens= 1.5%/ ^{o} C, Vsens = 0.15%/mV, Tdriftrate = 1.2 ^{o} C/second and Vdriftrate = 10mV/second, Interval = 0.5/[(1.5 x 1.2) + (0.15 x 10)] = 152ms. Since refresh interval = 7.8µs, ZQ_REFINTERVAL = 152ms/7.8µs = 0x4C1F

4.20 Read-Write Leveling Ramp Window Register (RDWR_LVL_RMP_WIN)

The RDWR_LVL_RMP_WIN register is described in the figure and table below.

Figure 4-20. Read-Write Leveling Ramp Window Register (RDWR_LVL_RMP_WIN)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-22. Read-Write Leveling Ramp Window Register (RDWR_LVL_RMP_WIN) Field Descriptions

Bit	Field	Attribute	Description
31-0	Reserved	R	Value = 0x0. This register is reserved, as ramp incremental leveling is not supported on Keystone-I devices.

4.21 Read-Write Leveling Ramp Control Register (RDWR_LVL_RMP_CTRL)

The RDWR_LVL_RMP_CTRL register is described in the figure and table below.

Figure 4-21. Read-Write Leveling Ramp Control Register (RDWR_LVL_RMP_CTRL)

31	30	0
RDWR_LVL_EN	Reserved	
RW=0x0	R=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-23. Read-Write Leveling Ramp Control Register (RDWR_LVL_RMP_CTRL) Field Descriptions

Bit	Field	Attribute	Description
31	RDWR_LVL_EN	RW	Value = 0x0 Global Read-Write leveling enable. • 0 Disable leveling (full and incremental) • 1 Enable leveling (full and incremental)
30-0	Reserved	R	Value = 0x0 These bits are reserved, as ramp incremental leveling is not supported on Keystone-I devices.

4.22 Read-Write Leveling Control Register (RDWR_LVL_CTRL)

The RDWR_LVL_CTRL register is described in the figure and table below.

Figure 4-22. Read-Write Leveling Control Register (RDWR_LVL_CTRL)

31	30 24	23 16	15 8	7 0
RDWRLVLFULL_START	RDWRLVLINC_PRE	RDLVLINC_INT	RDLVLGATEINC_INT	WRLVLINC_INT
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-24. Read-Write Leveling Control Register (RDWR_LVL_CTRL) Field Descriptions

Bit	Field	Description
31	RDWRLVLFULL_START	Value = 0x0 Full leveling trigger. • 0 No effect • 1 Trigger full leveling. This bit will self-clear to zero.
30-24	RDWRLVLINC_PRE	Value = 0x0 Incremental leveling pre-scalar in number of refresh periods. Value programmed is minus one the required value. Refresh period is defined by REFRESH_RATE in SDRFC register.
23-16	RDLVLINC_INT	Value = 0x0 Incremental read data eye training interval. Number of RDWRLVLINC_PRE intervals between incremental read data eye training. A value of zero will disable incremental read data eye training.
15-8	RDLVLGATEINC_INT	Value = 0x0 Incremental read DQS gate training interval. Number of RDWRLVLINC_PRE intervals between incremental read DQS gate training. A value of zero will disable incremental read DQS gate training.
7-0	WRLVLINC_INT	Value = 0x0 Incremental write leveling interval. Number of RDWRLVLINC_PRE intervals between incremental write leveling. A value of zero will disable incremental write leveling.

4.23 DDR PHY Control 1 Register (DDR_PHY_CTRL_1)

The DDR_PHY_CTRL_1 register is described in the following figure and table.

Figure 4-23. DDR PHY Control 1 Register (DDR_PHY_CTRL_1)

31 21	20	19 16	15	14
Reserved	EN_DYN_PWRDN	Reserved	PHY_RST	Reserved
R=0x0	RW=0x1	R=0x0	RW=0x0	R=0x0

13 12	11 10	9 8	7 5	4 0
IDLE_LOCAL_ODT	WR_LOCAL_ODT	RD_LOCAL_ODT	Reserved	READ_LATENCY
RW=0x0	RW=0x0	RW=0x1	R=0x0	RW=0xA

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-25. DDR PHY Control 1 Register (DDR_PHY_CTRL_1) Field Descriptions

Bit	Field	Attribute	Description
31-21	Reserved	R	Value = 0x0 Reserved.
20	EN_DYN_PWRDN	RW	Value = 0x1 • Enables dynamically powering down the IO Receiver when not performing a read 1 : IO Receiver for DQ, DQS always powered up 0 : IO Receiver for DQ, DQS powered up during a read
19-16	Reserved	R	Value = 0x0 Reserved
15	PHY_RST	RW	Controls DDR3 PHY reset • 0: Writing a 0 brings the DDR3 PHY out of reset • 1: Writing a 1 will hold the DDR3 PHY in reset
14	Reserved	R	Value = 0x0 Reserved
13-12	IDLE_LOCAL_ODT	RW	Value = 0x0 Program controller termination during idle cycles.
11-10	WR_LOCAL_ODT	RW	Value = 0x0 Program controller termination during write access.
9-8	RD_LOCAL_ODT	RW	Value = 0x1 Program controller termination during read access.
7-5	Reserved	RW	Value = 0x0 Reserved
4-0	READ_LATENCY	RW	Value = 0xA This field defines the read latency from DDR SDRAM in terms of DDR3 clock cycles. The value depends on the CAS latency used. The user can choose any value between max and min values given below. The programmed value should always be programmed as the chosen value minus one. • Maximum value possible = CAS latency + 7 • Minimum value possible = CAS Latency + 1

4.24 Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)

The PRI_COS_MAP register is described in the following figure and table.

Figure 4-24. Priority to Class-Of-Service Mapping Register (PRI_COS_MAP)

31	30 16	15 14	13 12	11 10
PRI_COS_MAP_EN	Reserved	PRI_7_COS	PRI_6_COS	PRI_5_COS
RW=0x0	R=0x0	RW=0x0	RW=0x0	RW=0x0

9 8	7 6	5 4	3 2	1 0
PRI_4_COS	PRI_3_COS	PRI_2_COS	PRI_1_COS	PRI_0_COS
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-26. Priority to Class-Of-Service Mapping Register (PRICOSMAP) Field Descriptions

Bit	Field	Description
31	PRI_COS_MAP_EN	Value = 0x0 Priority to Class-of-service mapping • 0 = Disable Priority to Class-of-service mapping • 1 = Enable Priority to Class-of-service mapping
30-16	Reserved	Value = 0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
15-14	PRI_7_COS	Class-of-service for commands with priority of 7 (lowest priority). • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
13-12	PRI_6_COS	Class-of-service for commands with priority of 6. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
11-10	PRI_5_COS	Class-of-service for commands with priority of 5. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
9-8	PRI_4_COS	Class-of-service for commands with priority of 4. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
7-6	PRI_3_COS	Class-of-service for commands with priority of 3. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
5-4	PRI_2_COS	Class-of-service for commands with priority of 2. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
3-2	PRI_1_COS	Class-of-service for commands with priority of 1. • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.
1-0	PRI_0_COS	Class-of-service for commands with priority of 0 (highest priority). • 1= Map to Class-of-service 1 • 2= Map to Class-of-service 2 • 0 or 3 will not assign any class of service.

4.25 Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP)

The MSTID_COS_1_MAP register is described in the following figure and table.

Figure 4-25. Master ID to Class-Of-Service 1 Mapping Register (MSTID_COS_1_MAP)

31	30 23	22 20
MSTID_COS_1_MAP_EN	MSTID_1_COS_1	MSK_1_COS_1
RW=0x0	RW=0x0	RW=0x0

19 12	11 10	9 2	1 0
MSTID_2_COS_1	MSK_2_COS_1	MSTID_3_COS_1	MSK_3_COS_1
RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-27. Master ID to Class-Of-Service Mapping 1 Register (MSTID_COS_1_MAP) Field Descriptions

Bit	Field	Description
31	MSTID_COS_1_MAP_EN	Master ID to Class-of-service 1 mapping. • 0 = Disable Master ID to Class-of-service 1 mapping • 1 = Enable Master ID to Class-of-service 1 mapping
30-23	MSTID_1_COS_1	Value = 0x0 Master ID value 1 for Class-of-service 1.
22-20	MSK_1_COS_1	Mask for master ID value 1 for Class-of-service 1. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
19-12	MSTID_2_COS_1	Value = 0x0 Master ID value 2 for Class-of-service 1.
11-10	MSK_2_COS_1	Mask for master ID value 2 for Class-of-service 1. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
9-2	MSTID_3_COS_1	Value = 0x0 Master ID value 3 for Class-of-service 1.
1-0	MSK_3_COS_1	Mask for master ID value 3 for Class-of-service 1. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0

4.26 Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP)

The MSTID_COS_2_MAP register is described in the following figure and table.

Figure 4-26. Master ID to Class-Of-Service 2 Mapping Register (MSTID_COS_2_MAP)

31	30 23	22 20	19 12	11 10	9 2	1 0
MSTID_COS_2_MAP_EN	MSTID_1_COS_2	MSK_1_COS_2	MSTID_2_COS_2	MSK_2_COS_2	MSTID_3_COS_2	MSK_3_COS_2
RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-28. Master ID to Class-Of-Service Mapping 2 Register (MSTID_COS_2_MAP) Field Descriptions

Bit	Field	Description
31	MSTID_COS_2_MAP_EN	Master ID to Class-of-service 2 mapping. • 0 = Disable Master ID to Class-of-service 2 mapping • 1 = Enable Master ID to Class-of-service 2 mapping
30-23	MSTID_1_COS_2	Value = 0x0 Master ID value 1 for Class-of-service 2.
22-20	MSK_1_COS_2	Mask for master ID value 1 for Class-of-service 2. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
19-12	MSTID_2_COS_2	Value = 0x0 Master ID value 2 for Class-of-service 2.
11-10	MSK_2_COS_2	Mask for master ID value 2 for Class-of-service 2. • 0 = Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0
9-2	MSTID_3_COS_2	Value = 0x0 Master ID value 3 for Class-of-service 2.
1-0	MSK_3_COS_2	Mask for master ID value 3 for Class-of-service 2. • 0 - Disable masking • 1 = Mask master ID bit 0 • 2 = Mask master ID bits 1-0 • 3 = Mask master ID bits 2-0

4.27 ECC Control Register (ECCCTL)

The ECCCTL register is described in the following figure and table.

Figure 4-27. ECC Control Register (ECCCTL)

31	30	29 2	1	0
ECC_EN	ECC_ADDR_RNG_PROT	Reserved	ECC_ADDR_RNG_2_EN	ECC_ADDR_RNG_1_EN
RW=0x0	RW=0x0	R=0x0	RW=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-29. ECC Control Register (ECCCTL) Field Descriptions

Bit	Field	Description
31	ECC_EN	ECC enable. Enabling ECC will cause the DDR3 controller to start the SDRAM initialization sequence. • 0 = Disable ECC • 1 = Enable ECC
30	ECC_ADDR_RNG_PROT	This bit is used to determine whether ECC calculation is allowed within address ranges described by ECC Address Range 1 and 2 Registers, provided ECC_EN is set to enable ECC. • 0 = Disable ECC calculation within address ranges defined in ECC Address Range 1 and 2 registers and enable calculation for accesses outside of these address ranges • 1 = Enable ECC calculation within address ranges defined in ECC Address Range 1 and 2 registers and disable calculation for accesses outside of these address ranges
29-2	Reserved	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
1	ECC_ADDR_RNG_2_EN	ECC Address Range 2 enable. • 0 = Disable ECC Address Range 2 • 1 = Enable ECC Address Range 2
0	ECC_ADDR_RNG_1_EN	ECC Address Range 1 enable. • 0 = Disable ECC Address Range 1 • 1 = Enable ECC Address Range 1

4.28 ECC Address Range 1 Register (ECCADDR1)

The ECCADDR1 register is described in the following figure and table.

Figure 4-28. ECC Address Range 1 Register (ECCADDR1)

31	16	15	0
ECC_END_ADDR_1		ECC_STRT_ADDR_1	
RW=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-30. ECC Address Range 1 Register Field Descriptions

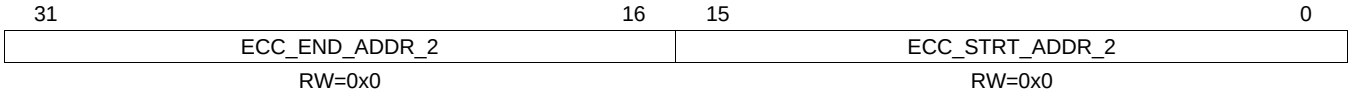
Bit	Field	Description
31-16	ECC_END_ADDR_1	End address [32-17] of 33-bit address for ECC address range 1
15-0	ECC_STRT_ADDR_1	Start address [32-17] of 33-bit address for ECC address range 1

NOTE: The range is inclusive of start and end addresses.

4.29 ECC Address Range 2 Register (ECCADDR2)

The ECCADDR2 register is described in the following figure and table.

Figure 4-29. ECC Address Range 2Register (ECCADDR2)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-31. ECC Address Range 2 Register Field Descriptions

Bit	Field	Description
31-16	ECC_END_ADDR_2	End address [32-17] of 33-bit address for ECC address range 2
15-0	ECC_STRT_ADDR_2	Start address [32-17] of 33-bit address for ECC address range 2

NOTE: The range is inclusive of start and end addresses.

4.30 Read Write Execution Threshold Register (RWTHRESH)

The RWTHRESH register is described in the following figure and table.

Figure 4-30. Read Write Execution Threshold Register (RWTHRESH)

31	13	12	8	7	5	4	0
Reserved		WR_THRSH		Reserved		RD_THRSH	
R=0x0		RW=0x3		R=0x0		RW=0x5	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-32. Read Write Execution Threshold Register (RWTHRESH) Field Descriptions

Bit	Field	Description
31-13	Reserved	Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
12-8	WR_THRSH	Write Threshold. Number of SDRAM write bursts after which the arbitration will switch to executing read commands. The value programmed is always minus 1 the required number.
7-5	Reserved	Value = 0x0 Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
4-0	RD_THRSH	Read Threshold. Number of SDRAM read bursts after which the arbitration will switch to executing write commands. The value programmed is always minus 1 the required number.

4.31 DDR3 Configuration 0 Register (DDR3_CONFIG_0)

The DDR3_CONFIG_0 register is described in the following figure and table.

Figure 4-31. DDR3 Configuration 0 Register (DDR3_CONFIG_0)

31	23	22	13	12	4	3	0
Reserved		CMD_PHY_CTRL_SLAVE_RATIO		Reserved		CMD_PHY_DLL_LOCK_DIFF	
R=0x0		RW=0x80		R0x0		RW=0x1	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

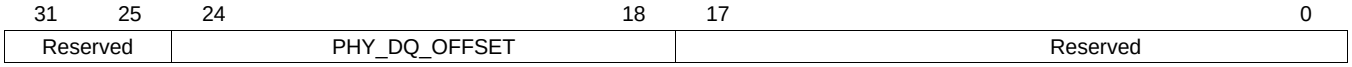
Table 4-33. DDR3_CONFIG_0 Register (0x02620404) Field Descriptions

Bits	Name	Description
31-23	Reserved	Reset = 0x0010000 Reserved. Do not write to this field.
22-13	CMD_PHY_CTRL_SLAVE_RATIO	Reset = 0x80 Program this to 0x100 if CMD_PHY_INVERT_CLKOUT in DDR3_CONFIG_12 is set to 1.
12-4	Reserved	Reset = 0x000
3-0	CMD_PHY_DLL_LOCK_DIFF	Reset = 0x1 Decides when DLL inside the DDR3 controller goes out of lock in case of jitter on the clock. Recommend program to 0xF.

4.32 DDR3 Configuration 1 Register (DDR3_CONFIG_1)

The DDR3_CONFIG_1 register is described in the following figure and table. This register is used to program the appropriate DQ-to-DQS timing relationship during writes for C665x devices and TCI6612/13/14. Do not program this register for any other device. Refer to the Keystone-I DDR3 Initialization app note for the proper programming sequence.

Figure 4-32. DDR3 Configuration 1 Register (DDR3_CONFIG_1)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

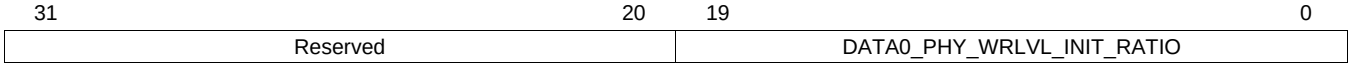
Table 4-34. DDR3_CONFIG_1 Register (0x02620408) Field Descriptions

Bits	Name	Description
31-25	Reserved	Reset = 0x0010000 Reserved. Do not write to this field.
24-18	PHY_DQ_OFFSET	Reset = 0x20 for C665x/TCI6612/13/14 Reset = 0x40 for other devices This field should be programmed to 0x40 for C665x and TCI6612/13/14 devices only, to set the proper DQ-DQS timing relationship for writes, and left unchanged for other devices because the default value already centers the DQ with the DQS. 0x40 is the only valid value. Other values are not supported.
17-0	Reserved	Reset = 0x000 Reserved

4.33 DDR3 Configuration 2 Register (DDR3_CONFIG_2)

The DDR3_CONFIG_2 register is described in the following figure and table.

Figure 4-33. DDR3 Configuration 2 Register (DDR3_CONFIG_2)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-35. DDR3_CONFIG_2 Register (0x0262040C) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA0_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 3 for C665x devices or Byte lane 7 for all other devices from the PHY calculation spreadsheet

4.34 DDR3 Configuration 3 Register (DDR3_CONFIG_3)

The DDR3_CONFIG_3 register is described in the following figure and table.

Figure 4-34. DDR3 Configuration 3 Register (DDR3_CONFIG_3)

31	20	19	0
Reserved		DATA1_PHY_WRLVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-36. DDR3_CONFIG_3 Register (0x02620410) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA1_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 2 for C665x devices or Byte lane 6 for all other devices from the PHY calculation spreadsheet.

4.35 DDR3 Configuration 4 Register (DDR3_CONFIG_4)

The DDR3_CONFIG_4 register is described in the following figure and table.

Figure 4-35. DDR3 Configuration 4 Register (DDR3_CONFIG_4)

31	20	19	0
Reserved		DATA2_PHY_WRLVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-37. DDR3_CONFIG_4 Register (0x02620414) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA2_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 1 for C665x devices or Byte lane 5 for all other devices from the PHY calculation spreadsheet.

4.36 DDR3 Configuration 5 Register (DDR3_CONFIG_5)

DDR3 Configuration Register 5 is used for full leveling, and is described in the following figure and table.

Figure 4-36. DDR3 Configuration 5 Register (DDR3_CONFIG_5)

31	20	19	0
Reserved		DATA3_PHY_WRLVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-38. DDR3_CONFIG_5 Register (0x02620418) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA3_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 0 for C665x devices or Byte lane 4 for all other devices from the PHY calculation spreadsheet.

4.37 DDR3 Configuration 6 Register (DDR3_CONFIG_6)

DDR3 Configuration Register 6 is used for full leveling, and is described in the following figure and table.

Figure 4-37. DDR3 Configuration 6 Register (DDR3_CONFIG_6)

31	20	19	0
Reserved		DATA4_PHY_WRLVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

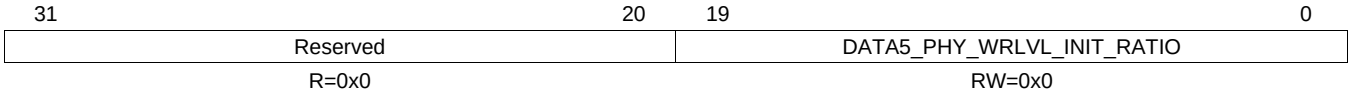
Table 4-39. DDR3_CONFIG_6 Register (0x0262041C) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA4_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 3 from the PHY calculation spreadsheet (NA for C665x devices).

4.38 DDR3 Configuration 7 Register (DDR3_CONFIG_7)

DDR3 Configuration Register 7 is used for full leveling, and is described in the following figure and table.

Figure 4-38. DDR3 Configuration 7 Register (DDR3_CONFIG_7)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

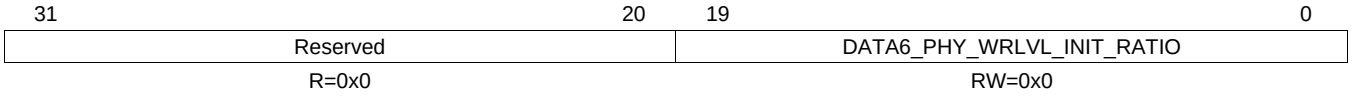
Table 4-40. DDR3_CONFIG_7 Register (0x02620420) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA5_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 2 from the PHY calculation spreadsheet (NA for C665x devices).

4.39 DDR3 Configuration 8 Register (DDR3_CONFIG_8)

DDR3 Configuration Register 8 is used for full leveling, and is described in the following figure and table.

Figure 4-39. DDR3 Configuration 8 Register (DDR3_CONFIG_8)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-41. DDR3_CONFIG_8 Register (0x02620424) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA6_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 1 from the PHY calculation spreadsheet (NA for C665x devices).

4.40 DDR3 Configuration 9 Register (DDR3_CONFIG_9)

DDR3 Configuration Register 9 is used for full leveling, and is described in the following figure and table.

Figure 4-40. DDR3 Configuration 9 Register (DDR3_CONFIG_9)

31	20	19	0
Reserved		DATA7_PHY_WRLVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-42. DDR3_CONFIG_9 Register (0x02620428) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA7_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 0 from the PHY calculation spreadsheet (NA for C665x devices).

4.41 DDR3 Configuration 10 Register (DDR3_CONFIG_10)

DDR3 Configuration Register 10 is used for full leveling, and is described in the following figure and table.

Figure 4-41. DDR3 Configuration 10 Register (DDR3_CONFIG_10)

31	20	19	0
Reserved		DATA8_PHY_WRLVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-43. DDR3_CONFIG_10 Register (0x0262042C) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA8_PHY_WRLVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_wrlvl_init_ratio value for Byte lane 8 (ECC byte lane) from the PHY calculation spreadsheet (same for all devices).

4.42 DDR3 Configuration 12 Register (DDR3_CONFIG_12)

DDR3 Configuration Register 12 is used if using invert clock out. See Section 2.13.7 on invert clockout for routing conditions under which invert clock out should be used.

Figure 4-42. DDR3 Configuration 12 Register (DDR3_CONFIG_12)

31 28	27	26	25 24	23 0
Reserved	CMD_PHY_INVERT_CLKOUT	Rsvd	USE_RANK0_DELAYS	Reserved
R=0x0	RW=0x0	R0x2000000	RW=0x0	R0x2000000

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-44. DDR3_CONFIG_12 Register (0x02620434) Field Descriptions

Bits	Name	Description
31-28	Reserved	Reset = 0x0 Reserved.
27	CMD_PHY_INVERT_CLKOUT	Reset = 0x0 • 0 - Don't use invert clock out • 1 - Use invert clockout.
26-25	Reserved	Reset = 0x2000000 Reserved.
24	USE_RANK0_DELAYS	This should be set to 1 after leveling is completed if using both chip selects for dual rank access. Note that this is part of a sequence of steps to enable dual rank support. See the DDR3 Initialization app note for details on how to sequence the initialization steps for dual rank support.
23-0	Reserved	Reset = 0x2000000 Reserved.

4.43 DDR3 Configuration 14 Register (DDR3_CONFIG_14)

DDR3 Configuration Register 14 is used for full leveling, and is described in the following figure and table.

Figure 4-43. DDR3 Configuration 14 Register (DDR3_CONFIG_14)

31 20	19 0
Reserved	DATA0_PHY_GATELVL_INIT_RATIO
R=0x0	RW=0x0

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-45. DDR3_CONFIG_14 Register (0x0262043C) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA0_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 3 for C665x devices or Byte lane 7 for all other devices from the PHY calculation spreadsheet.

4.44 DDR3 Configuration 15 Register (DDR3_CONFIG_15)

DDR3 Configuration Register 15 is used for full leveling, and is described in the following figure and table.

Figure 4-44. DDR3 Configuration 15 Register (DDR3_CONFIG_15)

31	20	19	0
Reserved		DATA1_PHY_GATELVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-46. DDR3_CONFIG_15 Register (0x02620440) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA1_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 2 for C665x devices or Byte lane 6 for all other devices from the PHY calculation spreadsheet.

4.45 DDR3 Configuration 16 Register (DDR3_CONFIG_16)

DDR3 Configuration Register 16 is used for full leveling, and is described in the following figure and table.

Figure 4-45. DDR3 Configuration 16 Register (DDR3_CONFIG_16)

31	20	19	0
Reserved		DATA2_PHY_GATELVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-47. DDR3_CONFIG_16 Register (0x02620444) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA2_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 1 for C665x devices or Byte lane 5 for all other devices from the PHY calculation spreadsheet.

4.46 DDR3 Configuration 17 Register (DDR3_CONFIG_17)

DDR3 Configuration Register 17 is used for full leveling, and is described in the following figure and table.

Figure 4-46. DDR3 Configuration 17 Register (DDR3_CONFIG_17)

31	20	19	0
Reserved		DATA3_PHY_GATELVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-48. DDR3_CONFIG_17 Register (0x02620448) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA3_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 0 for C665x devices or Byte lane 4 for all other devices from the PHY calculation spreadsheet.

4.47 DDR3 Configuration 18 Register (DDR3_CONFIG_18)

DDR3 Configuration Register 18 is used for full leveling, and is described in the following figure and table.

Figure 4-47. DDR3 Configuration 18 Register (DDR3_CONFIG_18)

31	20	19	0
Reserved		DATA4_PHY_GATELVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

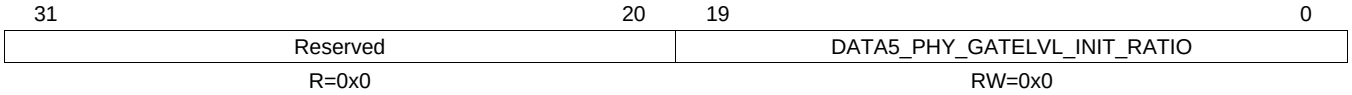
Table 4-49. DDR3_CONFIG_18 Register (0x0262044C) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA4_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 3 from the PHY calculation spreadsheet (NA for C665x devices).

4.48 DDR3 Configuration 19 Register (DDR3_CONFIG_19)

DDR3 Configuration Register 19 is used for full leveling, and is described in the following figure and table.

Figure 4-48. DDR3 Configuration 19 Register (DDR3_CONFIG_19)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

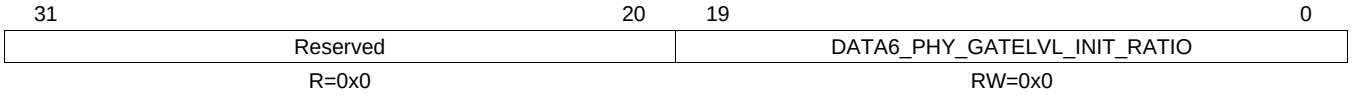
Table 4-50. DDR3_CONFIG_19 Register (0x02620450) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA5_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 2 from the PHY calculation spreadsheet (NA for C665x devices).

4.49 DDR3 Configuration 20 Register (DDR3_CONFIG_20)

DDR3 Configuration Register 20 is used for full leveling, and is described in the following figure and table.

Figure 4-49. DDR3 Configuration 20 Register (DDR3_CONFIG_20)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-51. DDR3_CONFIG_20 Register (0x02620454) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA6_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 1 from the PHY calculation spreadsheet (NA for C665x devices).

4.50 DDR3 Configuration 21 Register (DDR3_CONFIG_21)

DDR3 Configuration Register 21 is used for full leveling, and is described in the following figure and table.

Figure 4-50. DDR3 Configuration 21 Register (DDR3_CONFIG_21)

31	20	19	0
Reserved		DATA7_PHY_GATELVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-52. DDR3_CONFIG_21 Register (0x02620458) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA7_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 0 from the PHY calculation spreadsheet (NA for C665x devices).

4.51 DDR3 Configuration 22 Register (DDR3_CONFIG_22)

DDR3 Configuration Register 22 is used for full leveling, and is described in the following figure and table.

Figure 4-51. DDR3 Configuration 22 Register (DDR3_CONFIG_22)

31	20	19	0
Reserved		DATA8_PHY_GATELVL_INIT_RATIO	
R=0x0		RW=0x0	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-53. DDR3_CONFIG_22 Register (0x0262045C) Field Descriptions

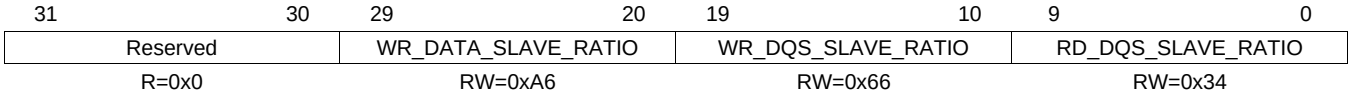
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA8_PHY_GATELVL_INIT_RATIO	Reset = 0x0 Plug in the reg_phy_gatelvl_init_ratio value for Byte lane 8 (ECC byte lane) from the PHY calculation spreadsheet (same for all devices).

4.52 DDR3 Configuration 23 Register (DDR3_CONFIG_23)

NOTE: NA for TCI6612/13/14 and C665x devices.

DDR3 Configuration Register 23 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-52. DDR3 Configuration 23 Register (DDR3_CONFIG_23)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-54. DDR3_CONFIG_23 Register (0x02620460) Field Descriptions

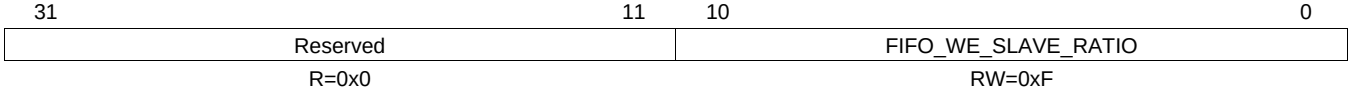
Bits	Name	Description
31-30	Reserved	Reset = 0x0 Reserved.
29-20	WR_DATA_SLAVE_RATIO	Reset = 0xA6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet.
19-10	WR_DQS_SLAVE_RATIO	Reset = 0x66 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet.
9-0	RD_DQS_SLAVE_RATIO	Reset = 0x34 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet.

4.53 DDR3 Configuration 24 Register (DDR3_CONFIG_24)

NOTE: NA for TCI6612/13/14 and C665x devices.

DDR3 Configuration Register 24 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-53. DDR3 Configuration 24 Register (DDR3_CONFIG_24)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-55. DDR3_CONFIG_24 Register (0x02620464) Field Descriptions

Bits	Name	Description
31-11	Reserved	Reset = 0x0 Reserved.
10-0	FIFO_WE_SLAVE_RATIO	Reset = 0x15 Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet.

4.54 DDR3 Configuration 25 Register (DDR3_CONFIG_25)

DDR3 Configuration Register 25 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-54. DDR3 Configuration 25 Register (DDR3_CONFIG_25)

31	22	21	0
Reserved		DATA0_FIFO_WE_SLAVE_RATIO	
R=0x0		RW=0xAD95B	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-56. DDR3_CONFIG_25 Register (0x02620468) Field Descriptions

Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA0_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 3 for C665x devices or Byte lane 7 for TCI6612/13/14.

4.55 DDR3 Configuration 26 Register (DDR3_CONFIG_26)

DDR3 Configuration Register 26 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-55. DDR3 Configuration 26 Register (DDR3_CONFIG_26)

31	22	21	0
Reserved		DATA1_FIFO_WE_SLAVE_RATIO	
R=0x0		RW=0xAD95B	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-57. DDR3_CONFIG_26 Register (0x0262046C) Field Descriptions

Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA1_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 2 for C665x devices or Byte lane 6 for TCI6612/13/14.

4.56 DDR3 Configuration 27 Register (DDR3_CONFIG_27)

DDR3 Configuration Register 27 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-56. DDR3 Configuration 27 Register (DDR3_CONFIG_27)

31	22	21	0
Reserved		DATA2_FIFO_WE_SLAVE_RATIO	
R=0x0		RW=0xAD95B	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-58. DDR3_CONFIG_27 Register (0x02620470) Field Descriptions

Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA2_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 1 for C665x devices or Byte lane 5 for TCI6612/13/14.

4.57 DDR3 Configuration 28 Register (DDR3_CONFIG_28)

DDR3 Configuration Register 28 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-57. DDR3 Configuration 28 Register (DDR3_CONFIG_28)

31	22	21	0
Reserved		DATA3_FIFO_WE_SLAVE_RATIO	
R=0x0		RW=0xAD95B	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-59. DDR3_CONFIG_28 Register (0x02620474) Field Descriptions

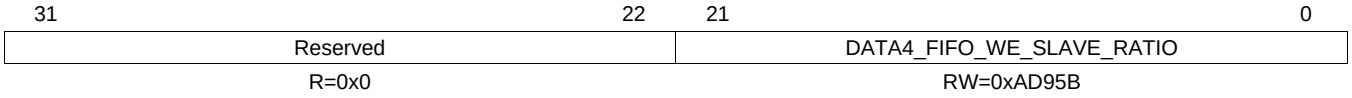
Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA3_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 0 for C665x devices or Byte lane 4 for TCI6612/13/14.

4.58 DDR3 Configuration 29 Register (DDR3_CONFIG_29)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 29 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-58. DDR3 Configuration 29 Register (DDR3_CONFIG_29)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-60. DDR3_CONFIG_29 Register (0x02620478) Field Descriptions

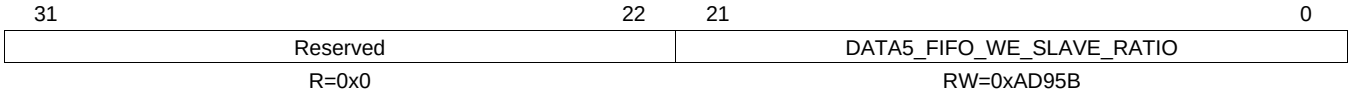
Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA4_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 3 for TCI6612/13/14.

4.59 DDR3 Configuration 30 Register (DDR3_CONFIG_30)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 30 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-59. DDR3 Configuration 30 Register (DDR3_CONFIG_30)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-61. DDR3_CONFIG_30 Register (0x0262047C) Field Descriptions

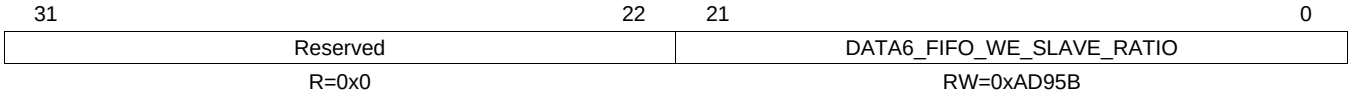
Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA5_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 2 for TCI6612/13/14.

4.60 DDR3 Configuration 31 Register (DDR3_CONFIG_31)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 31 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-60. DDR3 Configuration 31 Register (DDR3_CONFIG_31)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-62. DDR3_CONFIG_31 Register (0x02620480) Field Descriptions

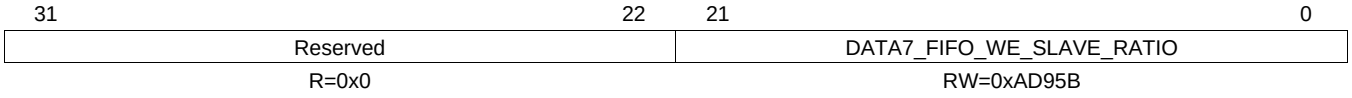
Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA6_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 1 for TCI6612/13/14.

4.61 DDR3 Configuration 32 Register (DDR3_CONFIG_32)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 32 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-61. DDR3 Configuration 32 Register (DDR3_CONFIG_32)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-63. DDR3_CONFIG_32 Register (0x02620484) Field Descriptions

Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA7_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for Byte lane 0 for TCI6612/13/14.

4.62 DDR3 Configuration 33 Register (DDR3_CONFIG_33)

DDR3 Configuration Register 33 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-62. DDR3 Configuration 33 Register (DDR3_CONFIG_33)

31	22	21	0
Reserved		DATA_ECC_FIFO_WE_SLAVE_RATIO	
R=0x0		RW=0xAD95B	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-64. DDR3_CONFIG_33 Register (0x02620488) Field Descriptions

Bits	Name	Description
31-22	Reserved	Reset = 0x0 Reserved.
21-0	DATA_ECC_FIFO_WE_SLAVE_RATIO	Reset = 0x000AD95B Plug in the effective reg_phy_fifo_we_slave_ratio value from the PHY calculation spreadsheet for ECC Byte lane (same for both devices).

4.63 DDR3 Configuration 34 Register (DDR3_CONFIG_34)

DDR3 Configuration Register 34 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-63. DDR3 Configuration 34 Register (DDR3_CONFIG_34)

31	20	19	0
Reserved		DATA0_WR_DATA_SLAVE_RATIO	
R=0x0		RW=0x298A6	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

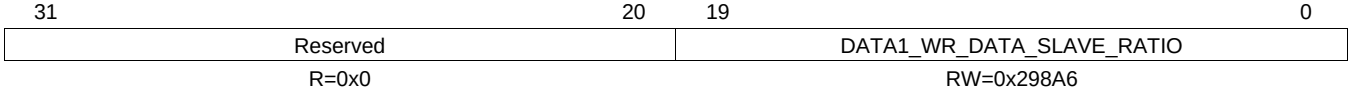
Table 4-65. DDR3_CONFIG_34 Register (0x0262048C) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA0_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 3 for C665x devices or Byte lane 7 for TCI6612/13/14.

4.64 DDR3 Configuration 35 Register (DDR3_CONFIG_35)

DDR3 Configuration Register 35 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-64. DDR3 Configuration 35 Register (DDR3_CONFIG_35)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

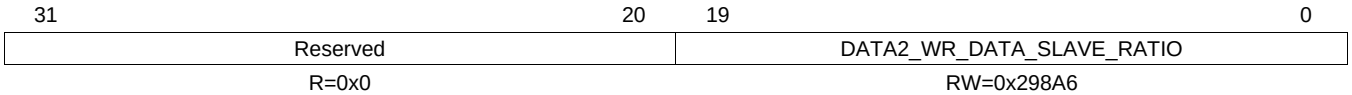
Table 4-66. DDR3_CONFIG_35 Register (0x02620490) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA1_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 2 for C665x devices or Byte lane 6 for TCI6612/13/14.

4.65 DDR3 Configuration 36 Register (DDR3_CONFIG_36)

DDR3 Configuration Register 36 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-65. DDR3 Configuration 36 Register (DDR3_CONFIG_36)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-67. DDR3_CONFIG_36 Register (0x02620494) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA2_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 1 for C665x devices or Byte lane 5 for TCI6612/13/14.

4.66 DDR3 Configuration 37 Register (DDR3_CONFIG_37)

DDR3 Configuration Register 37 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-66. DDR3 Configuration 37 Register (DDR3_CONFIG_37)

31	20	19	0
Reserved		DATA3_WR_DATA_SLAVE_RATIO	
R=0x0		RW=0x298A6	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-68. DDR3_CONFIG_37 Register (0x02620498) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA3_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 0 for C665x devices or Byte lane 4 for TCI6612/13/14.

4.67 DDR3 Configuration 38 Register (DDR3_CONFIG_38)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 38 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-67. DDR3 Configuration 38 Register (DDR3_CONFIG_38)

31	20	19	0
Reserved		DATA4_WR_DATA_SLAVE_RATIO	
R=0x0		RW=0x298A6	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-69. DDR3_CONFIG_38 Register (0x0262049C) Field Descriptions

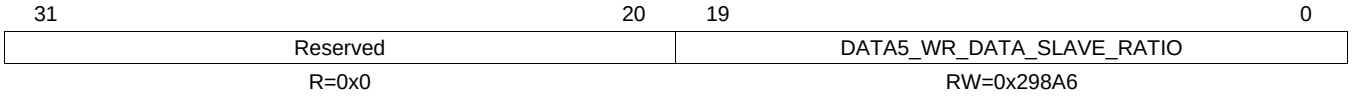
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA4_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 3 for TCI6612/13/14.

4.68 DDR3 Configuration 39 Register (DDR3_CONFIG_39)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 39 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-68. DDR3 Configuration 39 Register (DDR3_CONFIG_39)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-70. DDR3_CONFIG_39 Register (0x026204A0) Field Descriptions

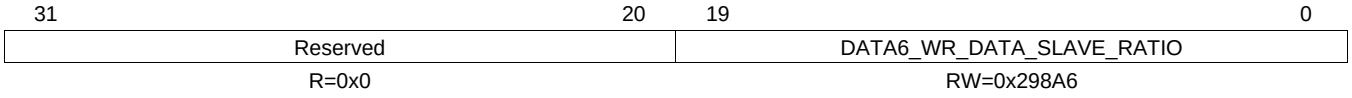
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA5_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 2 for TCI6612/13/14.

4.69 DDR3 Configuration 40 Register (DDR3_CONFIG_40)

NOTE: (TCI6612/13/14 only)

DDR3 Configuration Register 40 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-69. DDR3 Configuration 40 Register (DDR3_CONFIG_40)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-71. DDR3_CONFIG_40 Register (0x026204A4) Field Descriptions

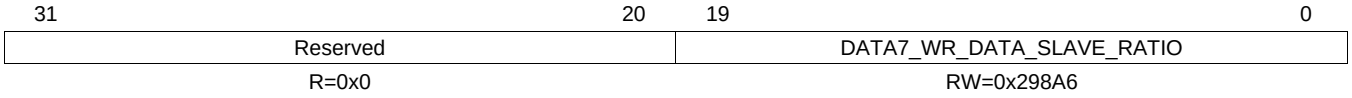
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA6_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 1 for TCI6612/13/14.

4.70 DDR3 Configuration 41 Register (DDR3_CONFIG_41)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 41 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-70. DDR3 Configuration 41 Register (DDR3_CONFIG_41)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

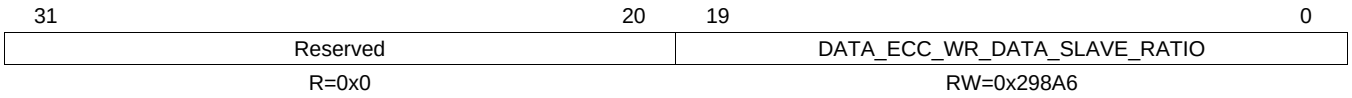
Table 4-72. DDR3_CONFIG_41 Register (0x026204A8) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA7_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for Byte lane 0 for TCI6612/13/14.

4.71 DDR3 Configuration 42 Register (DDR3_CONFIG_42)

DDR3 Configuration Register 42 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-71. DDR3 Configuration 42 Register (DDR3_CONFIG_42)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

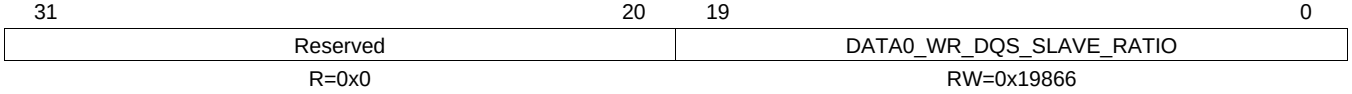
Table 4-73. DDR3_CONFIG_42 Register (0x026204AC) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA_ECC_WR_DATA_SLAVE_RATIO	Reset = 0x000298A6 Plug in the effective reg_phy_wr_data_slave_ratio value from the PHY calculation spreadsheet for ECC Byte lane (same for both devices)

4.72 DDR3 Configuration 43 Register (DDR3_CONFIG_43)

DDR3 Configuration Register 43 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-72. DDR3 Configuration 43 Register (DDR3_CONFIG_43)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

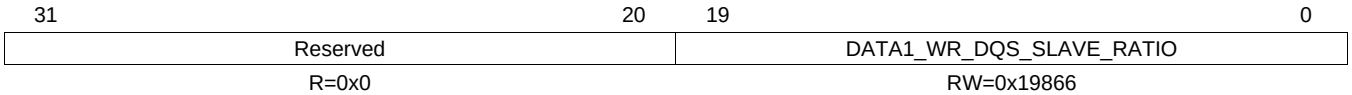
Table 4-74. DDR3_CONFIG_43 Register (0x026204B0) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA0_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 3 for C665x devices or Byte lane 7 for TCI6612/13/14.

4.73 DDR3 Configuration 44 Register (DDR3_CONFIG_44)

DDR3 Configuration Register 44 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-73. DDR3 Configuration 44 Register (DDR3_CONFIG_44)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

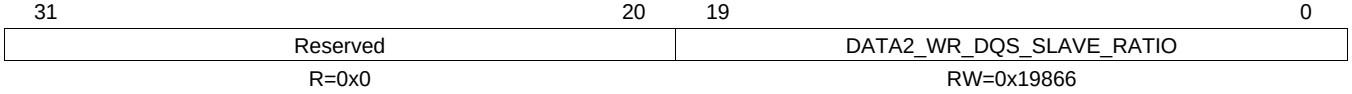
Table 4-75. DDR3_CONFIG_44 Register (0x026204B4) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA1_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 2 for C665x devices or Byte lane 6 for TCI6612/13/14.

4.74 DDR3 Configuration 45 Register (DDR3_CONFIG_45)

DDR3 Configuration Register 45 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-74. DDR3 Configuration 45 Register (DDR3_CONFIG_45)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

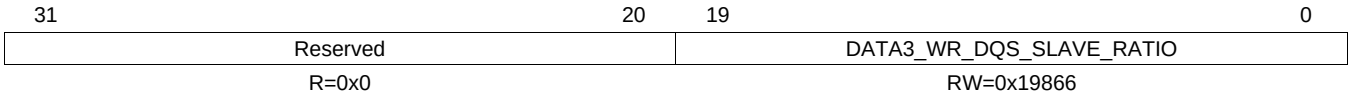
Table 4-76. DDR3_CONFIG_45 Register (0x026204B8) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA2_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 1 for C665x devices or Byte lane 5 for TCI6612/13/14.

4.75 DDR3 Configuration 46 Register (DDR3_CONFIG_46)

DDR3 Configuration Register 46 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-75. DDR3 Configuration 46 Register (DDR3_CONFIG_46)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-77. DDR3_CONFIG_46 Register (0x026204BC) Field Descriptions

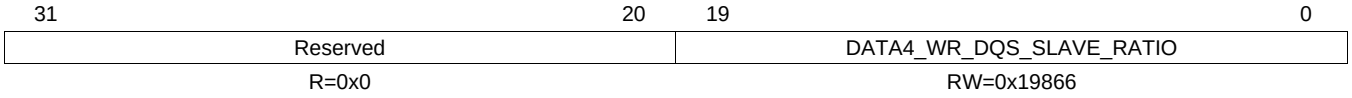
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA3_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 0 for C665x devices or Byte lane 4 for TCI6612/13/14.

4.76 DDR3 Configuration 47 Register (DDR3_CONFIG_47)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 47 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-76. DDR3 Configuration 47 Register (DDR3_CONFIG_47)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-78. DDR3_CONFIG_47 Register (0x026204C0) Field Descriptions

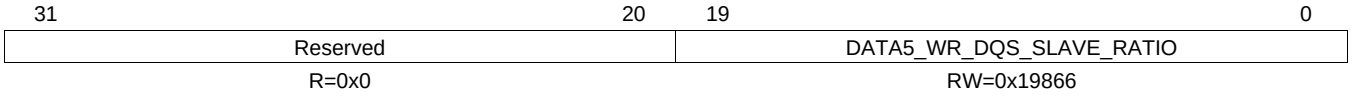
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA4_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 3 for TCI6612/13/14.

4.77 DDR3 Configuration 48 Register (DDR3_CONFIG_48)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 48 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-77. DDR3 Configuration 48 Register (DDR3_CONFIG_48)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-79. DDR3_CONFIG_48 Register (0x026204C4) Field Descriptions

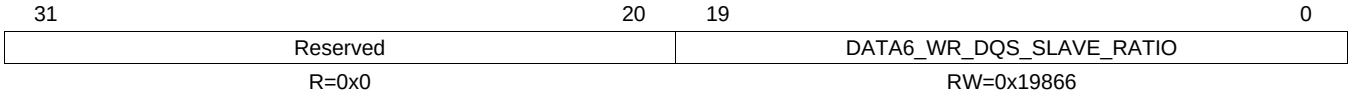
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA5_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 2 for TCI6612/13/14.

4.78 DDR3 Configuration 49 Register (DDR3_CONFIG_49)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 49 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-78. DDR3 Configuration 49 Register (DDR3_CONFIG_49)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-80. DDR3_CONFIG_49 Register (0x026204C8) Field Descriptions

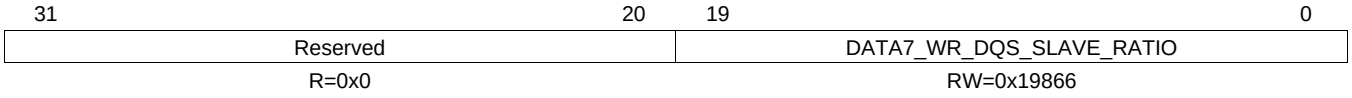
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA6_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 1 for TCI6612/13/14.

4.79 DDR3 Configuration 50 Register (DDR3_CONFIG_50)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 50 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-79. DDR3 Configuration 50 Register (DDR3_CONFIG_50)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

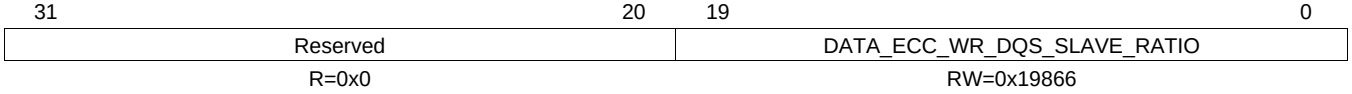
Table 4-81. DDR3_CONFIG_50 Register (0x026204CC) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA7_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 0 for TCI6612/13/14.

4.80 DDR3 Configuration 51 Register (DDR3_CONFIG_51)

DDR3 Configuration Register 51 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-80. DDR3 Configuration 51 Register (DDR3_CONFIG_51)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

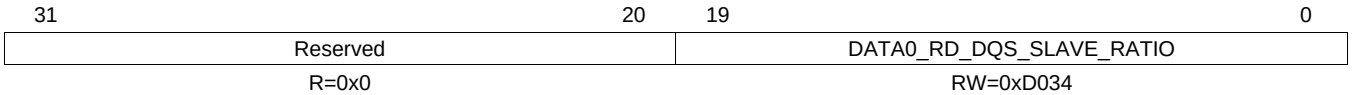
Table 4-82. DDR3_CONFIG_51 Register (0x026204D0) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA_ECC_WR_DQS_SLAVE_RATIO	Reset = 0x00019866 Plug in the effective reg_phy_wr_dqs_slave_ratio value from the PHY calculation spreadsheet for ECC Byte lane (same for both devices)

4.81 DDR3 Configuration 52 Register (DDR3_CONFIG_52)

DDR3 Configuration Register 52 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-81. DDR3 Configuration 52 Register (DDR3_CONFIG_52)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-83. DDR3_CONFIG_52 Register (0x026204D4) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA0_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 3 for C665x devices or Byte Lane 7 for TCI6612/13/14.

4.82 DDR3 Configuration 53 Register (DDR3_CONFIG_53)

DDR3 Configuration Register 53 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-82. DDR3 Configuration 53 Register (DDR3_CONFIG_53)

31	20	19	0
Reserved		DATA1_RD_DQS_SLAVE_RATIO	
R=0x0		RW=0xD034	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-84. DDR3_CONFIG_53 Register (0x026204D8) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA1_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 2 for C665x devices or Byte Lane 6 for TCI6612/13/14.

4.83 DDR3 Configuration 54 Register (DDR3_CONFIG_54)

DDR3 Configuration Register 54 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-83. DDR3 Configuration 54 Register (DDR3_CONFIG_54)

31	20	19	0
Reserved		DATA2_RD_DQS_SLAVE_RATIO	
R=0x0		RW=0xD034	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-85. DDR3_CONFIG_54 Register (0x026204DC) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA2_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 1 for C665x devices or Byte Lane 5 for TCI6612/13/14.

4.84 DDR3 Configuration 55 Register (DDR3_CONFIG_55)

DDR3 Configuration Register 55 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-84. DDR3 Configuration 55 Register (DDR3_CONFIG_55)

31	20	19	0
Reserved		DATA3_RD_DQS_SLAVE_RATIO	
R=0x0		RW=0xD034	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-86. DDR3_CONFIG_55 Register (0x026204E0) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA3_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte lane 0 for C665x devices or Byte Lane 4 for TCI6612/13/14.

4.85 DDR3 Configuration 56 Register (DDR3_CONFIG_56)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 56 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-85. DDR3 Configuration 56 Register (DDR3_CONFIG_56)

31	20	19	0
Reserved		DATA4_RD_DQS_SLAVE_RATIO	
R=0x0		RW=0xD034	

Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-87. DDR3_CONFIG_56 Register (0x026204E4) Field Descriptions

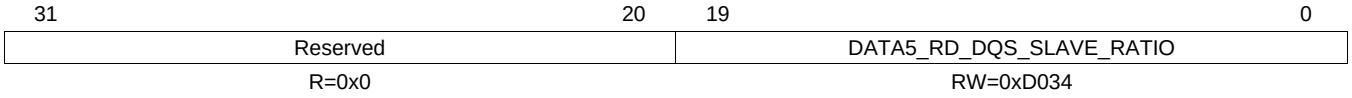
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA4_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte Lane 3 for TCI6612/13/14.

4.86 DDR3 Configuration 57 Register (DDR3_CONFIG_57)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 57 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-86. DDR3 Configuration 57 Register (DDR3_CONFIG_57)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-88. DDR3_CONFIG_57 Register (0x026204E8) Field Descriptions

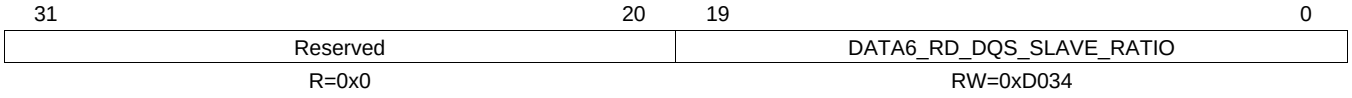
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA5_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte Lane 2 for TCI6612/13/14.

4.87 DDR3 Configuration 58 Register (DDR3_CONFIG_58)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 58 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-87. DDR3 Configuration 58 Register (DDR3_CONFIG_58)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-89. DDR3_CONFIG_58 Register (0x026204EC) Field Descriptions

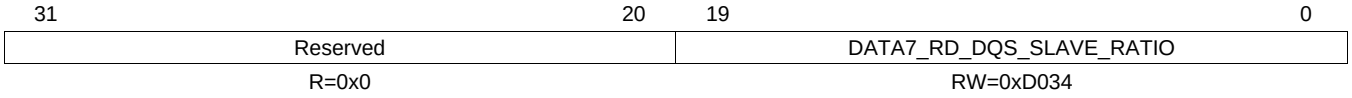
Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA6_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte Lane 1 for TCI6612/13/14.

4.88 DDR3 Configuration 59 Register (DDR3_CONFIG_59)

NOTE: TCI6612/13/14 only.

DDR3 Configuration Register 59 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-88. DDR3 Configuration 59 Register (DDR3_CONFIG_59)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

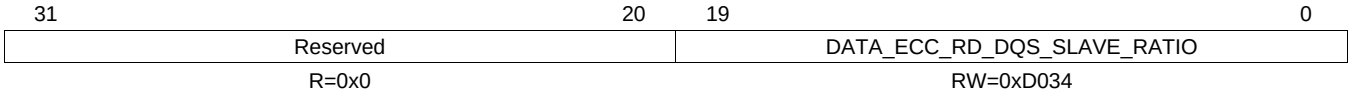
Table 4-90. DDR3_CONFIG_59 Register (0x026204F0) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA7_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for Byte Lane 0 for TCI6612/13/14.

4.89 DDR3 Configuration 60 Register (DDR3_CONFIG_60)

DDR3 Configuration Register 60 is used for forced ratio leveling, and is described in the following figure and table.

Figure 4-89. DDR3 Configuration 60 Register (DDR3_CONFIG_60)



Legend: R = Read only; W = Write only; - *n* = value after reset; -x, value is indeterminate — see the device-specific data manual

Table 4-91. DDR3_CONFIG_60 Register (0x026204F4) Field Descriptions

Bits	Name	Description
31-20	Reserved	Reset = 0x0 Reserved.
19-0	DATA_ECC_RD_DQS_SLAVE_RATIO	Reset = 0x0000D034 Plug in the effective reg_phy_rd_dqs_slave_ratio value from the PHY calculation spreadsheet for ECC Byte Lane (same for both devices)

Revision History

Changes from D Revision (April 2014) to E Revision **Page**

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