



Mukesh Mahajan

Moraya residency, Kartikeya nagar,
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Career Summary

Dynamic & career-oriented engineering professional having **10+ years of experience** as Assistant Professor of E&TC department skilled in VLSI design, FPGA based system design, Mechatronics, Integrated Circuits and mentoring students in Electronics engineering field. Looking forward for a responsible position in Electronics/IT industry with a view to utilize and enhance my skills and experience towards professional growth.

Technical Skills

- Subject Taught : VLSI Design, Digital Electronics, Control system, Integrated Circuits, Mechatronics, Electrical Circuits and Machines, Computer organization, SPOS, ASIC, SOC, Machine Learning
- Programming Languages : C, C++, Python, VHDL, VERILOG.
- FPGA Design : Xilinx ISE, Vivado, Altera Quartus-II.
- Simulation : XilinxIsim, Modelism simulator
- Verification Languages : System Verilog, UVM
- Operating Systems : Windows family and Linux.
- Certification : C, C++, Software Testing(IBM-Seed Infotech)
Fundamentals of Python (Amity future academy)
Python for Machine Learning (Great Learning)
Machine Learning (Tata steel e-learning academy)
- Tools : Xilinx ISE, Vivado, Altera Quartus-II, Cadence

Educational and Professional Credentials

- **M. Tech in VLSI Technology** with 7.58 CGPA from Dept. of Electronics, North Maharashtra University, Jalgaon. (2012)
- **B. E. in Electronics and Communication Engineering** with 67% from Pravara Rural Engineering College, Loni (SPPU, Pune).
- H. S. C. with 78.17% from A. S. C. College, Maharashtra board.
- S. S. C. with 87.20% from S. S. Patil Vidya mandir, Maharashtra board.

Work Experience (10+ Years)

- I. **Assistant Professor at Sandip Institute of Technology and Research Centre, Nashik**
July 2012 to present.

Responsibilities & Achievements:

- Conduction of weekly lectures and lab sessions, contributing to student engagement, comprehension and learning objectives.
- Used variety of learning modalities and support materials to facilitate learning process and accentuate presentations, including visual, aural and social learning modalities.

- Evaluated and supervised student activities and performance levels to provide reports on academic progress.
- Successfully handled the position of Training & Placement coordinator, Alumni Coordinator, Industry Institute interaction coordinator.
- Successfully handled the responsibilities of Exam Coordinator, IEI Students chapter coordinator, Earn & Learn Coordinator.
- Received grant of 85,000/- for research project funded by BCUD, SPPU Pune.
- Worked as Internship activity coordinator under MHRD Institute innovation council.
- Organized National Technical Events- Excellence, E-Tantra etc.
- Conducted workshop on FPGA based system design for engineering students.
- Arranged various workshops and lectures for Students prior to the campus drives.
- Organized Webinars for job readiness programs.
- Coordination with central placement cell for executing various placement drives.
- Participating in various administrative and academic tasks as per directions of Management.

II. **Lecturer at S. S. Patil Institute of Technology, Chopada**

July 2009 to July 2010.

Responsibilities:

- Taught diverse student population by employing various learning styles and abilities.
- Evaluated and revised lesson plans and course content to facilitate and moderate classroom discussions and student centered learning.
- Designed and distributed lecture handouts to round out material and increase student understanding.

Academic Projects

- ❖ Project Name : Embedded controller for Unmanned Ground vehicle
 - Client : DRDO, Dighi, Pune
 - Duration : 01/08/2007 to 30/04/2008
 - Programming Language : C
 - Role : Design Engineer
- ❖ Project Name : FPGA Implementation of ARM processor
 - Client : PG Project
 - Duration : 01/07/2011 to 31/05/2012
 - Programming Language : VHDL
 - FPGA : Xilinx spartan-6
 - Role : Design Engineer
- ❖ Project Name : On chip optical interconnect for high performance computing system
 - Client : BCUD, SSPPU, Pune
 - Duration : 01/07/2014 to 31/03/2016
 - Role : Design Engineer

Patents

Item	Titles of Inventions	Names of Inventors	Citizenship of inventors	Dates and registration numbers of applications / awards)
1	Automatic Toll collection Using RF Communication	Prof. M.P.Mahajan Komal Pardesi	Indian	Application No. 2672/MUM/2015 Date of publication 20/01/2017
2	Automatic T-shirt Folding Machine	Prof. M.P.Mahajan Shrishti Prasad Tejal Binnar Monika Tambe	Indian	Application No. 201621043027 Date of publication 22/06/2018
3	Patient alert system wrist watch	Prof. M.P.Mahajan Sheetal Shinde Shubhada Ugale Arti Sonawane	Indian	Application No. 201621043031 Date of publication 22/06/2018
4	Smart refrigerator using internet of things	Prof. M. P. Mahajan Rohit R. Nikam Vivek P. Patil Rahul D. Dond	Indian	Application No. 201621043033 Date of publication 22/06/2018

Publications

- Mukesh P. Mahajan, Pramod Aswale, Vivek Ugale, "FPGA Implementation of ARM Processor", IJAREEIE, Vol 3 Issue 11, pp-13120-13127, Nov 2014
- Mukesh P. Mahajan, Raveena Dua, Jeshmi Dudhat, Sachi Patel, "Tongue operated smart environment for paralytic people, IJIRCCE, Vol-2, Issue 12, pp-7489-7492, Dec-2014
- Mukesh P. Mahajan, P. G. Salunke, Y. M. Gaikwad, V. P. Jagtap, "Design And Simulation of 64 bit ALU", IJARECE, Vol 4 Issue 4, pp-1049-1051, Apr-2015
- Pramod S. Aswale, Mukesh P. Mahajan, Manjul V. Nikumbh, Omkar S. Vaidya, "Implementation of Baugh-Wooley Multiplier and Modified BaughWooley Multiplier Using Cadence (Encounter) RTL", IJSETR, Vol 4 Issue 2, pp-293-298, Feb 2015.
- Aniket R. Yeole, Sapana M. Bramhankar, Monali D. Wani, Mukesh P. Mahajan, "Smart Phone Controlled Robot Using ATMEGA328 Microcontroller", Vol 3 Issue 1, pp-352-356, Jan-2015
- Mukesh. P. Mahajan, Divyank Sunil Deshpande, Ganesh Ramdas Chavan, "PUC measurement system with information portal using GSM & RFID", IJETCR, Vol.4, Issue 2, PP 1-4, March 2016.
- Mukesh P. Mahajan¹, Devyani Badve², Pooja Sonar³, Sayali Sonawane, "Electronic Hand Glove Through Gestures For Verbally Challenged Persons", IJERA, Vol.6, Issue 4, pp-17-19, April-16.
- Prashant G. Salunke, Mukesh P. Mahajan, Gayatri M. Phade, "On Chip Optical Interconnect for High Speed Communication System, IJARCCCE, Vol.5, Issue, pp-17-19, July-16
- M. P. Mahajan, Sheetal N. Shinde, Shubhada B. Ugale, Arti Sonawane, "Review of Patient Alert System", Vol 6, Issue 2, pp 119-121, Feb 2017.
- Mukesh P. Mahajan, Rohit R. Nikam, Vivek P. Patil, Rahul D. Dond "Smart refrigerator using IOT", Vol.2, Issue 3, pp-86-91, March-17
- Mukesh Mahajan, Srishti prasad, Monica tambe, Tejal binnar, Automatic T- shirt Folding Machine", Vol.162, Issue 10, pp-13-16, March-17

Conference Proceedings

- Prashant Ingale, Tanay Dahale, Mukesh P. Mahajan, Pankaj kumar Gautam “Optimized solution for LUT’s in FPGA”, ICNB-2,pp-312-314, 28-29th Dec-2011
- Tanay Dahale, Prashant Ingale, Mukesh P. Mahajan, Pankaj kumar Gautam “Simulation and analysis of silicon nanowire transistor”,ICNB-2,pp-315-317,28-29th Dec-2011
- Pankaj Chaudhari, Mukesh Mahajan, Yogesh Apar, S.G. Galande,“Communication controller for payloads on UGV”,National conference on ETSPC,PP 262-266, dec-2007
- Pankaj Chaudhari, Mukesh Mahajan, Yogesh Apar , “Embedded controller for Robotic vision system”, National level technical fest-VORTICIZM’08, March-2008

Competencies

- ❖ Fast learner, adapt well to changes and pressures in workplace.
- ❖ Work effectively with diverse groups of people.
- ❖ Ambitious and committed to excellence.
- ❖ Ability to meet deadlines under pressure with multiple assignments.
- ❖ Strong decision-making skills with result-oriented approach.
- ❖ Good interpersonal skills.

Personal Details

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| ❖ Birth Date:
17th Jan, 1986 | ❖ Languages Known: English, Hindi and Marathi. |
| ❖ Nationality: Indian | ❖ Hobbies: Listening Music, Net Surfing |
| ❖ Gender: Male | ❖ Preference Location: Willing to relocate. |
| ❖ Marital Status:
Married | ❖ Passport status: J8394478. |
| | ❖ Notice period: 30 days |

Declaration

I confirm that the information provided by me is true to the best of my knowledge.

Place: Nashik
Date:

Signature:
Mr. Mukesh Pandit Mahajan