1.

```
/*
    Name the gates, switches and clocks.
    Number of inputs and outputs
    does not need to be defined for DTYPE
*/

DEVICES D1:DTYPE,
        D2:DTYPE,
        N1:NAND 2,
        C1:CLOCK 8, # Period is a power of 2
        S1:SWITCH 0,
        S2:SWITCH 1,
        S3:SWITCH 0 ;

/* connect inputs and outputs */
CONNECT S1 > D1.SET,
        S1 > D2.SET,
        S2 > D1.DATA,
        S3 > D1.CLEAR,
        S3 > D2.CLEAR,

        C1 > D1.CLK,
        C1 > D2.CLK,

        D1.Q > D2.DATA,
        D2.Q > N1.I1,
        D2.QBAR > N1.I2 ;

/* monitor certain signals */
MONITOR D1.QBAR,
        N1 ;

END
```

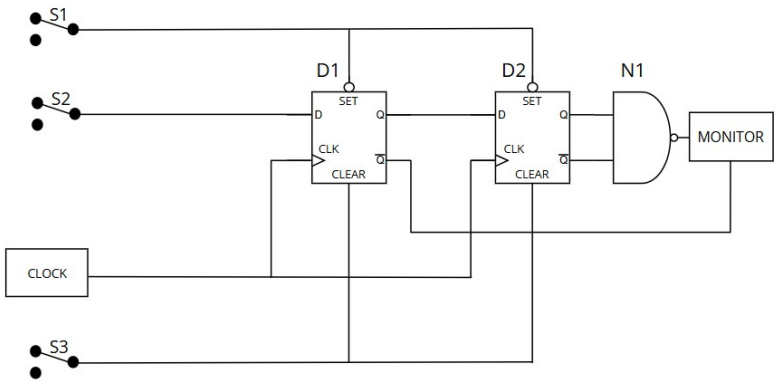


Figure 1: Visual logic circuit design for EBNF (example one) (1)

2.

```
/* This configuration is a full-adder */

/* name all devices */
DEVICES X1:XOR,
        X2:XOR,
        A1:AND 2,
        A2:AND 2,
        NO1:NOR 2,
        O1:OR 2,
        S1:SWITCH 1,
        S2:SWITCH 1,
        S3:SWITCH 0 ;

/* connect inputs and outputs */
CONNECT S1 > X1.I1,
        S1 > A1.I1,
        S2 > X1.I2,
        S2 > A1.I2,
        S3 > X2.I2,
        S3 > A2.I2,
        X1 > X2.I1,
        X1 > A2.I1,
        X2 > NO1.I1,
        A1 > O1.I1,
        A2 > O1.I2,
        O1 > NO1.I2 ;

/* monitor particular signals */
MONITOR X2, # this is the summer bit
        O1, # this is the carry bit
        NO1 ;

END
```

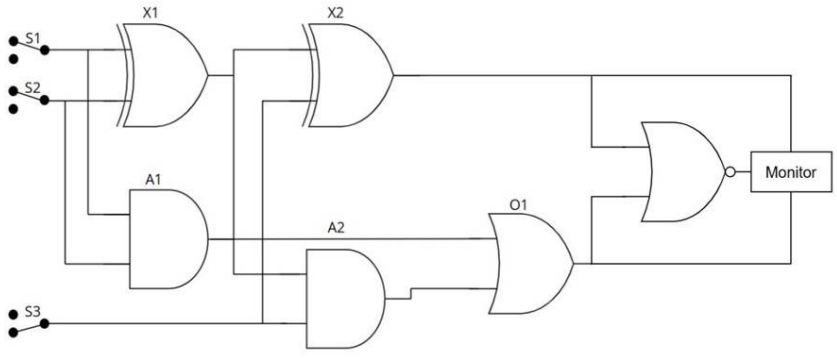
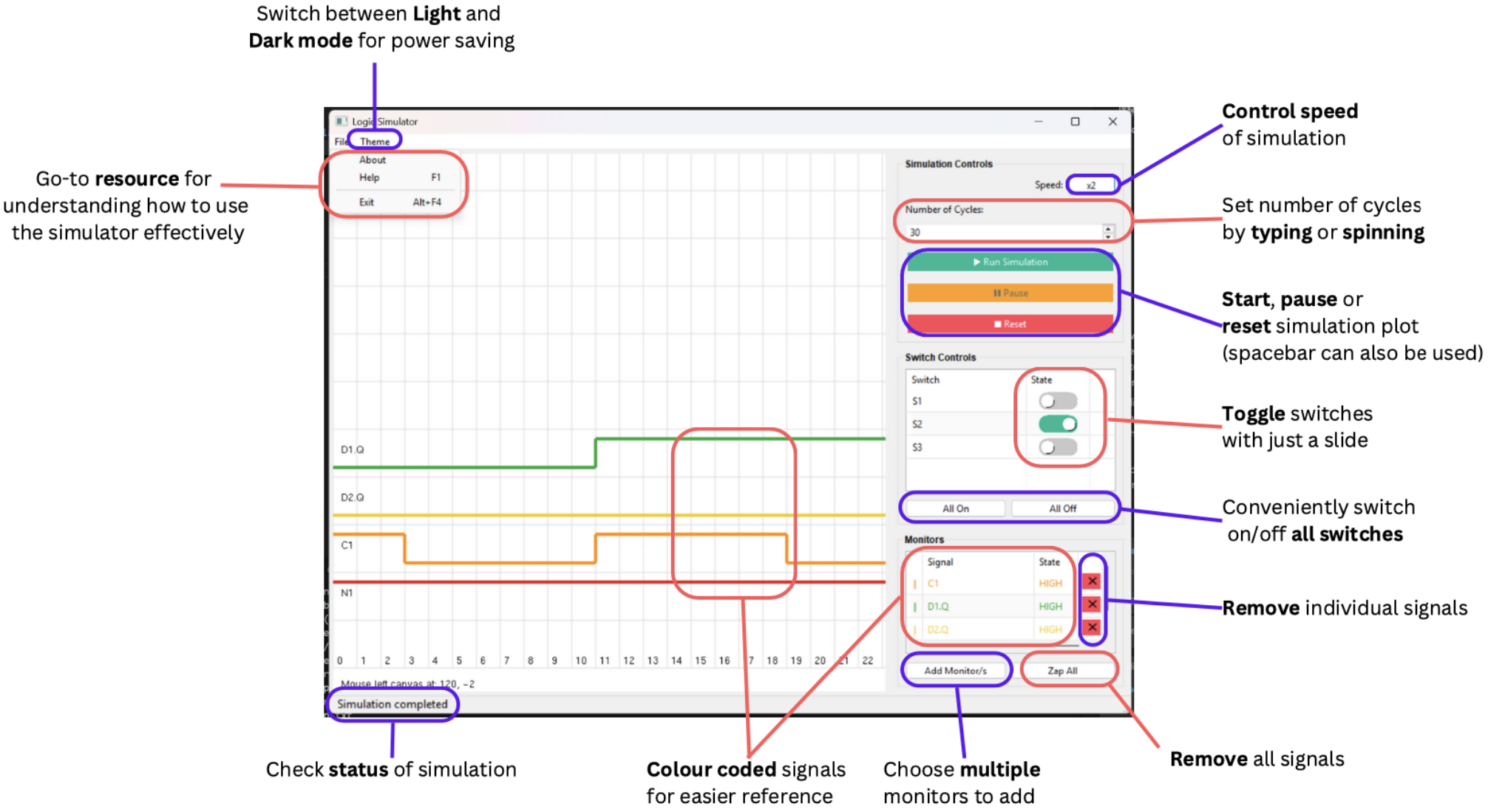


Figure 2: Visual logic circuit design for EBNF (example two) (1)



Simulate your own logic circuit.

1. Clone our repository
2. Change directory to GF2_logic_simulator/logsim
3. Code the circuit using LogicHDL language
4. Run python logsim.py <filename.txt> in the terminal
5. GUI will pop up if successful.
6. Add signals to monitor
7. Start simulation

Simulate a full-adder and a flip flop

1. Clone our repository
2. Change directory to GF2_logic_simulator/logsim
3. In the terminal, you can run these predefined files
   a. python logsim.py full_adder.txt
   b. python logsim.py flip_flop.txt
4. GUI will pop up if successful.
5. Add signals to monitor
6. Start simulation