Industrial Evaluation of DRAM Tests

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Abstract

*This paper presents the results of 44 well known memory tests applied to 1896 1M*4 DRAM chips, using up to 96 different stress combinations with each test. The results show the importance of selecting the right stress combination, and that the theoretically better tests (i.e. those covering more different functional faults) also have a higher fault coverage. However, the currently used fault models still leave much to be explained; e.g., the used data backgrounds and address orders show an unexplainable large variation in fault coverage.*

1. Introduction

DRAM production tests currently are required to have a PPM level which approaches the single digit numbers. This implies that a single memory test is not sufficient; a set of tests has to be used. In addition, in order to obtain economically acceptable test times, the set of tests has to be optimized for the particular technology used, requiring manual optimization of the test set.

Much work has been done on designing memory tests [9] [3] [4] [6] [7] [5], optimized to detect a particular class of faults, which may have an academic origin or is based on inductive fault analysis and SPICE simulation. The question remains as how effective these tests are. [9] has applied a small set of tests to 2K*8 SRAMs and found that the fault coverage was heavily dependent on the used data backgrounds and address orders. [2] reports results of testing 1024 128K*8 SRAM chips using a small number of tests; the results indicated that the fault coverage was heavily dependent on the used stresses such as the load used on the output pins, and/or the power supply voltage. No results have been reported for DRAMs.

This paper presents the results of an *Initial Test Set (ITS)* consisting of 44 tests, applied to 1896 1M*4 DRAM chips [1]. A *test* consists of a *base test (BT)* applied using a particular *stress combination (SC)*. An SC consists of a combination of values for the different *stresses*; e.g.; $V_{DD} = 4.5V$, Temp $= 70^oC$, etc. BTs have been performed with up to 96 different SCs.

The organization of the paper is as follows: Section 2 gives an overview of the used BTs and stresses, Section 3 describes the results of the tests, while Section 4 ends with conclusions.

2. Used base tests and stresses

As already explained in Section 1, a test consists of a base test (BT), applied using a particular stress combination (SC). Section 2.1 gives an overview of the used BTs, the stresses (which are the components of a SC) are described in Section 2.2, and an overview of the used tests is given in Section 2.3.

2.1. Overview of the used base tests

The used set of 42 BTs is composed of BTs from the following classes (The number between brackets shows the number of BTs the class consists of.):

1. Electrical tests (11)
2. March tests (19)
3. Base cell tests (6)
4. Repetitive tests (3)
5. Pseudo-random tests (3)

1. Electrical tests. The class of electrical BTs consists of the contact test, DC parametric and AC parametric tests. The symbol $\Uparrow$ is used to denote the increasing address order (i.e., address 0,1,2, etc.); in addition, the required test time is given behind the name of the BT; n denotes the number of memory words.

1. Contact check: Verifies DUT–memory tester contact
2. Input leakage current high (INP_LKH): Verifies $I_{I(L)-max}$

3. Input leakage current low (INP_LKL): Verifies $I_{I(L)-min}$
4. Output leakage current high (OUT_LKH): Verifies $I_{O(L)-max}$
5. Output leakage current low (OUT_LKL): Verifies $I_{O(L)-min}$
6. Operating current (ICC1): Verifies I_{CC1}
7. Standby current (ICC2): Verifies I_{CC2}
8. Refresh current (ICC3): Verifies I_{CC3}
9. Data retention ($4n + 6t_s$) [Note: t_s is the settling time = 5ms; $Del = 1.2 * t_{REF}$]: {$\Uparrow$ (w$checkerb$);Vcc ← Vcc-min; Del; Vcc ← Vcc-typ; $\Uparrow$ (r$checkerb$)}. Repeat test for data-complement
10. Volatility ($6n + 6t_s$): {$\Uparrow$ (w$checkerb$);Vcc ← Vcc-min; $\Uparrow$ (r$checkerb$); Vcc ← Vcc-typ;$\Uparrow$ (r$checkerb$)}. Repeat test for data-complement
11. Vcc_R/W ($8n + 6t_s$): {Vcc ← Vcc-max; $\Uparrow$ (wd); Vcc ← Vcc-min; $\Uparrow$ (rd); $\Uparrow$ (wd); Vcc ← Vcc-max; $\Uparrow$ (rd)}. Repeat for $d = d^*$

2. March tests. March tests are very popular tests for functional faults such as address decoder faults, coupling faults, etc [5]. The notation used for these tests is as follows: $\Uparrow$ denotes an increasing address order, $\Downarrow$ denotes a decreasing address order, while $\Updownarrow$ denotes that the to be used address order can be chosen arbitrarily to be $\Uparrow$ or $\Downarrow$. Some tests occur in different versions, such as March $C-$ and March $C - R$, because, for experimentation purposes, extra read operations have been added to the march elements. 'D' denotes the delay time for DRFs.

12. Scan ($4n$): $\{\Updownarrow(w0); \Updownarrow(r0); \Updownarrow(w1); \Updownarrow(r1)\}$
13. Mats+ ($5n$): $\{\Updownarrow(w0); \Uparrow(r0, w1); \Downarrow(r1, w0)\}$
14. Mats++ ($6n$): $\{\Updownarrow(w0); \Uparrow(r0, w1); \Downarrow(r1, w0, r0)\}$
15. March A ($15n$): $\{\Updownarrow(w0); \Uparrow(r0, w1, w0, w1);$ $\Uparrow(r1, w0, w1); \Downarrow(r1, w0, w1, w0); \Downarrow(r0, w1, w0)\}$
16. March B ($17n$): $\{\Updownarrow(w0); \Uparrow(r0, w1, r1, w0, r0, w1);$ $\Uparrow(r1, w0, w1); \Downarrow(r1, w0, w1, w0); \Downarrow(r0, w1, w0)\}$
17. March C- ($10n$): $\{\Updownarrow(w0); \Uparrow(r0, w1);$ $\Uparrow(r1, w0); \Downarrow(r0, w1); \Downarrow(r1, w0); \Updownarrow(r0)\}$
18. March C-R ($15n$): $\{\Updownarrow(w0); \Uparrow(r0, r0, w1);$ $\Uparrow(r1, r1, w0); \Downarrow(r0, r0, w1); \Downarrow(r1, r1, w0);$ $\Updownarrow(r0, r0)\}$
19. PMOVI ($13n$): $\{\Downarrow(w0); \Uparrow(r0, w1, r1);$ $\Uparrow(r1, w0, r0); \Downarrow(r0, w1, r1); \Downarrow(r1, w0, r0)\}$
20. PMOVI-R ($17n$): $\{\Downarrow(w0); \Uparrow(r0, w1, r1, r1);$ $\Uparrow(r1, w0, r0, r0); \Downarrow(r0, w1, r1, r1); \Downarrow(r1, w0, r0, r0)\}$
21. March G ($23n + 2D$): $\{\Updownarrow(w0); \Uparrow(r0, w1, r1, w0, r0, w1);$ $\Uparrow(r1, w0, w1); \Downarrow(r1, w0, w1, w0); \Downarrow(r0, w1, w0);$ $D; \Updownarrow(r0, w1, r1); D; \Updownarrow(r1, w0, r0)\}$
22. March U ($13n$): $\{\Updownarrow(w0); \Uparrow(r0, w1, r1, w0);$ $\Uparrow(r0, w1); \Downarrow(r1, w0, r0, w1); \Downarrow(r1, w0)\}$
23. March UD ($13n + 2D$): $\{\Updownarrow(w0); \Uparrow(r0, w1, r1, w0);$ $D; \Uparrow(r0, w1); D; \Downarrow(r1, w0, r0, w1); \Downarrow(r1, w0)\}$
24. March U-R ($15n$): $\{\Updownarrow(w0); \Uparrow(r0, w1, r1, r1, w0);$ $\Uparrow(r0, w1); \Downarrow(r1, w0, r0, r0, w1); \Downarrow(r1, w0)\}$
25. March LR ($14n$): $\{\Updownarrow(w0); \Downarrow(r0, w1);$ $\Uparrow(r1, w0, r0, w1); \Uparrow(r1, w0); \Uparrow(r0, w1, r1, w0);$ $\Downarrow(r0)\}$
26. March LA ($22n$): $\{\Updownarrow(w0); \Uparrow(r0, w1, w0, w1, r1);$ $\Uparrow(r1, w0, w1, w0, r0); \Downarrow(r0, w1, w0, w1, r1);$ $\Downarrow(r1, w0, w1, w0, r0); \Downarrow(r0)\}$
27. March Y ($8n$): $\{\Updownarrow(w0); \Uparrow(r0, w1, r1); \Downarrow(r1, w0, r0); \Updownarrow(r0)\}$
28. WOM ($33n$): Word oriented memory test, designed to detect concurrent coupling faults between bits within a word [8]. $\{\Uparrow_x(w0000, w1111, r1111);$ $\Downarrow_y(r1111, w0000, r0000);$ $\Downarrow_x(r0000, w0111, r0111);$ $\Uparrow_y(r0111, w1000, r1000); \Uparrow_x(r1000, w0000);$ $\Downarrow_x(w1011, r1011); \Downarrow_y(r1011, w0100, r0100);$ $\Uparrow_x(r0110, w0000); \Uparrow_y(w1101, r1101);$ $\Downarrow_x(r1101, w0010, r0010); \Uparrow_x(r0010, w0000);$ $\Downarrow_y(w1110, r1110); \Uparrow_y(r1110, w0001, r0001);$ $\Downarrow_y(r0001)\}$
29. XMOVI ($17n * log_2 n$): Repeat PMOVI for X-address increment $= 2^i$ $(0 \le i \le 9)$
30. YMOVI ($17n * log_2 n$): Repeat PMOVI for Y-address increment $= 2^i$ $(0 \le i \le 9)$

3. Base cell tests. This class of tests has been designed to detect the influence of a disturbance of the base cell on other cells, or vise versa [5]. The following notation is used:

row :address incrementing along row of base cell, skip base cell.
col :address incrementing along column of base cell, skip base cell.
$\diamond$:addressing N,E,S, and W neighbors of base cell.
$w1_b, r0_b$:$w1$ in base cell, $r0$ from base cell.

31. Butterfly ($14n$): $\{\Uparrow(w0); \Uparrow(w1_b, \diamond(r0), w0_b);$ $\Uparrow(w1); \Uparrow(w0_b, \diamond(r1), w1_b)\}$
32. Galcol ($2n + 4n\sqrt{n}$): $\{\Uparrow(w0); \Uparrow(w1_b, col(r0, r1_b), w0_b); \Uparrow(w1);$ $\Uparrow(w0_b, col(r1, r0_b), w1_b)\}$
33. Galrow ($2n + 4n\sqrt{n}$): $\{\Uparrow(w0); \Uparrow(w1_b, row(r0, r1_b), w0_b); \Uparrow(w1);$ $\Uparrow(w0_b, row(r1, r0_b), w1_b)\}$
34. Walkcol ($6n + 2n\sqrt{n}$): $\{\Uparrow(w0); \Uparrow(w1_b, col(r0), r1_b, w0_b); \Uparrow(w1);$ $\Uparrow(w0_b, col(r1), r0_b, w1_b)\}$
35. Walkrow ($6n + 2n\sqrt{n}$): $\{\Uparrow(w0); \Uparrow(w1_b, row(r0), r1_b, w0_b); \Uparrow(w1);$ $\Uparrow(w0_b, row(r1), r0_b, w1_b)\}$
36. SldDiag ($4n\sqrt{n}$): {for each diagonal: w-non-d0, wd1,r;w-non-d1, wd0,r}.

4. Repetitive tests. Repetitive tests perform multiple read or write operations to a single cell; denoted by rx^y or rw^y, whereby the rx or wx operation is repeated y times. Purpose: To make partial fault effects become full fault effects. $\nearrow$ denotes an address increment along the main diagonal.

37. HamRd ($40b$): $\{\Uparrow(w0); \Uparrow(r0, w1, r1^{16}, w0);$
$\Uparrow(w1); \Uparrow(r1, w0, r0^{16}, w1)\}$
38. Hammer ($4n + 2002\sqrt{n}$): $\{\Uparrow(w0);$
$\nearrow(w1_b^{1000}, row(r0), r1_b, col(r0), r1_b, w0_b); \Uparrow(w1);$
$\nearrow(w0_b^{1000}, row(r1), r0_b, col(r1), r0_b, w1_b))\}$
39. HamWr ($4n + 2\sqrt{n}$): $\{\Uparrow(w0);$
$\nearrow(w1_b^{16}, col(r0); w0_b);$
$\Uparrow(w1); row(w0_b^{16}, col(r1); w1_b)\}$

5. Pseudo-random tests. Many types of Pseudo-random (PR) tests exist, depending on whether:

- PR values are used for the addresses, the data, and the read/write signal.
- The number and types of r and w operations in the used march elements.

Note: x denotes number of times the PR test is performed; ? denotes a PR value.

40. PRscan ($x * 4n$): $\{\Uparrow(w?_1); Repeat[\Uparrow(r?_1); \Uparrow(w?_2)]\}$; SCAN test equivalent
41. PRmarch C- ($x * 4n$): $\{\Uparrow(w?_1); Repeat[\Uparrow(r?_1, w?_2)]\}$; March C- equivalent
42. PRPMOVI ($x * 4n$): $\{\Uparrow(w?_1); Repeat[\Uparrow(r?_1, w?_2, r?_2)]\}$; PMOVI equivalent

2.2. Used stresses

A *stress* can be a refinement of a certain operation of a BT (e.g., the address order or the to-be-written data), or can be an external condition applied to the *Device Under Test (DUT)* with the intent to make faults easier detectable. To the latter stress class belong timing, voltage, temperature and load stress. In the evaluation reported in this paper only the typical value for the load is used, it consists of the equivalent of two TTL loads and 100pF.

- Address stress
  - Ax Fast X: Increment column address ($\Uparrow_x$ or $\Downarrow_x$)
  - Ay Fast Y: Increment row address ($\Uparrow_y$ or $\Downarrow_y$)
  - Ac Address complement: Example (000,111,001,110,010,101,011,100)
  - Ai Increment 2^i (For MOVI test)
- Data background stress
  - Ds Solid: All 0s, all 1s
  - Dh Checkerboard: 01010 . . . /1010 . . .
  - Dr Row stripe: 0000 . . . /1111 . . .
  - Dc Column stripe: 0101 . . .
- Timing stress
  - $S-$ MinTime: Use minimum t_{RCD} (RAS to CAS delay)
  - $S+$ MaxTime: Use maximum t_{RCD}
  - Sl Long cycle: $t_{RAS-max}$ (for DRAMs typically 10 msec.) and min t_{RCD}.
- Voltage stress
  - $V-$ Vcc-min $= 4.5V$
  - $V+$ Vcc-max $= 5.5V$
- Temperature stress
  - Tt Typical (25^oC)
  - Tm Max (70^oC)

Table 1. Used tests forming the ITS

\# All Base tests with total test time
\# Results of 1896 DUTs of which 731 fails

# Base test	ID	Cnt	GR	SCs	Time	TotTim
CONTACT	5	1	0	1	0.02	0.02
INP_LKH	20	2	1	1	0.02	0.02
INP_LKL	22	3	1	1	0.02	0.02
OUT_LKH	25	4	1	1	0.02	0.02
OUT_LKL	27	5	1	1	0.02	0.02
ICC1	30	6	2	1	0.04	0.04
ICC2	35	7	2	1	0.04	0.04
ICC3	40	8	2	1	0.04	0.04
DATA_RETENTION	70	9	3	4	0.49	1.97
VOLATILITY	80	10	3	4	0.72	2.89
VCC_R/W	90	11	3	4	0.95	3.81
SCAN	100	12	4	48	0.46	22.15
MATS+	110	13	5	48	0.58	27.68
MATS++	120	14	5	48	0.69	33.22
MARCH_A	130	15	5	48	1.73	83.05
MARCH_B	140	16	5	48	1.96	94.12
MARCH_C-	150	17	5	48	1.15	55.36
MARCH_C-R	155	18	5	32	1.73	55.36
PMOVI	160	19	5	48	1.50	71.97
PMOVI-R	165	20	5	32	1.96	62.75
MARCH_G	170	21	5	48	2.69	128.91
MARCH_U	180	22	5	48	1.50	71.97
MARCH_UD	183	23	5	48	1.53	73.55
MARCH_U-R	186	24	5	32	1.73	55.36
MARCH_LR	190	25	5	48	1.61	77.51
MARCH_LA	200	26	5	48	2.54	121.80
MARCH_Y	210	27	5	48	0.92	44.29
WOM	220	28	6	4	3.92	15.69
XMOVI	230	29	7	16	14.99	239.91
YMOVI	235	30	7	16	14.99	239.91
BUTTERFLY	300	31	8	16	1.61	25.84
GALPAT_COL	310	32	8	1	472.68	472.68
GALPAT_ROW	313	33	8	1	472.68	472.68
WALK1/0_COL	320	34	8	1	236.92	236.92
WALK1/0_ROW	323	35	8	1	236.92	236.92
SLIDDIAG	340	36	8	1	472.45	472.45
HAMMER_R	400	37	9	16	4.61	73.82
HAMMER	410	38	9	16	0.69	10.99
HAMMER_W	420	39	9	16	4.15	66.44
PRSCAN	500	40	10	40	0.46	18.45
PRMARCH_C-	510	41	10	40	0.46	18.45
PRPMOVI	520	42	10	40	0.46	18.45
SCAN_L	650	43	11	8	42.07	336.55
MARCHC-L	660	44	11	8	105.17	841.38
# Total time						4885.48

2.3. Overview of used tests

Table 1 shows the tests which together form the ITS. The column 'Base test' lists the base tests, 'ID' lists the BT number as used by the test programs, 'Cnt' is a sequential number given to the corresponding BT, which is the same number as used for the description of the tests in Section 2.2. 'GR' is the group a BT belongs to (related tests are considered to belong to the same group), 'SCs' lists the number of different SCs used with the corresponding BT, 'Time' is the required execution time for the corresponding BT, 'TotTim' is the total execution time required for executing the corresponding BT for each of the SCs.

Note that the XMOVI and YMOVI tests are identical to the PMOVI tests, whereby additionally the test is repeated a number of times equal to the number of x or y address bits, respectively; with each repetition, the incrementing takes place with a different value of 2^i. For example, for a 3-bit x-address and $i = 1$, the increment is $2^1 = 2$ and the resulting address sequence is: $000, 010, 100, 110, 001, 011, 101, 111$. Note additionally that tests 43 and 44 (Scan-L and MarchC-L) are identical to test 12 and 17, except for the use of the long cycle with $t_{RAS} = 10ms$. (see Section 2.2).

3. Test Results

The tests of Section 2 have been applied with two different values for the temperature stress $T = 25^oC$ (Phase 1) and $T = 70^oC$ (Phase 2). A total of 1896 chips (DUTs) have been tested during Phase 1, while those passing Phase 1 (except for 25 DUTs which had a jam in the handler) entered the Phase 2 tests (Note: Ideally all 1896 DUTs should have been tested in both phases). The tester used was the Advantest T3332 tester. The total test time to perform all tests is $4885s = 1h21m$ per DUT (see Table 1). Considering the fact that the T3332 tester tests 32 DUTs in parallel, this results in a total test time of: $4885{*}1896/(32{*}3600) = 80.4h$ for Phase 1 and $4885 * 1140/(32 * 3600) = 48.5h$ for Phase 2.

The application of the BTs with the different SCs to the 1896 DUTs resulted in a large data base, which had to be simplified for analysis purposes. Therefore the notions of union and intersection have been introduced. The *union* represents the total number of faulty DUTs (faults) detected by a group of tests; the *intersection* represents the set of common faults detected by a group of tests.

Table 2 shows the Phase 1 test results. A *fault* is defined as a DUT which has been identified to be defective. The column 'Uni' lists, for the particular BT, the union of the faults over all applied SCs; e.g., the BT March C- has been applied with 48 different SCs, resulting in a total detection of 234 faults. The column 'Int' list, for the particular BT, the intersection of the faults over all applied SCs; for March C- this is 39. In addition to Uni and Int, Table 2 also has columns denoted by 'U' and 'I'. The column 'U' denotes the number of faults detected for all SCs; whereby one stress has a given value (e.g., of the 48 applied March C- tests, 215 faults were detected for voltage stress $V\ = V- = 4.5V$); similarly 'I' represents the intersection for a given stress (for March C- and $V\ = V- = 4.5V$, this is 39). From Table 2 the most effective BTs and SCs can be determined:

1. The best tests are (see column 'Uni'): March C-L, Scan-L, and March Y.
2. The most effective stresses are (see column-pairs $V-$ through Ac): Ay (fast Y addressing), and Ds (solid data background).
3. The effect of adding extra read operations to the march elements (indicated by the BT suffix '-R') is the following:
   (a) Extra reads added to the beginning of march elements (March C-R, test ID=155): the *fault coverage (FC)* decreased from 234 (for March C-) to 213.
   (b) Extra reads in the middle of march elements (March U-R): The FC decreased from 234 to 217.
   (c) Extra read operations added to the end of march elements (PMOVI-R): The FC increased from 201 to 208. It appears that extra read operations only contribute to the FC when added to the end of the march elements.
4. The effect of delays in the BTs (Del = t_{REF} = 16.4 msec) is as follows: for March UD the FC increases from 234 to 243, and for March G (which is identical to March B, except for the added delays), the FC decreased from 232 to 230. Preliminary conclusion: adding delays increases the FC because of better detection capabilities for DRFs.
5. The results of the pseudo-random tests are not impressive, because they were applied with few SCs and too few repetitions.

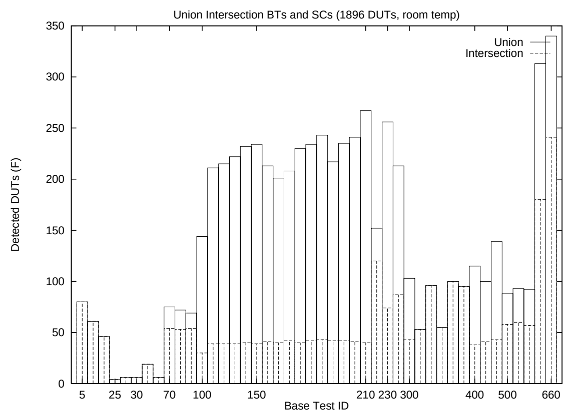

Figure 1. Phase 1 Unions and Intersections per BT.

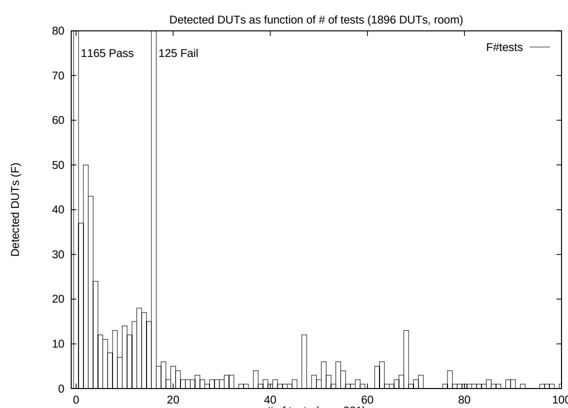

Figure 2. Phase 1 faulty DUTs as function of # tests.

Table 2. Phase 1 Unions and Intersections of BTs and SCs

```
# Union & Intersection of BT & SCs
# Results of 1896 DUTs of which 731 fails
# All tests          1896 DUTs of which 731 failing, Fail%= 38.554852%
#
```

# Base test	ID	GR	Time	SCs	Uni	Int	U V-	V- I	U V+	V+ I	U S-	S- I	U S+	S+ I	U Ds	Ds I	U Dh	Dh I	U Dr	Dr I	U Dc	Dc I	U Ax	Ax I	U Ay	Ay I	U Ac	Ac I
CONTACT	5	0	0.020	1	80	80	80	80	0	0	80	80	0	0	80	80	0	0	0	0	0	0	80	80	0	0	0	0
INP_LKH	20	1	0.020	1	61	61	61	61	0	0	61	61	0	0	61	61	0	0	0	0	0	0	61	61	0	0	0	0
INP_LKL	22	1	0.020	1	46	46	46	46	0	0	46	46	0	0	46	46	0	0	0	0	0	0	46	46	0	0	0	0
OUT_LKH	25	1	0.020	1	4	4	4	4	0	0	4	4	0	0	4	4	0	0	0	0	0	0	4	4	0	0	0	0
OUT_LKL	27	1	0.020	1	6	6	6	6	0	0	6	6	0	0	6	6	0	0	0	0	0	0	6	6	0	0	0	0
ICC1	30	2	0.040	1	6	6	6	6	0	0	6	6	0	0	6	6	0	0	0	0	0	0	6	6	0	0	0	0
ICC2	35	2	0.040	1	19	19	19	19	0	0	19	19	0	0	19	19	0	0	0	0	0	0	19	19	0	0	0	0
ICC3	40	2	0.040	1	6	6	6	6	0	0	6	6	0	0	6	6	0	0	0	0	0	0	6	6	0	0	0	0
DATA_RETENTION	70	3	0.491	4	75	54	73	59	68	54	70	61	65	58	75	54	0	0	0	0	0	0	75	54	0	0	0	0
VOLATILITY	80	3	0.722	4	72	53	70	56	71	54	69	63	62	57	72	53	0	0	0	0	0	0	72	53	0	0	0	0
VCC_R/W	90	3	0.953	4	69	54	67	55	68	54	65	63	59	57	69	54	0	0	0	0	0	0	69	54	0	0	0	0
SCAN	100	4	0.461	48	144	30	124	33	128	31	137	31	136	35	97	38	66	32	116	38	53	34	75	31	120	32	85	33
MATS+	110	5	0.577	48	211	39	197	39	182	39	205	41	193	41	179	51	128	39	109	43	58	39	108	39	184	39	109	40
MATS++	120	5	0.692	48	215	39	203	39	183	40	209	42	195	42	182	52	121	40	117	44	60	39	111	40	180	40	110	39
MARCH_A	130	5	1.730	48	222	39	206	39	193	39	211	41	205	42	186	52	126	39	144	43	64	39	119	40	202	40	113	39
MARCH_B	140	5	1.961	48	232	40	214	40	196	40	218	42	206	45	185	54	141	40	147	45	68	40	121	40	210	42	116	40
MARCH_C-	150	5	1.153	48	234	39	215	39	200	39	229	41	202	44	198	57	142	39	125	44	66	40	119	40	213	41	111	39
MARCH_C-R	155	5	1.730	32	213	41	195	41	185	42	207	43	187	45	178	60	133	42	129	45	66	42	123	41	205	42	0	0
PMOVI	160	5	1.499	48	201	40	185	40	178	41	194	42	185	44	189	55	105	42	131	46	98	42	105	40	170	60	109	41
PMOVI-R	165	5	1.961	32	208	42	187	42	189	42	194	44	192	45	186	60	127	42	141	47	112	43	107	42	192	73	0	0
MARCH_G	170	5	2.686	48	230	40	208	40	206	41	225	42	204	44	188	55	136	41	145	45	64	40	124	40	205	42	117	41
MARCH_U	180	5	1.499	48	234	42	219	42	201	43	222	45	215	45	191	63	128	42	150	46	71	44	133	43	210	44	120	42
MARCH_UD	183	5	1.532	48	243	43	224	43	213	43	238	46	211	46	199	67	151	44	155	48	72	45	140	43	221	44	128	45
MARCH_U-R	186	5	1.730	32	217	42	200	42	197	43	210	44	201	45	176	64	117	42	148	45	66	43	133	42	204	43	0	0
MARCH_LR	190	5	1.615	48	235	42	217	42	209	42	229	44	206	45	197	66	140	42	150	45	66	43	130	42	216	42	121	42
MARCH_LA	200	5	2.538	48	241	41	216	41	210	42	228	44	213	44	198	59	145	41	141	47	74	42	125	41	220	44	117	42
MARCH_Y	210	5	0.923	48	267	40	250	40	212	42	234	43	239	44	222	54	144	41	128	45	59	41	116	40	240	42	112	41
WOM	220	6	3.922	4	152	120	140	125	145	128	141	126	145	126	152	120	0	0	0	0	0	0	152	120	0	0	0	0
XMOVI	230	7	14.995	16	256	74	226	75	237	86	251	80	237	78	209	148	164	106	172	124	150	108	256	74	0	0	0	0
YMOVI	235	7	14.995	16	213	87	195	93	195	92	209	91	188	93	193	141	138	102	173	132	133	98	0	0	213	87	0	0
BUTTERFLY	300	8	1.615	16	103	43	101	43	85	43	94	45	95	46	99	69	55	43	67	48	55	45	103	43	0	0	0	0
GALPAT_COL	310	8	472.677	1	53	53	0	0	53	53	0	0	53	53	0	0	0	0	0	0	53	53	53	53	0	0	0	0
GALPAT_ROW	313	8	472.677	1	96	96	0	0	96	96	0	0	96	96	0	0	0	0	0	0	96	96	96	96	0	0	0	0
WALK1/0_COL	320	8	236.915	1	55	55	0	0	55	55	0	0	55	55	0	0	0	0	0	0	55	55	55	55	0	0	0	0
WALK1/0_ROW	323	8	236.915	1	100	100	0	0	100	100	0	0	100	100	0	0	0	0	0	0	100	100	100	100	0	0	0	0
SLIDDIAG	340	8	472.446	1	95	95	0	0	95	95	0	0	95	95	0	0	0	0	0	0	95	95	95	95	0	0	0	0
HAMMER_R	400	9	4.614	16	115	38	111	38	99	44	109	41	101	46	100	64	60	45	99	71	62	45	115	38	0	0	0	0
HAMMER	410	9	0.687	16	100	41	94	42	89	44	92	43	90	47	77	57	57	43	89	67	57	43	100	41	0	0	0	0
HAMMER_W	420	9	4.152	16	139	43	129	43	124	44	134	45	126	50	83	60	69	51	129	95	60	45	139	43	0	0	0	0
PRSCAN	500	10	0.461	40	88	58	84	61	78	60	83	61	72	65	88	58	0	0	0	0	0	0	88	58	0	0	0	0
PRMARCH_C-	510	10	0.461	40	93	60	88	60	82	62	89	62	74	66	93	60	0	0	0	0	0	0	93	60	0	0	0	0
PRPMOVI	520	10	0.461	40	92	57	84	58	79	61	85	60	75	65	92	57	0	0	0	0	0	0	92	57	0	0	0	0
SCAN_L	650	11	42.069	8	313	180	304	215	283	183	0	0	313	180	286	251	249	211	288	237	246	210	313	180	0	0	0	0
MARCHC-L	660	11	105.172	8	340	241	331	271	309	246	0	0	340	241	319	282	298	252	318	281	292	255	340	241	0	0	0	0
# Total					731	0	678	0	617	27	470	0	655	28	652	0	519	31	496	35	475	29	645	0	378	31	140	32

Figure 1 shows the Phase 1 unions (the solid bars) and the intersections (the dashed bars) per BT (indicated by ID number, see Table 1); it is a graphical representation of the columns 'Uni' and 'Int' of Table 2. The figure shows the high FC of the '-L' tests (Scan-L and March C-L); while the large difference between the unions and intersections per BT indicates the importance of the SC. For example, for March Y the FC varies between 250 (for V=$V-$) to 112 (for A=Ac); actually, the FC varies even more drastically, from 181 (for $AyDsS{+}V{-}Tt$) to 45 (for $AcDcS{-}V{+}Tt$, as well as for $AcDcS{+}V{-}Tt$), when individual SCs are taken into account (not shown in Figure 1).

Figure 2 shows the FC on the Y-axis versus the #-of-tests the faulty DUTs are detected with. E.g., 0 tests find faults in 1185 DUTs (those DUTs pass Phase 1), 37 DUTs have been detected by a single test each (Denoted as *single faults*), 50 faulty DUTs have been detected by two tests (Denoted as *pair faults*), etc. The 37 DUTs detected by a single test are interesting to analyze, because these tests will be required in order to get a FC of 100%.

Table 3 shows the Phase 1 tests which detect single faults, together with the SC for which the faulty DUT was detected; for the 20 tests a total test time of 1270 sec. is required. Note that March Y is the only march test in the table; it uniquely identifies 16 faulty DUTs; this indicates that the march tests cover similar faults.

Of the 731 faults detected in Phase 1, 37 have been detected only by a single test (see Figure 2 and Table 3), while 50 have been detected by two tests; see Table 4. Note that the 50 DUTs which have been identified as being faulty by two different tests each; such that the total number of detected faults is 100, as shown in Table 4. Of the list of 38 tests, 11 tests also appear in Table 3; they are marked with an '*'. Note that of the 38 tests, the contribution of the march tests to the FC is very low (only MarchC- and MarchY are pure march tests!). The nonlinear tests (marked with 'N') detect a total of 43 faults and the long tests (marked with 'L') detect a total of 13 faults. Note that the SCs for the singles and fault pairs show a large variation, indicating that for a high FC the ITS should include many SCs.

Figure 3 shows the FC as a function of the test time for different optimization algorithms. The Remove Hardest 'RemHdt' algorithm has the best performance (therefore

Table 3. Phase 1 tests which detect single faults

```
# tests (BT SC combination) which detect Single faults
# Results of 1896 DUTs of which 731 fails
# Base test       ID GR    Time SC:         Cnt
        CONTACT   5  0    0.02 AxDsS-V-Tt    1
        INP_LKH  20  1    0.02 AxDsS-V-Tt    2
           ICC2  35  2    0.04 AxDsS-V-Tt    1
           SCAN 100  4    0.46 AxDrS+V-Tt    1
        PMOVI-R 165  5    1.96 AyDrS-V+Tt    1
        MARCH_G 170  5    2.69 AyDhS-V-Tt    2
        MARCH_Y 210  5    0.92 AyDsS+V-Tt   16
        MARCH_Y 210  5    0.92 AyDhS-V-Tt    1
          XMOVI 230  7   14.99 AxDsS-V-Tt    1
          XMOVI 230  7   14.99 AxDsS-V+Tt    1
          XMOVI 230  7   14.99 AxDcS-V+Tt    1
    WALK1/0_ROW 323  8  236.92 AxDcS+V+Tt    1
       SLIDDIAG 340  8  472.45 AxDcS+V+Tt    1
       HAMMER_W 420  9    4.15 AxDrS-V+Tt    1
         SCAN_L 650 11   42.07 AxDhS+V-Tt    1
         SCAN_L 650 11   42.07 AxDrS+V-Tt    1
       MARCHC-L 660 11  105.17 AxDhS+V-Tt    1
       MARCHC-L 660 11  105.17 AxDrS+V-Tt    1
       MARCHC-L 660 11  105.17 AxDrS+V+Tt    1
       MARCHC-L 660 11  105.17 AxDcS+V+Tt    1
# Totals                1270.36             37
```

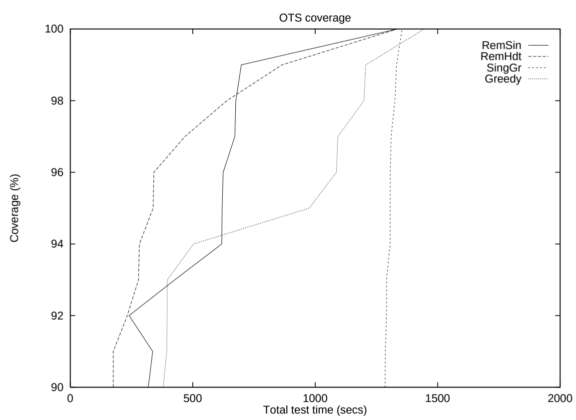

Figure 3. Phase 1 optimizations

the others will not be discussed); it first removes those single faults which require the longest test time to detect (are the Hardest), then it removes pairs of faults which are hardest to detect, etc. A graph like this can be used to make an economical trade off between the FC and the test time (=test cost).

Table 5 shows the intersections of the unions of the groups; column 'GR' of Table 1 shows which tests belong to which group. The diagonal entries show the total FC of each group; non-diagonal entries show the intersections. The largest contributions to the total FC of 731 are: Group 5 (march tests) FC=372, group 11 (the '-L' tests) FC=342, and group 7 (the XMOVI and YMOVI tests) FC=282. From row or column 11 one can see that of the 342 faults detected by the '-L' tests, few faults are detected by tests of any of the other groups. This could be expected because of the unique timing used with the '-L' tests (see Section 2.2). From Table 5 one can see that the march tests (group 5) have a total FC of 372, and the scan test (group 4) of 144; the intersection of groups 4 and 5 is 141, which means that the march tests almost completely cover the scan test.

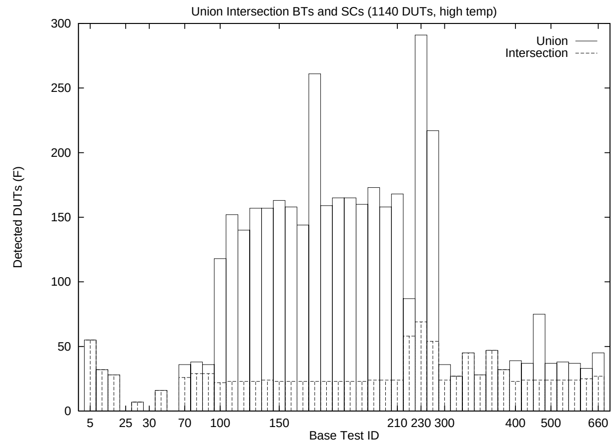

Figure 4. Phase 2 Union and Intersection per BT

Figure 4 is the Phase 2 equivalent of Figure 1. The difference between the union and intersection values per BT is even more striking; indicating that the used SC is even more important for tests with $T = Tm = 70^oC$. Also note the high FCs for MOVI tests (test IDs 165, 230 and 235, see Table 1). Note furthermore that the '-L' tests (test IDs 650 and 660) have a relative low FC; probably due to the fact that DUTs which exhibited leakage have already been detected and eliminated in Phase 1. The most effective tests are XMOVI, PMOVI-R and YMOVI.

Table 6 shows the Phase 2 tests which detect single faults (it is the Phase 2 equivalent of Table 3). A total of 32 DUTs have been found faulty by a single test each. Note that of the list of 13 tests only 2 tests (March U and March Y) are regular march tests; the single most effective test is MOVI and its variants. When comparing Table 6 and Table 3, one can conclude that for Phase 2 ($T = 70^oC$) fewer test are required (13) to detect all single faults, and that in addition, the test time is much shorter; 55 sec. versus 1270 sec. Similarly, Table 7 shows the Phase 2 equivalent of Table 4; it consists of 22 tests (as compared with 38 for Table 4; i.e., Phase 1), it detects 29 faults (as compared with 50 for Phase 1) and requires a test time of 220 sec. (as compared with 2104 sec. for Phase 1). From this one can conclude that testing at $T = 70^oC$ is more effective than at room temperature.

Table 8 shows the FC of some of the BTs; they have been placed in the order of increasing fault detection capabilities, based on theoretical expectations [5]. From the Phase 1 'Uni' column, which has been taken from Table 2,

Table 8. Fault coverage of BTs ordered according to theoretical expectations

	Phase 1 results: $T = 25^o C$				Phase 2 results: $T = 70^o C$			
BT	Uni	Int	Max	Min	Uni	Int	Max	Min
Scan	144	30	67: $AcDsS$–V–	38: $AcDhS$–V+	118	22	105:$AyDrS$–V+	25: $AxDcS$+V–
Mats+	211	39	140:$AyDsS$–V+	44: $AyDhS$+V–	152	23	109:$AyDrS$–V+	24: $AcDhS$+V–
Mats++	215	39	137:$AyDsS$–V+	43: $AcDcS$–V+	140	23	98:$AyDrS$–V+	23: $AcDhS$+V–
March Y	267	40	181:$AyDsS$+V–	45: $AcDcS$–V+	168	24	113:$AyDrS$–V+	24: $AcDhS$+V–
March C-	234	39	155:$AyDsS$–V+	45: $AcDhS$–V+	163	23	119:$AyDrS$–V+	23: $AcDhS$+V–
March U	234	42	154:$AyDsS$–V+	48: $AcDhS$–V+	165	23	123:$AyDrS$–V+	23: $AcDhS$+V–
PMOVI	201	40	138:$AyDsS$–V+	46: $AcDcS$–V+	144	23	113:$AyDs$	23: $AcDhS$+V–
March A	222	39	143:$AyDsS$+V–	44: $AcDcS$–V+	157	23	118:$AyDrS$–V+	25: $AcDhS$+V–
March B	232	40	144:$AyDsS$+V–	44: $AcDcS$–V+	157	24	111:$AyDrS$–V+	24: $AcDhS$+V–
March LR	235	42	155:$AyDsS$–V+	48: $AcDcS$–V+	173	24	126:$AyDrS$–V+	24: $AcDhS$+V–
March LA	241	41	157:$AyDsS$–V+	47: $AcDcS$–V+	158	24	108:$AyDrS$–V+	24: $AcDhS$+V–

one can conclude that the industrial results correspond with the theoretically expected results. This with the exception of March Y [5] which, for unclear reasons, does better; and for PMOVI which does worse. The Phase 1 column 'Max' shows the BT–SC combination with the highest FC; again here the industrial results are according to the theoretical expectations, except again for March Y and PMOVI. Note that the max FC is consistently obtained for SC =$AyDs$ (fast Y addressing and solid data). The Phase 1 'Min' FC is almost identical for all BTs and occurs for SC =$AcDcS$–V+. The column 'Uni' for the Phase 2 results shows a more irregular picture as what one would predict based on the theory, however, the 'Max' FC is consistently obtained for SC =$AyDrS$–V+. The 'Int' results are almost identical for all BTs and the 'Min' FC is consistently obtained for SC =$AcDhS$+V–.

4. Conclusions

This paper summarizes the results of applying 42 base tests, each with up to 96 different stress conditions; resulting in a total of 1962 tests applied to 1896 chips. From this the following can be concluded:

- The most effective Phase 1 BTs are: the tests using the long timing (Scan-L and March C-L), likely due to cell leakage, and March Y; for Phase 2 they are XMOVI, PMOVI-R, and YMOVI (They all belong to the class of MOVI tests, indicating that the X and Y decoder paths are very timing critical).
- The FC for a given BT depends to a large extent on the used SC; hence, the determination of the most effective SC is very important. This is especially true for the tests which detect singles and pair faults.
- The Ac (address complement) address stress consistently scores worst; this indicates that faults are most likely between neighbor cells in the same row or column.
- BTs can be put in groups. From the FC at the group level (Table 5) one can conclude that many of the groups (such as the groups with the MOVI and the '-L' tests) cover faults of a specific class.
- Tests performed at a high temperature ($T = 70^o C$) are more efficient; in order to detect single and pair faults, a significant fewer number of tests are required with a significant reduction in test time.
- The SC which results in the highest FC for Phase 1 is $AyDsS$–V+ or $AyDsS$+V–, and applies to all tests; for Phase 2 it is $AyDrS$–V+ for all tests (see Table 8). The lowest FC for Phase 1 is $AcDcS$–V+ and for Phase 2 it is $AcDhS$+V–; this indicates that Ac (address complement addressing) and Dh (the checkerboard data background) consistently produce the lowest FC.
- Variations on existing BTs increase the FC; when read operations are added to the end of the march elements, or when delays are added to the tests.
- In order to reduce the test time to an economically acceptable number (which is about 120 sec.) the nonlinear tests have to be eliminated. This requires a better understanding of the detected faults such that linear tests optimized for the specific faults can be designed.
- It has been shown that the tests with the most promising FC, based on what could be expected from the theory, also have the highest FC in practice. However, much still needs to be explained.
- No theoretical base exists to model stresses and predict the FC of a given SC; this still is a research topic.
- Last: The results have been obtained for the DRAM chips of [1]. For other chips, different results can be expected because of differences in design and fabrication process.

References

[1] Fujitsu limited. *Fujitsu Semiconductor Data Sheet, CMOS 1Mx4 Bit Fast Page Mode DRAM.*

Table 4. Phase 1 tests which detect pair faults

tests (BT SC combination) which detect Pair faults
Results of 1896 DUTs of which 731 fails

# Base test	ID	GR	Time	SC:	Cnt
CONTACT	5	0	0.02	AxDsS-V-Tt	11*
INP_LKH	20	1	0.02	AxDsS-V-Tt	12*
OUT_LKH	25	1	0.02	AxDsS-V-Tt	1
DATA_RETENTION	70	3	0.49	AxDsS+V-Tt	1
MARCH_C-	150	5	1.15	AyDhS-V-Tt	1
MARCH_UD	183	5	1.53	AyDsS-V+Tt	1
MARCH_UD	183	5	1.53	AyDhS-V-Tt	1
MARCH_UD	183	5	1.53	AyDhS-V+Tt	1
MARCH_LR	190	5	1.61	AyDhS-V-Tt	1
MARCH_Y	210	5	0.92	AyDsS-V+Tt	4
MARCH_Y	210	5	0.92	AyDsS+V-Tt	5*
MARCH_Y	210	5	0.92	AyDhS-V-Tt	1*
XMOVI	230	7	14.99	AxDsS-V+Tt	2 N
XMOVI	230	7	14.99	AxDsS+V+Tt	2 N
XMOVI	230	7	14.99	AxDhS-V+Tt	4 N
XMOVI	230	7	14.99	AxDhS+V+Tt	4 N
XMOVI	230	7	14.99	AxDcS-V+Tt	1 N
XMOVI	230	7	14.99	AxDcS+V+Tt	1 N
YMOVI	235	7	14.99	AyDsS-V-Tt	1 N
YMOVI	235	7	14.99	AyDsS+V-Tt	1 N
YMOVI	235	7	14.99	AyDrS-V-Tt	1 N
YMOVI	235	7	14.99	AyDrS+V-Tt	1 N
BUTTERFLY	300	8	1.61	AxDsS-V-Tt	1
BUTTERFLY	300	8	1.61	AxDsS+V-Tt	1
GALPAT_ROW	313	8	472.68	AxDcS+V+Tt	12 N
WALK1/0_ROW	323	8	236.92	AxDcS+V+Tt	12*N
SLIDDIAG	340	8	472.45	AxDcS+V+Tt	1*N
PRMARCH_C-	510	10	0.46	AxDsS-V+Tt	1
PRPMOVI	520	10	0.46	AxDsS-V+Tt	1
SCAN_L	650	11	42.07	AxDhS+V-Tt	1*L
SCAN_L	650	11	42.07	AxDrS-V-Tt	1*L
SCAN_L	650	11	42.07	AxDrS+V+Tt	1 L
MARCHC-L	660	11	105.17	AxDsS+V-Tt	3 L
MARCHC-L	660	11	105.17	AxDhS+V-Tt	1*L
MARCHC-L	660	11	105.17	AxDhS+V+Tt	1 L
MARCHC-L	660	11	105.17	AxDrS+V-Tt	3*L
MARCHC-L	660	11	105.17	AxDrS+V+Tt	1*L
MARCHC-L	660	11	105.17	AxDcS+V-Tt	1 L
# Totals			2104.06		100

[2] S. N. H. Goto and K. Iwasaki. Experimental fault analysis of 1Mb SRAM chips. *Proc. 15th IEEE VLSI Test Symposium*, pages 31–36, 1997.

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Table 5. Phase 1 Intersection of Unions of groups.

Intersection of group Unions
Results of 1896 DUTs of which 731 fails

# GR	0	1	2	3	4	5	6	7	8	9	10	11
0	80	58	8	25	26	34	28	29	25	25	24	30
1	58	67	8	8	10	19	14	15	10	11	9	15
2	8	8	19	14	14	15	15	15	16	15	15	16
3	25	8	14	78	70	74	61	70	69	69	52	57
4	26	10	14	70	144	141	86	125	97	109	63	75
5	34	19	15	74	141	372	132	240	135	142	76	108
6	28	14	15	61	86	132	152	133	97	97	86	74
7	29	15	15	70	125	240	133	282	132	145	77	102
8	25	10	16	69	97	135	97	132	161	120	75	85
9	25	11	15	69	109	142	97	145	120	157	76	88
10	24	9	15	52	63	76	86	77	75	76	102	63
11	30	15	16	57	75	108	74	102	85	88	63	342

Table 6. Phase 2 tests which detect single faults

tests (BT SC combination) which detect Single faults
Results of 1140 DUTs of which 475 fails

# Base test	ID	GR	Time	SC:	Cnt
CONTACT	5	0	0.02	AxDsS-V-Tm	2
INP_LKH	20	1	0.02	AxDsS-V-Tm	1
INP_LKL	22	1	0.02	AxDsS-V-Tm	1
ICC2	35	2	0.04	AxDsS-V-Tm	5
PMOVI-R	165	5	1.96	AyDsS+V+Tm	3
PMOVI-R	165	5	1.96	AyDhS+V+Tm	1
PMOVI-R	165	5	1.96	AyDrS+V-Tm	5
PMOVI-R	165	5	1.96	AyDrS+V+Tm	2
MARCH_U	180	5	1.50	AyDhS+V-Tm	1
MARCH_Y	210	5	0.92	AyDsS+V-Tm	6
XMOVI	230	7	14.99	AxDcS-V+Tm	1
YMOVI	235	7	14.99	AyDhS-V+Tm	1
YMOVI	235	7	14.99	AyDrS-V+Tm	3
# Totals			55.35		32

Table 7. Phase 2 tests which detect pair faults

tests (BT SC combination) which detect Pair faults
Results of 1140 DUTs of which 475 fails

# Base test	ID	GR	Time	SC:	Cnt
CONTACT	5	0	0.02	A1D1S1V1T2	8
INP_LKH	20	1	0.02	A1D1S1V1T2	8
MARCH_C-	150	5	1.15	A1D3S2V2T2	1
MARCH_C-	150	5	1.15	A1D4S1V2T2	1
MARCH_C-	150	5	1.15	A2D3S1V2T2	1
PMOVI-RD	165	5	1.96	A2D1S1V2T2	6
PMOVI-RD	165	5	1.96	A2D1S2V2T2	7
PMOVI-RD	165	5	1.96	A2D3S2V2T2	1
PMOVI-RD	165	5	1.96	A2D4S1V2T2	2
PMOVI-RD	165	5	1.96	A2D4S2V2T2	2
MARCH_LR	190	5	1.61	A2D3S1V2T2	1
MARCH_Y	210	5	0.92	A2D1S1V2T2	1
MARCH_Y	210	5	0.92	A2D1S2V1T2	2
XMOVI	230	7	14.99	A1D3S1V2T2	2
XMOVI	230	7	14.99	A1D3S2V2T2	1
XMOVI	230	7	14.99	A1D4S1V2T2	3
XMOVI	230	7	14.99	A1D4S2V2T2	2
YMOVI	235	7	14.99	A2D3S1V2T2	2
YMOVI	235	7	14.99	A2D3S2V2T2	2
HAMMER_WT	420	9	4.15	A1D3S1V2T2	2
HAMMER_WT	420	9	4.15	A1D3S2V2T2	2
MARCHC-LNG	660	11	105.17	A1D3S2V1T2	1
# Totals			220.21		58