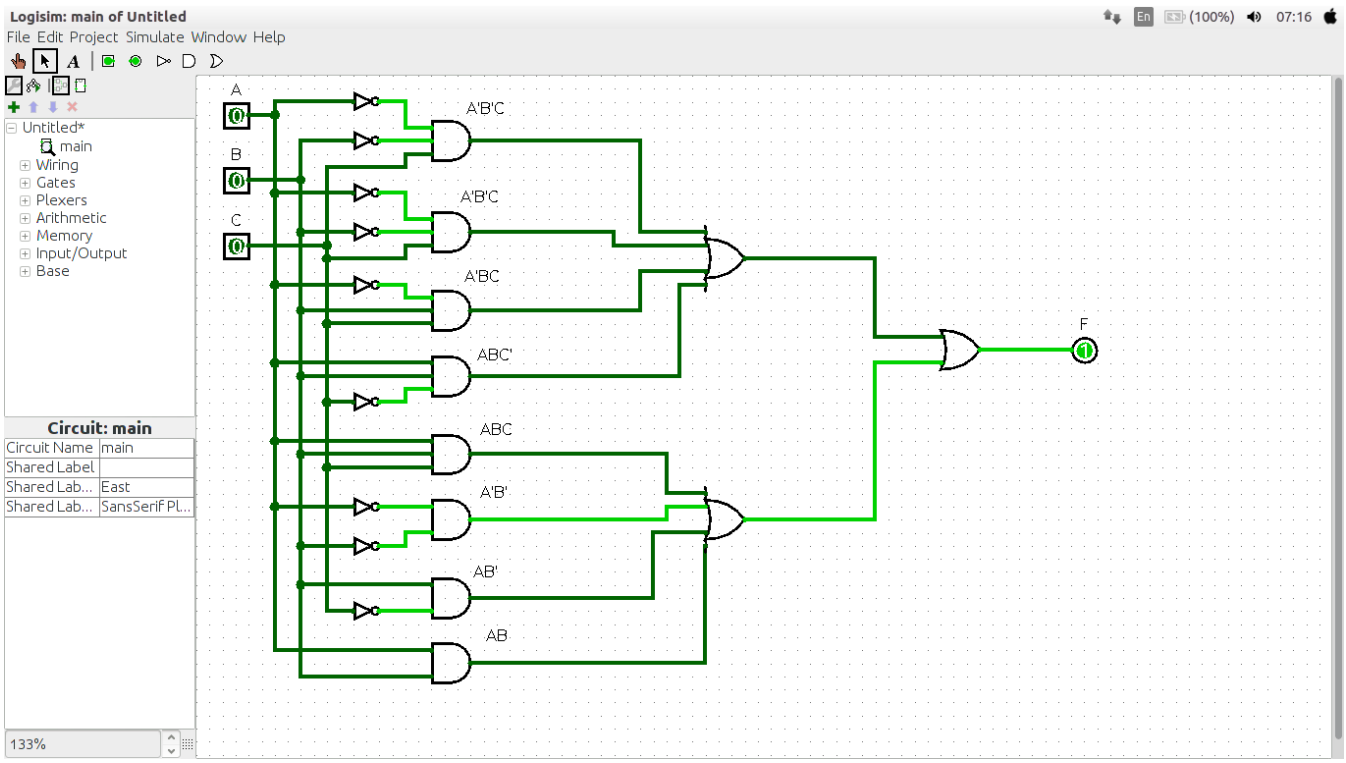
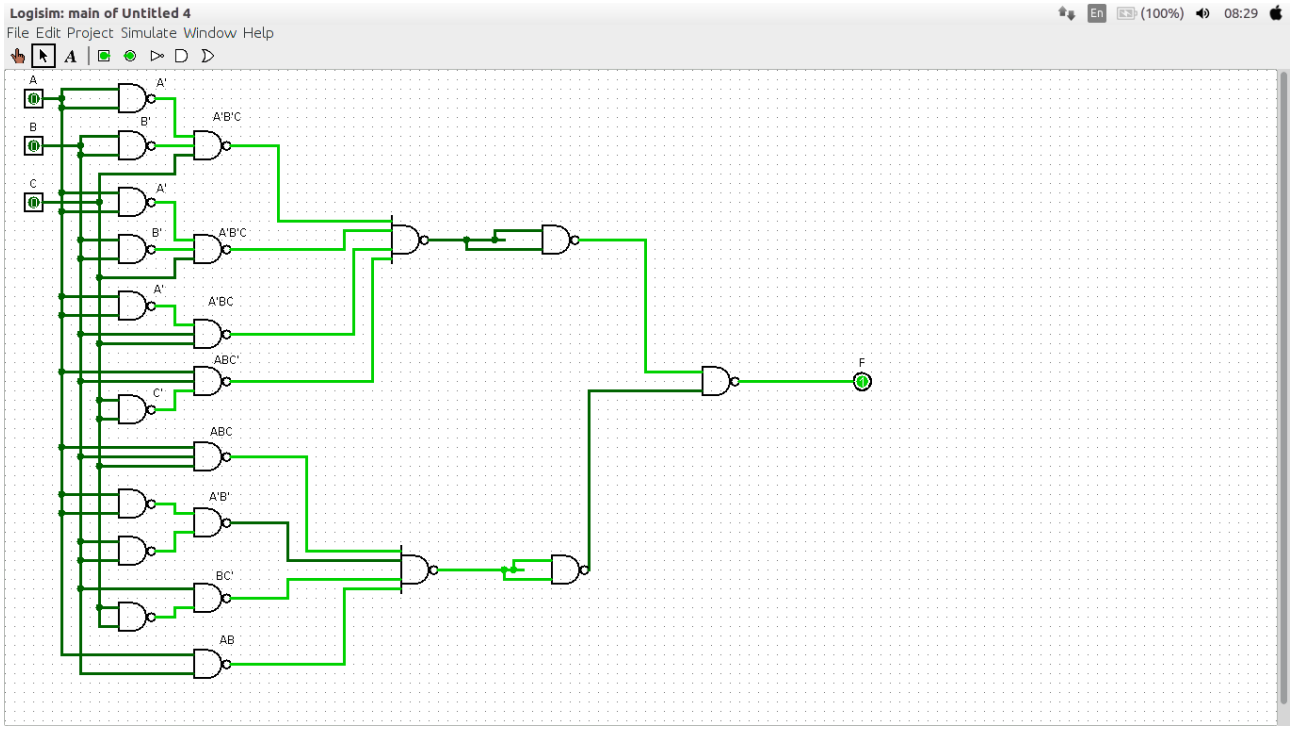
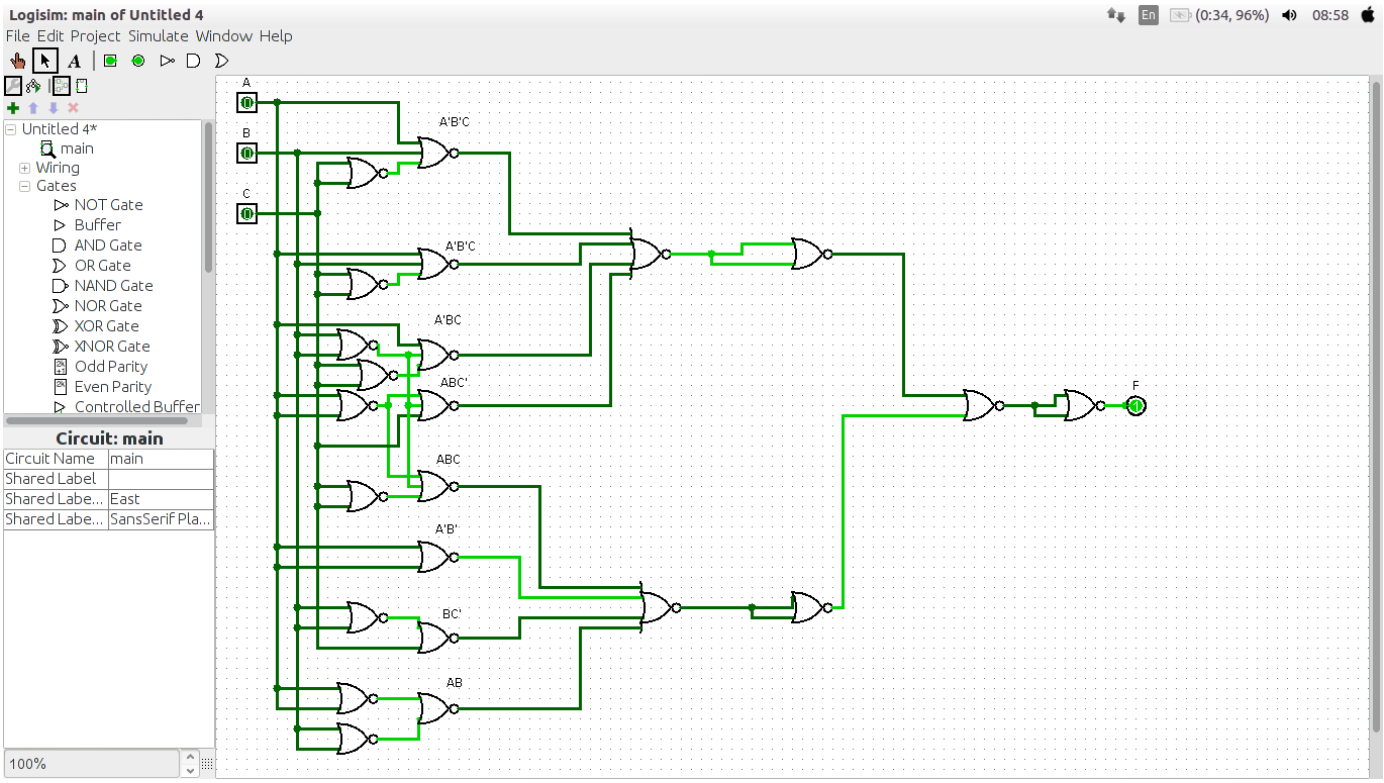
Lab : 1

F1 = A’B’C+A’B’C+A’BC+ABC’+ABC+A’B’+BC’+AB

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

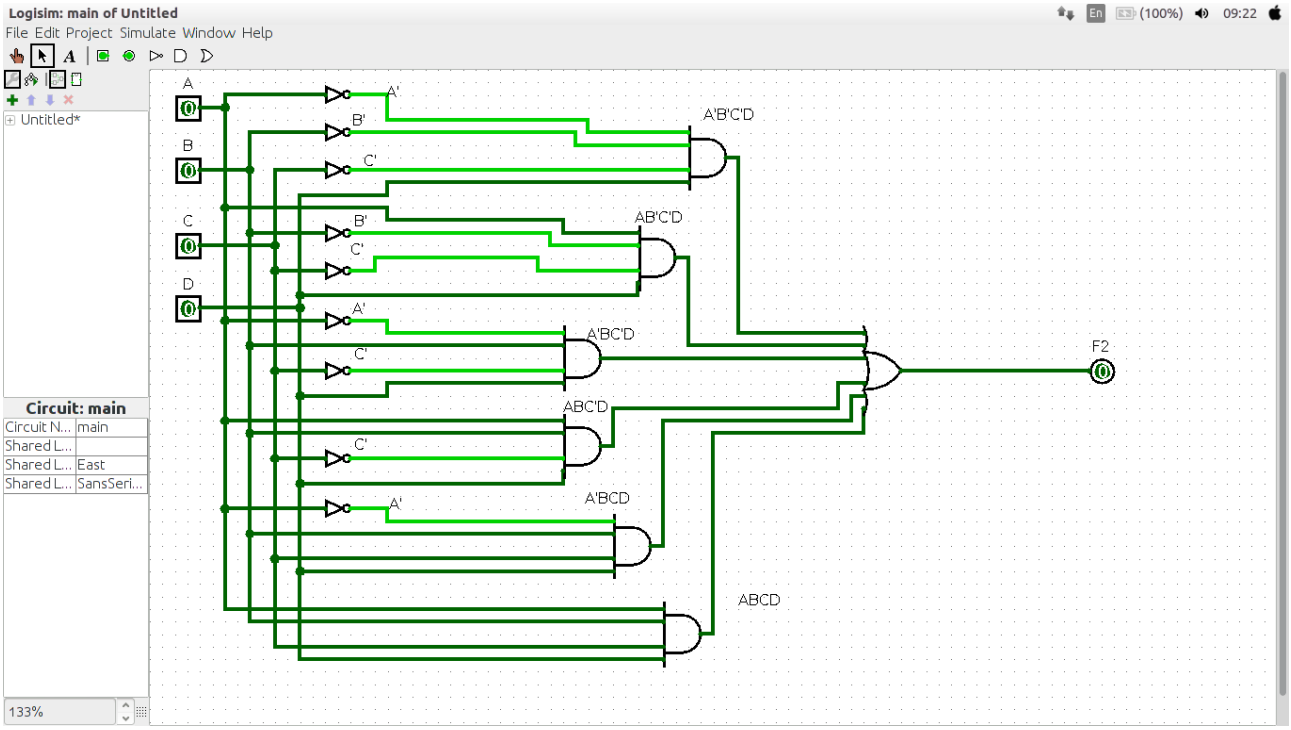


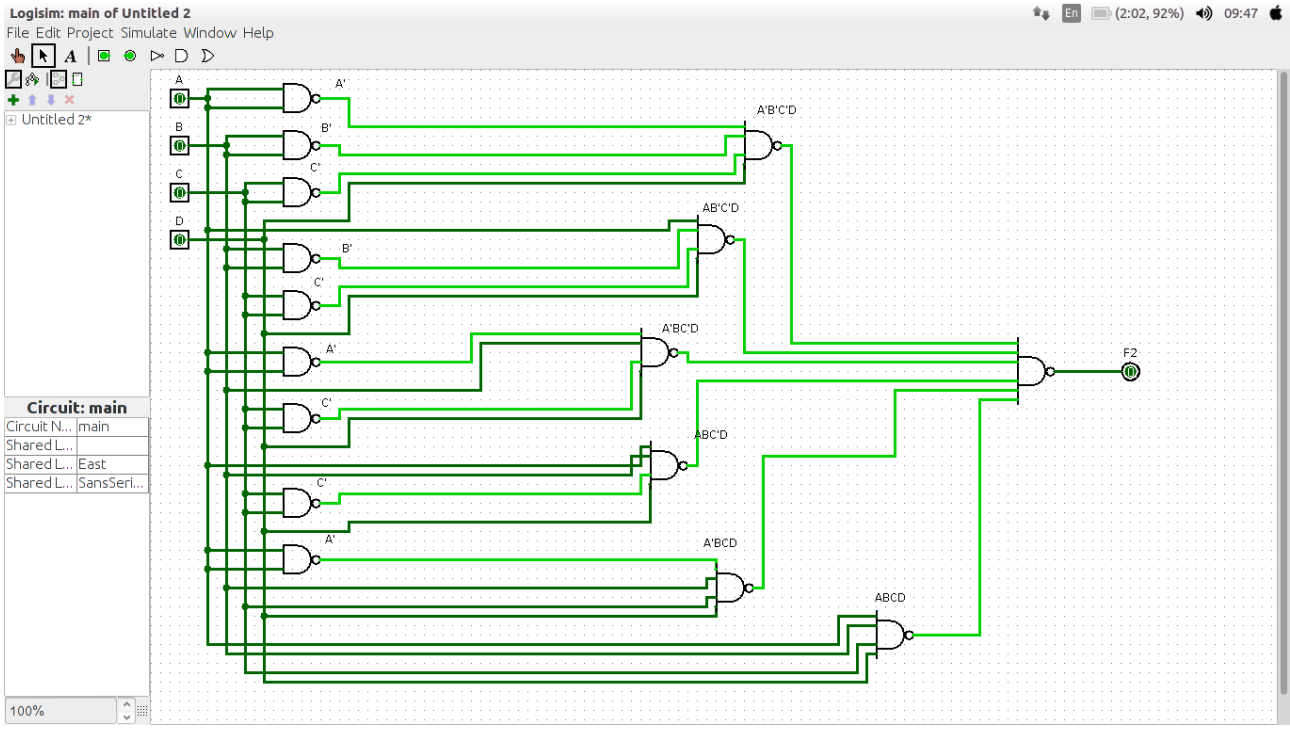

Logisim: main of Untitled 4
File Edit Project Simulate Window Help
A
B
C
A'
B'
A'B'C
A'
B'
A'B'C
A'
A'BC
ABC'
C'
ABC
A'B'
BC'
AB
F

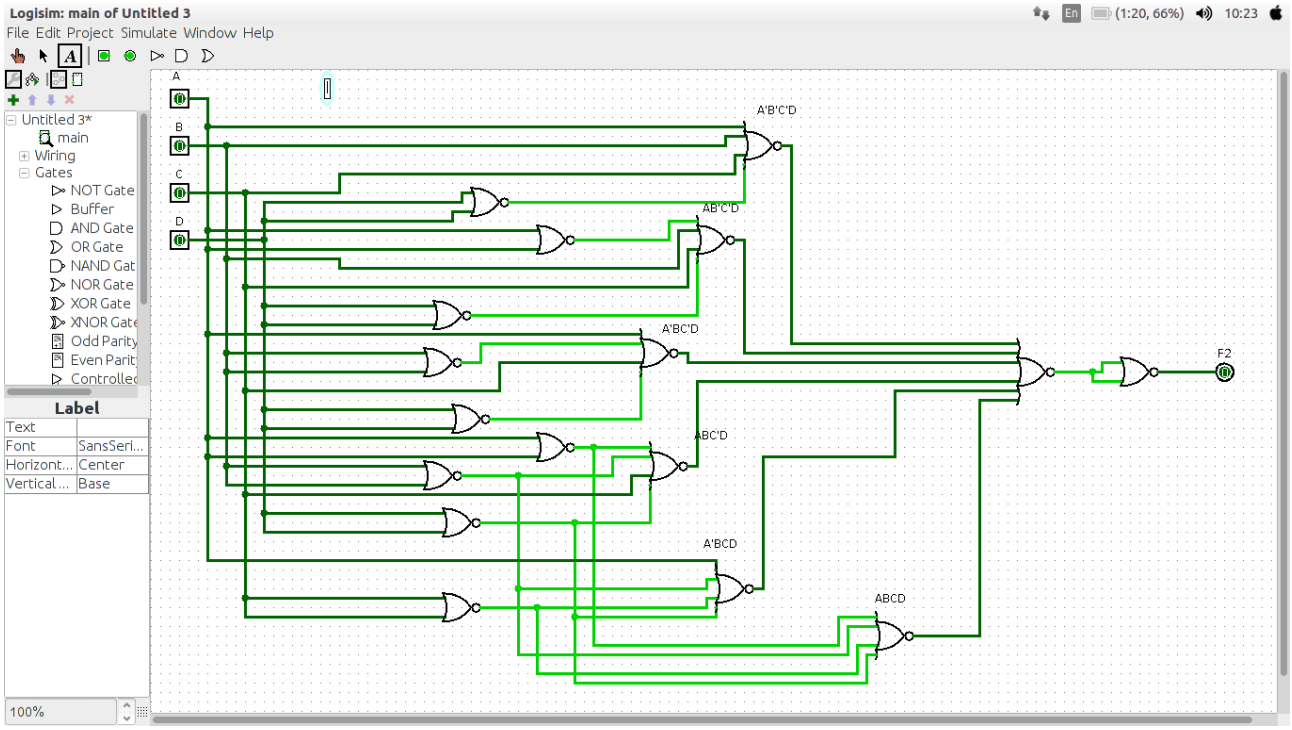

Logisim: main of Untitled 4
File Edit Project Simulate Window Help
Untitled 4*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gate
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parity
Controlled Buffer
Circuit: main
Circuit Name
main
Shared Label
Shared Labe...
East
Shared Labe...
SansSerif Pla...
100%
A
B
C
A'B'C
A'B'C
A'BC
ABC'
ABC
A'B'
BC'
AB
F

F2 = A’B’C’D+AB’C’D+A’BC’D+ABC’D+A’BCD+ABCD

A	B	C	D	F2
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1


Logisim: main of Untitled
File Edit Project Simulate Window Help
Untitled*
Circuit: main
Circuit N... main
Shared L...
Shared L... East
Shared L... SansSeri...
133%
A
B
C
D
A'
B'
C'
A'B'C'D
AB'C'D
A'BC'D
ABC'D
A'BCD
ABCD
F2

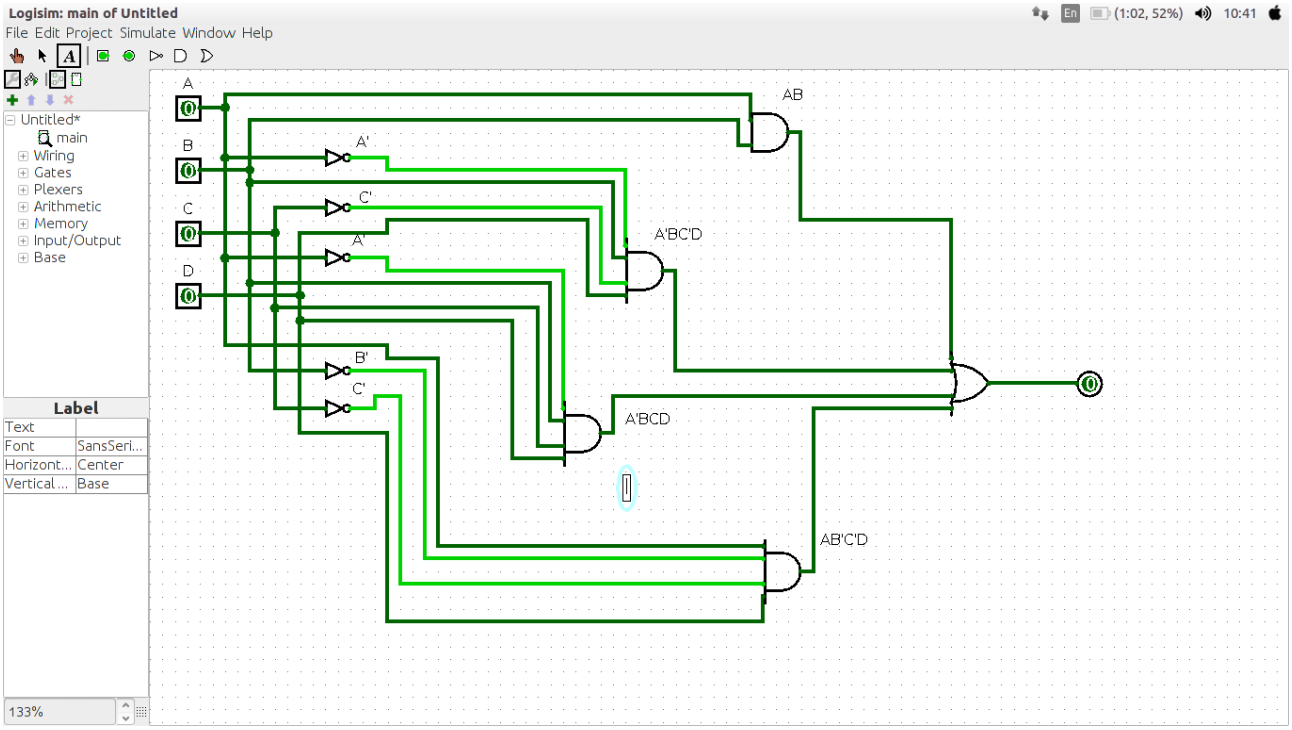

Logisim: main of Untitled 2
File Edit Project Simulate Window Help
Untitled 2*
Circuit: main
Circuit N... main
Shared L...
Shared L... East
Shared L... SansSeri...
100%
A
B
C
D
A'
B'
C'
A'B'C'D
AB'C'D
A'BC'D
ABC'D
A'BCD
ABCD
F2

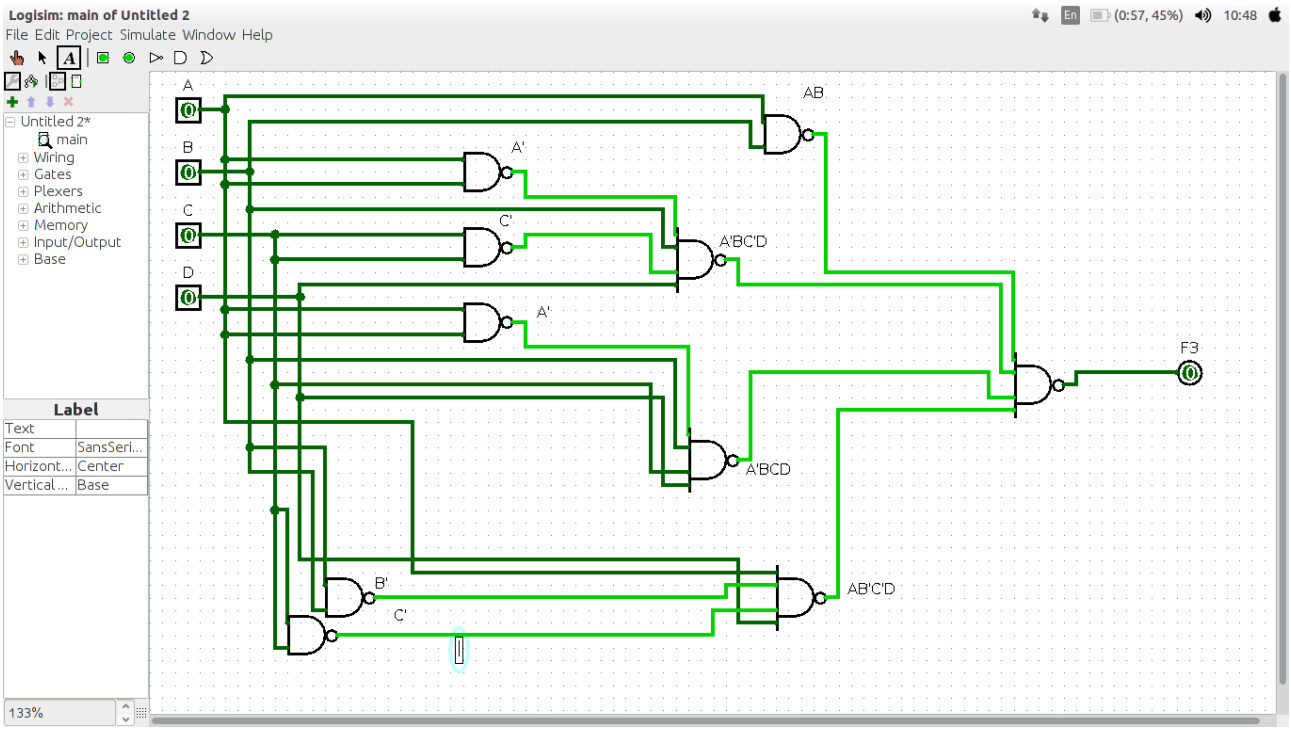


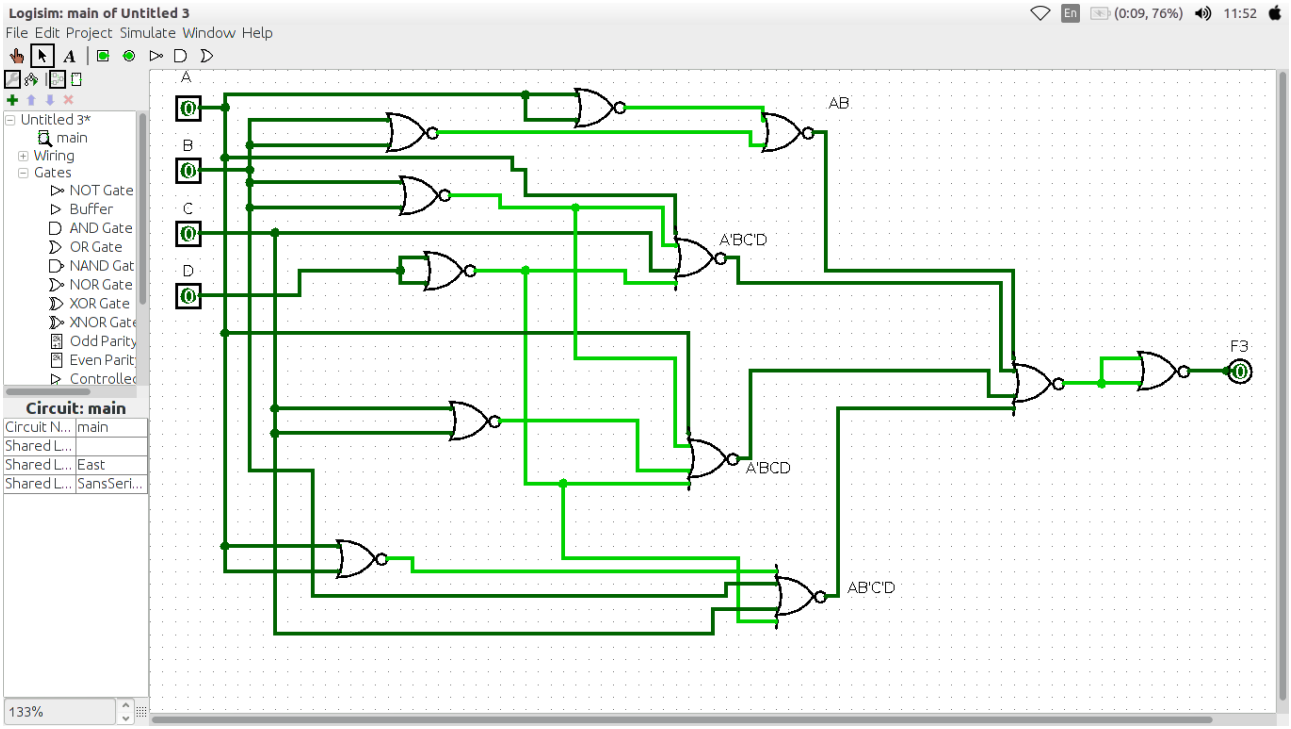
F3 = AB+A’BC’D+A’BCD+AB’C’D

A	B	C	D	F3
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1

1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

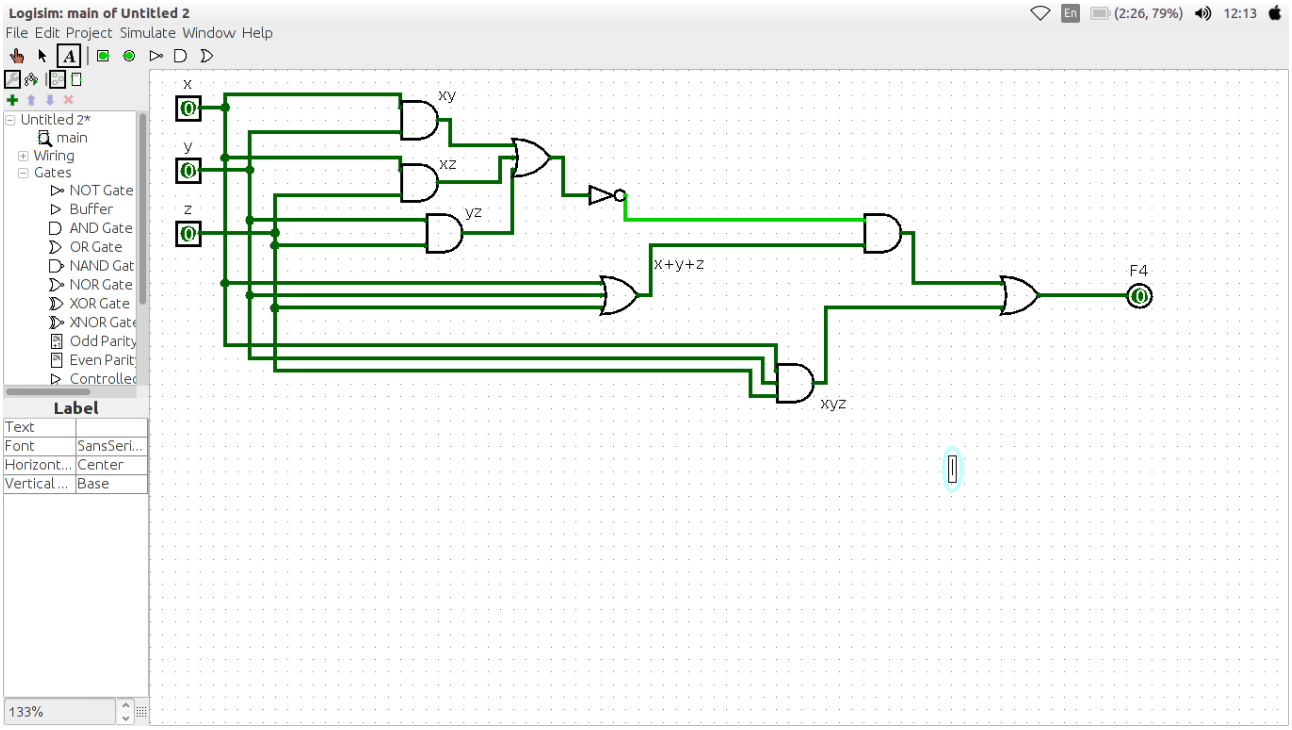


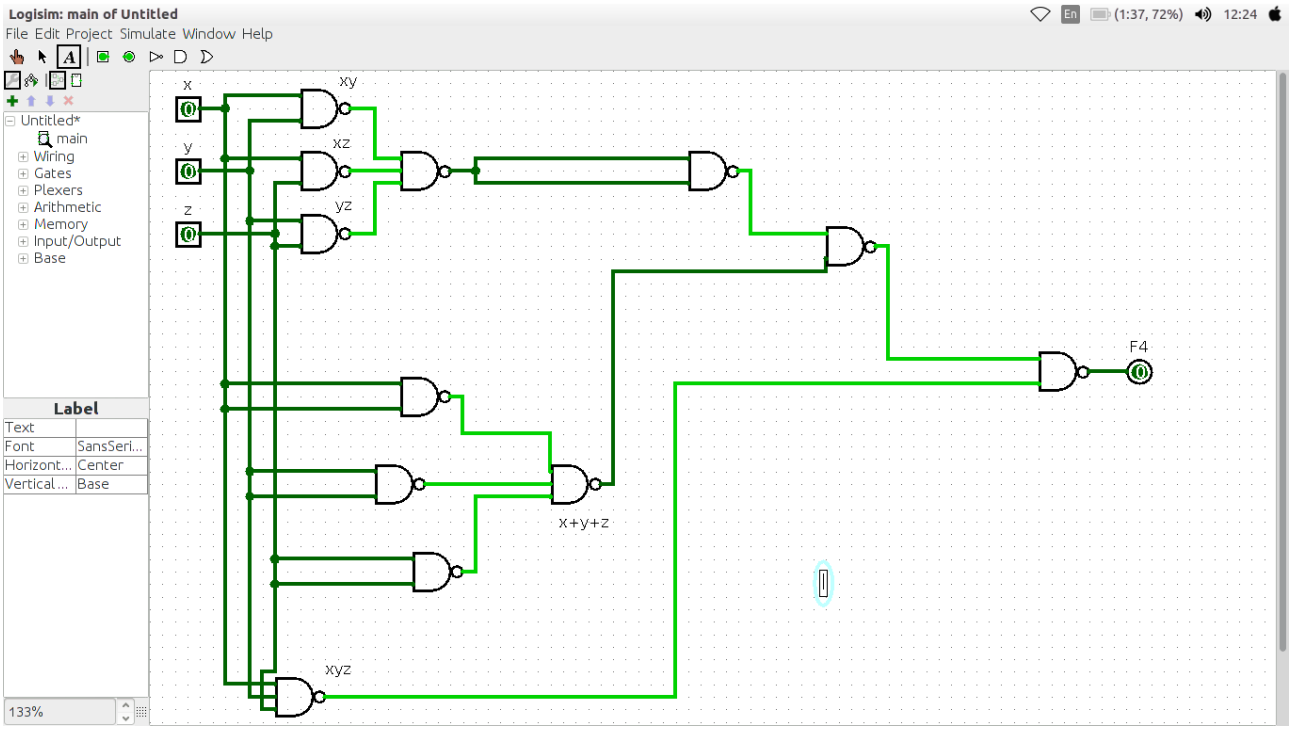


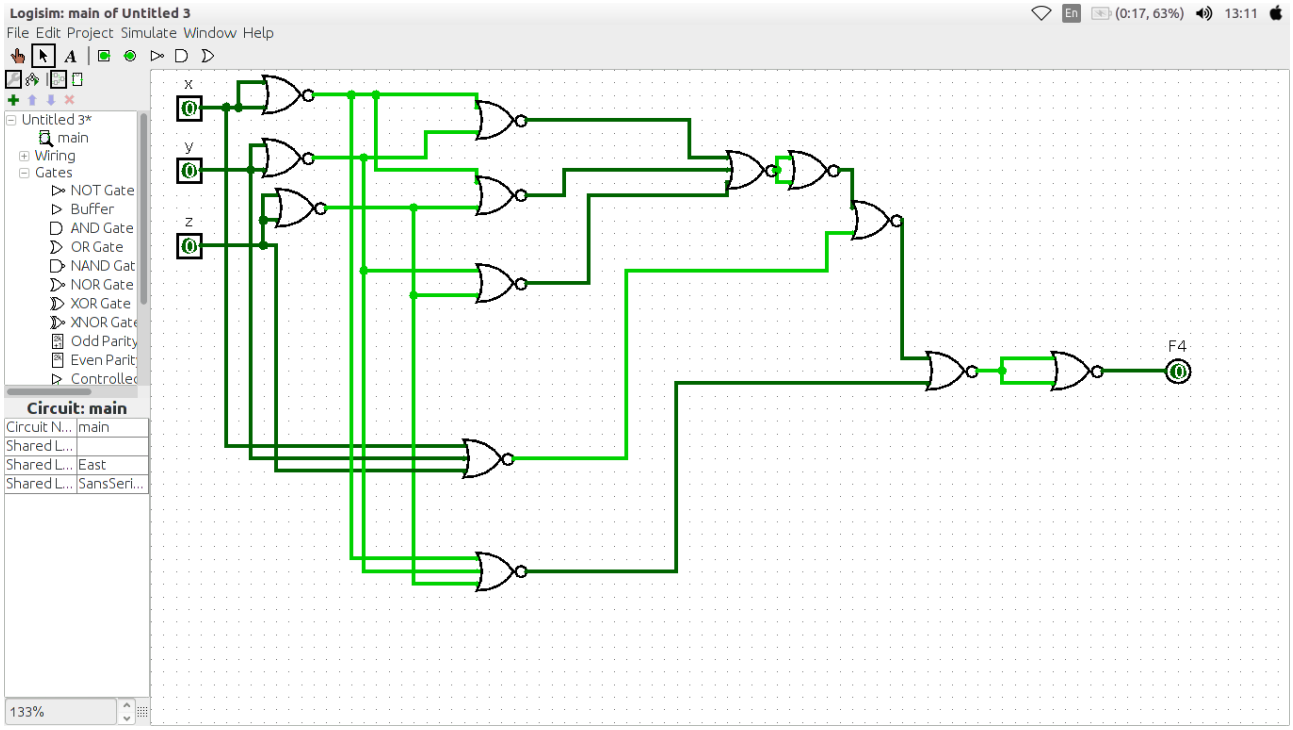


F4 = C + S where C = xy + xz + yz and S = C’ (x + y+ z) + xyz

x	y	z	F4
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1


Logisim: main of Untitled 2
File Edit Project Simulate Window Help
Untitled 2*
main
Wiring
Gates
NOT Gate
Buffer
AND Gate
OR Gate
NAND Gat
NOR Gate
XOR Gate
XNOR Gate
Odd Parity
Even Parit
Controlled
Label
Text
Font
SansSeri...
Horizont...
Center
Vertical ...
Base
133%
x
y
z
xy
xz
yz
x+y+z
xyz
F4


Logisim: main of Untitled
File Edit Project Simulate Window Help
Untitled*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Label
Text
Font
SansSeri...
Horizont...
Center
Vertical ...
Base
133%
x
y
z
xy
xz
yz
x+y+z
xyz
F4



Lab: 2-3

F1 = A’B’+AB’C+’BC+AB’+C+AB’+C’+AB

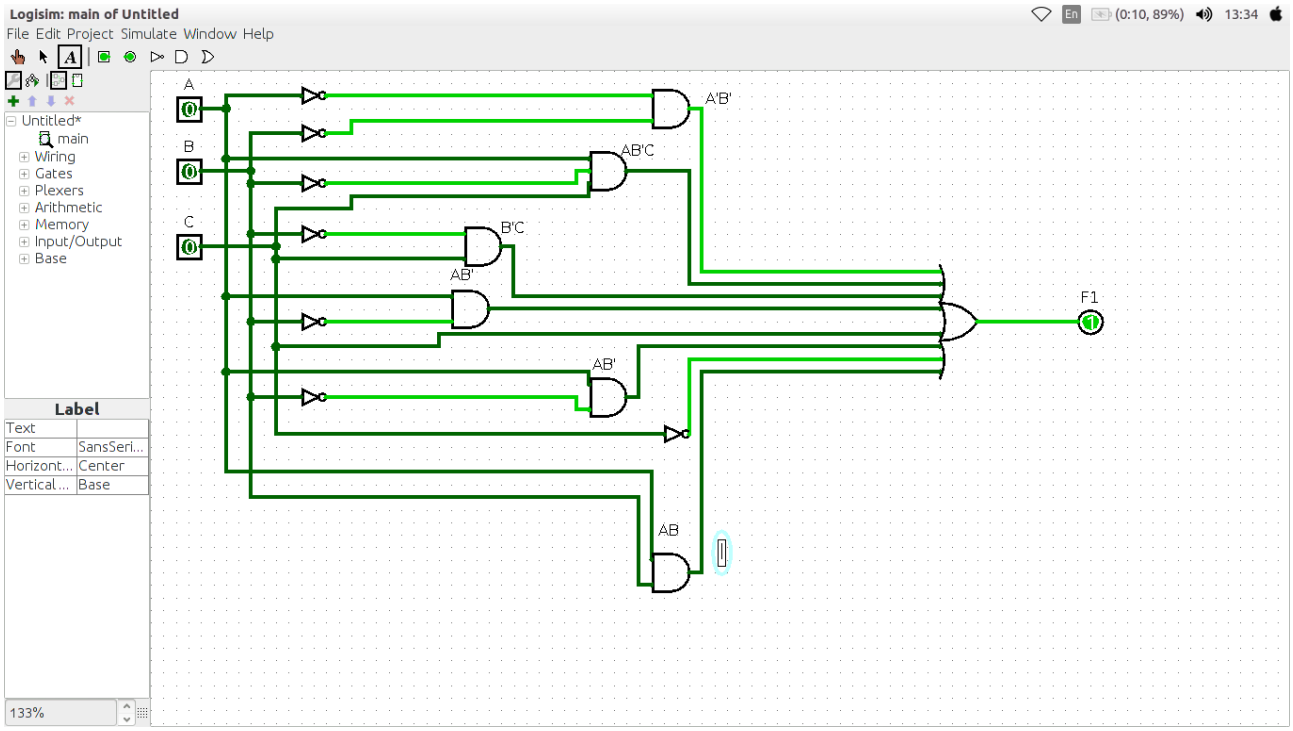
1.

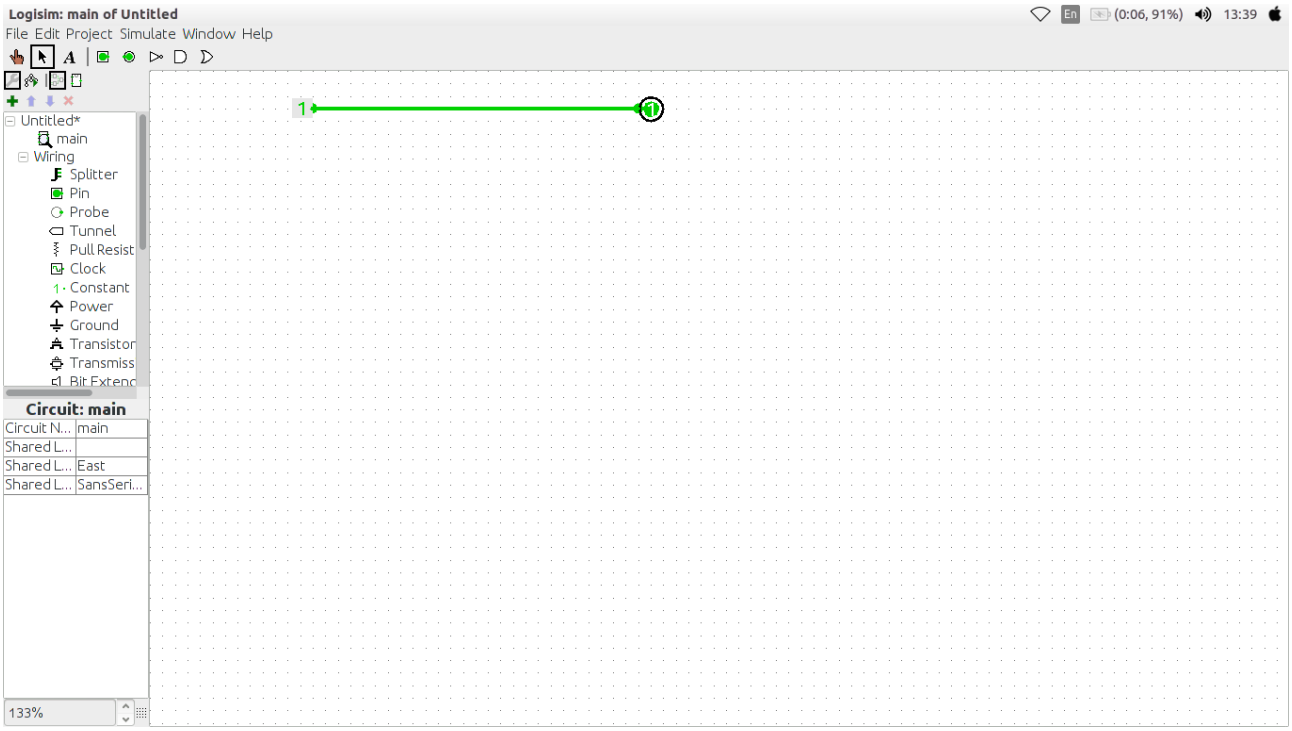
A	B	C	F1
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

2.

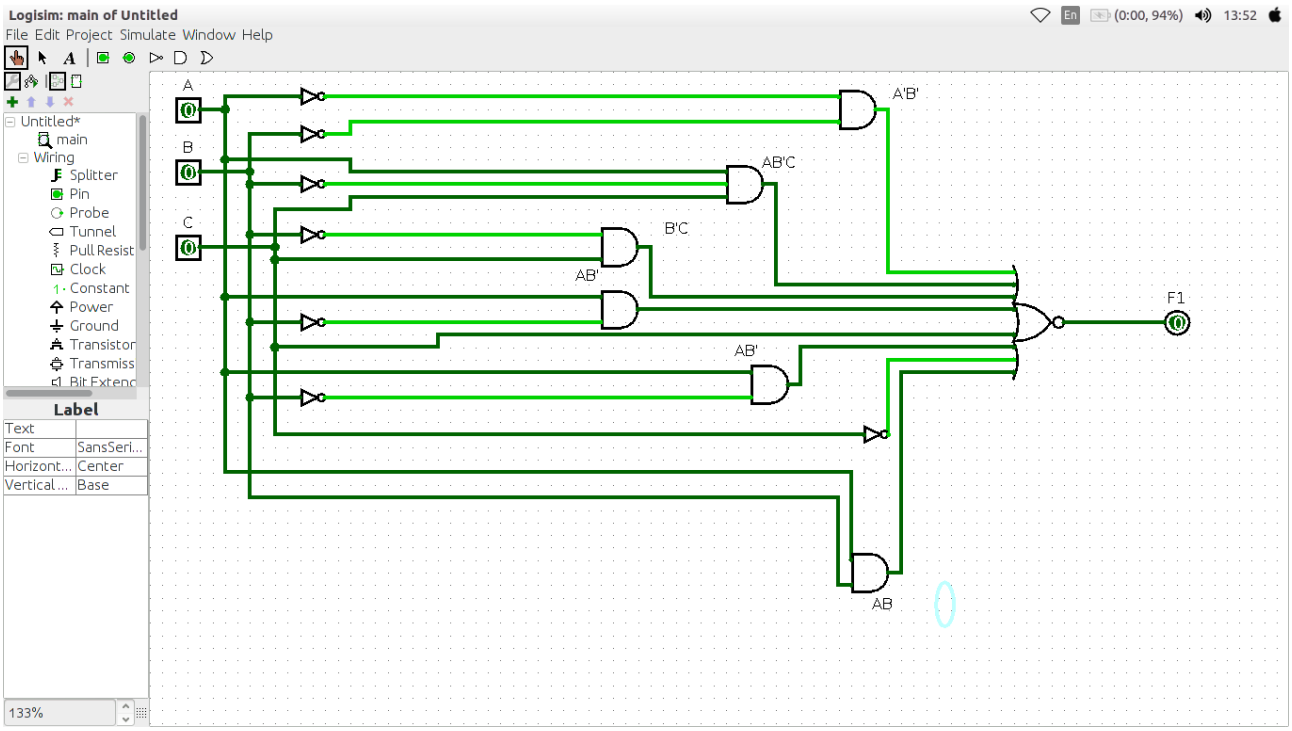
Min terms = A’B’C’ + A’B’C + A’BC’ + A’BC’ + AB’C + AB’C’ + ABC’ + ABC
Max terms = no Max terms

3.




Logisim: main of Untitled
File Edit Project Simulate Window Help
Untitled*
main
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resist
Clock
Constant
Power
Ground
Transistor
Transmiss
Circuit: main
Circuit N... main
Shared L...
Shared L... East
Shared L... SansSeri...
133%
1

4.


Logisim: main of Untitled
File Edit Project Simulate Window Help
Untitled*
main
Wiring
Splitter
Pin
Probe
Tunnel
Pull Resist
Clock
Constant
Power
Ground
Transistor
Transmiss
Label
Text
Font SansSeri...
Horizont... Center
Vertical ... Base
133%
A
B
C
A'B'
AB'C
B'C
AB'
AB'
AB
F1

F2 = AB’C’D+ABC’+C’D+BC’D+A’B+AD

1.

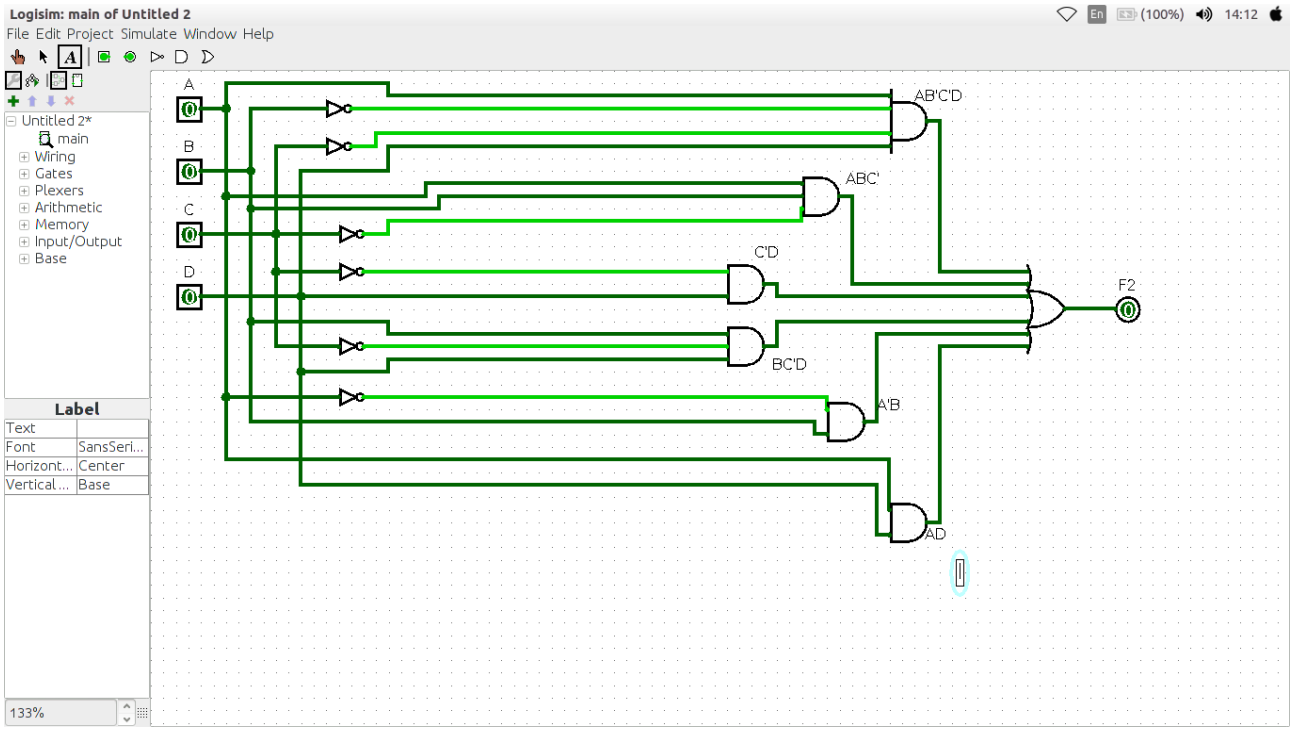
A	B	C	D	F2
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

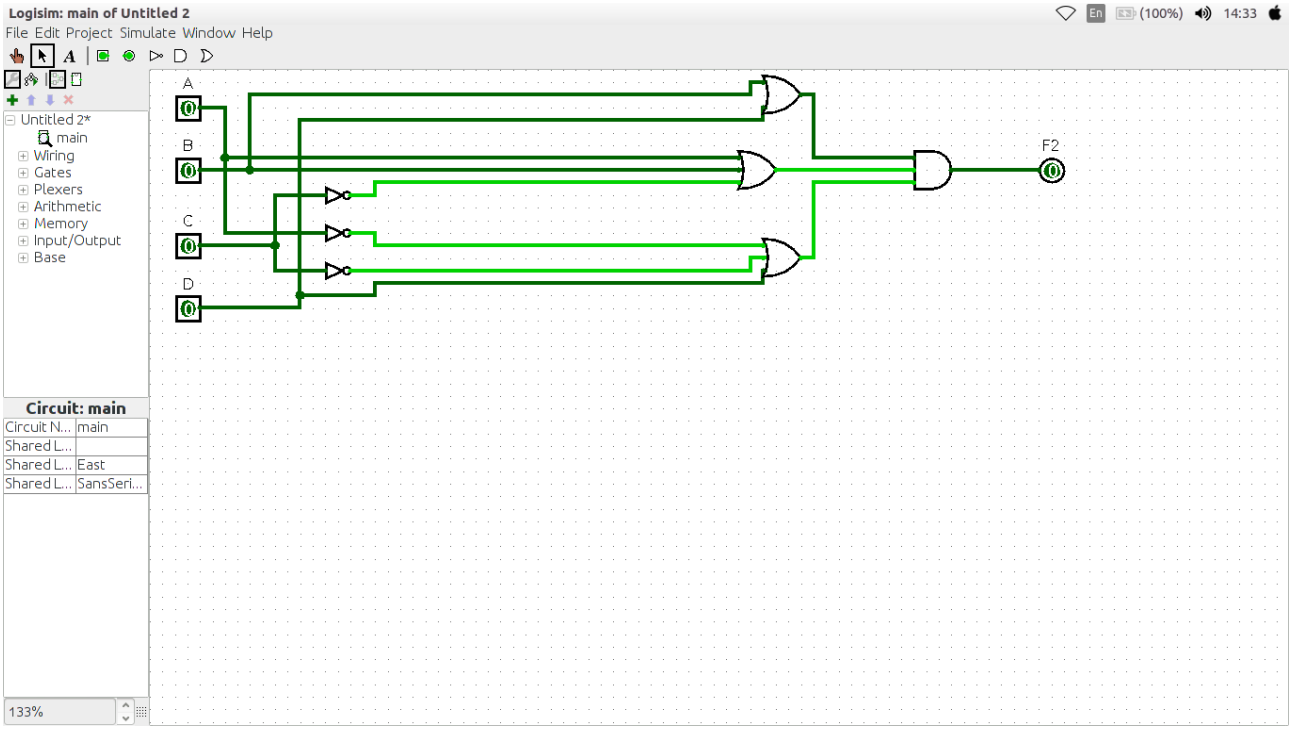
2.

Min Terms = A’B’C’D + A’BC’D’ + A’BC’D + A’BCD’ + A’BCD + AB’C’ D+ AB’CD + ABC’D’ + ABC’D + ABCD

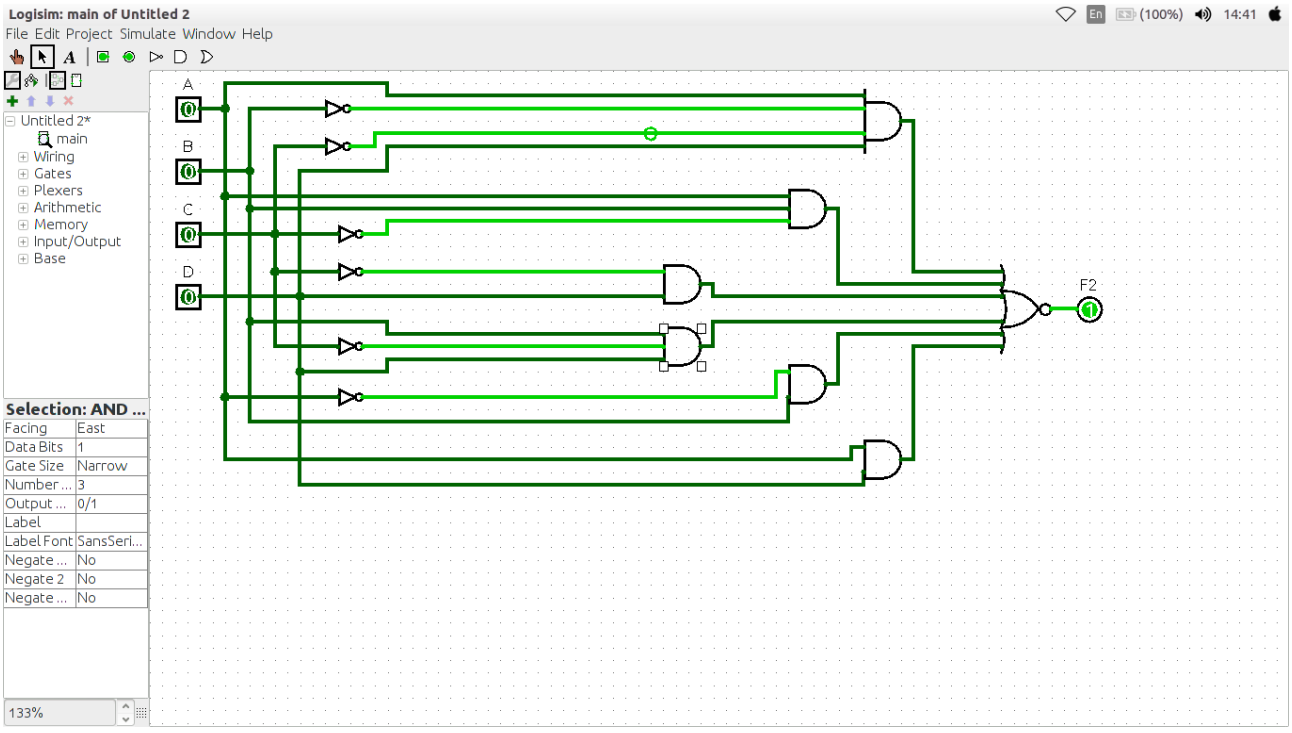
MaX Terms = (A+B+C+D) (A+B+C’+D)(A+B+C’+D’) (A’+B+C+D)(A’+B+C’+D)(A’+B’+C’+D)

3.





4.



F3 = AB+A’B’D+A’B+AB’C’D

1.

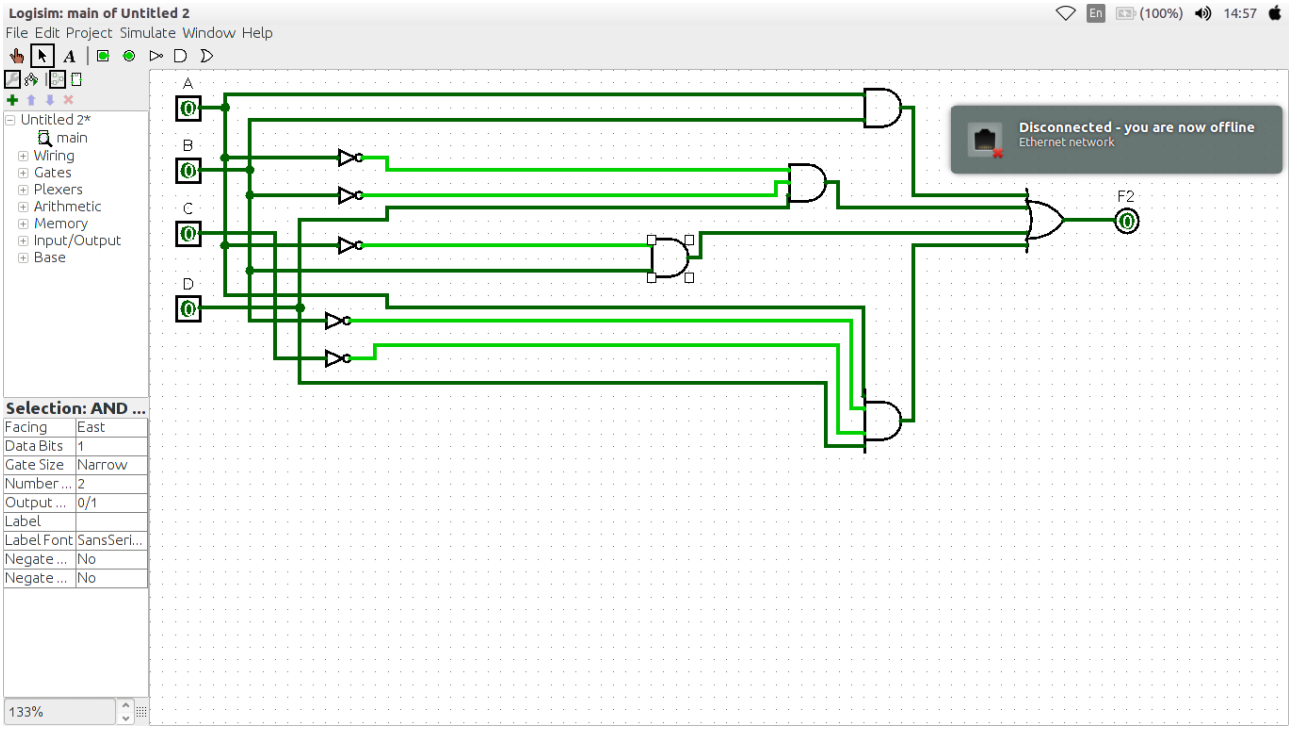
A	B	C	D	F3
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

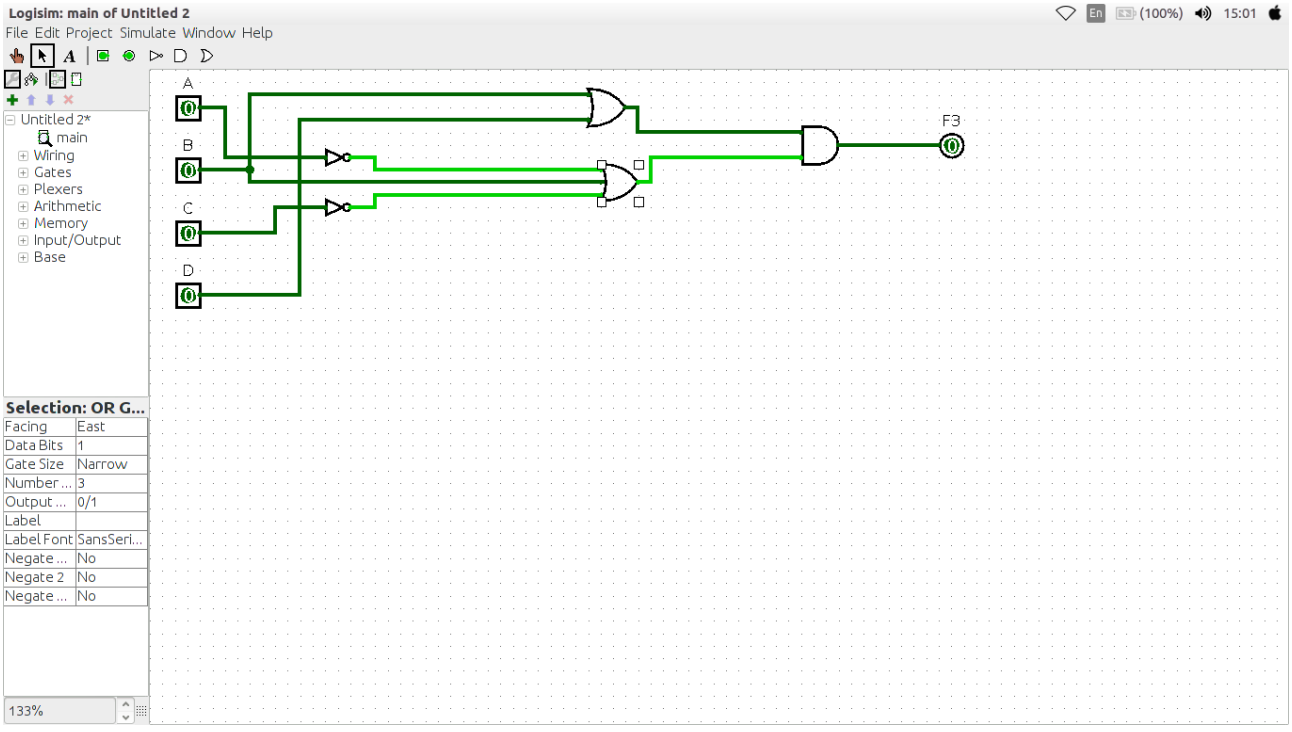
2.

Min Terms = A’B’C’D+A’B’CD+A’BC’D’+A’BC’D+A’BCD’
A’BCD+AB’C’D+ABC’D’+ABC’D+ABCD’+ABCD

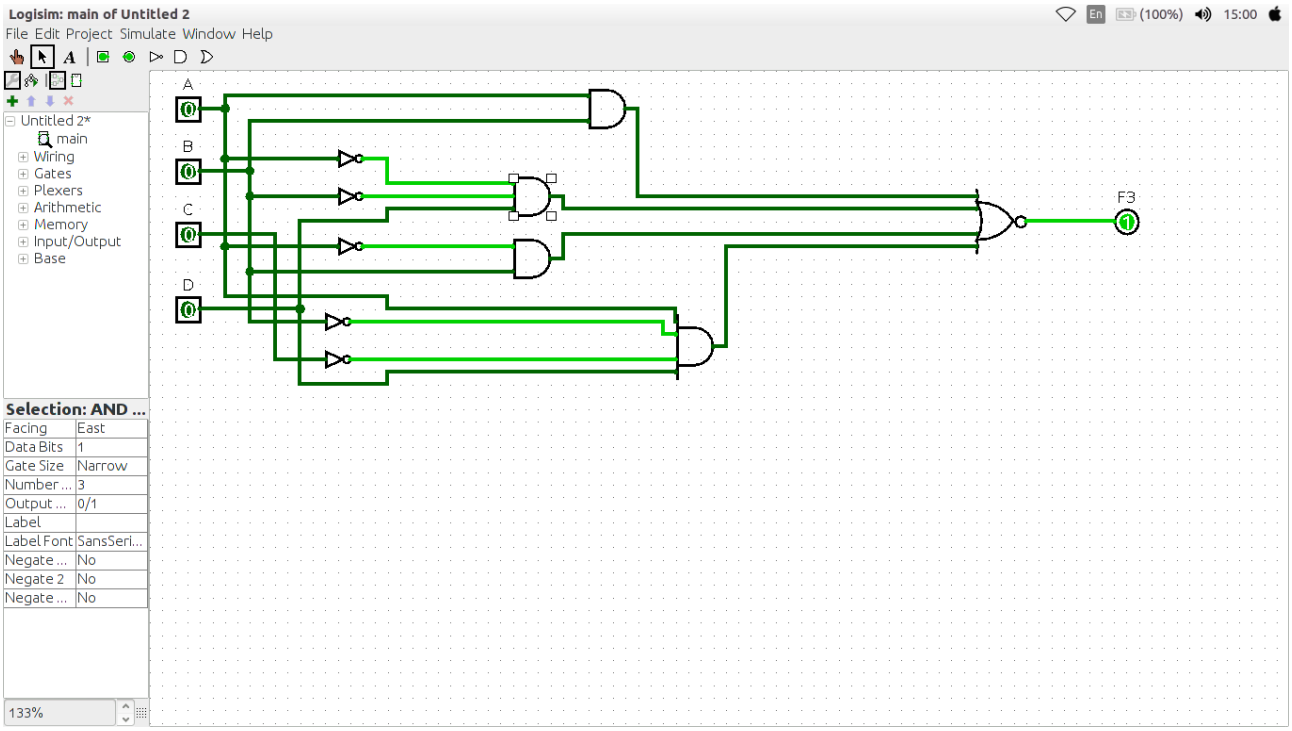
Max Terms = (A+B+C+D)(A+B+C’+D)(A’+B+C+D)
(A’+B+C’+D)(A’+B+C’+D’)

3.


Logisim: main of Untitled 2
File Edit Project Simulate Window Help
(100%) 14:57
Untitled 2*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Selection: AND ...
Facing East
Data Bits 1
Gate Size Narrow
Number ... 2
Output ... 0/1
Label
Label Font SansSeri...
Negate ... No
Negate ... No
133%
A
B
C
D
F2
Disconnected - you are now offline
Ethernet network


Logisim: main of Untitled 2
File Edit Project Simulate Window Help
(100%) 15:01
Untitled 2*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Selection: OR G...
Facing East
Data Bits 1
Gate Size Narrow
Number ... 3
Output ... 0/1
Label
Label Font SansSeri...
Negate ... No
Negate 2 No
Negate ... No
133%
A
B
C
D
F3

4.



F4 = C + S where C = xy + yz and S = C’ (x + y) + xyz

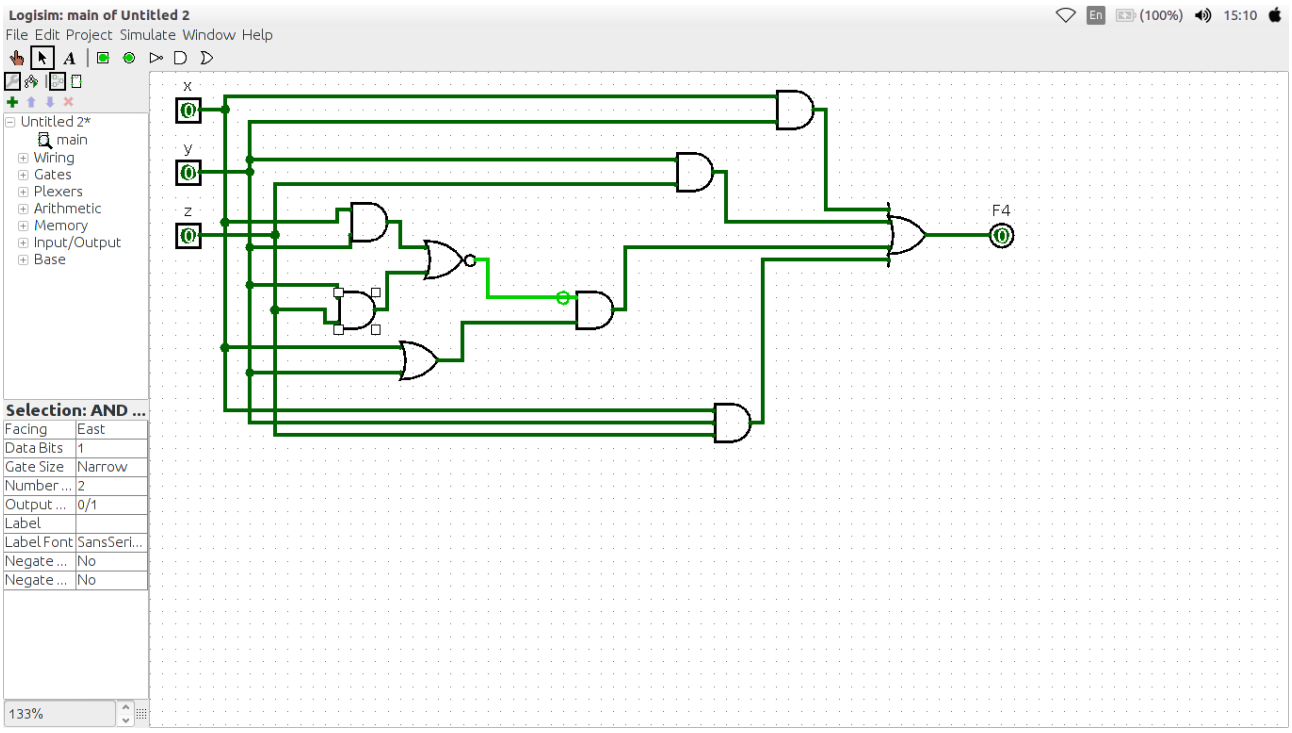
x	y	z	F4
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

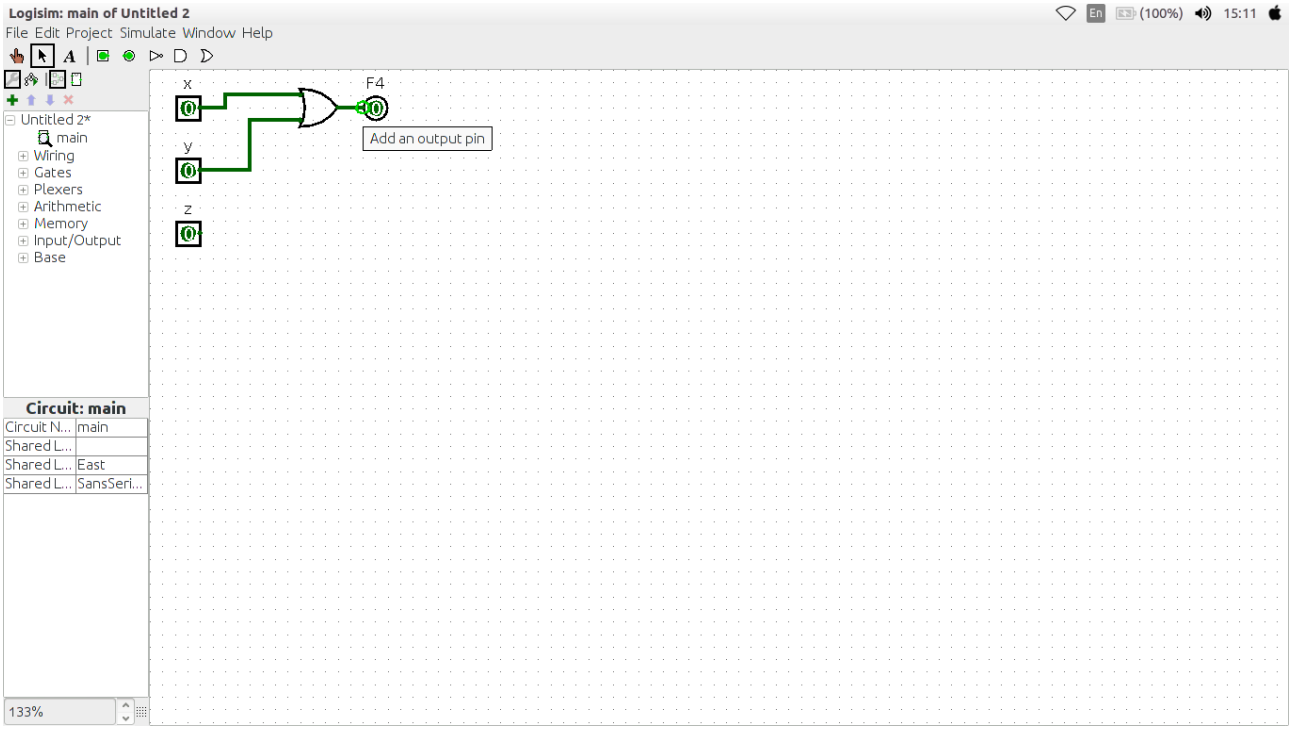
2.

Min Terms = x’yz’+x’yz+xy’z’+xy’z+xyz’+xyz

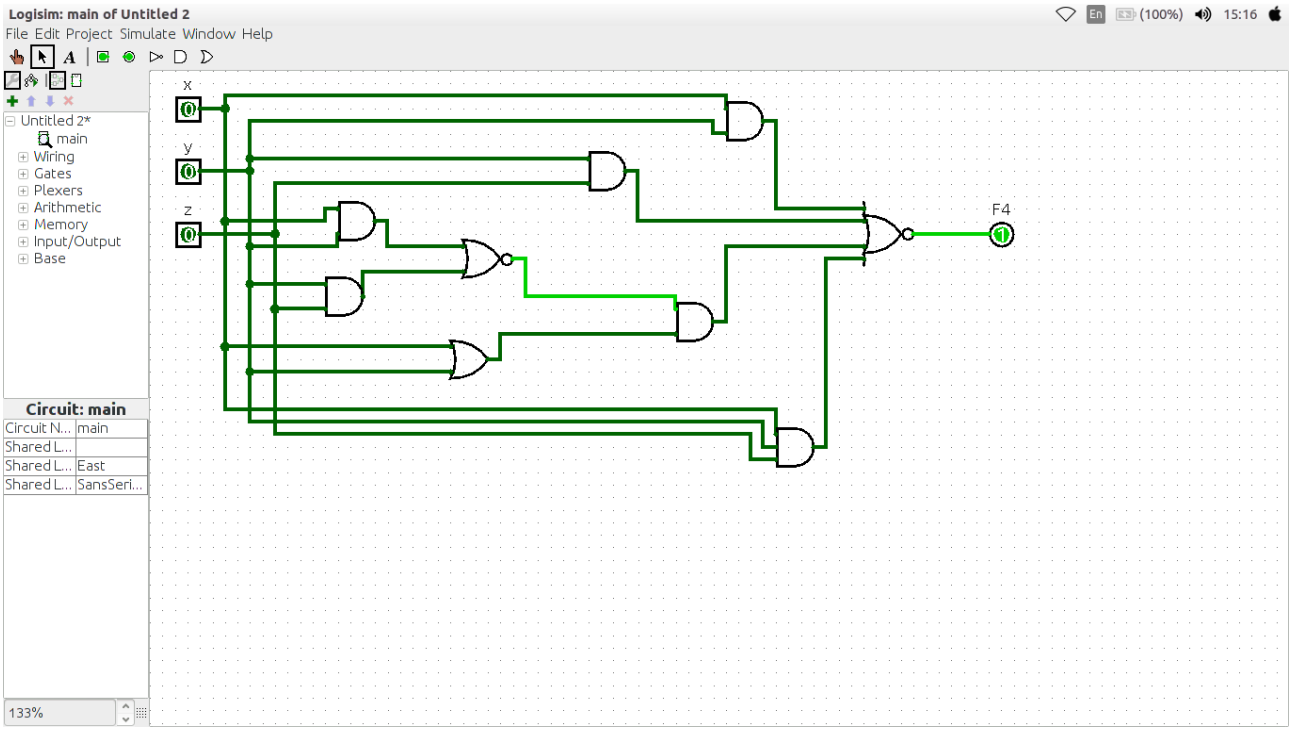
Max Terms = (x+y+z)(x+y+z’)

3.




Logisim: main of Untitled 2
File Edit Project Simulate Window Help
(100%) 15:11
Untitled 2*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: main
Circuit N... main
Shared L...
Shared L... East
Shared L... SansSeri...
133%
x
y
z
F4
Add an output pin

4.


Logisim: main of Untitled 2
File Edit Project Simulate Window Help
(100%) 15:16
Untitled 2*
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Circuit: main
Circuit N... main
Shared L...
Shared L... East
Shared L... SansSeri...
133%
x
y
z
F4

Lab: 4-5

F1 = A’B’+AB’C+A’BC+AB’+C+AB’+C’+AB

1.

A	B	C	F1
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

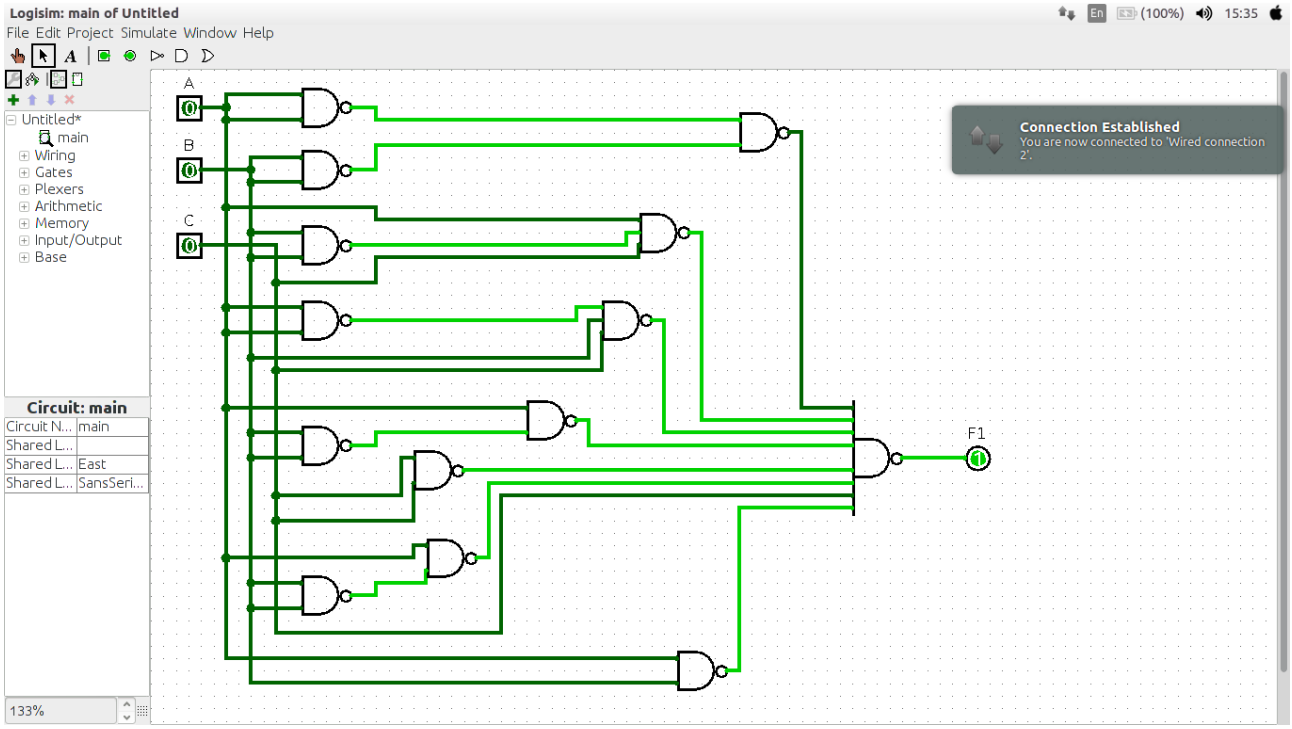
2.

K-MAP

1	1	1	1
1	1	1	1

EQUATION IS : 1

3.



F2 = AB’C’D+AC’D+C’D+C’D+A’B+AD

1.

A	B	C	D	F2
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1

1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

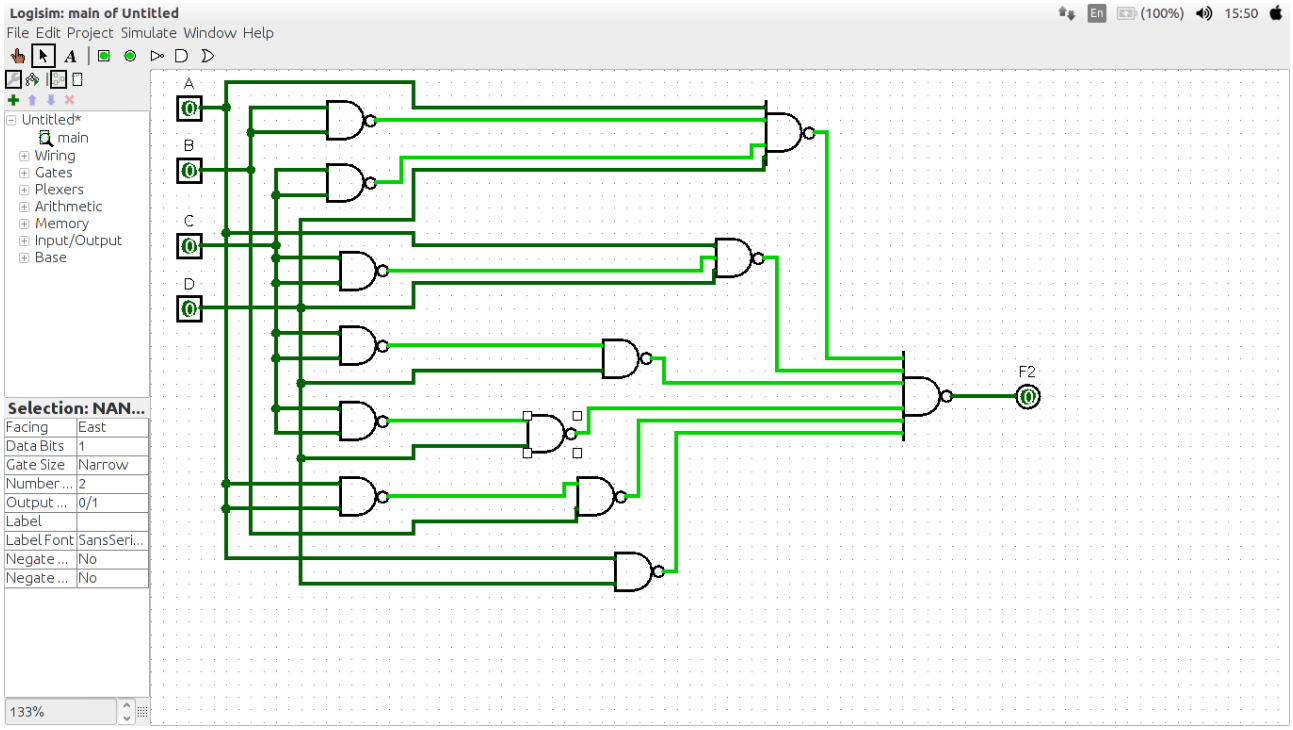
2.

K-MAP

0	1	0	0
1	1	1	1
0	1	1	0
0	1	1	0

EQUATION IS : C’D + A’B + AD

3.



F3 = AB+A’C’D+A’BD+AB’C’

1.

A	B	C	D	F3
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0

1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

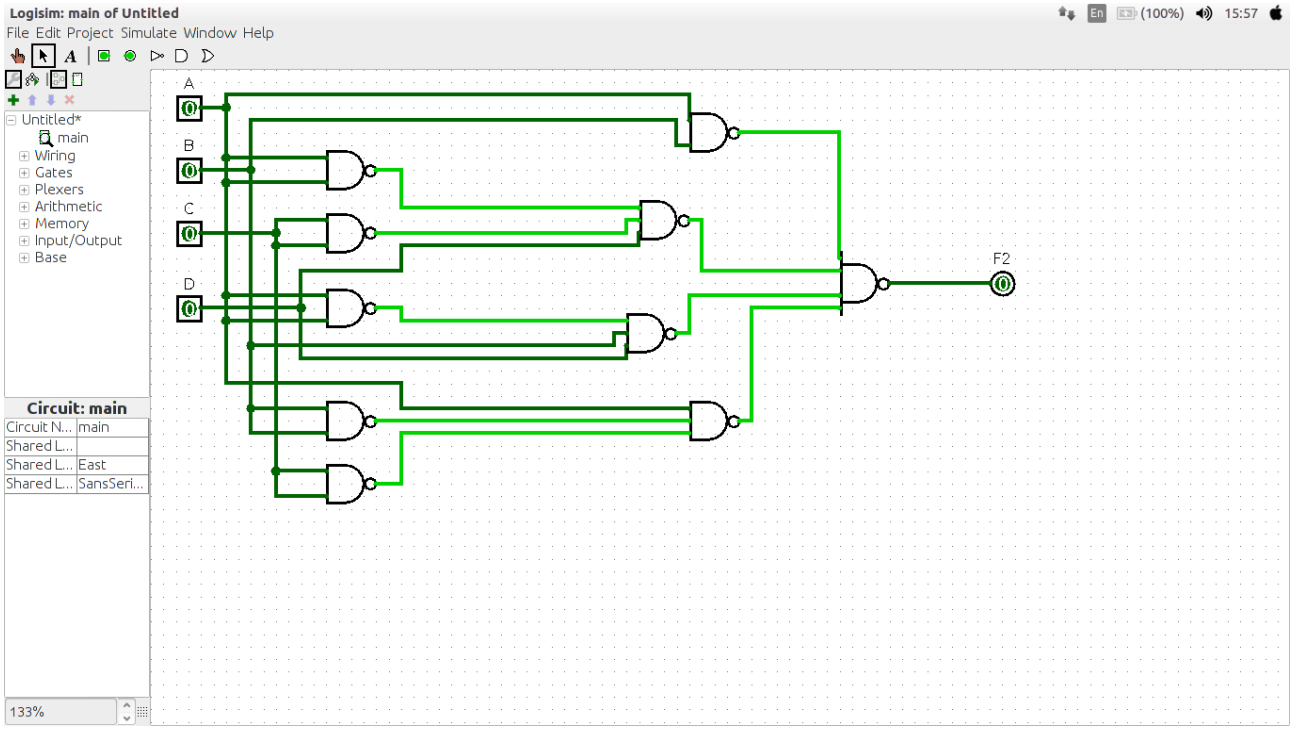
2.

K-MAP

0	1	0	0
0	1	1	0
1	1	1	1
1	1	0	0

EQUATION IS : C’D + BD+ AC’ + AB

3.



F4 = C + S where C = xy + yz and S = C’ (x + y) + xyz

1.

x	y	z	F4
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

2.

k-map

0	0	1	1
1	1	1	1

Equation is : x + y

3.