

Chapter 2

AGC Fundamentals

From a practical point of view, the most general description of an AGC system is presented in Fig. 2.1. The input signal V_{IN} is amplified by a variable gain amplifier (VGA), whose gain is controlled by a signal V_C . In order to adjust the gain of the VGA to its optimal output level V_{OUT} , the AGC generally, first detects the strength level of the signal using the peak detector; it then compares this level with a reference voltage V_{REF} and finally, it filters and generates the required control voltage. This function can be performed by detecting the signal at the output of the VGA, so the architecture is called “feedback” AGC (Fig. 2.1a), or at the input, in which case it is identified as “feedforward” AGC (Fig. 2.1b) [1].

Both structures present different inherent characteristics which means choosing one or the other depending on the target application.

Feedback AGCs The advantages of using feedback AGC are: first, the dynamic range required at the detector input is reduced in the same way as the AGC gain range; and second, the circuit linearity is high due to the feedback loops’ inherent characteristic. On the other hand, this architecture also has the following disadvantages. The high level of feedback required to reach high compression ratios makes feedback processors more likely to exhibit instabilities if high compression ratios are managed. Instability is also likely in feedback expanders where high expansion ratios are desired. Finally, the feedback loop will always have a maximum boundary bandwidth in order to maintain stability. This maximum bandwidth entails a minimum settling-time [2]. In many applications this is not a significant issue, since several signal periods are processed before the gain is changed. However, in other cases the standard imposes a maximum settling-time that precludes the use of conventional feedback configurations [3, 4]. Moreover, in order to keep the settling-time constant, the feedback configuration requires the use of specific control voltage generation functions.

Feedforward AGCs High compression and high expansion ratios are possible with this configuration [5]. Moreover, the feedforward AGC offers a time constant that mainly depends on the peak detector response, so this loop is ideally not affected by the minimum settling-time restriction. In contrast, the disadvantages of a feedforward AGC are that the level detector is exposed to the entire dynamic range of

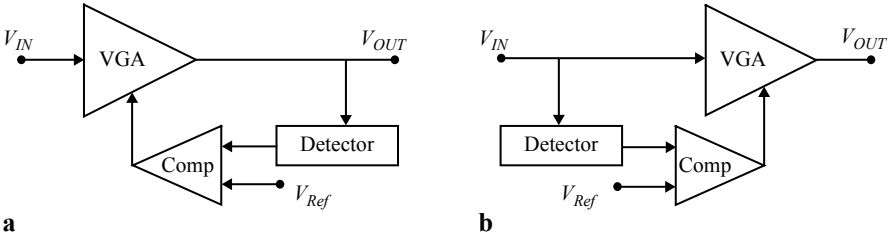


Fig. 2.1 Simplified block diagrams of feedback (a) and feedforward (b) AGCs

Table 2.1 Summary of main AGC loop control characteristics

	Advantages	Disadvantages
Feedback Loop	Lower input dynamic range required by peak detector Inherently higher linearity	Instabilities with high compression or expansion Higher settling-time
Feedforward Loop	No instability problems Ideally, zero settling-time	AGC input dynamic range required by peak detector High linearity required in loop

the input signal and that the loop requires higher linearity, since the feedback loop inherent linearity improvement is now absent. Table 2.1 summarizes the main characteristics of these two configurations.

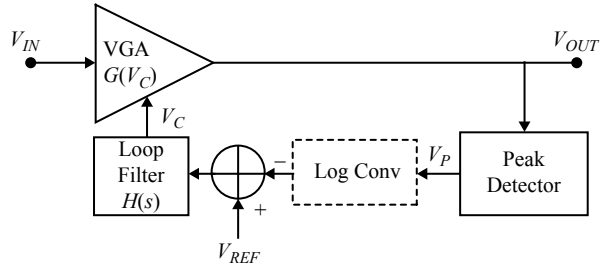
To provide a deep insight into the theory and design of AGC circuits, this chapter will be focused on the study of the control theory involved behind the primary idea of an AGC system, for both the feedback and feedforward configurations. After that, a few practical AGC circuits will be simulated and the obtained performances analyzed.

2.1 AGC Loop Fundamentals

2.1.1 AGC with Feedback Loop

Typically, the AGC circuit has to adjust the amplitude of the incoming signal before the ADC continues with the recovery of data from the input signal. This adjustment usually occurs during a predetermined preamble where known data are transmitted and whose duration should be minimized to attain an efficient use of the channel bandwidth. One of the key issues in feedback control loops is that if the control voltage generation function is not correctly chosen, the acquisition time will be a function of the input amplitude and the preamble will be shorter than the slowest possible AGC circuit acquisition time [6, 7]. Consequently, to optimize system

Fig. 2.2 Common block diagram of feedback AGC



performance, the AGC loop settling time should be well defined and signal independent.

A typical feedback AGC scheme is shown in Fig. 2.2. It consists of a variable gain amplifier, a peak detector and a loop filter. The loop filter is required to generate the DC level required to manage the VGA and in feedback AGCs, it is especially important to settle loop bandwidth and keep it stable. In this scheme, V_{IN} is the input signal to be adjusted; V_{OUT} is the output signal which must have a constant amplitude associated to V_{REF} ; V_P is the amplitude level detected by the peak detector; V_{REF} is the reference which fixes the required output amplitude; and V_C is the control signal which varies the gain of the VGA by means of a function $G(V_C)$ in order to obtain the desired output.

Although the AGC loop is typically a nonlinear system, the employment of a logarithmic converter, shown in the scheme in dashed lines, together with the correct function $G(V_C)$, will result in a linear system in decibels (dB) [8]. As will be shown in the following analysis, this result is the most common condition required to obtain the essential property of a constant acquisition time [9]. The loop works by increasing or reducing V_C until V_P is made equal to the reference voltage V_{REF} which determines the output amplitude.

Consider now input V_{IN} and output V_{OUT} signals given by the general expressions:

$$\begin{aligned} V_{IN}(t) &= A_{IN}(t)f(wt) \\ V_{OUT}(t) &= A_{OUT}(t)f(wt), \end{aligned} \quad (2.1)$$

where A_i corresponds to the amplitude term and f is a function which introduces the frequency dependence.

Since the AGC loop responds only to the amplitude level of the signals, let us continue this analysis considering only $A_{IN}(t)$ and $A_{OUT}(t)$. From Fig. 2.2 the relationship between the input and output amplitude is given by:

$$A_{OUT} = G(V_C)A_{IN}. \quad (2.2)$$

To facilitate analysis, the AGC of Fig. 2.2 is reshaped to the logarithmic domain, so in the following, the equivalent representation of the AGC shown in Fig. 2.3 will be used. This AGC model employs logarithmic blocks to express the main input

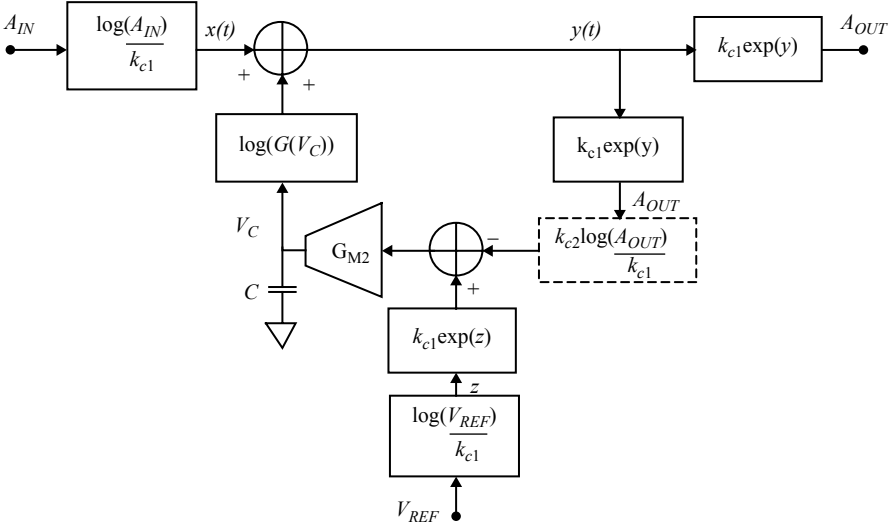


Fig. 2.3 Model of generalized feedback AGC

signals in dBs. Thus, x , y and z are now the input, output and reference signals respectively. The peak detector block has been removed from the AGC in Fig. 2.3, since it has been considered that the peak detector extracts the amplitude of V_{OUT} linearly and much faster than the loop basic operation, so it has no effect on the loop dynamics. The loop filter $H(s)$ is represented as a low pass filter with the transfer function equal to G_{M2}/sC . Again, as shown in the figure, only amplitude levels are taken into account.

Thus, (2.2) can be rewritten as:

$$A_{OUT} = k_{c1} \exp \left\{ \log [G(V_C)] + \log \left[\frac{A_{IN}}{k_{c1}} \right] \right\}, \quad (2.3)$$

where k_{c1} is a constant with the same dimensions as A_{IN} and A_{OUT} .

On the other hand, according to Fig. 2.3, the output of the AGC can be expressed as:

$$y(t) = x(t) + \log [G(V_C)] \quad (2.4)$$

and the control voltage is given by this expression:

$$V_C(t) = \int_0^t \frac{G_{M2}}{C} \{k_{c1} e^z - k_{c2} \log [e^{y(\tau)}]\} d\tau. \quad (2.5)$$

Taking the derivative with respect to the time of (2.4) and introducing the result in (2.5), the following equation is obtained:

$$\frac{dy}{dt} = \frac{dx}{dt} + \frac{1}{G(V_C)} \frac{dG}{dV_C} \frac{G_{M2}}{C} \{k_{c1} e^z - k_{c2} \log [e^{y(t)}]\}, \quad (2.6)$$

which represents a nonlinear system response of the output y to the input x , depending on the function $G(V_C)$. Let us rewrite (2.6) in the following way:

$$\frac{dy}{dt} + s(V_C)k_{c1}y(t) = \frac{dx}{dt} + s(V_C)V_{REF}, \quad (2.7)$$

where

$$s(V_C) = \frac{1}{G(V_C)} \frac{dG}{dV_C} \frac{G_{M2}}{C}. \quad (2.8)$$

Equation (2.7) describes a first-order linear system having a high pass response with a time constant given by:

$$\tau = \frac{1}{s(V_C)k_{c2}} = \left[\frac{1}{G(V_C)} \frac{dG}{dV_C} \frac{G_{M2}}{C} k_{c2} \right]^{-1}. \quad (2.9)$$

We are now going to look at different system responses depending on the choice of $G(V_C)$ function. Many different functions could be employed though only main cases will be analyzed in this work.

Linear function Let us begin with the simplest case taking $G(V_C)$ as a linear function: $G(V_C) = aV_C$, where a is a constant. With this selection, the time constant in (2.9) yields to:

$$\tau = \left[\frac{1}{V_C} \frac{G_{M2}}{C} k_{c2} \right]^{-1}. \quad (2.10)$$

As shown in (2.10), the time constant, τ , depends on the control voltage, V_C . As a result, τ depends on the input signal strength, since V_C will vary inversely proportional to the input level. In many receivers, input dynamic range can be up to 80 dB [10, 11]. This means the time constant for small signals would be ten thousand times longer than the minimum τ . As a result, given that the ADC must wait until all the previous blocks characteristics are fixed, the time performance of the full receiver would be degraded.

Exponential function The solution to the above problem is to employ a function $G(V_C)$ so that the associated time constant is kept steady throughout the full dynamic range: the most popular solution is to fix G_{M2} and C in Fig. 2.3 and to make τ constant by choosing the correct function $G(V_C)$. Thus, we need only to solve the differential equation below:

$$\frac{1}{G(V_C)} \frac{dG}{dV_C} = k_{G1}, \quad (2.11)$$

which has the unique solution given by:

$$G(V_C) = k_{G2}e^{k_{G1}V_C}, \quad (2.12)$$

so the time constant depends only on certain internal circuit characteristics:

$$\tau_{\exp-\log} = \frac{C}{G_{M2}k_{G1}k_{c2}} = \text{constant}. \quad (2.13)$$

The function in (2.12) is the most popular solution employed to implement AGCs. This has lead many designers to try to implement the VGA with an exponential control voltage [10–13]. This is not difficult if BiCMOS technology is used [14], but the logarithmic block (in dotted lines) is quite complicated to implement in CMOS technologies, and consequently, in some CMOS systems this block is omitted [15]. In these cases, it is also possible to meet the constant settling-time objective considering small signal approximations. Using (2.8) and considering $s(V_C) = k_x$, (2.6) without the \log function is rewritten as:

$$\frac{dy}{dt} = \frac{dx}{dt} + k_x[V_{REF} - k_{c1}e^{y(t)}]. \quad (2.14)$$

Assuming that the output amplitude of the AGC loop is operating near its fully converged state $A_{OUT} \approx V_{REF}$, or equivalently, $(y-z) \ll 1$, the exponential function in (2.14) can be expanded in Taylor series as shown below:

$$e^{y(t)} \approx e^z[1 + y(t) - z + \dots]. \quad (2.15)$$

Since $k_{c1}e^z = V_{REF}$, the following expression is obtained from (2.14):

$$\frac{dy}{dt} + k_x V_{REF} y(t) = \frac{dx}{dt} + k_x V_{REF} \log\left(\frac{V_{REF}}{k_{c1}}\right), \quad (2.16)$$

where the first-order linear system described by (2.16) again has a high pass response with the following time constant:

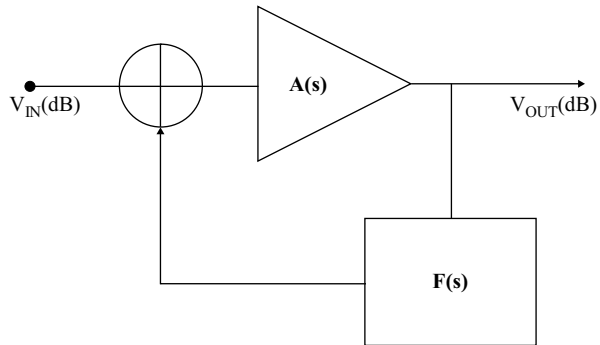
$$\tau = \frac{1}{V_{REF}k_x} = \left[\frac{1}{G(V_C)} \frac{dG}{dV_C} \frac{G_{M2}}{C} V_{REF} \right]^{-1}. \quad (2.17)$$

Bearing in mind once again the assumptions required to develop (2.11) and (2.12) (i.e. G_{M2} , C = constant and $G(V_C)$ exponential), the time constant is given by:

$$\tau_{\exp} = \frac{C}{G_{M2}k_{G1}V_{REF}}. \quad (2.18)$$

Notice that in this case the settling time is a function of the input variable V_{REF} indicating that the system is fundamentally nonlinear. On the contrary, (2.13) is independent of any bias condition, since in this case the circuit is perfectly modelled as a linear system in the logarithmic domain.

Fig. 2.4 Equivalent AGC loop diagram



Although the most popular, solution (2.11) is not the only way to achieve a constant settling-time. As shown in (2.9), the function of the time constant depends on more parameters which can be employed to fix it to a constant value. In fact, a more general solution would be to consider a variable G_{M2} , while C is kept constant due to the difficulty in varying its value in a continuous way. In this more general case, the settling-time will be constant if

$$\frac{G_{M2}}{G(V_C)} \frac{dG}{dV_C} = k_x C = \text{constant}. \quad (2.19)$$

Many solutions exist which satisfy (2.19), however in this chapter only the simplest one will be commented on briefly. This solution, already proposed in [9], is to consider again a linear variation G with the control voltage V_C , but in this case G_{M2} varies in the same way as G . Therefore, dG/dV_C is constant due to its linear dependence and $G_{M2}(V_C)/G(V_C)$ is constant because both functions are changed together in the same way. Thus, a constant settling-time is achieved without employing any complex function.

A second key issue in feedback AGCs is the stability of the loop. As in any other feedback loop, designer must be careful when choosing parameters to guarantee the loop is stable for all conditions. Consider the equivalent feedback AGC loop diagram in logarithmic domain shown in Fig. 2.4.

Its transfer function can be given as in standard feedback theory by

$$H(s) = \frac{A(s)}{1 + A(s)F(s)}. \quad (2.20)$$

where $A(s)$ is VGA transfer function and $F(s)$ is AGC loop transfer function.

For the study of stability, the well-known rules of feedback theory apply [16]. Many AGC stability analysis only consider the loop filter poles [17, 18]. However, in any practical AGC design, at least two other secondary poles should be considered: one main pole associated to the VGA and another one to the peak detector. Here, as we are only interested in minimum stability conditions and their effects on loop performance, just a first order filter, VGA and peak detector are considered to

simplify the analysis, but any higher number of poles would only introduce more limitations to loop stability conditions.

The choice of VGA main pole must be done considering input signal bandwidth and noise constraints. The pole must be high enough, so that the amplifier can manage the full input signal bandwidth. On the other hand, this pole cannot be chosen infinitely high as this is very power expensive and it would increase the noise introduced in the system. Thus, the usual choice is to match the VGA pole at the input signal highest frequency.

One of the simplest ways to detect signal strength is to first rectify and next filter it. To correctly detect signal strength, detector output ripple must be low. This is possible if the signal strength is detected by averaging many signal cycles. However, this also means that the detector pole is much lower than the main signal frequency or, in other words, much lower than the VGA pole.

Finally, AGC loop filter introduces a third pole. As said before, a first order filter is considered to simplify this analysis. The main function of this filter is to reduce the ripple generated by the detector to generate a cleaner control voltage. Thus, to accomplish this function and to avoid the stability problems generated by having two poles very close in a feedback loop, this pole is chosen still smaller than the peak detector pole, which at the same time was smaller than the VGA pole:

$$p_F \ll p_{PD} \ll p_{VGA}. \quad (2.21)$$

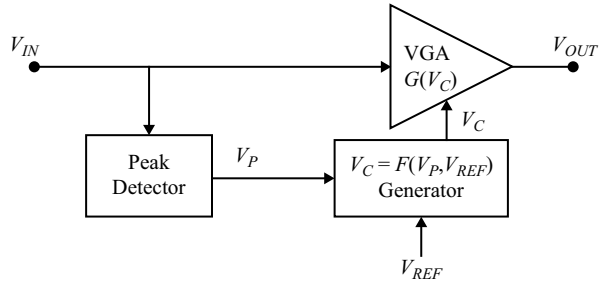
Consequently, the feedback AGC loop bandwidth is much smaller than VGA's one, so loop response is much slower than input signal. That is a limitation in fast-settling applications, as mentioned in Chap. 1.

2.1.2 AGC with Feedforward Loop

Feedforward loop does not have the stability problems which can arise in feedback loop, as the circuit is open loop [1]. This loop responds in a predefined way to the input signals and so, its settling-time depends only on the time required by the level detector to follow the input signal, which is usually much lower than the feedback loop filter time constant. In consequence, feedforward loop has much faster convergence and does not present the time-constant variation problems explained in Sec. 2.1.1.

A typical feedforward AGC scheme is shown in Fig. 2.5, which consists of a variable gain amplifier, a peak detector and a control voltage generation circuit. The nodes in this scheme have equivalent meaning to those of feedback AGC: V_{IN} is the input signal that must be adjusted; V_{OUT} is the output signal which must have a constant amplitude associated to V_{REF} ; V_P is the amplitude level detected by the peak detector; V_{REF} is the reference which fixes the required output amplitude; and V_C is the control signal generated as a function of V_P and V_{REF} to vary the gain of the VGA by means of function $G(V_C)$ to obtain the wanted output.

Fig. 2.5 Common block diagram of feedforward AGC



The key problem associated with feedforward AGCs is that the peak detector needs to be linear in the full VGA input dynamic range. This drawback can lead to a very power hungry detector or in some cases, makes its implementation impossible. In order to reduce the required dynamic range, multi-stage VGAs can be employed, so that the total input dynamic range is shared out between them and the detector sees only a small part of the full range.

2.2 Matlab Simulations

In order to verify the convergence response for the different AGC loops, behavioural simulations were carried out in Matlab using Simulink, a tool for modelling, simulating and analyzing multi-domain dynamic systems [19]. Five loop cases are analyzed: four feedback and one feedforward, one for each solution given in a previous section. Feedback models are based on Fig. 2.3 where different $G(V_C)$ are employed. The feedforward model is based on a VGA and loop linear in dB response; although any other function where the loop response is interrelated with the VGA gain function would ideally have the same result.

2.2.1 AGC with Feedback Loop

Simulink models based on the AGC loop in Fig. 2.3 are implemented for the feedback case. Differences are then introduced in the model depending on the function $G(V_C)$. All the cases will undergo the same test conditions so that a direct comparison can be made. To facilitate simulations, only amplitude signals are considered. The reference signal, V_{ref} is arbitrarily chosen equal to 0.1 V, but any other value would not affect the model dynamics. As a result, three different stepwise signals are introduced which start at $t = 0$ s with an amplitude of 0.2 V; at $t = 5$ μ s these signals change abruptly to 100, 20 or 2 mV, values which correspond to 6, 20 and 40 dB steps, respectively, and keep constant at these values until $t = 10$ μ s. The reference signal is set at 100 mV and the loop filter is chosen to have a DC gain equal to 20 dB.

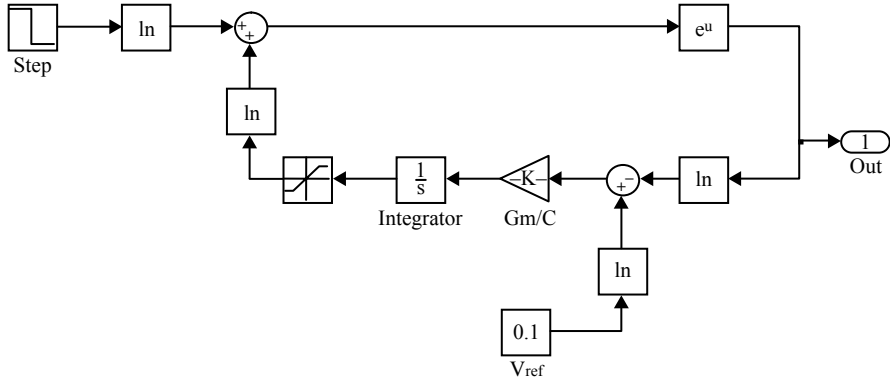
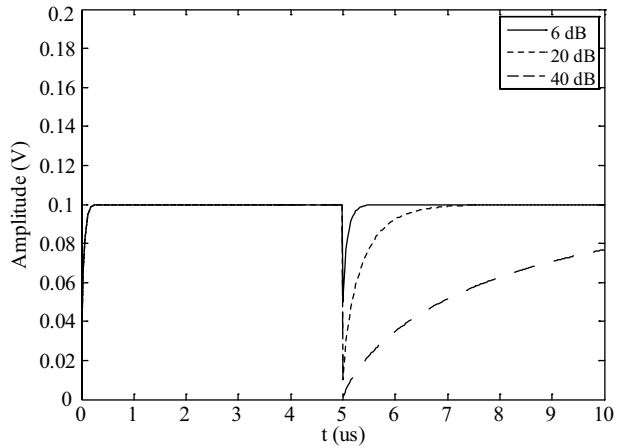


Fig. 2.6 AGC1: Simulink model

Fig. 2.7 Convergence response of AGC1 for different stepwise changes



2.2.1.1 Case 1: Linear AGC

The first analyzed case is the linear AGC, whose convergence is described by:

$$\tau = \left[\frac{1}{V_C} \frac{G_{M2}}{C} k_{c2} \right]^{-1}. \quad (2.22)$$

The equivalent Simulink model can be seen in Fig. 2.6, where $G(V_C) = V_C$.

According to (2.22), the settling-time of this AGC should increase as long as the input signal decreases. Thus, as expected, the output transient response shown in Fig. 2.7 validates the expected result for the linear AGC.

2.2.1.2 Case 2: Exponential AGC

The second case employs an exponential function $G(V_C)$ to obtain a constant settling-time as shown in

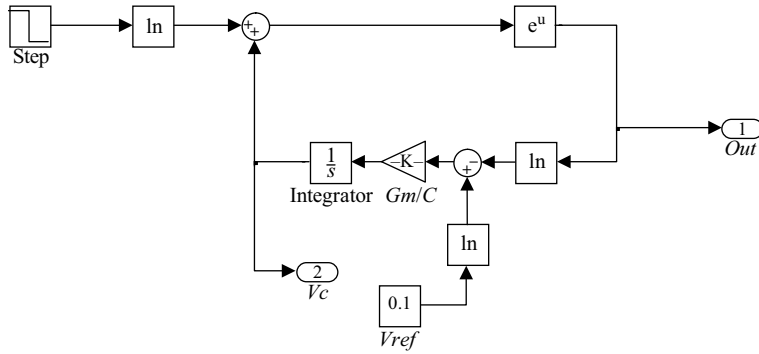
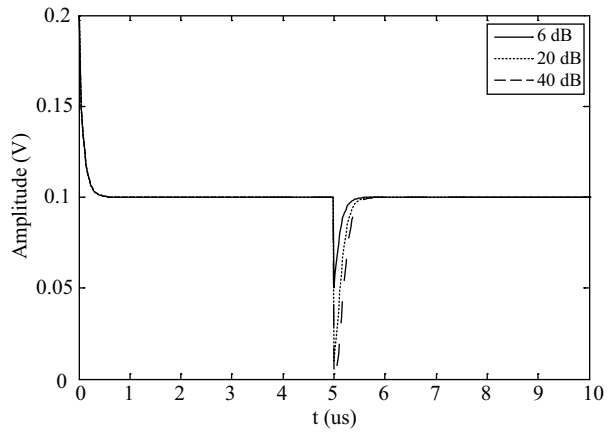


Fig. 2.8 AGC2: Simulink model

Fig. 2.9 Convergence response of AGC2 for different stepwise changes



$$\frac{1}{G(V_C)} \frac{dG}{dV_C} = k_{G1}, \quad (2.23)$$

which has the unique solution:

$$G(V_C) = k_{G2} e^{k_{G1} V_C}, \quad (2.24)$$

so

$$\tau_{\text{exp-log}} = \frac{C}{G_{M2} k_{G1} k_{c2}} = \text{constant}. \quad (2.25)$$

The employed Simulink model is the one in Fig. 2.8.

The same simulation conditions have been employed as in the previous model. Results are expressed in Fig. 2.9. The settling-time is constant and independent of any external parameter, this behaviour makes this AGC model one of the most popular options among AGC designers.

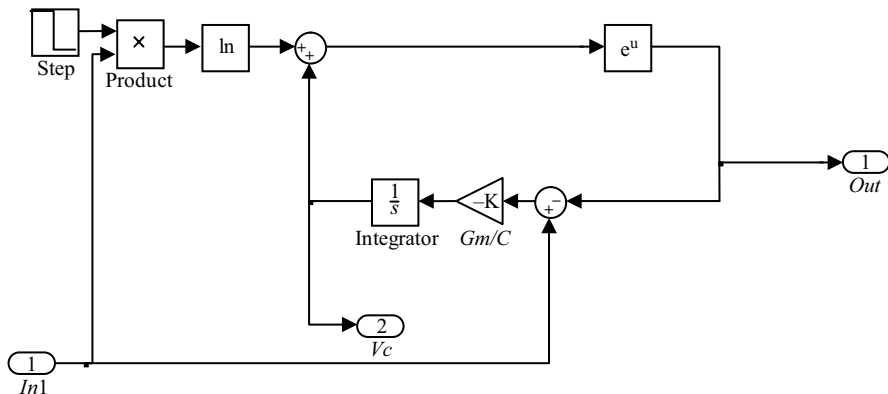
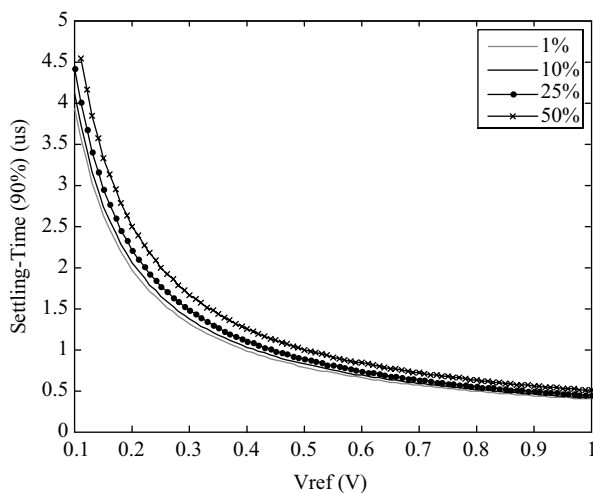


Fig. 2.10 AGC3: Simulink model

Fig. 2.11 Settling-time versus reference voltage for different input signal steps



2.2.1.3 Case 3: Exponential AGC without log-converter

The model in Fig. 2.8, still employs a logarithmic block in the AGC loop. This block is very complicated to be implemented in CMOS technology. However, it can be avoided. The Simulink model in Fig. 2.10 verifies this response, which was previously analyzed in (2.18):

$$\tau_{\text{exp}} = \frac{C}{G_{M2}k_{G1}V_{REF}}. \quad (2.26)$$

Considering small variations of the output signal versus the reference signal, this AGC settling-time could be considered constant. Figure 2.11 illustrates the variation of the time constant (defined as the time required to converge to $\pm 10\%$ of the

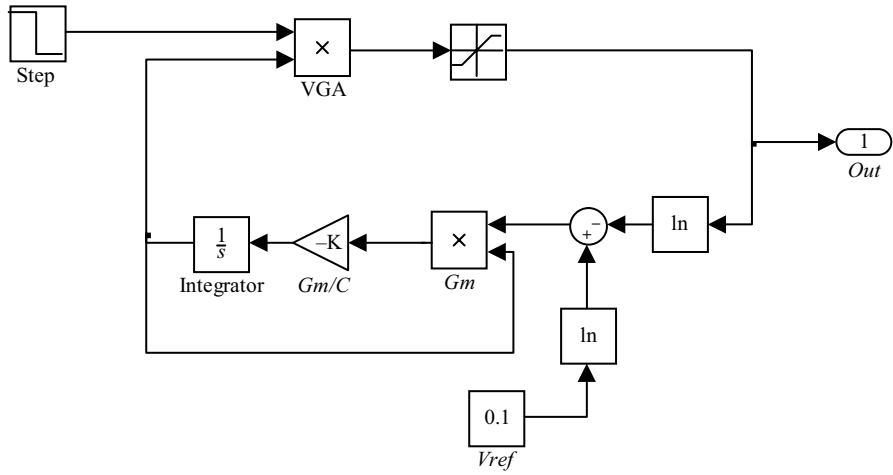


Fig. 2.12 AGC4: Simulink model

reference voltage) versus the reference voltage. The simulated response verifies that expected in (2.18). The same simulation has been carried out for input signals with changes around V_{REF} of 1, 10, 25 and 50%. Again, as expected, an almost constant settling-time is obtained where the response is degraded when the variation percentage increases.

2.2.1.4 Case 4: Linear VGA with linear loop filter

The last feedback AGC model means to verify the response expected from:

$$\frac{G_{M2}}{G(V_C)} \frac{dG}{dV_C} = k_x C = \text{constant}. \quad (2.27)$$

A linear $G(V_C)$ response is employed together with a linear $G_{M2}(V_C)$ filter response so that (2.27) is achieved. The corresponding Simulink model can be seen in Fig. 2.12.

This model ideally offers a constant settling-time and the response is confirmed in Fig. 2.13.

2.2.2 AGC with Feedforward Loop

Finally, in order to compare all previous feedback AGC models with a feedforward AGC, the model in Fig. 2.14 was simulated.

Fig. 2.13 Convergence response of AGC4 for different stepwise changes

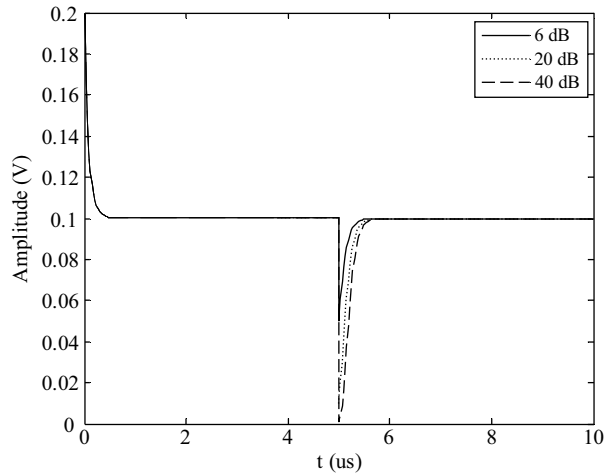
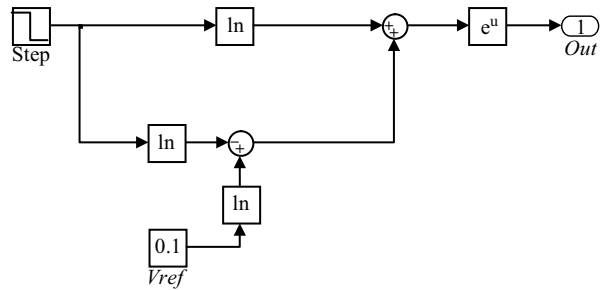


Fig. 2.14 AGC5: Simulink model



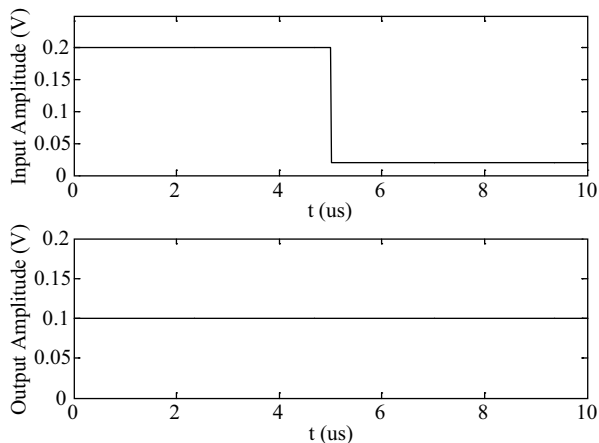
2.2.2.1 Case 5: Feedforward AGC

As shown in Fig. 2.4 and 2.14, no filter is needed in this AGC as stability will not suffer the lack of this block. Since the peak detector response is supposed to be immediate and given that ideally there is no other block to limit the frequency response of the loop, the ideal settling-time of this AGC is constant and immediate as shown in Fig. 2.15.

2.3 Conclusions

In this chapter, the two main AGC configurations have been introduced: feedback and feedforward loops. An analysis has been made which, though not exhaustive, it highlights each of the main topology properties. Furthermore, Simulink-Matlab toolbox has been employed to verify these results by behavioural simulation.

Fig. 2.15 Convergence response of AGC5 for a stepwise change



Each architecture offers different advantages and drawbacks, which must be taken into account when choosing one for a target application.

Conventional feedback AGC facilitates peak detector design and intrinsically offers higher linearity. On the other hand, high compression or expansion ratios make feedback processors more likely to exhibit instabilities; their correct design only allows the use of certain given control functions in order to obtain a constant settling-time circuit and furthermore, these circuits submit a trade-off between time constant and stability which precludes the possibility of designing AGCs with a very fast convergence.

Alternatively, feedforward AGC requires a highly linear peak detector; since it responds in a predefined way to the input signals. However, stability is not a concern in these AGCs. In consequence, settling-time can be made ideally zero and much faster convergence is achieved.

Due to the stringent time constraints in modern communication receivers, and due to the lack of available literature, this book will focus attention on the exploration of feedforward AGCs: new devices, circuits and techniques must be studied, developed and implemented to answer the demands of wireless technology, which is becoming ever faster, smaller and more complex. This study will be made mainly in standard CMOS technology, but also in SiGe BiCMOS technology which offers great advantages in performance with a cost difference that is rapidly increasing thanks to current submicron CMOS technologies.

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