An FPGA-Based Hardware Acceleration Platform for Low Density Parity Check Code Evaluation

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BACKGROUND AND MOTIVATION

- Error Correction Coding is a means to safeguard messages from being corrupted by noise

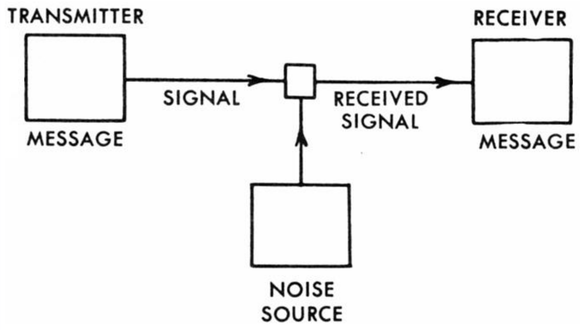

Figure 1: Schematic Diagram of a general communication system

- Low Density Parity Check (LDPC) Codes are a class of Error Correcting codes used in standards such as IEEE 802.11
- and WiMax [1]
- LDPC codes are designed through extensive computer simulations
- But software simulations take hours or even days to complete for low Bit Error Rate
- Sometimes, software simulations don't even reveal all the performance limitations about a particular code
  - For example, the phenomena of error flooring that occurs at a very low Bit Error Rate
- Can we do better than software simulations?

PROJECT GOAL

Design and implement a hardware acceleration platform for the simulation of Low Density Parity Check codes

PROJECT REQUIREMENTS

- The hardware platform shall be flexible enough to accommodate a wide variety of Low Density Parity Check Codes
- Due to limited FPGA resources, flexibility parameters are defined as follows:

Maximum size of parity check matrix	672 x 588
Maximum codeword length	672
Maximum degree of check node	32
Maximum degree of variable node	6
Number of iterations	Programmable
Supports both regular / irregular codes	Yes
Rates supported	N/M where N is in {1, …, 6} and M is in {1, …. , 32}

Table 1: Supported specifications of the hardware acceleration platform

DESIGN AND IMPLEMENTATION

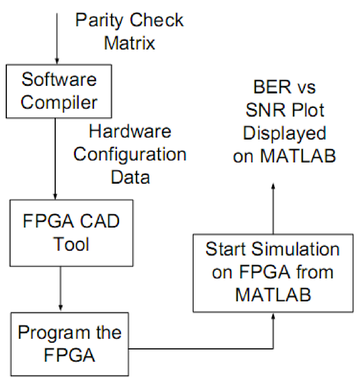

Figure 2: Hardware Emulation Flow

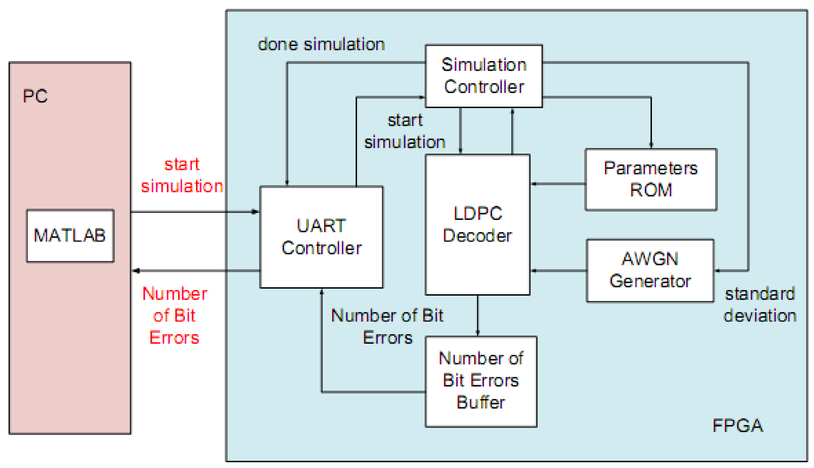

Figure 3: Hardware Emulation System

VERIFICATION AND RESULTS

- A software model was developed to verify the hardware decoder - 100% correlation of results was seen

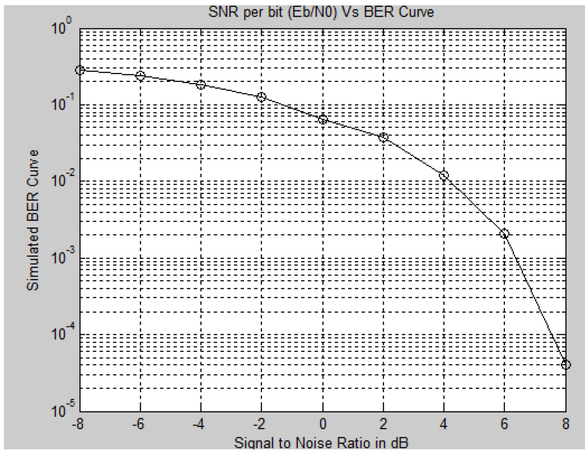

Figure 3: Generated BER vs. SNR plot

- As expected, the hardware outperformed the software in speed

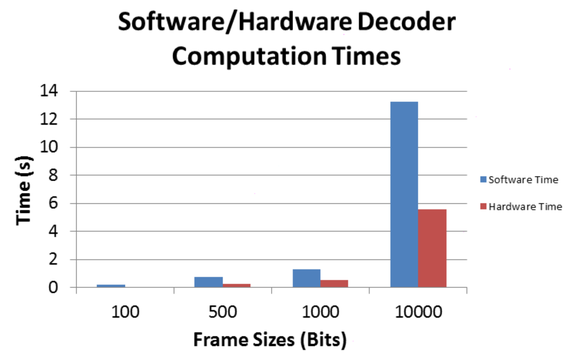

Figure 4: Comparison of decoding times

ACKNOWLEDGEMENTS

A special thanks to Professor Paul Chow for lending us the Xilinx board

REFERENCES

[1] R. Gallager. *Low-Density Parity-Check Codes*. PhD thesis, Massachusetts Institute of Technology, 1963.