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Sincerely yours,
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A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non-Idealities and Its Application — Part II: Full Device Model and Circuit Performance Benchmarking

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Abstract. This paper presents a complete circuit-compatible compact model for single-walled Carbon Nanotube Field-Effect Transistors (CNFETs), as an extension to the work in [1]. For the first time, a universal circuit-compatible CNFET model including the practical device non-idealities is implemented with HSPICE. In addition to the non-idealities included in [1], this paper includes the elastic scattering in the channel region, the resistive source/drain (S/D), the Schottky Barrier (SB) resistance, and the parasitic gate capacitances. More than one nanotube per device can be modeled.

Compared to silicon technology, CNFET show much better device performance based on the intrinsic CV/I gate delay metric (6× for nFET and 14× for pFET) than MOSFET device at the 32 nm node, even with device non-idealities. This large speed improvement is significantly degraded (by a factor of 5 to 8) by interconnect capacitance in a real circuit environment. We performed circuit performance comparison with all the standard digital library cells between CMOS random logic and CNFET random logic with HSPICE simulation. Compared to CMOS circuits, CNFET circuits with 1 to 10 CNTs per device is about 2× to 10× faster, the energy consumption per cycle is about 7× to 2× lower, and the energy-delay product (EDP) is about 15× to 20× lower, considering the realistic layout pattern and the interconnect wiring capacitance.

Index Terms: CNFET, Compact Model, Analytical Model, Carbon Nanotube, SPICE, Screening Effect, Performance Benchmarking

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1. Introduction

Ballistic or near-ballistic transport is observed with intrinsic CNT under low voltage bias because of the ultra long (~1μm) scattering mean-free-path (MFP) [2,3,4,5]. The quasi-1D structure provides better electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (e.g. fully depleted SOI) [6]. These properties make CNFET one of the promising new devices to extend or complement traditional silicon technology [7].

Various CNFET models at the device level have been reported in recent years [1,8,9,10,11]. In a previous paper [1], we report that there is ~13× CV/I improvement of intrinsic CNFET with (19,0) CNT over bulk n-type MOSFET at the 32 nm node. In order for CNFET to develop into a viable technology, the CNFET performance in a real circuit environment, instead of the intrinsic CNFET device performance, should be evaluated. The parasitic capacitance and resistance of the source/drain region and interconnect are likely to degrade the circuit performance. In addition, the performance degradation due to device and material parameter variations also needs to be considered [12]. In this paper, we start from the model reported in [1], and present a complete device model that includes the channel elastic scattering, the doped source/drain region, Schottky barrier (SB) resistance, multiple CNTs per device and other device/circuit non-idealities, and its applications.

This paper is organized as follows: first, we describe the organization of this model from the circuit point of view. Next, we show both the mathematical expressions and the circuit representations of each major component. Finally to illustrate the application of this model, we report the circuit performance comparison between CNFET and CMOS circuits at 32 nm node.

2. Circuit Topology

A MOSFET-like CNFET device structure (Fig. 1 in [1]) is used for the modeling in [1] and this paper because of both the fabrication feasibility and superior device performance of the

MOSFET-like CNFET as compared to the SB-controlled FET [1]. The complete CNFET device model is implemented hierarchically in three levels (Fig. 1). Device non-idealities are included hierarchically at each level. Level 1, denoted as CNFET_L1, models the intrinsic behavior of MOSFET-like CNFET. The model at this level is similar to the device-level models such as [8,9]. The second level, denoted as CNFET_L2, includes the device non-idealities: the capacitance and resistance of the doped S/D CNT region, as well as the possible Schottky Barrier (SB) resistances of S/D contacts. The first two levels deal with only one CNT under the gate. The top level, denoted as CNFET_L3, models the interface between CNFET device and CNFET circuits. This level deals with multiple CNTs per device, and includes the parasitic gate capacitance and screening due to adjacent CNTs. This paper presents the second level and the third level model, as an extension to the first level model, CNFET_L1, in [1].

3. Device Model – The 2nd Level

As an extension to the first level CNFET model, CNFET_L1, of the intrinsic channel region [1], this level models the device non-idealities, including the elastic scattering in the channel region, the quantum / series resistance and the parasitic capacitance of the doped source/drain region, as well as the Schottky barrier resistance at the interface between the doped CNT and the source/drain metal contacts. The equivalent circuit diagram is shown in Figure 2.

3.1 Channel Resistance

We consider three typical scattering mechanisms in the channel region: (1) acoustic phonon scattering (near elastic process [5]), (2) optical phonon scattering (inelastic process [4]), and (3) elastic scattering. Both the acoustic phonon scattering and optical phonon scattering are treated in the first level device modeling [1]. The elastic scattering rate and thereby the MFP are assumed to be independent of the carrier energy. We include the elastic scattering in this paper in a computationally-efficient way.

Though the elastic scattering MFP of intrinsic CNT can be longer than 1 μm [3], the fabricated CNTs often contain non-ideal scattering centers (e.g. defects) which may degrade the MFP significantly and in turn cause additional potential drop along the channel region. The total potential drop (V_{DS}) across the channel region is a summation of the potential drop ($V_{ch,DS}$) due to the channel quantum resistance $R_{ch,c}$ and the potential drop ($V_{ch,el}$) over the channel resistance $R_{ch,el}$ due to the elastic scattering (Fig. 3), i.e. $V_{DS} = V_{ch,DS}+V_{ch,el}$, $V_{ch,DS} = I_{DS}R_{ch,c}$ and $V_{ch,el} = I_{DS}R_{ch,el}$. $R_{ch,el}$ equals to $(1-T_{ch})/T_{ch}\cdot R_{ch,c}$ [13], where T_{ch} is the transmission probability in the channel region, $T_{ch}=l_{eff} / (L_g+l_{eff})$, L_g and l_{eff} are the channel length and the effective elastic scattering MFP, respectively. We further assume the MFP l_{eff} is linearly proportional to the nanotube's diameter [14,15], i.e. $l_{eff} = D_{CNT}/(1.5\text{nm})\cdot\lambda_{eff}$ where D_{CNT} is the CNT diameter and λ_{eff} (~200 nm [16]) is the elastic scattering MFP for 1.5 nm in diameter CNT. With the above equations, we can represent the potential drop over $R_{ch,el}$ as,

$$V_{ch,el} = \frac{L_g}{L_g + \frac{D_{CNT}}{1.5nm}\cdot l_{eff}} V_{DS} \qquad (1)$$

Representing the effect of the channel resistance due to elastic scattering as a voltage-controlled voltage source $V_{ch,el}$ (Fig. 2) can avoid calculating $R_{ch,el}$ directly, thereby simplifying the computation.

3.2 Doped Source/Drain CNT

The heavily doped nanotube regions of CNFET act as both the source/drain extension region and the local interconnect between two adjacent devices. We use a π model to represent the equivalent circuit of the doped source/drain region (Fig. 2).

Resistance: First, we discuss the model for the resistance of the doped CNT region. Similar to the channel region, CNT can be either metallic or semiconducting. The source/drain resistance is modeled as two paralleled resistors: $R_{semi,s}$ ($R_{semi,d}$) due to the semiconducting sub-bands, and

$R_{metal,s}$ ($R_{metal,d}$) due to the metallic sub-bands of metallic nanotubes. We consider two typical cases for device connectivity: (1) the drain of one CNFET is connected to the source of another CNFET, i.e. the doped CNT acts as interconnect between two devices in series (Fig. 4(a)) without a metal contact in between; (2) the drain/source of one CNFET is connected to the metal contact, e.g. at the output node (Fig. 4(b)). For the first case, the two segment doped nanotubes should be the same as one continuous doped nanotube in the model, i.e. the potential profile along the two segments is continuous (Fig. 4(a)). Furthermore, we describe the device intrinsic behavior with source/drain input Fermi levels (μ_s, μ_d) as above, while the input source Fermi level μ_s of one device is connected to the output source Fermi level μ_s' of another device (Fig. 4). Thus we need to convert the output port of the equivalent circuit model from μ_d to μ_s' for this case. For the second case, the ideal metal contact is an electron reservoir that has infinite DOS and acts as an infinite scattering center so that there is additional potential drop across the boundary between the doped CNT and the metal contact (called the quantum contact resistance [13]) due to mode mismatch (Fig. 4(b)). The device model is able to handle both cases correctly as described below.

We define two parameters S_{out} (D_{out}) representing the source/drain connectivity: equal to 0 if source (drain) is connected to doped CNT, otherwise equal to 1. Consider the Fermi level profiles for both cases in Figure 4, following a similar approach as in Section 3.1, we obtain the total effective resistance of the doped source/drain region,

$$R_{x,s} = L_s /(l_{sd} G_{x,c}) \qquad (2a)$$

$$R_{x,d} = h_{deff} / G_{x,c} \qquad (2b)$$

$$h_{deff} = \begin{cases} (L_d - l_{sd}) / l_{sd} & , D_{out} = 0 \\ L_d / l_{sd} & , D_{out} = 1 \end{cases} \qquad (2c)$$

The subscript x denotes either "*semi*" or "*metal*". L_s and L_d are the lengths of the doped

source and drain region, respectively. λ_{sd} is the impurity scattering MFP, assumed a constant with a default value of 15 nm, a pessimistic estimation, for degenerately doped nanotubes. A longer MFP, 20 nm to 50 nm, can be derived from the work in [17] with charge transfer doping.

$G_{x,c}$ is the quantum conductance of doped CNT. $G_{x,c}$ depends on CNT diameter, the doping level (E_f), and the source and drain Fermi level difference ($eV_c=|\mu_s-\mu_d|$). With applied bias at the two ends, the source and drain Fermi levels splits apart (the inset in Fig. 5) by V_c which results in carrier re-distribution between $+k$ states and $-k$ states while keeping the total number of carriers Q_o the same. Denoting the surface potential changes by $\Delta\Phi_s$ referred to the source Fermi level, the total carriers of semiconducting sub-bands per unit length are given by,

$$Q_o = \sum_{\substack{k_m \\ m=1}}^{M} \int_{E_{m,0}}^{E_{\max}} \frac{D(E)}{2} \cdot [\, f_{FD}(E - E_f - \Delta\Phi_s) + f_{FD}(E - E_f - \Delta\Phi_s + V_c)]dE \qquad (3)$$

$f_{FD}(E)$ is the Fermi-Dirac distribution function. $E_{m,0}$ is the half band gap of the m^{th} sub-band, and k_m is the wave number due to the quantum confinement in the circumferential direction [1]. $D(E)$ is the CNT universal density of states (DOS) [18], given by

$$D(E) = \begin{cases} D_0 \cdot E / \sqrt{E^2 - E_{m,0}^2} & E > E_{m,0} \\ 0 & E \le E_{m,0} \end{cases} \qquad (4a)$$

$$E_{m,0} = \frac{\sqrt{3}}{2} a V_p k_m \qquad (4b)$$

D_o is a constant $8/(3\pi V_\pi \cdot d)$ where d is the carbon-carbon bond distance, about 0.144 nm. For heavily doped nanotubes of typical CNFETs, we assume the doping level E_f is above the first semiconducting subband, but does not exceed the third semiconducting subband. At room temperature, $f_{FD}()$ is quite steep, thus the normalized charge $Q_{Ef} = 2Q_o/D_o$ with small V_c is approximately,

$$Q_{Ef} \approx \begin{cases} 2\sqrt{E_f^2 - E_{1,0}^2} & , E_{1,0} < E_f < E_{2,0} \\ 2\left(\sqrt{E_f^2 - E_{1,0}^2} + \sqrt{E_f^2 - E_{2,0}^2}\right) & , E_{2,0} \le E_f < E_{3,0} \end{cases} \quad (5)$$

At the point $V_c = E_f - E_{1,0} + \Delta\Phi_{s,\max}$, Q_{Ef} is given by,

$$Q_{Ef} \approx \begin{cases} \sqrt{(E_f + \Delta\Phi_{s,\max})^2 - E_{1,0}^2} & , E_{1,0} < E_f + \Delta\Phi_{s,\max} < E_{2,0} \\ \sqrt{(E_f + \Delta\Phi_{s,\max})^2 - E_{1,0}^2} + \sqrt{(E_f + \Delta\Phi_{s,\max})^2 - E_{2,0}^2} & , E_{2,0} \le E_f + \Delta\Phi_{s,\max} < E_{3,0} \end{cases} \quad (6)$$

Equating the equations (5) and (6), we obtain the maximum surface potential change,

$$\Delta\Phi_{s,\max} \approx \begin{cases} \sqrt{{Q_{Ef}}^2 + E_{1,0}^2} - E_f & , E_{1,0} < E_f + \Delta\Phi_{s,\max} < E_{2,0} \\ \dfrac{\sqrt{(E_{2,0}^2 - E_{1,0}^2)^2 + 2(E_{2,0}^2 + E_{1,0}^2){Q_{Ef}}^2 + {Q_{Ef}}^4}}{2Q_{Ef}} - E_f & , E_{2,0} \le E_f + \Delta\Phi_{s,\max} < E_{3,0} \end{cases} \quad (7)$$

Q_{Ef} is given by equation (5). We assume the ratio of ($\mu_s - E_f$) over ($E_f - \mu_d$) is constant respect to V_c in the non-saturation region ($V_c < E_f - E_{1,0} + \Delta\Phi_{s,\max}$), thus the surface potential change is normalized as,

$$\Delta\Phi_s(V_c) = \Delta\Phi_{s,\max} \frac{\min(V_c, E_f - E_{1,0} + \Delta\Phi_{s,\max})}{E_f - E_{1,0} + \Delta\Phi_{s,\max}} \quad (8)$$

Following the similar approach in [1], we obtain the quantum conductance of the semiconducting sub-bands,

$$G_{semi,c}(V_c) = \frac{4e^2}{h} \sum_{\substack{k_m \\ m=1}}^{2} \left[1 + \frac{kT}{eV_c} \ln\left(\frac{1 + e^{(E_{m,0} - E_f - \Delta\Phi_s)/kT}}{1 + e^{(E_{m,0} - E_f - \Delta\Phi_s + eV_c)/kT}} \right) \right] \quad (9)$$

The analytic model accurately describes the quantum conductance of doped semiconducting CNT as a function of bias provided $E_f > E_{1,0}$, compared to the more accurate numerical simulation results with tight banding band structure [19] (Fig. 5). With small drain bias ($V_c < E_f - E_{1,0} + \Delta\Phi_{s,\max}$), $G_{semi,c}$ can be approximated as a constant, $G_{semi,c} \approx 4e^2/(\mathrm{m} \cdot h)$, where m is the number of sub-bands below E_f. With large drain bias ($V_c > E_f - E_{1,0} + \Delta\Phi_{s,\max}$), e.g. in the saturation region, the maximum surface potential change referred to μ_s will be pinned at $\Delta\Phi_{s,\max,}$ and the

drain Fermi level will be pushed below the first sub-band which cause a rapid increase in resistance. Therefore the source/drain resistance increases with increasing current (drain bias). On the other hand, the quantum conductance of the metallic sub-bands is almost independent of bias because the DOS is constant, $G_{metal,c} = (1\text{-}m0)4e^2/h$, where $m0$=0 if mod(n_1-n_2,3)=0 with (n_1, n_2) CNT, otherwise 1. The internal parameter V_c is related to the circuit parameter $V_{series,s}$ or $V_{series,d}$ (the potential drop over the series resistor at the source side or the drain side, respectively) by equation $V_c = V_{series,d}/\eta_{deff} = V_{series,s}\lambda_{sd}/L_s$. With the above equations, we are ready to calculate the source/drain resistance as voltage controlled resistors ($R_{semi,s}$, $R_{semi,d}$, $R_{metal,s}$, $R_{metal,d}$).

Capacitance: Similar to the channel region [1], there are two implementations for the extrinsic capacitor network: (1) the 6-capacitor model consists of the electrostatic capacitance and quantum capacitance (Fig. 2(a)), or (2) the 4-capacitor model with 4 trans-capacitances (Fig. 2(b)). The two implementations are equivalent in terms of ac response. The 4 equivalent capacitances can be expressed in terms of the six physical capacitors in Figure 2(a) by,

$$C_{gzz} = \frac{L_z \cdot C_{of} C_Q}{2(C_Q + C_{of} + C_{sub})} \qquad \text{(10a)}$$

$$C_{bzz} = \frac{L_z \cdot C_{sub} C_Q}{2(C_Q + C_{of} + C_{sub})} \qquad \text{(10b)}$$

The subscript "*z*" denotes either "*s*" or "*d*", thus L_z is the length of either source or drain. C_Q is the quantum capacitance of the doped source/drain region. For the channel region, we need to model C_Q accurately because the gate capacitance (C_{ox}) is comparable to C_Q. However, for the heavily doped CNT region, C_Q (~400 aF/μm per sub-band) is typically much larger than the electrostatic capacitance (C_E) between CNT and ground (typically << 100aF/μm). Thus we approximate C_Q to first order as $C_Q = [\Theta(E_f - E_{1,0}) + \Theta(E_f - E_{2,0})] \times 400$ aF/μm, where $\Theta(x)$ is a step function that equals to 1 if $x > 0$, otherwise 0. For multiple CNTs per gate, the gate outer-fringe capacitance (C_{of}), are grouped into the fringe capacitance between gate and S/D CNT at the two

edges (C_{of_e}) and the fringe capacitance between gate and S/D CNT in the middle (C_{of_m}) in this work, as described in [20].

3.3 Schottky Barrier Resistance

Schottky Barrier (SB) may exist at the interface between CNT and metal contact [21,22,23], and in carbon nanotube heterojunctions between metallic and semiconducting CNTs [24]. In this paper, we use a simplified model to describe SB resistance between doped CNT and metallic electrode to include some signature effects of SB on device performance. We made the following simplifying assumptions in this model: (1) the doped CNT region is long enough so that there is no surface potential modification due to the quantum confinement within a short CNT; (2) dipole effects are ignored; (3) no pinning effects [25]; (4) the depletion profile is steep. Figure 6(a) shows an example of the potential profile of SB at the source side. In this simple model, we only consider tunneling through the first sub-band, assuming the carriers injecting from the metal contact can re-distribute over all the sub-bands near the contact region. The potential barriers seen by the carriers at the metal contact side (Φ_1) and the doped CNT side (Φ_2) are given by,

$$\Phi_1 = \Phi_M - \Phi_C + E_{1,0} \qquad (11a)$$

$$\Phi_2 = \begin{cases} \Phi_1 + \left|V_{sb,s}\right| + \Delta\Phi_s & , Source - SB \\ \Phi_1 - \left|V_{sb,d}\right| - V_c + \Delta\Phi_s & , Drain - SB \end{cases} \qquad (11b)$$

$V_{sb,s}$ and $V_{sb,d}$ are the potential drops over the equivalent SB resistor at the source side and drain side, respectively, from the equivalent circuit point of view. Φ_M and Φ_C are the metal work function and CNT work function, respectively. With positive bias V_{DS} and V_{GS}, the carriers of the source side see a higher SB, while the carriers of drain side see a lower SB.

With doping level E_f, the normalized volume doping density is,

$$N_D = \frac{32E_{1,0}^2}{3p^2V_p^3d^3}\sqrt{E_f^2 - E_{1,0}^2} \qquad (12)$$

The depletion length is then approximately,

$$W_d = \sqrt{\frac{2k_2 e_0}{eN_D} V_{bi}} \qquad (13a)$$

$$V_{bi} = E_f - E_{1,0} + \Phi_2 \qquad (13b)$$

V_{bi} is the build in potential with applied bias. For low doping level (< 2×10^{-4}), the depletion width for CNT is microns or so, precluding a nanoscale device [23]. At high doping (> 10^{-3}), the length scale becomes small enough so that the contact is essentially ohmic through tunneling. The conduction band potential profile is,

$$E_C(x) = \frac{eN_D(W_d - x)^2}{2k_2 e_0} + E_{1,0} - E_f - \Phi_2 + \Phi_1 \qquad (14)$$

We approximate the potential profile with a triangular potential profile with the same classical turning points, 0, W_1 (before bias), and W_2 (after bias) (Fig. 6(a)),

$$W_1 = \sqrt{\frac{2k_2 e_0}{eN_D}}\left(\sqrt{V_{bi}} - \sqrt{E_f - E_{1,0} + \Phi_2 - \Phi_1}\right) \qquad (15a)$$

$$W_2 = \sqrt{\frac{2k_2 e_0}{eN_D}}\left(\sqrt{V_{bi}} - \sqrt{E_f - E_{1,0}}\right) \qquad (15b)$$

Using the WKB approximation, we obtain the tunneling probability through a triangular potential barrier with height v and width w,

$$\ln T \cong -2\int_0^w |k(x)|dx = -\frac{4\sqrt{2m^*}w\sqrt{v}}{3\mathbf{h}} = -\frac{4w}{9r}\sqrt{\frac{2v}{E_{1,0}}} \qquad (16)$$

The average transmission probability through the 1st sub-band is approximately,

$$T_{SB} \approx \frac{\int_{\Phi_1}^{\Phi_2} T dE}{\Phi_2 - \Phi_1} \approx \frac{2}{3(\Phi_2 - \Phi_1)t^{\frac{2}{3}}}\left[\Gamma(\frac{2}{3}, t\cdot\Phi_1^{\frac{3}{2}}) - \Gamma(\frac{2}{3}, t\cdot\Phi_2^{\frac{3}{2}})\right] \qquad (17a)$$

$$t \approx \frac{4\sqrt{2}\cdot W_2}{9r\sqrt{E_{1,0}}\cdot\Phi_2} \qquad (17b)$$

The potential barrier height Φ_2 and thickness W_2 depends on the bias. With high degenerate doping which is satisfied in this work, to improve run-time, the above equation can be approximated with,

$$T_{SB} \approx 0.5 \times \left(\exp(-t \cdot \Phi_1^{\frac{3}{2}}) + \exp(-t \cdot \Phi_2^{\frac{3}{2}}) \right) \quad (18)$$

The equivalent SB series resistance is then given by,

$$R_{sb} = \frac{1}{G_{semi,c}} \left(\frac{1}{T_{SB}} - 1 \right) (1 - X_{out}) \quad (19)$$

The symbol *"X"* denotes either "S" (source side SB) or "D" (drain side SB) which are defined as either 0 or 1 in Section 3.2. The SB resistance is modeled as a voltage-controlled resistor (Fig. 2). The equations in this section are highly simplified and only valid for heavily doped CNT, i.e. $E_f > E_{1,0}$, otherwise the performance of CNFET will be heavily limited by source/drain resistance which is out of the scope of this work[+]. With this model, we can observe that the source (drain) SB resistance increases (decreases) with increased source-drain current (incresed V_{DS} and V_{GS}) due to the increased (reduced) SB seen by the carriers tunneling from doped CNT to metal contact (Fig. 6(b)). With high doping (~0.8%) and $\Phi_M = \Phi_C = 4.5$ eV, SB resistance can be suppressed to a small value (<1 KΩ) compared to the typical device resistance (~40 KΩ), thus it can be ignored in most applications if this high level of doping can be achieved experimentally [26,27].

4. Device Model – The 3rd Level

This level is the top level of the device model, which allows for multiple CNTs for each device (Fig. 7). Consider the case where there are N CNTs under the gate. The CNTs are grouped into (1) a number of min(N,2) CNTs at the two edges; (2) the other (N-min(N,2)) CNTs in the middle. The direct coupling capacitance (C_{gsub}) between gate and the substrate is simply

[+] For a more accurate model of the short channel SB-controlled CNFET, see [22].

expressed as $C_{gsub} \approx 2\pi L_g k_2 \varepsilon_0 / \ln(4H_{sub}/H_{gate})$, where H_{sub} is the insulating bulk thickness and H_{gate} is the gate height. C_{gsub} is about 1 aF, about 1/3 of the gate intrinsic capacitance, assuming a 10 μm thick SiO_2 bulk, a 64 nm gate height and a 32 nm channel length, and an infinitely large substrate.

5. Gate and Interconnect Parasitic Capacitance

To be compatible with CMOS process, we assume CNFET circuits use the same conventional metal interconnect technology (the feature size is defined by photolithography) as that for silicon technology. Consider the layout in Figure 1, the gate parasitic capacitance between gate and the adjacent gate/source/drain contacts per unit length is given by Equ. 19 in [20]. For devices at 32 nm node (L_{sd}=32nm, L_g=32nm, H_{gate}=64nm, k_2=3.9), C_{gtg} is about 110 aF/μm for one side (each gate has two sides). Thus C_{gtg} of such a device with 32 nm gate width is about 11 aF (including Miller effect) which is more than 2× larger than the intrinsic gate capacitance (~ 4 aF per CNT channel). Therefore, it is very important to include the extrinsic parasitic capacitances for ac performance evaluation.

6. CNFET Device and Circuits Performance

In this section, we compare our model with experimental data and use the model to project circuit performance of CNFET circuits. The above model is implemented in HSPICE[+].

Both the dc and ac performance evaluated with the device model match well with the experimental data of the fabricated CNFET RF device [16]. The observable 10% mismatch between the simulation and the experimental data may due to two reasons: (1) this model uses simplified band structure. This may introduce inaccuracy for the DOS which will affect the transconductance. (2) We assume a linear potential profile in both the channel region and the source/drain region which may not be accurate enough for the fabricated device.

[+] The same model is also implemented in Verilog-A and is available at https://www.stanford.edu/group/nanoelectronics/model_downloads.htm

Next, we evaluate CNFET device and circuits performance at the 32 nm node with a 0.9 V power supply for high performance logic. All CNTs are assumed to be (19, 0) semiconducting carbon nanotubes with 1.5 nm diameter, and 0.6 eV (~0.8%) source/drain doping level[++], otherwise specified. The gate dielectric is 3 nm thick HfO_2 (dielectric constant k_1=16) on top of 10 μm thick SiO_2. The metal work function is assumed to be the same as the CNT work function (4.5 eV). Figure 8 shows the device current in the presence of non-idealities. The ballistic current of a 32 nm gate length CNFET is about 42 μA. The scattering in the channel region decreases the on-current by about 10%. The SB resistance further reduces the on-current by another 5%. The largest current drive detractor is the source/drain series resistance due to the heavily doped CNTs, which reduces the on-current to 22 μA. Compared to silicon bulk CMOS technology (benchmarked with the BSIM4 predictive model [28,29,30]), CNFET shows better single device performance based on intrinsic CV/I gate delay metric (6× for nFET and 14× for pFET) than MOSFET (where C is the intrinsic gate capacitance) in the 32 nm node, even with device non-idealities (Table 1). The device performance improvement (~ 6× for nFET) is smaller than the value (~13×) reported in [1], because the current is degraded by about a factor of two due to the source/drain extension resistance and SB resistance considering the actual device layout.

The CNFET circuit performance depends on CNT diameter. Figure 9 shows CNFET inverter fan-out of one (FO1) delay as a function of the CNT diameter (simulated by choosing CNTs with different chiral number (n_1, n_2) randomly). The off current per unit gate capacitance is set to the same as that of MOSFET by setting the appropriate flat band gate voltage (V_{FB}). The effective gate capacitance is almost independent of CNT diameter (Fig. 9 inset). This is because only the first subband is likely to be populated in with sub-1V power supply (assuming the same off current). The CNT diameter dependence of the on-current comes from the source/drain

[++] The effect of a mixture of CNT chirality and doping variations have been reported in [12] using this model.

resistance, instead of the channel resistance. The Fermi level of doped CNTs with different diameters is almost constant (~ 0.6 eV) for the same doping level (0.8%), as shown by the lower-left inset in Figure 9. As a result, for CNTs of less than 1.3 nm in diameter, only the first subband is degenerate which results in a higher source/drain resistance and a smaller current drive and, therefore, lower speed (Fig. 9). This result illustrates the need to account for the band structure of the CNT correctly in the compact model. It further shows that in order to avoid large variation of circuit speed, the CNT diameter should be targeted away from the 1.25 nm range with 0.8% doping level.

For the CNFET inverter with one CNT per device without including gate parasitics and interconnect capacitance, the FO1 delay (~ 0.6 ps) is about 10 times smaller than that of 32 nm bulk CMOS inverter. This result corroborates the performance improvement at the device level reported in Table 1. Though large improvement of CNFET over CMOS can be potentially achieved at the device level, the circuit performance is likely to be limited by the circuit parasitics, e.g. the interconnect capacitance. Next, we consider the realistic layout pattern for CNFET circuits. All the related interconnect capacitances are extracted and included in the circuit simulation.

We now compare CNFET circuit performance with CMOS circuits benchmarked with the standard digital library cells. The number of CNTs per device, m, is increased from 1 to 10 in order to evaluate the trade-off between speed and energy. The FO1 speed improvement of the ideal CNFET (CNFET_L1 intrinsic device without any parasitics) circuits over bulk CMOS circuits is about 20× to 40× (Fig. 10(a)). This large number is degraded by a factor of 2 or so, represented by the curve with “Cload=0” in Fig. 10(a), by the source/drain and SB resistance considering the device layout. After including the interconnect wiring capacitance extracted from the circuit layout pattern, the speed improvement of CNFET circuits with one CNT per device

over bulk CMOS circuits is further degraded to ~ 2×, by another factor of 5 or so, because of the small CNT quantum-capacitance-limited effective gate capacitance. Increasing the number of CNTs per device illustrates the trade-off between the speed and energy consumption. With 1 to 10 CNTs per device, the FO1 speed of CNFET circuits is about 2× to 10× faster compared to CMOS circuits (Fig. 10(a)), the energy consumption per cycle is about 7× to 2× lower (Fig. 10(b)), and the energy-delay product is about 15× to 20× lower (Fig. 10(c)). Large advantages of CNFET circuits over CMOS circuits can be potentially achieved even with the traditional (Cu) interconnect technology.

7. Summary

We present a circuit-compatible compact model for single-walled Carbon Nanotube Field-Effect Transistors (CNFETs), as an extension to [1]. A universal model including the practical device non-idealities is implemented with HSPICE. More than one CNT per device is allowed, and the screening effect by the parallel channels is also included in the device model. Good agreement for both dc and ac characteristics between the device model and the experimental data has been verified with the fabricated CNFET RF device.

The source/drain resistance and SB resistance degrade CNFET on-current by a factor of 2 at the 32 nm node. Compared to silicon technology, CNFET shows better device performance (based on the intrinsic CV/I gate delay metric (6× for nFET and 14× for pFET)) than MOSFET device at the 32 nm node, with device non-idealities. This large speed improvement is significantly degraded (~5× degradation) by interconnect capacitance in a real circuit environment. Increasing the number of CNTs per device is the most effective way to improve the circuit speed. Compared to CMOS circuits, CNFET circuits with 1 to 10 CNTs per device is about 2× to 10× faster, the energy consumption per cycle is about 7× to 2× lower, and the energy-delay product (EDP) is about 15× to 20× lower, considering the realistic layout pattern

and the interconnect capacitance.

Further improvements to the implemented device model may include the following: (1) This model utilizes a simplified band structure which restricts the use of this model for the applications that requires a high power supply and high CNT surface potential (>>1.0eV). A more complete band structure model can alleviate this issue. Separating the operation region into multiple sections and deriving approximated analytical equations in each section is another way to both enlarging the applicable range and improving the run time. (2) For a better sub-threshold behavior modeling, the surface potential lowering and consequent higher current caused by the holes (electrons) pile up in the nFET (pFET) channel region should be considered, especially in the high bias region ($V_{ch,DS} > E_{1,0}$) [1,31]. (3) We ignored the diffusion capacitance due to the minor carriers at the source/drain junctions which may affect the ac response of small signal analog circuits. (4) One way to further improve CNFET circuit performance is to use metallic CNTs, multi-walled CNTs, or large diameter CNTs as interconnects because of the much higher current density and much smaller parasitic fringe capacitance. Thus a simple and universal interconnect model, similar to the model by [32], is necessary to evaluate all-CNT CNFET circuit performance. The kinetic inductance may also be included as discussed in Appendix. (5) A more accurate device model should also include the defect and device reliability analysis. Most of the carrier scattering and thermal relaxation processes occur around the contact/junction region due to the near-ballistics transport, thus defects are likely to accumulate along the nanotubes especially around the contact region for short gate CNFET.

Acknowledgements

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Appendix: Discussion on Inductance

In this part, we estimate with first order approximation if inductance needs to be included in the CNFET device model. Since the magnetic inductance is about 4 orders smaller than the kinetic inductance [33], we ignore the magnetic inductance in this work. The simplest CNT model is a transmission line (Fig. 4 in [33]) . With "*N*" modes contributing to the current flow, the quantum resistance is about 25.6/*N* kΩ [13]. Assuming ~1μm elastic scattering mean free path (MFP) for the optimistic intrinsic CNT and ~50nm for the doped CNT, the series resistance (R_s) is ~25.6/*N* kΩ/μm and ~512/*N* kΩ/μm, respectively. The kinetic inductance (L_k) is ~16/*N* nH/μm, and the quantum capacitance (C_Q) is ~100*N* aF/μm [33]. The shunt capacitance (C_s) is the series combination of the quantum capacitance (C_Q) and the electrostatic capacitance (C_E) due to the gate electrode, i.e. $C_s = C_Q C_E/(C_Q+C_E)$. The critical frequencies at which the conductance of the inductor and capacitor become comparable to the series resistance are $f_L=R_s/(2\pi L_k)$ and $f_c=1/(2\pi R_s C_s)$, respectively. f_L is independent of the CNT length, and f_c is a function of the inverse square of CNT length. Both f_L and f_c are independent of the number of modes. There are three typical cases: (1) In the intrinsic channel region: R_s is typically much larger than 25.6/*N* kΩ/μm in the saturation region, say 80/*N* kΩ/μm in the optimal case (~50μA on-current per doubly degenerated subband with 1V power supply), and $C_s \approx C_Q$. Thus f_L ~ 800 GHz, and f_c ~ 20 GHz·μm^2. (2) In doped CNT source/drain region: R_s is about 512/*N* kΩ/μm in the linear region and assuming $C_s \approx C_E \approx 30$ aF/μm << C_Q, which gives f_L ~ 5 THz and f_c ~ 10.4*N* GHz·μm^2. (3) For intrinsic metallic CNT as an interconnect: f_L ~ 255 GHz and f_c ~ 207*N* GHz·μm^2. For CNFET, the inductance becomes significant when the signal frequency is higher than 800 GHz in the channel region and 5 THz in the source/drain region, respectively, which are far beyond our interested frequency range for typical applications. For metallic CNT interconnect, the kinetic inductance becomes significant above 255 GHz and its effect is more significant than the effect of C_Q with interconnect length shorter than 1.8 μm (assuming *N*=4). Local, device level metallic CNT bridge wiring is unlikely to be as long as 1.8 μm. Thus we ignore the inductance for CNFET device modeling. However, kinetic inductance must be included for metallic CNT and/or larger diameter CNT interconnect modeling.

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Figure Captions:

Figure 1. The complete CNFET device model is implemented with hierarchical three levels. Level 1, CNFET_L1, models the intrinsic behavior of CNFET. The second level, CNFET_L2, includes the device non-idealities. The first two levels deal with only one CNT under the gate. The top level, CNFET_L3, models the interface between CNFET device and CNFET circuits. This level deals with multiple CNTs per device, and includes the parasitic gate capacitance and screening due to adjacent CNTs.

Figure 2. The 2nd level equivalent circuit model CNFET_L2 for CNFET. (a) The 6-capacitor model, and (b) the 4-capacitor model.

Figure 3. The Fermi level profile for 1-D device with series resistance (finite MFP along CNT). The Fermi level profile is approximated as a linear function of the position along the channel.

Figure 4. The related Fermi level profiles for (a) Two CNFETs are connected with doped CNT, and (b) two CNFETs are connected by an ideal metal contact (without considering the Schottky Barriers between CNT and metal interface). Superposed are the equivalent source/drain resistors.

Figure 5. Comparison of the quantum resistance calculated with the analytical model and the more complete numerical simulations with tight binding band structure, for (19,0) semiconducting CNT with a doping level which varies from 0.4 eV to 0.7 eV. The inset shows the *E-k* dispersion relationship and the Fermi levels (the solid arrows denote the Fermi levels with smaller V_c and the dashed arrows denote the Fermi levels with larger V_c) for doped nanotube with (n-type) doping level E_f. The shaded regions are filled with electrons. With applied drain bias, the source Fermi level (μ_s) and drain Fermi level (μ_d) splits apart due to the finite carrier DOS. Referred to μ_s, the surface potential of nanotube changes by $\Delta\Phi_s$. $\Delta\Phi_{s,max}$ is the maximum

surface potential change with applied bias V_c.

Figure 6. (a) The energy band diagram for the contacted metal and doped CNT with bias. The potential barrier in the tunneling region (shaded area) is approximated as a triangle potential barrier. (b) Schottky Barrier (SB) resistances as a function of the current, with different metal/CNT work functions and different CNT doping levels. Both smaller barrier height and higher CNT doping level help to reduce SB resistance significantly.

Figure 7. The 3rd level equivalent circuit model CNFET_L3 for CNFET. There are N nanotubes under the gate. These CNTs are grouped into (1) a number of min(N, 2) CNTs at the two edges; (2) the other N-min(N, 2) CNTs in the middle. All CNTs in each group are treated identically. C_{gtg} is the gate parasitic coupling capacitance connected between the gate and the source/drain/ground or the gate of the adjacent devices, according to the device layout.

Figure 8. The drain current @ (V_{gs}=0.9V, V_{FB}=0V) for (19, 0) chirality CNFET with incremental device non-idealities. The front gate dielectric is 3 nm thick HfO_2, and insulating bulk is 10 μm thick SiO_2. The metal work function and CNT work function are 4.6eV and 4.5eV, respectively.

Figure 9. The FO1 delay vs. CNT diameter for CNFET inverter at the 32 nm node. Gate parasitic capacitance and interconnect capacitance are not included. The lower-left inset shows the first two subbands (E_1, E_2) and the Fermi level (E_f) with 0.8% doping level. The upper-right inset shows both the on-current (lest axes) and the effective gate capacitance (right axes) as a function of CNT diameter. The off-currents of CNFETs are trimmed to the same as that of MOSFET, as shown in Table 1.

Figure 10. (a) The circuit speed, (b) dynamic energy per cycle, and (c) the energy-delay-product (EDP) comparison between CMOS circuits and CNFET circuits with realistic layout pattern and

interconnect capacitance, in 32 nm technology node. All values are normalized to the performance of a CMOS FO1 inverter. The number of nanotubes per device (m) for CNFET circuits ranges from 1 to 10. Also shown are the relative performances of CNFET circuits (1) without interconnect capacitance (Cload=0), and (2) with ideal CNFET (assuming zero series resistance for doped CNTs, and zero parasitic capacitance).

Table Captions:

TABLE1. The gate effective capacitance and on-current comparison between CNFET and MOSFET at the 32 nm node. The off-currents per gate capacitance for CNFET and MOSFET are adjusted to the same value.

Figures:

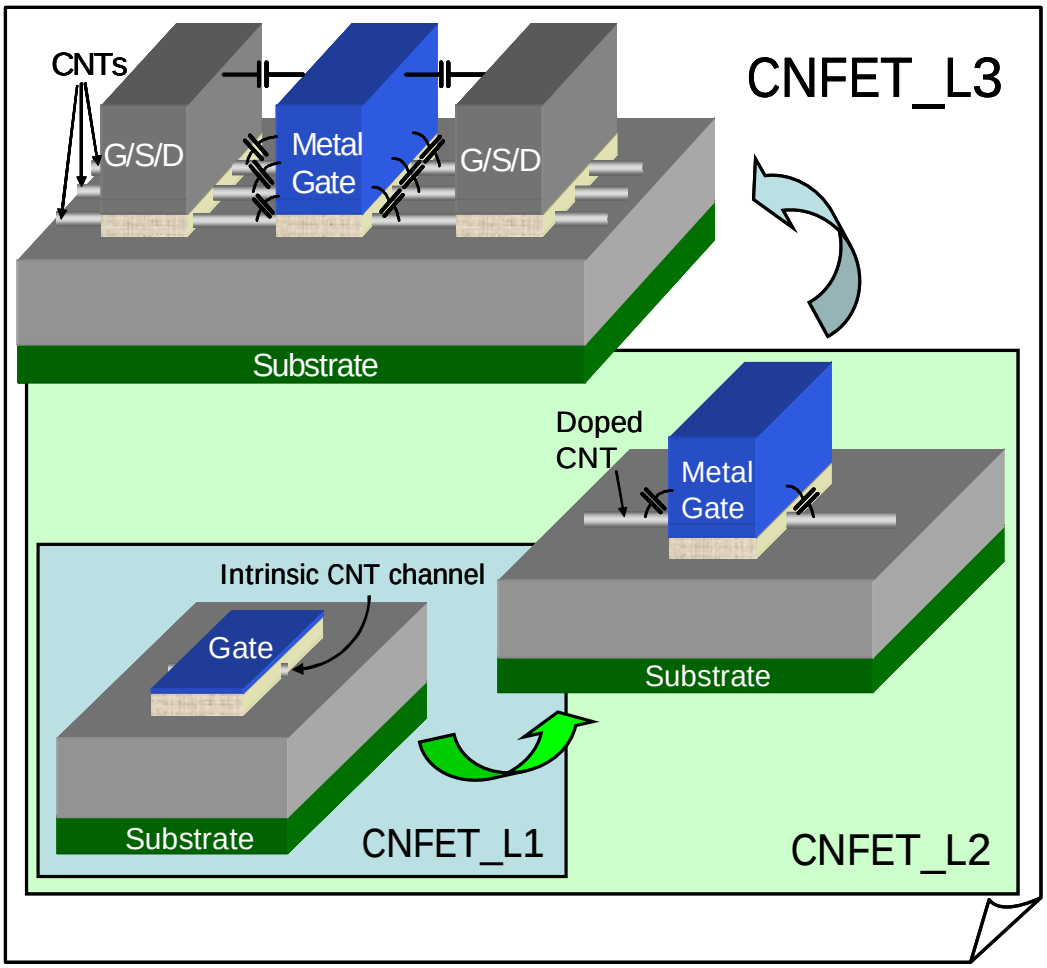
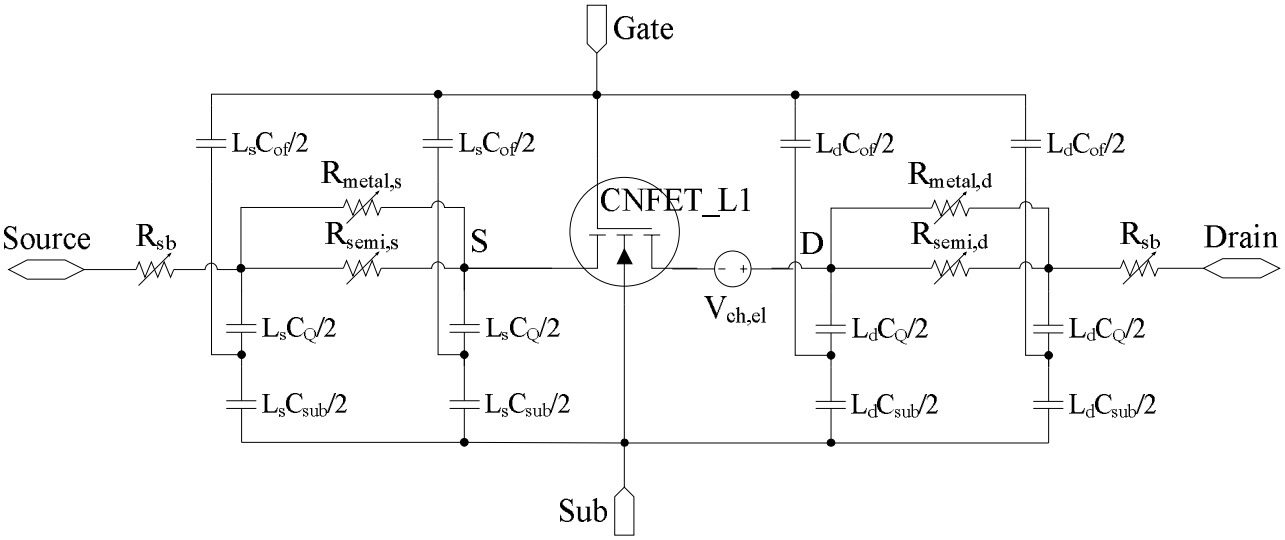
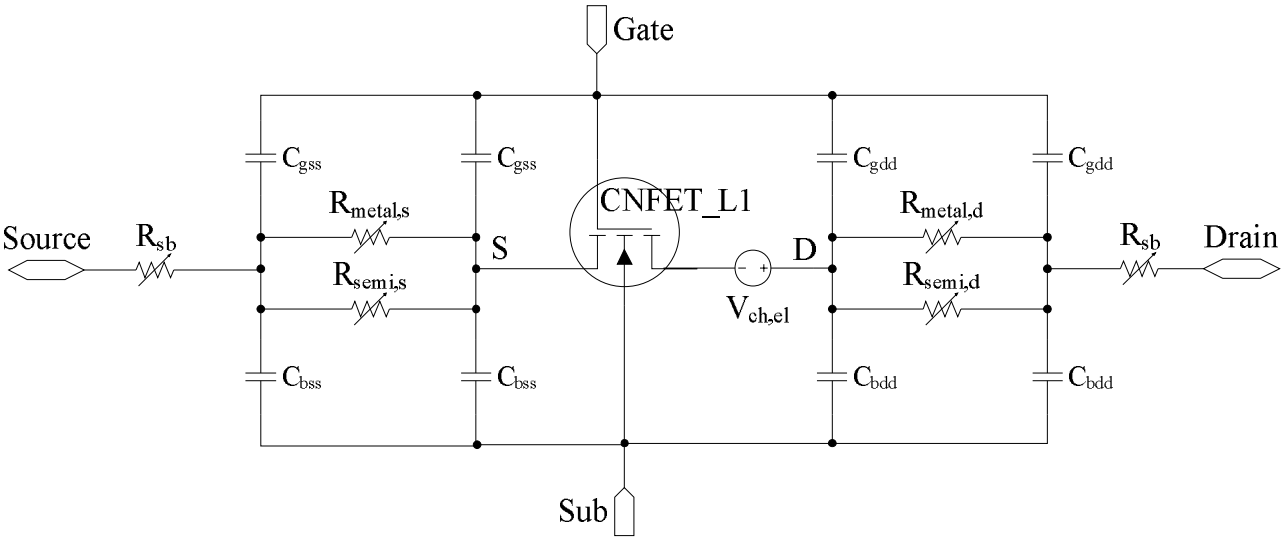


Figure 1.


Gate
$L_sC_{of}/2$
$L_sC_{of}/2$
$L_dC_{of}/2$
$L_dC_{of}/2$
$R_{metal,s}$
$R_{metal,d}$
CNFET_L1
Source
R_{sb}
$R_{semi,s}$
S
D
$R_{semi,d}$
R_{sb}
Drain
$V_{ch,el}$
$L_sC_Q/2$
$L_sC_Q/2$
$L_dC_Q/2$
$L_dC_Q/2$
$L_sC_{sub}/2$
$L_sC_{sub}/2$
$L_dC_{sub}/2$
$L_dC_{sub}/2$
Sub

(a)


Gate
C_{gss}
C_{gss}
C_{gdd}
C_{gdd}
$R_{metal,s}$
CNFET_L1
$R_{metal,d}$
Source
R_{sb}
S
D
R_{sb}
Drain
$R_{semi,s}$
$R_{semi,d}$
$V_{ch,el}$
C_{bss}
C_{bss}
C_{bdd}
C_{bdd}
Sub

(b)

Figure 2.

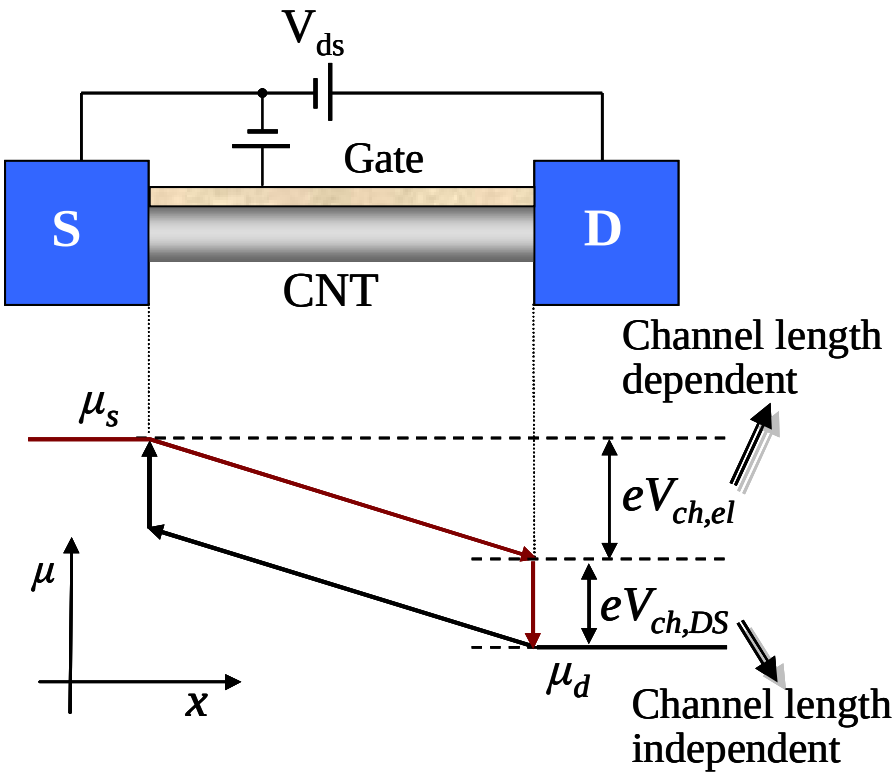
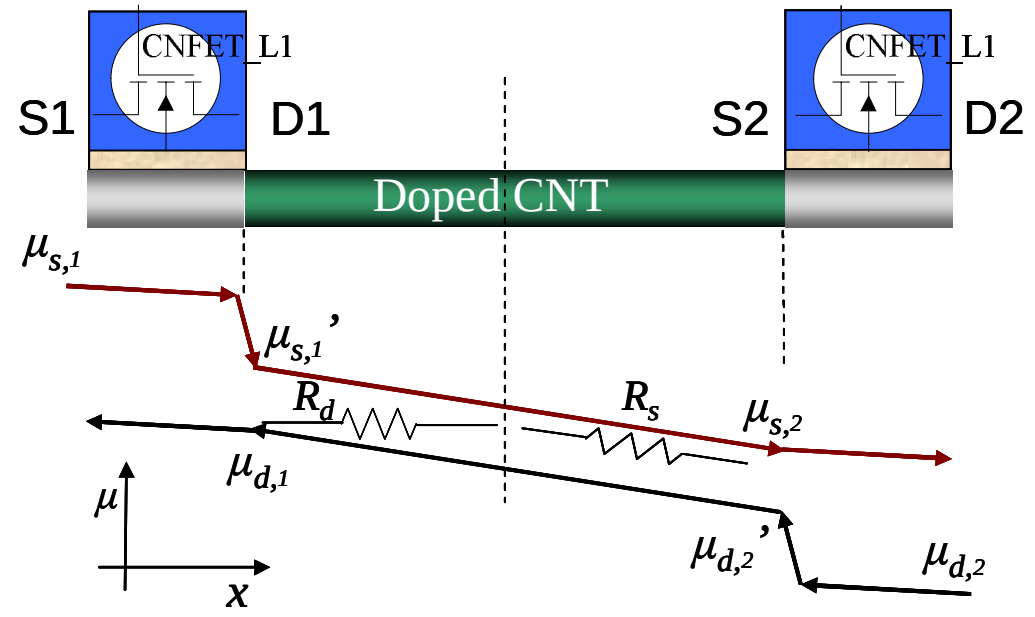
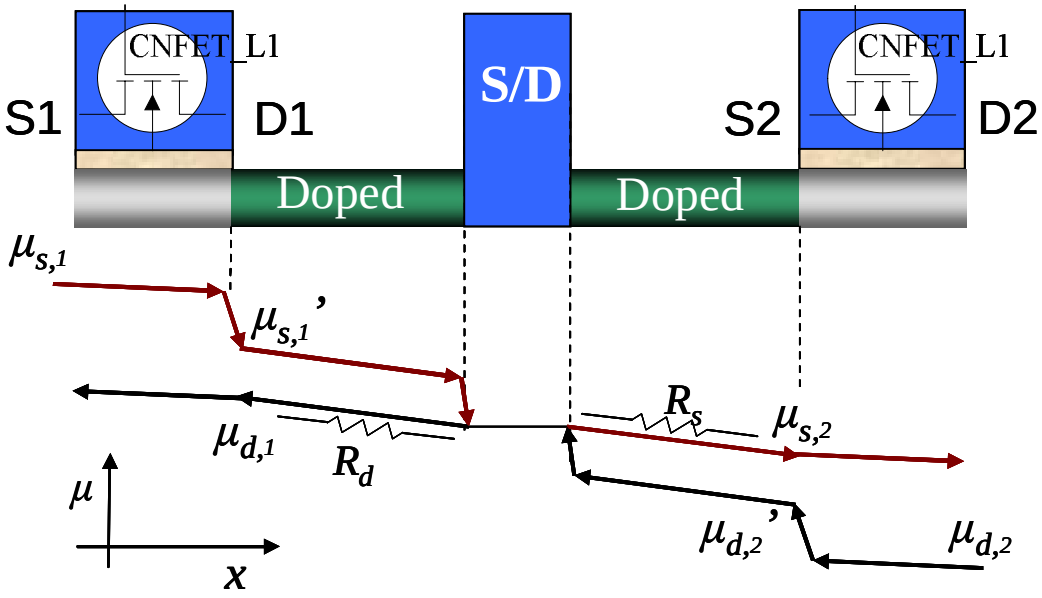

V ds
Gate
S
D
CNT
Channel length dependent
μs
eVch,el
eVch,DS
μd
μ
x
Channel length independent

Figure 3.


CNFET_L1
CNFET_L1
S1
D1
S2
D2
Doped CNT
$\mu_{s,1}$
$\mu_{s,1}$'
R_d
R_s
$\mu_{s,2}$
$\mu_{d,1}$
μ
x
$\mu_{d,2}$'
$\mu_{d,2}$

(a)


CNFET_L1
CNFET_L1
S/D
S1
D1
S2
D2
Doped
Doped
$\mu_{s,1}$
$\mu_{s,1}$'
R_s
$\mu_{s,2}$
$\mu_{d,1}$
R_d
μ
x
$\mu_{d,2}$'
$\mu_{d,2}$

(b)

Figure 4.

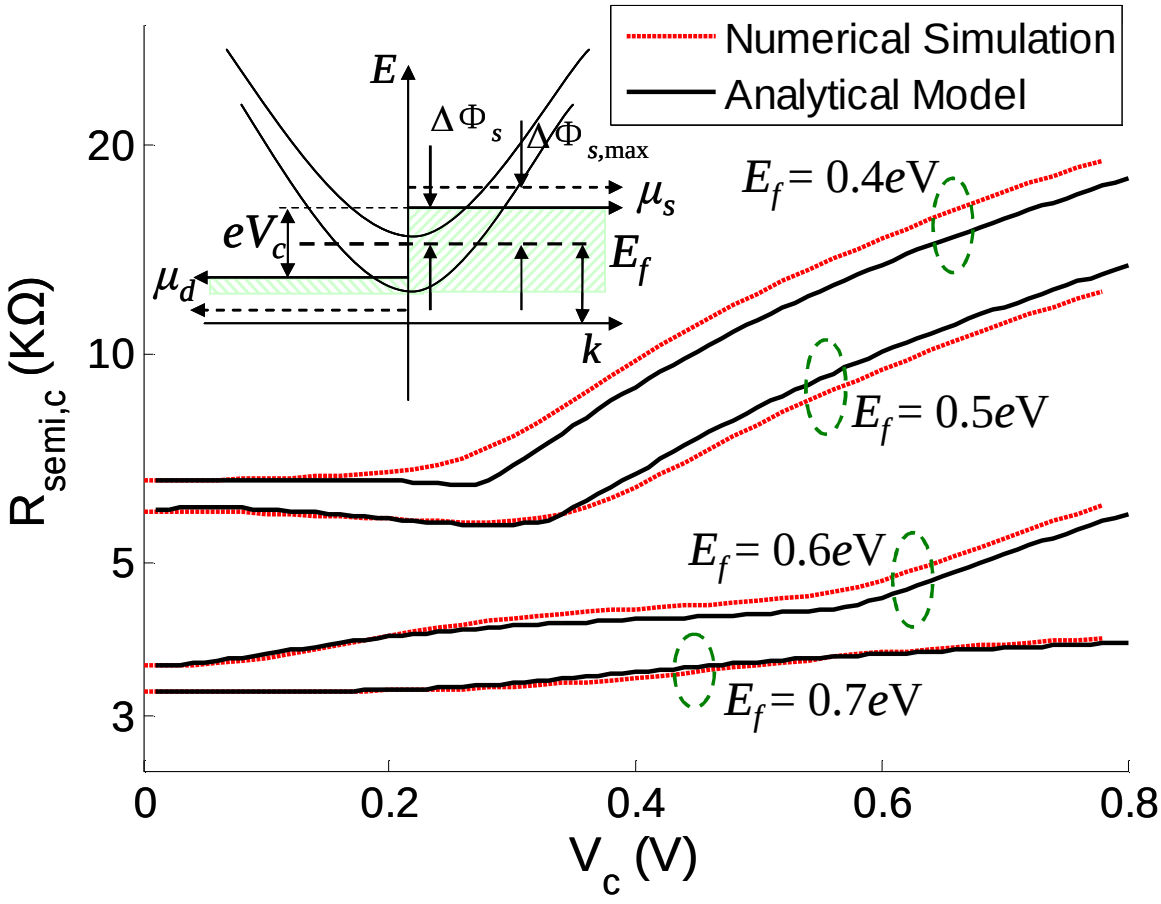
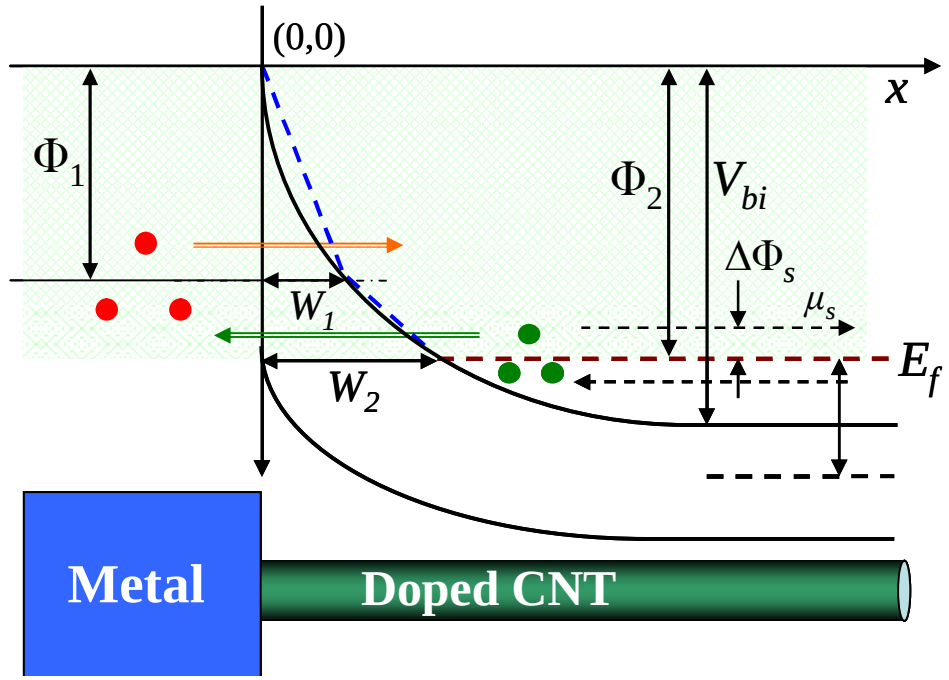
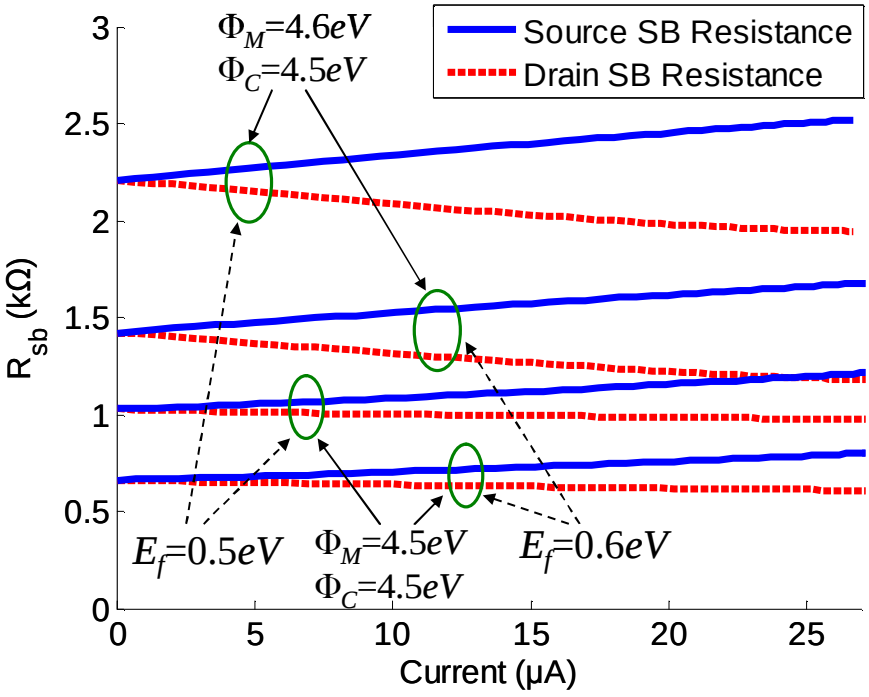

Numerical Simulation
Analytical Model
E
ΔΦ_s
ΔΦ_s,max
μ_s
eV_c
E_f
μ_d
k
E_f = 0.4eV
E_f = 0.5eV
E_f = 0.6eV
E_f = 0.7eV
R_semi,c (KΩ)
V_c (V)
20
10
5
3
0
0.2
0.4
0.6
0.8

Figure 5.


(0,0)
x
Φ_1
Φ_2
V_{bi}
$\Delta\Phi_s$
μ_s
W_1
W_2
E_f
Metal
Doped CNT

(a)


Φ_M=4.6eV
Φ_C=4.5eV
Source SB Resistance
Drain SB Resistance
R_{sb} (kΩ)
Current (μA)
E_f=0.5eV
Φ_M=4.5eV
Φ_C=4.5eV
E_f=0.6eV

(b)

Figure 6.

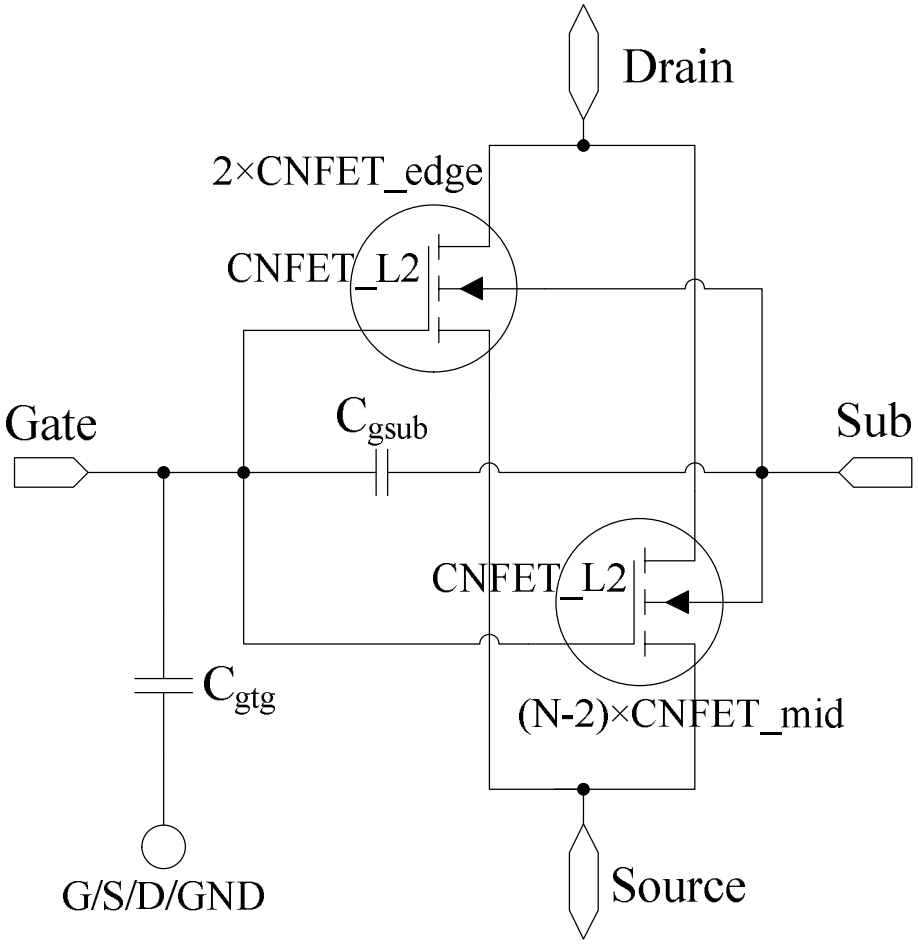

Drain
2×CNFET_edge
CNFET_L2
Gate
C_{gsub}
Sub
CNFET_L2
C_{gtg}
(N-2)×CNFET_mid
G/S/D/GND
Source

Figure 7.

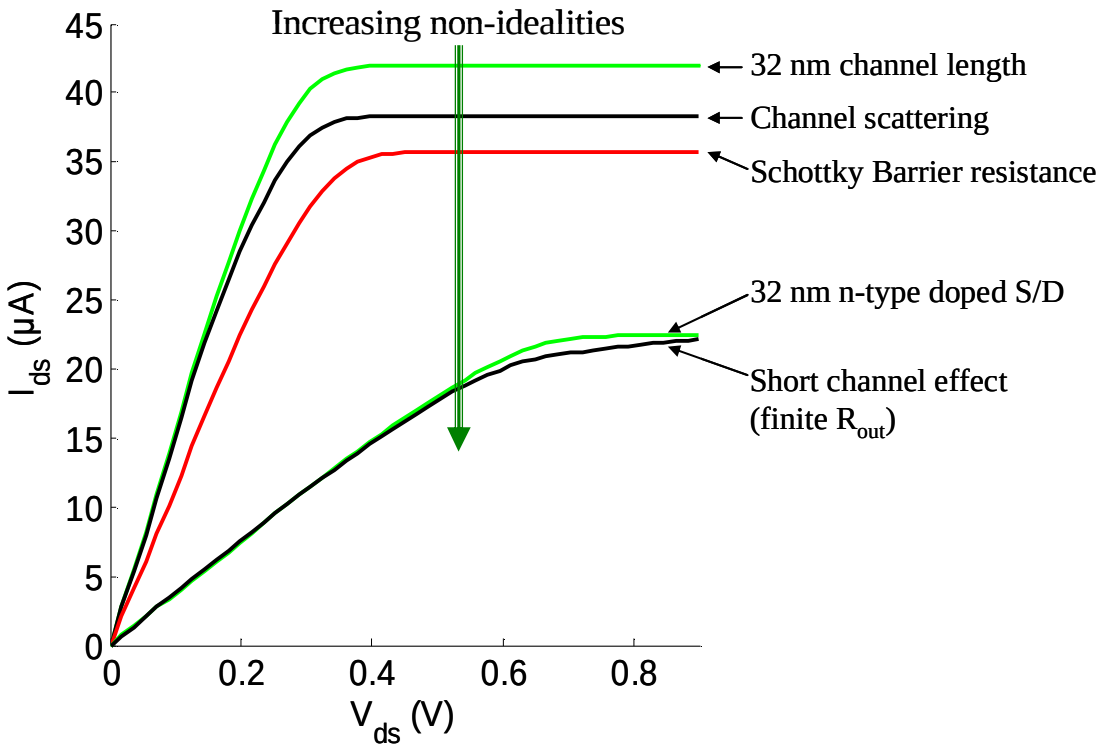

Increasing non-idealities
32 nm channel length
Channel scattering
Schottky Barrier resistance
32 nm n-type doped S/D
Short channel effect
(finite R_out)
I_ds (μA)
V_ds (V)
0
5
10
15
20
25
30
35
40
45
0
0.2
0.4
0.6
0.8

Figure 8.

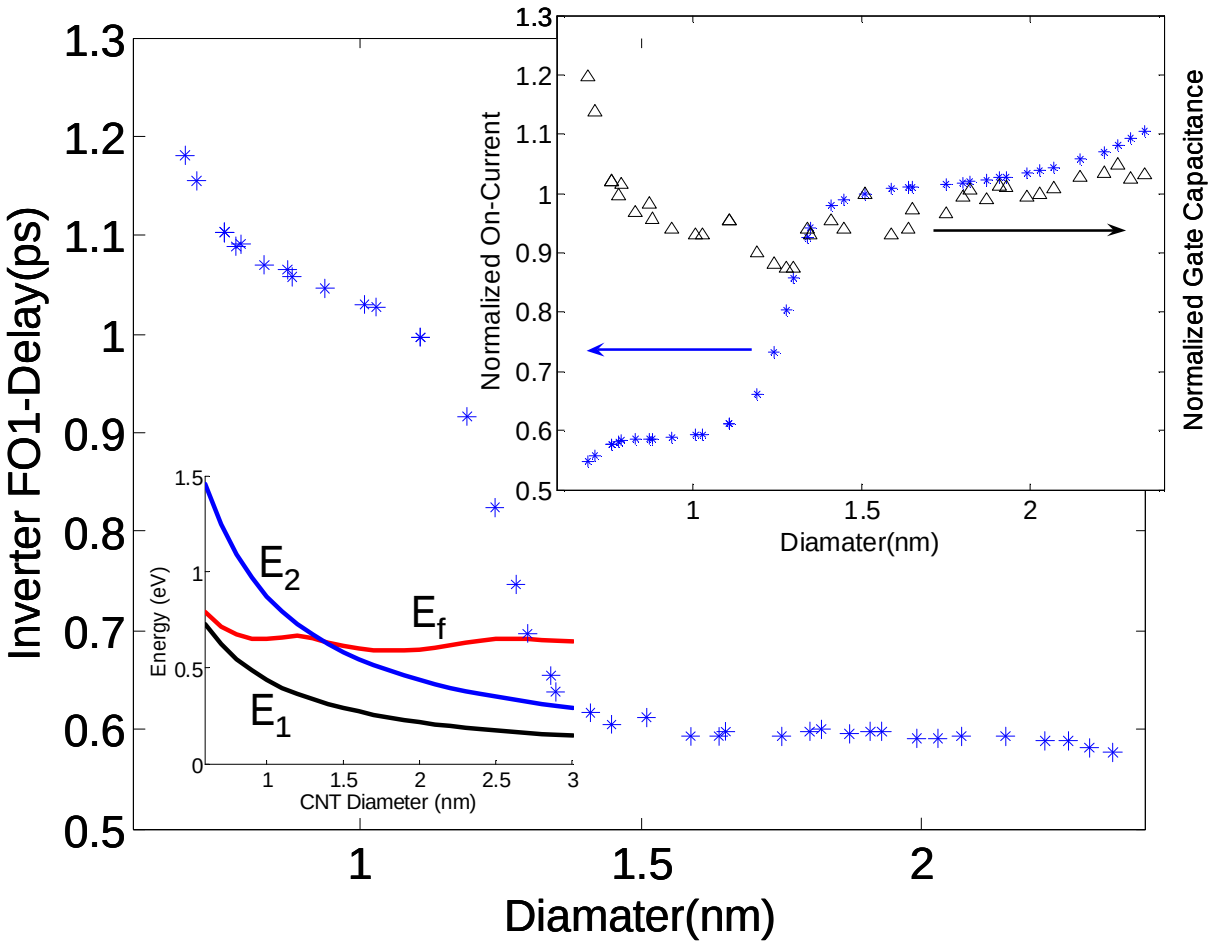
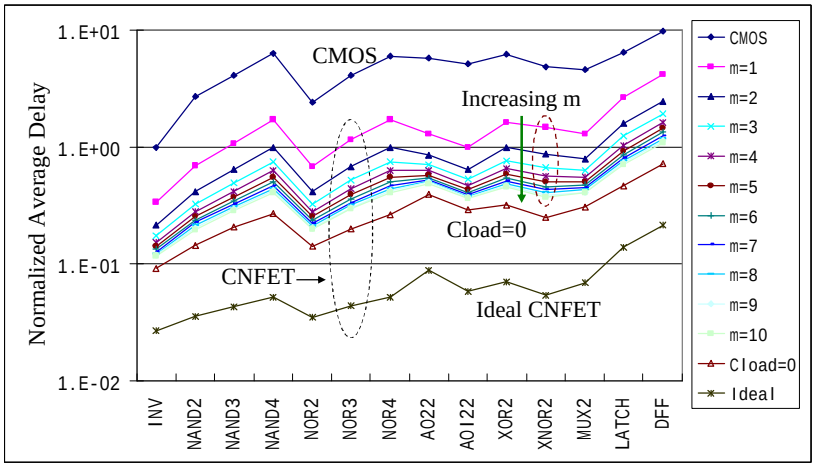
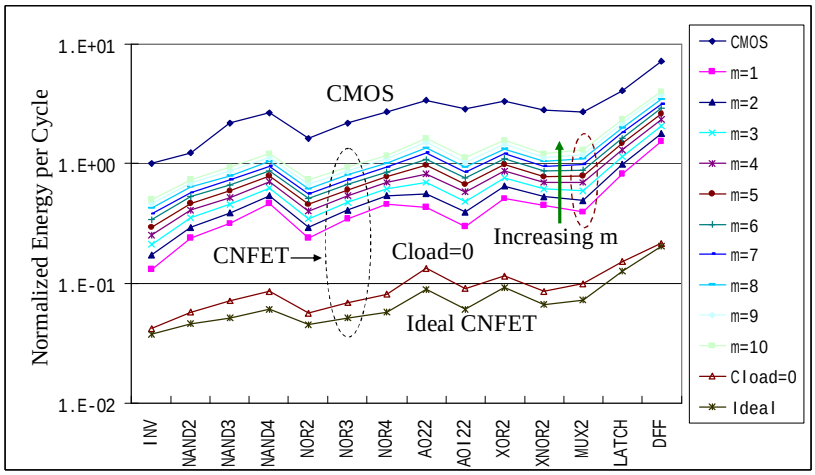

Inverter FO1-Delay(ps)
Diamater(nm)
Normalized On-Current
Normalized Gate Capacitance
Diamater(nm)
Energy (eV)
CNT Diameter (nm)
E2
Ef
E1

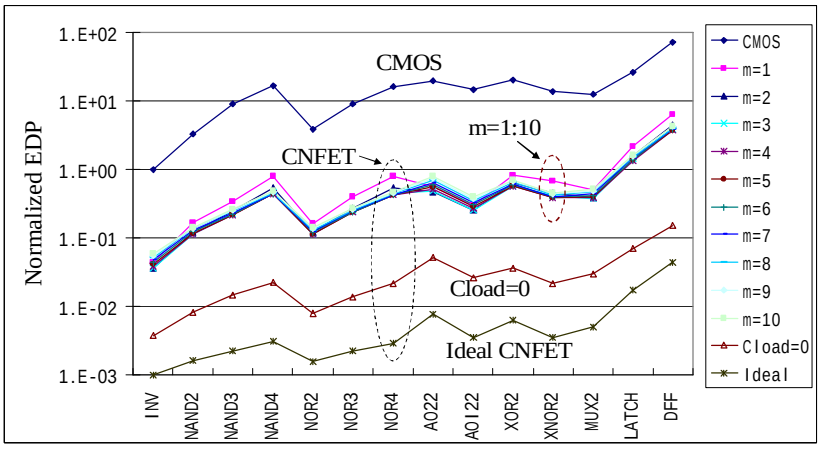
Figure 9.



(a)



(b)



(c)

Figure 10.

Tables:

TABLE1. The gate effective capacitance and on-current comparison between CNFET and MOSFET at the 32 nm node. The off-currents per gate capacitance for CNFET and MOSFET are adjusted to the same value.

$L_{Channel}$ =18nm	Gate C_{eff}	$I_{off\ (nA/fF)}$	$I_{on\ (mA/fF)}$	I_{on}/I_{off}	CNFET/MOS
nMOS	1.1 fF/μm	383	1.2	3.1×10^{3}	N/A
nCNFET	3.6 aF/FET	383	7.2	1.9×10^{4}	~ 6
pMOS	1.1 fF/μm	253	0.5	2.1×10^{3}	N/A
pCNFET	3.6 aF/FET	253	7.1	2.8×10^{4}	~ 14