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Enclosed for your consideration is a manuscript of the paper, entitled "**Modeling and Analysis of Planar Gate Capacitance for 1-D FET with Multiple Cylindrical Conducting Channels**". This paper proposes a new device scaling scenario. As such it belongs to the "Devices and Process Modeling" or the "Nanoelectronics" category.

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Sincerely yours,
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Modeling and Analysis of Planar Gate Capacitance for 1-D FET with Multiple Cylindrical Conducting Channels

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Abstract. This paper presents accurate analytical models to calculate the gate capacitance of 1-D field effect transistors (FETs) with multiple cylinder conducting channels. The gate capacitance C_{gg} is decomposed into three major components: the capacitance C_{gc} between the gate and the parallel cylinder conducting channels (the number of channels ≥ 1) in dual-layer dielectric materials, the outer-fringe capacitance C_{of} between the gate and the source/drain cylinder conductors, and the coupling capacitance C_{gtg} between the adjacent gates. A realistic planar gate structure with high-*k* gate dielectric material is considered in this paper, including the screening effect of the parallel conductors and different dielectric material on capacitance. 10% accuracy is achieved with the analytic models, compared with the values simulated by 3-D numerical field solvers. Using a simple analytical expression for the gate delay that includes the parasitic capacitance and screening of multiple parallel conducting channels, this paper also shows that both increasing the number of channels per gate and reducing the gate height are effective ways to improve device speed.

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I. Introduction

In recent years, 1-D field effect transistors (FETs) with cylinder conducting channels (e.g. semiconductor nanowire FET [1-3], carbon nanotube FET [4-8], and tri-gate transistors [9]) are proposed and reported due to the better electrostatic performance over planar devices (bulk CMOS) and SOI. Either a gate-all-around (GAA) gate structure or a planar gate structure with single conducting channel in a uniform dielectric material (Fig. 1) was usually used to evaluate the gate capacitance and device performance [10-12]. However, for the devices with high-*k* gate dielectric whose permittivity is not the same as the substrate permittivity, 10% to 40% error will be incurred by these approximations. In addition, due to the small drive current that can be delivered by a single channel, multiple conducting channels per gate are usually required for 1-D FET to achieve competitive performance over the traditional silicon devices [6, 13]. For a device with multiple conducting channels, a planar gate structure with high-*k* gate dielectric material is a realistic structure. In the limit of ballistic or near-ballistic transport, the drive current of 1-D device highly depends the gate to channel capacitance (C_{gc}). The parallel conducting channels have screening / imaging effect on the actual potential profile in the gate region, therefore affect the capacitance. Previous work treated the screening effect for calculating C_{gc} using 2-D numerical modeling [14, 15]. However there have no reported analytical models available to offer insights for device design. In addition to C_{gc}, the device speed also strongly depends on the parasitic gate capacitance, including the outer-fringe gate capacitance (C_{of}) and the gate to gate (source/drain) coupling capacitance (C_{gtg}). It is very important to model the various components of total gate capacitance (C_{gg}) with reasonable accuracy in order to evaluate and predict the 1-D FET circuit performance (on-current, speed, and power). The contributions of this paper are two fold: (1) we present an analytical model of the gate capacitance (including screening and fringing

field effects) that can be incorporated in a compact model such as SPICE [16]; (2) using this simple analytical model for the gate capacitance, one can, for the first time, obtain a realistic estimate of circuit performance including the parasitic capacitance and screening effect from multiple parallel channels.

II. Gate Capacitance Modeling

In this paper, we consider a planar gate structure with multiple cylindrical conducting channels and high-*k* gate dielectric material on a substrate with a different dielectric constant as illustrated in Figure 2. Multiple devices may be connected in series (e.g. in a NAND structure). The diameter of the cylinder is '*d*'. The normal distance between the gate and the cylinder center is denoted by '*h*', and the distance between the centers of the two adjacent parallel conductors is denoted by '*s*'. To be general, we start from a description of the methodology to calculate the capacitance including the screening effect of the neighboring conductors.

The important capacitances to be modeled are

(1) Gate to channel capacitance, C_{gc}

(2) Outer fringe capacitance, C_{of}

(3) Gate to gate, or gate to source/drain coupling capacitance, C_{gtg}

For C_{gc}, the image charge across the dielectric boundary should be taken into account. The outer fringe capacitance is a strong function of the device geometry. Both C_{gc} and C_{of} are strongly affected by screening of neighboring channels especially for closely spaced channels which provide large current drive per unit device width. This screening effect must be properly

accounted for in the model. C_{gtg} cannot be simply modeled by a parallel plate approximation because the parallel plate dimension is comparable to the other 3-D geometrical dimensions. In the following sections, we derive simple analytical equations to model these three capacitances. We verify their accuracy by comparing the results with numerical solutions from a 3-D field solver [17].

2.1 Capacitance Model for the Object in an Array

Consider the structure in Figure 3(a). We represent the parallel conducting channels as N ($N \geq 1$) identical objects in parallel, and the gate electrode as the planar electrode #0. In order to calculate the coupling capacitance C_{01} between the electrode #0 and the object #1, the total effects of the other (N-1) objects around the object #1 on C_{01} can be lumped and approximated as the two nearest objects, #2 and #3 (Fig. 3(b)), because the objects with a large distance from object #1 have rather weak influence on the electrical field distribution between electrode #0 and #1. Approximating the (N-*1*) objects with more than two objects may achieve better accuracy at the cost of a more complex equation for the general case.

Applying the same voltage V_1 between the objects #1, #2, #3 and the electrode #0, an amount of charges Q_1, $\eta_1 Q_1$, and $\eta_2 Q_1$ are induced on the three objects #1, #2, and #3, respectively, due to the different coupling capacitance C_{01}, C_{02}, and C_{03}. C_{0i} is the equivalent coupling capacitance between the electrode #0 and the object #i. We can define η_1 and η_2 as the ratio of C_{02} and C_{03}, respectively, over C_{01}, given by,

$$\eta_1 = \frac{C_{02}}{C_{01}} \qquad \eta_2 = \frac{C_{03}}{C_{01}} \tag{1}$$

The charges on objects #2 and #3 will affect the electric field and electrostatic potential profile between the electrode #0 and the object #1. For a 1-D device geometry, we ignore the charge re-distribution in the circumferential direction. Using the superposition principle, the capacitance C_{01} can be expressed as:

$$C_{01} = \frac{Q_1}{V_1} = \frac{Q_1}{V_o + V_{adj}} \qquad (2)$$

V_o and V_{adj} are the potential differences between the electrode #0 and the object #1 caused by the charges on the object #1 and the adjacent objects (#2 and #3), respectively, acting as independent electrodes. Normalized to the same amount of charge Q_1, V_{adj} is rewritten as:

$$V_{adj} = \eta_1 \cdot V_{adj,1} + \eta_2 \cdot V_{adj,2} \qquad (3)$$

$V_{adj,1}$ and $V_{adj,2}$ are the potential differences between the electrode #0 and the object #1 caused by the objects #2 and #3, respectively, with the same amount of charge Q_1. With equations (2) and (3), we obtain,

$$C_{01} = \frac{1}{\frac{V_o}{Q_1} + \eta_1 \cdot \frac{V_{adj,1}}{Q_1} + \eta_2 \cdot \frac{V_{adj,2}}{Q_1}} = \frac{1}{\frac{1}{C_{\inf}} + \eta_1 \cdot \frac{1}{C_{sr,1}} + \eta_2 \cdot \frac{1}{C_{sr,2}}} \qquad (4)$$

The capacitance C_{01} is a series combination of the capacitance $C_{\inf}$, $C_{sr,1}/\eta_1$, and $C_{sr,2}/\eta_2$. $C_{\inf}$ is the capacitance between the electrode #0 and the object #1 without the screening of all other objects. $C_{sr,1}$ and $C_{sr,2}$ are the equivalent capacitances due to the screening effects of the objects #2 and #3, respectively. η_1, η_2 are functions of the geometry, the number of the objects of the array, and the position of the object in the array. In some particular cases, equation (4) can be

simplified.

For the objects at the ends of an array, the screening objects are only at one side, therefore $\eta_2=0$. This capacitance, C_e, can be expressed as:

$$C_e = \frac{C_{sr,1} \cdot C_{\inf}}{C_{sr,1} + \eta_1 \cdot C_{\inf}} \qquad (5)$$

For the objects around the middle of an array, because the geometry is symmetric around the object ($\eta_1 \cong \eta_2$ and $C_{sr,1} \cong C_{sr,2}$), the capacitance between the electrode and the object in the middle, C_m, can be approximated as

$$C_m = \frac{C_{sr,1} \cdot C_{\inf}}{C_{sr,1} + 2\eta_2 \cdot C_{\inf}} \qquad (6)$$

With equations (5) and (6), we can eliminate $C_{sr,1}$ and express C_m as a function of C_e and $C_{\inf}$,

$$C_m = \frac{\eta_1 \cdot C_e \cdot C_{\inf}}{2\eta_2 \cdot C_{\inf} + (\eta_1 - 2\eta_2) \cdot C_e} \qquad (7)$$

If we denote $\eta_2 = \alpha \cdot \frac{C_e}{C_m}$ (the reason will be discussed next), then C_m is given by,

$$C_m = \frac{2\alpha}{\eta_1} \cdot C_e + (1 - \frac{2\alpha}{\eta_1}) \cdot C_{\inf} \qquad (8)$$

The summation of the coefficients of C_e and $C_{\inf}$ equals to 1. For a given geometry, the parameter η_1 is a function of the number of objects per array, and the parameter α is a function of both the number of objects per array and the position of the object in the array.

There are two special cases with which we can determine the parameters η_1 and/or α directly.

Case 1: For an array with only two objects, the two objects are identical and both objects are at the end. From equation (1), we know η_1=1. There is only one component of capacitance denoted by C_e, given by:

$$C_e = \frac{C_{sr,1} \cdot C_{\inf}}{C_{sr,1} + C_{\inf}} \tag{9}$$

Case 2: For an array with only three objects, there are two components of capacitances: the capacitance between #0 and the two objects at the ends (C_e) and the capacitance between #0 and the one object in the middle (C_m). When calculating C_e, we approximate the two objects #1 and #3 as one object in the position of object #1 as in Fig. 3. By the definition of η_2 and α, we know α=1. Thus C_e and C_m are given by,

$$\begin{aligned} C_e &= \frac{C_{sr} \cdot C_{\inf}}{C_{sr} + \eta_1 \cdot C_{\inf}} \\ C_m &= \frac{2}{\eta_1} \cdot C_e + (1 - \frac{2}{\eta_1}) \cdot C_{\inf} \end{aligned} \tag{10}$$

We will be able to calculate C_e and C_m once we know the expressions of η_1, $C_{\inf}$ and C_{sr}. In the following sections, we derive η_1, $C_{\inf}$ and C_{sr} for different gate regions along the channel length direction.

2.2 Gate to Channel Capacitance

In this section, we calculate the gate to channel capacitance per unit length (C_{gc}) for the planar gate structure with high-k gate dielectric material and multiple parallel conducting cylindrical

channels (Fig. 2). We ignore the end effect in the axial direction, i.e. the cylindrical channel is considered as an infinitely long wire.

$\boldsymbol{C_{gc,inf}}$: First, we calculate $C_{gc,\mathrm{inf}}$, the capacitance between the gate and a single isolated cylinder with diameter 'd'. First, consider the case where there is no metal gate on top of the cylinder. For an arbitrary charge Q at (x_0, y_0), we consider two image charges Q_1 at (x_1, y_1), Q_2 at (x_2, y_2), as a first approximation (Fig. 4(a)). The interface between the two dielectric materials is along the line y=0. Applying the following boundary conditions:

1) The tangential component of the electric field along the boundary is continuous, i.e. $E_{\|}(x, 0^{+})= E_{\|}(x, 0^{-})$

2) The normal component of the D-field across the boundary is continuous, i.e. $D\perp(x, 0^{+})= D\perp(x, 0^{-})$,

then the only solutions are given by,

$$\begin{aligned} &x_1 = x_2 = x_0 \qquad y_1 = -y_0 \qquad y_2 = y_0 \\ &Q_1 = \lambda_1 \cdot Q \qquad \lambda_1 = \frac{k_1 - k_2}{k_1 + k_2} \\ &Q_2 = \lambda_2 \cdot Q \qquad \lambda_2 = \frac{2k_2}{k_1 + k_2} \end{aligned} \tag{11}$$

λ_1 and λ_2 are the pre-factors that account for the interface due to $k_1 \neq k_2$. Thus the positions of the two image charges are symmetric across the interface y=0. k_1 and k_2 are the relative permittivity of the dielectric materials in region A and region B, respectively. To calculate the electrostatic properties in region A, only the image charge Q_1 in region B is required, we therefore ignore Q_2

in the following analysis.

Next, we consider the case of a metal gate on top of the cylinder along the interface $y=y_3$, and a uniform dielectric material ($k_1=k_2$) (Fig. 4(b)). The relationships between the geometry parameters are,

$$b = h - \sqrt{h^2 - r^2} \qquad c = r - h + \sqrt{h^2 - r^2} \tag{12}$$

where r is the radius of the cylinder.

Combining the above two geometries, there will be an infinite number of image charges in the whole space, as shown in Figure 4(c) due to the gate mirroring effect and the refection across the two interfaces $y=0$ and $y=y_3$. To simplify the analysis, we assume the charge distribution profile around the cylinder is not changed by the interface between the two dielectric materials. Mathematically, there are 4 image line charges in each group,

$$Q_{imag\_m,i} = (-1)^{i+1} \cdot \lambda_1^{\,m} \cdot Q \qquad i = 1,2,3,4 \qquad m = 1,2,3,... \tag{13}$$

The potential drop between the cylinder and the metal gate caused by the m^{th} image line charges group is given by,

$$V_{imag\_m} = \sum_{i=1}^{4} V_{imag\_m,i} = \frac{(-1)^{m+1}}{2\pi k_1 \varepsilon_o} \cdot \lambda_1^{\,m} \cdot Q \cdot \ln\left(\frac{(2mh+md)^2}{(2mh+md)^2 - (2h-2b)^2} \right) \tag{14}$$

The gate to channel capacitance can be expressed as,

$$C_{gc\_\inf} = \frac{Q}{V} = \frac{Q}{V_o + \sum_{m=1}^{\infty} V_{imag\_m}} = \frac{1}{\frac{1}{C_{gco}} + \frac{1}{C_{gc\_imag}}} \qquad (15)$$

Where C_{gco} is the capacitance when k_1=k_2, and C_{gc_imag} is the equivalent series capacitance caused by the image charges when $k_1 \neq k_2$, given by,

$$C_{gco} = \frac{2\pi k_1 \varepsilon_o}{\cosh^{-1}(\frac{2h}{d})} \qquad (16)$$

$$C_{gc\_imag} = \frac{Q}{\sum_{m=1}^{\infty} V_{imag\_m}} = \frac{2\pi k_1 \varepsilon_o}{\sum_{m=1}^{\infty} (-1)^{m+1} \cdot \lambda_1{}^m \cdot \ln\left(\frac{(2mh+md)^2}{(2mh+md)^2 - (2h-2b)^2}\right)} \qquad (17)$$

For a typical CNFET device (1.5 nm in diameter (d=1.5nm) conducting channel, 4 nm thick (h=4nm) HfO_2 gate dielectric material (k_1=16) with SiO_2 substrate (k_2=3.9)), C_{gco} is about 377 pF/μm and C_{gc_imag} is about 1380 pF/μm. Therefore C_{gc_inf} is 296 pF/μm using equation (15) which is within 2% of the numerical simulation result (~302 pF/μm), while the simple model C_{gco} (Equ. 16) used in the literature [11, 12] overestimates the capacitance by 26%.

To simply the above equation, we approximate the effects of all the image line charges as one image line charge $\lambda_1 Q$ at (0, -r), the image capacitance is simplified as,

$$C_{gc\_imag} = \frac{2\pi k_1 \varepsilon_o}{\lambda_1 \cdot \ln\left(\frac{2h+2d}{3d}\right)} \qquad (18)$$

The discrepancy between the capacitance $C_{gc\_\inf}$ calculated by both analytical models (Equ.

(15-18)) and the numerical simulation is within 2% (Fig. 5). The results indicate that lumping the effects of all the image charges due to $k_1 \neq k_2$ as one image line charge $\lambda_1 Q$ at (0,-r) is a good approximation.

***C_{gc_e}* and *C_{gc_m}*:** Next, we consider the effects of the adjacent parallel cylinders on C_{gc} for a more general gate structure and derive the expressions for C_{gc_e} and C_{gc_m}. Consider a gate with two conducting channels, cylinder A and cylinder B, in parallel (Fig. 6). Only two image line charges with each real line charge Q is considered: the image line charge $-Q$ due to metal gate mirroring, and the image line charge $\lambda_1 Q$ due to $k_1 \neq k_2$ (Fig. 6). Due to the screening effect, in addition to the potential difference caused by the isolated cylinder A itself, there are additional potential drops between cylinder A and the gate caused the real and image line charges by cylinder B. The additional potential difference caused by the line charge Q_B and the image line charge -Q_B is given by,

$$V_{adj,1} = \frac{Q_B}{2\pi k_1 \varepsilon_o} \ln\left(\frac{\overline{O_{Bi}^{'} O_A^{''}}}{\overline{O_B^{'} O_A^{''}}}\right) = \frac{Q_B}{4\pi k_1 \varepsilon_o} \ln\left(\frac{s^2 + 2(h-r)\cdot[h+\sqrt{h^2-r^2}]}{s^2 + 2(h-r)\cdot[h-\sqrt{h^2-r^2}]}\right) \qquad (19)$$

The additional potential difference caused by the image line charge $\lambda_1 Q_B$ is,

$$V_{adj,2} = f(h,r,s)\frac{\lambda_1 Q_B}{2\pi k_1 \varepsilon_o} \ln\left(\frac{\overline{O_{Bii} O_o}}{\overline{O_{Bii} O_A^{''}}}\right) = f(h,r,s)\frac{\lambda_1 Q_B}{4\pi k_1 \varepsilon_o} \ln\left(\frac{(h+d)^2 + s^2}{9r^2 + s^2}\right) \qquad (20)$$

The function f (h, r, s) models the charge redistribution effects when the two cylinders are close enough. Due to the Coulomb interaction between adjacent charges, the displacement of the equivalent charge position from the center of the cylinder is of the form tanh(μ_o) where μ_o is a function of the geometry. Based on this observation, we empirically represent f (h, r, s) as a tanh()

function of the ratio of the vertical distance over the horizontal distance between these conductors,

$$f(h,r,s) = \tanh\left(\frac{h+r}{s-d}\right) \qquad (21)$$

When the same potential is applied to the two parallel cylinders, the charge distribution profiles in the regions around cylinder A and cylinder B should be identical. The equivalent series capacitance due to the adjacent channel screening is then given by,

$$C_{gc\_sr} = \frac{Q_B}{V_{adj,1} + V_{adj,2}} \qquad (22)$$

Since the electric field is well confined within the gate dielectric for the typical gate structure, we assume the cylinders which are more than '*s*' distance apart away have a minor effect on each other, i.e. the gate to channel capacitance does not depend on the number of the cylinders in the array. Applying η_1=1 (recall Equ. 10), with equations (10, 11, 15-22), the capacitances per unit length in the channel region are,

$$C_{gc\_e} = \frac{C_{gc\_\inf} \cdot C_{gc\_sr}}{C_{gc\_\inf} + C_{gc\_sr}} \qquad C_{gc\_m} = 2C_{gc\_e} - C_{gc\_\inf}$$

$$C_{gc\_sr} = \frac{4\pi k_1 \varepsilon_o}{\ln\left(\frac{s^2 + 2(h-r)\cdot[h+\sqrt{h^2-r^2}]}{s^2 + 2(h-r)\cdot[h-\sqrt{h^2-r^2}]}\right) + \lambda_1 \cdot \ln\left(\frac{(h+d)^2+s^2}{9r^2+s^2}\right)\cdot\tanh\left(\frac{h+r}{s-d}\right)} \qquad (23)$$

$$C_{gc\_\inf} = \frac{2\pi k_1 \varepsilon_o}{\cosh^{-1}(\frac{2h}{d}) + \lambda_1 \cdot \ln\left(\frac{2h+2d}{3d}\right)} \qquad \lambda_1 = \frac{k_1 - k_2}{k_1 + k_2}$$

C_{gc_e} is the unit capacitance of the gate to the cylinders at the two ends, and C_{gc_m} is the unit

capacitance of the gate to the cylinders in the middle. The difference between the values calculated by the analytic model and the numeric 3-D field solver simulation is within 10% with various parameter settings and different number of channels per gate (Fig. 7). The discrepancy comes from two sources: 1) we approximate all the image charges due to $k_1 \neq k_2$ with a single image line charge, 2) the gate capacitance is only classified into two groups, C_{gc_e} and C_{gc_m}, which are assumed to be independent of the number of channels per gate. More accurate results can be obtained by carefully choosing the parameters η_1 and α for each channel under the gate.

2.3 Gate Outer-Fringe Capacitance

To evaluate the device speed accurately, it is necessary to include the parasitic gate capacitance, e.g. the outer-fringe capacitance (C_{of}), and the gate to gate (or gate to source/drain) coupling capacitance (C_{gtg})[+] (Fig.2). Since the channel region is screened by the conducting cylinders, the inner fringe capacitance is ignored and uniform dielectric material with relative permittivity k_2 is assumed (Fig. 8). 3-D numerical simulation results show that C_{of} is a weak function of the gate height (Fig. 9): for the device with 32 nm long gate length (L_g), reducing the gate height (H_{gate}) from 64 nm to 10 nm results in less than 10% difference in C_{of} with 400 nm source/drain length (L_{sd}). Within a wide parameter range (the ratio of L_{sd} over L_g is less than 13 and the ratio of H_{gate} over L_g is larger than 0.3), it is reasonable to assume the outer-fringe capacitance (C_{of}) is independent of H_{gate} in order to simplify the analysis.

First we calculate C_{of_inf}, the capacitance between the gate and the isolated S/D cylinder. It is convenient to calculate the capacitance if the cylinder is parallel with the sidewall of the gate, as

[+] To simplify the notation, we use C_{gtg} even for the case of gate to source/drain capacitance. The two cases are identical from the electrostatics point of view.

shown by the inset in Figure 8. For a 2-D structure, it is possible to convert from an elliptical system to an equivalent parallel system using conformal mapping, while it is hard for a 3-D structure. We define an equivalent distance between the S/D cylinder and the sidewall of the gate as H_{eff}, in the form of,

$$H_{eff} = \sqrt{h^2 + (\gamma \cdot L_{sd})^2} \qquad (24)$$

The parameter γ is a fitting parameter which is function of the geometry. γ is set to 0.28 empirically. Thus $C_{of\_\inf}$ is given by,

$$C_{of\_\inf} = \alpha_{of\_sr} \cdot \frac{2\pi k_2 \varepsilon_o L_{sd}}{\cosh^{-1}(\frac{2H_{eff}}{d})} = \alpha_{of\_sr} \cdot \frac{2\pi k_2 \varepsilon_o L_{sd}}{\cosh^{-1}(\frac{2\sqrt{h^2 + (0.28L_{sd})^2}}{d})} \qquad (25)$$

where α_{of_sr} is the factor due to the screening of the adjacent gate/source/drain. α_{of_sr} = 1 if the height of the adjacent gate/source/drain H_{adj} = 0, and α_{of_sr} = 0.5 if $H_{adj} = H_{gate}$ which is the usual case (Fig. 8). Equation (25) models the isolated outer-fringe capacitance accurately for both cases (Fig. 9). We choose α_{of_sr} = 0.5 in the following assuming multiple devices are in series (as in a NAND stack).

With more than one channel per gate, there will be additional potential drop between the two electrodes of the capacitor C_{of} caused by the adjacent cylinders (Fig. 10). The equivalent series capacitance due to adjacent cylinder screening is,

$$C_{of\_sr} = \alpha_{of\_sr} \cdot \frac{2\pi k_2 \varepsilon_o L_{sd}}{\ln\left(\frac{\overline{O_B' Q_A}}{\overline{O_B O_A}}\right)} = \frac{\pi k_2 \varepsilon_o L_{sd}}{\ln\left(\frac{\sqrt{(2H_{eff})^2 + s^2}}{s}\right)} \qquad (26)$$

The simulation results show that it is reasonable to group the fringe capacitances into two components: (a) the capacitance between gate and S/D at the ends (C_{of_e}) and (b) the capacitance between gate and S/D in between (C_{of_m}). Recall equations (5, 8), we have to determine the parameters η_1 and α to calculate C_{of_e} and C_{of_m}. The outer-channel region is a more open structure than the inner channel region, thus we cannot use the simplified equation (10) for $N > 2$, where N is the number of cylinders per gate, as in the channel region. Both η_1 and α are functions of N. η_1=1 for N=2, and α=1 for N=3 as described before. For $N > 2$, because the additional potential drop imposed by line charges decreases logarithmically with the distance, we empirically represent η_1 and α as,

$$\eta_1 = \exp\left(\frac{\sqrt{N^2-2N}+N-2}{\tau_1 N}\right), \quad N \geq 2$$
$$\alpha = \exp\left(\frac{N-3}{\tau_2 N}\right), \quad N \geq 3 \qquad (27)$$

τ_1 and τ_2 are fitting parameters which describes how fast the electric flux of the adjacent cylinders decreases with increasing distance. With equations (5, 8, 25, 26), we get the fringe capacitances,

$$C_{of\_e} = \frac{\pi k_2 \varepsilon_o L_{sd}}{\ln\left(\frac{\sqrt{(2h)^2+(0.56L_{sd})^2+s^2}}{s}\right)+\eta_1 \cdot \cosh^{-1}\left(\frac{\sqrt{(2h)^2+(0.56L_{sd})^2}}{d}\right)}$$
$$C_{of\_m} = \frac{2\alpha}{\eta_1}\cdot C_{of\_e} + \left(1-\frac{2\alpha}{\eta_1}\right)\cdot \frac{\pi k_2 \varepsilon_o L_{sd}}{\cosh^{-1}\left(\frac{\sqrt{(2h)^2+(0.56L_{sd})^2}}{d}\right)} \qquad (28)$$

where η_1 and α are given by equation (27), and τ_1 and τ_2 are empirically set as 2.5 and 2,

respectively, to make C_{of_m} as the average value of the fringe capacitances for the cylinders in the middle of the array. The analytical models match the 3-D simulation values very well with various number of cylinders per gate and various parameter settings (Fig. 11, Fig. 12).

2.4 Gate to Gate Capacitance

The gate to gate capacitance (C_{gtg}) is another major component of the gate capacitance. We separate C_{gtg} into two components (Fig. 13): the gate to gate fringe capacitance per unit length (C_{gtg_fr}) and the gate to gate plate capacitance per unit length (C_{gtg_nr}). C_{gtg_nr} is due to the normal electrical filed between the two parallel plates,

$$C_{gtg\_nr} = \frac{k_2 \varepsilon_o H_{gate}}{L_{sd}} \qquad (29)$$

Where L_{sd} is the distance between the two parallel plates, and H_{gate} is the gate height.

The fringe field caused by the top plates (A_1A_2, B_1B_2), bottom plates (A_3A_4, B_3B_4), and back plates (A_2A_3, B_2B_3) contribute to the fringe capacitance C_{gtg_fr}. We approximate C_{gtg_fr} as the capacitance between two parallel cylinders with equivalent radius R_{eff} (Fig. 13),

$$R_{eff} = \frac{2L_g + \tau_{bk} H_{gate}}{2\pi} \qquad (30)$$

where τ_{bk} is the factor which accounts for the effects of the back plates (A_2A_3, B_2B_3) on C_{gtg_fr}. Because the potential caused by fringe flux decreases logarithmically with the distance, $\tau_{bk} \to 0$ when $L_{sd} \to 0$, and $\tau_{bk} \to 1$ when $L_{sd} \to \infty$. We empirically approximate τ_{bk} as,

$$\tau_{bk} = \exp\left(2 - 2\sqrt{1 + \frac{2(H_{gate} + L_g)}{L_{sd}}}\right) \qquad (31)$$

Thus C_{gtg_fr} is given by,

$$C_{gtg\_fr} = \alpha_{gtg\_sr} \cdot \frac{\pi k_2 \varepsilon_o}{\ln\left(\frac{L_{sd} + L_g}{R_{eff}}\right)} \qquad (32)$$

The parameter α_{gtg_sr} is the factor due to the screening of the adjacent gate/source/drain and interconnects. $\alpha_{gtg\_sr} = 1$ if the height of the adjacent gate/source/drain $H_{adj} = 0$. α_{gtg_sr} is fitted to be 0.7 for the case $H_{adj} = H_{gate}$ (Fig. 13). The total gate to gate capacitance per unit length is the summation of C_{gtg_fr} and C_{gtg_nr}. With equations (29, 30, 32), we get,

$$C_{gtg} = \frac{k_2 \varepsilon_o H_{gate}}{L_{sd}} + \alpha_{gtg\_sr} \cdot \frac{\pi k_2 \varepsilon_o}{\ln\left(\frac{2\pi(L_{sd} + L_g)}{2L_g + \tau_{bk} H_{gate}}\right)} \qquad (33)$$

τ_{bk} is given by equation (31). The above model accurately calculates the gate to gate capacitance with negligible mismatch with the numerical simulation results (Fig. 14). We use $\alpha_{gtg\_sr} = 0.7$ in the following analysis.

III. Gate Capacitance Analysis – Impact on Device Speed

In this section, we apply the above models to analyze the effects of gate capacitance (C_{gg}) on device performance. Ignoring the quantum capacitance of the conducting cylinders, the total gate capacitance is expressed as,

$$\begin{aligned} C_{gg} &= C_{gc} \cdot L_g + f_{miller} \cdot 2(C_{of} + C_{gtg} W_{pitch}) \\ C_{gc} &= \min(N,2) \cdot C_{gc\_e} + \max(N-2,0) \cdot C_{gc\_m} \\ C_{of} &= \min(N,2) \cdot C_{of\_e} + \max(N-2,0) \cdot C_{of\_m} \end{aligned} \qquad (34)$$

The parameter f_{miller} is the Miller factor, set to be 1.5 for the switching device in inverter. N is the number of channels per gate, L_g is the physical gate length, and W_{pitch} is the device pitch in the width direction (Fig. 14). We evaluate the gate capacitance and device performance for a 32 nm node technology assuming metal-1 pitch=L_g=32 nm, k_1=16, k_2=3.9, channel diameter d=1.5 nm (e.g. (19,0) carbon nanotube) or d=5 nm (e.g. silicon/germanium nanowire), and the gate oxide thickness (h-r) is 3 nm. For a minimum size device, the width of the channel region (W) is assumed to be the same as L_g, and the device pitch in the width direction (W_{pitch}) is about 3W.

Figure 15 shows C_{gg} and its components as a function of the source/drain length (L_{sd}), and the number of channels per gate (Fig. 15). We define the total gate to channel capacitance as C_{gc_tot}=C_{gc}·L_g, the total outer fringe capacitance as C_{of_tot}=2f_{miller}·C_{of}, the total gate to gate (source/drain) capacitance as C_{gtg_tot}=2f_{miller}·C_{gtg}·W_{pitch}, and the total parasitic gate capacitance as C_{par}=C_{of_tot}+C_{gtg_tot}. Unlike 3-D or 2-D devices, underlapped gate structure is not likely to improve the device speed for 1-D device because the fringe capacitance C_{of_tot} is not a major component of C_{gg}. For the device with a single channel per gate, C_{gtg_tot} is the largest component, far more than 50% of C_{gg}. There are three ways to improve the percentage of C_{gc_tot} out of C_{gg} (Fig. 15): 1) Increase the source/drain length. While C_{of_tot} increases with L_{sd}, C_{gtg_tot} decreases more quickly with increasing L_{sd}. This results in a smaller C_{gg}, at the cost of larger source/drain extension resistance (R_{ext}) and lower device density. 2) Increase the number of channels per gate. In this case, C_{gtg_tot} remains almost the same. Because the parallel channels are screened by adjacent cylinders, C_{of_tot} increases slower than C_{gc_tot} as a function of N due to the more open

geometry (due to less gate shielding) of the region outside the gate than the inner channel region. With about 4 to 5 channels per gate, C_{gc_tot} is comparable to the parasitic capacitance (C_{par} =C_{of_tot}+C_{gtg_tot}). 3) Reduce the gate height. Both C_{gc_tot} and C_{of_tot} are almost independent of H_{gate} while C_{gtg_tot} decreases with H_{gate}. Reducing H_{gate} from 64 nm (H_{gate}=2L_g) to 32 nm (H_{gate}=L_g) results in 20% to 30% smaller C_{gtg} with varying source/drain length (Fig. 15).

To evaluate the device speed, we assume the drive current is proportional to gate to channel capacitance per unit channel length (C_{gc}), i.e. $I_{on} \propto C_{gc}$, for a given L_{sd}[+]. The local interconnect series resistance between devices (R_s) is usually much smaller than the device intrinsic resistance (R_{on}) (including channel resistance R_{ch}, source/drain extension resistance R_{ext}, and source/drain contact resistance R_c), thus the device delay is proportional to C_{gg},

$$\tau_{delay} \propto \frac{C_{gc} \cdot L_g + 3(C_{of} + C_{gtg} W_{pitch})}{C_{gc}} \qquad (35)$$

For a device with a single channel, doubling the number of channels improves device speed by 35%, and halving the gate height makes the device 20% faster (Fig. 16). Both increasing the number of channels per gate and reducing the gate height are effective ways in improving the device delay, while reducing the gate height is also efficient in reducing the dynamic power consumption due to the smaller parasitic capacitance.

IV. Conclusions

This paper presents accurate analytical models to calculate the gate capacitance of the device with high-*k* gate dielectric material and multiple cylindrical conducting channels including the

[+] This assumption is valid in the ballistic transport region [12]

screening effect. The accuracy of the analytic models is within 10% of the values simulated by 3-D numerical field solvers. For non-cylindrical conducting channels, 15% accuracy can be achieved for the devices with square cross-section channels by substituting the channel diameter in equations with the square width. For rectangular cross-section channels with an arbitrary aspect ratio, the capacitance equations can be derived analogously using the procedures described in this paper. These models are suitable for incorporation into compact models for circuit simulations such as SPICE [13].

Using these simple analytical models, one can gain insights into device performance as a function of various device design parameters. Using these simple analytical formulae for the gate capacitance, one can obtain a realistic estimate of circuit performance (Equ. 35) including the parasitic capacitance. We show that the gate to gate capacitance (C_{gtg}) is the largest component of the total gate capacitance (C_{gg}) for typical 1-D device. Unlike 3-D or 2-D devices, underlapped gate structure is not likely to improve the device speed for 1-D device because the fringe capacitance (C_{of}) is not a major component of C_{gg}. Both increasing the number of channels per gate and reducing the gate height are effective in improving the device speed. The analysis made in this paper ignored quantum capacitance related with nanoscale device and used a simplified model to estimate I_{on}. A more accurate estimate of the dependence of device performance on device parameters (e.g. N, L_{sd}, L_g, T_{ox}) can be made by incorporating the capacitance models developed here with realistic device current models and quantum capacitance model [18]. This is outside the scope of this present paper. On the other hand, the analytical capacitance model presented in this paper is broadly applicable to all 1-D devices such as carbon nanotube transistors [4-8], 1-D semiconductor nanowire transistor [1-3], and scaled down tri-gate FET [9] or FINFET with a small aspect ratio. Our analysis of device speed shows the importance of

accurately modeling the parasitic capacitance for performance evaluation of these 1-D FETs.

Acknowledgements

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Figure Captions:

Figure 1. (a) Gate-All-Around (GAA) structure, and (b) Planar gate structure with single channel in a uniform gate dielectric material.

Figure 2. (a) The 3-D structure of the devices with multiple channels and high-k gate dielectric material, and the related parasitic gate capacitances. (b) The 2-D view of the cross section in the channel region and the related gate to channel capacitance.

Figure 3. (a) There are N identical objects in parallel in an array. (b) In order to calculate the coupling capacitance C_{01}, the effects of the (N-1) objects around the object #1 can be lumped into the two nearest objects #2 and #3. C_{02} and C_{03} are the equivalent capacitances assuming all the other (N-1) objects are lumped at the position of #2 and #3.

Figure 4. (a) One real charge Q in dielectric material k_1, and the related image charges Q_1 and Q_2 due to $k_1 \neq k_2$. (b) The charge profile of one conducting cylinder under an infinite large metal gate in a uniform dielectric material k_1. (c) Combining the case (a) and (b), in order to calculate the potential profile in the shaded region. There is an infinite number of image charges (dashed circles) due to metal gate screening and the interface between k_1 and k_2.

Figure 5. The comparison between the analytic models and the numerical simulations to calculate the gate to channel capacitance $C_{gc\_\inf}$ with isolated cylinder channel. The simple model in Figure 1(b) overestimates $C_{gc\_\inf}$ by about 10% to 35%. Our model using either one approximated image charge or the first two group (8) image charges due to $k_1 \neq k_2$ achieves 2% or better accuracy.

Figure 6. Two parallel cylinders A and B are under the same metal gate. The images charges are

denoted by the dashed circles. The effects of the infinite number of image charges in Figure 5(c) due to the gate screening and the interface between k_1 and k_2 are approximated as one image charge $\lambda_1 Q_A$ ($\lambda_1 Q_B$). The charge distribution profile for Q_A(Q_B) and -Q_A(-Q_B) are assumed not to be affected by the image line charge $\lambda_1 Q_A$ ($\lambda_1 Q_B$).

Figure 7. The comparison between the analytic model (solid lines) and the numerical simulation results (symbols) as a function of the distance between the adjacent channels (s). The gate to channel capacitance (C_{gc}) with different number of channels (N=2, 3, 7) per gate are plotted in the plot. C_{gc} converges into two groups: the capacitance between the gate and the two channels at the ends (C_{gc_e}) and the capacitance between the gate and the channels between the ends (C_{gc_m}). 10% accuracy is obtained with various parameter settings.

Figure 8. The structure to calculate the gate outer-fringe capacitance. The inset shows a parallel system with equivalent distance H_{eff} between the cylinder and the plate electrode in order to calculate the outer-fringe capacitance C_{of}.

Figure 9. The comparison between the analytic model and 3-D simulation to calculate the fringe capacitance C_{of} for the device with single isolated channel, with different gate height. The gate length (L_g) is 32 nm, d = 1.5 nm, h = 4 nm, and k_2 = 3.9.

Figure 10. The equivalent parallel system in order to calculate the fringe capacitance C_{of} with two parallel cylinders in the source/drain region. The actual potential difference between the cylinder A and the metal gate is affected by the adjacent line charge Q_B and its image line charge -Q_B.

Figure 11. The comparison between the analytic model and 3-D simulation to calculate the fringe capacitance C_{of_e} and C_{of_m} for the device with (a) 2 parallel cylinders per gate, and (b) 3 parallel

cylinders per gate, with different distance between the adjacent cylinders. L_g = 32 nm, H_{gate} = 64 nm, d = 1.5 nm, h = 4 nm, and k_2 = 3.9.

Figure 12. The comparison between the analytic model and 3-D simulation to calculate the fringe capacitance C_{of_e} and C_{of_m} for the device with different number of cylinders per gate. L_g = 32 nm, d = 1.5 nm, h = 4 nm, k_2 = 3.9, and the distance between the adjacent cylinders (s) is 8 nm.

Figure 13. The gate to gate (source/drain) coupling capacitance (C_{gtg}) can be decomposed into two components: the parallel plate capacitance (C_{gtg_nr}) due to the normal electric field between the gates, and the fringe capacitance between two cylinders (C_{gtg_fr}) with equivalent radius R_{eff} due to the fringing electric field between the gates.

Figure 14. The comparison between the analytic model and simulation to calculate gate to gate capacitance (C_{gtg}) with different gate height. The inset shows the gate structure for simulation. L_g = 32 nm, d = 1.5 nm, h = 4 nm, and k_2 = 3.9.

Figure 15. The gate capacitance C_{gg} and its components as function of (a) the source/drain length, and (b) the number of channels per gate. The results with two gate heights (32 nm & 64 nm) are plotted. The width of gate region with high-k dielectric is 32 nm, the device pitch in the width direction (W_{pitch}) is 96 nm, L_g = 32 nm, d = 1.5 nm, k_2 = 3.9, and the gate oxide thickness (h-r) is 3 nm.

Figure 16. The device delay as a function of the number of channels per gate, with different gate height. The width of gate region with high-k dielectric is 32 nm, the device pitch in the width direction (W_{pitch}) is 96 nm, L_g=32nm, k_1=16, k_2=3.9. The channel diameter d = 1.5 nm for the left plot, and d = 5 nm for the right plot. The gate oxide thickness (h-r) is 3 nm for both plots.

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Figures:

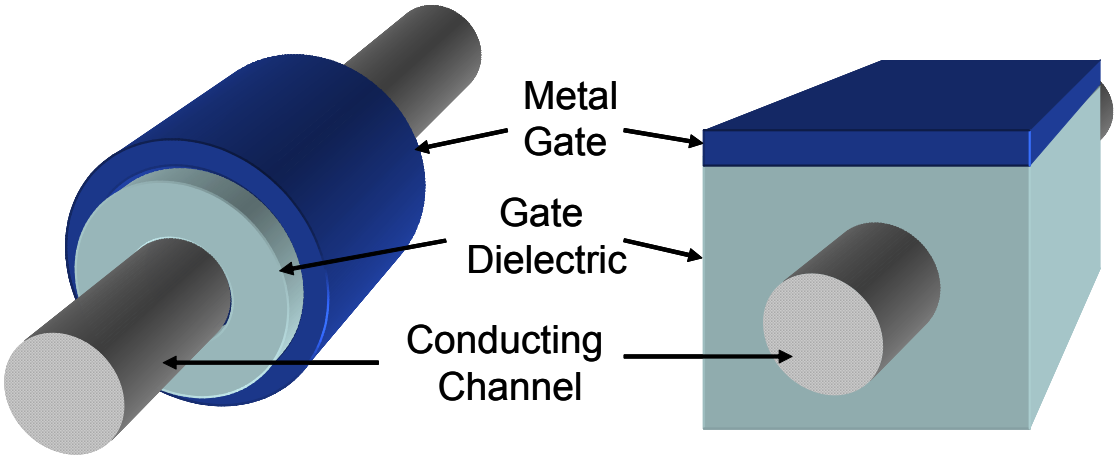
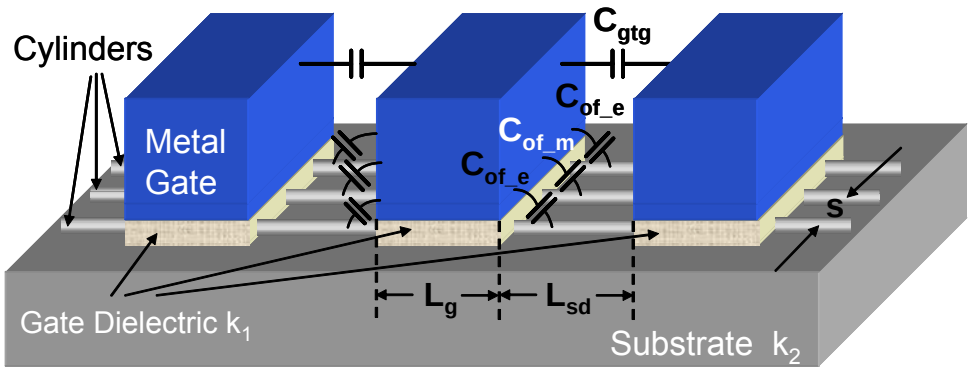
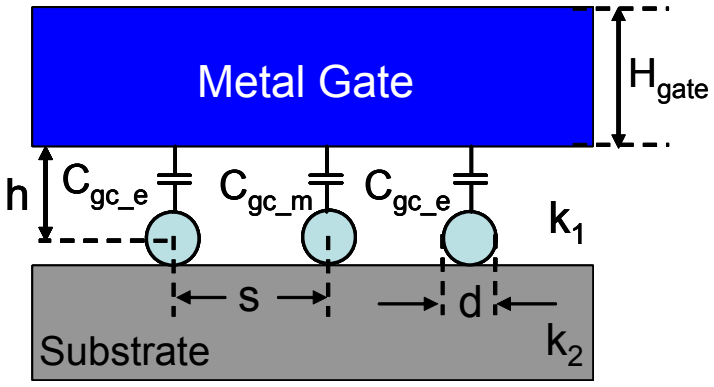


Figure 1


Cylinders
Metal Gate
C_{gtg}
C_{of_e}
C_{of_m}
C_{of_e}
s
L_g
L_{sd}
Gate Dielectric k_1
Substrate k_2

(a)


Metal Gate
H_{gate}
h
C_{gc_e}
C_{gc_m}
C_{gc_e}
k_1
s
d
Substrate
k_2

(b)

Figure 2

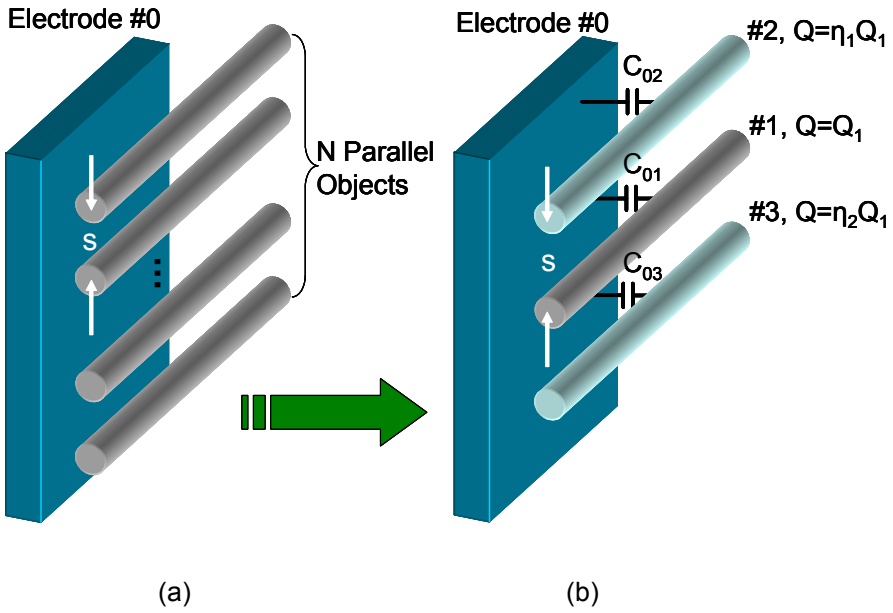

Electrode #0
N Parallel Objects
S
Electrode #0
C_{02}
C_{01}
C_{03}
#2, $Q=\eta_1 Q_1$
#1, $Q=Q_1$
#3, $Q=\eta_2 Q_1$
S
(a)
(b)

Figure 3

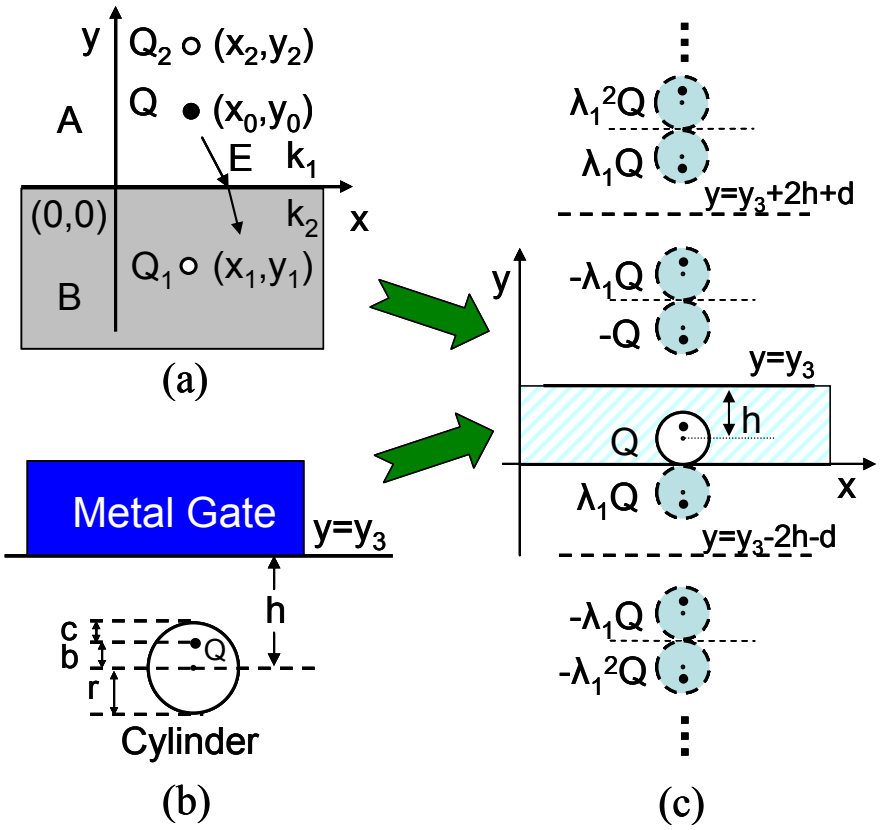

y
Q2 o (x2,y2)
A
Q (x0,y0)
E k1
(0,0)
k2
x
Q1 o (x1,y1)
B
(a)
Metal Gate
y=y3
h
c
b
r
Q
Cylinder
(b)
λ1²Q
λ1Q
y=y3+2h+d
y
-λ1Q
-Q
y=y3
h
Q
x
λ1Q
y=y3-2h-d
-λ1Q
-λ1²Q
(c)

Figure 4

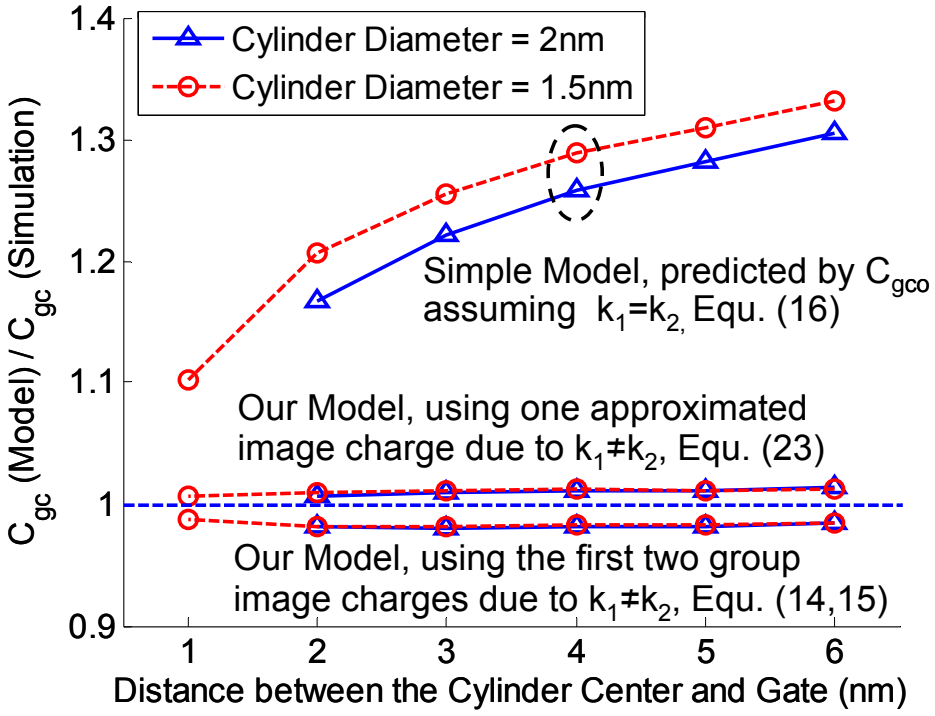

Cylinder Diameter = 2nm
Cylinder Diameter = 1.5nm
Simple Model, predicted by C_{gco} assuming $k_1=k_2$, Equ. (16)
Our Model, using one approximated image charge due to $k_1 \neq k_2$, Equ. (23)
Our Model, using the first two group image charges due to $k_1 \neq k_2$, Equ. (14,15)
C_{gc} (Model) / C_{gc} (Simulation)
Distance between the Cylinder Center and Gate (nm)
1.4
1.3
1.2
1.1
1
0.9
1
2
3
4
5
6

Figure 5

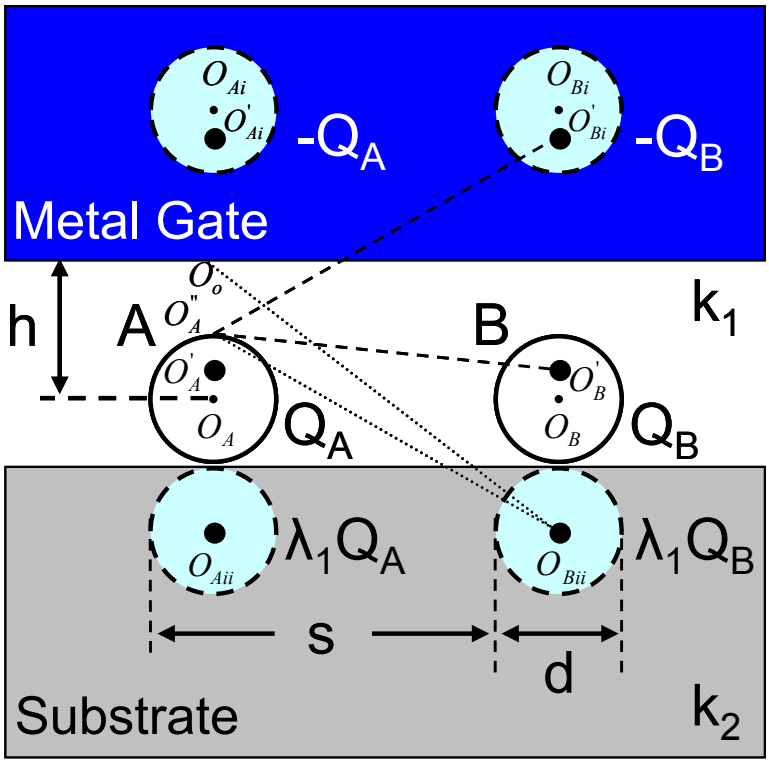


Figure 6

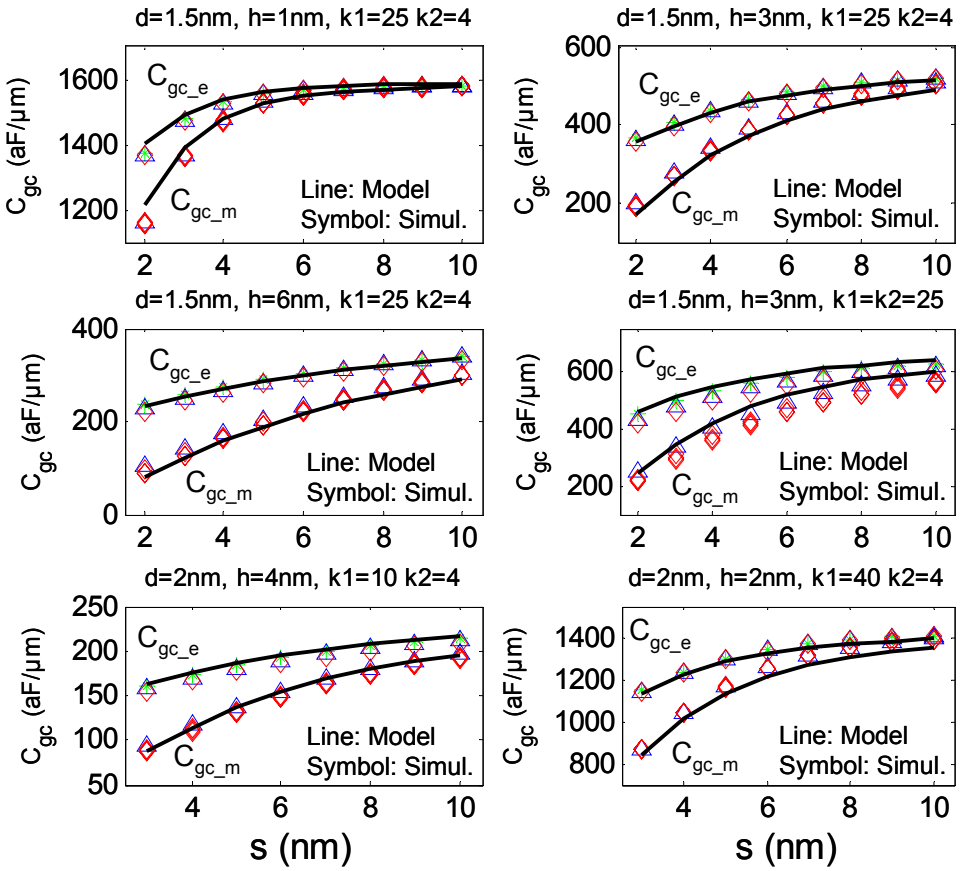

d=1.5nm, h=1nm, k1=25 k2=4
d=1.5nm, h=3nm, k1=25 k2=4
d=1.5nm, h=6nm, k1=25 k2=4
d=1.5nm, h=3nm, k1=k2=25
d=2nm, h=4nm, k1=10 k2=4
d=2nm, h=2nm, k1=40 k2=4
C_gc_e
C_gc_m
Line: Model
Symbol: Simul.
C_gc (aF/μm)
s (nm)

Figure 7

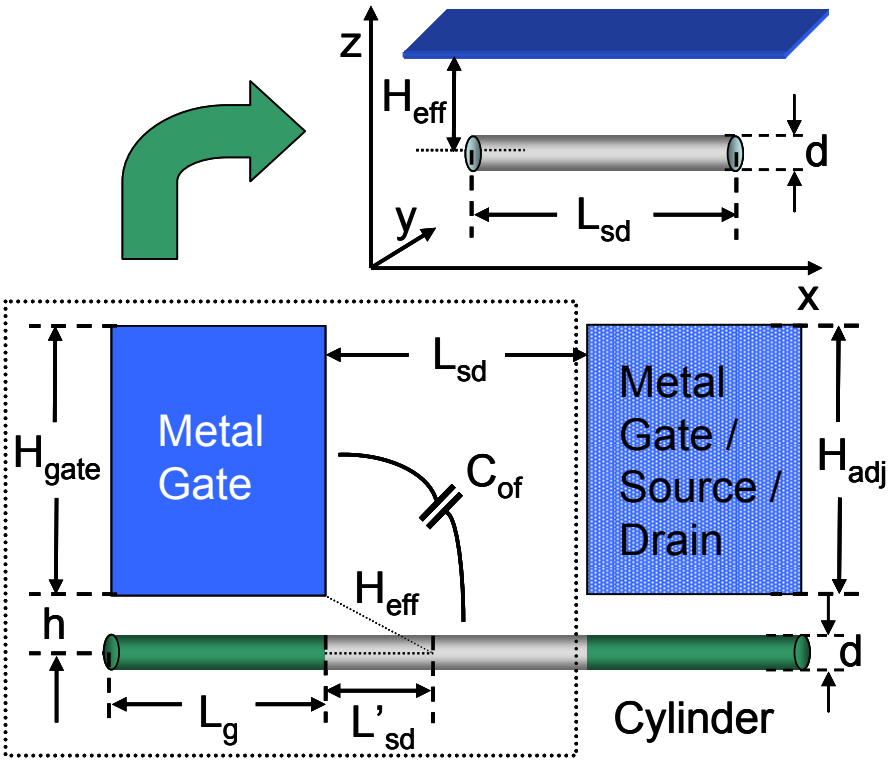

z
H_{eff}
d
y
L_{sd}
x
H_{gate}
Metal Gate
L_{sd}
C_{of}
Metal Gate / Source / Drain
H_{adj}
H_{eff}
h
d
L_g
L'_{sd}
Cylinder

Figure 8

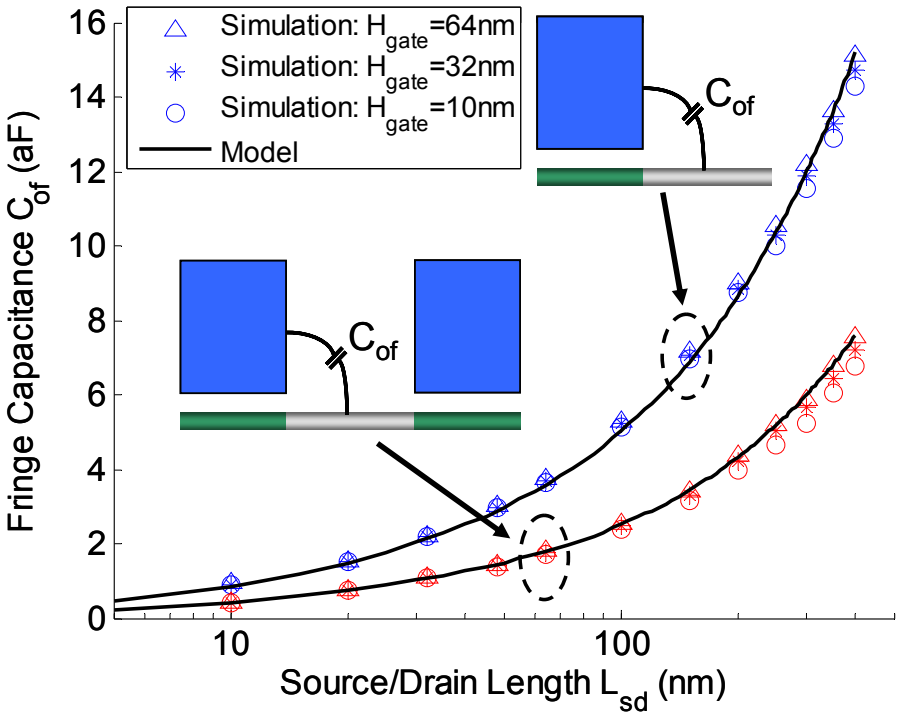

Simulation: H_gate=64nm
Simulation: H_gate=32nm
Simulation: H_gate=10nm
Model
C_of
C_of
Fringe Capacitance C_of (aF)
Source/Drain Length L_sd (nm)
0
2
4
6
8
10
12
14
16
10
100

Figure 9

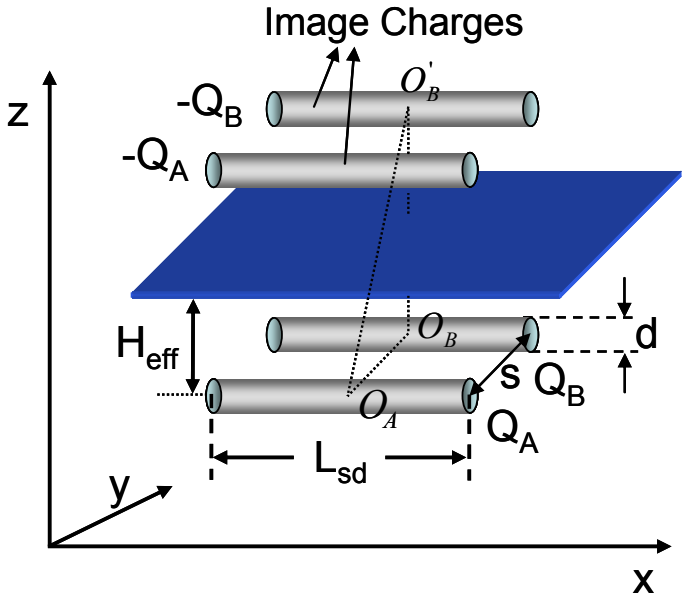
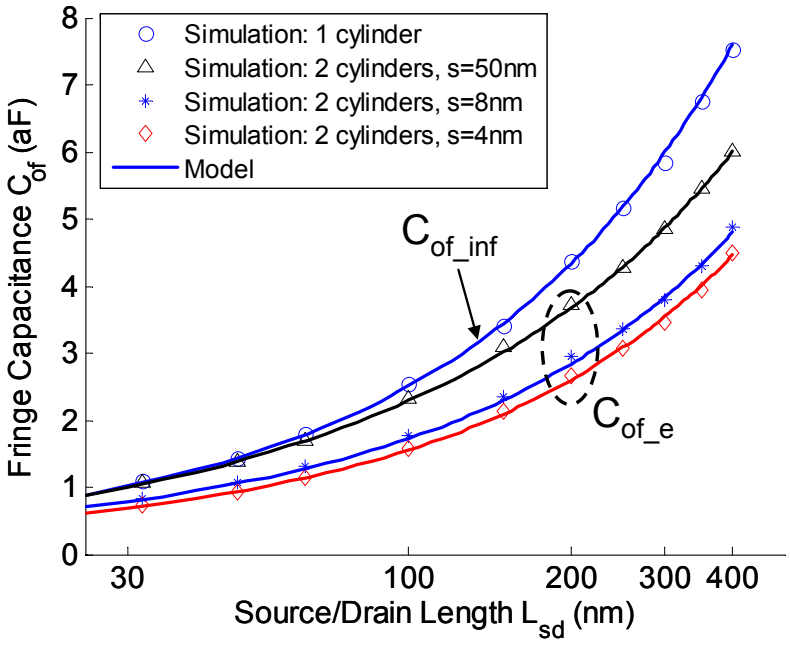
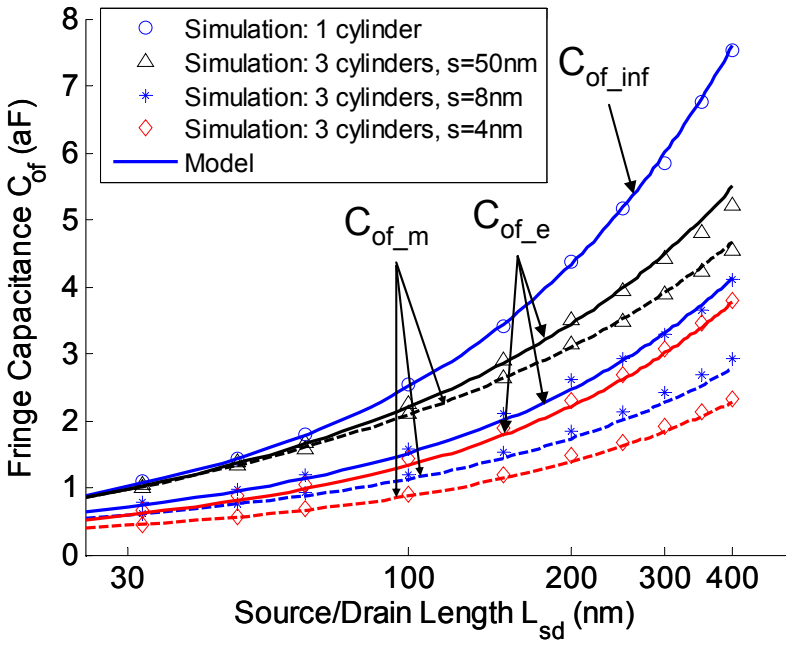


Figure 10


Simulation: 1 cylinder
Simulation: 2 cylinders, s=50nm
Simulation: 2 cylinders, s=8nm
Simulation: 2 cylinders, s=4nm
Model
C of_inf
C of_e
Fringe Capacitance C of (aF)
Source/Drain Length L sd (nm)
0
1
2
3
4
5
6
7
8
30
100
200
300
400

(a)


Simulation: 1 cylinder
Simulation: 3 cylinders, s=50nm
Simulation: 3 cylinders, s=8nm
Simulation: 3 cylinders, s=4nm
Model
C of_inf
C of_m
C of_e
Fringe Capacitance C of (aF)
Source/Drain Length L sd (nm)
0
1
2
3
4
5
6
7
8
30
100
200
300
400

(b)

Figure 11

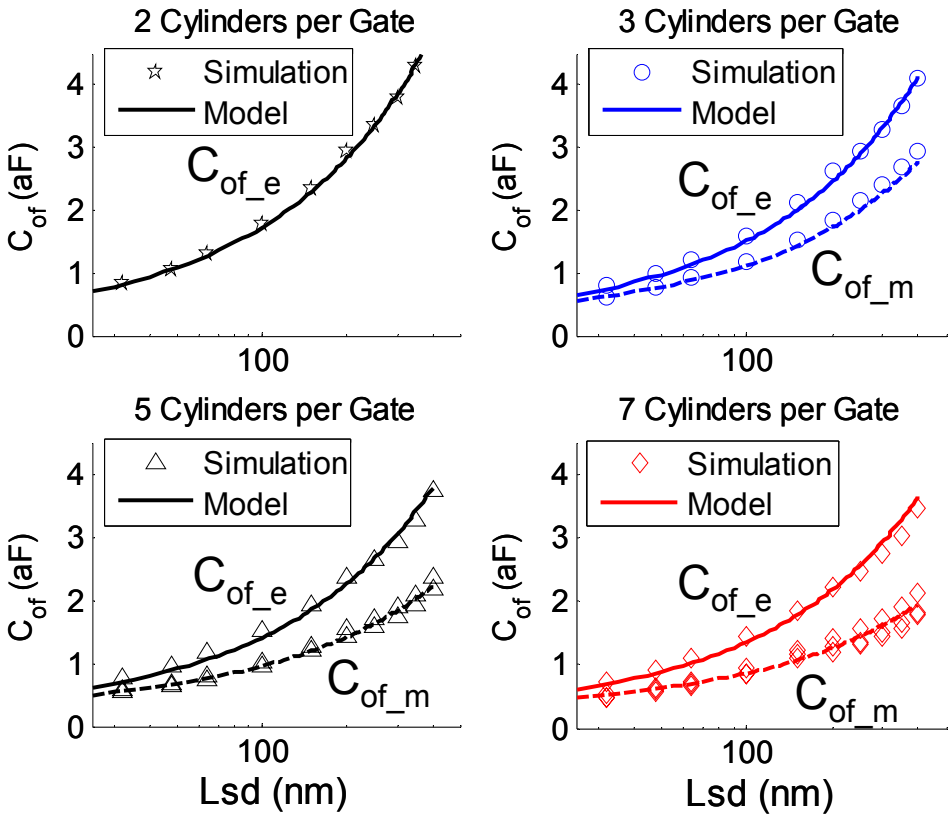

2 Cylinders per Gate
3 Cylinders per Gate
5 Cylinders per Gate
7 Cylinders per Gate
Simulation
Model
C_of_e
C_of_m
C_of (aF)
Lsd (nm)
0
1
2
3
4
100

Figure 12

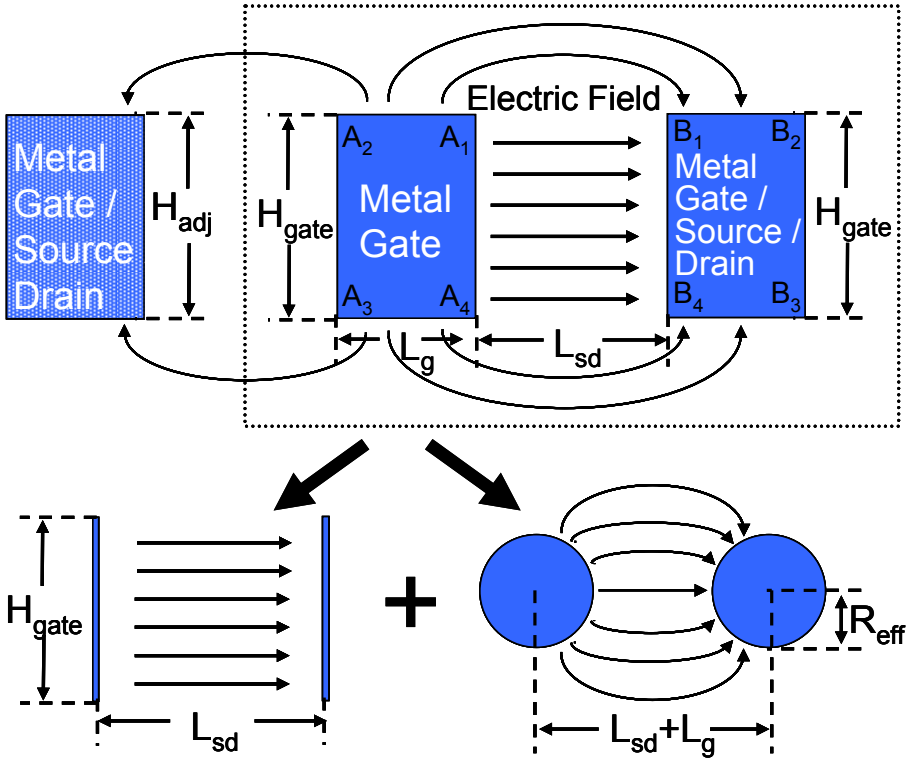

Electric Field
Metal Gate / Source Drain
H_{adj}
H_{gate}
A_2
A_1
Metal Gate
A_3
A_4
B_1
B_2
Metal Gate / Source / Drain
B_4
B_3
H_{gate}
L_g
L_{sd}
H_{gate}
L_{sd}
R_{eff}
$L_{sd}+L_g$

Figure 13

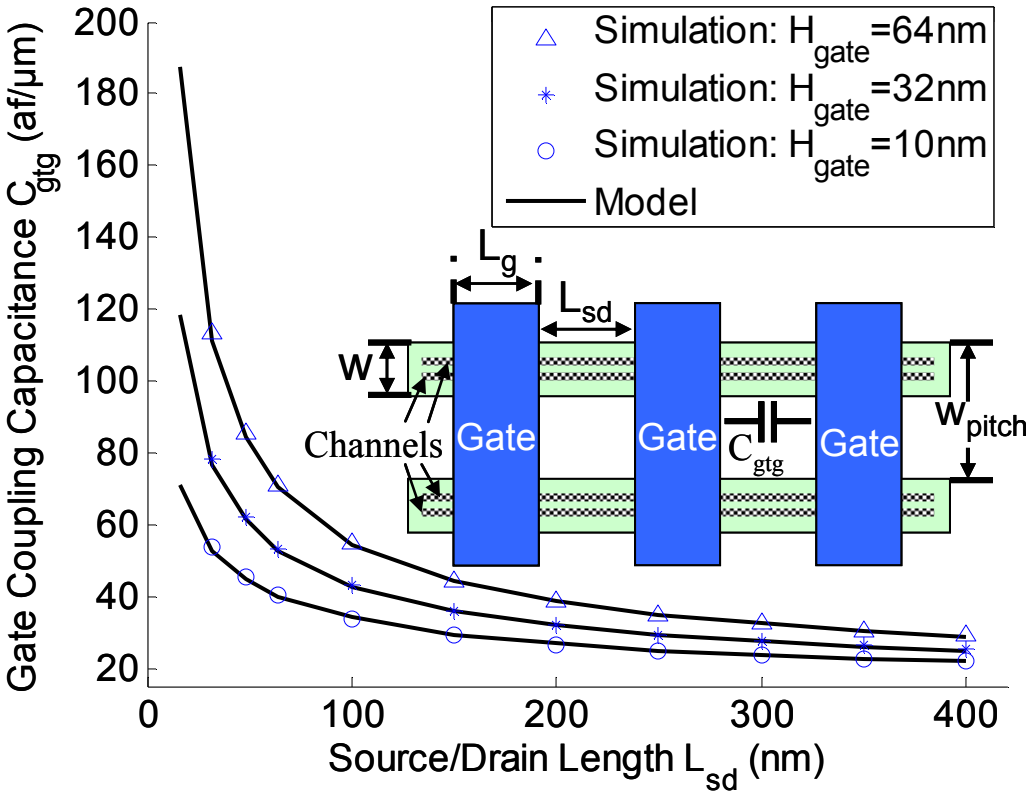

Simulation: H_gate=64nm
Simulation: H_gate=32nm
Simulation: H_gate=10nm
Model
Gate Coupling Capacitance C_gtg (af/μm)
Source/Drain Length L_sd (nm)
L_g
L_sd
W
W_pitch
Channels
Gate
Gate
Gate
C_gtg
200
180
160
140
120
100
80
60
40
20
0
100
200
300
400

Figure 14

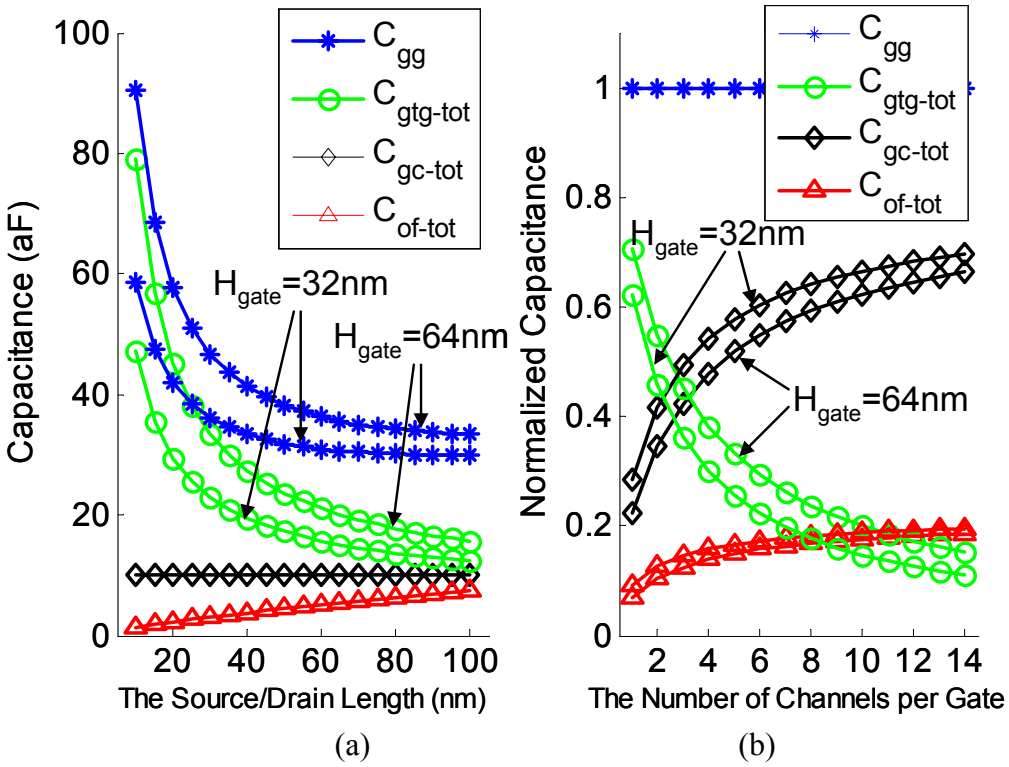

100
80
60
40
20
0
Capacitance (aF)
20
40
60
80
100
The Source/Drain Length (nm)
C gg
C gtg-tot
C gc-tot
C of-tot
H gate=32nm
H gate=64nm
(a)
1
0.8
0.6
0.4
0.2
0
Normalized Capacitance
2
4
6
8
10
12
14
The Number of Channels per Gate
C gg
C gtg-tot
C gc-tot
C of-tot
H gate=32nm
H gate=64nm
(b)

Figure 15

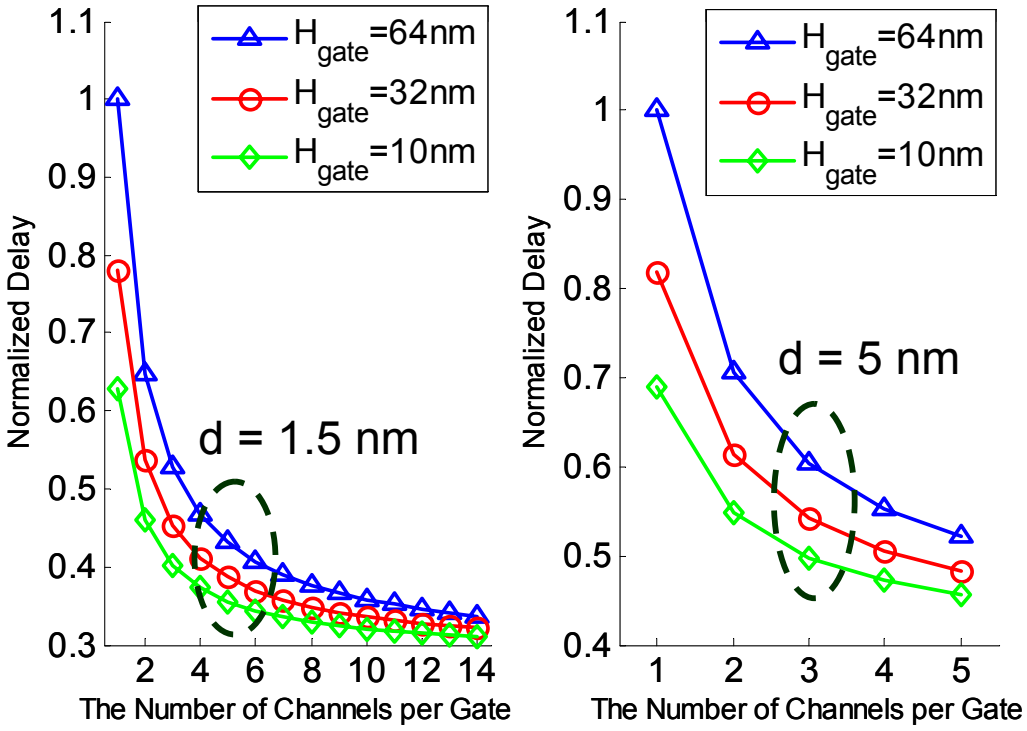

Normalized Delay
The Number of Channels per Gate
H_gate=64nm
H_gate=32nm
H_gate=10nm
d = 1.5 nm
d = 5 nm

Figure 16