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Enclosed for your consideration is the revised manuscript of the paper MS# 5245R, entitled "**A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non-Idealities and Its Application — Part I: Model of the Intrinsic Channel Region**". As such it belongs to the "Devices and Process Modeling" or the "Nanoelectronics" category.

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Sincerely yours,
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A Compact SPICE Model for Carbon Nanotube Field Effect Transistors Including Non-Idealities and Its Application — Part I: Model of the Intrinsic Channel Region

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Abstract. This paper presents a circuit-compatible compact model for the intrinsic channel region of MOSFET-like single-walled Carbon Nanotube Field-Effect Transistors (CNFETs). This model is valid for CNFET with a wide range of chiralities and diameters, and CNFET with either metallic or semiconducting CNT conducting channel. The modeled non-idealities include the quantum confinement effects on both circumferential and axial directions, the acoustical/optical phonon scattering in the channel region, and the screening effect by the parallel CNTs for CNFET with multiple CNTs. In order to be compatible with both large signal (digital) applications and small signal (analog) applications, a complete trans-capacitance network is implemented to deliver the real time dynamic response. This model is implemented with HSPICE. Using this model, we project a 13× CV/I improvement of intrinsic CNFET with (19,0) CNT over bulk n-type MOSFET at the 32 nm node. The model described in this paper serves as a starting point towards the complete CNFET device model incorporating additional device/circuit level non-idealities and multiple CNTs reported in [1].

Index Terms: CNFET, Compact Model, Analytical Model, Carbon Nanotube, SPICE, Intrinsic, Ballistic, Screening Effect.

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1. Introduction

As one of the promising new transistors, CNFET avoids most of the fundamental limitations for traditional silicon MOSFETs. With ultra long (~1μm) mean-free-path (MFP) for elastic scattering, ballistic or near-ballistic transport can be obtained with intrinsic CNT under low voltage bias to achieve the ultimate device performance [2,3,4,5]. The quasi-1D structure provides better electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (e.g. fully depleted SOI) structures [6].

Efforts have been made in recent years on modeling semiconducting CNFET [7,8,9,10] for digital logic applications and CNT for interconnects [11,12] in order to evaluate the potential performance at the device level. The reported compact models to date [7,8,9,10] used one or more lumped static gate capacitances and an ideal ballistic transport model. These simplifications make it questionable when evaluating the transient response and device dynamic performance. The integral function used in [7,8] requires intensive calculation efforts and thereby makes it difficult to implement in circuit simulators, e.g. HSPICE [13]. The polynomial fitting approach used in [9] improves the run time significantly, but it makes evaluating CNFET performance with different device parameters inconvenient. The simple coaxial or planer gate structures utilized in [7,8,10] differ from the typical realistic CNFET gate structure that consists of high-*k* gate oxide on top of SiO_2 insulating bulk. For a CNFET with multiple parallel CNTs [3], these published models cannot examine the multiple CNT-to-CNT screening effect on both the driving current and the effective gate capacitance. To evaluate CNFET circuit performance with improved accuracy, a CNFET device model with a more complete circuit-compatible structure and also incorporating the typical device/circuit non-idealities is necessary.

Considering both the fabrication feasibility [14] and superior device performance of the MOSFET-like CNFET as compared to the SB-controlled FET, we choose to focus on

MOSFET-like CNFETs in this work. This paper models the intrinsic channel region of the CNFET which serves as the first level modeling of the complete device model. This model includes the quantum confinement on both the circumferential and the axial directions, the acoustical/optical phonon scattering in the channel region, the screening effect by the parallel CNTs for CNFET with multiple CNTs, and the intrinsic ac behavior which is delivered by a dynamic gate capacitance network. The complete device model that includes the channel elastic scattering, the doped source/drain region, Schottky barrier (SB) resistance, multiple CNTs per device and other device/circuit non-idealities, and its applications are reported in [1][+]. The modeling approach and methodology described in this work is generally applicable to other 1-D device, e.g. silicon nanowire FET [6], provided that the appropriate equations for the band structure and/or density of states (DOS) are used.

This paper is organized as follows: First, we describe the device structure used for the modeling. Next, we show both the mathematical expressions and the circuit representations of each major component. Finally we will discuss the application of this model for a complete device model for circuit simulation [1].

2. Device Structure

A typical layout of a MOSFET-like CNFET device is illustrated in Figure 1. The CNT channel region is undoped, and the other regions are heavily doped, acting as both the source/drain extension region and/or interconnects between two adjacent devices (un-contacted source-gate/gate-drain configurations).

This paper describes the modeling of one single intrinsic channel of CNFET, as shown in Figure 1 inset, which is a starting point towards the complete device model reported in [1]. For MOSFET-like CNFET, since pFET behavior is similar to nFET, we only describe the equations

[+] The model is available at https://www.stanford.edu/group/nanoelectronics/model_downloads.htm

for nFET in this paper, though we implemented both nFET and pFET for the SPICE simulations.

3. Model of the Intrinsic Channel Region

This part models the intrinsic channel region of CNFET with near-ballistic transport, and without any parasitic capacitance and parasitic resistance. The equivalent circuit model is shown as Figure 2. Figure 2(a) is the equivalent circuit implemented with HSPICE, and Figure 2(b, c) are the other two possible implementations for the trans-capacitance network which will be discussed in Section 3.2.

The Fermi level profiles and the energy band diagram in the channel region with ballistic transport are illustrated in Figure 3(a). The potential differences μ_s-μ_s' and μ_d-μ_d' are determined by both the applied bias and the property of the source/drain extension regions. We will treat the non-ballistic transport and the potential drop at the source/drain extension region and the contacts in the complete device model [1]. We assume near-ballistic transport and ideal (reflectionless) contacts in this paper, i.e. $eV_{DS} \approx \mu_d - \mu_s$, so μ_s (μ_d) remains almost constant in the source-channel (drain-channel) region (Fig. 3(a)).

3.1 Current Sources

The single-walled carbon nanotube (SWCNT) is treated as quasi 1-D quantum wire in this work. For SWCNT with chiralities (n_1, n_2), the diameter (D_{CNT}) is given by (a = 2.49 Å is the lattice constant) [15],

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{p} \qquad (1)$$

SWCNTs can be grouped as either metallic nanotubes or semiconducting nanotubes [15]. For SWCNT with a finite length (L_g) and a finite diameter (D_{CNT}), applying the Born-von Karman boundary condition on both the circumferential direction and the axial (channel length) direction, the E-k dispersion relation is quantized into discrete sub-states. We denote (m,l) as the l^{th} sub-state at the m^{th} sub-band, k_m as the wave-number of the m^{th} sub-band in circumferential

direction, and k_l as the wave-number of the l th sub-state in current flow direction. We define the sub-bands with positive band gap as "semiconducting sub-bands", and the sub-bands with zero or negative band gap as "metallic sub-bands". Thus the band structure of metallic nanotubes can be treated as a summation of metallic sub-bands and semiconducting sub-bands.

The wave numbers related with semiconducting sub-bands are given by [15,16],

$$k_m = \frac{2p}{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}} \cdot l \qquad (2a)$$

$$l = \begin{cases} \dfrac{6m - 3 - (-1)^m}{12} & m = 1,2,... \quad , \mathrm{mod}(n_1 - n_2, 3) \neq 0 \\ m & m = 0,1,... \quad , \mathrm{mod}(n_1 - n_2, 3) = 0 \end{cases} \qquad (2b)$$

$$k_l = \frac{2p}{L_g} l \quad , l = 0,1,2,... \qquad (2c)$$

m=0 is reserved for the metallic sub-band. k_l approaches continuous values for large L_g. Around the Fermi point with carrier energy $E_{m,l} << V_\pi$ (~3.033eV, the carbon π-π bond energy in the tight bonding model), CNT E-k dispersion relation can be approximated as [15],

$$E_{m,l} \approx \frac{\sqrt{3}}{2} a V_p \sqrt{k_m^2 + k_l^2} \qquad (3)$$

$E_{m,l}$ is the carrier energy at the (m,l) sub-state above the intrinsic level E_i, and $E_{m,0}$ is the half band gap of the m^{th} sub-band.

We consider three current sources in CNFET model: (1) the thermionic current contributed by the semiconduting sub-bands (I_{semi}) with the classical band theory, (2) the current contributed by the metallic sub-bands (I_{metal}), and (3) the leakage current (I_{btbt}) caused by the band to band tunneling mechanism through the semiconducting sub-bands.

***I_{semi}*:** For semiconducting sub-bands, we only consider the electron current for the nFET because the hole current is suppressed by the n-type heavily doped source/drain. The current contributed by the sub-state (m,l) is given by,

$$J_{m,l}(V_{xs}, \Delta\Phi_B) = 2env_F \qquad (4)$$

V_{xs} is potential difference between node x and source. The Fermi velocity $v_F=1/\hbar\cdot\partial E/\partial k_l$. The factor of 2 is due to electron spin degeneracy, e is the unit electronic charge, and n is the number of electrons that occupy the sub-state (m,l), given by,

$$n = \frac{f_{FD}(E_{m,l} + eV_{xs} - \Delta\Phi_B)}{L_g} \qquad (5a)$$

$$f_{FD}(E) = \frac{1}{1+e^{E/kT}} \qquad (5b)$$

$\Delta\Phi_B$ is the channel surface potential change with gate/drain bias. $f_{FD}(E)$ is the Fermi-Dirac distribution function. k is the Boltzmann constant and T is the temperature in Kelvin. $E_{m,l}$ is the carrier energy at the substate (m, l).

With equations (4, 5), we obtain,

$$J_{m,l}(V_{xs}, \Delta\Phi_B) = \frac{2e}{h}\frac{\sqrt{3}apV_p}{L_g}\frac{k_l}{\sqrt{k_m^2 + k_l^2}}\frac{1}{1+e^{(E_{m,l}+eV_{xs}-\Delta\Phi_B)/kT}} \qquad (6)$$

The total current contributed by all sub-states is equal to the current flowing from the drain to the source (+k branch) minus the current flowing from the source to the drain (-k branch),

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) = 2\sum_{\substack{k_m \\ m=1}}^{M}\sum_{\substack{k_l \\ l=1}}^{L}\left[T_{LR}J_{m,l}(0,\Delta\Phi_B)\big|_{+k} - T_{RL}J_{m,l}(V_{ch,DS},\Delta\Phi_B)\big|_{-k}\right] \qquad (7)$$

$V_{ch,DS}$ and $V_{ch,GS}$ denotes the Fermi potential differences near source side within the channel. The factor of 2 is due to the double-degeneracy of the sub-band. M and L are the number of sub-bands and the number of sub-states, respectively. For typical devices with appropriate diameter range (D_{CNT} < 3nm) and short gate length ($L_g \leq$ 100nm), only the first 2 or 3 sub-bands and the first 10~15 sub-states have a significant impact on the current using a sub-1V power supply. Including more sub-bands should be done with more caution due to two limitations: (1) the band structure model used in this work requires $E_{m,l} << V_\pi$, (2) the complex phonon modes at high energy level. For long channel devices (L_g > 100nm), one can either approximate the current for short device equation (7) by setting L_g=100nm in equations (2c, 5a, 6), or use the long

channel model introduced in equation (14) below. T_{LR} and T_{RL} are the transmission probability of the carriers at the sub-state (m,l) in $+k$ branch and $-k$ branch, respectively. We consider three typical scattering mechanisms in the channel region: (1) acoustic phonon scattering (near elastic process [5]), (2) optical phonon scattering (inelastic process [4]), and (3) elastic scattering. The elastic scattering probability is assumed to be independent of the carrier energy, and will be treated in the complete device modeling [1]. Both the acoustic phonon scattering and optical phonon scattering depend on the carrier energy. Only intra-band scatterings are considered in this paper. Random angle scatterings are suppressed and only backscattering and forward scattering can occur in a 1-D quantum wire due to the Pauli's Exclusion principle and the confined k-space [17]. A scattering event from the sub-state (m,l_1) in $+/-k$ branch to the sub-state (m,l_2) in $-/+k$ branch can occur only if two conditions are satisfied: (1) the sub-state (m,l_1) is filled with electrons. (2) the sub-state (m,l_2) is empty so it can accept the scattered carrier from (m,l_1). Assuming the optical phonon scattering mean free path (MFP) (λ_{op} ~ 15 nm [18]) and the acoustic phonon scattering MFP (λ_{ap} ~ 500 nm [19]) are constant if both conditions are met, we normalize the effective acoustic phonon scattering MFP (l_{ap}) and the effective optical phonon scattering MFP (l_{op}) of the semiconducting sub-bands to the available target empty states,

$$l_{ap}(V_{xs},m,l)=\frac{l_{ap}D_o}{D(E_{m,l})[1-f_{FD}(E_{m,l}-\Delta\Phi_B+eV_{xs})]} \qquad (8a)$$

$$l_{op}(V_{xs},m,l)=\frac{l_{op}D_o}{D(E_{m,l}-\mathbf{h}\Omega)[1-f_{FD}(E_{m,l}-\mathbf{h}\Omega-\Delta\Phi_B+eV_{xs})]} \qquad (8b)$$

$\hbar\Omega$ (~0.16eV [18]) is the optical phonon energy that a carrier attains before a optical phonon scattering can occur. Optical phonon scattering becomes more significant at high $V_{ch,DS}$ bias. D_o is a constant $8/(3\pi V_\pi \cdot d)$ where d is the carbon-carbon bond distance, about 0.144 nm. $D(E)$ is the CNT universal density of states (DOS) which is valid in the range $E_{m,l} << V_\pi$ [15],

$$D(E) = \begin{cases} D_0 \cdot E / \sqrt{E^2 - E_{m,0}^2} & E > E_{m,0} \\ 0 & E \le E_{m,0} \end{cases} \qquad (9)$$

The effective phonon scattering MFP is in the form of,

$$\frac{1}{l_{eff}(V_{xs}, m, l)} = \frac{1}{l_{ap}(V_{xs}, m, l)} + \frac{1}{l_{op}(V_{xs}, m, l)} \qquad (10)$$

It is reasonable to assume that the phonon back-scattered carriers are not likely to be back-scattered again due to the energy loss and/or the occupied states. Thus the transmission probabilities in equation (7) are given by,

$$T_{LR} = \frac{l_{eff}(V_{ch,DS}, m, l)}{l_{eff}(V_{ch,DS}, m, l) + L_g} \qquad (11a)$$

$$T_{RL} = \frac{l_{eff}(0, m, l)}{l_{eff}(0, m, l) + L_g} \qquad (11b)$$

The key parameter for evaluating CNFET current is $\Delta\Phi_B$, the channel surface potential change in response to changes in gate and source/drain bias. As shown in Figure 3(b), there are three electrostatic coupling capacitors assuming the channel material is with infinite DOS: the capacitance (C_{ox}) between the gate and channel, the capacitance (C_{sub}) between channel and substrate, and the capacitance (C_c) between channel and external drain (D') / source (S'). $\Delta\Phi_B$ is dynamically affected by the drain bias. βC_c is a fitting parameter that describes this effect due to two mechanisms: (1) the surface potential lowering due to the electrostatic coupling between the channel region and the external drain electrode through fringing electric field; (2) the surface potential lowering due to non-uniform channel surface potential profile caused by DIBL effect. Operationally, the parameters C_c and β are chosen to fit the sub-threshold slope and the measured short channel effect. For a semiconducting channel with a finite DOS, the channel surface potential $\Delta\Phi_B$ changes with the gate bias at a rate $\Delta\Phi_B/\Delta V_{GS} < 1$, a phenomenon known as the effect of quantum capacitance. We calculate $\Delta\Phi_B$ using the charge conservation equations,

$$Q_{cap} = Q_{CNT} \qquad (12a)$$

$$Q_{cap} = C_{ox}(V_{ch,GS} - V_{FB}) + C_{sub}V_{ch,BS} + bC_cV_{ch,D'S} + (1-b)C_cV_{ch,S'S} - (C_{ox} + C_{sub} + C_c)\frac{\Delta\Phi_B}{e} \quad (12b)$$

$$Q_{CNT} = \frac{4e}{L_g}\sum_{\substack{k_m \\ m=m0}}^{M}\sum_{\substack{k_l \\ l=0}}^{L}\left[\frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B)/kT}} + \frac{1}{1+e^{(E_{m,l}-\Delta\Phi_B+eV_{DS})/kT}}\right] \quad (12c)$$

$$m0 = \begin{cases} 1 & ,\mathrm{mod}(n_1 - n_2, 3) \neq 0 \\ 0 & ,\mathrm{mod}(n_1 - n_2, 3) = 0 \end{cases} \quad (12d)$$

The factor of 4 includes both the spin degeneracy and the double-degeneracy of the sub-band. V_{FB} is the flat band voltage, and V_{BS} is the potential difference between substrate and source. Q_{cap} is the charge induced by the electrodes, and Q_{CNT} is the total charge induced on SWCNT surface. We solve equation (12) iteratively using a construct in HSPICE (Fig. 2(a)).

The front gate capacitance C_{ox} is modeled as a planar gate structure with high-k gate dielectric on top of SiO_2 insulating layer (Fig. 1). For the device with multiple SWCNTs in parallel, C_{ox} is grouped into the capacitance between gate and SWCNT at the two ends (C_{ox_e}), and the capacitance between gate and SWCNT in the middle (C_{ox_m}) [20]. For SWCNT of 1.5 nm diameter with 4 nm thick HfO_2 (k_1=16) and 5 nm inter-CNT spacing, C_{ox_e} = 246 aF/μm and C_{ox_m} = 186 aF/μm. The substrate to gate capacitance C_{sub} can either be calculated similarly if a double gate device is desired, or be calculated with the simple equation, $C_{sub} = 2\pi k_2\varepsilon_0/\ln(2H_{sub}/r)$.

For a long channel device (L_g >> 100 nm), the wave number k_l can be represented as a continuous variable. By replacing the inner summation with the integral function and assuming T_{LR}=T_{RL}=T_m, equation (7) can be simplified as,

$$I_{semi}(V_{ch,DS}, V_{ch,GS}) \approx \frac{4e^2}{h}\sum_{\substack{k_m \\ m=1}}^{M} T_m \cdot \left[V_{ch,DS} + \frac{kT}{e}\ln\left(\frac{1+e^{(E_{m,0}-\Delta\Phi_B)/kT}}{1+e^{(E_{m,0}-\Delta\Phi_B+eV_{ch,DS})/kT}}\right)\right] \quad (14)$$

The above equations utilize the approximated SWCNT band structure (Equ. 2, 3) which is valid in the range $E_{m,l} << V_\pi$. A more accurate model can be obtained by replacing the simplified band-structure with the tight binding model [21] at the cost of more intensive calculations (~3x), or an exact analytical form valid only for achiral CNTs [22]. Little difference is found for both

the *E-k* relationship and the current drive in low energy range (Fig. 4). The chirality difference for SWCNTs with the same diameter can also be ignored for our purpose, in the range where the carrier energy is less than 1.0 eV (Fig. 4).

I_{metal}: For metallic sub-bands of metallic nanotubes, the current includes both the electron current and the hole current,

$$I_{metal} = 2(1-m0)T_{metal}\sum_{\substack{k_l \\ l=1}}^{L}\left[J_{ele\_0,l} + J_{hole\_0,l}\right] \qquad (15a)$$

$$J_{ele\_0,l} = \frac{2e}{h}\frac{\sqrt{3}apV_p}{L_g}\left(f_{FD}(E_{0,l} - \Delta\Phi_B) - f_{FD}(E_{0,l} + eV_{ch,DS} - \Delta\Phi_B)\right) \qquad (15b)$$

$$J_{hole\_0,l} = \frac{2e}{h}\frac{\sqrt{3}apV_p}{L_g}\left(f_{FD}(-E_{0,l} - \Delta\Phi_B) - f_{FD}(-E_{0,l} + eV_{ch,DS} - \Delta\Phi_B)\right) \qquad (15c)$$

The transmission probability T_{metal} is given by,

$$T_{metal} = \frac{l_{ap}\,l_{op}}{l_{ap}\,l_{op} + (l_{ap} + l_{op})\cdot L_g} \qquad (16)$$

If the summation function is replaced with an integral, equation (15) can be simplified to,

$$I_{metal} = (1-m0)\frac{4e^2}{h}T_{metal}V_{ch,DS} \qquad (17)$$

Thus I_{metal} is independent of the channel surface potential change $\Delta\Phi_B$ as expected because the DOS of metallic CNT is independent of the carrier energy. For metallic CNTs of less than 3 nm in diameter, the half band-gap of the first semiconducting subband is larger than 0.43 eV. Considering the large quantum capacitance of metallic CNT and the typical gate electrostatic capacitance discussed in Section 4, the semiconducting subbands in a metallic CNT are not likely to be populated in and thereby contribute to the current with sub-1V power supply.

***I_{btbt}*:** In the sub-threshold region, especially with negative gate bias (nFET), the band-to-band tunneling (BTBT) current from drain to source becomes significant. As shown in Figure 5, there are two possible tunneling regions: the “n” shape region 1 and the “L” shape

region 2. With $V_{ch,DS} > E_{1,0}$, the tunneling through the drain junction in region 1 causes holes (electrons) pile up in the nFET (pFET) channel region because the source junction prohibits the holes (electrons) from escaping away. The hole (electron) pile up results in surface potential lowering and thereby a higher current and worse sub-threshold behavior [23]. Little such effect is observed for well-tempered devices [14]. To simplify the modeling, we ignore this effect in this work. Because the tunneling through the source junction in region 1 is prohibited, we only consider the BTBT current through the drain junction in region 2. Assuming ballistic transport for the tunneling process, the BTBT current is approximated by the BTBT tunneling probability (T_{btbt}) times the maximum possible tunneling current integrating from the conduction band at drain side up to the valance band at source side,

$$I_{btbt} = \frac{4e}{h} kT \cdot \sum_{\substack{k_m \\ m=1}}^{M} \left[T_{btbt} \ln\left(\frac{1+e^{(eV_{ch,DS}-E_{m,0}-E_f)/kT}}{1+e^{(E_{m,0}-E_f)/kT}} \right) \cdot \frac{\max(eV_{ch,DS}-2E_{m,0},0)}{eV_{ch,DS}-2E_{m,0}} \right] \qquad (18)$$

E_f is the Fermi level of the doped source/drain nanotube in units of eV. Following the work of Kane [24,25], the WKB-like transmission coefficient is given by,

$$T_{btbt} \approx \frac{p^2}{9} \exp\left(-\frac{p m^{*(1/2)} (h_m 2E_{m,0})^{3/2}}{2^{3/2} e \cdot \mathbf{h} \cdot F} \right) \qquad (19)$$

η_m is a fitting parameter, set to 0.5 in this work, which represents the band gap narrowing effect under high electrical field [26,27]. $F = (V_{ch,DS} + (E_f - \Delta\Phi_B)/e)/l_{relax}$ is the electrical field triggering the tunneling process near the drain side junction. The potential drop across channel-drain junction is assumed to relax over the distance l_{relax} which affects both BTBT current slope and its magnitude. m^* is the effective electron mass, defined as $\hbar^2/(\partial^2 E_{m,l}/\partial k_l^2)$ [+].

3.2 Trans-Capacitance Network

To model the intrinsic ac response of CNFET device, we use a controlled trans-capacitance array among the four electrodes (*G*, *S*, *D*, *B*) with the Meyer capacitor model [28]. C_{IJ} is the mathematically derived trans-capacitance per unit gate length (L_g) between the node *i* and node *j*,

[+] m^* is about $0.05m_o$ and $0.10m_o$ for the carriers in the 1st and the 2nd (semiconducting) sub-band, respectively, where m_o is the electron rest mass.

defined as $|\partial Q_I/\partial V_J|$. The actual trans-capacitance in the channel region is $C_{ij} = C_{IJ}L_g$ (Fig. 2(a)).

First, we consider the source/drain capacitance with respect to gate/substrate voltage variation. There are two methods to assign the charges in channel region to the source and the drain: (1) assuming near-ballistic transport in the channel, the carrier distribution along the channel should be almost uniform, i.e. $Q_{s,ch} \approx Q_{d,ch}=Q_{cap}/2=Q_{CNT}/2$; (2) all the carriers from $+k$ branches are assigned to the source and all the carriers from $-k$ branches are assigned to the drain. The first approach is more reasonable in representing the physical meaning of the capacitor (a carrier reservoir which does not distinguish where the carriers come from), while it may result in $C_{ij} \neq C_{ji}$. We first discuss the former (charge separation) approach which results in the equivalent circuit model in Figure 2(a). All the carriers in both the channel region and the source/drain nodes (Fig. 3(b)) come from the (external) source and drain electrodes, thus $Q_S = L_g \cdot (Q_{cap}/2 + (1-\beta)C_c \cdot \Delta\Phi_B)$ and $Q_D = L_g \cdot (Q_{cap}/2 + \beta C_c(\Delta\Phi_B - V_{DS}))$. We denote the total electrostatic coupling capacitance per unit length between channel and other electrodes as $C_{tot}=C_{ox}+C_{sub}+C_c$. Taking the partial dirivative of Q_S and Q_D over V_G, we obtain,

$$C_{sg} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot} - 2(1-b)C_c}{\partial V_G / \partial \Delta\Phi_B} \right) \qquad (20a)$$

$$C_{dg} = \frac{L_g}{2}\left(C_{ox} - \frac{1}{e}\frac{C_{tot} - 2bC_c}{\partial V_G / \partial \Delta\Phi_B} \right) \qquad (20b)$$

$\partial V_G/\partial\Delta\Phi_B$ can be calculated by equating $\partial Q_{cap}/\partial\Delta\Phi_B$ and $\partial Q_{CNT}/\partial\Delta\Phi_B$ with fixed $V_{ch,S}$, $V_{ch,D}$ and V_B using Equ. (12b, 12c),

$$\frac{\partial V_G}{\partial \Delta\Phi_B} = \frac{1}{eC_{ox}}\left(C_{tot} + C_{Qs} + C_{Qd}\right) \qquad (21a)$$

$$C_{Qs} = \frac{4e^2}{L_g \cdot kT} \sum_{\substack{k_m \\ m=m0}}^{M} \sum_{\substack{k_l \\ l=0}}^{L} \left[\frac{e^{(E_{m,l}-\Delta\Phi_B)/kT}}{(1+e^{(E_{m,l}-\Delta\Phi_B)/kT})^2} \right] \qquad (21b)$$

$$C_{Qd} = \frac{4e^2}{L_g \cdot kT} \sum_{\substack{k_m \\ m=m0}}^{M} \sum_{\substack{k_l \\ l=0}}^{L} \left[\frac{e^{(E_{m,l}-\Delta\Phi_B+eV_{ch,DS})/kT}}{(1+e^{(E_{m,l}-\Delta\Phi_B+eV_{ch,DS})/kT})^2} \right] \qquad (21c)$$

We define C_{Qs} and C_{Qd} as the quantum capacitance due to the carriers from source (+k branch) and drain (−k branch), respectively. With small gate bias ($E_{m,0}$>>$\Delta\Phi_B$), $\partial V_G/\partial\Delta\Phi_B \approx C_{tot}/(eC_{ox})$, thus the channel acts as a linear voltage divider which has little dependence on quantum capacitance. With large gate bias ($E_{m,0}$ < $\Delta\Phi_B$), $\partial V_G/\partial\Delta\Phi_B > C_{tot}/(eC_{ox})$, thus the surface potential will be limited by the quantum capacitance. With equations (20, 21), we obtain,

$$C_{sg} = \frac{L_g C_{ox}}{2} \frac{C_{Qs} + C_{Qd} + 2(1-b)C_c}{C_{tot} + C_{Qs} + C_{Qd}} \qquad (22a)$$

$$C_{dg} = \frac{L_g C_{ox}}{2} \frac{C_{Qs} + C_{Qd} + 2bC_c}{C_{tot} + C_{Qs} + C_{Qd}} \qquad (22b)$$

We can follow a similar approach to calculate the capacitance C_{sb} and C_{db} as $C_{sb}=C_{sg}\cdot(C_{sub}/C_{ox})$ and $C_{db}=C_{dg}\cdot(C_{sub}/C_{ox})$, respectively.

The charges accumulated on the gate and substrate (back gate) electrodes are given by $Q_G=L_g\cdot C_{ox}\cdot(V_{GS}-V_{FB}-\Delta\Phi_B)$ and $Q_B= L_g\cdot C_{sub}\cdot(V_{BS}-\Delta\Phi_B)$, respectively. With a similar approach, the coupling capacitance between the gate and the substrate is derived as,

$$C_{bg} = C_{gb} = \frac{L_g C_{sub} C_{ox}}{C_{tot} + C_{Qs} + C_{Qd}} \qquad (23)$$

Next, we consider the gate/substrate capacitance due to source/drain voltage variation. With the similar approach as above, we obtain,

$$C_{gs} = \frac{L_g C_{ox}[C_{Qs} + (1-b)C_c]}{C_{tot} + C_{Qs} + C_{Qd}} \qquad (24a)$$

$$C_{gd} = \frac{L_g C_{ox}(C_{Qd} + bC_c)}{C_{tot} + C_{Qs} + C_{Qd}} \qquad (24b)$$

$$C_{bs} = C_{gs}\frac{C_{sub}}{C_{ox}} \qquad (24c)$$

$$C_{bd} = C_{gd}\frac{C_{sub}}{C_{ox}} \qquad (24d)$$

The above equations give the values of the 9 capacitors in Figure 2(a). If we use the second

channel charge separation approach (+k carriers for source and −k carriers for drain), reciprocality is guaranteed and $C_{sg}=C_{gs}$, $C_{dg}=C_{gd}$, $C_{sb}=C_{bs}$, and $C_{db}=C_{bd}$, thus the gate capacitance network can be simply represented by the 5-capacitor model in Fig. 2(b), or by the 6-capacitor model, as shown in Fig. 2(c), that shows explicitly the electrostatic capacitance and the quantum capacitance with the same transfer function as the 5-capacitor model.

4. Discussion

Figure 6 shows the intrinsic channel current with incremental non-idealities. Assuming ballistic transport, there is little difference (< 3%) between the on-current for an infinitely long gate length and the on-current for a 100 nm gate length device, thus it is reasonable to assume the ideal device current drive with gate length longer than 100 nm to be independent of the gate length. With 32 nm gate length, the on-current is about 90% of the long channel value. This slight ballistic current drop from long channel device to short channel device is due to the energy quantization (k_l quantization) in the axial direction. Phonon scattering in the 32 nm long channel region further reduces the on-current by ~7%. BTBT current is only significant with high V_{ds} bias, and the sub-threshold slope gets worse with larger electrostatic capacitance between the channel and the substrate (the inset in Fig. 6).

The intrinsic on-current ($I_{on}@V_{ds}=V_{gs}=0.9V$) dependence on the gate length is illustrated in Figure 7. With ideal ballistic transport, the on-current is almost constant with respect to the gate length except for a slight current drop for short gate lengths (L_g < 100 nm) due to the energy quantization in the axial direction. This small current drop is likely to be smeared out by phonon scattering in practice. Optical phonon scattering depends on the carrier energy. A smaller current means a smaller number of high-energy carriers, and therefore there is less chance that optical phonon scattering can occur. As a result, the current reduction rate with only optical phonon scattering becomes smaller as L_g increases because optical phonon scattering rate decreases as

current decreases. Optical phonon scattering is important for short channel device due to its short MFP (~15nm). Acoustic phonon scattering with longer MFP (~500nm) continues to be important as L_g increases as the acoustic phonon energy is small (assuming zero in the model), and therefore acoustic phonon scattering has a weak dependence on the carrier energy. Diffusive transport ($I_{on} \propto 1/L_g$) dominates as L_g increases and acoustic phonon scattering increases.

For the device with multiple CNTs, screening by the parallel CNTs affects both the gate to channel capacitance and the current drive (Fig. 8). With a typical realistic gate structure (3 nm thick HfO_2), the currents carried by the individual CNTs are almost identical if the inter-CNT pitch is larger than 20 nm. A factor of 2 reduction in current can be observed for dense CNT array (~ 2.5 nm inter-CNT pitch). The screening effect should be seriously taken into account when designing high-performance CNFET circuits to avoid overestimating the circuit performance.

Two types of CNFET device connections and the resultant trans-capacitances are illustrated by Figure 9. All the capacitances are non-linear components which depend on the bias due to the energy-dependent DOS. With MOS-CAP connection (Fig. 9(b)), the two peaks correspond to the position of the first two sub-bands (~0.3eV for the 1st subband and ~0.6eV for the 2nd subband, for (19,0) CNT). This property can potentially be used to determine the nanotube diameter once the gate capacitance is measured [29]. The CNFET effective gate capacitance for one CNT per gate is about 3.6 aF with 18 nm physical gate length, which is about 4% of the bulk CMOS gate capacitance (predictive BSIM model [30,31,32]) with minimum gate width (48 nm) at the 32 nm node. Considering the large drive current which can be delivered by a single CNT (~35μA@V_{dd}=0.9V, ~50% of the bulk n-type MOSFET on-current with 48 nm gate width), the CV/I improvement of intrinsic CNFET over bulk MOSFET device is about 13× better. This large improvement comes from both the much higher carrier velocity of CNT with ballistic transport

(the Fermi velocity $v_{F,CNT} \approx 8.0\times10^7$ cm/s, $v_{F,si} \approx 2.5\times10^7$ cm/s), and the large parasitic gate capacitance of MOSFET device. We will show in [1] that this optimistic performance advantage is not achievable in a practical device structure and will be significantly degraded by the device/circuit non-idealities, including the series resistance of doped source/drain region, the Schottky barrier (SB) resistance at the metal/CNT interface, the gate outer-fringe capacitance, and the interconnect wiring capacitance.

5. Summary

We present a circuit-compatible compact model of the intrinsic channel region of MOSFET-like single-walled Carbon Nanotube Field-Effect Transistors (CNFETs) including some channel region non-idealities. Comparison with a more accurate device model using the tight binding band structure model shows that this model is valid for CNFET with a wide range of chiralities and diameters. This model uses a sub-state summation approach, instead of the integral, to calculate the parameters. This approach makes the modeling methodology described in this paper is generally applicable to other 1-D devices, e.g. silicon nanowire FET, and requires less computation efforts, thereby is more compatible with a circuit simulator. The complete dynamic gate capacitance network makes the model suitable for both small signal (analog) and large signal (digital) applications. This model serves as a start point towards the complete CNFET device model including device/circuit level non-idealities and multiple CNTs which is reported in [1].

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Figure Captions:

Figure 1. The 3-D device structure of CNFETs with multiple channels, high-*k* gate dielectric material, and the related parasitic gate capacitances. In this example, three CNFETs are fabricated along one single CNT. The channel region of CNTs is un-doped, and the other regions of CNTs are heavily doped. The inset shows the 3-D device structure of CNFET that is modeled in this paper, with only the intrinsic channel region.

Figure 2. The equivalent circuit model for the intrinsic channel region of CNFET. (a) The 9-capacitor model assuming the carrier distribution along the channel is uniform. Exxx is the voltage controlled voltage source, and the potential of Vxxx equals to the controlling voltage source. R_{dummy} is a large value (>1E15) resistor to keep the circuit stable. (b) The 5-capacitor model, and (c) the 6-capacitor model, assuming all the carriers from $+k$ branches are assigned to the source and all the carriers from $-k$ branches are assigned to the drain.

Figure 3. (a) Ideal CNFET with ballistic (intrinsic) channel. Superposed are the Fermi level profiles (solid arrows) from source to drain and the energy band diagram (dashed lines) with bias $V_{DS} = (\mu_d - \mu_s)/e$. (b) The electrostatic capacitor model used to calculate the channel surface potential change $\Delta\Phi_B$ before and after Gate/Source/Drain/Substrate bias. All the node potentials are referred to the input source Fermi level. Superposed is the energy band diagram (only the first sub-band shown) from the external source node S' to the external drain node D'.

Figure 4. The comparison of the band structure calculated by the simple model used in this work (the dotted curves) and the corresponding results calculated using tight binding models with the same CNT diameter (1.5nm) for three different chiralities (the solid curve is for (19,0) CNT, the dot-dashed curve is for (18,2) CNT, and the dashed curve is for (16,5) CNT). The simple model matches well with the tight banding models for the first two subbands with $E_{m,l}$ < 1.0 eV, and significant discrepancies among the four models are found for the 3rd and higher subbands with

$E_{m,l}$ > 1.0 eV.

Figure 5. Energy band diagram (only the first sub-band is shown) and the associated Fermi levels at source/drain side for CNFET with moderate gate and drain bias. There are two possible tunneling regions: region 1 and region 2, which are shaded on the plot. We only consider the tunneling through region 2 in this work.

Figure 6. The drain current @ (V_{gs}=0.9V, V_{FB}=0V) for (19, 0) chirality CNFET with incremental non-idealities. The front gate dielectric material is 3 nm thick HfO_2 on top of 10 μm thick SiO_2 insulating layer. Inset plot shows the drain current as a function of V_{gs} with different channel to substrate electrostatic capacitance.

Figure 7. The on-current @ (V_{gs}=V_{ds}=0.9V) as a function of the gate length L_g. With ballistic transport, the on-current is almost constant for long gate (L_g > 100 nm) CNFET, and there is a slight drop in on-current for short gate (L_g < 100 nm) CNFET due to energy quantization in the axial direction. Optical phonon scattering is important for shorter gate lengths because of its short MFP (~15nm). Acoustic phonon scattering continues to be important as L_g increases.

Figure 8. For CNFET with multiple parallel CNTs, the CNT to CNT screening reduces both the gate to channel electrostatic capacitance (inset) and the drain current. For a typical gate structure with 3 nm thick HfO_2 gate dielectric material, the screening effect is easily observable when the inter-CNT pitch is smaller than 20 nm.

Figure 9. (a) The trans-capacitances C_{IJ} per unit length as a function of V_{ds} @ (V_{gs}=0.9V), and (b) the gate and substrate node capacitances (C_{gg} and C_{bb}) per unit length as a function of the channel surface potential $\Delta\Phi_B$, for (19,0) semiconducting CNFET at room temperature (T=300K). The flat band voltage is zero. The front gate dielectric is 3 nm thick HfO_2 on top of 10 μm thick SiO_2 insulting layer.

Figures:

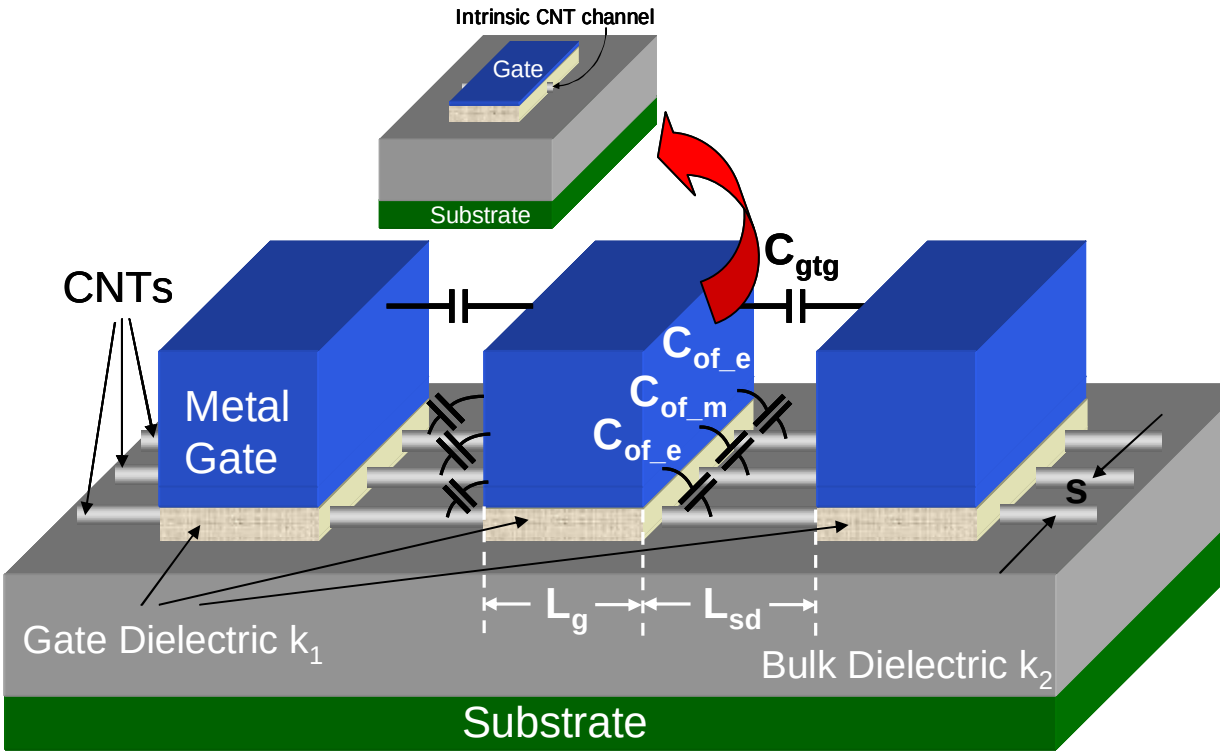


Figure 1.

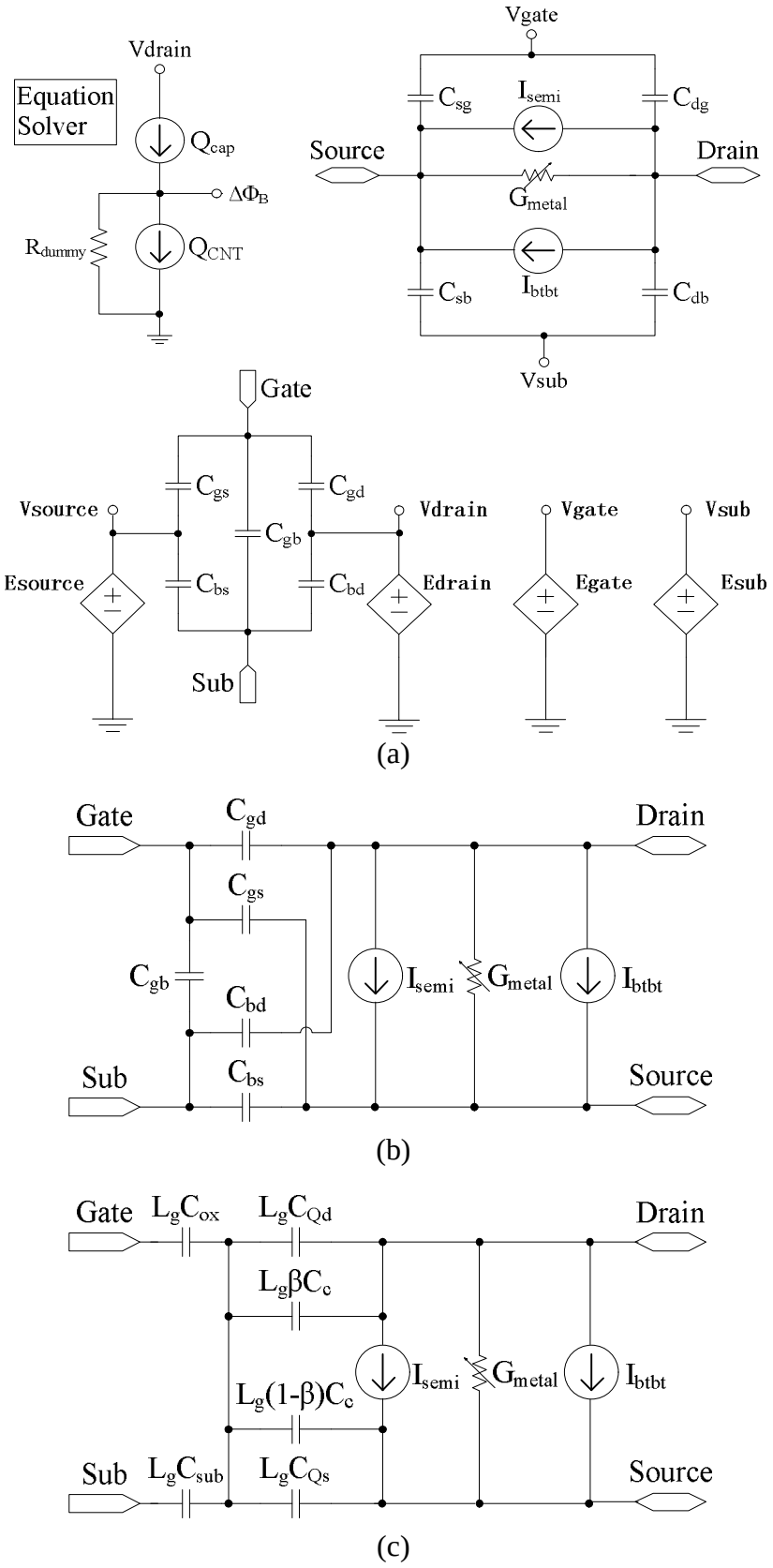
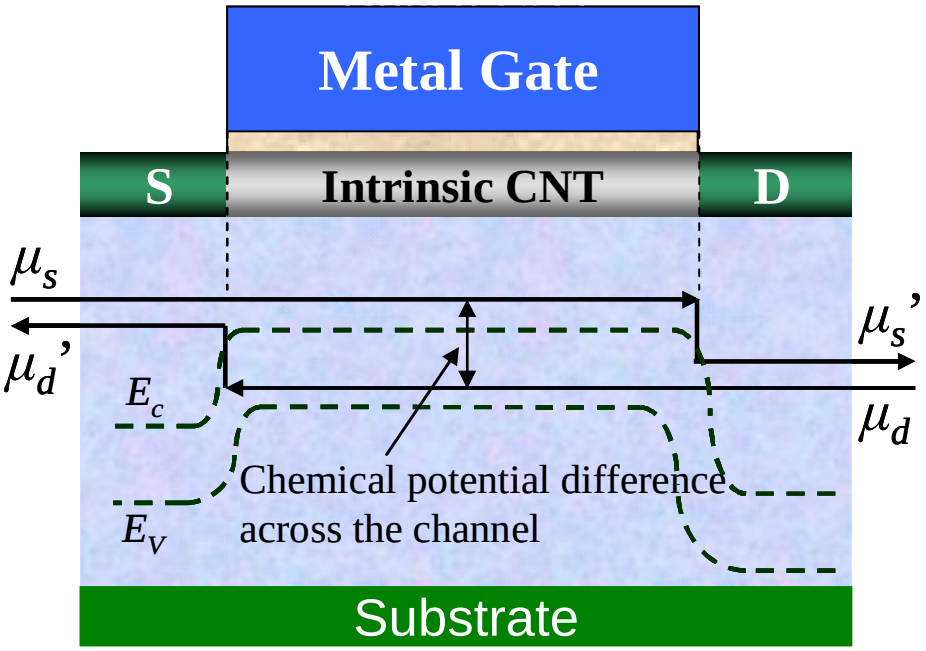
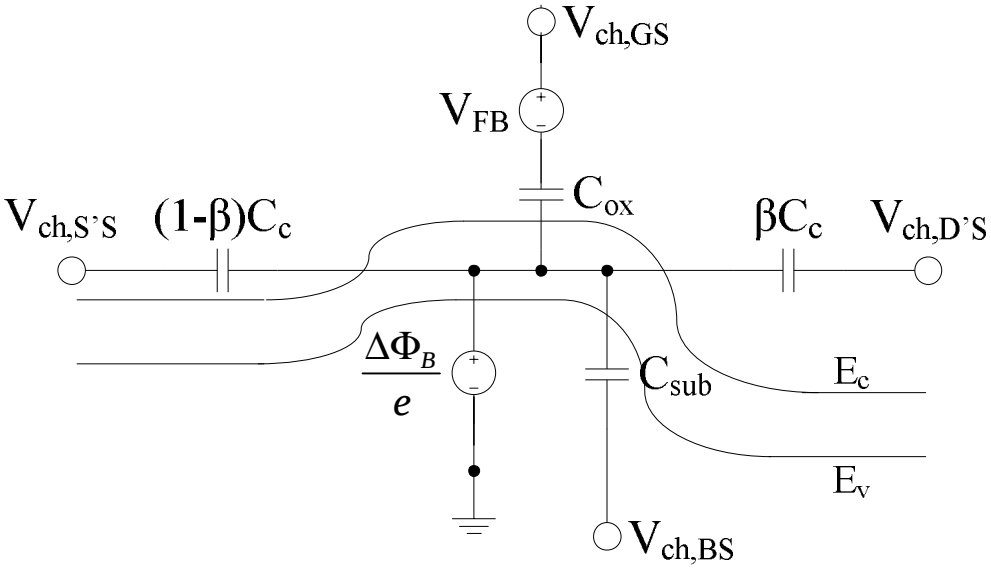

Vdrain
Equation Solver
Qcap
ΔΦB
Rdummy
QCNT
Vgate
Csg
Isemi
Cdg
Source
Drain
Gmetal
Csb
Ibtbt
Cdb
Vsub
Gate
Cgs
Cgd
Vsource
Vdrain
Cgb
Esource
Cbs
Cbd
Edrain
Sub
Vgate
Egate
Vsub
Esub
(a)
Gate
Cgd
Drain
Cgs
Cgb
Isemi
Gmetal
Ibtbt
Cbd
Sub
Cbs
Source
(b)
Gate
LgCox
LgCQd
Drain
LgβCc
Isemi
Gmetal
Ibtbt
Lg(1-β)Cc
Sub
LgCsub
LgCQs
Source
(c)

Figure 2.


Metal Gate
S
Intrinsic CNT
D
μ_s
μ_d'
μ_s'
μ_d
E_c
E_V
Chemical potential difference
across the channel
Substrate

(a)


$V_{ch,GS}$
V_{FB}
C_{ox}
$V_{ch,S'S}$
$(1-\beta)C_c$
βC_c
$V_{ch,D'S}$
$\frac{\Delta\Phi_B}{e}$
C_{sub}
E_c
E_v
$V_{ch,BS}$

(b)

Figure 3.

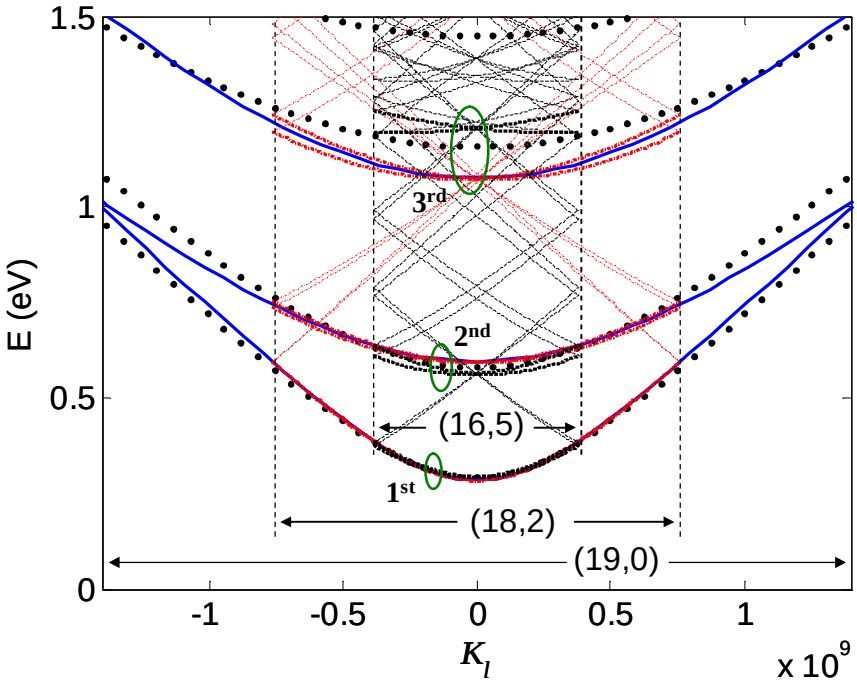


Figure 4.

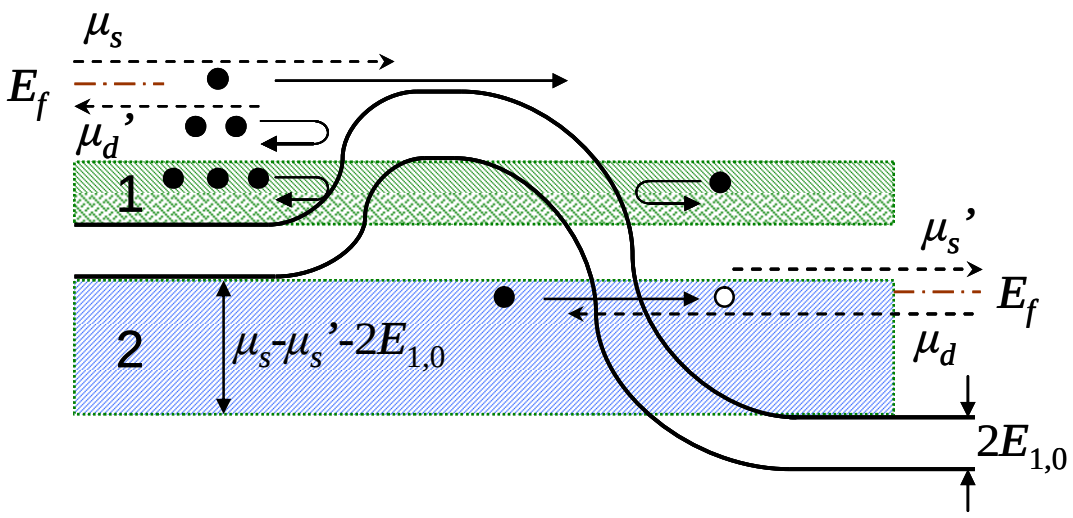


Figure 5.

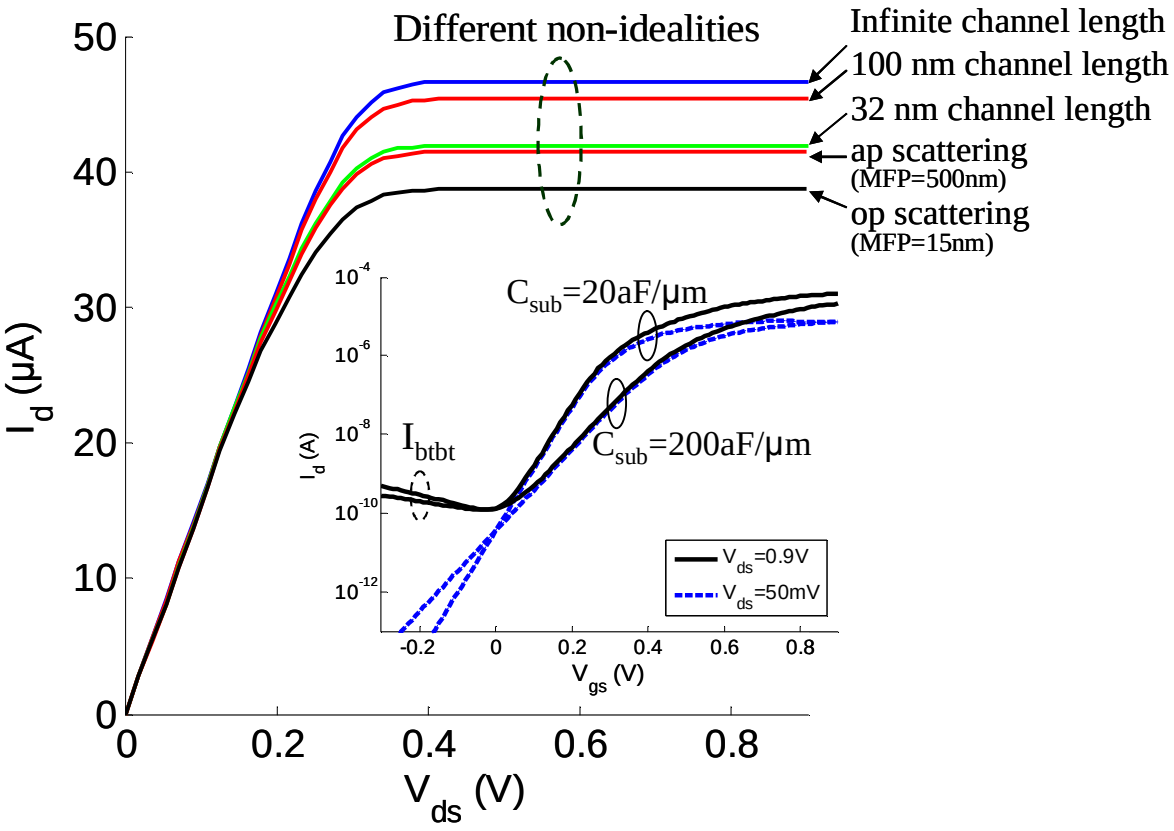

Different non-idealities
Infinite channel length
100 nm channel length
32 nm channel length
ap scattering
(MFP=500nm)
op scattering
(MFP=15nm)
I_d (μA)
V_{ds} (V)
C_{sub}=20aF/μm
C_{sub}=200aF/μm
I_{btbt}
I_d (A)
V_{gs} (V)
V_{ds}=0.9V
V_{ds}=50mV

Figure 6.

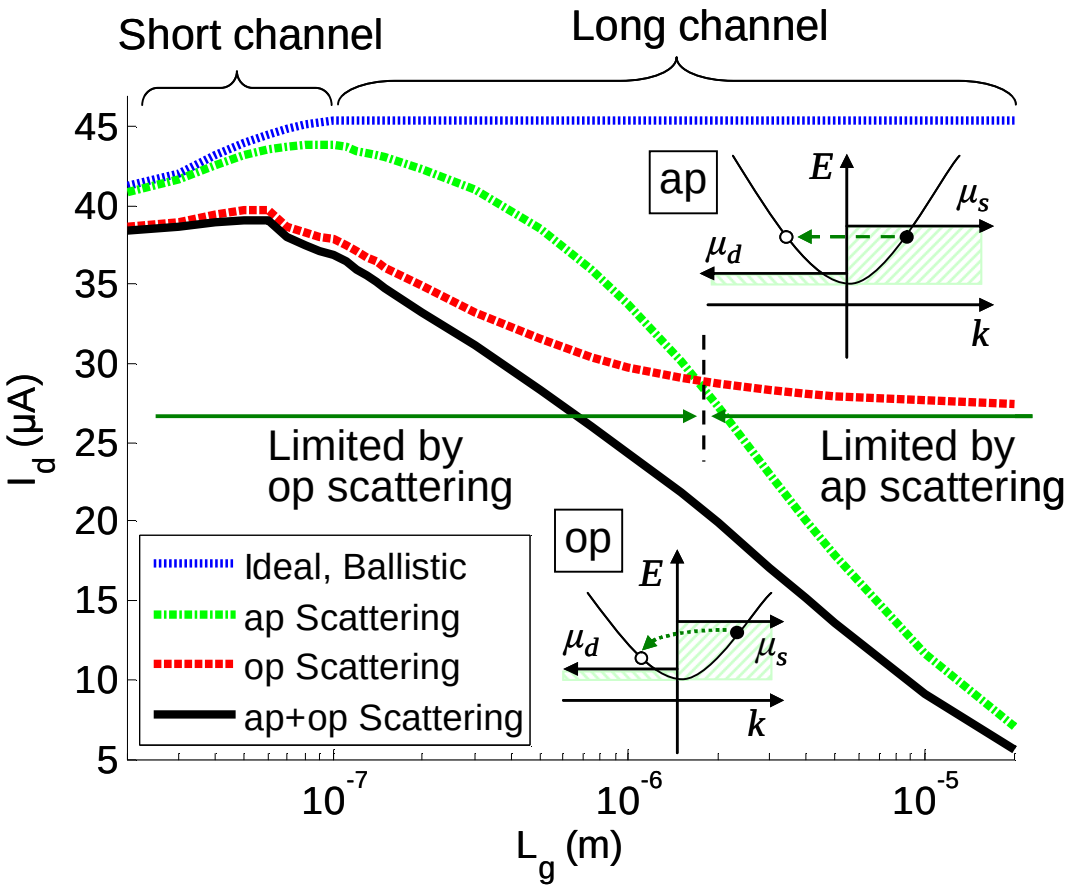

Short channel
Long channel
45
40
35
30
25
20
15
10
5
I_d (μA)
10^{-7}
10^{-6}
10^{-5}
L_g (m)
Limited by
op scattering
Limited by
ap scattering
Ideal, Ballistic
ap Scattering
op Scattering
ap+op Scattering
ap
op
E
k
μ_s
μ_d

Figure 7.

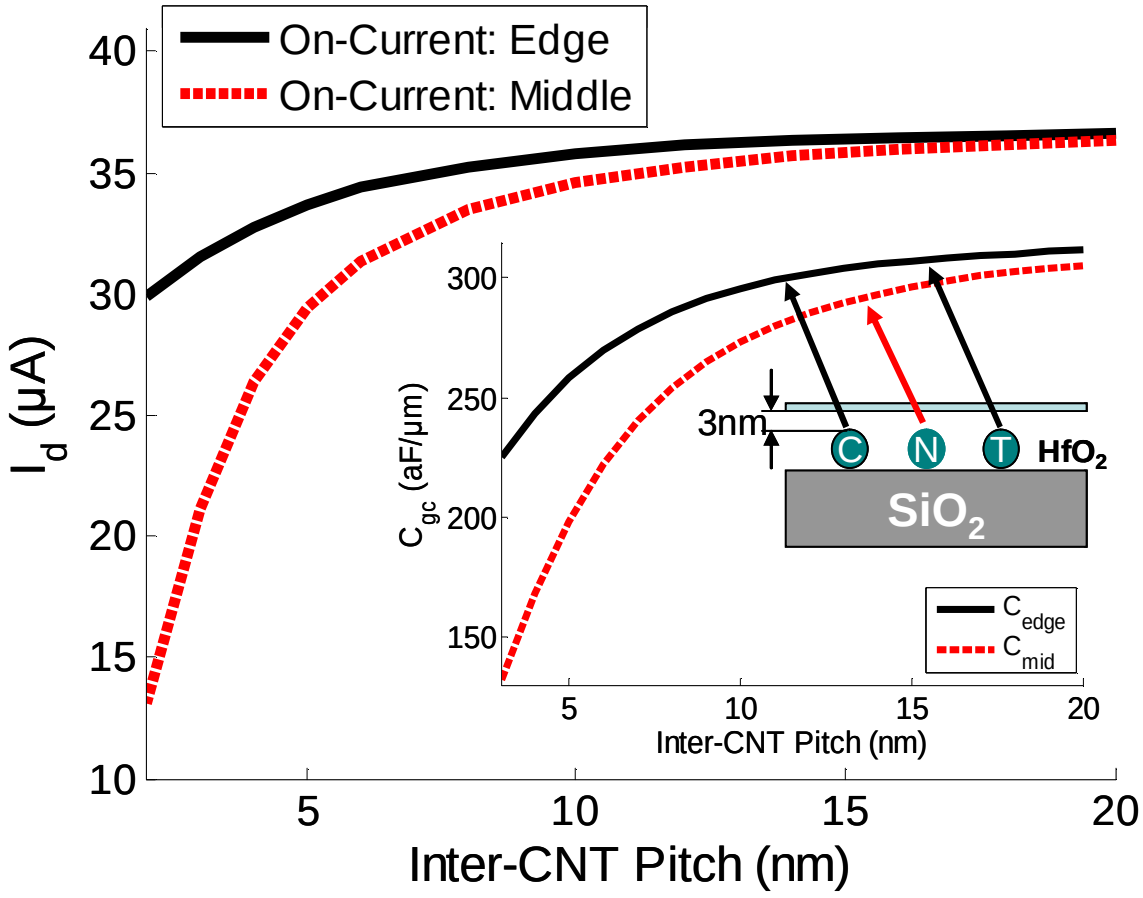
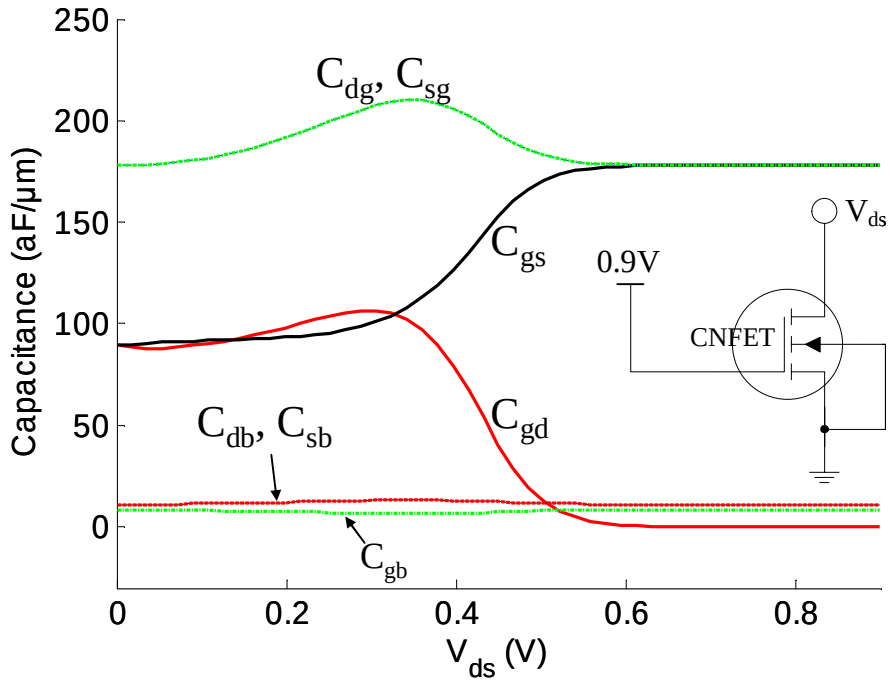
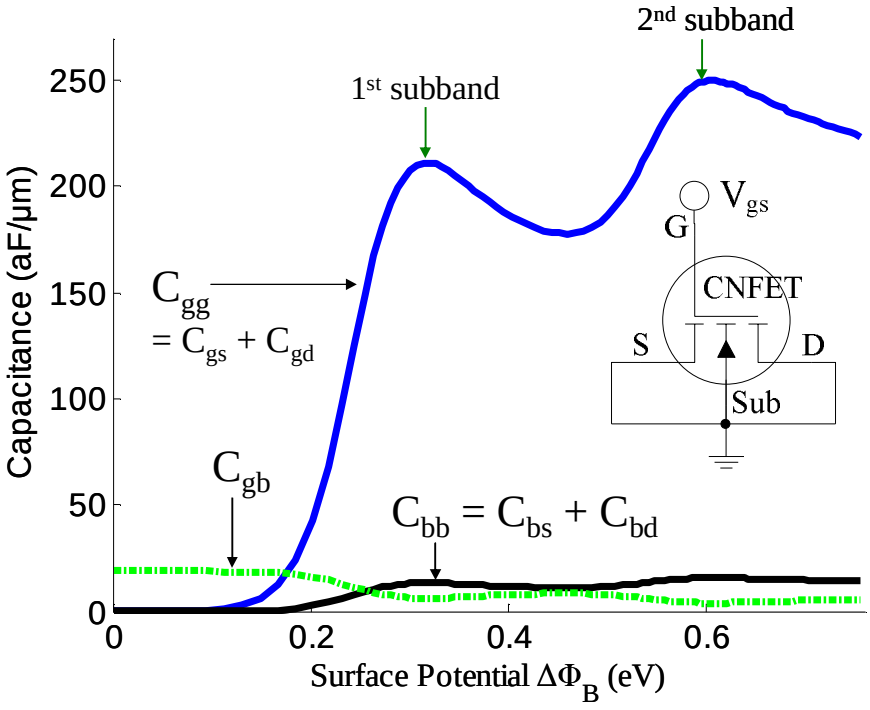

On-Current: Edge
On-Current: Middle
I_d (μA)
Inter-CNT Pitch (nm)
C_{gc} (aF/μm)
3nm
C
N
T
HfO_2
SiO_2
C_{edge}
C_{mid}

Figure 8.


250
200
150
100
50
0
Capacitance (aF/μm)
0
0.2
0.4
0.6
0.8
V_ds (V)
C_dg, C_sg
C_gs
C_gd
C_db, C_sb
C_gb
0.9V
V_ds
CNFET

(a)


250
200
150
100
50
0
Capacitance (aF/μm)
0
0.2
0.4
0.6
Surface Potential ΔΦ_B (eV)
2nd subband
1st subband
C_gg
= C_gs + C_gd
C_gb
C_bb = C_bs + C_bd
V_gs
G
CNFET
S
D
Sub

(b)

Figure 9.