PART 1: Multiple Choice

Select the single most appropriate response for each question.
Note that none of the above MAY be a VALID ANSWER.

(Solution at end)

(1) A possible consequence of *insufficient* timing margin is:
- (A) sensitivity to relative humidity
- (B) sensitivity to operating temperature
- (C) sensitivity to switching noise
- (D) all of the above
- (E) none of the above

(2) An application where internal port pin *pull-ups* would be useful is:
- (A) sourcing current to an LED
- (B) sinking current from an LED
- (C) driving a CMOS load
- (D) inputting a switch contact closure to ground
- (E) none of the above

(3) Interrupt servicing latency is defined as:
- (A) the time it takes to execute an interrupt service routine
- (B) the time it takes to get to an interrupt service routine once the interrupt request is recognized
- (C) the time it takes to fetch the first instruction of the interrupt service routine once the interrupt request is asserted
- (D) the time it takes to clear the device flag once the interrupt request is asserted
- (E) none of the above

(4) The difference between “special” and “normal” HC(S)12 operating modes is:
- (A) the processor feels better about itself when operating in “special” mode
- (B) certain registers can be changed only once in “normal” mode, but can be changed any number of times in “special” mode
- (C) certain registers can only be modified when the processor is running in “special” mode
- (D) certain registers can be changed only once in “special” mode, but can be changed any number of times in “normal” mode
- (E) none of the above

(5) If memory mapping conflicts occur, the HC(S)12 gives the *lowest* priority to:
- (A) register space
- (B) internal SRAM
- (C) byte-erasable EEPROM
- (D) flash EEPROM
- (E) external memory

(6) On the 9S12C, if an XIRQ request interrupts an IRQ service routine that is in progress, it is referred to as:
(A) presumption
(B) recursion
(C) preemption
(D) election
(E) none of the above

(7) The following step is *not* performed when the 9S12C switches context to an IRQ ISR:
(A) setting the "I" bit of the CCR
(B) setting the "X" bit of the CCR
(C) pushing all of the CPU registers onto the stack
(D) loading the interrupt vector into the program counter
(E) none of the above

(8) The purpose of a Digital Binky™ (interrupt enable/masking capability) is:
(A) to prevent a pending interrupt from causing a hardware interrupt
(B) to prevent preemption of an interrupt that is currently being serviced
(C) to prevent interrupt recursion
(D) to prevent an interrupt from vectoring
(E) none of the above

(9) The word "multiplexed", when used to describe an expanded microprocessor bus, means:
(A) address and data are sent over the same wires simultaneously
(B) address and data are sent over the same wires, but not at the same time
(C) address and data are sent over the same wires bi-directionally
(D) address and data are sent over separate wires, but not at the same time
(E) none of the above

(10) In the read timing cycle discussed in class, the "Green Line" refers to the instant that the data "absolutely, positively has to be there", which is:
(A) the read setup time prior to the end of the bus cycle
(B) the bus cycle length minus the address generation delay
(C) the bus cycle length minus the data generation delay
(D) the read hold time prior to the end of the bus cycle
(E) none of the above

(11) If the value on the data bus changes *before* the "Green Line":
(A) bus fighting might occur
(B) the wrong value might be read by the processor
(C) metastability might occur
(D) all of the above
(E) none of the above

Questions 12-20 refer to the timing chart on the page that follows.

(12) The address generation delay (**t_{AD}**) is:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(13) The amount of read setup time available (**t_{RS}**) is:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(14) The write data float delay (**t_{WZ}**) is:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(15) The nominal chip enable access time (**t_{CE}**) available is:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(16) The nominal output enable access time (**t_{OE}**) available is:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(17) If an SRAM with t_{AA} = 30 ns, t_{CE} = 30 ns, t_{OE} = 10 ns, and t_{OH} = 10 ns (referenced from the negation of OE) is interfaced to the processor depicted in this timing chart, the read timing margin provided will be:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(18) If an SRAM with t_{AW} = 30 ns, t_{CW} = 30 ns, t_{IS} = 20 ns, and t_{IH} = 0 ns is interfaced to the processor depicted in this timing chart, the write timing margin provided will be:

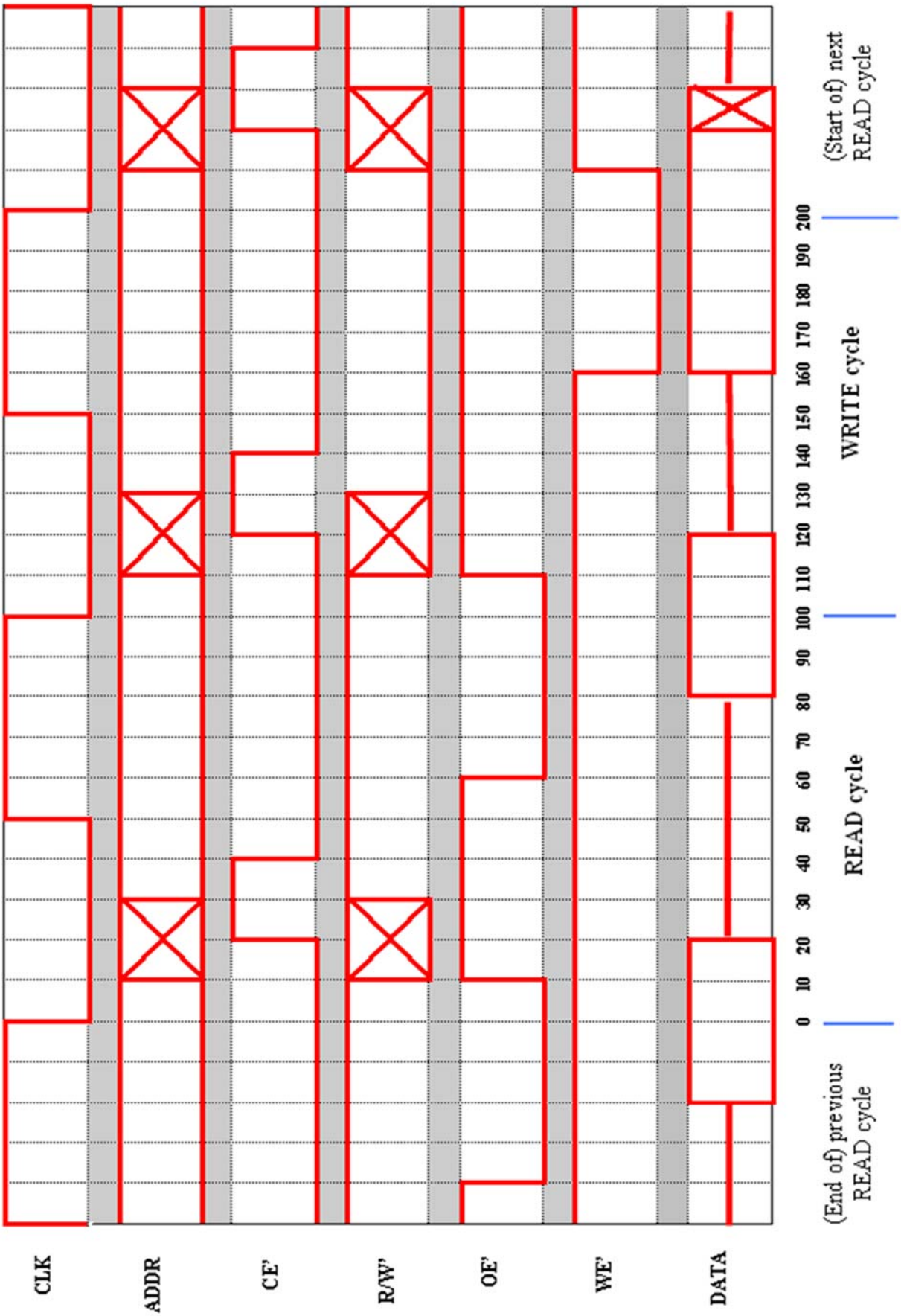
(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(19) The maximum amount of output float delay t_{OZ} (referenced from the *end of* t_{OH}*)* that can be tolerated is:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of the above

(20) If the maximum t_{OZ} (determined in Problem 19, above) is *exceeded* by a ***small*** *amount* (e.g., less than 10%), the ***most likely*** result will be:
(A) higher power dissipation/heat generation
(B) slower bus cycles
(C) burned out port pin drivers
(D) incorrect data read
(E) none of the above

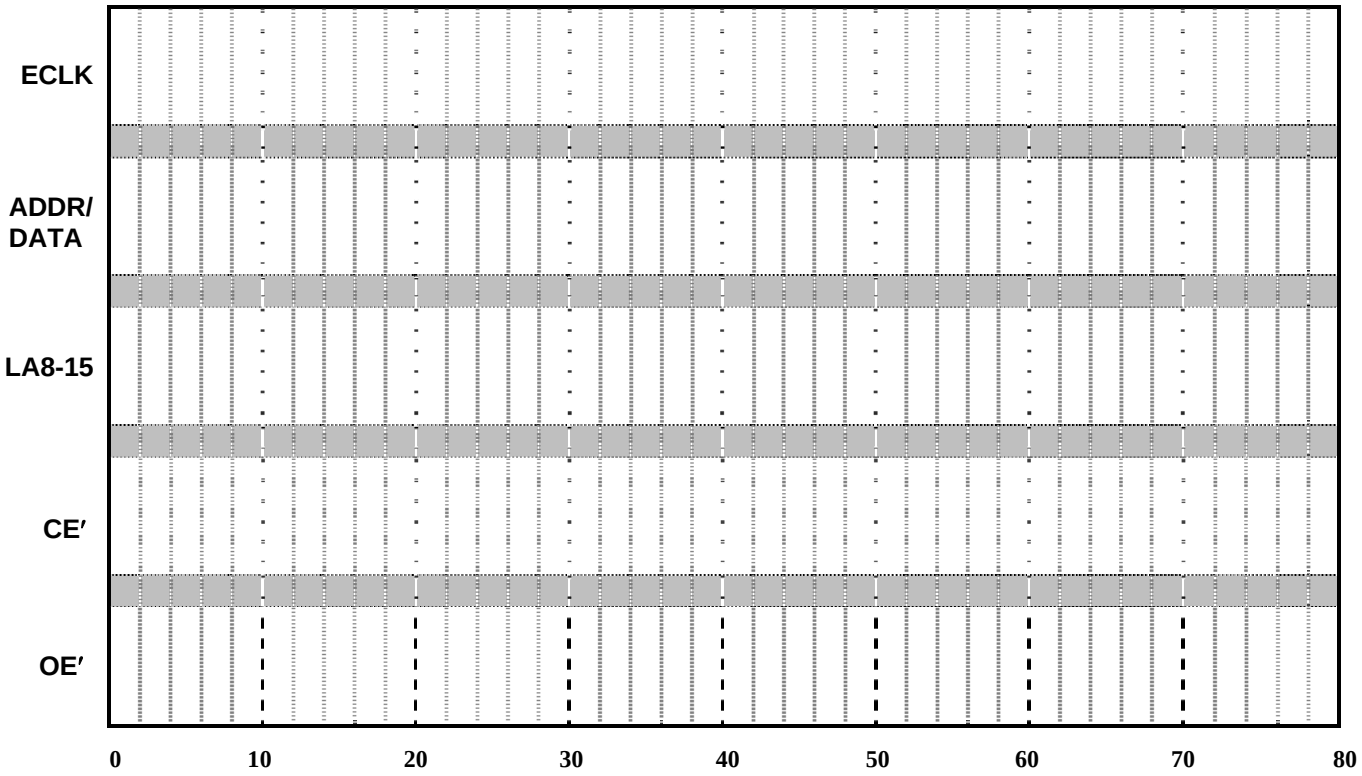
Bus Timing Analysis Reference Sheet for Questions 12-20



Part 2: Design/Application Problem

Determine the ***maximum clock speed*** a **9S12C128** CPU (5 V) can run at in ***expanded narrow mode*** **without stretch** if a **7C199-10** SRAM is used in conjunction with an **LC4032B-25T44C** PLD to implement the "glue" logic (round your result to the nearest one-tenth MHz). Note that your determination should include an SRAM **read timing margin of 10%.** Show your calculations, and ***draw a detailed, to-scale read timing diagram*** documenting your results in the space provided below (**note: horizontal scale is 2.0 ns/division**).

The ABEL file is the same one used for the homework. Use **ispLever** to perform a timing analysis of the critical read cycle paths.



Grading breakdown:

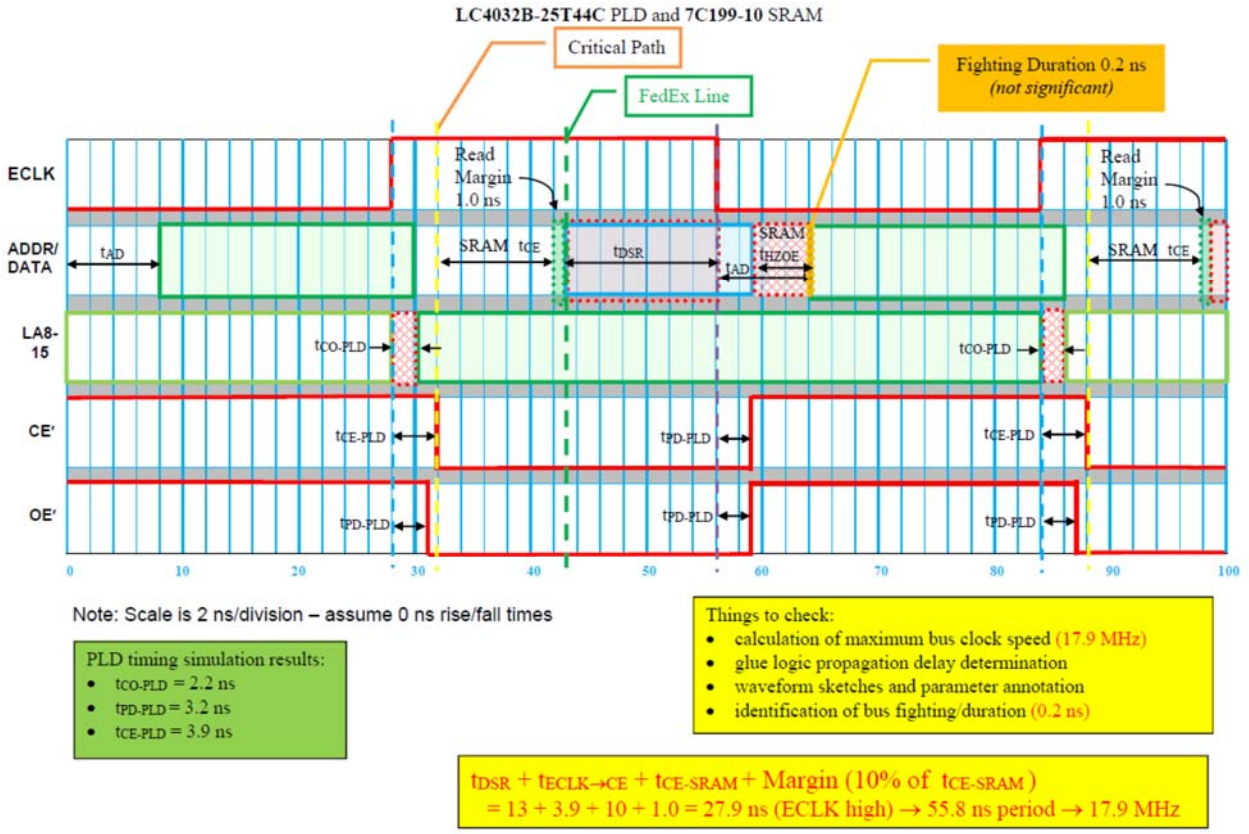
- detailed timing chart, annotated with all pertinent timing parameters
- maximum ECLK speed = _____ MHz (rounded to nearest *one-tenth* – show work)

- timing simulation, ECLK rise to CE′ assertion for PLD specified = ____ ns
- timing simulation, ECLK assertion to OE′ assertion for PLD specified = ____ ns
- duration of potential bus fighting due to SRAM float delay = ____ ns

Part 1 solution key:

1-B, 2-D, 3-C, 4-B, 5-E, 6-C, 7-B, 8-A, 9-B, 10-A, 11-E, 12-C, 13-B, 14-A, 15-D, 16-B, 17-A, 18-C, 19-D, 20-A

Part 2 solution: <same as Problem #4 on Homework #3>



Note: Scale is 2 ns/division – assume 0 ns rise/fall times

PLD timing simulation results:
- $t_{CO\text{-}PLD}$ = 2.2 ns
- $t_{PD\text{-}PLD}$ = 3.2 ns
- $t_{CE\text{-}PLD}$ = 3.9 ns

Things to check:
- calculation of maximum bus clock speed (17.9 MHz)
- glue logic propagation delay determination
- waveform sketches and parameter annotation
- identification of bus fighting/duration (0.2 ns)

$t_{DSR} + t_{ECLK \rightarrow CE} + t_{CE\text{-}SRAM}$ + Margin (10% of $t_{CE\text{-}SRAM}$)
= 13 + 3.9 + 10 + 1.0 = 27.9 ns (ECLK high) → 55.8 ns period → 17.9 MHz