Multi-Cycle Processor

Group Members:
Avi Tanwar, 2019A8PS0332P
Ishan Garg, 2019A7PS0034P
Jagrit Lodha, 2019A3PS0165P

Instruction Type	IF Phase	ID Phase	EX Phase	MEM Phase	WB Phase
Addition (Register)	complete	complete	complete	complete	N.A.
Addition (Immediate)	complete	complete	complete	complete	N.A.
Subtraction (Register)	complete	complete	complete	complete	N.A.
Subtraction (Immediate)	complete	complete	complete	complete	N.A.
Shift Logical Left	complete	complete	complete	complete	N.A.
Shift Logical Right	complete	complete	complete	complete	N.A.
Shift Arithmetic Right	complete	complete	complete	complete	N.A.
Load Word	complete	complete	complete	complete	complete
Store Word	complete	complete	complete	complete	N.A.
Jump	complete	complete	complete	N.A.	N.A.
Branch Equal	complete	partial	incomplete	N.A.	N.A.
Branch Not Equal	complete	complete	complete	N.A.	N.A.
Logical (Nand)	complete	complete	complete	complete	N.A.
Logical (Nor)	complete	complete	complete	complete	N.A.

Notes:

- We have split the Memory module into 2 modules: Instruction Memory (IM), and Data Memory (DM), because we were facing difficulty in choosing the data file from which to read based on the control passed. For some reason, the control was not firing inside the module.
- We were facing weird delays in displaying outputs in the testbench. For our 1st test case, the output is printed 4 times, either with don't care values in the registers, or with correct

values. But it is getting repeated 4 times, when it should only be displayed once. So as a temporary corrective measure, we have put 3 dummy test cases on top of our actual test cases, and labeled them as “DUMMY”. This is just to get our outputs in order. **Our actual output starts from the 4th test case.**