CS 2204 DIGITAL LOGIC & STATE MACHINE DESIGN FALL 2019

GENERAL
CS2204 LAB & ENGINEERING FUNDAMENTALS

1. Introduction

CS 2204 covers theory, design analysis of digital circuits. The CS 2204 lab helps students achieve the intellectual, technical and non-technical goals mentioned in the Syllabus. In addition, the lab supports lectures and introduces practical aspects of digital logic, such as current design and analysis techniques and tools as well as engineering environment fundamentals. Hence, students

(i) Develop a term project that reinforces concepts introduced in class, and

(ii) Experience the digital design engineering environment and acquire the skill for it by emulating the environment where the professor, TAs and students are the project manager, senior engineers and junior engineers, respectively.

The lab emphasizes the design more than analysis by focusing on a semester-long term project. The reason is that it is harder to design than analyze. One has to practice design considerably in order to master it. The CS 2204 lab helps students practice design throughout the semester ! Students' lab performance affects the term grade directly and also indirectly since each exam has questions on topics covered in the lab.

This handout presents points important for the CS 2204 lab. The points are also important after this semester is over and ***after graduation***. Specific topics covered in this handout are the lab structure and engineering environment fundamentals. Students need to bring this handout to the lab and refer to it as often as they can.

2. Digital Design Today

Today's digital design engineering environment is a fast-paced and very dynamic environment. In order to be ready for this pressure-filled work place, college students need to learn and follow the technical and non-technical practices of the engineering environment. The lectures and especially the lab are designed to introduce them. They are described briefly in this handout and will be discussed throughout the semester. Note that these digital circuit (digital hardware) engineering fundamentals are similar to software engineering and analog hardware engineering fundamentals and so can be used for those environments as well.

Today, digital hardware engineers develop products that are one of the three below :

- A chip
- A printed circuit board (PCB)
  - Chips cannot be used by themselves. New chips developed must be on a new PCB eventually !
- A circuit as an intellectual property (IP) whose description is contained by a set of computer files.

Engineers use product goals to make decisions during the design. The goals include :

- Design goals (factors) that include include :
  - Speed, cost, size, power consumption, weight, reliability, upgradibility of the chip/PCB.
    - It is not easy to satisfy the goals at the same time ! For example, increasing the speed will increase the cost and power consumption !
- The input/output relationship, i.e. the operation or purpose of the product
- Technolgy used for the product, i.e., electrical properties of the product

3. Lab Hardware and Software :

The CS 2204 lab is 227RH. The lab hardware is the **Digilent** NEXYS-4 DDR field programmable gate array (**FPGA**) prototyping board. The FPGA chip on the board is the Xilinx Artix-7 chip. An FPGA chip is a **hardware programmable** chip. It emulates the circuit designed. FPGA chips are used to test the design when a **new chip** is developed as well as in final products. For example, they are used to machine learning applications. Also, FPGA chips are on Mars rovers !

The Xilinx Artix-7 FPGA chip contains configurable (programmable) logic blocks (CLBs) and programmable connections. The Artix-7 we will use has 7925 CLBs organized as a 2-dimensional array on the chip. The FPGA chip also contains 4860Kbit RAM, and other hardware structures. The Digilent URL is **http://www.digilentinc.com.** The Xilinx URL is **http://www.xilinx.com**.

The lab software is Xilinx Vivado 2018.3 computer aided design (CAD) software tool and Digilent ADEPT tool. The Xilinx tool will be used to develop projects, i.e. we design and test our projects on computers. This tool includes **schematic** and *Hardware Description Language* (HDL) design editors and logic and timing simulators. The Digilent tool has FPGA interfaces and downloaders (programmers). It will be used to program the FPGA chip. The CS 2204 design will be a HDL design. We will use Verilog which is a HDL language. VHDL which is the other popular HDL will be discussed from time to time.

- The lab PCs are installed the full version Xilinx Vivado 2018.3 CAD tool which requires a license. It can be used only if students login to the LABS domain in the lab. The LABS domain also provides students with another software tool, the Digilent ADEPT tool to program the FPGA chip and a special storage area which is called the "S drive." Students can login to the LABS domain only if they enroll in CS 2204. To access the S drive students need to have (i) a LABS domain account and (ii) an S drive access right. The S drive is a networked drive accessable out of the lab.

- Students will install a smaller version of the Xilinx software called WebPACK Vivado 2018.3 whose license is free. WebPACK is sufficient for students to develop the term project. They can also install the Digilent ADEPT on their laptops as it does not require a license. If students do not own the Digilent FPGA board, they do not need to install the Digilent software on their laptops.

- Students will be asked to work on projects both in the lab and out of the lab as they will have the Xilinx tool on their laptops. They need to keep their projects organized on their laptops : Projects are built on earlier projects. If not organized well, students may waste time to locate them or to redesign the same circuits from scratch. Students are suggested that on their laptops, they have a CS2204 folder. In this folder they create a folder for each lab or phase.

- Students are suggested that they use the PCs when they are in the lab since they will work with their partners and share the FPGA boards. Thus, they will use the S drive in the lab which means they need to keep their projects organized on the S drive as well. However, students need to make sure that their laptops and the S drive are synchronized all the time. They have to make sure that the S drive is up to date before arriving to the lab and the laptop is up to date after leaving the lab for continuous efficient work this semester. Copying the project from one storage area to the other means that the folder containing the project is copied and pasted.

- When students get in to the lab, they login to the LABS domain and start the Xilinx software whose icon is named "**Vivado 2018.3**." Students make sure they can access the S drive on the PC they are using and it is up to date.

- Students should avoid touching the FPGA board except only those parts that are **not sensitive to static electricity**, such as switches and pushbuttons. Touching the FPGA should be avoided in order not to damage it.

- Students are suggested that they download necessary pages from Xilinx, Digilent, the Wakerly textbook and Texas Instruments web sites and keep them handy. Students can print certain pages that are frequently used.

4. Lab Work :

There are three (3) phases to learn about the lab hardware and software and to complete the projects. All three phases will be graded and used to determine the lab grade.

- The lab performance of students will affect the term grade : 15% of the term grade will be based on student's work in the lab that includes quizzes, exercises and the final project.
    - Students must be present and working on the assigned topics with their teammates **well** in the lab.
    - Students must work well on the homework with their teammates as well.
        - Attending the lab session and being on time are required. Attendance is recorded in every lab session.
            - Students arriving late would have difficulty in adjusting to the lab session, delaying team's work.
    - Project grades are based on the corresponding Check List handout to be distributed in the lab.
        - Students' each lab work will determine their term grade.
        - A student who has fallen behind, i.e. not attending the lectures and not doing the homework and project, cannot develop the term project. When it is week 11, 12 or 13, you may realize it and it will be too late!
    - The lab performance affects the term grade **more** : Exams include the labs, i.e. circuits and concepts studied in the lab. In addition, a student working well in the lab solves problems faster during exams
- Each lab session starts with taking attendance. Teammates "synchronize" with each other and the professor answers questions from the teams. Then, the professor gives a presentation to discuss important points of the lab session. Afterwards, teams continue with the lab work under TAs' supervision.
- Students must be motivated for the lab (timely arrival to the lab session, session long presence in the lab, attention to the work), concentrate on the experiments (focusing on the design), and work well with teammates. During the lab session, students are required that they not be distractive, not talk with others except with their partners only if necessary and not loudly and not go out and come back frequently.
    - Students can have food and drinks in the lab, but they have to be careful not to spill on the board.
        - Students can leave the lab to get food or a drink, provided that it is short and teammates accept it. Students must keep the project due date in mind and make sure they are on schedule to complete it. The project due date will not be postponed for a team.
- When the lab is over, students need to log off and turn off both the monitor and the FPGA board.
- The lab will be available to students to work on experiments when a lab session is **not** scheduled. A TA will be present in the lab.
    - We will call these hours Open Lab Hours. They will be announced soon.

5. Team Work :

Team-based design is an unquestionable necessity in digital engineering environment today. Members of a team think on a problem simultaneously, arriving at an acceptable solution faster. Although it may seem simple to do team work, it is not the case. The success of the team depends on the members' ability to *cooperate*. Hence, college students need to learn basics of team work. Team work in CS 2204 targets practicing simultaneous cooperative work on a problem by a number of students to arrive at an acceptable solution fast.

- The lab projects and the homework will be done by 3- or 4-student teams. Students will choose their partners from their own lab section. In order to ensure effective cooperation, as soon as a team is formed, members of the team need to exchange their contact information : Telephone numbers, email addresses, their semester schedule, (class and work schedule), etc. to determine their weekly meeting times.

- Students will submit homework and lab projects as a team : Just one per team. This requires coordination ! So, students have to be in touch with their partners all the time. Thus, team members must carry each other's complete contact information with them all the time.

    - A student who misses a lab session will discuss with his/her lab partner(s) as to how to try to catch up. Based on partners' suggestions, the student can do the work in the CS 2204 lab during Open Lab hours.

- Note that **every student has to work as if he/she has no partner**. First, the exams will have lab related questions. Second, a partner might withdraw from the course and the smaller team would be doing the homework and the lab project. Finally, these should not be any concern since the homework and lab experiments are designed so that they can be done by a single student, **provided that the student has not fallen behind**.

6. Engineering Environment Fundamentals :

Today's digital engineering environment requires constant learning and adaptation. The environment is also team-based and global. Thus, engineers must (i) know how to learn fast, (ii) know how to interact with people well and (iii) have a solid technical foundation. The environment can be stressful even for experienced engineers. Thus, it is important for students to be ready for it before they graduate. The CS 2204 lab is a good medium to prepare for it. It is designed to help students learn about the environment. Students need to take the advantage of this opportunity !

In today's globalized engineering environment with tight deadlines and tight budgets, managers/employers want their engineers to be the following :

- Being **systems oriented** ! Even on a global scale ! They want you to know not only the part (block) of the system you work on, but also the other parts. So, you know how the whole system (black box) works and how the pieces relate to each other. This requires that you interact well with your partners who describe their blocks to you as well as you describe your block to them so that everyone is systems oriented. The employer does **not** want to hear "My job is only this part (block) ! I don't know about the rest !"

- Being **problem solvers** ! Even on a global scale ! When there is a problem to be solved, the employer wants to hear from you "No problem ! I can solve it !" They do **not** want to hear "I don't know about it ! I never learned it ! I cannot do it !"

These two properties become more important when there is an economic recession that causes staff reductions. The remaining staff has to do more work as there are less people at the company !

On the non-technical side, students need to realize that the following are important points for engineers :

- Technical performance and skills are **not** everything.
- One should **not** take anything that is **not** earned : Someone else's intellectual property (IP).
    - But, it does not mean one has to be on a one-person crusade. First, we are not machines. Second, we all need each other.
- Help others (colleagues) before asking for help.
    - No one can survive alone. One should not ignore people around.
- Find the balance !

Non-technical skill means : One knows what to do how, where and when in the work place. For senior engineers it also means to be able to speak well and to be patient, a good listener, inspirational, motivational, and firm but fair.

- A **smile** can unlock many doors !

CS 2204 is designed to help students be system oriented problem solvers. It is also designed to help students understand the above engineering environment dynamics : Both technical and **non-technical**, the latter of which is sometimes more important than the first. The professor expects students treat the course as a cultivating ground of preparation for engineering life : The lab is the place engineering environment basics are learned and improved upon :

- Team-oriented labs and homework,
- Rules and conventions in the lab and classroom to bolster technical and non-technical skills, and
- The professor and TAs are the project manager and senior engineers, supervising students who are junior engineers.

The professor will convey messages to remind students about the engineering environment by giving analogies from the college environment and ask from students to train for the engineering life by practicing college analogies :

- In college, students should not do things that they would not do as engineers. Such as :
    - Arguing with the project manager ?
    - Arguing with team members ?
    - Arriving late at a team meeting ?
    - Delaying the completion of the project part (block) assigned ?

7. Digital Design Trends

Today's digital circuits are very complex, requiring specific techniques and tools. The techniques include :

- **Top-down** design :
    - Block-based, layered, structured design : Simple concepts, blocks and subblocks, are dealt with first, not circuits. Therefore, one starts with the input/output relationship of a block, partitions it into subblocks and continues this process until each (sub)block is simple enough to be implemented by circuits quickly.

- CS2204 top-down design : A project is a black box in the beginning with a specific input/output relationship (operation). It is then partitioned into blocks each of which is partitioned into sub-blocks, subsubblocks, and so on.

- **Team-based** design :
  - Digital hardware is designed in parallel by team members to complete the product in time for mass production : Time-To-Market (**TTM**). The number of team members depends on the complexity of the design.

  - CS 2204 teams : 3- or 4-student teams complete the project by the last lab session of the semester!

- **Core-based** design :
  - Most difficult blocks (IP) are licensed from other companies to save time.
  - CS 2204 core-based design : Students will be given core blocks. They will design the remaining blocks.

Even if the above techniques are utilized (top-down, team-based and core-based design), today's circuits are still too complicated. Thus, one needs powerful tools and devices to further simplify the task of digital design :

- **Computer aided design** (CAD) software tools are used to develop digital circuits on computers. The CAD software abstracts (hides) the details unnecessary at the moment and so speeds up the development phase.

  - CS2204 CAD software : Xilinx Vivado 2018.3 software.

- **Field programmable gate array** (FPGA) prototyping boards are used to test the new chip design physically. FPGAs emulate the new chip, allowing the designers to catch additional errors, not caught during simulations on CAD software..

  - The CS2204 FPGA board : Digilent NEXYS-4 DDR FPGA board to do project designs.

    - CS2204 FPGA : Xilinx Artix-7 XC7A100T-1CSG324C.

- There is a web site that has been set up to help Xilinx university users : **http://www.xilinx.com/univ**.

8. Digital Design Conventions

Industry and digital logic books use the following conventions. Students need to know them :

a. Digital Circuit Drawing Conventions when <u>schematic</u> design is done :

➔ On the lower right corner of the printout (after taping if more than one sheet) information identifying the students that produced the work is shown. That is, the names of team members, "CS 2204" the Lab section and the semester are placed on the **lower right** corner of the printout.

➔ When drawing lines to connect gates/FFs/black boxes, **horizontal** and **vertical** lines are drawn. Note that some CAD software does allow 45^{o} <u>angled</u> wires. But, the Xilinx software does **not** allow such angled wires.

➔ Wires are **not** drawn over blocks, circuits, chips, buffers, pads, labels, etc. Wires are drawn around them horizontally and vertically.

➔ Remember to **beautify** the circuit on the screen after determining that it works. This means components that do similar work form horizontal and vertical lines, line tanglings are minimized and unnecessary wire turns are eliminated.

➔ CS 2204 Students :

➲ Make sure to check the Check List handouts, if provided, as you draw schematics.

b) Logic Circuit Design Conventions :

➔ Following block-based design, circuits for individual blocks are drawn block by block. In order to help the reader, circuits for different blocks are placed with enough distance between them. A block may consist of subblocks in which case each subblock circuit must have enough distance from its neighbor subblocks. Also, a block or subblock should not have its components all over the screen : the components must be close to each other to signal a block or a subblock.

➔ No output can be short circuited to any other output unless the outputs are tri-state outputs. Thus, no totem-pole, gate, flip-flop and chip output can be short circuited with any other output.

➔ If an output is not needed, leave it **unconnected**.

➔ A high-impedance (Hi-Z) output value must be carefully examined to see if it is correct.

➔ CS 2204 students :

➲ Make sure the schematic files are saved.

➲ Perform a **logic simulation** on each (sub)block. If you cannot figure out the cause, do a Xilinx IMPLEMENTATION and follow the error and warning messages in the Implementation Log File.

➲ Make sure that you continuously look at the Check List handouts to remember and follow design conventions and avoid errors.

➲ Important : if students cannot make progress, they are referred to the earlier handouts that are about simpler but similar circuits. Exercises in some of the handouts also give detailed coverage of input/output relationship determination and implementation possibilities. In addition, students should refer to the "*General Design Rules*" handout.

c. Digital Circuit Printing Conventions :

➔ The circuit printout must be readable : characters, labels, gates, FFs, blocks, chips must be readable.

➔ If the circuit is large, a readable printout requires more than one page. In that case :

➲ A one-page printout is not acceptable, unless otherwise indicated,
⇨ All sheets must be attached to each other (such as a scotch tape on **both** sides of the sheets),

⇨ Lines, chips, names must be continuous (requiring cutting sheets along the edges before taping).

➔ CS 2204 students :

➲ If students are asked to identify blocks, they should do so with a color pen, a **green** pen. It is green in order not to cause confusion with the red pen the professor uses. Students should draw a circle (or rectangle) around each block. Students must make sure that they circle each block carefully, without leaving out any circuit that belongs to the block.

➲ If Students are also asked to name the blocks, they should use the same color pen and make sure the name matches the block.

9. Related Web Sites

There are a number of web sites that have projects for FPGA chips. A search on the web will yield such web sites as **fpga4fun**, **fpgaarcade** and **Hamsterworks**, for example.