UNIVERSIDAD POLITÉCNICA
TAIWAN – PARAGUAY
臺灣-巴拉圭科技大學

Digital Logic Design
Laboratory #9

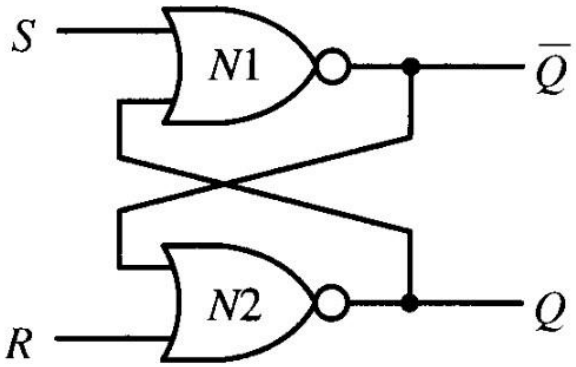
Latches

Activities

Write a vdhl code to implement the circuits with the following functions

a. NOR latch

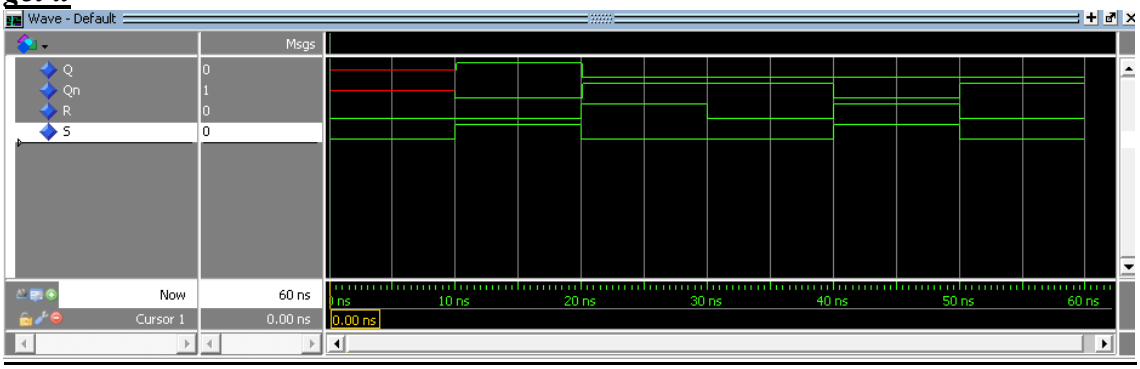
a.1 Copy and compile the entity/architecture



a.2 Explain why error occurs while compiling code.

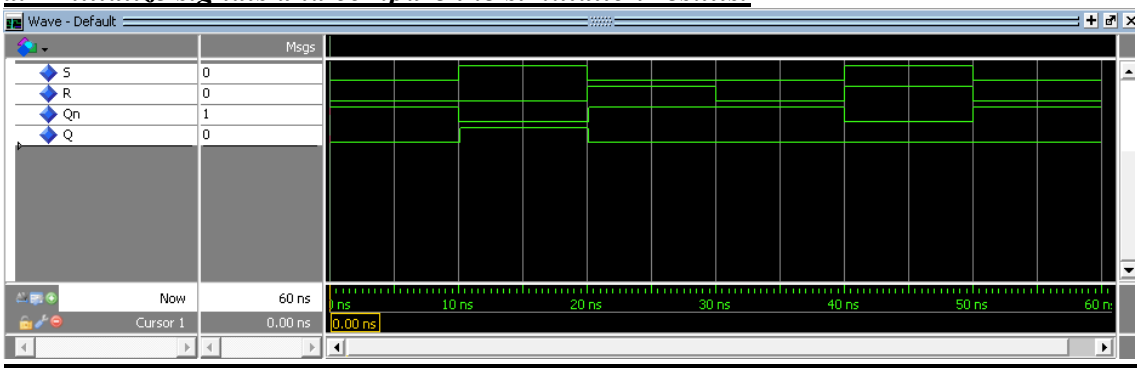
Basically, you can't connect the output of a black box component as an input of the black box without a wire (signal).

a.3 Add intermediate signals and simulate with test bench (`tb_sr_latch_nor.vhd`, available at last page of this guide) Explain the reason why undetermined output is get u



Because when the value is 0,0 it holds the value of Q and Q' and since it is not initialized it is U.

a.4 Initialize signals and compare the simulation results.

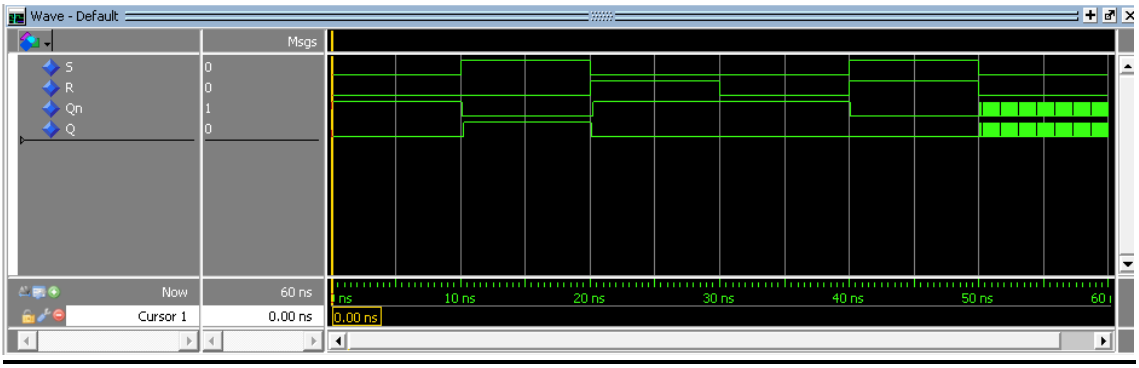


The difference between this result and the previous is that the Q and Q' values are initialized.

a.5 Explain the reason of this error. `# ** Error: (vsim-3601) Iteration limit reached at time 50 ns.`

This error occurs because the assignments are immediate and mutually dependent, creating a feedback loop that the simulator cannot resolve. This loop keeps evaluating indefinitely, causing the simulator to reach its iteration limit without stabilizing.

a.6 Add 0.1ns delay to signal assignment

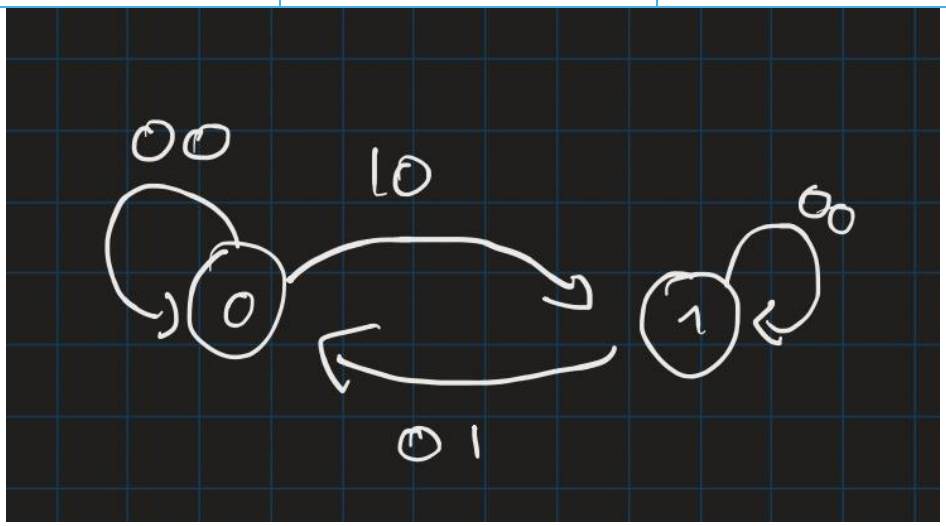


a.7 Analyze output waveform after `50 ns.`

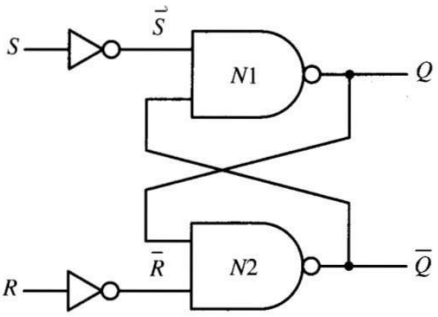
After the 50 ns the tb passes from S=1 and R=1 to S=0 and R=0 and this doesn't stabilize so enters a loop that passes Q and Q' from 1 to 0 and then from 0 to 1 infinitely.

a.8 Draw a state diagram considering only valid inputs.

S	R	Q
0	0	HOLDS
0	1	RESET
1	0	SET
1	1	ILLEGAL

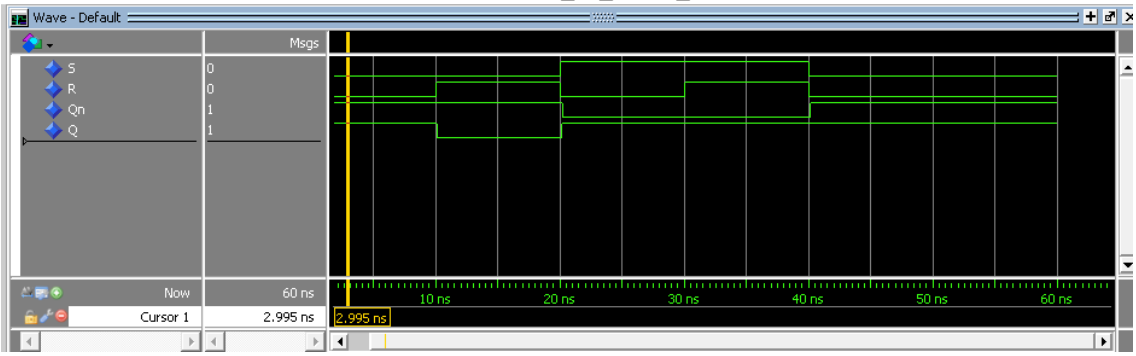


b. NAND latch

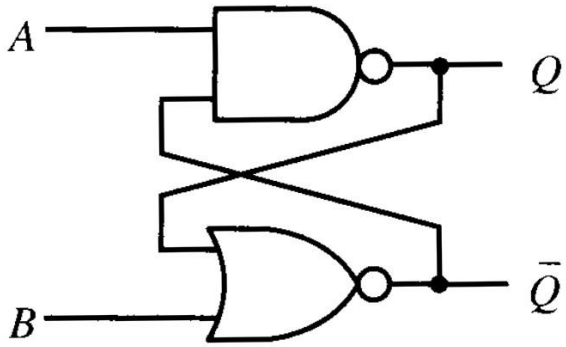


b.1. Design an architecture for the entity:

b.2. Simulate and verify using testbench `tb_sr_latch_rtl.vhd`



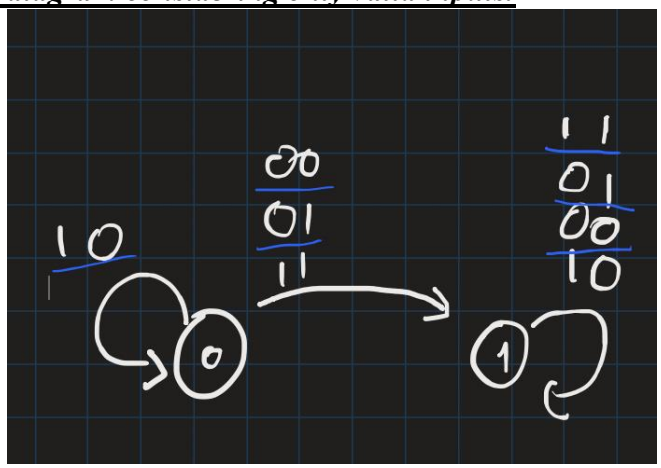
c. Latch circuit



c.1 Write the truth table considering all possible combinational inputs and initial states.

A	B	Q	Q*	function
0	0	0	1	Set
0	0	1	1	Set
0	1	0	1	Set
0	1	1	1	Set
1	0	0	0	Hold
1	0	1	1	Hold
1	1	0	1	Set
1	1	1	1	Set

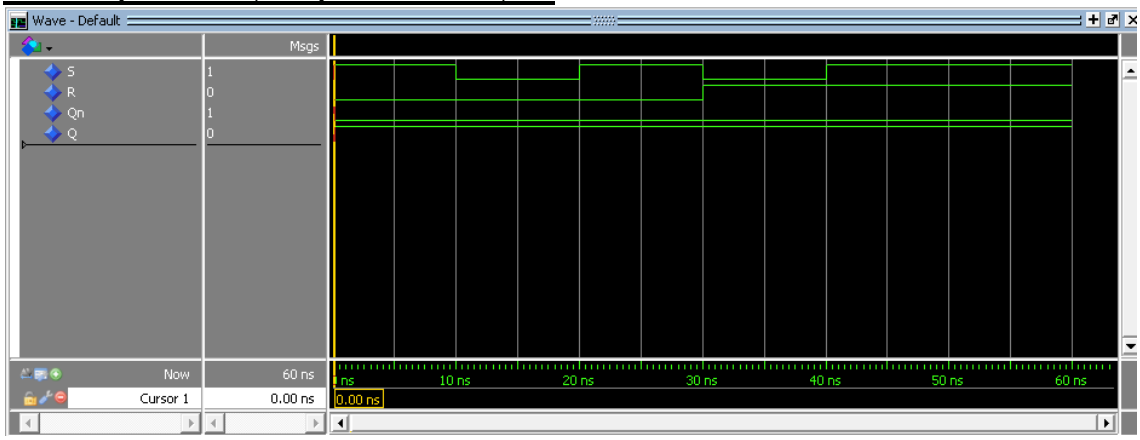
c.2. Draw its state diagram considering only valid inputs.



c.3. Design an entity/architecture for this circuit. Consider 0.1ns delay for nand/nor gates.

c.4. Simulate initializing Q=0 and Q'=1, and using the following stimulus

c.5. Compare with your previous analysis.



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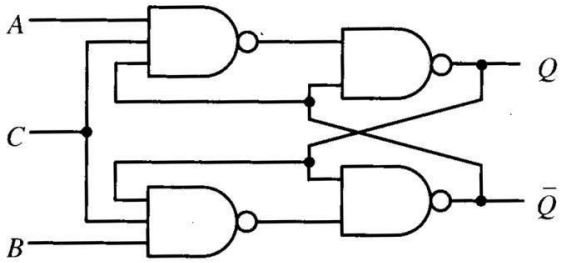

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0	0	1	0	0	Hold
0	0	1	1	1	Hold
0	1	0	0	0	Hold
0	1	0	1	1	Hold
0	1	1	0	0	Hold
0	1	1	1	1	Hold
1	0	0	0	0	Hold
1	0	0	1	1	Hold
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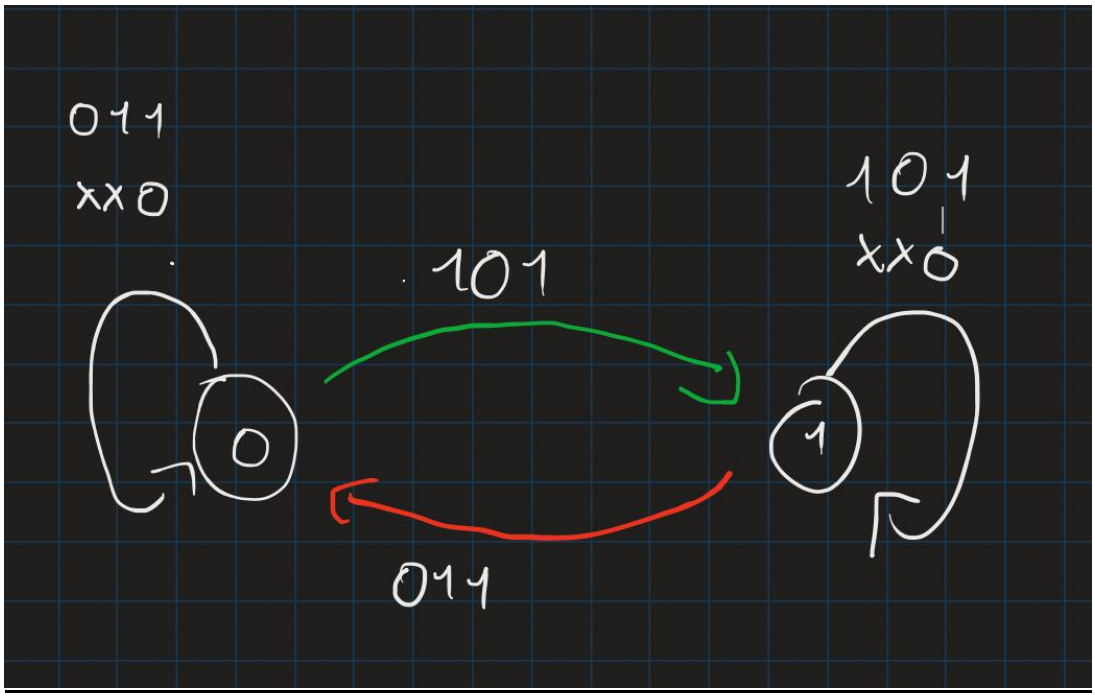

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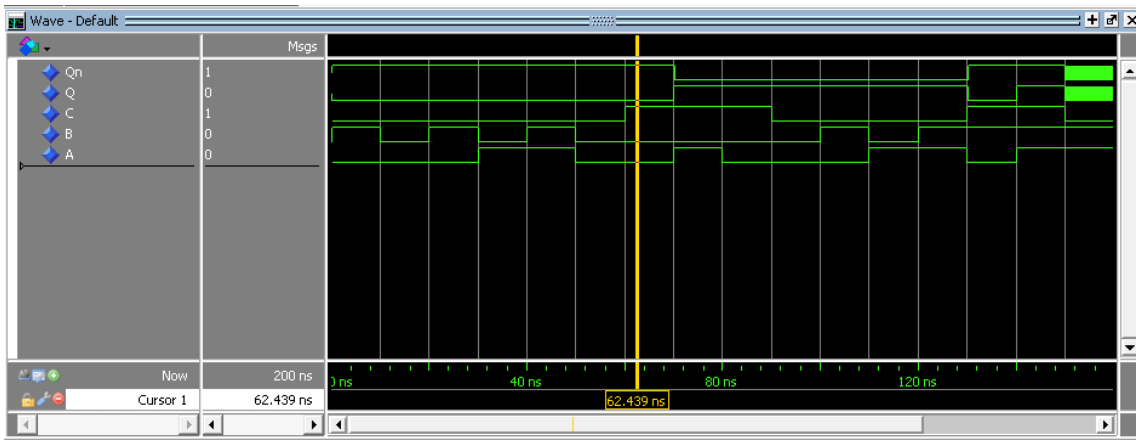

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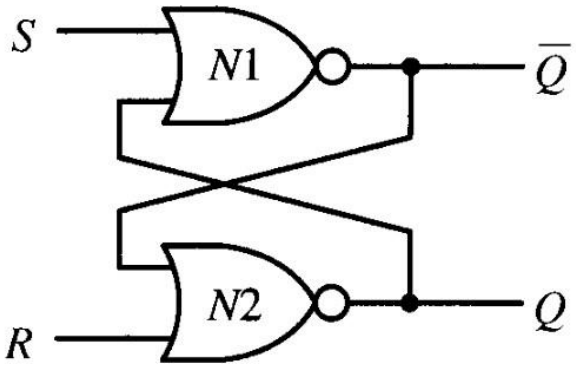

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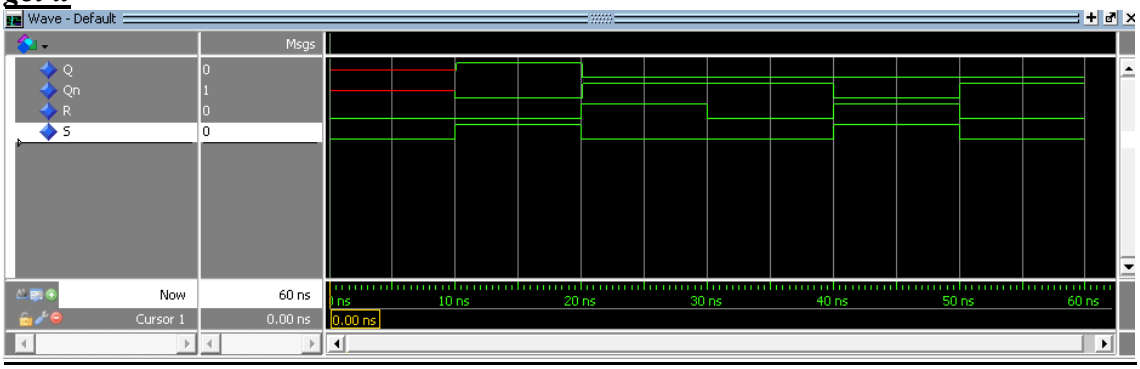

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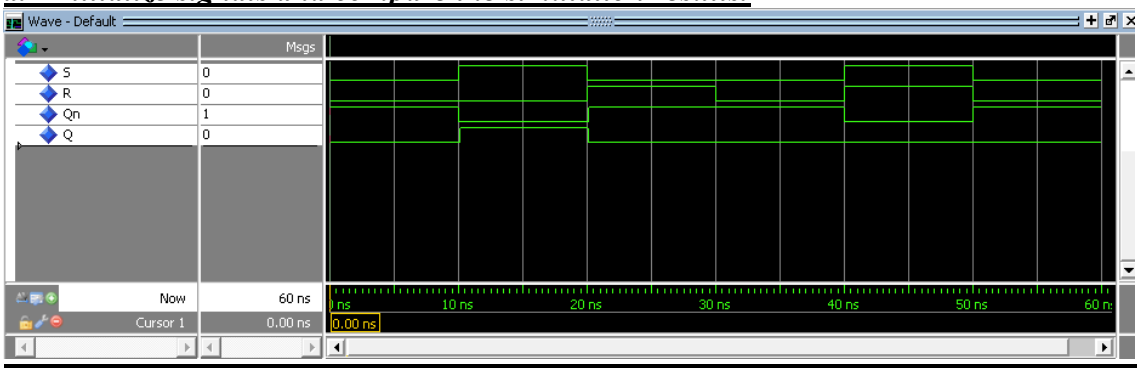

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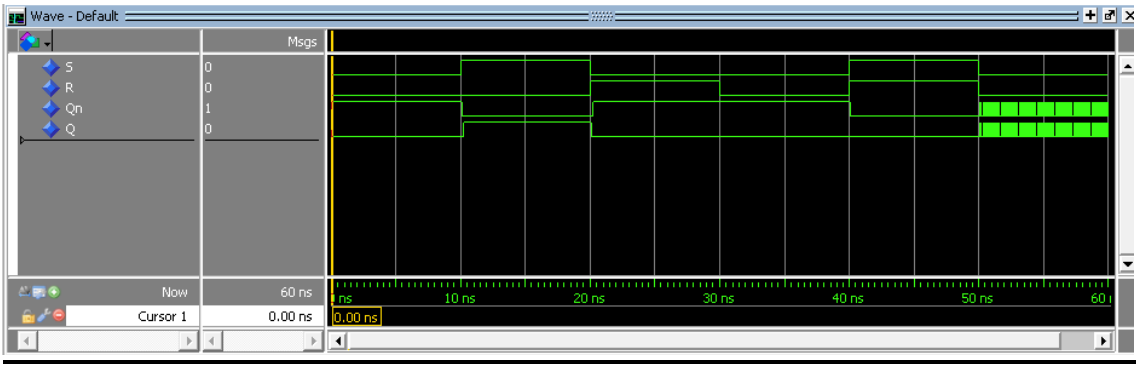

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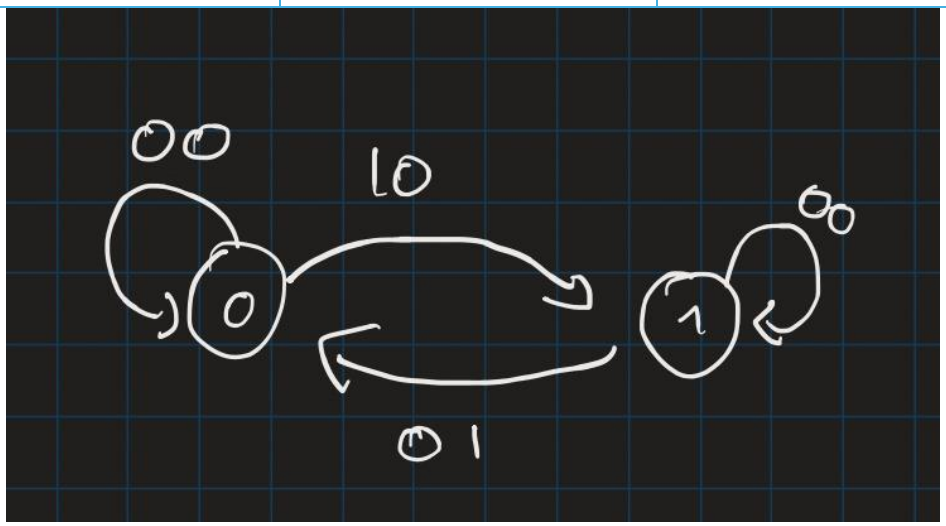

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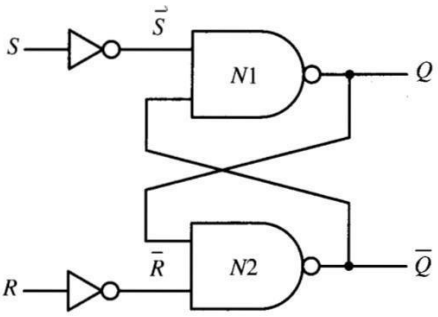

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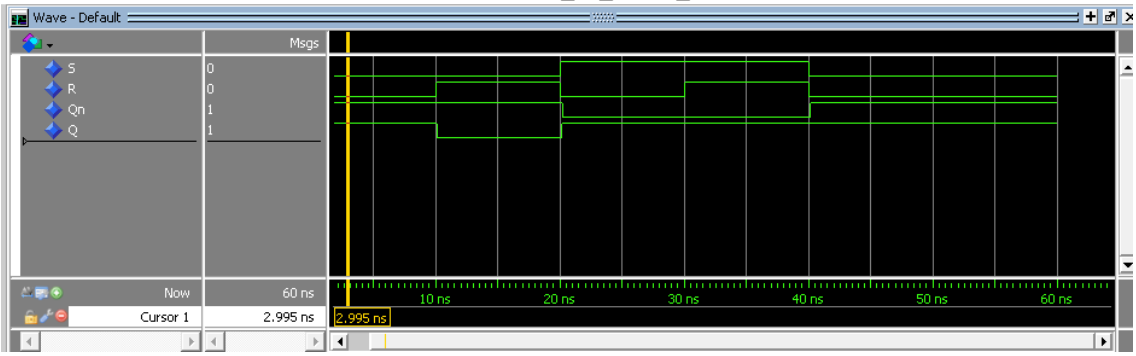

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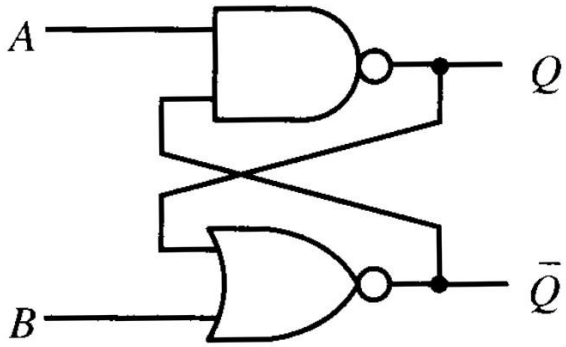

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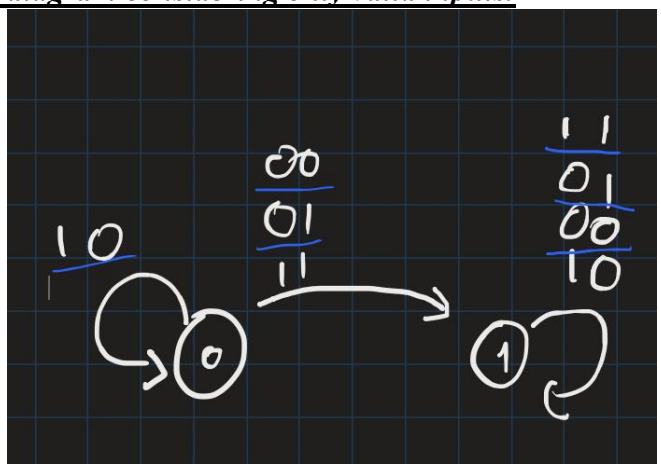

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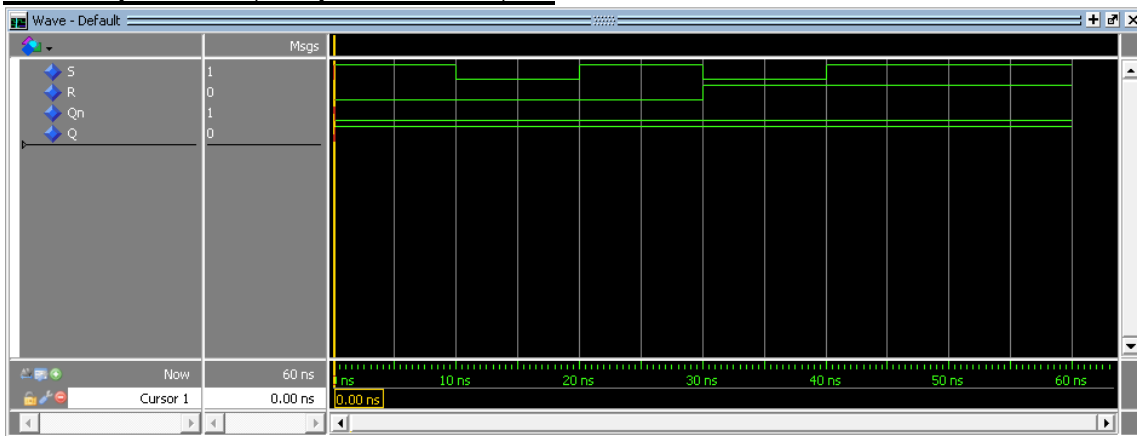

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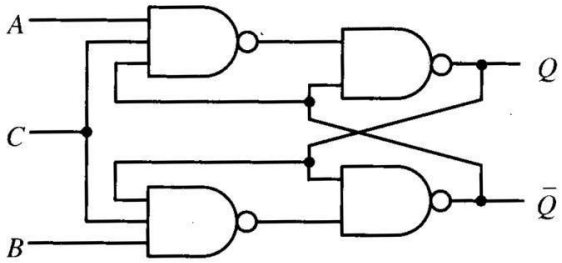

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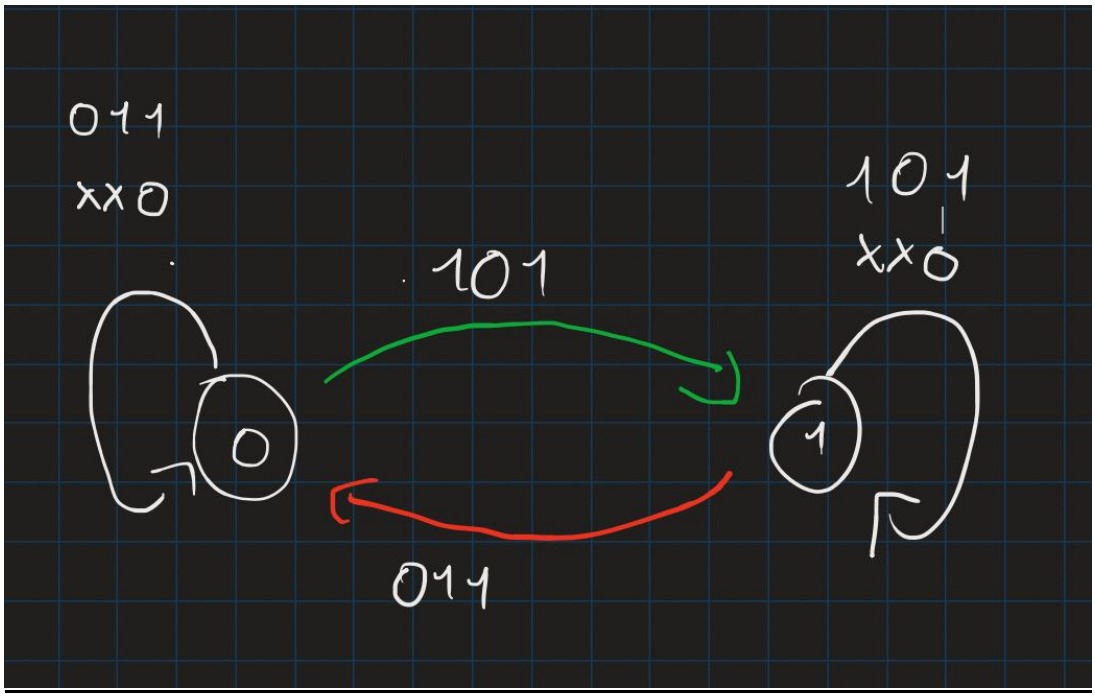

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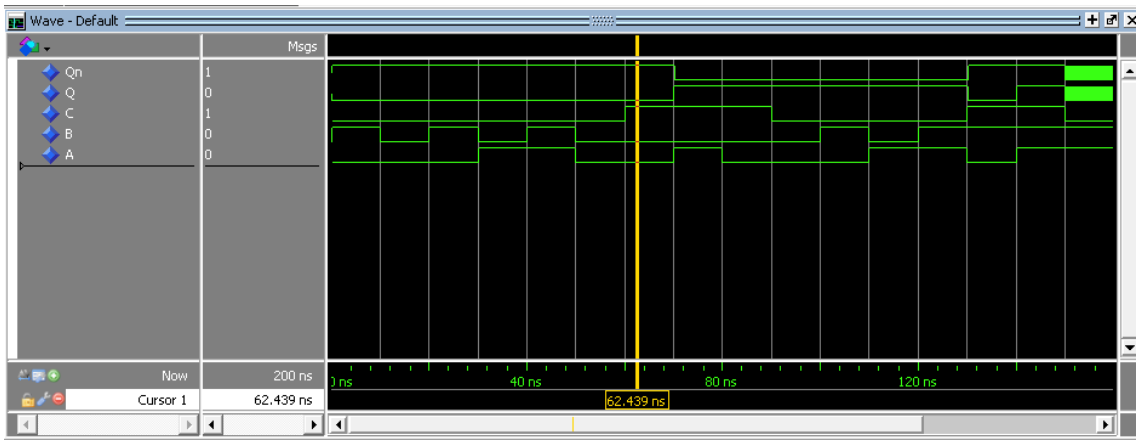

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