

CHAPTER 4

FET BIASING

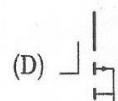
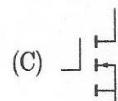
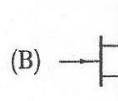
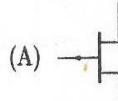
QUESTION 4.1

A JFET

- (A) is current controlled device
- (B) has low input resistance
- (C) has high gate current
- (D) is a voltage controlled device

QUESTION 4.2

Which of the following is the schematic symbol for an *N*-channel JFET?



QUESTION 4.3

For small values of drain-to-source voltage, JFET behaves like a

- (A) resistor
- (B) constant-current source
- (C) constant-voltage source
- (D) negative resistance

QUESTION 4.4

At pitch off voltage in a JFET device,

- (A) Channel width is zero and I_D becomes zero
- (B) Channel width is zero, but I_D is not zero
- (C) V_{GS} becomes zero
- (D) None of these

QUESTION 4.5

For an *n*-channel JFET, the parameters are $I_{DSS} = 6$ mA and $V_P = -3$ V. If $V_{DS} > V_{DS(sat)}$ and $V_{GS} = -2$ V, then I_D is

- (A) 16.67 mA
- (B) 0.67 mA
- (C) 5.55 mA
- (D) 1.67 mA

QUESTION 4.6

In a JFET, drain current is maximum when

- (A) V_{GS} is positive
- (B) V_{DS} is negative
- (C) V_{GS} is zero
- (D) V_{DS} is zero

~~Answer: D~~ JFET operates source-drain in saturation mode at

QUESTION 4.7

A JFET can operate in

- (A) Depletion mode only
- (B) enhancement mode only
- (C) depletion and enhancement mode
- (D) neither depletion nor enhancement mode

QUESTION 4.8

A p-channel JFET biased in the saturation region with $V_{GS} = 1$ V has a drain current of $I_D = 2.8$ mA, and $I_D = 0.3$ mA at $V_{GS} = 3$ V. The value of I_{DSS} is

----- mA

QUESTION 4.9

The transconductance of a JFET is 2 mS and its dynamic drain resistance is $80\text{ k}\Omega$. It should have an amplification factor of

- (A) 80
- (B) 40
- (C) 82
- (D) 160

QUESTION 4.10

The pinch off voltage V_p in the case of n-channel JFET is proportional to

- (A) N_D^2
- (B) $\frac{1}{N_D}$
- (C) $\frac{1}{\sqrt{N_D}}$
- (D) N_D

QUESTION 4.11

Compared to BJT, JFET is

- (A) Less noisy
- (B) more noisy
- (C) Same noisy
- (D) can't be said

QUESTION 4.12

MOSFET can be used as a

- (A) current controlled capacitor
- (B) voltage controlled capacitor
- (C) current controlled inductor
- (D) voltage controlled inductor

QUESTION 4.13

For an NMOS, the parameters are

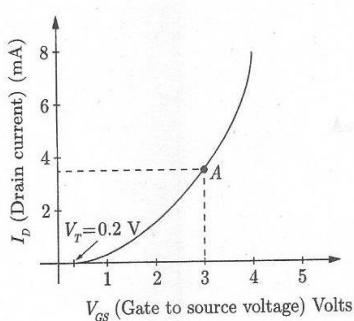
$$\frac{W}{L} = 100, \\ k_n = 100 \mu\text{A}/\text{V}^2, \\ V_{TN} = 0.75 \text{ V}$$

If gate to source voltage is $V_{GS} = 5$ V, then the value of ON resistance of the transistor is

----- Ω

QUESTION 4.14

The transfer characteristic of MOSFET is shown in figure below. The transistor parameter is $K = 0.445 \text{ mA/V}^2$. The values of drain current I_D and transconductance g_m at point A are, respectively



- (A) 3.488 mA, 2 mS
- (B) 1.724 mA, 2.5 mS
- (C) 1.7725 mS, 2 mS
- (D) 3.488 mA, 2.5 mS

QUESTION 4.15

Transconductance of an n -channel MOSFET operating in saturation region is g_{m1} . If the parameter W/L is doubled with current remaining constant, then new transconductance g_{m2} will be

- (A) $g_{m2} = g_{m1}$
- (B) $g_{m2} = g_{m1}/2$
- (C) $g_{m2} = \sqrt{2} g_{m1}$
- (D) $g_{m2} = 2g_{m1}$

QUESTION 4.16

Depletion MOSFETs can operate in

- (A) depletion mode only
- (B) enhancement mode only
- (C) both depletion and enhancement modes
- (D) none of the above

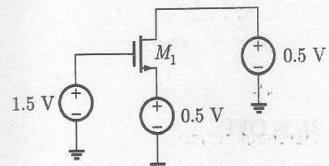
QUESTION 4.17

For a depletion-type MOSFET given that $I_{DSS} = 9.5 \text{ mA}$. For the drain current, $I_D = 14 \text{ mA}$ at $V_{GS} = 1 \text{ V}$. The value of pinch off voltage V_P is

$$V_P = \frac{V_{GS} - V_T}{K} I_D = \frac{1 - 0.2}{0.445} \times 14 = 2.5 \text{ V}$$

QUESTION 4.18

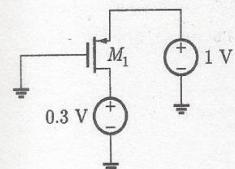
In the following circuit, the region of operation of M_1 is ($V_{TH} = 0.4 \text{ V}$)



- (A) Linear
- (B) Saturation
- (C) M_1 is off
- (D) Cannot be determined

QUESTION 4.19

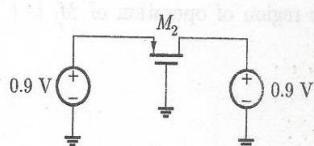
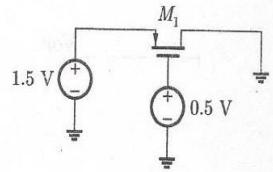
In the given circuit of figure if $V_{TH} = -0.4 \text{ V}$, the transistor M_1 is operating in



- (A) Linear region
- (B) Saturation region
- (C) M_1 is off
- (D) Cannot be determined

QUESTION 4.20

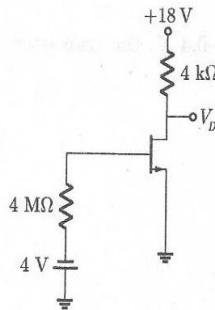
In the given circuit of figure, transistors M_1 and M_2 are operating in ($V_{TH} = 0.4 \text{ V}$)



- (A) M_1 is in linear region, M_2 is OFF
- (B) both M_1 and M_2 are OFF
- (C) M_1 is in saturation, M_2 is in linear region
- (D) both M_1 and M_2 are in saturation region

QUESTION 4.21

For the circuit shown below, the transistor parameters are $V_P = -4 \text{ V}$, $I_{DSS} = 8 \text{ mA}$ and $\lambda = 0$



What is the value of drain voltage V_D ?

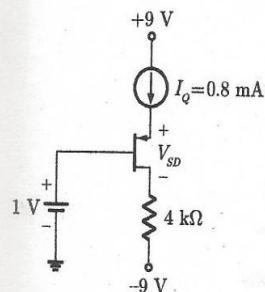
----- Volt

QUESTION 4.22

In the given circuit parameters of *p*-channel JFET transistor are

$$I_{DSS} = 2.5 \text{ mA}$$

$$V_P = +2.5 \text{ V} \text{ and } \lambda = 0$$



What is the value of source to drain voltage V_{SD} ?

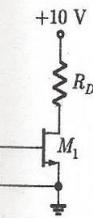
----- Volt

QUESTION 4.23

For the circuit shown below, transistor parameters are given as

$$I_{DSS} = 4 \text{ mA}, V_P = -3 \text{ V}, V_{DS} = 3 \text{ V}$$

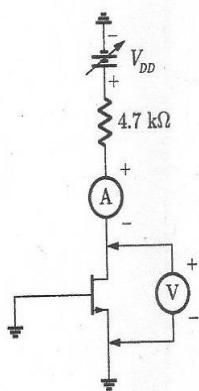
What is the value of resistance R_D ?



----- kΩ

QUESTION 4.24

Consider the circuit shown in figure below.

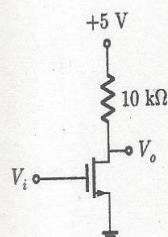


The JFET parameter is : $V_{GS(OFF)} = -4$ V. Assume that we increase the supply voltage 0 to V_{DD} until the ammeter reaches a steady value. At the point when the ammeter reaches a steady value, the value of voltmeter reading is

_____ Volt

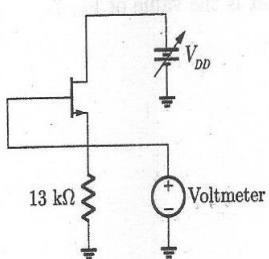
QUESTION 4.26

For the circuit shown below, the transistor parameters are $V_{TN} = 0.8$ V and $K_n' = 30 \mu\text{A}/\text{V}^2$. If output voltage is $V_o = 0.1$ V for input $V_i = 4.2$ V, then the required transistor width-to length ratio is



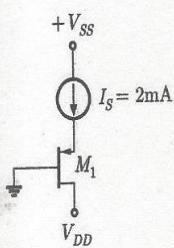
QUESTION 4.25

In the given circuit, when V_{DD} is increased the reading of voltmeter increases until V_{DD} reading reaches 16 V, after which the value of voltmeter reading is constant at 13 V. The value of I_{DSS} for the FET is



QUESTION 4.27

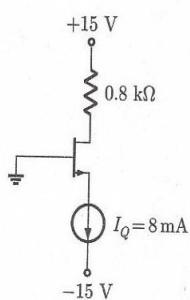
In the following circuit, pinch-off voltage is $V_P = 2.5$ V. What is the required value of V_{DD} such that the transistor operates in saturation ?



- (A) $V_{DD} \leq 2.5$ V
- (B) $V_{DD} \leq -2.5$ V
- (C) $V_{DD} \geq -2.5$ V
- (D) $V_{DD} \geq 2.5$ V

QUESTION 4.28

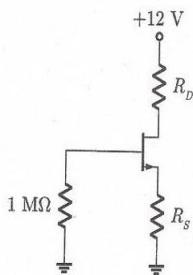
For the circuit shown below the transistor parameters are $V_p = -3.5$ V, $I_{DSS} = 18$ mA, and $\lambda = 0$. What is the value of V_{DS} ?



----- Volt

QUESTION 4.29

Consider the self bias circuit shown in figure below. The parameter of JFET is as follows: $I_{DSS} = 16$ mA, $V_p = -4$ V.



For the mid point bias in the circuit, what are the values of resistors R_D and R_S respectively ?

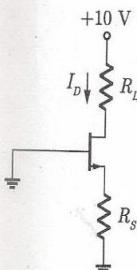
- (A) $147\ \Omega$, $603\ \Omega$
- (B) $1.47\ \text{k}\Omega$, $6.03\ \text{k}\Omega$
- (C) $603\ \Omega$, $147\ \Omega$
- (D) $6.03\ \text{k}\Omega$, $1.47\ \text{k}\Omega$

QUESTION 4.30

Consider an *n*-channel depletion mode JFET shown in figure below. The parameters of JFET are as follows:

$$I_{DSS} = 5\ \text{mV},$$

$$V_p = -4\ \text{V}, \lambda = 0$$



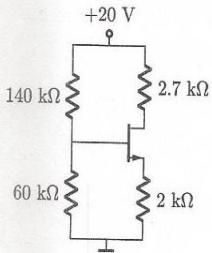
If the value of drain current is $I_D = 2$ mA and drain to source voltage is $V_{DS} = 6$ V, then the value of drain resistance (R_D) and source resistance (R_S) will be

- (A) $0.735\ \text{k}\Omega$, $1.27\ \text{k}\Omega$
- (B) $0.8\ \text{k}\Omega$, $1.2\ \text{k}\Omega$
- (C) $1.2\ \text{k}\Omega$, $0.8\ \text{k}\Omega$
- (D) $1.27\ \text{k}\Omega$, $0.735\ \text{k}\Omega$

The question has been modified to reflect the correct answer.

QUESTION 4.31

The transistor in the circuit shown below has parameters $I_{DSS} = 8$ mA and $V_p = -4$ V. What is the value of V_{DS} ?



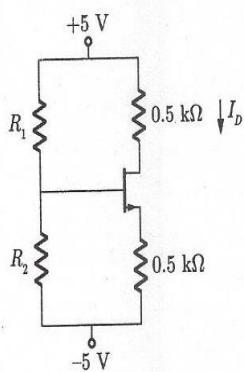
----- Volt

QUESTION 4.32

Consider a JFET circuit with a voltage divider biasing circuit. The parameter of transistor is as follows :

$$I_{DSS} = 12 \text{ mA}$$

$$V_P = -3.5 \text{ V}$$



The value of $R_1 + R_2 = 100 \text{ k}\Omega$ and drain current $I_D = 5 \text{ mA}$. What will be the value of resistances R_1 and R_2 respectively ?

- (A) $12.6 \text{ k}\Omega, 87.4 \text{ k}\Omega$
- (B) $37.4 \text{ k}\Omega, 62.6 \text{ k}\Omega$
- (C) $62.6 \text{ k}\Omega, 37.4 \text{ k}\Omega$
- (D) $87.4 \text{ k}\Omega, 12.6 \text{ k}\Omega$

QUESTION 4.33

If there is an internal open between the source and the drain in a CS amplifier, the drain voltage will be

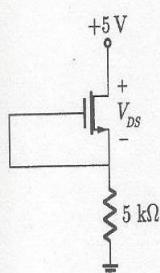
- (A) 0 V
- (B) V_{GS}
- (C) V_{DD}
- (D) $\frac{V_{DD}}{2}$

QUESTION 4.34

Consider the circuit shown below. The transistor parameters are as follows.

$$K_n = 0.1 \text{ mA/V}^2$$

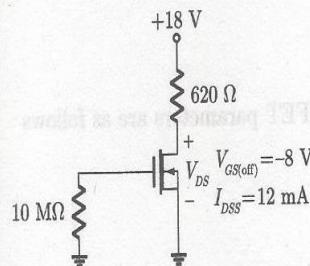
$$V_{TN} = -2 \text{ V}$$



What is the value of drain to source voltage V_{DS} ?

QUESTION 4.35

Consider the circuit shown in figure below. What is the value of drain to source voltage, V_{DS} ?

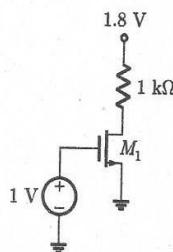


QUESTION 4.36

In the given circuit of figure, transistor parameters are given as

$$V_{TH} = 0.4 \text{ V}$$

$$\mu_n C_{ox} = 200 \frac{\mu\text{A}}{\text{V}^2}$$



If transistor operates at the edge of saturation, then parameter W/L is nearly equal to

- (A) 20
- (B) 10
- (C) 33
- (D) 40

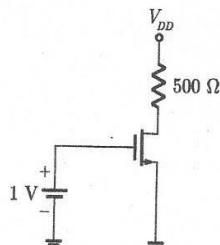
QUESTION 4.37

In the given circuit, the MOSFET parameters are as follows

$$\mu_n C_{ox} = 200 \frac{\mu\text{A}}{\text{V}^2}$$

$$\frac{W}{L} = 55.55$$

$$V_{TH} = 0.4 \text{ V}$$

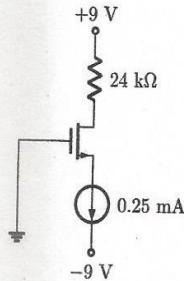


What is the minimum value of V_{DD} power supply so that MOSFET remains in saturation?

----- Volt

QUESTION 4.38

The parameter of the transistor shown below are $V_{TN} = 0.6 \text{ V}$ and $K_n = 0.2 \text{ mA/V}^2$. What is the voltage V_S ?



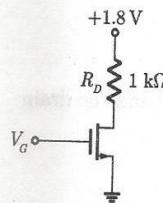
QUESTION 4.39

In the given circuit, the MOSFET parameters are given as

$$\mu_n C_{ox} = 10 \frac{\mu\text{A}}{\text{V}^2}$$

$$V_{TH} = 0.4$$

$$\frac{W}{L} = 11.11$$

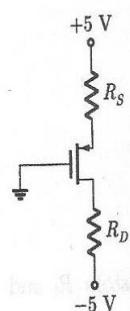


What is the maximum value of gate voltage so that MOSFET remains in saturation?

----- Volt

QUESTION 4.40

The PMOS transistor shown below has parameters $V_{TP} = -1.2$ V, $\frac{W}{L} = 20$, and $K_p = 30 \mu\text{A}/\text{V}^2$.

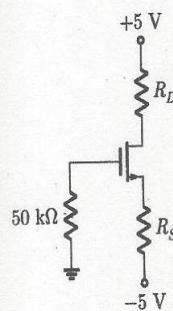


If $I_D = 0.5$ mA and $V_D = -3$ V, then value of R_s and R_D are respectively

- (A) 4 k Ω , 5.8 k Ω
- (B) 4 k Ω , 5 k Ω
- (C) 5.8 k Ω , 4 k Ω
- (D) 5 k Ω , 4 k Ω

QUESTION 4.42

In the circuit shown below the transistor parameters are $V_{TN} = 1.7$ V and $K_n = 0.4 \text{ mA/V}^2$.

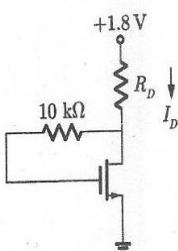


If $I_D = 0.8$ mA and $V_D = 1$ V, then value of resistor R_s and R_D are respectively

- (A) 2.36 k Ω , 5 k Ω
- (B) 5 k Ω , 2.36 k Ω
- (C) 6.43 k Ω , 8.4 k Ω
- (D) 8.4 k Ω , 6.43 k Ω

QUESTION 4.41

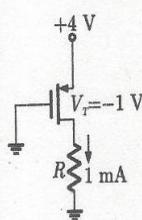
Consider the self bias circuit shown below. The parameter of MOSFET is as follows $V_{TN} = 0.4$ V.



For the value of drain current $I_D = 1$ mA and a transconductance $g_m = 10 \text{ mS}$, the value of resistor R_D is _____ k Ω .

QUESTION 4.43

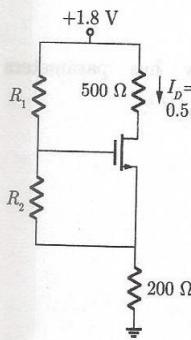
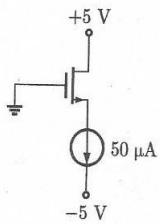
The value of R , for which the PMOS transistor in figure will be biased in linear region, is



- (A) 220 Ω
- (B) 470 Ω
- (C) 680 Ω
- (D) 1200 Ω

QUESTION 4.44

The parameter of the transistor shown below are $V_{TN} = 1.2$ V, $K_n = 0.5 \text{ mA/V}^2$, and $\lambda = 0$. The voltage V_{DS} is

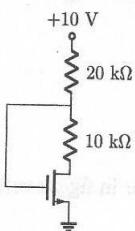


For the value of $I_D = 0.5 \text{ mA}$, the value of resistors R_1 and R_2 are respectively

- (A) 12.24 kΩ, 21.56 kΩ
- (B) 21.56 kΩ, 12.24 kΩ
- (C) 1.22 kΩ, 2.156 kΩ
- (D) 2.156 kΩ, 1.22 kΩ

QUESTION 4.45

For the transistor shown below, parameters are $V_{TN} = 1$ V and $K_n = 12.5 \mu\text{A/V}^2$. The Q-point (I_D, V_{DS}) is



- (A) (1 mA, 8 V)
- (B) (0.2 mA, 4 V)
- (C) (1.17 mA, 8 V)
- (D) (0.23 mA, 3.1 V)

QUESTION 4.46

In the circuit shown below, the MOSFET parameters are as follows:

$$V_{TN} = 0.4 \text{ V}$$

$$\mu_n C_{ox} = 200 \mu\text{A/V}^2$$

$$\frac{W}{L} = 111$$

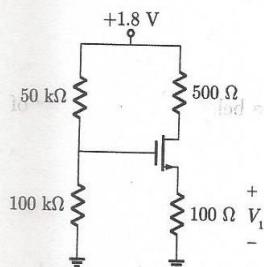
The current flowing through R_2 is one tenth of I_{D1} .

QUESTION 4.47

In the given circuit of figure, MOSFET parameters are

$$\mu_n C_{ox} = 200 \mu\text{A/V}^2$$

Voltage drop across the source resistance 100Ω is $V_t = 0.2 \text{ V}$. If MOSFET must remain in saturation then the minimum value of W/L is



QUESTION 4.48

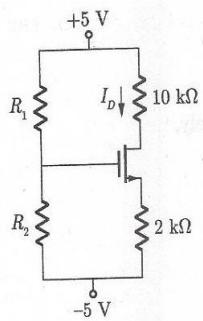
Consider the circuit shown below, the transistor parameter are as follows:

$$V_{TN} = 2 \text{ V}$$

$$k_n^i = 80 \mu\text{A}/\text{V}^2$$

$$\frac{W}{L} = 4$$

Drain current I_D of the circuit I_D is 0.5 mA and current in resistor R_2 is 1/10 of I_D .



The value of resistors R_1 and R_2 are, respectively

- (A) 95.4 kΩ, 104.6 kΩ
- (B) 142.3 kΩ, 57.7 kΩ
- (C) 57.7 kΩ, 142.3 kΩ
- (D) 104.6 kΩ, 95.4 kΩ

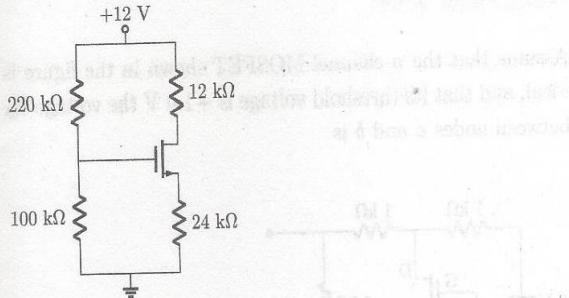
QUESTION 4.49

Consider a circuit shown in figure below. The parameter of NMOS is given as

$$k_n^i = 100 \mu\text{A}/\text{V}^2$$

$$\frac{W}{L} = 5$$

$$V_{TN} = +1 \text{ V}$$



The value of Q-Point (V_{DSQ}, I_{DQ}) is

- (A) 8.77 V, 89.7 μA
- (B) 1.599 V, 89.7 μA
- (C) 8.77 V, 143.7 μA
- (D) 6.82 V, 143.7 μA

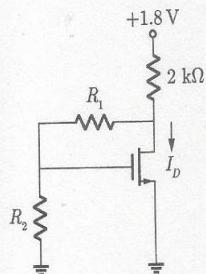
QUESTION 4.50

In the circuit shown below, the MOSFET parameters are as follows:

$$V_{TN} = 0.4 \text{ V}$$

$$\mu_n C_{ox} = 200 \mu\text{A}/\text{V}^2$$

$$\frac{W}{L} = 278$$

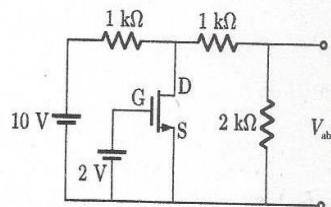


Current flowing through resistor R_2 equals to one tenth (1/10) of I_D (Drain current). For the value of Drain current $I_D = 0.5 \text{ mA}$, the value of resistors R_1 and R_2 are respectively

- (A) 5.32 kΩ, 10.68 kΩ
- (B) 1.068 kΩ, 14.932 kΩ
- (C) 10.68 kΩ, 3.32 kΩ
- (D) 3.32 kΩ, 10.68 kΩ

QUESTION 4.51

Assume that the *n*-channel MOSFET shown in the figure is ideal, and that its threshold voltage is +1.0 V the voltage V_{ab} between nodes *a* and *b* is



QUESTION 4.52

Consider the circuit shown below. The transistors have following parameters:

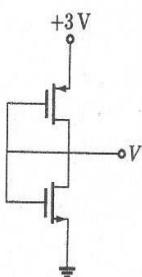
$$\mu_n C_{ox} = 2.5 \mu_p C_{ox} = 20 \mu\text{A/V}^2$$

$$V_{TN} = 1 \text{ V}$$

$$V_{TP} = -1 \text{ V}, \lambda = 0$$

$$\frac{W}{L} = 3$$

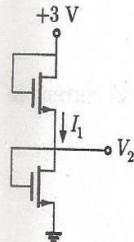
What is value of voltage V ?



QUESTION 4.53

For the circuit shown below, both transistors are identical and has following parameters:

$$\mu_n C_{ox} = 2.5 \mu\text{A/V}^2, V_{TH} = 1 \text{ V}, \frac{W}{L} = 3$$

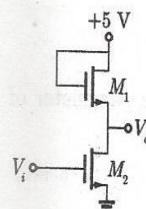


Current I_1 and voltage V_2 are respectively,

- (A) 15 μA , 3 V
- (B) 7.5 μA , 1.5
- (C) 15 μA , 1.5 V
- (D) 7.5 μA , 3 V

QUESTION 4.54

The transistors in the circuit shown below have parameter $V_{TN} = 0.8 \text{ V}$, $k'_n = 40 \mu\text{A/V}^2$ and $\lambda = 0$. The width-to-length ratio of M_2 is $(\frac{W}{L})_2 = 1$. If $V_o = 0.10 \text{ V}$ and $V_i = 5 \text{ V}$, then $(\frac{W}{L})_1$ for M_1 is



$$\times 10^{-3}$$

QUESTION 4.55

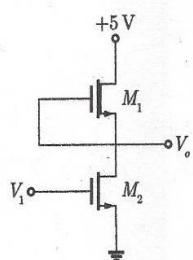
Consider the circuit shown below. The transistor parameters are as follows

$$\text{For } M_2 \quad V_{TN2} = 1 \text{ V for } M_1$$

$$K_{n2} = 50 \mu\text{A/V}^2$$

$$\text{For } M_1 \quad V_{TN1} = -2 \text{ V}$$

$$K_{n1} = 10 \mu\text{A/V}^2$$



If $V_i = 5 \text{ V}$, then what is the value of output voltage (V_o) ?

----- Volt

QUESTION 4.56

In the circuit shown below, the PMOS transistor has parameters $V_{TP} = -1.5 \text{ V}$, $k_p = 25 \mu\text{A/V}^2$, $L = 4 \mu\text{m}$ and $\lambda = 0$. If $I_D = 0.1 \text{ mA}$ and $V_{SD} = 2.5 \text{ V}$, then value of W will be



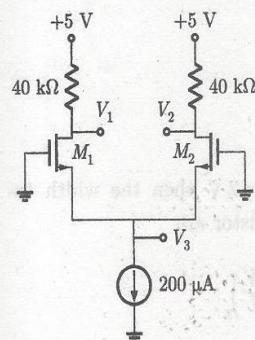
QUESTION 4.57

In the following circuit, transistors Q_1 and Q_2 has following parameters:

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 20$$

$$(V_{TH})_1 = (V_{TH})_2 = 1 \text{ V}$$

$$(k'_n)_1 = (k'_n)_2 = 100 \mu\text{A/V}^2$$

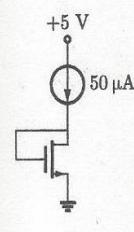


The voltages V_1 , V_2 and V_3 are respectively

- (A) 1 V, 1 V, -1.1 V
- (B) 1 V, 2 V, 1 V
- (C) 2 V, 1 V, 1.32 V
- (D) 1 V, 1 V, -1.32 V

QUESTION 4.58

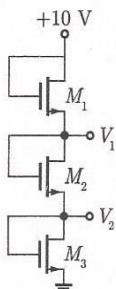
The parameter of the transistor shown below are $V_{TN} = 1.2 \text{ V}$, $K_n = 0.5 \text{ mA/V}^2$ and $\lambda = 0$. The voltage V_{DS} is



----- Volt

QUESTION 4.59

In the circuit shown below, the transistor parameters are $V_{TN} = 1\text{ V}$ and $K_n = 36\text{ }\mu\text{A/V}^2$.



If $I_D = 0.5\text{ mA}$, $V_1 = 5\text{ V}$ and $V_2 = 2\text{ V}$ then the width to length ratio required in each transistor are

- | | $(\frac{W}{L})_1$ | $(\frac{W}{L})_2$ | $(\frac{W}{L})_3$ |
|-----|-------------------|-------------------|-------------------|
| (A) | 1.75 | 6.94 | 27.8 |
| (B) | 4.93 | 10.56 | 50.43 |
| (C) | 35.5 | 22.4 | 5.53 |
| (D) | 56.4 | 38.21 | 12.56 |

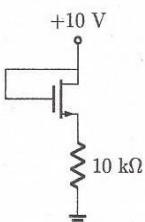
QUESTION 4.61

An FET cannot operate at $V_{GS} = 0\text{ V}$. The FET is

- (A) JFET
- (B) D-MOSFET
- (C) E-MOSFET
- (D) both (a) and (b)

QUESTION 4.60

The parameters for the transistor shown below are $V_{TN} = 2\text{ V}$ and $K_n = 0.2\text{ }\mu\text{A/V}^2$. The power dissipated in the transistor is



mW

Answer

4.1	D
4.2	B
4.3	A
4.4	B
4.5	B
4.6	C
4.7	A
4.8	5
4.9	D
4.10	D
4.11	A
4.12	B
4.13	23
4.14	D
4.15	C
4.16	C
4.17	-4.67V
4.18	A
4.19	B
4.20	C
4.21	18
4.22	5.71
4.23	1.75
4.24	4
4.25	1
4.26	0.731
4.27	B
4.28	7.43
4.29	C
4.30	D
4.31	2.85

4.32	D
4.33	C
4.34	3
4.35	10.56
4.36	C
4.37	1.6
4.38	-1.72
4.39	1.35
4.40	D
4.41	1.2
4.42	A
4.43	D
4.44	6.52
4.45	D
4.46	B
4.47	56
4.48	D
4.49	A
4.50	D
4.51	0
4.52	1.39
4.53	B
4.54	49.37
4.55	0.1
4.56	32
4.57	D
4.58	1.52
4.59	A
4.60	2.35
4.61	C

CHAPTER 5

FET AMPLIFIERS

QUESTION 5.1

For an *n*-channel MOSFET biased in the saturation region, the parameters are:

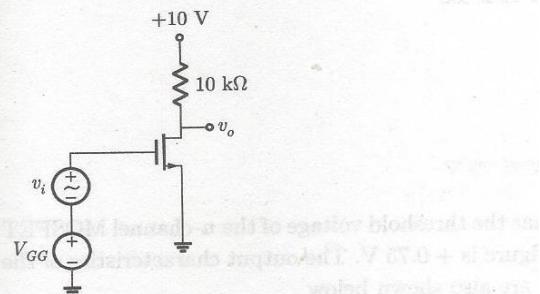
$$V_{TN} = 1 \text{ V},$$

$$\frac{1}{2}\mu_n C_{ax} = 18 \mu\text{A/V}^2,$$

$$\lambda = 0.015 \text{ V}^{-1}, \text{ and}$$

and $I_{DQ} = 2 \text{ mA}.$

If transconductance is $g_m = 3.4 \text{ mA/V}$, then what is the width-to-length ratio?



If I_{DQ} is to be 0.4 mA , the value of V_{GSQ} is

- (A) 514 V
- (B) 4.36 V
- (C) 2.89 V
- (D) 1.83 V

QUESTION 5.2

For an *n*-channel MOSFET biased in the saturation region, the parameters are $K_n = 0.5 \text{ mA/V}^2$, $V_{TN} = 0.8 \text{ V}$, $\lambda = 0.01 \text{ V}^{-1}$, and $I_{DQ} = 0.75 \text{ mA}$. The value of g_m and r_o are

- (A) 0.68 mS, $603 \text{ k}\Omega$
- (B) 1.22 mS, $603 \text{ k}\Omega$
- (C) 1.22 mS, $133 \text{ k}\Omega$
- (D) 0.68 mS, $133 \text{ k}\Omega$

QUESTION 5.4

In previous question the values of g_m and r_o are

- (A) 0.89 mS, ∞
- (B) 0.89 mS, 0
- (C) 1.48 mS, 0
- (D) 1.48 mS, ∞

QUESTION 5.3

For the circuit shown below transistor parameters are $V_{TN} = 2 \text{ V}$, $K_n = 0.5 \text{ mA/V}^2$ and $\lambda = 0$. The transistor is in saturation.

QUESTION 5.5

In Q 3 the small signal voltage gain A_v is

- (A) 14.3
- (B) -14.3
- (C) -8.9
- (D) 8.9

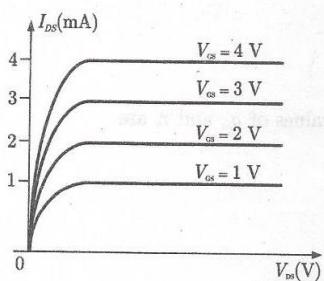
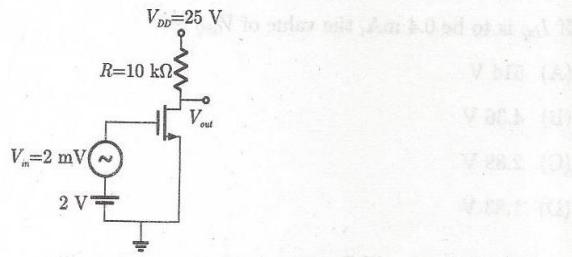
QUESTION 5.6

Which of the following amplifier has high input resistance and high output resistance

- (A) Common-source
- (B) Common-drain
- (C) Common-gate
- (D) None of these

QUESTION 5.7

Assume that the threshold voltage of the *n*-channel MOSFET shown in figure is +0.75 V. The output characteristics of the MOSFET are also shown below.



What is the transconductance of the MOSFET ?

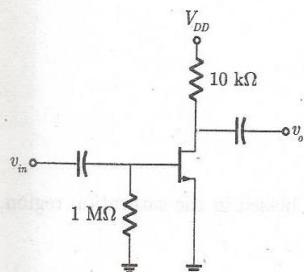
----- mS

QUESTION 5.8

In previous question what is the voltage gain of the amplifier?

QUESTION 5.9

Consider the circuit of common source amplifier shown in figure below.



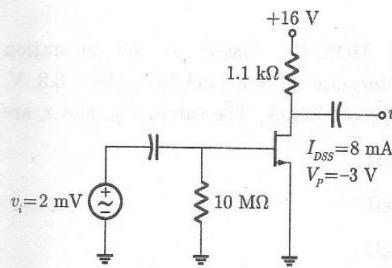
FET parameters are as follows :

$I_{DSS} = 2.0 \text{ mA}$, and $g_m = 2 \text{ mS}$. If $V_{GS} = -1 \text{ V}$,

What is the value of small signal voltage gain $A_v = \frac{v_o}{v_i}$?

QUESTION 5.10

Consider a circuit shown below.



What is the value of transconductance g_m ?

----- mS

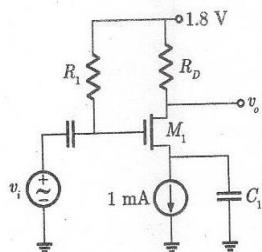
QUESTION 5.11

In previous question what is the value of output voltage v_o ?

----- mV

QUESTION 5.12

Consider the common source circuit shown below.



Transistor parameters are given as

$$\lambda = 0, V_{TH} = 0.4 \text{ V}, \mu_n C_{ox} = 200 \mu\text{A/V}^2$$

What is the maximum allowable value of resistor R_D for M_1 to remain in saturation?

- _____ kΩ
 (A) -224
 (B) -280
 (C) -80
 (D) -54

What is the value of input impedance R_{in} ?

- (A) infinity
 (B) zero
 (C) $1 \text{ M}\Omega$
 (D) None of the above

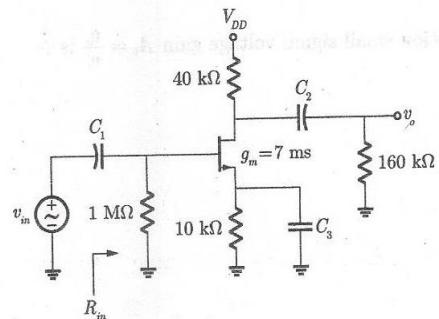
QUESTION 5.13

In previous question if voltage gain $A_v = 5$, then parameter (W/L) is

- (A) 630.80
 (B) 390.6
 (C) 220.56
 (D) 150.95

QUESTION 5.14

Consider the circuit shown in figure below.



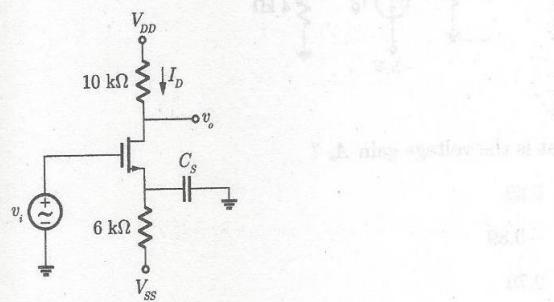
QUESTION 5.15

In previous question what is the value of small signal voltage gain $A_v = \frac{v_o}{v_i}$?

- (A) -224
 (B) -280
 (C) -80
 (D) -54

QUESTION 5.16

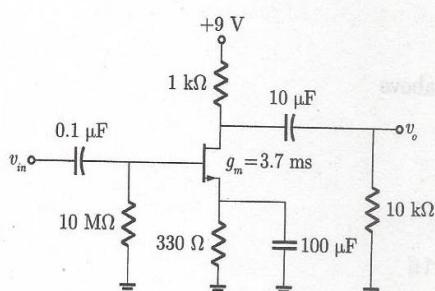
For the amplifier circuit, given that the drain current is $I_D = 1 \text{ mA}$, transconductance is $g_m = 1 \text{ mA/V}^2$, and 3 dB frequency for capacitor C_s is $f_L = 10 \text{ Hz}$. What will be the value of capacitance C_s ?



_____ μF

QUESTION 5.17 A cascaded stage is shown below

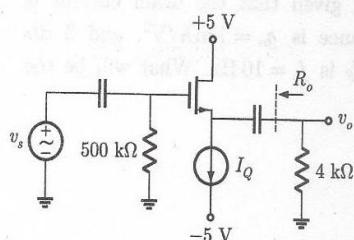
Consider the circuit shown below.



If a 10 mV rms signal is applied to the input of the amplifier, then what will be the rms value of the output signal?

QUESTION 5.18

Consider the source-follower circuit shown below. The values of parameter are $g_m = 2 \text{ mS}$ and $r_o = 100 \text{ k}\Omega$.



What is the voltage gain A_v ?

- (A) 0.89
- (B) -0.89
- (C) 2.79
- (D) -2.79

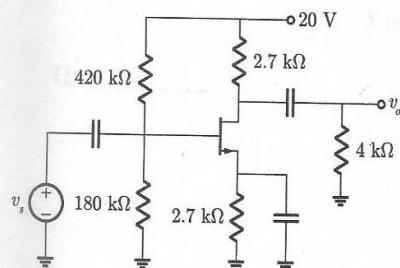
QUESTION 5.19

In previous question the output resistance R_o is

- (A) $100 \text{ k}\Omega$
- (B) $0.498 \text{ k}\Omega$
- (C) $1.33 \text{ k}\Omega$
- (D) None of these

QUESTION 5.20

A *n*-channel JFET amplifier circuit is shown in figure below.



Transistor parameters are given as

$$I_{DSS} = 12 \text{ mA}, V_P = -4 \text{ V}, \lambda = .008 \text{ V}^{-1}$$

What is the small signal transconductance g_m ?

- (A) 9.01 mA/V
- (B) 1.5 mA/V
- (C) 4.5 mA/V
- (D) 2.98 mA/V

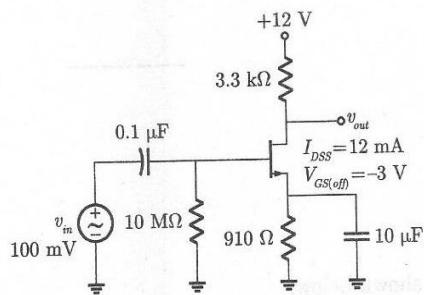
QUESTION 5.21

In previous question small signal voltage gain $A_v = \frac{v_o}{v_s}$ is

- (A) -9.25
- (B) -27.72
- (C) -4.62
- (D) -41.58

QUESTION 5.22

Consider the amplifier circuit shown below.

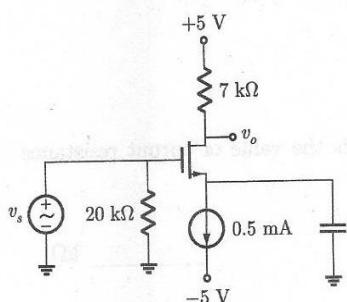


What is the output voltage of the amplifier due to given input voltage (v_m) ?

_____ Volt(rms)

QUESTION 5.23

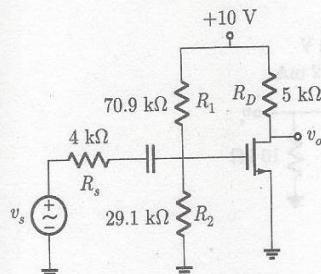
Consider the common-source circuit with source bypass capacitor. The signal frequency is sufficiently large. The transistor parameters are $V_{TN} = 0.8$ V, $K_n = 1$ mA/V² and $\lambda = 0$. The voltage gain is



- (A) -15.6
- (B) -9.9
- (C) -6.8
- (D) -3.2

QUESTION 5.24

Consider the common source amplifier shown below. The transistor parameter are $V_{TN} = 1.5$ V, $K_n = 0.5$ mA/V², an $\lambda = 0.01$ V⁻¹. The resistance of source is $R_s = 4$ kΩ.



What is the small-signal voltage gain A_v ?

- (A) -8.2
- (B) -5.6
- (C) -3.1
- (D) -1.9

QUESTION 5.25

In previous question the amplifier output resistance is

- (A) 4.76 kΩ
- (B) 100 kΩ
- (C) 5 kΩ
- (D) 0

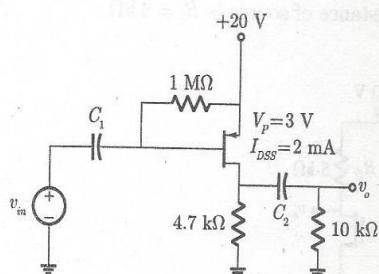
QUESTION 5.26

In Q 24 the amplifier input resistance is

- (A) 20.6 kΩ
- (B) 70.9 kΩ
- (C) 29.1 kΩ
- (D) 104 kΩ

QUESTION 5.27

Consider the JFET amplifier circuit shown in figure below.



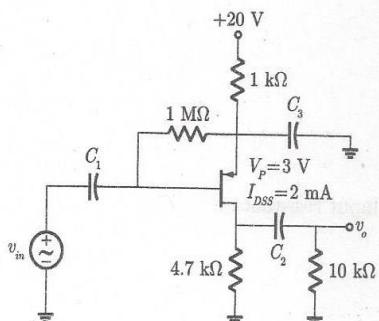
What is the value of Transconductance g_m ?

QUESTION 5.28

In previous question what is the small signal voltage gain $A_v = \frac{v_o}{v_{in}}$?

QUESTION 5.29

Consider the JFET amplifier circuit shown in figure.



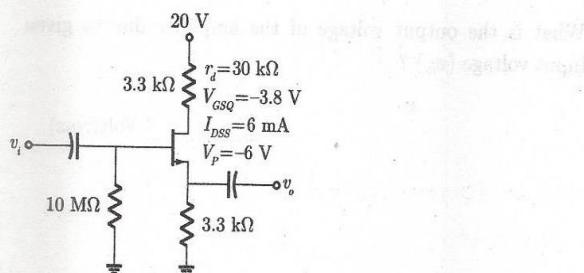
What is the value of transconductance g_m ?

QUESTION 5.30

In previous question what is small signal voltage gain $A_v = \frac{v_o}{v_{in}}$?

QUESTION 5.31

Consider the circuit shown below.



What is the value of transconductance g_m ?

QUESTION 5.32

A) In previous question what is the value of output resistance R_o ?

B) _____ kΩ

QUESTION 5.33

In Q 31 what is the small signal voltage gain $A_v = \frac{v_o}{v_{in}}$?

mS

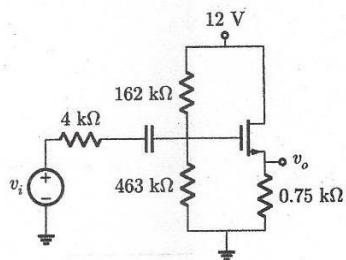
QUESTION 5.34

Consider the source follower amplifier circuit shown in figure. Transistors parameters are

$$V_{TH} = 1.5 \text{ V},$$

$$K_n = 4 \text{ mA/V}^2,$$

$$\lambda = 0.01 \text{ V}^{-1}$$



Small signal transconductance is

- (A) 29.52 mA/V
- (B) 59.04 mA/V
- (C) 11.3 mA/V
- (D) 5.65 mA/V

QUESTION 5.35

In previous question the small signal voltage gain $A_v = \frac{v_o}{v_i}$ is

- (A) 1.20
- (B) 0.86
- (C) 1.13
- (D) 0.98

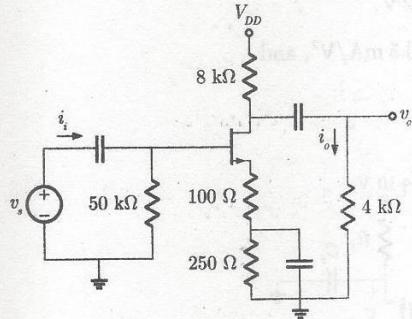
QUESTION 5.36

In Q 34.output resistance of the amplifier circuit is

- (A) 707 Ω
- (B) 12.5 kΩ
- (C) 67.1 Ω
- (D) 78.7 Ω

QUESTION 5.37

Consider the JFET amplifier circuit shown in figure.



Transistors parameters are

$$I_{DSS} = 2 \text{ mA}, V_P = -2, \lambda = 0$$

Transconductance is

- (A) 1.57 mA/V
- (B) 0.785 mA/V
- (C) 11.28 mA/V
- (D) 13.81 mA/V

QUESTION 5.38

In previous question small signal voltage gain A_v is

- (A) -1.81
- (B) -31.86
- (C) -26.01
- (D) -3.62

QUESTION 5.39

In Q 37 current gain $A_i = \frac{i_o}{i_i}$ is

- (A) -22.63
- (B) -398.25
- (C) -45.3
- (D) -0.29

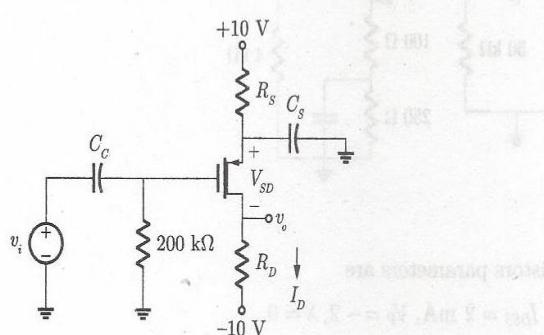
QUESTION 5.40

Consider the amplifier circuit shown below. The transistor parameter are as follows :

$$V_{TP} = 2 \text{ V},$$

$$K_p = 0.5 \text{ mA/V}^2, \text{ and}$$

$$\lambda = 0$$



If the value of source to drain voltage is $V_{SD} = 6 \text{ V}$ and drain current is $I_D = 2 \text{ mA}$, then the value of R_D and R_s , respectively are

- (A) $5 \text{ k}\Omega, 2 \text{ k}\Omega$
- (B) $3 \text{ k}\Omega, 4 \text{ k}\Omega$
- (C) $4 \text{ k}\Omega, 3 \text{ k}\Omega$
- (D) $2 \text{ k}\Omega, 5 \text{ k}\Omega$

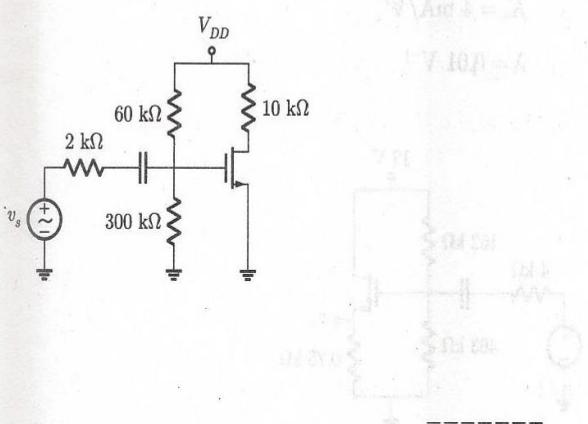
QUESTION 5.41

In previous question what is the value of small signal voltage gain $A_v = \frac{v_o}{v_i}$?

- (A) -2
- (B) -8
- (C) -4
- (D) None of the above

QUESTION 5.42

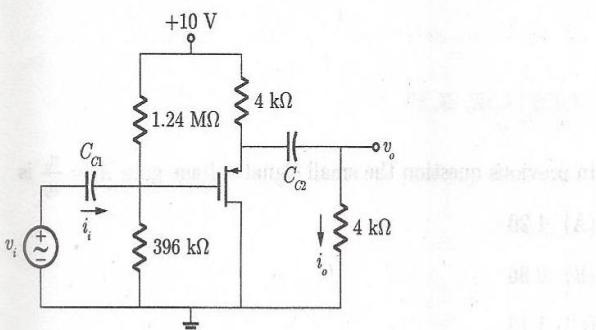
In the circuit shown below, the parameters are $g_m = 1 \text{ mA/V}$, $r_o = 50 \text{ k}\Omega$. What will be the voltage gain $A_v = \frac{v_o}{v_s}$?



QUESTION 5.43

Consider a source follower circuit shown in figure below. Transistor has the parameters as follows:

$$K_p = 2 \text{ mA/V}^2, V_{TP} = -2 \text{ V} \text{ and } \lambda = 0.02 \text{ V}^{-1}$$



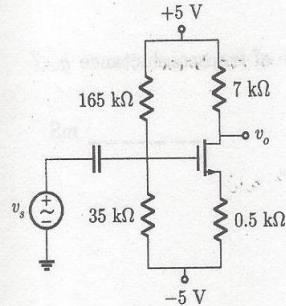
The value of Q point (V_{SDQ}, I_{DQ}) is

- (A) 2.78 V, 1.21 mA
- (B) 1.0985, 1.62 mA
- (C) 5.16 V, 1.21 mA
- (D) 3.52 V, 1.62 mA

QUESTION 5.44

In previous question the value of transconductance g_m and small signal output resistance r_o , respectively are

- (A) 41.3 mA/V^2 , $3.11 \text{ k}\Omega$
- (B) 3.11 mA/V^2 , $41.3 \text{ k}\Omega$
- (C) 3.6 mA/V^2 , $30.86 \text{ k}\Omega$
- (D) 30.86 mA/V^2 , $3.6 \text{ k}\Omega$



QUESTION 5.45

In Q 43 what is the small signal voltage gain $A_v = \frac{v_o}{v_{in}}$?

- (A) 0.886
- (B) 0.98
- (C) 2.98
- (D) 2.886

QUESTION 5.46

Which of the following amplifier has high input impedance, low output impedance and low voltage gain ?

- (A) Common-gate
- (B) Common-Drain
- (C) Common-Source
- (D) None of these



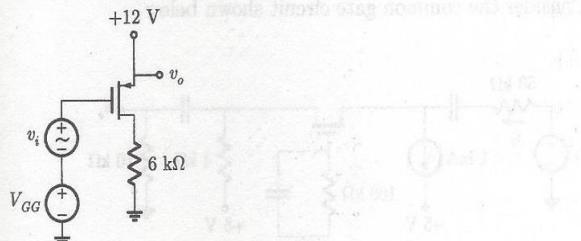
QUESTION 5.46

In Q 43 what is the value of small signal current gain $A_i = i_o / i_i$?

- (A) 64.2
- (B) 0.882
- (C) 0.214
- (D) 11.339

QUESTION 5.49

For the circuit shown below transistor parameters are $V_{TP} = -1 \text{ V}$, $K_p = 2 \text{ mA/V}^2$, and $\lambda = 0$. The transistor is in saturation.



If $V_{SDQ} = 7 \text{ V}$, then what is the value of V_{SGQ} ?

Volt

QUESTION 5.50

In previous question what is the of transconductance g_m ?

mS

Small signal transconductance is

- (A) 2 mA/V
- (B) 8 mA/V
- (C) 1 mA/V
- (D) 4 mA/V

QUESTION 5.51

In Q 49 what is the small signal voltage gain A_v ?

QUESTION 5.54

In previous question if the input current is

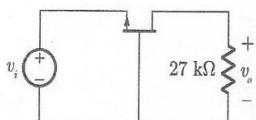
$$i_i = (100 \sin \omega t) \mu A$$

then output v_o is

- (A) $(1.13 \sin \omega t)$ V
- (B) $(0.283 \sin \omega t)$ V
- (C) $(1.13 \cos \omega t)$ V
- (D) $(0.283 \cos \omega t)$ V

QUESTION 5.52

If $I_D = 1$ mA, $I_{DSS} = 5$ mA and $V_{TH} = -2$ V for the common gate circuit shown in figure, what will be the input resistance to the circuit ?

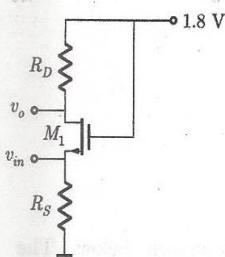


QUESTION 5.55

In the following amplifier circuit, M_1 operates 100 mV away from triode region providing a voltage gain of 4. Power dissipated in M_1 is 2 mW.

Transistor parameters are

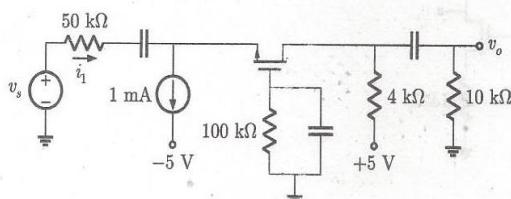
$$\lambda = 0, \mu_n C_{ax} = 200 \mu A/V^2, V_{TH} = 0.4 V$$



What is the value of resistor R_D ?

QUESTION 5.53

Consider the common gate circuit shown below.



Transistor parameters are

$$V_{TH} = 1 V, K_n = 1 \text{ mA/V}^2, \lambda = 0$$

QUESTION 5.56

In previous question what is the resistance R_S ?

$$\underline{\hspace{2cm}} \text{k}\Omega$$

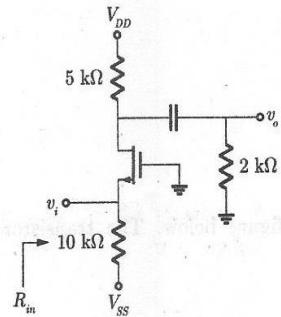
QUESTION 5.57

In Q 55 what is the value of parameter $\frac{W}{L}$?

$$\underline{\hspace{2cm}}$$

QUESTION 5.58

Consider the circuit shown in figure below.



Given that g_m (transconductance) = 5 mA/V. What is the value of voltage gain $A_v = \frac{v_o}{v_i}$?

QUESTION 5.59

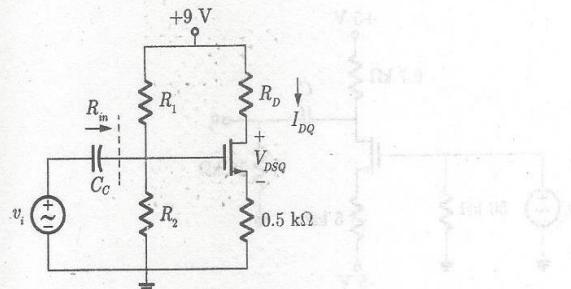
In previous question what is the value of input Resistance R_{in} ?

$$\underline{\hspace{2cm}} \Omega$$

QUESTION 5.60

Consider the circuit shown in below. The transistor parameters are:

$$K_n = 0.2 \text{ mA/V}^2, V_{TN} = 1.5 \text{ V}, \text{ and } \lambda = 0$$



Given that drain current, $I_{DQ} = 0.5 \text{ mA}$ and drain to source voltage, $V_{DS} = 4.5 \text{ V}$. What is the value of resistance R_D ?

- (A) 9 kΩ
- (B) 0.5 kΩ
- (C) 8.5 kΩ
- (D) 1.75 kΩ

QUESTION 5.61

In previous question if input resistance of circuit is $R_{in} = 200 \text{ k}\Omega$ then the value of resistors R_1 and R_2 respectively are

- (A) 317 kΩ, 541 kΩ
- (B) 636 kΩ, 291 kΩ
- (C) 291 kΩ, 636 kΩ
- (D) 541 kΩ, 317 kΩ

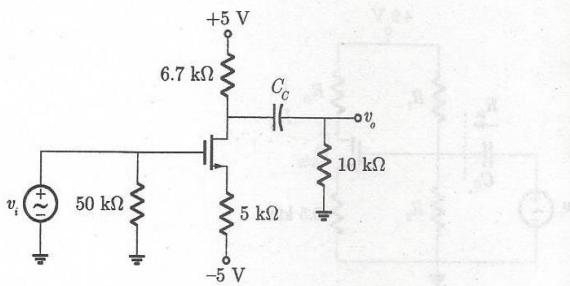
QUESTION 5.62

In Q 60 if 3 dB frequency due to C_C is 20 Hz then the value of coupling capacitor C_C is

- (A) 0.0398 μF
- (B) 88.46 μF
- (C) 3.98 nF
- (D) 0.884 μF

QUESTION 5.63

Consider the circuit shown in figure below. If the lower corner frequency due to coupling capacitor C_C is $f_L = 20$ Hz, then the value of coupling capacitor C_C is



QUESTION 5.65

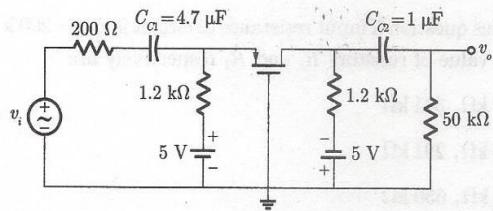
In previous question what is the value of 3 dB frequency due to coupling capacitor C_C ?

- (A) 70 Hz
- (B) 24.1 Hz
- (C) 59.4 Hz
- (D) 170 Hz

QUESTION 5.64

Consider the circuit shown in figure below. The Transistor parameters are:

$$K_P = 1 \text{ mA/V}^2, V_{TP} = -1.5 \text{ V} \text{ and } \lambda = 0$$



The values of small signal parameters g_m and r_o are, respectively

- (A) 8.68 mA/V, $\infty \Omega$
- (B) 4.34 mA/V, 0.55 kΩ
- (C) 2.68 mA/V, 55 kΩ
- (D) 2.68 mA/V, $\infty \Omega$

QUESTION 5.66

In Q 64 what is the value of 3 dB frequency due to coupling capacitor C_C2 ?

- (A) 3.1 Hz
- (B) 19.5 Hz
- (C) 132.6 Hz
- (D) None of the above

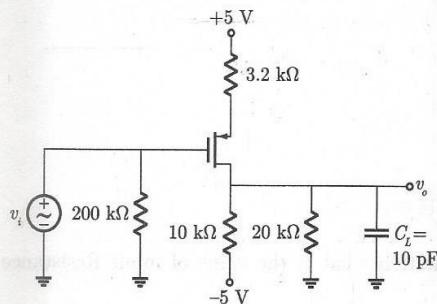
QUESTION 5.67

Consider a circuit shown in figure below. The transistor parameters are:

$$V_{TP} = -2 \text{ V}$$

$$K_p = 0.25 \text{ mA/V}^2$$

$$\lambda = 0$$



What is the value of transconductance g_m

$$\text{_____ mA/V}^2$$

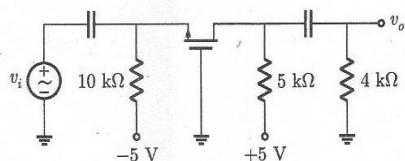
QUESTION 5.68

In previous question what is the value of 3 dB corner frequency due to capacitor C_L ?

----- MHz

QUESTION 5.69

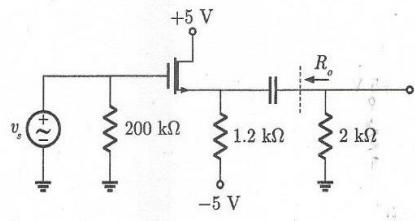
Consider the NMOS common-gate circuit shown below. The parameters are $g_m = 2 \text{ mS}$ and $r_o = \infty$. The voltage gain A_v is



- (A) 4.44
- (B) -4.44
- (C) 2.22
- (D) -2.22

QUESTION 5.70

A depletion NMOS transistor circuit is shown in figure.



Transistor parameters are given as

$V_{TH} = -2 \text{ V}$, $K_n = 5 \text{ mA/V}^2$, $\lambda = 0.01 \text{ V}^{-1}$

Transconductance g_m is

- (A) 5 mA/V
- (B) 3.33 mA/V
- (C) 10 mA/V
- (D) 6.81 mA/V

QUESTION 5.71

In previous question voltage gain $A_v = \frac{v_o}{v_s}$ is

- (A) 0.290
- (B) 0.878
- (C) 0.60
- (D) 0.44

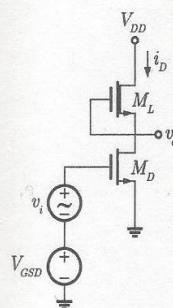
QUESTION 5.72

In Q 70 output impedance R_o is

- (A) 20 kΩ
- (B) 1.13 kΩ
- (C) 137 Ω
- (D) 91.9 Ω

QUESTION 5.73

An NMOS amplifier with depletion load (M_L) is shown in figure. Parameters for transistors M_D and M_L are $V_{THD} = +0.8 \text{ V}$, $K_{nD} = 1 \text{ mA/V}^2$, $\lambda_D = 0.01 \text{ V}^{-1}$, $V_{THL} = -1.5 \text{ V}$, $K_{nL} = 0.2 \text{ mA/V}^2$ and $\lambda_L = 0.01 \text{ V}^{-1}$.



If the transistors are biased at $i_D = 0.2 \text{ mA}$, then small signal voltage gain A_v is

- (A) -224
- (B) -111.75
- (C) 894
- (D) -894

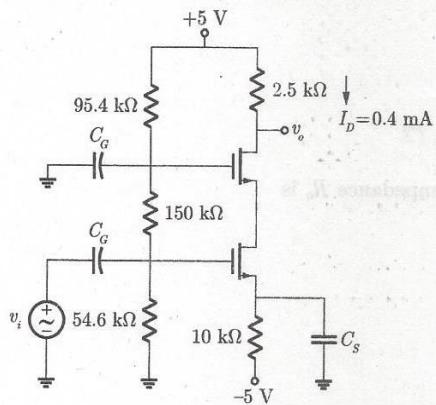
QUESTION 6.74

Consider the cascode circuit shown below. The transistor parameter are:

$$V_{TN1} = V_{TN2} = 1.2 \text{ V}$$

$$K_{n1} = K_{n2} = 0.8 \text{ mA/V}^2$$

$$\lambda_1 = \lambda_2 = 0$$



Given the common drain current for both MOSFETs,

$$I_D = 0.4 \text{ mA}$$

The values of transconductance g_{m1} and g_{m2} for MOS M_1 and MOS M_2 are respectively

- (A) 1.14 mA/V, 0.565 mA/V
- (B) 0.56 mA/V, 0.565 mA/V
- (C) 0.64 mA/V, 0.64 mA/V
- (D) 1.14 mA/V, 1.14 mA/V

Answer

5.1	80.6
5.2	C
5.3	C
5.4	A
5.5	C
5.6	A
5.7	1
5.8	-10
5.9	-10
5.10	5.33
5.11	11.73
5.12	0.4K [^]
5.13	B
5.14	C
5.15	A
5.16	18.57
5.17	33.63
5.18	A
5.19	B
5.20	D
5.21	C
5.22	1.07
5.23	B
5.24	B
5.25	A
5.26	A
5.27	1.33
5.28	-4.25
5.29	1.33
5.30	-4.25
5.31	0.733
5.32	1
5.33	0.66
5.34	C
5.35	B
5.36	D
5.37	A

5.38	D
5.39	C
5.40	D
5.41	C
5.42	-8.01
5.43	C
5.44	B
5.45	A
5.46	A
5.47	-5.76
5.48	B
5.49	1.65
5.50	2.6
5.51	-15.6
5.52	447
5.53	A
5.54	B
5.55	270
5.56	1.13
5.57	493.8
5.58	7.14
5.59	200
5.60	C
5.61	D
5.62	A
5.63	0.477
5.64	D
5.65	A
5.66	A
5.67	0.705
5.68	2.39
5.69	A
5.70	C
5.71	B
5.72	D
5.73	A
5.74	D

CHAPTER 6

OUTPUT STAGES AND POWER AMPLIFIERS

QUESTION 6.1

The output signal power of a power amplifier is several times the input signal power. It is possible because

- (A) a positive feedback exists in the circuit
- (B) a negative feedback is introduced in the circuit
- (C) the circuit converts a part of dc power from the dc supply into ac signal power
- (D) a step-up transformer is used in the circuit

QUESTION 6.2

Conversion efficiency is defined as

- (A) Power dissipated in the load divided by the power dissipated in the output stage of the amplifier.
- (B) Power dissipated in the load divided by the total power supplied by the power supplies.
- (C) Decreasing gain with increasing frequency.
- (D) First increasing and then decreasing gain with increasing frequency

QUESTION 6.3

If the load power is 3 mW and the dc power is 150 mW, the efficiency is

- (A) 0%
- (B) 2%
- (C) 3%
- (D) 20%

QUESTION 6.4

A power BJT operating at a high current density, $I_E = 5 \text{ A}$ is found to have a base current of 0.2 A and a base-input resistance of 0.72Ω .

The base spreading resistance is

- (A) 0.125Ω
- (B) 0.72Ω
- (C) 0.595Ω
- (D) 0.835Ω

QUESTION 6.5

In which of the following amplifier classes, the active device operates for the whole of the input signal cycle?

- (A) Class A
- (B) Class AB
- (C) Class B
- (D) Class C

QUESTION 6.6

The feedback in emitter follower circuit is

- (A) 50%
- (B) 100%
- (C) 0%
- (D) 0.1%

QUESTION 6.7

Which of the following best describes a class A amplifier ?

- (A) High efficiency and high distortion
- (B) Low efficiency and high distortion
- (C) Low efficiency and low distortion
- (D) High efficiency and low distortion

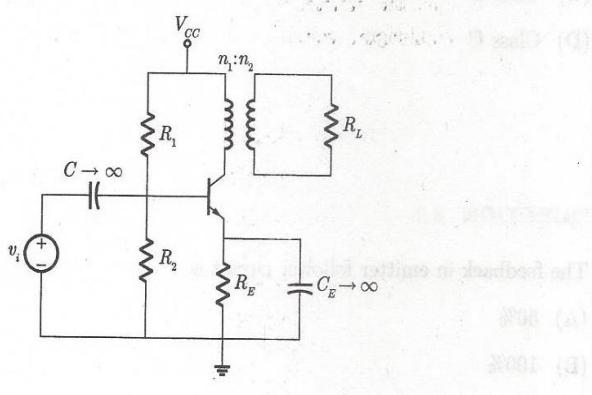
A class A common-emitter circuit is an application of the two Q-point rule. A class A amplifier need a small of bias at the output.

The collector circuit efficiency of a single-ended class-A power amplifier can never be

- (A) 20%
- (B) 30%
- (C) 40%
- (D) 50%

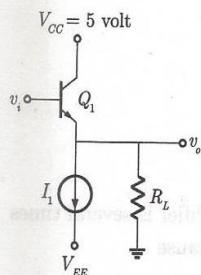
QUESTION 6.9

The parameters for the transformer-coupled common-emitter circuit shown in figure are $V_{CC} = 36$ V and $n_1 : n_2 = 4 : 1$. If the signal power delivered to the load is 2 W, what will be the rms voltage across the load ?



QUESTION 6.10

Consider the emitter follower shown in figure. We wish to deliver a power of 0.5 W to $R_L = 8 \Omega$. (Assume $V_{BE(ON)} \approx 800$ mV)

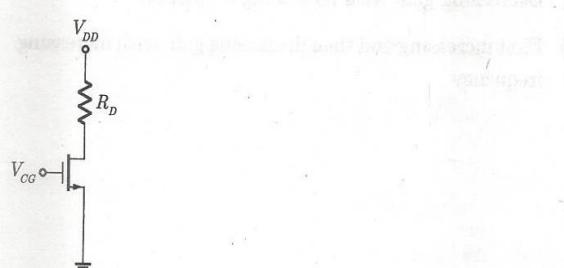


The value of I_1 for a small-signal voltage gain of 0.8 will be

- (A) 40 mA
- (B) 5 mA
- (C) 18 mA
- (D) 13 mA

QUESTION 6.11

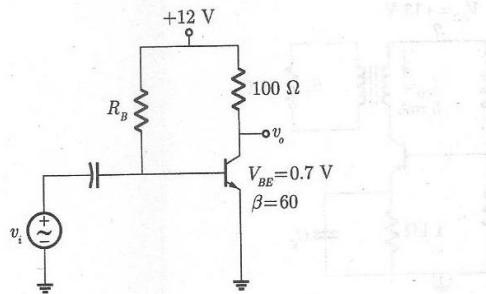
Consider the common-source circuit shown in figure below. The maximum current, voltage and power ratings of the power transistor are: 5 A, 80 V and 25 W, respectively. If $V_{DD} = 80$ V, what will be the value of R_D ?



Volt

QUESTION 6.12

Consider the class A power amplifier circuit given below.

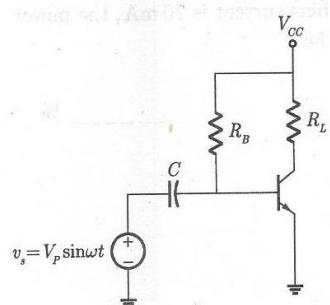


What is the value of R_B that locates the Q -point at the centre of the load line?

_____ kΩ

QUESTION 6.13

The common-emitter circuit shown in figure below is biased at $V_{CC} = 24$ V. The maximum transistor power is $P_{D,\max} = 20$ W and the current gain is $\beta = 80$.

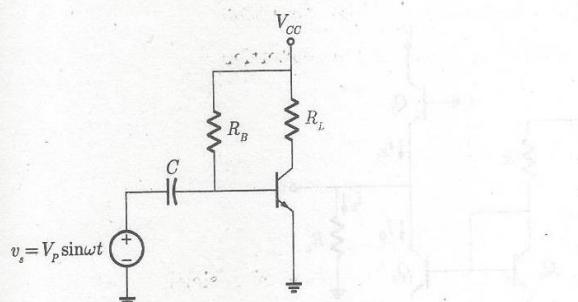


What will be the values of R_B and base current I_B such that the maximum power is delivered to the load R_L ?

- | | |
|---------------|---------------|
| R_B (in kΩ) | I_B (in mA) |
| (A) 20.8 | 1.12 |
| (B) 1.12 | 20.8 |
| (C) 7.2 | 20.8 |
| (D) 1.12 | 7.2 |

QUESTION 6.14

For the transistor in the common-emitter circuit shown in figure below, the parameters are: $\beta = 100$, $P_{D,\max} = 2.5$ W, $V_{CE(\text{sat})} = 25$ V and $I_{C,\max} = 500$ mA.

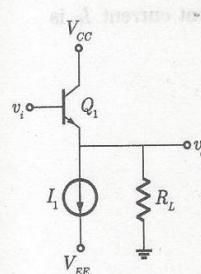


Let $R_L = 100$ Ω. What are the required values of V_{CC} and R_B that delivers the maximum power to the load?

V_{CC} (in V)	R_B (in kΩ)
(A) 20.8	25
(B) 19.4	25
(C) 25	19.4
(D) 19.4	20.8

QUESTION 6.15

A student designs the emitter follower as shown in figure below for a small-signal voltage gain of 0.7 and a load resistance of 4 Ω.

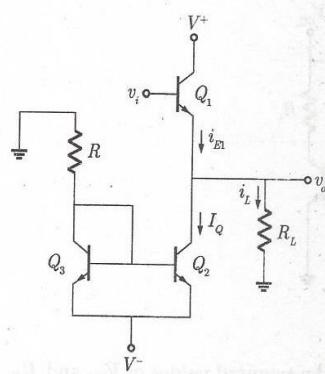


For a sinusoidal input, what is the maximum average power that can be delivered to the load, R_L without turning Q_1 off?

_____ Watt

QUESTION 6.16

The circuit parameters for the class-A emitter follower shown in figure below are: $V^+ = 12 \text{ V}$, $V^- = -12 \text{ V}$ and $R_L = 100 \Omega$. The transistor parameters are : $\beta = 200$, $V_{BE} = 0.7 \text{ V}$ and $V_{CE(\text{sat})} = 0.2 \text{ V}$.

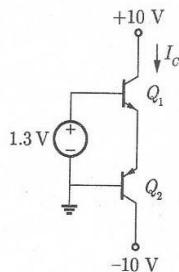


If the output voltage is to vary between $+10 \text{ V}$ and -10 V , what are the minimum required values of I_Q and R ?

$I_Q(\text{min})$ (in mA)	R (in Ω)
(A) 113	100
(B) 100	113
(C) 10	11.3
(D) 11.3	10

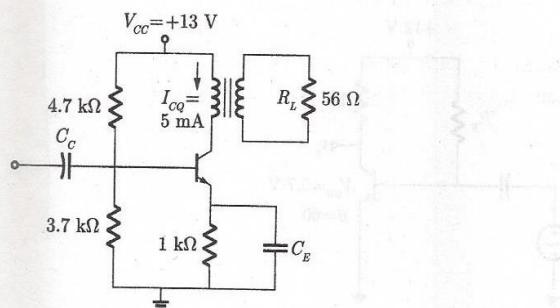
QUESTION 6.17

Consider the case AB stage amplifier shown in figure with $V_{\text{thermal}} = 25 \text{ mV}$. If both transistors have reverse saturation current $I_S = 10^{-15} \text{ A}$, the value of Quiescent current I_C is



QUESTION 6.18

Consider the circuit class A amplifier shown in figure below.



If transformer has an 80% efficiency, then the maximum efficiency of the class A amplifier is

- (A) 50%
- (B) 33.33%
- (C) 24.6%
- (D) 78.6%

QUESTION 6.19

An emitter follower delivers a peak swing of 0.5 V to an 8Ω load with $V_{CC} = 2 \text{ V}$. If the bias current is 70 mA , the power efficiency of the circuit will be

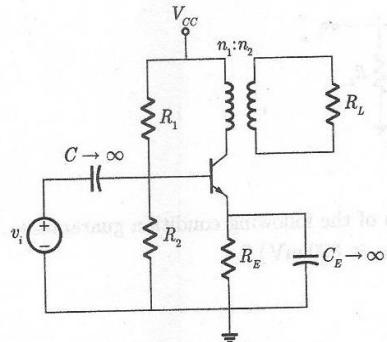
QUESTION 6.20

What is the basic meaning of total harmonic distortion ?

- (A) The nonlinearity that arises due to non-constant gain of the amplifier.
- (B) The amount of power that appears in the harmonic components as a percentage of the power appearing in the fundamental.
- (C) The amount of crossover distortion.
- (D) The sum of the voltages of the harmonics divided by the voltage of the harmonic.

QUESTION 6.21

Consider the transformer-coupled common-emitter circuit shown in figure. The parameters are: $V_{CC} = 10\text{ V}$, $R_L = 8\Omega$, $n_1:n_2 = 3:1$, $R_1 = 0.73\text{ k}\Omega$, $R_2 = 1.55\text{ k}\Omega$ and $R_E = 20\Omega$. The transistor parameters are $\beta = 25$ and $V_{BE(on)} = 0.7\text{ V}$. The amplitude of the sinusoidal input voltage is 17 mV.

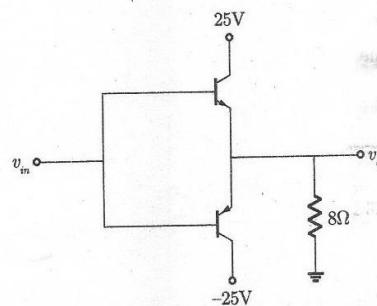


What will be the ac power delivered to the load ?

_____ mW

QUESTION 6.22

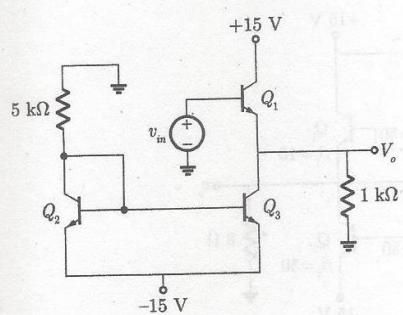
The circuit of a class B push-pull amplifier is shown in Fig. If the peak output voltage, V_o is 16 V, the power drawn from the dc source would be



- (A) 10 W
- (B) 16 W
- (C) 20 W
- (D) 32 W

QUESTION 6.23

Consider the class-A emitter follower shown in figure. All the transistors are identical. Assume that $V_{BE} = 0.7\text{ V}$ in the active region and that $V_{CEsat} = 0.2\text{ V}$.



What is the maximum and minimum output voltage V_o for which Q_1 remains in the active region.

- (A) $V_{o(max)} = 14.8\text{ V}$, $V_{o(min)} = -2.86\text{ V}$
- (B) $V_{o(max)} = 14.8\text{ V}$, $V_{o(min)} = 0\text{ V}$
- (C) $V_{o(max)} = 2.86\text{ V}$, $V_{o(min)} = 0\text{ V}$
- (D) $V_{o(max)} = 2.86\text{ V}$, $V_{o(min)} = -2.86\text{ V}$

QUESTION 6.24

Which of the following amplifier class suffers mainly from the problem of crossover distortion ?

- (A) Class A
- (B) Class B
- (C) Class AB
- (D) Class C

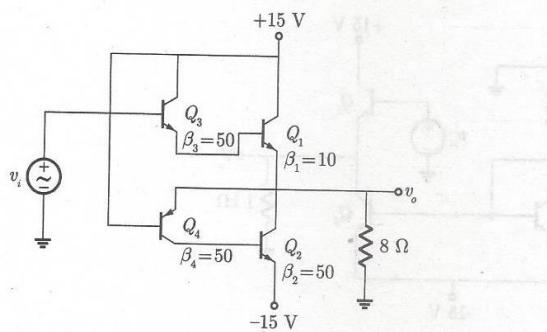
QUESTION 6.25

The probable cause for harmonic distortion in a two-stage RC -coupled amplifier is

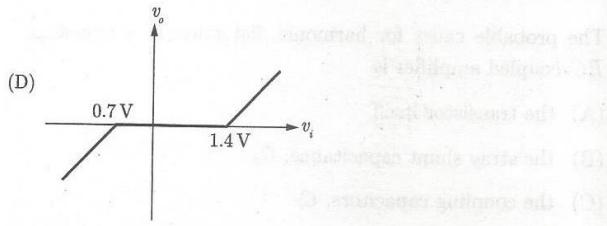
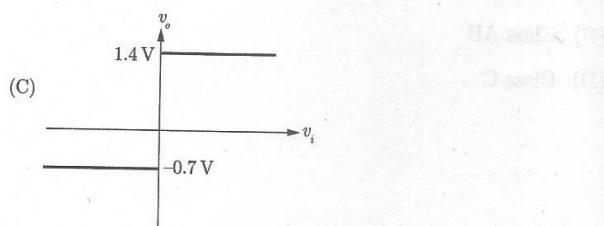
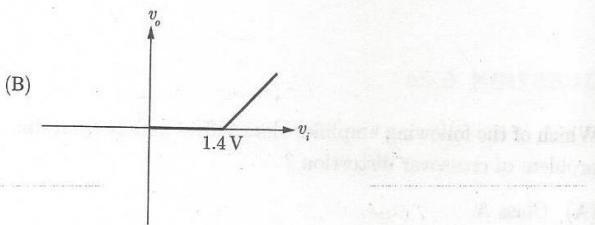
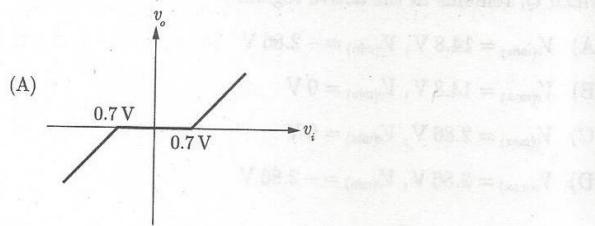
- (A) the transistor itself
- (B) the stray shunt capacitance, C_{sh}
- (C) the coupling capacitors, C_C
- (D) the biasing resistors

QUESTION 6.26

Consider the class-B output stage shown in figure below. For the transistor, assume the $V_{BE} = 0.7$ V in the active and $V_{CE(sat)} = 0.2$ for saturation.

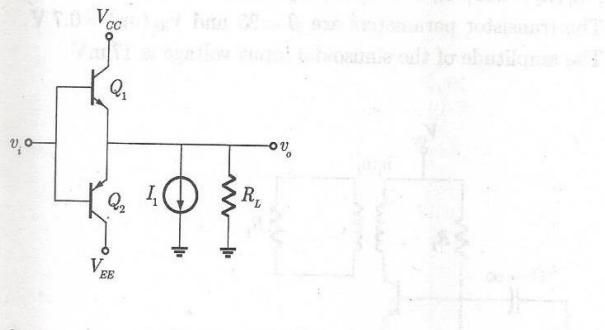


The transfer characteristic (v_o versus v_i) for the circuit is



QUESTION 6.27

Consider the push-pull stage depicted in figure, where a current source, I_1 , is tied from the output node to ground.

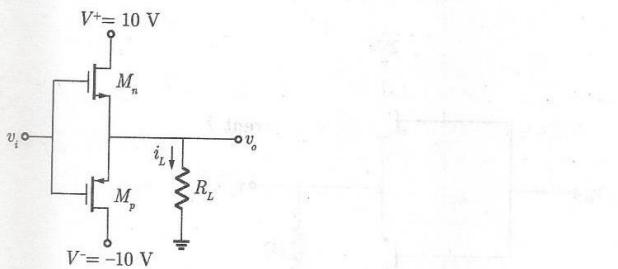


Suppose $v_i = 0$. Which of the following condition guarantees that Q_1 is ON (i.e., $V_{BE1} \approx 800$ mV) ?

- (A) $I_1 R_L \geq 800$ mV
- (B) $I_1 R_L < 800$ mV
- (C) $\frac{I}{R_L} \geq 800$ mV
- (D) $\frac{I}{R_L} < 800$ mV

QUESTION 6.28

Consider the class-B output stage with complementary MOSFETs shown in figure below. The transistor parameters are $V_{TN} = V_{TP} = 0$ and $K_n = K_p = 0.4$ mA/V². Let $R_L = 5$ kΩ

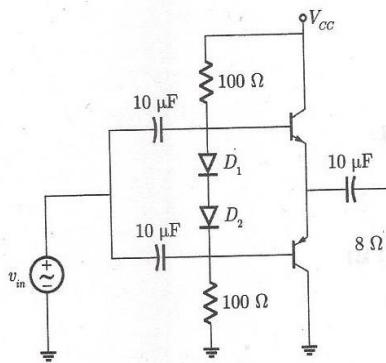


What is the maximum output voltage such that M_n remains biased in the saturation region ?

- (A) 8 V
- (B) 10.25 V
- (C) 12.5 V
- (D) 20.5 V

QUESTION 6.29

Consider the circuit shown in figure below.



The maximum ac output power and the dc input power of the amplifier are respectively

- (A) 12.5 W, 15.5 W
- (B) 3.25 W, 7.96 W
- (C) 6.25 W, 3.25 W
- (D) 6.25 W, 7.96 W

QUESTION 6.30

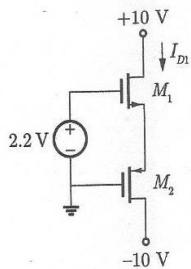
Consider the class-AB stage shown below. The transistor parameters are

$$K_p = 300 \mu\text{A/V}^2 = K_n$$

$$V_{TN} = 0.75 \text{ V}$$

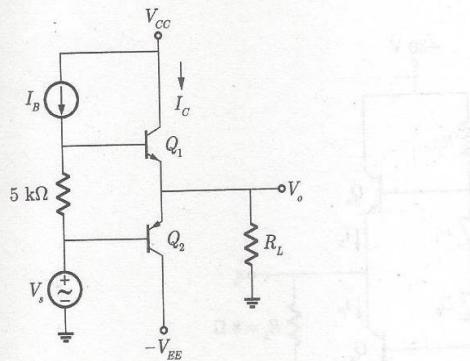
$$V_{TP} = -0.75 \text{ V}$$

What is the value of quiescent current I_{DQ} ?



QUESTION 6.31

Consider the class-AB stage amplifier shown in figure having $V_{\text{thermal}} = 25 \text{ mV}$.



For the *npn* transistor, $I_S = 10^{-15} \text{ A}$, and for *pnp* transistor $I_S = 10^{-16} \text{ A}$. Assume that β_F is very large and output voltage is $v_o = 0 \text{ V}$. If $I_B = 250 \mu\text{A}$, what is the value of quiescent current I_{CQ} ?

$$\text{_____ } \mu\text{A}$$

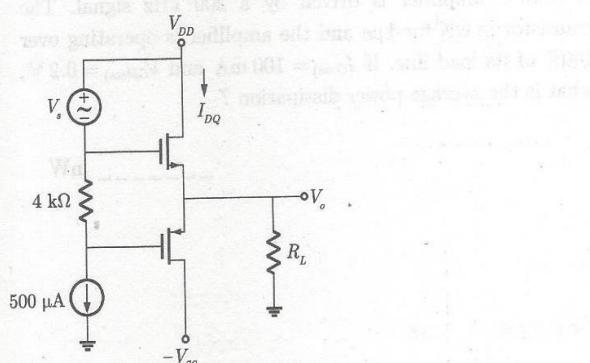
QUESTION 6.32

Consider the circuit of class AB stage amplifier shown in figure below. The transistor parameters are:

$$V_{TN} = 0.75 \text{ V}, V_{TP} = -0.75 \text{ V}$$

$$K_n = 250 \mu\text{A/V}^2, K_p = 100 \mu\text{A/V}^2$$

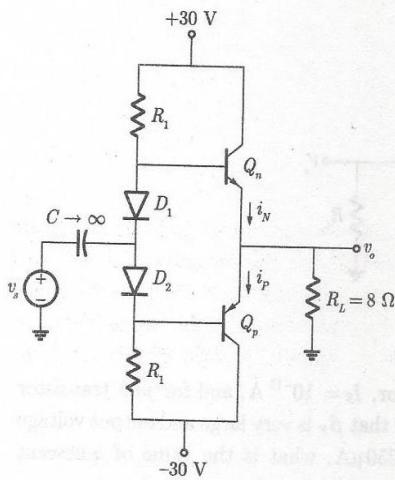
What is the value of Quiescent current I_D ?



$$\text{_____ } \mu\text{A}$$

QUESTION 6.33

Consider the class-AB output stage shown in figure below. The diodes and transistors are matched with parameters $I_S = 6 \times 10^{-12} \text{ A}$ and $\beta = 40$.



At $v_o = 24 \text{ V}$, if the minimum current in the diodes D_1 and D_2 is 25 mA, what will be the value of R_1 ?

- (A) 18.52Ω
- (B) 98.2Ω
- (C) 53.97Ω
- (D) 5.3Ω

QUESTION 6.34

A class-C amplifier is driven by a 200 kHz signal. The transistor is ON for $1\mu\text{s}$ and the amplifier is operating over 100% of its load line. If $I_{Q(\text{sat})} = 100 \text{ mA}$ and $V_{CE(\text{sat})} = 0.2 \text{ V}$, what is the average power dissipation?

----- mW

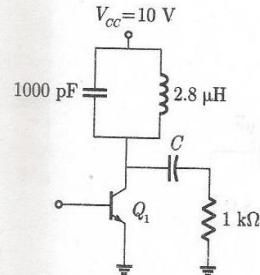
QUESTION 6.35

A push-pull stage operating from $V_{CC} = 3 \text{ V}$ delivers a power of 0.2 W to an 8Ω load. The efficiency of the circuit is

----- %

QUESTION 6.36

Consider the basic class C amplifier circuit shown in figure having $V_{CE(\text{sat})} = 0.3 \text{ V}$.



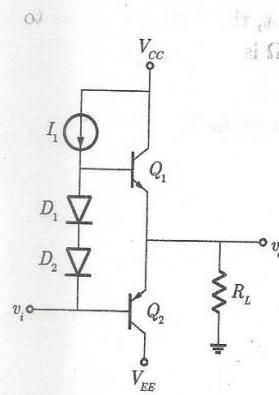
What is the value of ac output power?

- (A) 47 mW
- (B) 23.5 mW
- (C) 94 mW
- (D) 50 mW

QUESTION 6.37

Consider the output stage shown in figure. Assume I_1 is an ideal current source and the load resistance, $R_L = 8 \Omega$. If the output must achieve a small-signal voltage gain of 0.8, what is the required bias current of Q_1 and Q_2 ?

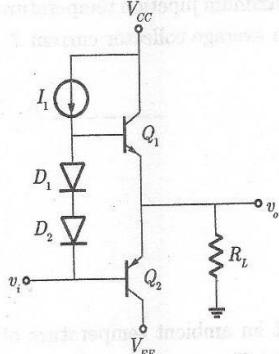
(Neglect the incremental resistance of diodes D_1 and D_2)



----- mA

QUESTION 6.38

Consider the output stage depicted in figure.

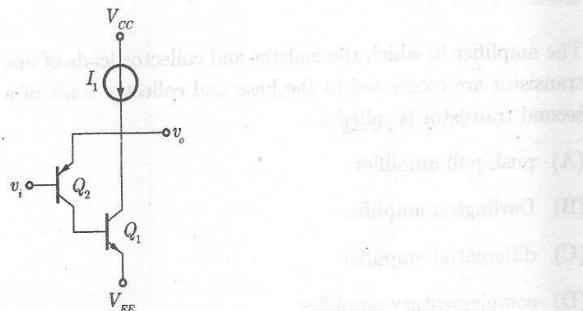


Assume that I_1 is an ideal current source. The small-signal voltage gain is (Neglect the incremental resistance of diodes D_1 and D_2)

- (A) $\frac{g_{m1}R_L}{g_{m2}}$
- (B) $\frac{R_L}{(g_{m1} + g_{m2})}$
- (C) $(g_{m1} + g_{m2})R_L$
- (D) $\frac{(g_{m1} + g_{m2})}{R_L}$

QUESTION 6.39

Consider the composite stage shown in figure. Assume $\beta_1 = 40$ and $\beta_2 = 50$. In the circuit, the value of I_1 so as to obtain an output impedance of 1Ω is



QUESTION 6.40

A push-pull stage is designed to deliver a peak swing of V_p to a load resistance of R_L . What is the efficiency, if the circuit delivers a swing of only $V_p/2$?

QUESTION 6.41

The principal harmonic in a certain 15 kHz signal having a 10 V peak fundamental are the second and fourth. All other harmonics are negligible small. If the total harmonic distortion is 12% and the amplitude of the second harmonic is 0.5 V peak, what is the amplitude of the 60 kHz harmonic ?

Volt

QUESTION 6.42

A signal may have frequency components which lie in the range of 0.001 Hz to 10 Hz. Which one of the following types of couplings should be chosen in a multistage amplifier designed to amplify this signal ?

- (A) RC coupling
- (B) Transformer coupling
- (C) Direct coupling
- (D) Double-tuned transformer

QUESTION 6.43

Negative feedback in amplifiers

- (A) lowers its lower cut-off frequency
- (B) raises its upper cut-off frequency
- (C) increases the bandwidth
- (D) all the above

mA

QUESTION 6.44

Heat sinks reduce

- (A) the transistor power
- (B) the ambient temperature
- (C) the collector current
- (D) the junction temperature

QUESTION 6.45

A BJT must dissipate 25 W of power. The maximum junction temperature is $T_{j,\max} = 200^\circ\text{C}$, the ambient temperature is 25°C and the device-to-case thermal resistance is 3°C/W . What will be the maximum permissible thermal resistance between the case and ambient ?

$$\text{----- } ^\circ\text{C/W}$$

QUESTION 6.46

A BJT has a rated power of 15 W and a maximum junction temperature of 175°C . The ambient temperature is 25°C and the thermal resistance parameters are: $\theta_{\text{sink-amb}} = 4^\circ\text{C/W}$ and $\theta_{\text{case-snk}} = 1^\circ\text{C/W}$. The actual power (in watts) that can be safely dissipated in the transistor is

$$\text{----- Watt}$$

QUESTION 6.47

The power rating of a transistor can be increased by

- (A) raising the temperature
- (B) using a heat sink
- (C) using class-A operation
- (D) operating with no input signal

QUESTION 6.48

A transistor having a thermal resistance $Q_{JA} = 2^\circ\text{C/W}$ is operating at an ambient temperature of 30°C with a collector-emitter voltage of 20 V. If the maximum junction temperature is 130°C , what is the maximum average collector current ?

$$\text{----- A}$$

QUESTION 6.49

A power transistor operating at an ambient temperature of 50°C , dissipates power of 30 W. The thermal resistance of the transistor is 3°C/W . What is the maximum junction temperature ?

$$\text{----- } ^\circ\text{C}$$

QUESTION 6.50

A power transistor for which $T_{j,\max} = 180^\circ\text{C}$ can dissipate 50 W at a case temperature of 50°C if it is connected to a heat sink using an insulating washer for which the thermal resistance is 0.6°C/W . What is heat sink temperature necessary for safe operation at 30 W ?

$$\text{----- } ^\circ\text{C}$$

QUESTION 6.51

The amplifier in which the emitter and collector leads of one transistor are connected to the base and collector leads of a second transistor is called a

- (A) push-pull amplifier
- (B) Darlington amplifier
- (C) differential amplifier
- (D) complementary amplifier

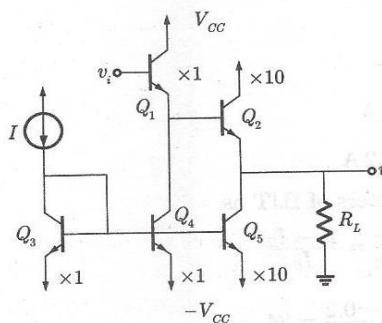
QUESTION 6.52

The follower design shown is intended to provide a relatively high input resistance. Assume $V_{CC} = 5\text{ V}$, $V_{EB} = 0.7\text{ V}$, $V_{CE\text{sat}} = 0.2\text{ V}$ (Note the transistor sizing indicated by the notation $\times n$)

- (B) $Q_1(184\text{ }\mu\text{A}, 7.85\text{ V}), Q_2(325\text{ }\mu\text{A}, 7.16\text{ A})$

- (C) $Q_1(325\text{ }\mu\text{A}, 6.04\text{ V}), Q_2(184\text{ }\mu\text{A}, 7.85\text{ V})$

- (D) $Q_1(184\text{ }\mu\text{A}, 6.04\text{ V}), Q_2(186\text{ }\mu\text{A}, 7.85\text{ V})$

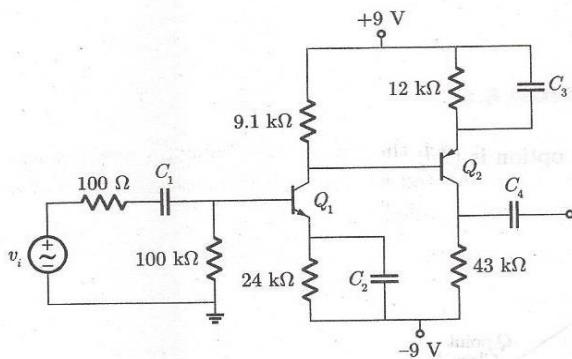


What is the largest possible unclipped zero-average sine wave output?

- (A) 9 V
 (B) 4.1 V
 (C) 5.9 V
 (D) 0.9 V

QUESTION 6.53

Consider the direct coupled amplifier shown in figure.



What are the values of Q -points of the transistors Q_1 and Q_2 ?

- (A) $Q_1(325\text{ }\mu\text{A}, 7.16\text{ V}), Q_2(184\text{ }\mu\text{A}, 7.85\text{ V})$

Answer

6.1	
6.2	
6.3	
6.4	
6.5	
6.6	B
6.7	C
6.8	D
6.9	6.36
6.10	D
6.11	64
6.12	11.3
6.13	B
6.14	C
6.15	0.45
6.16	B
6.17	196
6.18	C
6.19	5.6
6.20	B
6.21	345mW
6.22	B
6.23	A
6.24	B
6.25	A
6.26	D
6.27	A

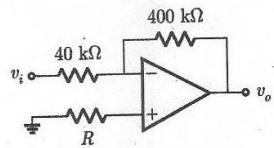
6.28	A
6.29	D
6.30	36.8
6.31	22.8
6.32	9.38
6.33	C
6.34	4
6.35	46.8
6.36	A
6.37	1.3
6.38	C
6.39	24.6
6.40	39
6.41	1.091
6.42	C
6.43	D
6.44	D
6.45	4
6.46	10
6.47	B
6.48	2.5
6.49	140
6.50	84
6.51	B
6.52	B
6.53	A

CHAPTER 7

OP-AMP CHARACTERISTICS AND BASIC CIRCUITS

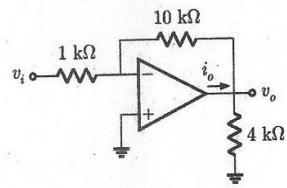
QUESTION 7.1

For the circuit shown below the value of $A_v = \frac{v_o}{v_i}$ is



QUESTION 7.2

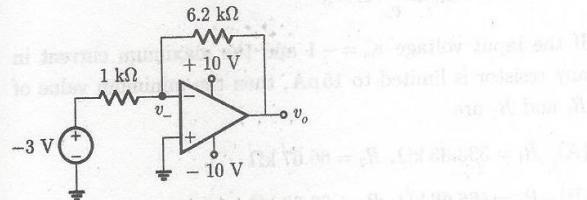
The input to the circuit shown below is $v_i = 2 \sin \omega t$ mV. The current i_o is



- (A) $-2 \sin \omega t$ μA
- (B) $-7 \sin \omega t$ μA
- (C) $-5 \sin \omega t$ μA
- (D) 0

QUESTION 7.3

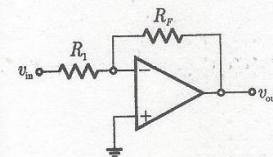
In following amplifier circuit, the op-amp is ideal. The voltage v_- at inverting terminal is



- (A) 0 V
- (B) -1.2 V
- (C) -3 V
- (D) 2.1 V

QUESTION 7.4

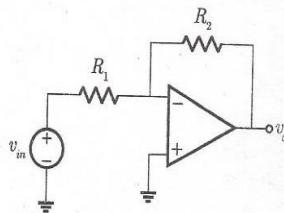
Consider the inverting amplifier, using an ideal operational amplifier shown in the figure. The designer wishes to realize the input resistance seen by the small-signal source to be as large as possible, while keeping the voltage gain between -10 and -25. The upper limit on R_F is 1 MΩ. The value of R_1 should be



- (A) Infinity
- (B) 1 MΩ
- (C) 100 kΩ
- (D) 40 kΩ

QUESTION 7.5

Consider the op-amp circuit shown below.



The closed loop voltage gain is

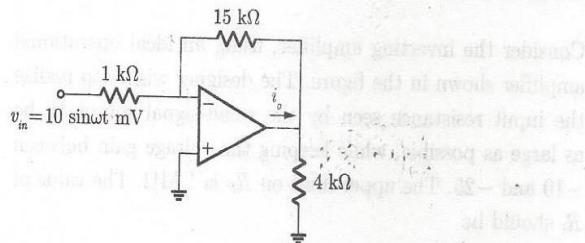
$$A_v = \frac{v_o}{v_{in}} = -8$$

If the input voltage $v_{in} = -1$ and the maximum current in any resistor is limited to $15\text{ }\mu\text{A}$, then the minimum value of R_1 and R_2 are

- (A) $R_1 = 533.33\text{ k}\Omega$, $R_2 = 66.67\text{ k}\Omega$
- (B) $R_1 = 466.69\text{ k}\Omega$, $R_2 = 66.67\text{ k}\Omega$
- (C) $R_1 = 66.67\text{ k}\Omega$, $R_2 = 533.33\text{ k}\Omega$
- (D) $R_1 = 66.67\text{ k}\Omega$, $R_2 = 466.69\text{ k}\Omega$

QUESTION 7.6

Consider the circuit shown in below

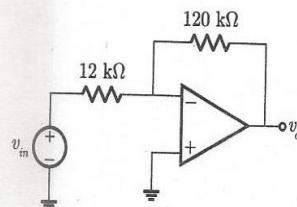


What is the value of current i_o ?

- (A) $-27.5 \sin \omega t \mu\text{A}$
- (B) $-47.5 \sin \omega t \mu\text{A}$
- (C) $-37.5 \sin \omega t \mu\text{A}$
- (D) None of the above

QUESTION 7.7

Consider the amplifier circuit shown in figure below. The op-amp is ideal.

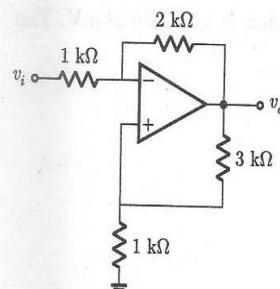


What is the value of input and output resistance?

- (A) $120\text{ k}\Omega$, $0\text{ k}\Omega$
- (B) $12\text{ k}\Omega$, $\infty\text{ k}\Omega$
- (C) $12\text{ k}\Omega$, $0\text{ k}\Omega$
- (D) $132\text{ k}\Omega$, $\infty\text{ k}\Omega$

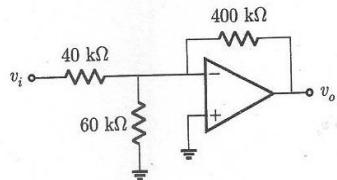
QUESTION 7.8

For the circuit shown below the value of $A_v = \frac{v_o}{v_i}$ is



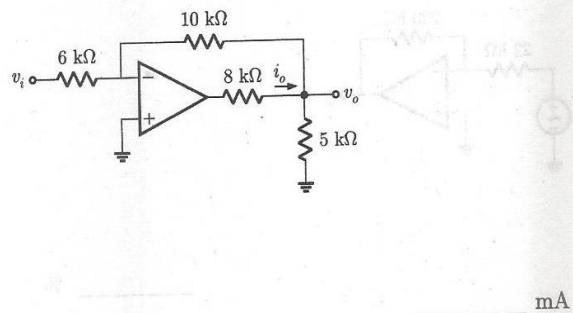
QUESTION 7.9

For the circuit shown below the value of $A_v = \frac{v_o}{v_i}$ is



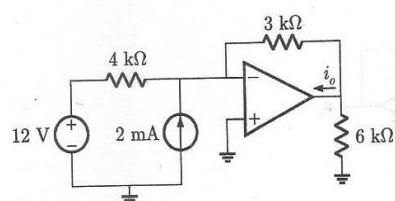
QUESTION 7.10

For the circuit shown below the input voltage v_i is 1.5 V. The current i_o is



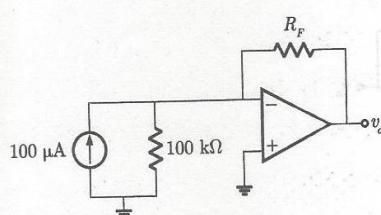
QUESTION 7.11

For the circuit shown below the value of i_o is



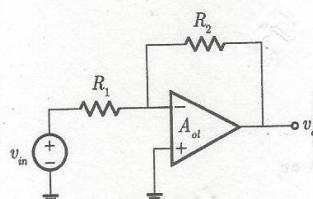
QUESTION 7.12

For the circuit shown below, if the output voltage $v_o = -10$ V, then the value of resistor R_F is



QUESTION 7.13

Consider an ideal op-amp circuit shown in following figure. If open loop gain of op-amp is A_{ol} , then closed loop voltage gain A_v is



$$(A) \frac{-R_2}{R_1} \frac{1}{\left[1 + \frac{1}{A_{ol}} \left(1 + \frac{R_2}{R_1}\right)\right]}$$

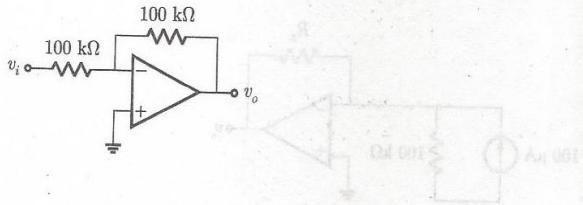
$$(B) \frac{A_{ol}}{1 + \frac{A_{ol}}{\left(1 + \frac{R_2}{R_1}\right)}}$$

$$(C) \frac{-R_2}{R_1} \frac{1}{\left[1 + A_{ol} \frac{R_2}{R_1}\right]}$$

$$(D) \frac{A_{ol}}{\left(1 + \frac{R_2}{R_1}\right)}$$

QUESTION 7.14

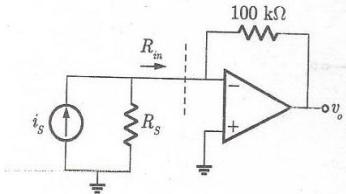
For the op-amp shown below open loop differential gain is $A_{od} = 10^3$. The output voltage v_o for $v_i = 2 \text{ V}$ is



- (A) -1.996
- (B) -1.998
- (C) -2.004
- (D) -2.006

QUESTION 7.15

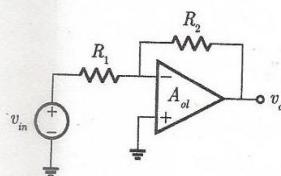
Consider an op-amp circuit shown in figure below, having an open loop gain of $A_{ol} = 10^5$. The value of input resistance R_{in} is



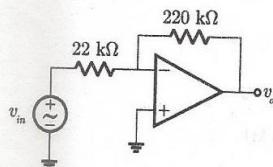
- (A) $100 \text{ k}\Omega$
- (B) 0.979
- (C) 0.999Ω
- (D) Can't determined+

QUESTION 7.16

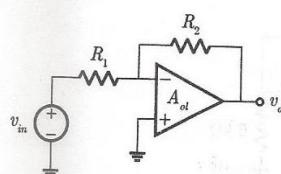
An inverting amplifier shown in figure is designed to provide a voltage gain of 8 and gain error of 0.2%, then minimum required open loop gain of op-amp is

**QUESTION 7.17**

In the following inverting amplifier shown in figure, op-amp has an open loop gain of 92 dB, gain error of amplifier is

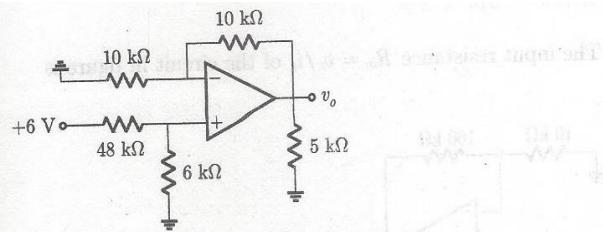
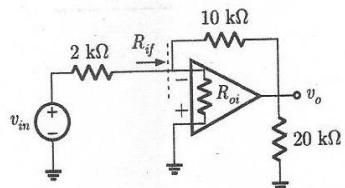
**QUESTION 7.18**

An inverting amplifier shown in figure, has an open gain of 1000 and closed loop gain of 4, gain error is



QUESTION 7.19

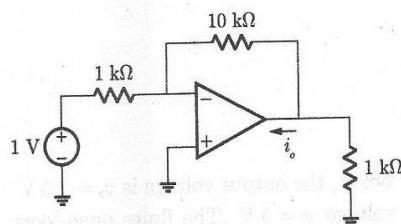
Consider an op-amp circuit shown in figure, with an open loop gain of $A_{ol} = 10^5$ and open loop input impedance $R_{oi} = 10 \text{ k}\Omega$. If output resistance of op-amp is zero, then closed loop input impedance (R_{if}) at the inverting terminal of op-amp is



- (A) $R_{if} = 10 \text{ k}\Omega$
- (B) $R_{if} = 1 \Omega$
- (C) $R_{if} = 40 \text{ k}\Omega$
- (D) $R_{if} = 0.1 \Omega$

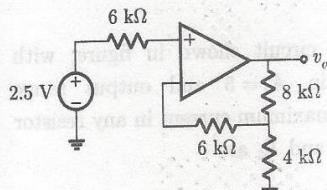
QUESTION 7.20

An inverting amplifier is shown in figure below. Assume op-amp is ideal. What is the value of current i_o ?



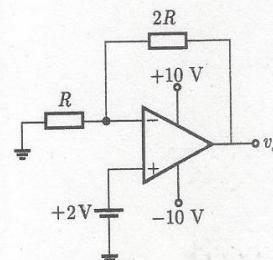
QUESTION 7.22

For the circuit shown below the value of v_o is



QUESTION 7.23

Given that the op-amp is ideal. The output voltage v_o is



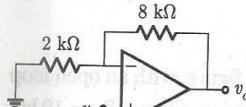
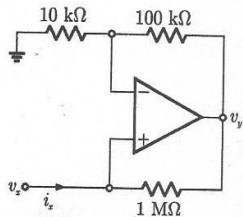
QUESTION 7.24

For the circuit shown below the value of v_o is

(A) 10 V
(B) 8 V
(C) 6 V
(D) 4 V

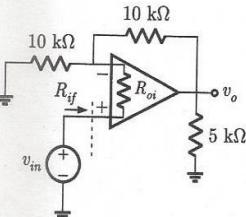
QUESTION 7.24

The input resistance $R_{in} = v_x/i_x$ of the circuit in figure is



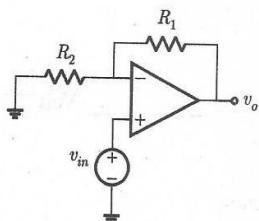
QUESTION 7.27

In the following op-amp circuit, given that open loop voltage gain $A_{ol} = 10^5$ and open loop input impedance $R_{oi} = 10 \text{ k}\Omega$. If output resistance of op-amp is zero then closed loop input impedance at non-inverting terminal of op-amp is



QUESTION 7.25

Consider an ideal op-amp circuit shown in figure, with a closed loop voltage gain $A_v = 5$ and output range $-10 \text{ V} \leq v_o \leq 10 \text{ V}$. If the maximum current in any resistor is limited to $50 \mu\text{A}$, then R_1 and R_2 are



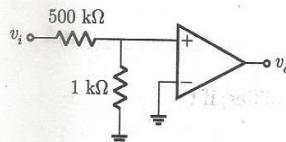
- (A) $R_1 = 40 \text{ k}\Omega$ and $R_2 = 200 \text{ k}\Omega$
- (B) $R_1 = 160 \text{ k}\Omega$ and $R_2 = 40 \text{ k}\Omega$
- (C) $R_1 = 200 \text{ k}\Omega$ and $R_2 = 40 \text{ k}\Omega$
- (D) $R_1 = 40 \text{ k}\Omega$ and $R_2 = 160 \text{ k}\Omega$

QUESTION 7.26

QUESTION 7.26

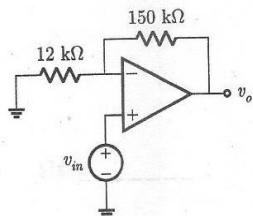
The op-amp shown below has a very poor open-loop voltage gain of 45 but is otherwise ideal. The closed-loop gain of amplifier is

- (A) 5×10^4
- (B) 250.5
- (C) 2×10^4
- (D) 501



QUESTION 7.20

In the following non-inverting amplifier, the op-amp has an open loop gain of 86 dB, gain error is



- (A) 0.0125%
- (B) 0.13%
- (C) 0.930%
- (D) 0.0675%

(A) 1.5×10^5

(B) 1

(C) 0.999

(D) 0.987

QUESTION 7.30

A voltage follower is built using an op-amp whose open loop gain is A_o , gain error is

- (A) $\frac{A_o}{1 + A_o}$
- (B) $\frac{1}{1 + A_o}$
- (C) $\frac{1 + A_o}{A_o}$
- (D) None of these

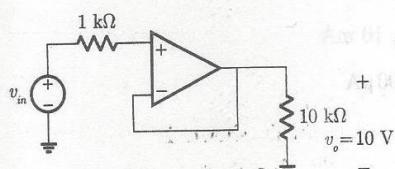
QUESTION 7.32

In the circuit shown below, the op-amp parameters are:

Input resistance $R_{id} = 100 \text{ k}\Omega$

Open loop gain $A = 10^5$

Output resistance $R_o = 100 \Omega$

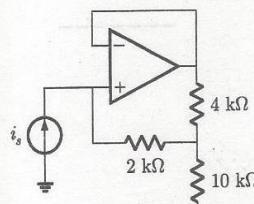


If the op-amp input current is neglected, what is the value of v_{in} ?

- (A) $10.1 \times 10^{-5} \text{ V}$
- (B) 0.999 V
- (C) 10.0001 V
- (D) $9.999 \times 10^{-5} \text{ V}$

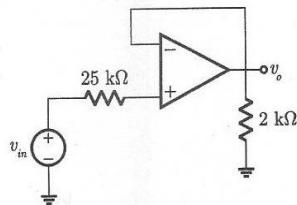
QUESTION 7.33

For the circuit shown below what is the input resistance?



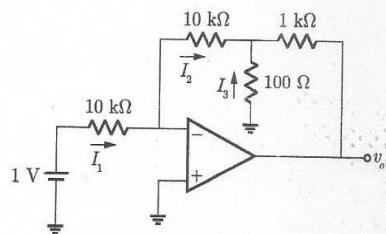
QUESTION 7.31

In the following non-inverting amplifier, if the op-amp has an open loop gain 1.5×10^5 , then close loop gain of op-amp is



QUESTION 7.34

In the following amplifier circuit, the op-amp is ideal.

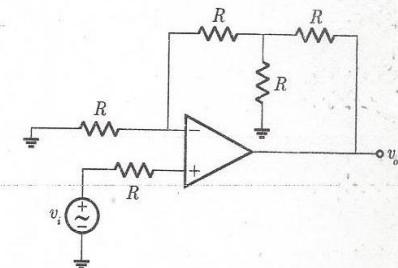


What is the value of current I_1 , I_2 and I_3 respectively?

- (A) 10 mA, 1 μA, 100 μA
- (B) 100 μA, 100 μA, 1 μA
- (C) 100 μA, 100 μA, 10 mA
- (D) 10 mA, 1 μA, 100 μA

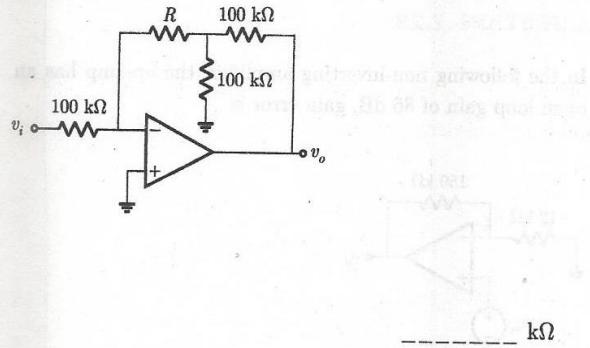
QUESTION 7.35

For the circuit shown below the value of $A_v = \frac{v_o}{v_i}$ is



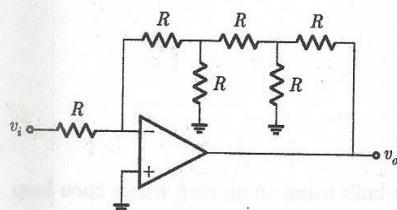
QUESTION 7.36

For the circuit shown below, gain is $A_v = v_o/v_i = -10$. The value of R is



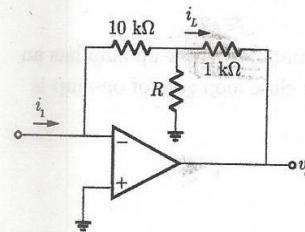
QUESTION 7.37

For the op-amp circuit shown below the voltage gain $A_v = v_o/v_i$ is



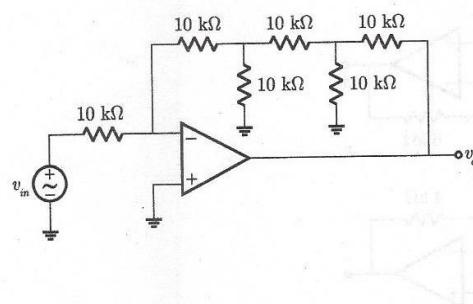
QUESTION 7.38

In the following amplifier circuit, the op-amp is ideal. If current gain $A_i = \frac{i_L}{i_i} = 20$, then the value of resistor R



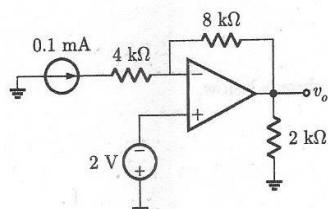
QUESTION 7.39

Consider the amplifier circuit shown below. Assume that op-amp is ideal. What is the value of voltage gain $A_v = \frac{v_o}{v_{in}}$?



QUESTION 7.40

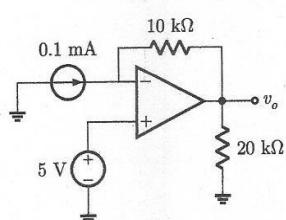
For the circuit shown below, the value of v_o is



Volt

QUESTION 7.41

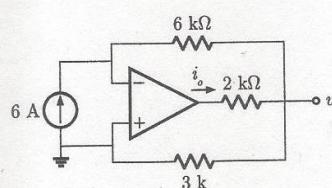
For the circuit shown below the value of v_o is



Volt

QUESTION 7.42

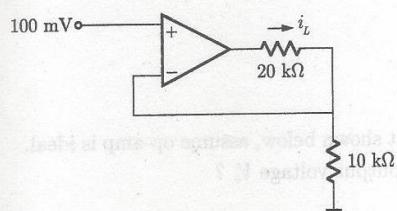
For the circuit shown below, the value of i_o is



Amp

QUESTION 7.43

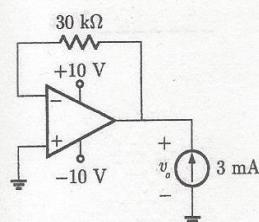
In the circuit shown below, the op-amp is ideal. What is the value of current i_L ?



µA

QUESTION 7.44

In the circuit shown in figure below, assume op-amp is ideal.

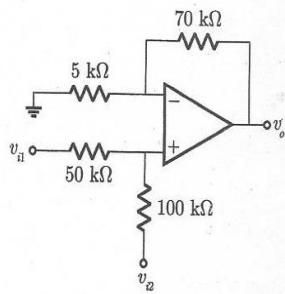


What is the value of output voltage v_o ?

Volt

QUESTION 7.45

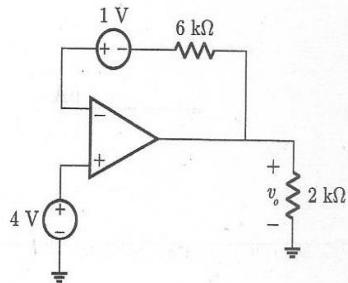
For the circuit shown below, the value of output voltage v_o is



- (A) $v_o = 10v_{i1} + 5v_{i2}$
- (B) $v_o = 5v_{i1} + 10v_{i2}$
- (C) $v_o = v_{i1} + v_{i2}$
- (D) $v_o = 15(v_{i2} - v_{i1})$

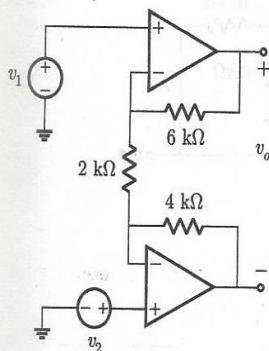
QUESTION 7.46

In the following circuit shown below, assume op-amp is ideal. What is the value of output voltage V_o ?



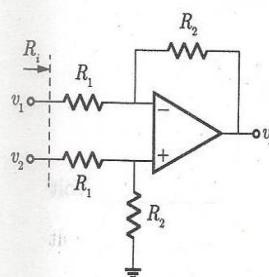
QUESTION 7.47

For the circuit shown below the voltage gain $A_{vd} = \frac{v_o}{(v_1 - v_2)}$ is



QUESTION 7.48

Consider the op-amp circuit shown below.

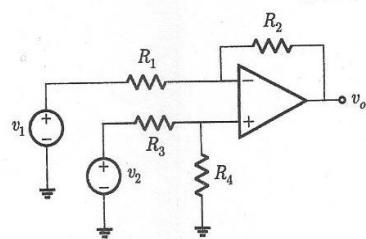


If the differential gain is $A_d = \frac{v_o}{v_2 - v_1} = 30$ and the input resistance $R_i = 50 \text{ k}\Omega$,

- then the value of resistor R_1 and R_2 respectively are
- (A) $750 \text{ k}\Omega, 25 \text{ k}\Omega$
 - (B) $50 \text{ k}\Omega, 1500 \text{ k}\Omega$
 - (C) $1.56 \text{ k}\Omega, 46.87 \text{ k}\Omega$
 - (D) $25 \text{ k}\Omega, 750 \text{ k}\Omega$

QUESTION 7.49

Consider the ideal op-amp circuit shown below.



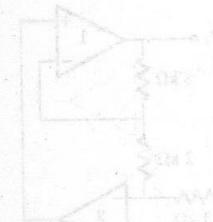
If it is given that $\frac{R_2}{R_1} = 10$, $\frac{R_4}{R_3} = 11$ then the common mode rejection ratio (CMRR) is

$$(A) 100 \text{ mV}, -440 \text{ mV}$$

$$(B) 110 \text{ mV}, -500 \text{ mV}$$

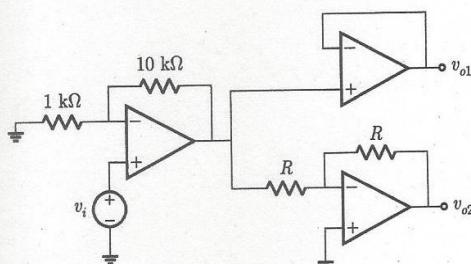
$$(C) 110 \text{ mV}, -490 \text{ mV}$$

$$(D) 100 \text{ mV}, -490 \text{ mV}$$



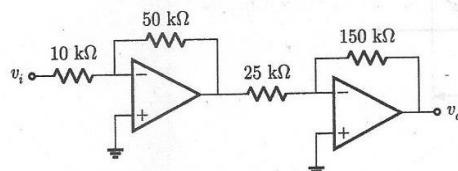
QUESTION 7.52

For the circuit shown below the true relation is



QUESTION 7.50

In circuit shown below, the input voltage v_i is 0.2 V. The output voltage v_o is



----- Volt

$$(A) v_{o1} = v_{o2}$$

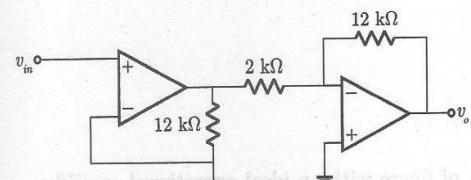
$$(B) v_{o1} = -v_{o2}$$

$$(C) v_o = 2v_{o2}$$

$$(D) 2v_{o1} = v_{o2}$$

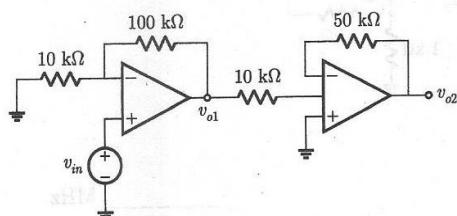
QUESTION 7.53

In the circuit shown below, assume op-amp is ideal. The voltage gain $A_v = \frac{v_o}{v_{in}}$ is



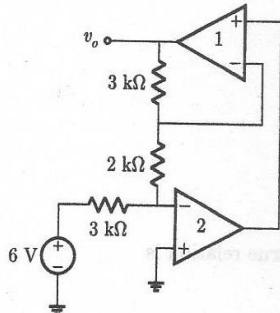
QUESTION 7.51

In the following amplifier circuit, each op-amp has an input offset voltage of 10 mV, op-amp is ideal otherwise, output v_{o1} and v_{o2} for an input $v_{in} = 0$ respectively are



QUESTION 7.54

For the circuit shown below the value of v_o is



- (A) 6 V
- (B) -6 V
- (C) -10 V
- (D) 10 V

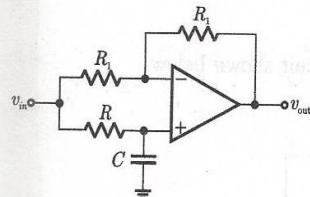
QUESTION 7.55

An audio amplifier is designed to have a small signal bandwidth of 20 kHz. The open loop low-frequency voltage gain of the op-amp is 10^5 and unity gain bandwidth is 1 MHz. What is the maximum closed-loop voltage gain for this amplifier?

- (A) 500
- (B) 5×10^6
- (C) 2×10^6
- (D) 50

QUESTION 7.56

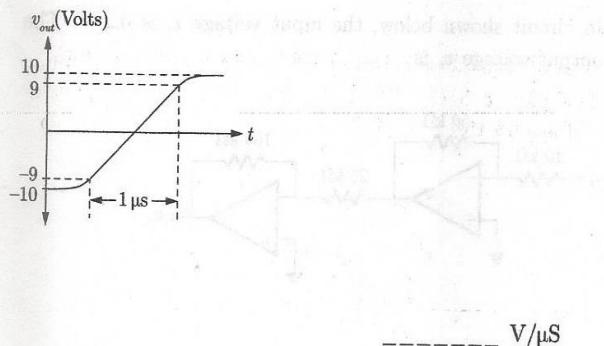
For the circuit of figure with an ideal operational amplifier, the maximum phase shift of the output v_{out} with reference to the input v_{in} is



- (A) 0°
- (B) -90°
- (C) $+90^\circ$
- (D) $\pm 180^\circ$

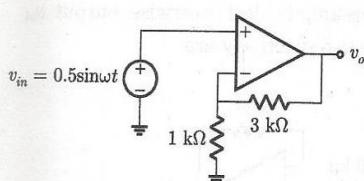
QUESTION 7.57

For the step input, the output response of an op-amp is shown below. What is the value of slew rate?



QUESTION 7.58

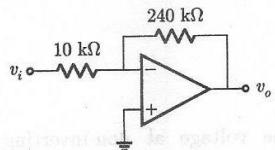
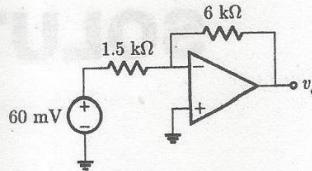
The op-amp shown in figure, has a slew rate of 1 V/ns. What is the highest input frequency for which no slewing occurs?



MHz

QUESTION 7.59

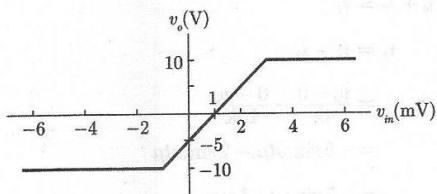
In the circuit shown below, the op-amp slew rate is $SR = 0.5 \text{ V}/\mu\text{s}$. If the amplitude of input signal is 0.02 V, then the maximum frequency that may be used is



- (A) $0.55 \times 10^6 \text{ rad/s}$
- (B) 0.55 rad/s
- (C) $1.1 \times 10^6 \text{ rad/s}$
- (D) 1.1 rad/s

QUESTION 7.60

The voltage transfer characteristic of an operational amplifier is shown in figure. What are the values of gain and offset voltage for this op-amp?



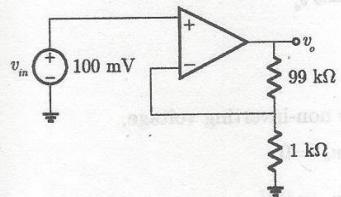
- (A) $10, 1 \text{ mV}$
- (B) $7500, -1 \text{ mV}$
- (C) $20, 2 \text{ mV}$
- (D) $7500, -2 \text{ mV}$

QUESTION 7.61

In the following circuit of figure, the op-amp is ideal except that it has an input offset voltage of 2 mV. Output v_o is

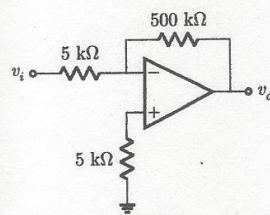
QUESTION 7.62

In the following circuit, the op-amp is ideal except that it has an input offset voltage of 5 mV. Then the output voltage v_o is



QUESTION 7.63

In the circuit shown below the input offset voltage and input offset current are $V_{io} = 4 \text{ mV}$ and $I_{io} = 150 \text{ nA}$. The total output offset voltage is



Answer

7.1	-10
7.2	B
7.3	B
7.4	C
7.5	C
7.6	B
7.7	C
7.8	-8
7.9	-10
7.10	-0.75
7.11	7.5
7.12	100
7.13	A
7.14	A
7.15	C
7.16	4500
7.17	0.0275%
7.18	0.5
7.19	D
7.20	11
7.21	1.333
7.22	7.5
7.23	6
7.24	-100
7.25	B
7.26	4.5
7.27	500M [^]
7.28	B
7.29	D
7.30	B
7.31	C
7.32	C

7.33	17
7.34	C
7.35	5
7.36	450
7.37	-8
7.38	0.53
7.39	-8
7.40	-2.8
7.41	4
7.42	-18
7.43	10
7.44	0
7.45	A
7.46	3
7.47	6
7.48	D
7.49	41.6
7.50	6
7.51	C
7.52	B
7.53	-42
7.54	C
7.55	D
7.56	D
7.57	18
7.58	79.6
7.59	C
7.60	B
7.61	-230
7.62	10.5
7.63	479

CHAPTER 8

OP - AMP APPLICATION

QUESTION 8.1

An amplifier has open gain of 10^4 and input resistance of $50\text{ k}\Omega$. Input resistance of series-shunt feedback amplifier using the above amplifier with a feedback factor of 0.10 is

_____ M Ω

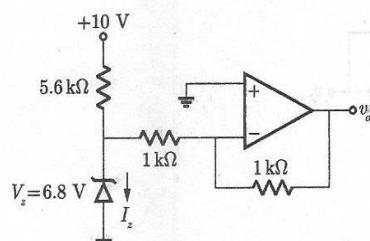
QUESTION 8.2

An op-amp has an open-loop gain of 105 and an open-loop upper cut-off frequency of 10 Hz. If this op-amp is connected as an amplifier with a closed-loop gain of 100, then the new upper cut-off frequency is

_____ kHz

QUESTION 8.3

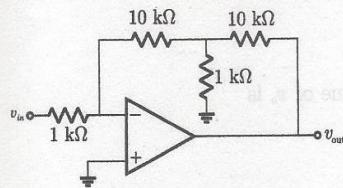
Consider the voltage reference circuit shown in figure. Assume op-amp is ideal. What is the value of zener current I_z ?



_____ mA

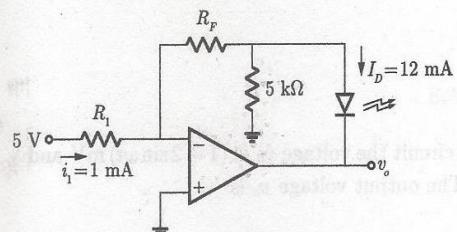
QUESTION 8.4

Assuming the operational amplifier to be ideal, the gain v_{out}/v_{in} for the circuit shown in figure is



QUESTION 8.5

Consider a circuit shown in figure. Assume op-amp is ideal.



The values of resistors R_1 and R_f respectively are

- (A) 5 k Ω , 5 k Ω
- (B) 55 k Ω , 5 k Ω
- (C) 55 k Ω , 55 k Ω
- (D) 5 k Ω , 55 k Ω

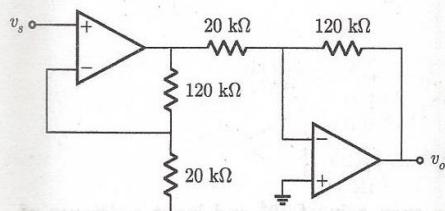
QUESTION 8.6

Three ideal amplifiers having voltage gain of A_1, A_2 , and A_3 connected in cascade. Then over-all voltage gain is

- (A) $A_1 A_2 A_3$
- (B) $A_1 + A_2 + A_3$
- (C) $A_1 = A_2 - V_3$
- (D) None of these

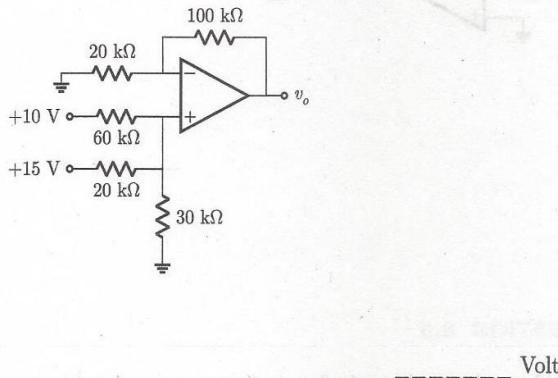
QUESTION 8.9

In the following circuit, op-amps are ideal. What is the output v_o for $v_s = 0.2 \text{ V}$?



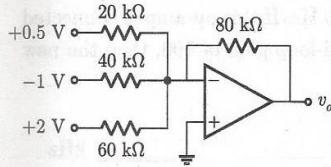
QUESTION 8.7

In following circuit, the value of v_o is



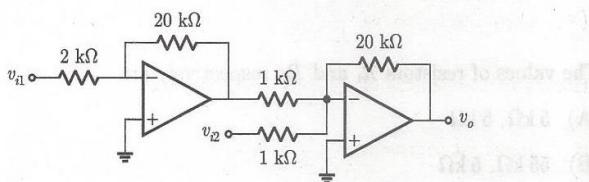
QUESTION 8.10

In the following circuit, what is the output voltage v_o ?



QUESTION 8.8

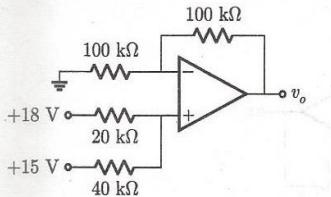
In the following circuit the voltage v_{i1} is $(1 + 2 \sin \omega t) \text{ mV}$ and $v_{i2} = -10 \text{ mV}$. The output voltage v_o is



- (A) $-0.4(1 + \sin \omega t) \text{ mV}$
- (B) $0.4(1 + \sin \omega t) \text{ mV}$
- (C) $-0.4(1 + 2 \sin \omega t) \text{ mV}$
- (D) $0.4(1 + 2 \sin \omega t) \text{ mV}$

QUESTION 8.11

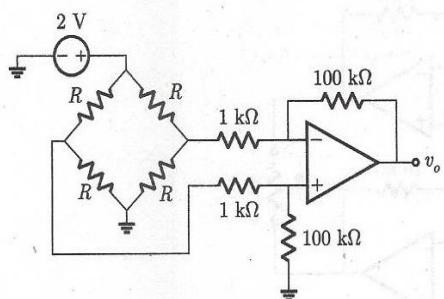
In following circuit what is the value of v_o ?



Volt

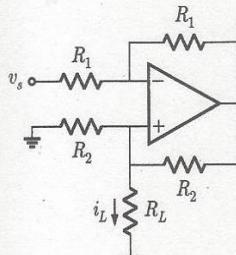
QUESTION 8.12

In the circuit shown below, the CMRR of the op-amp is 60 dB. What is the magnitude of the v_o ?



QUESTION 8.14

In the following op-amp circuit, the load current i_L is



(A) $-\frac{v_s}{R_2}$

(B) $\frac{v_s}{R_2}$

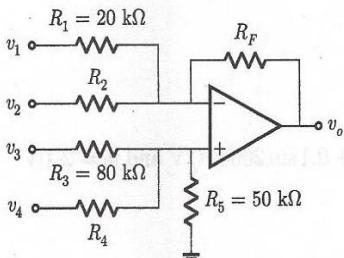
(C) $-\frac{v_s}{R_L}$

(D) $\frac{v_s}{R_L}$

QUESTION 8.13

In following circuit output is given as

$$v_o = -10v_1 - 4v_2 + 5v_3 + 2v_4$$

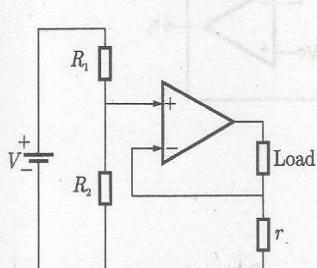


The resistance R_2 , R_4 and R_F respectively are

- (A) 50 kΩ, 200 kΩ, 500 kΩ
- (B) 50 kΩ, 100 kΩ, 80 kΩ
- (C) 50 kΩ, 200 kΩ, 200 kΩ
- (D) 50 kΩ, 80 kΩ, 100 kΩ

QUESTION 8.15

The circuit shown in the figure is



(A) a voltage source of $\frac{rV}{R_1 \parallel R_2}$

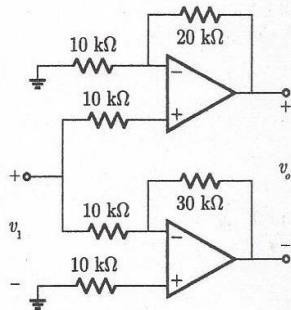
(B) a voltage source of $\frac{r \parallel R_2}{R_1} V$

(C) a current source of $\left(\frac{r \parallel R_2}{R_1 + R_2} \right) V$

(D) a current source of $\left(\frac{R_2}{R_1 + R_2} \right) \frac{V}{r}$

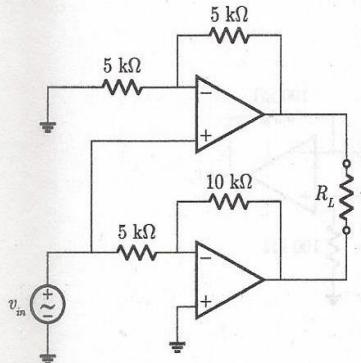
QUESTION 8.16

Consider the amplifier circuit shown in figure below. Assume op-amp is ideal. What is the value of voltage gain $A_v = \frac{v_o}{v_i}$?



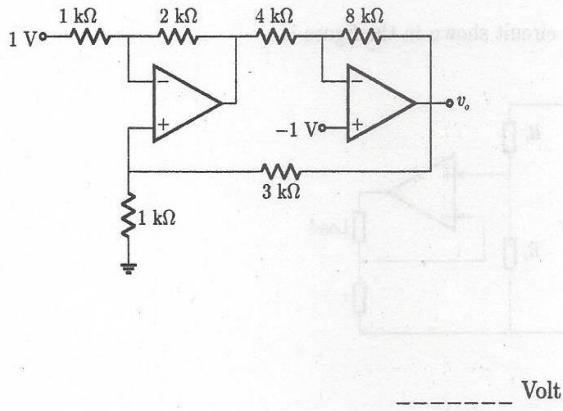
QUESTION 8.19

Consider the given amplifier circuit. Assume op-amp is ideal.



QUESTION 8.17

For the op-amp circuit shown in figure. Assume that the op-amps are ideal. What is the output voltage v_o ?



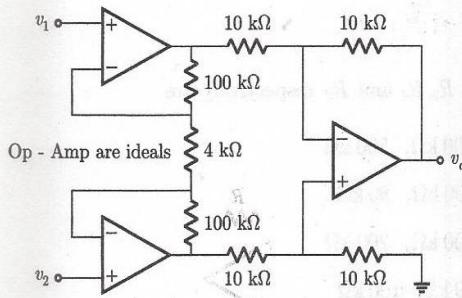
QUESTION 8.18

A first order, low pass filter is given with $R = 50 \Omega$ and $C = 5 \mu\text{F}$. What is the frequency at which the gain of the voltage transfer function of the filter is 0.25 ?

----- kHz

QUESTION 8.20

In the given circuit if $v_1 = (2 + 0.1 \sin 2000\pi t)$ V and $v_2 = 2.1$ V , output v_o is



(A) $(5.1 + 5.1 \sin 2000\pi t)$ V

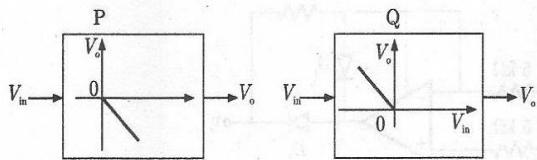
(B) $(209.1 + 5.1 \sin 2000\pi t)$ V

(C) $(5.1 - 5.1 \sin 2000\pi t)$ V

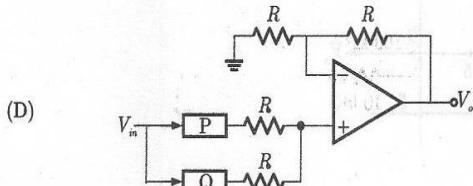
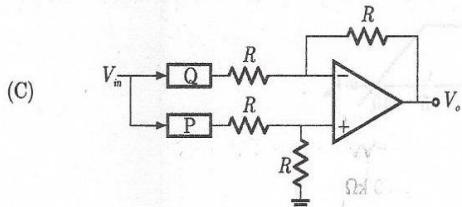
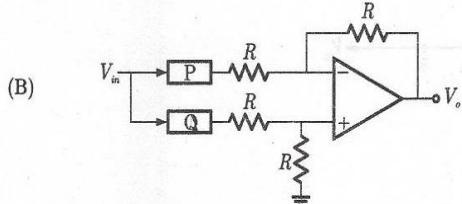
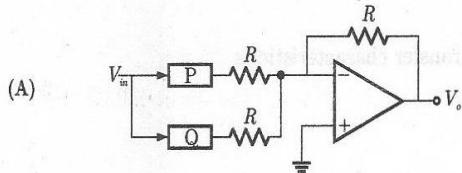
(D) $(209.1 - 2.1 \sin 2000\pi t)$ V

QUESTION 8.21

The block diagrams of two half wave rectifiers are shown in the figure. The transfer characteristics of the rectifiers are also shown within the block.

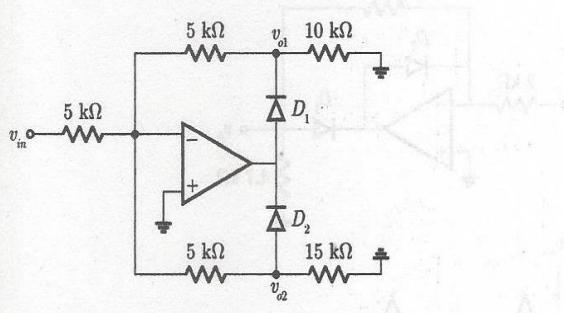


It is desired to make full wave rectifier using above two half-wave rectifiers. The resultant circuit will be

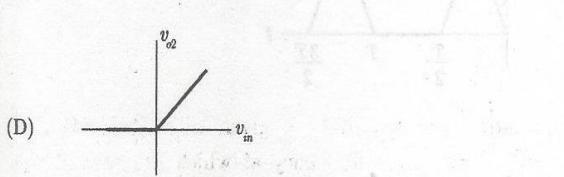
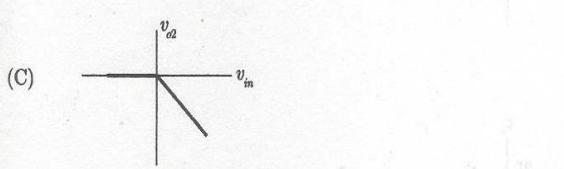
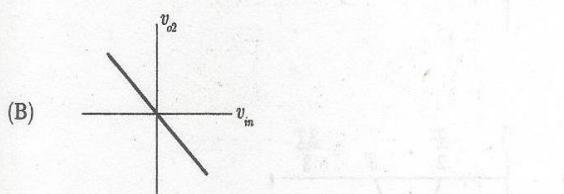
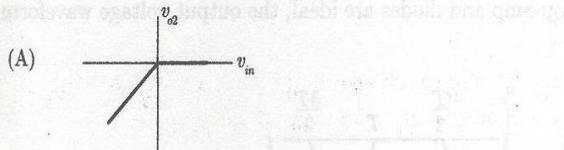


QUESTION 8.22

Consider the circuit shown in below. Assume diodes and op-amps are ideal.

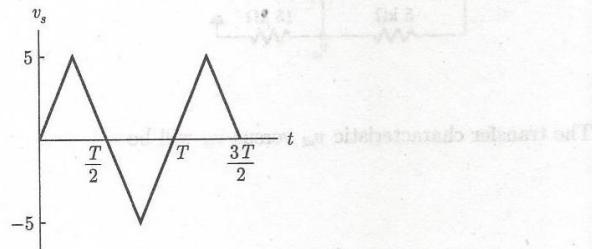
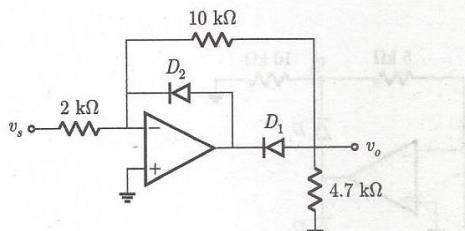


The transfer characteristic v_{o2} versus v_{in} will be

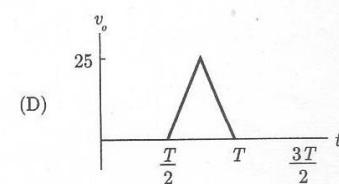
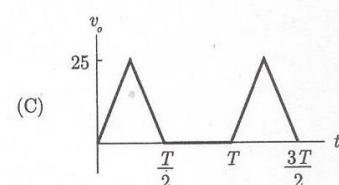
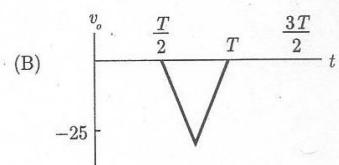
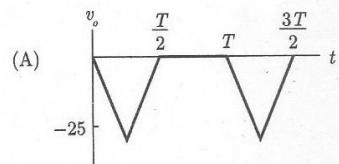


QUESTION 8.23

Consider the following circuit and input voltage to it.

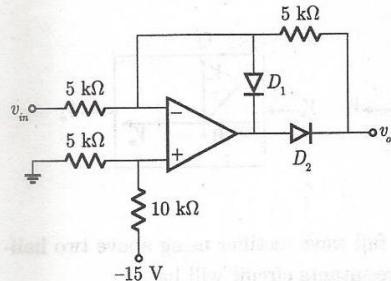


If op-amp and diodes are ideal, the output voltage waveform is

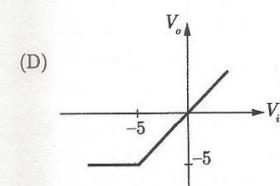
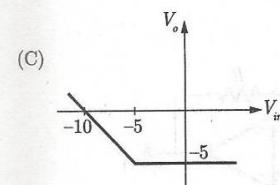
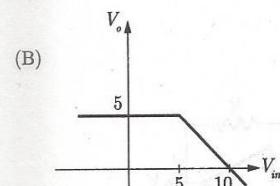
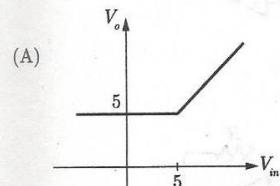


QUESTION 8.24

Consider the circuit shown below. Assume diodes and op-amps are ideal.

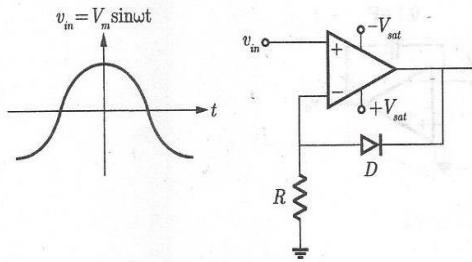


The plot of transfer characteristic is

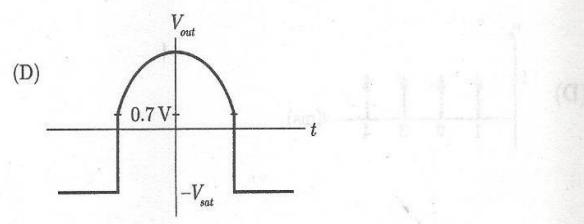
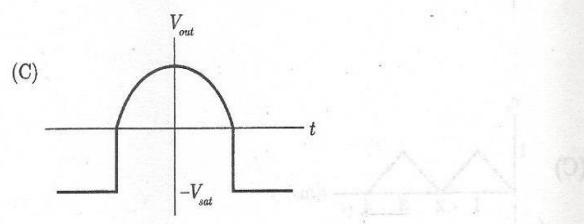
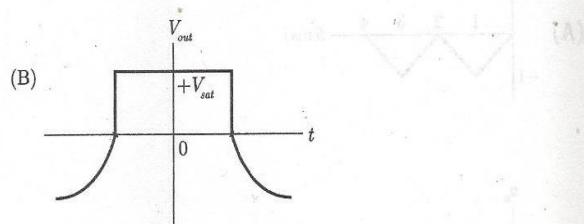
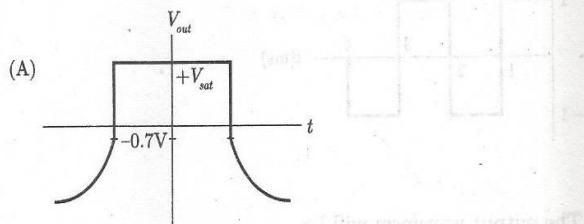


QUESTION 8.25

Consider the circuit shown in figure below. Cut in voltage of diode is 0.7 V and op-amp is ideal.

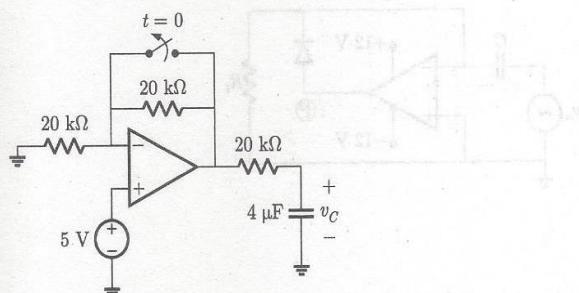


If $V_m = V_m \cos \omega t$, then the output waveform V_{out} is



QUESTION 8.26

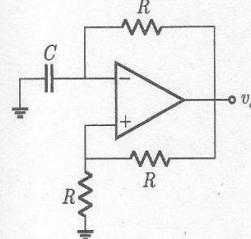
The circuit shown below is at steady state before the switch opens at $t = 0$. The $v_C(t)$ for $t > 0$ is



- (A) $10 - 5e^{-12.5t}$ V
- (B) $5 + 5e^{-12.5t}$ V
- (C) $5 + 5e^{-\frac{t}{12.5}}$ V
- (D) $10 - 5e^{-\frac{t}{12.5}}$ V

QUESTION 8.27

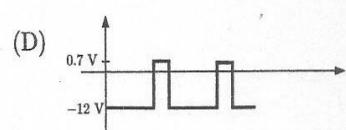
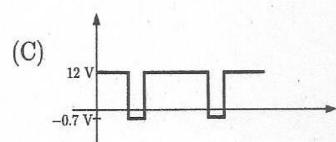
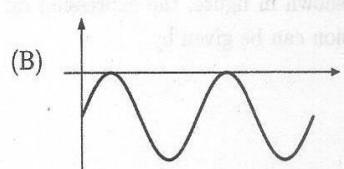
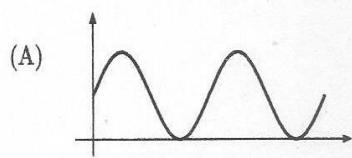
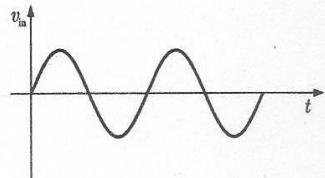
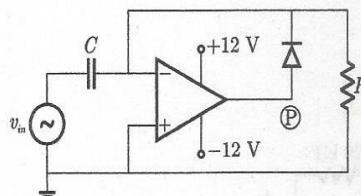
For the oscillator circuit shown in figure, the expression for the time period of oscillation can be given by
(where $\tau = RC$)



- (A) $\tau \ln 3$
- (B) $2\tau \ln 3$
- (C) $\tau \ln 2$
- (D) $2\tau \ln 2$

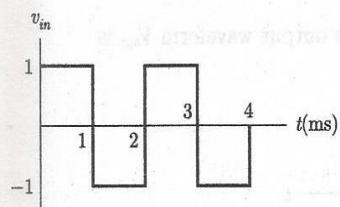
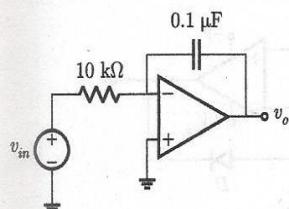
QUESTION 8.28

For a given sinusoidal input voltage, the voltage waveform at point P of the clamper circuit shown in figure will be

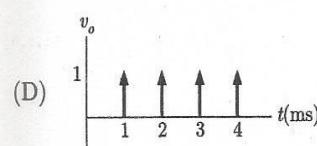
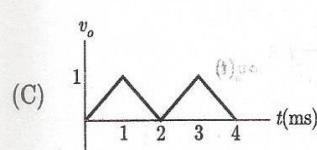
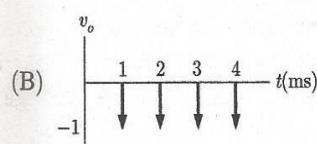
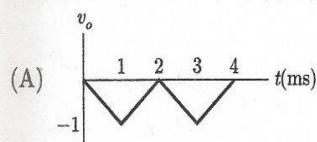


QUESTION 8.29

Consider an op-amp circuit and input to the circuit as shown in figure. Initially voltage across capacitor is zero.

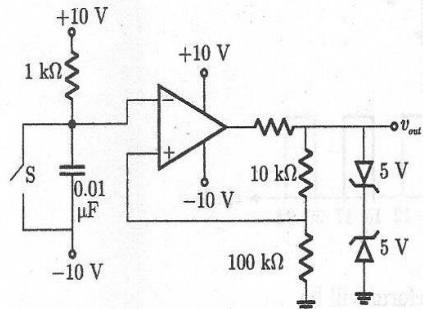


The output waveform will be



QUESTION 8.30

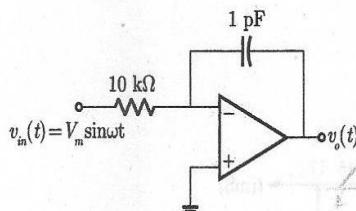
The switch S in the circuit of the figure is initially closed, it is opened at time $t = 0$. You may neglect the zener diode forward voltage drops. What is the behavior of v_{out} for $t > 0$?



- (A) It makes a transition from -5 V to $+5 \text{ V}$ at $t = 12.98 \mu\text{s}$
- (B) It makes a transition from -5 V to $+5 \text{ V}$ at $t = 2.57 \mu\text{s}$
- (C) It makes a transition from $+5 \text{ V}$ to -5 V at $t = 12.98 \mu\text{s}$
- (D) It makes a transition from $+5 \text{ V}$ to -5 V at $t = 2.57 \mu\text{s}$

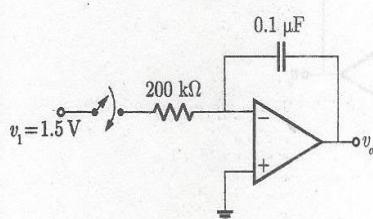
QUESTION 8.31

Consider the integrator circuit shown in figure below. Assume op-amp is ideal. If the amplifier circuit amplifies the input by a factor of 10, then what is the frequency of input voltage?

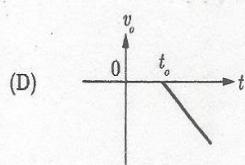
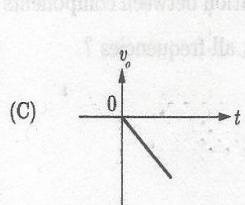
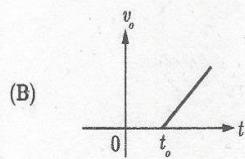
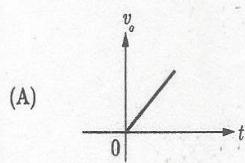


QUESTION 8.32

Consider the circuit shown in figure below. Assume op-amp is ideal.

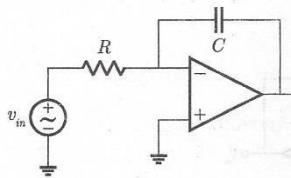


The output wave form is



QUESTION 8.33

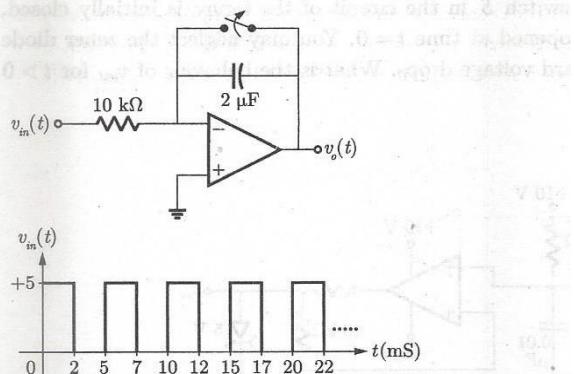
Consider the integrator shown in figure.



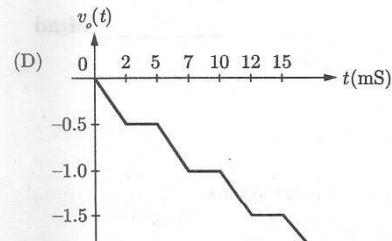
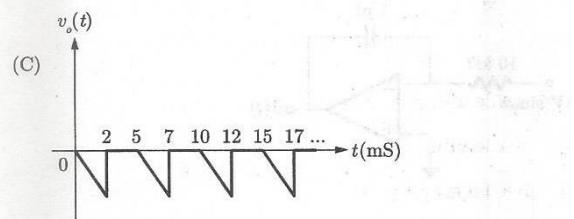
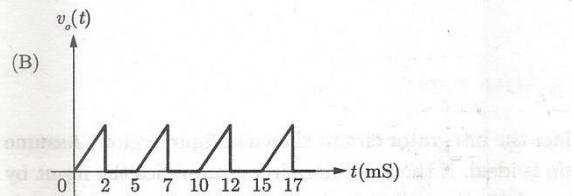
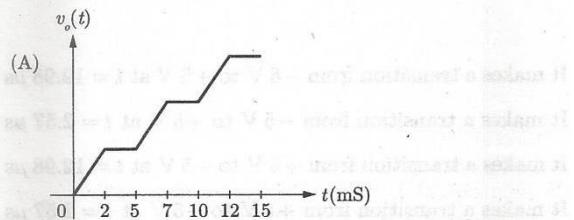
If op-amp having an input impedance of R_{in} , and open loop gain A_{ol} then what is the pole location of the integrator circuit ?

- (A) $-\frac{1}{RC} \left(1 + \frac{R}{R_{in}}\right)$
- (B) $-\frac{1}{RC}$
- (C) $-\frac{1}{RC \left(1 + \frac{1}{A_{ol}}\right)} \left(1 + \frac{R}{R_{in}}\right)$
- (D) $-\frac{1}{RC(1 + A_{ol})} \left(1 + \frac{R}{R_{in}}\right)$

Input waveform is also shown in this figure.



The output waveform will be



QUESTION 8.34

In previous question what is the relation between components $R_1 C_1$ and $R_2 C_2$, if $\left| \frac{V_{out}}{V_{in}} \right|$ is unity at all frequencies ?

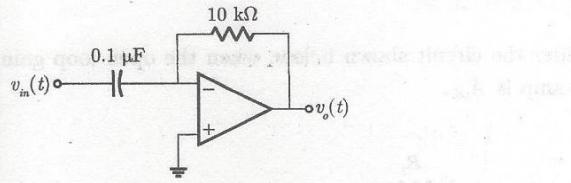
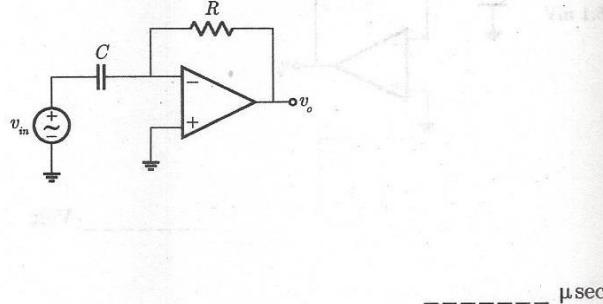
- (A) $\frac{\frac{1}{sC_1} || R_1}{\frac{1}{sC_2} || R_2} = \frac{A_{OL} + 1}{A_{OL} - 1}$
- (B) $\frac{\frac{1}{sC_2} || R_2}{\frac{1}{sC_1} || R_1} = \frac{A_{OL} + 1}{A_{OL} - 1}$
- (C) $\frac{R_2 || \frac{1}{sC_2}}{R_1 || \frac{1}{sC_1}} = \frac{1}{A_{OL} - 1}$
- (D) $\frac{R_2 || \frac{1}{sC_2}}{R_1 || \frac{1}{sC_1}} = \frac{A_{OL} - 1}{1}$

QUESTION 8.35

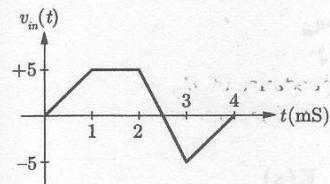
Consider the circuit shown in below. Assume op-amp is ideal.

QUESTION 8.36

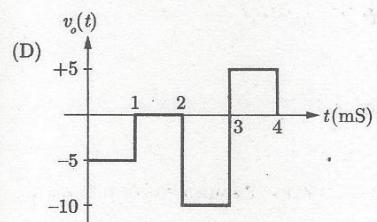
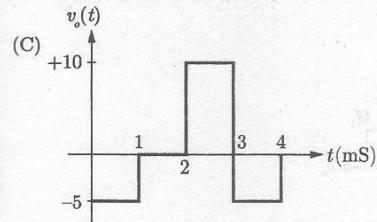
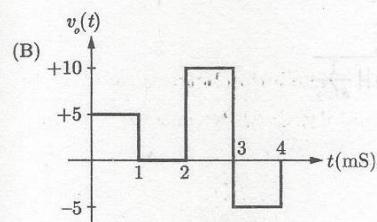
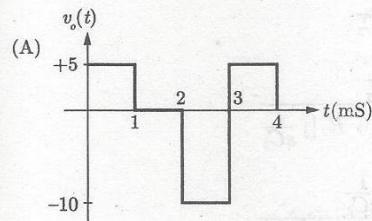
For the differentiator circuit shown in figure below assume op-amp is ideal. This circuit is used to amplify the input by a factor of 5 at a frequency 1 MHz. What is the value of RC ?



Input voltage waveform is shown in following figure.

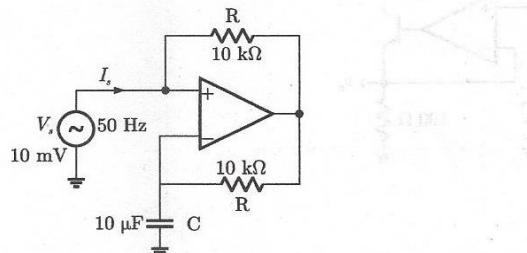


The output voltage waveform will be



QUESTION 8.37

The following circuit has $R = 10 \text{ k}\Omega$, $C = 10 \mu\text{F}$. The input voltage is a sinusoidal at 50 Hz with an rms value of 10 V. Under ideal conditions, the current I_s from the source is



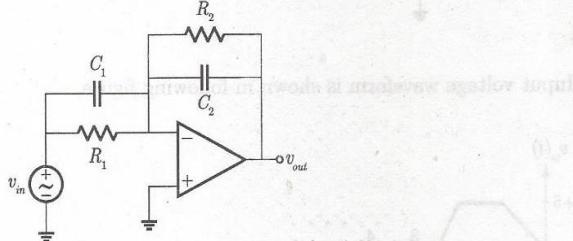
- (A) $10\pi \text{ mA}$ leading by 90°
- (B) $20\pi \text{ mA}$ leading by 90°
- (C) $20\pi \text{ mA}$ lagging by 90°
- (D) $10\pi \text{ mA}$ lagging by 90°

QUESTION 8.38

Consider the circuit shown in below. Assume op-amp is ideal.

QUESTION 8.39

Consider the circuit shown below, when the open loop gain of op-amp is A_{OL} .

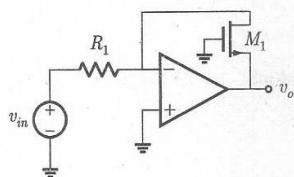


The transfer function $T(s) = \frac{V_o(s)}{V_{in}(s)}$ is

- (A) $-\frac{A_{OL}R_2 || \frac{1}{sC_2}}{R_1 || \frac{1}{sC_1} + R_2 || \frac{1}{sC_2}}$
- (B) $-\frac{R_2 || \frac{1}{sC_2}}{(1 + A_{OL})R_1 || \frac{1}{sC_1} + R_2 || \frac{1}{sC_2}}$
- (C) $-\frac{A_{OL}R_2 || \frac{1}{sC_2}}{(1 + A_{OL})R_1 || \frac{1}{sC_1} + R_2 || \frac{1}{sC_2}}$
- (D) $-A_{OL} \frac{R_1 || \frac{1}{sC_1}}{R_1 || \frac{1}{sC_1} + R_2 || \frac{1}{sC_2}}$

QUESTION 8.40

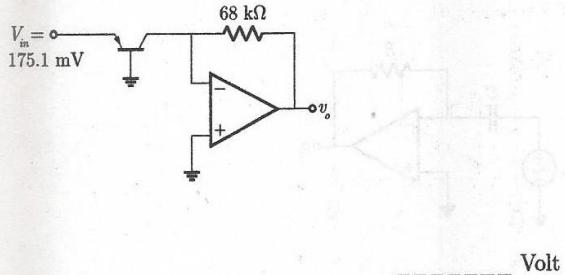
If M_1 is operating in saturation, the circuit shown below acts as a



- (A) Logarithm amplifier
- (B) Precision rectifier
- (C) Square root amplifier
- (D) Voltage follower

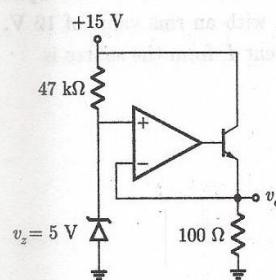
QUESTION 8.41

Consider the circuit shown in figure below. Assume that op-amp is ideal and $V_{thermal} = 25 \text{ mV}$. If reverse saturation current $I_o = 40 \text{ nA}$, then the output voltage v_o is



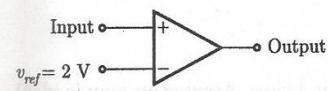
QUESTION 8.42

In the following circuit, the op-amp is ideal. If $\beta_F = 60$, then the total current supplied by the 15 V source is



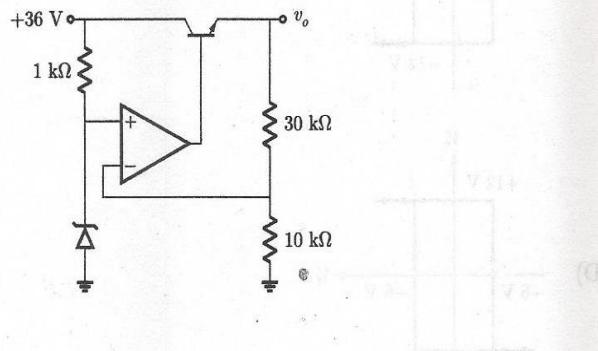
QUESTION 8.43

If the input to the following ideal comparator is a sinusoidal signal of 8 V (peak to peak) without any DC component. The output of the comparator has a duty cycle of



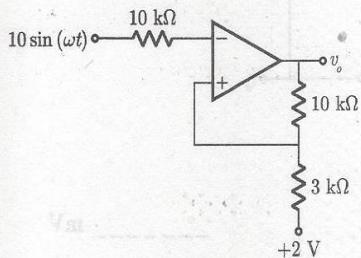
QUESTION 8.44

In the op-amp series regulator circuit shown below, $v_z = 6.2 \text{ V}$, $V_{BE} = 0.7 \text{ V}$ and $\beta = 60$. The output voltage v_o is



QUESTION 8.46

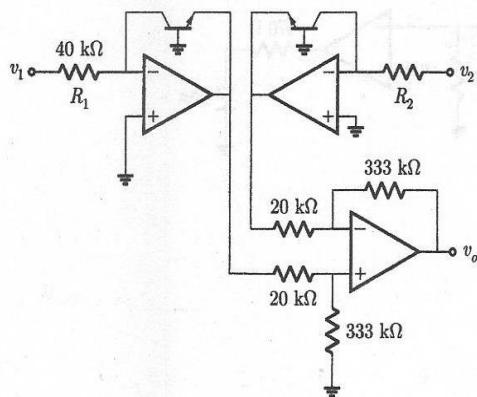
The output voltage (v_o) of the Schmitt trigger shown in figure swings between $+15 \text{ V}$ and -15 V . Assume that the operational amplifier is ideal. The output will change from $+15 \text{ V}$ to -15 V when the instantaneous value of the input sine wave is



Volt

QUESTION 8.45

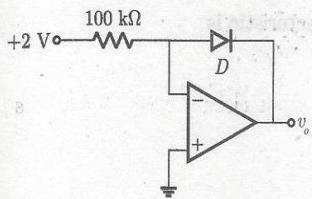
In the given circuit both transistors Q_1 and Q_2 are identical. The output voltage at $T = 300 \text{ K}$ is



- (A) $2 \log_{10} \left(\frac{v_2 R_1}{v_1 R_2} \right)$
- (B) $\log_{10} \left(\frac{v_2 R_1}{v_1 R_2} \right)$
- (C) $2.303 \log_{10} \left(\frac{v_2 R_1}{v_1 R_2} \right)$
- (D) $4.605 \log_{10} \left(\frac{v_2 R_1}{v_1 R_2} \right)$

QUESTION 8.47

Consider the circuit shown in below. Assume op-amp is ideal and $V_{\text{thermal}} = 25 \text{ mV}$

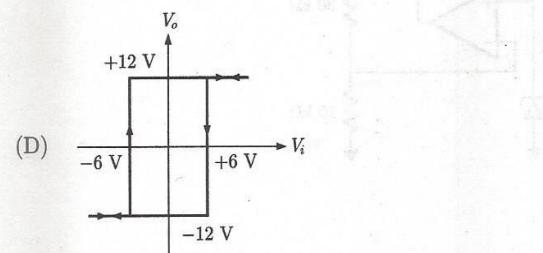
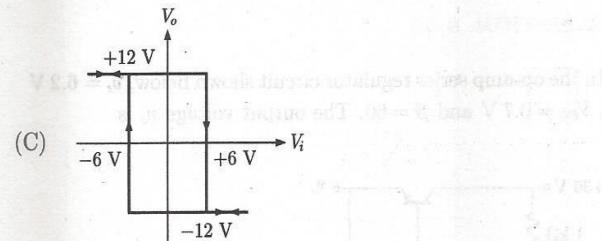
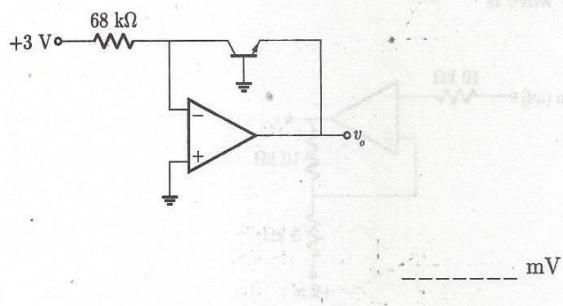


Volt

Given that reverse leakage current I_R of the diode D is $I_0 = 50 \text{ nA}$, then the value of output voltage v_o is

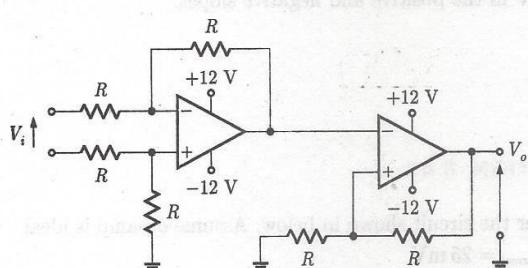
QUESTION 8.48

Consider the circuit shown in figure below. Assume op-amp is ideal and $V_{\text{thermal}} = 25 \text{ mV}$. If the reverse saturation current of transistor is $I_b = 40 \text{ nA}$, then the output voltage of the circuit is

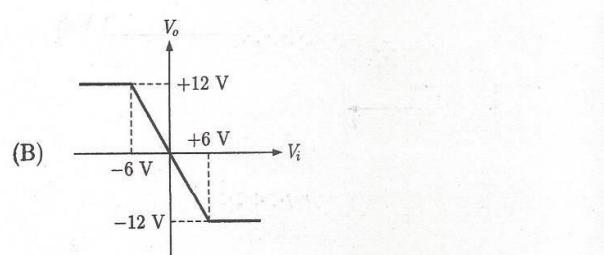
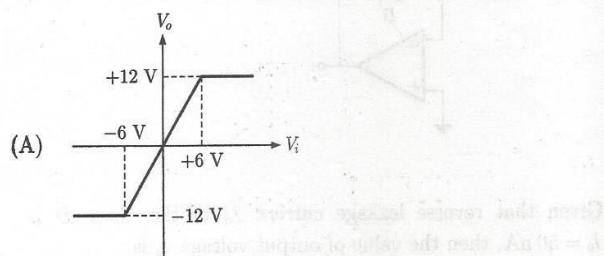


QUESTION 8.49

Consider the circuit shown below.

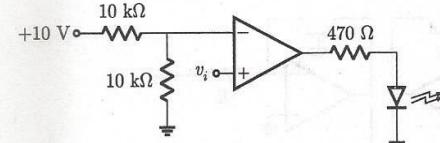


The CORRECT transfer characteristic is



QUESTION 8.50

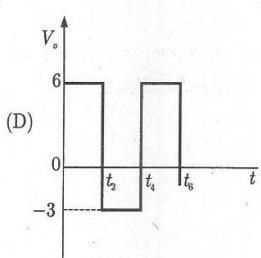
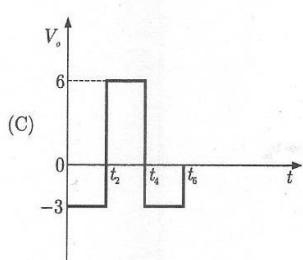
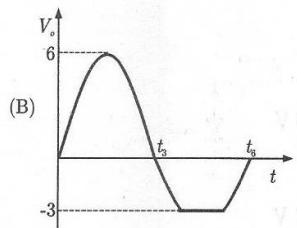
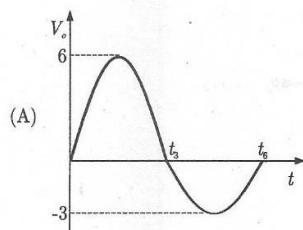
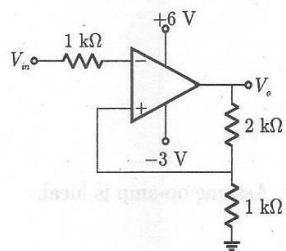
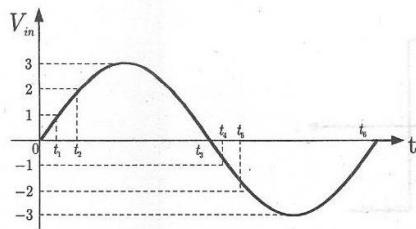
The LED in the following circuit will be ON if v_i is



- (A) $> 10 \text{ V}$
- (B) $< 10 \text{ V}$
- (C) $> 5 \text{ V}$
- (D) $< 5 \text{ V}$

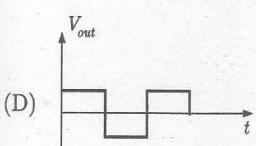
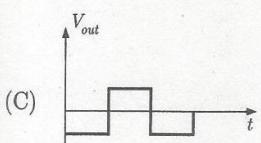
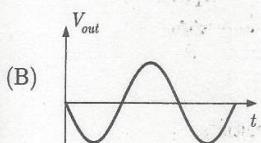
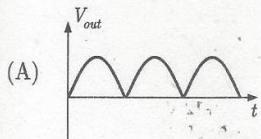
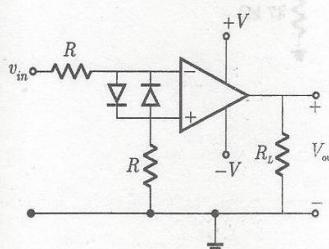
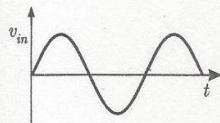
QUESTION 8.51

An ideal op-amp circuit and its input wave form are shown in the figures. The output waveform of this circuit will be



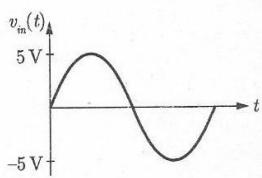
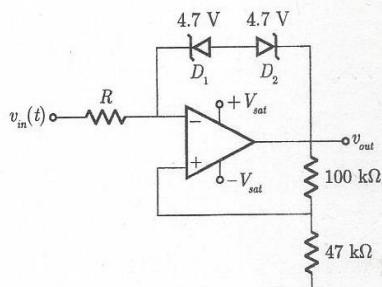
QUESTION 8.52

In the given figure, if the input is a sinusoidal signal, the output will appear as

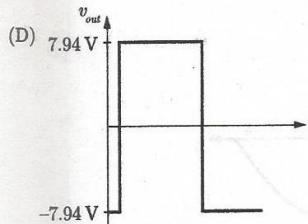
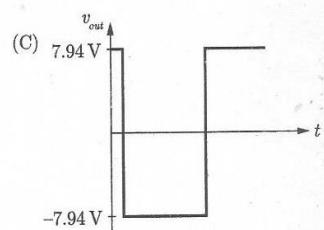
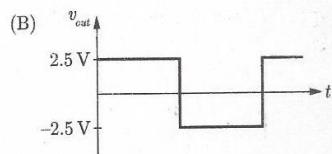
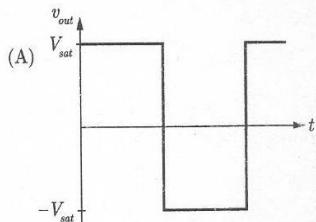


QUESTION 8.53

For the circuit shown below, assume op-amp is ideal. The input waveform to the circuit is also shown in the figure.

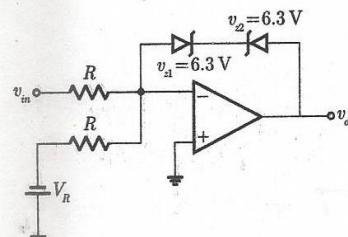


So, the output voltage waveform is



QUESTION 8.54

Consider the circuit shown below. Assume op-amp is ideal.



Given

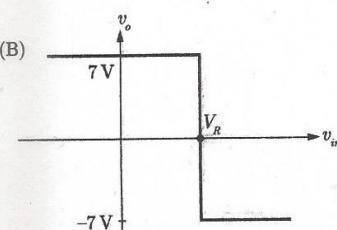
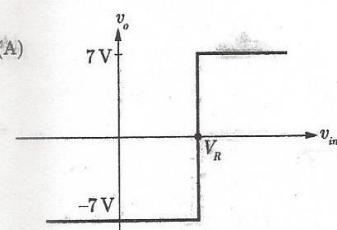
Zener diode voltage,

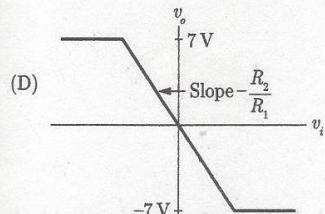
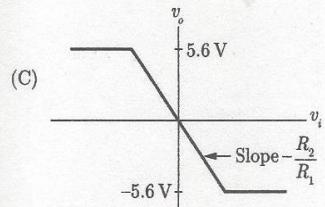
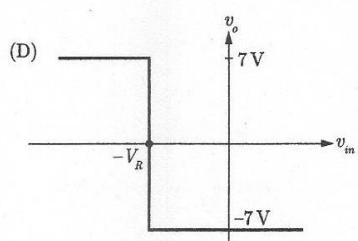
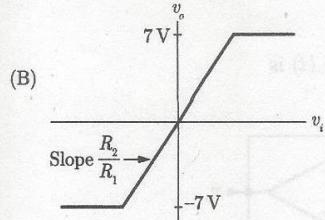
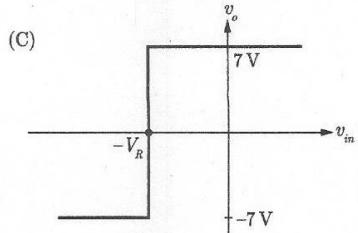
$$v_{z1} = v_{z2} = 6.3 \text{ V}$$

Forward bias voltage,

$$v_{r1} = v_{r2} = 0.7 \text{ V}$$

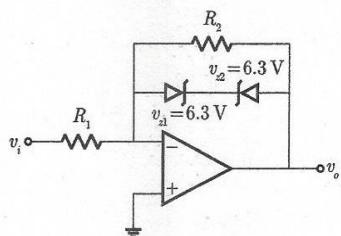
The plot v_o versus v_{in} will be



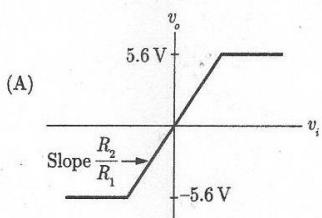


QUESTION 8.55

Consider the circuit shown below. Assume op-amp is ideal.

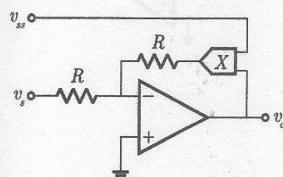


Given that zener diode voltage $v_{z1} = v_{z2} = 6.3 \text{ V}$ and diode forward bias voltage $V_f = 0.7 \text{ V}$, then the plot between the v_o versus v_i will be



QUESTION 8.56

The analog multiplier X shown below has the characteristics $v_p = v_1 v_2$. The output of this circuit is



(A) $v_s v_{ss}$

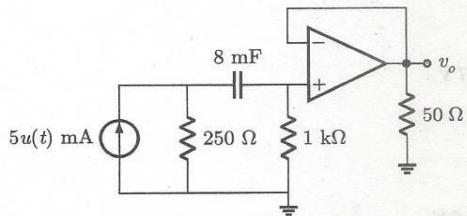
(B) $-v_s v_{ss}$

(C) $-\frac{v_s}{v_{ss}}$

(D) $\frac{v_s}{v_{ss}}$

QUESTION 8.57

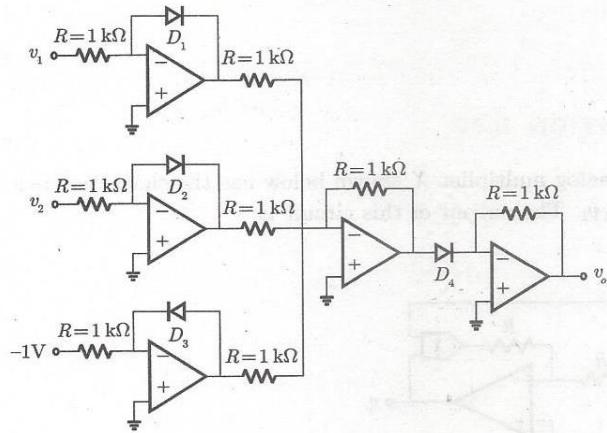
In following circuit output $v_o(t)$ is



- (A) $e^{\frac{t}{10}} u(t)$ V
- (B) $-e^{-\frac{t}{10}} u(t)$ V
- (C) $e^{-\frac{t}{10}} u(t)$ V
- (D) $-e^{-\frac{t}{10}} u(t)$ V

QUESTION 8.58

Consider the circuit shown below. Assume op-amp is ideal and input $v_1, v_2 > 0$



What is the value of output voltage

- (A) $v_1 v_2$
- (B) $-v_1 v_2$
- (C) $-(v_1 + v_2)$
- (D) $v_1 + v_2$

Answer

8.1	50
8.2	10
8.3	0
8.4	-120
8.5	D
8.6	A
8.7	5.5
8.8	B
8.9	-8.4
8.10	-2.67
8.11	34
8.12	100
8.13	C
8.14	A
8.15	D
8.16	6
8.17	-0.571
8.18	2.46
8.19	D
8.20	C
8.21	B
8.22	C
8.23	A
8.24	C
8.25	A
8.26	A
8.27	B
8.28	B
8.29	A

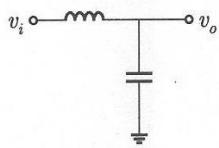
8.30	B
8.31	10
8.32	C
8.33	D
8.34	B
8.35	D
8.36	0.795
8.37	A
8.38	C
8.39	C
8.40	C
8.41	-3
8.42	49.4
8.43	0.33
8.44	24.8
8.45	B
8.46	A
8.47	-0.15
8.48	-175.1
8.49	D
8.50	C
8.51	D
8.52	C
8.53	C
8.54	B
8.55	D
8.56	C
8.57	A
8.58	B

CHAPTER 9

ACTIVE FILTERS

QUESTION 9.1

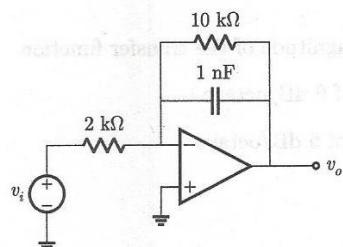
The network shown below is a



- (A) low pass filter
- (B) high pass filter
- (C) band stop filter
- (D) band pass filter

QUESTION 9.2

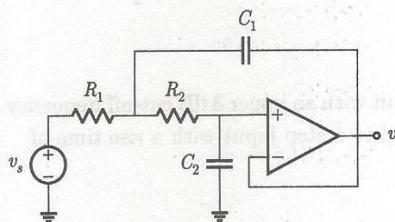
Circuit shown below is a



- (A) low pass filter with cut-off frequency $f_c = 15.9$ kHz
- (B) High pass filter will cut-off frequency $f_c = 15.9$ kHz
- (C) High pass filter with cut-off frequency $f_c = 79.5$ kHz
- (D) Low pass filter with cut-off frequency $f_c = 79.5$ kHz

QUESTION 9.3

The following circuit is a



- (A) Band pass filter
- (B) Low pass filter
- (C) High pass filter
- (D) Band Reject filter

A low-pass circuit can be also

- (A) an integrator circuit
- (B) a differentiator circuit
- (C) either a differentiator or an integrator circuit
- (D) none of these

QUESTION 9.5

A low-pass circuit is fed with a periodic wave form of time period T . For this circuit to function like an integrator, the necessary condition to be satisfied is

- (A) $RC = T$
- (B) $RC \ll T$
- (C) $RC \gg T$
- (D) none of these

QUESTION 9.6

An RC integrator circuit with an upper 3 dB cut-off frequency of 3.5 kHz will respond to a step input with a rise time of

- (A) $100\ \mu s$
- (B) $10\ \mu s$
- (C) $100\ ms$
- (D) indeterminate from given data

QUESTION 9.7

A multistage low pass filter using N -identical op-amps is designed to have overall gain of 1000, a bandwidth of 20 kHz and a response that rolls off at high frequencies at a rate of $-60\ dB/sec$. What are the value of N , gain and bandwidth of each op-amp

- (A) 3, 333.3, 6.66 kHz
- (B) 3, 10, 39.2 kHz
- (C) 6, 10, 6.66 kHz
- (D) 3, 10, 2.71 kHz

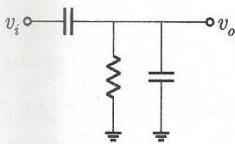
QUESTION 9.8

Reduction in gain at $f = 2f_{3dB}$ for a one-pole low-pass filter will be

----- dB

QUESTION 9.9

The network shown below is a



- (A) low pass filter
- (B) high pass filter
- (C) band stop filter
- (D) band pass filter

QUESTION 9.10

A high-pass circuit can also possibly be

- (A) an integrator circuit
- (B) a differentiator circuit
- (C) either a differentiator or an integrator circuit
- (D) none of these

QUESTION 9.11

At a pole frequency, the magnitude of the transfer function

- (A) Increases at the rate of 6 dB/octave
- (B) Decreases at the rate of 6 dB/octave
- (C) Becomes infinite
- (D) Becomes zero

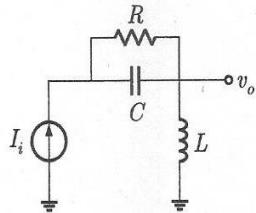
QUESTION 9.12

The reduction in gain at $f = 2f_{3dB}$ for a three-pole low-pass filter will be

----- dB

QUESTION 9.13

In some applications, the input to a filter may be provided in the form of a current as shown below :



The transfer function, v_o/i_i , of the circuit is

- (A) R/sL
- (B) $1/sL$
- (C) sRL
- (D) sL

QUESTION 9.14

At half-power cut-off frequency, the gain of a low pass filter is equal to

- (A) 0.707 dB
- (B) 0 dB
- (C) 3 dB
- (D) Maximum gain - 3 dB

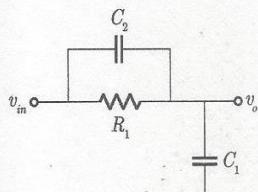
QUESTION 9.15

A first-order active filter has a roll-off of

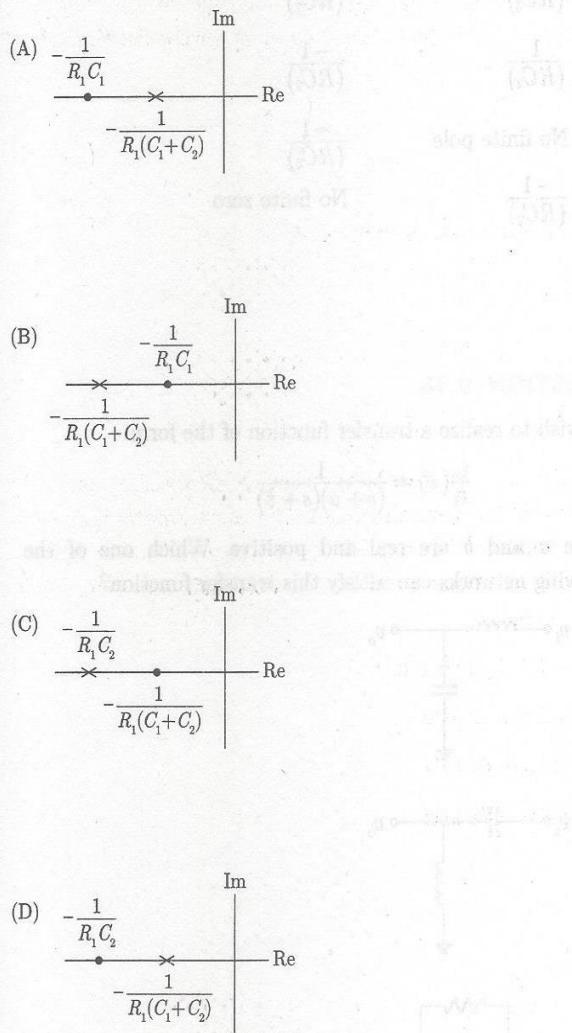
- (A) 20 dB/decade
- (B) 20 dB/octave
- (C) 3 dB/decade
- (D) 3 dB/octave

QUESTION 9.16

Consider the circuit shown below,

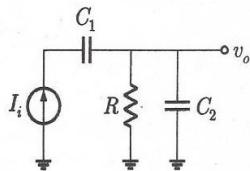


The pole-zero diagram of the transfer function $\frac{v_o}{v_i}$ is



QUESTION 9.17

Consider the filter with the input provided in the form of a current as shown below :



What are the poles and zeroes of the transfer function

$$T.F. = \frac{v_o}{I_i}$$

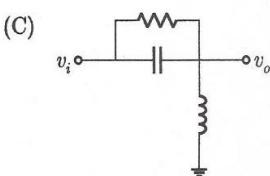
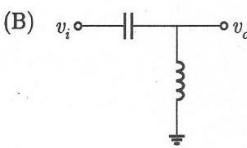
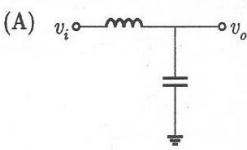
- | Pole | Zero |
|-------------------------|---------------------|
| (A) $\frac{-1}{(RC_2)}$ | $\frac{1}{(RC_2)}$ |
| (B) $\frac{1}{(RC_2)}$ | $\frac{-1}{(RC_2)}$ |
| (C) No finite pole | $\frac{-1}{(RC_2)}$ |
| (D) $\frac{-1}{(RC_2)}$ | No finite zero |

QUESTION 9.18

We wish to realize a transfer function of the form

$$\frac{v_o}{v_i}(s) = \frac{1}{(s+a)(s+b)}$$

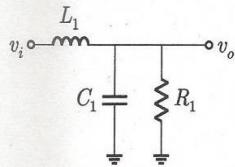
where a and b are real and positive. Which one of the following networks can satisfy this transfer function?



- (D) None of these

QUESTION 9.19

The low-pass filter shown in figure below is designed to contain two real poles.



The transfer function of the filter is

- (A) $\frac{1}{L_1 C_1} \frac{1}{s^2 - \frac{1}{R_1 C_1} s + \frac{1}{L_1 C_1}}$
- (B) $\frac{1}{L_1 C_1} \frac{1}{s^2 + \frac{1}{R_1 C_1} s + \frac{1}{L_1 C_1}}$
- (C) $\frac{L_1}{C_1} \frac{1}{s^2 + \frac{1}{R_1 C_1} s + \frac{1}{L_1 C_1}}$
- (D) $\frac{L_1}{C_1} \frac{1}{s^2 - \frac{1}{R_1 C_1} s + \frac{1}{L_1 C_1}}$

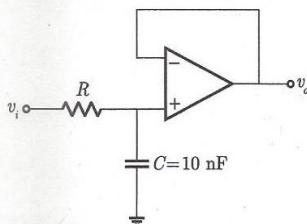
QUESTION 9.20

In previous question which of the following condition guarantees that the poles are real ?

- (A) $\frac{1}{R_1 C_1} \geq \frac{2}{\sqrt{L_1 C_1}}$
- (B) $\frac{1}{R_1 C_1} < \frac{2}{\sqrt{L_1 C_1}}$
- (C) $\frac{1}{R_1 C_1} \geq 2\sqrt{\frac{R_1}{L_1}}$
- (D) $\frac{1}{R_1 C_1} < 2\sqrt{\frac{R_1}{L_1}}$

QUESTION 9.21

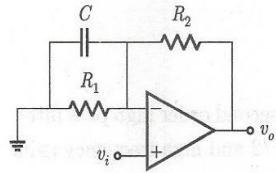
In the given circuit if the 3 dB frequency is 5 kHz, then the value of Resistor R is



kΩ

QUESTION 9.22

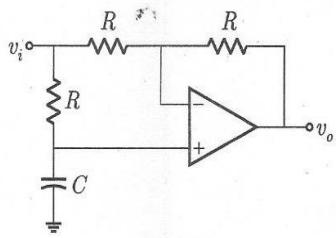
In the following op-amp, cut-off frequency f_{3-dB} is



- (A) $\frac{1}{2\pi R_1 C}$
- (B) $\frac{1}{2\pi R_2 C}$
- (C) $\frac{1}{2\pi\sqrt{R_1 R_2} C}$
- (D) $\frac{1}{2\pi} \left(\frac{R_1 + R_2}{R_1 R_2 C} \right)$

QUESTION 9.23

Consider the circuit shown in figure below

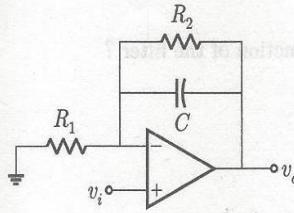


The magnitude and phase of the voltage transfer function are respectively

- (A) $1, 2\tan^{-1}(\omega RC)$
- (B) $1, -2\tan^{-1}(\omega RC)$
- (C) $1/2, -\tan^{-1}(\omega RC)$
- (D) $1/2, \tan^{-1}(\omega RC)$

QUESTION 9.24

Consider the circuit shown below



The voltage transfer function is

- (A) $\left(1 + \frac{R_2}{R_1}\right) \frac{1 + s(R_1 || R_2)C}{(1 + sR_2 C)}$
- (B) $\left(1 + \frac{R_1}{R_2}\right) \frac{1 + s(R_1 || R_2)C}{(1 + sR_2 C)}$
- (C) $\left(1 + \frac{R_1}{R_2}\right) \frac{1 + s(R_1 || R_2)C}{(1 + sR_1 C)}$
- (D) $\left(1 + \frac{R_2}{R_1}\right) \frac{1 + s(R_1 || R_2)C}{(1 + sR_1 C)}$

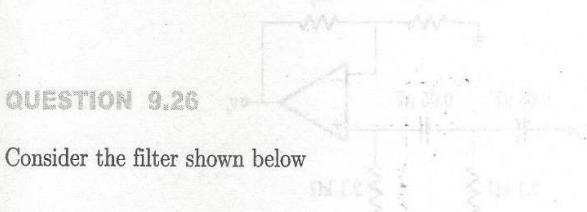
QUESTION 9.25

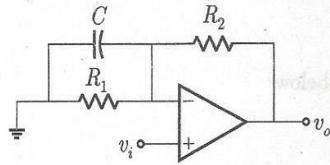
In previous question what is the cutoff frequency, f_{3-dB} for the circuit ?

- (A) $\frac{1}{2\pi(R_1 + R_2)C}$
- (B) $\frac{1}{(R_1 || R_2)C}$
- (C) $\frac{1}{(R_1 + R_2)C}$
- (D) $\frac{1}{2\pi(R_1 || R_2)C}$

QUESTION 9.26

Consider the filter shown below





kHz

What is the voltage transfer function of the filter?

- (A) $\left(1 + \frac{R_2}{R_1}\right)[1 + s(R_1 || R_2)C]$
- (B) $\left(1 + \frac{R_1}{R_2}\right)[1 + s(R_1 || R_2)C]$
- (C) $s\left(1 + \frac{R_2}{R_1}\right)(R_1 || R_2)C$
- (D) $s\left(1 + \frac{R_1}{R_2}\right)(R_1 || R_2)C$

QUESTION 9.29

What is the transfer function of a second order high pass filter with pole location at $-0.5 \pm j\sqrt{3}/2$ and high frequency gain of unity?

- (A) $\frac{s}{s^2 + s + 1}$
- (B) $\frac{s+1}{s^2 - s + 1}$
- (C) $\frac{s^2}{s^2 - s + 1}$
- (D) $\frac{s^2}{s^2 + s + 1}$

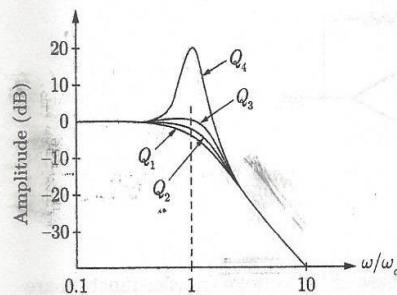
QUESTION 9.27

In previous question the 3 dB cut off frequency of the filter is

- (A) $\frac{1}{(R_1 + R_2)C}$
- (B) $\frac{1}{(R_1 || R_2)C}$
- (C) $\frac{1}{2\pi(R_1 || R_2)C}$
- (D) $\frac{1}{2\pi(R_1 + R_2)C}$

QUESTION 9.30

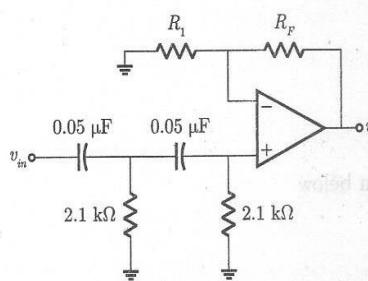
Consider the amplitude response of low pass 2 pole filter with Q as parameter. The ascending order of Q is



QUESTION 9.28

Consider the second order high pass filter shown as figure.

What is the value of cutoff frequency?



- (A) $Q_1 > Q_2 > Q_3 > Q_4$

- (B) $Q_1 < Q_2 < Q_3 < Q_4$

- (C) $Q_1 > Q_3 > Q_2 > Q_4$

- (D) $Q_1 < Q_3 < Q_2 < Q_4$

QUESTION 9.31

The higher the Q , the

- (A) lower the center frequency of the filter.
- (B) greater the bandwidth of the filter.
- (C) less selective the filter.
- (D) more selective the filter.

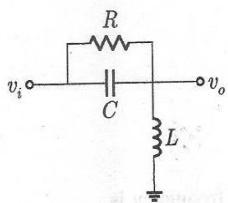
QUESTION 9.32

Consider a second order bandpass filter that is geometrically symmetrical around the centre frequency ω_0 . The ω_1 and ω_2 are the frequencies of each sides of centre frequency ω_0 for which $|T(j\omega_1)| = |T(j\omega_2)|$. What is the expression of centre frequency ω_0 ?

- (A) $\omega_0^2 = 2\omega_1\omega_2$
- (B) $\omega_0^2 = 3\omega_1\omega_2$
- (C) $\omega_0^2 = \omega_1\omega_2$
- (D) None of the above

QUESTION 9.33

Consider the network shown below :



The zeros of the transfer function of the network are

- (A) $0, -\frac{1}{RC}$
- (B) $0, \frac{1}{RC}$
- (C) $0, -RC$
- (D) $0, RC$

QUESTION 9.34

In previous question the poles of the transfer function of the network are

- (A) $-\frac{1}{RC} + \sqrt{\left(\frac{1}{RC}\right)^2 - \frac{4}{LC}}, -\frac{1}{RC} - \sqrt{\left(\frac{1}{RC}\right)^2 - \frac{4}{LC}}$
- (B) $\frac{1}{RC} + \sqrt{\left(\frac{1}{RC}\right)^2 - \frac{4}{LC}}, \frac{1}{RC} - \sqrt{\left(\frac{1}{RC}\right)^2 - \frac{4}{LC}}$
- (C) $-\frac{1}{RC} + \sqrt{\left(\frac{1}{RC}\right)^2 + \frac{4}{LC}}, -\frac{1}{RC} - \sqrt{\left(\frac{1}{RC}\right)^2 + \frac{4}{LC}}$
- (D) $\frac{1}{RC} + \sqrt{\left(\frac{1}{RC}\right)^2 + \frac{4}{LC}}, \frac{1}{RC} - \sqrt{\left(\frac{1}{RC}\right)^2 + \frac{4}{LC}}$

QUESTION 9.35

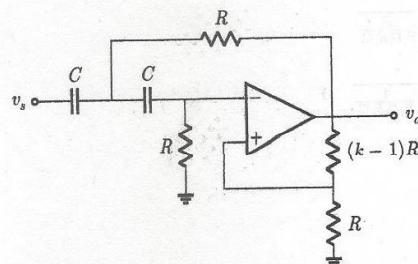
In Q 33 the network is a

- (A) low pass filter
- (B) high pass filter
- (C) band stop filter
- (D) band pass filter



QUESTION 9.36

Consider the following circuit



The above circuit is

- (A) Low pass filter
- (B) Band pass filter
- (C) Band Reject filter
- (D) High pass filter

QUESTION 9.37

In previous question what is the gain of the filter at cut-off frequency?

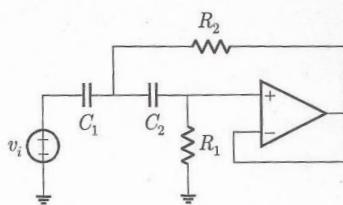
- (A) $\frac{k}{3+k}$
- (B) $\frac{3-k}{k}$
- (C) k
- (D) $\frac{k}{3-k}$

$$(C) \frac{1}{\sqrt{R_2 C_2 R_1 C_1}}$$

$$(D) \frac{1}{R_2 C_2 R_1 C_1}$$

QUESTION 9.38

Consider a high-pass Sallen and Key filter shown below



The transfer function of the filter is

- (A) $\frac{s^2}{s^2 + \left(\frac{C_1 + C_2}{C_1 R_1 C_2}\right)s + \frac{1}{R_1 C_2 R_1 C_1}}$
- (B) $\frac{s^2}{s^2 + \left(\frac{C_1 + C_2}{C_1 R_1 C_2}\right)s + \frac{1}{R_1 C_2 R_1 C_1}}$
- (C) $\frac{s^2}{1 + \left(\frac{C_1 + C_2}{C_1 R_1 C_2}\right)s + \frac{s^2}{R_1 C_2 R_1 C_1}}$
- (D) $\frac{1}{s^2 + \left(\frac{C_1 + C_2}{C_1 R_1 C_2}\right)s + \frac{1}{R_1 C_2 R_1 C_1}}$

QUESTION 9.39

In previous question pole frequency, ω_p of the second order filter function is

- (A) $\frac{1}{\sqrt{R_2 C_2}}$
- (B) $\frac{1}{\sqrt{R_1 C_1}}$

QUESTION 9.40

Pole quality factor, Q of the second order filter function is

- (A) $\sqrt{\frac{C_2 R_1}{C_1 R_2}} \left(\frac{1}{C_1 + C_2} \right)$
- (B) $\sqrt{\frac{C_2 C_1 R_2}{R_1}} \left(\frac{1}{C_1 + C_2} \right)$
- (C) $\sqrt{\frac{C_1 R_1}{C_2 R_2}} \left(\frac{1}{C_1 + C_2} \right)$
- (D) $\sqrt{\frac{C_2 C_1 R_1}{R_2}} \left(\frac{1}{C_1 + C_2} \right)$

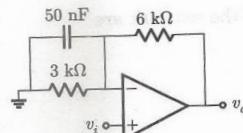
QUESTION 9.41

In an ideal band pass filter,

- (A) Pass band gain is 0 dB and stop band gain is $-\infty$ dB
- (B) Pass band gain is 1 dB and stop band gain is 0 dB
- (C) Pass band gain is 1 dB and width of transition band is 0
- (D) Transition bands have different gain roll off

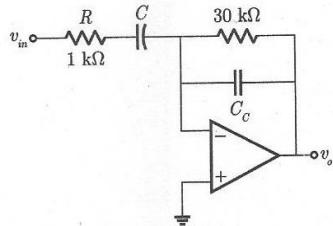
QUESTION 9.42

In the following circuit the 3 dB cutoff frequency is



QUESTION 9.43

Consider a bandpass filter circuit shown in figure below.

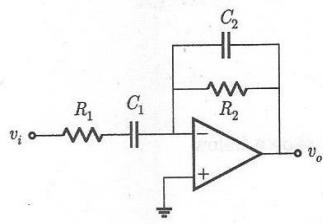


If due to capacitor C , frequency $f_1 = 1\text{ kHz}$ and due to capacitor C_C , frequency $f_2 = 5\text{ kHz}$. Then, the values of C and C_C respectively are

- (A) $1.1\text{ nF}, 0.159\text{ }\mu\text{F}$
- (B) $1\text{ }\mu\text{F}, 33.3\text{ nF}$
- (C) $33.3\text{ nF}, 1\text{ }\mu\text{F}$
- (D) $0.159\text{ }\mu\text{F}, 1.1\text{ nF}$

QUESTION 9.44

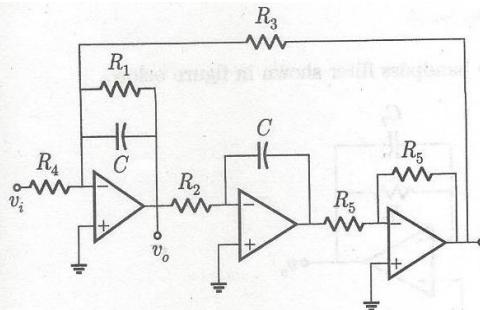
The following op-amp circuit is



- (A) Band-pass filter
- (B) Second order low pass filter
- (C) Second order high pass filter
- (D) Band Reject filter

QUESTION 9.45

Consider the bandpass filter shown in figure.



Assume

$$\begin{aligned}C &= 0.1\text{ }\mu\text{F}, \\R_1 &= 85\text{ k}\Omega, \\R_2 &= R_3 = 300\text{ }\Omega, \\R_4 &= 3\text{ k}\Omega, \text{ and} \\R_5 &= 30\text{ }\Omega.\end{aligned}$$

The maximum voltage gain, $|A_v(\max)|$ is

- (A) 85
- (B) 0.036
- (C) 0.33
- (D) 28.3

QUESTION 9.46

In previous question the frequency, f_0 at which $|A_v(\max)|$ occurs is

- (A) 2.653 kHz
- (B) 5.305 kHz
- (C) 10.6 kHz
- (D) 1.59 kHz

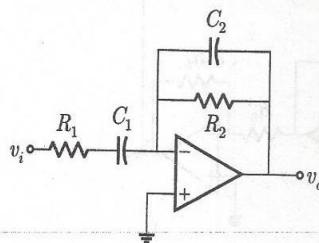
QUESTION 9.47

In Q 45 the 3 dB frequencies of the bandpass filter are

- (A) $5.296\text{ kHz}, 5.315\text{ kHz}$
- (B) $10.592\text{ kHz}, 10.63\text{ kHz}$
- (C) $2.648\text{ kHz}, 2.657\text{ kHz}$
- (D) $7.489\text{ kHz}, 7.516\text{ kHz}$

QUESTION 9.48

Consider the bandpass filter shown in figure below.



- (A) Low pass filter
- (B) High pass filter
- (C) All pass filter
- (D) Band pass filter

The voltage transfer function of the bandpass filter is

- (A) $-\frac{R_2}{R_1} \left[\frac{1}{sR_1C_1} + \left(1 + \frac{R_2C_2}{R_1C_1}\right) + sR_2C_2 \right]$
- (B) $\frac{R_2}{R_1} \left[\frac{1}{sR_1C_1} + \left(1 + \frac{R_2C_2}{R_1C_1}\right) + sR_2C_2 \right]$
- (C) $-\frac{R_2}{R_1} \left[\frac{1}{sR_2C_2} + \left(1 + \frac{R_2C_2}{R_1C_1}\right) + sR_1C_1 \right]$
- (D) $\frac{R_2}{R_1} \left[\frac{1}{sR_2C_2} + \left(1 + \frac{R_2C_2}{R_1C_1}\right) + sR_1C_1 \right]$

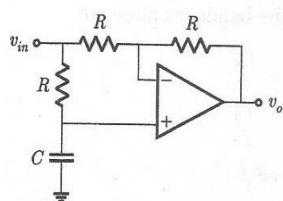
QUESTION 9.49

In previous question if $R_1 = 10 \text{ k}\Omega$, what will be the values of R_2 , C_1 , and C_2 such that the magnitude of the midband gain is 50 and the cutoff frequencies are 200 Hz and 5 kHz?

R_2 (in $\text{k}\Omega$)	C_1 (in μF)	C_2 (in pF)
(A) 66.3	524	0.0732
(B) 524	0.0732	66.3
(C) 66.3	524	0.0732
(D) 524	66.3	0.0732

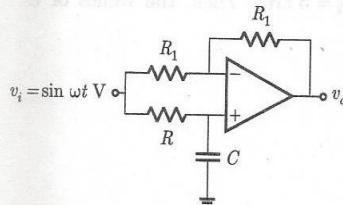
QUESTION 9.50

The following circuit is



QUESTION 9.51

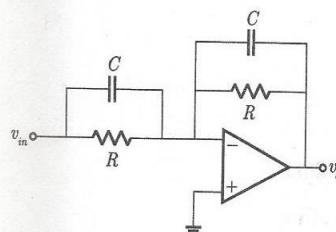
In the following circuit, output voltage is $|v_o| = 1 \text{ V}$ for a certain set of ω , R , and C . The $|v_o|$ will be 2 V if



- (A) ω is doubled
- (B) ω is halved
- (C) R is doubled
- (D) None of the above

QUESTION 9.52

Consider the following circuit shown below



The circuit is

- (A) low pass filter
- (B) all pass filter
- (C) Band reject filter
- (D) high pass filter

QUESTION 9.53

We wish to design a Butterworth filter with a roll-off of 1 dB at $\omega = 0.9\omega_0$. What is the required order of the Butterworth filter? (ω_0 is the pass band edge)

- (A) 7th order
- (B) 6th order
- (C) 9th order
- (D) 8th order

QUESTION 9.54

A low-pass filter is to have a cutoff frequency of 10 kHz and is to have a gain at 20 kHz, which is reduced by at least 25 dB from its maximum value. What is the minimum number of poles required for a Butterworth filter?

- (A) 5
- (B) 6
- (C) 4
- (D) 7

QUESTION 9.55

A low-pass Butterworth filter must provide a passband flatness of 0.5 dB for $f < f_i = 1 \text{ MHz}$. If the order of the filter must not exceed 5, what is the greatest stopband attenuation at $f = 2 \text{ MHz}$?

dB

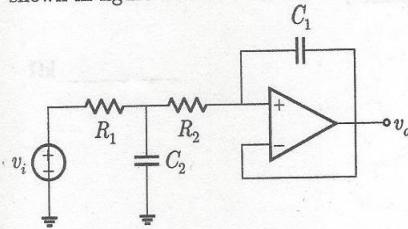
QUESTION 9.56

The roll-off rate in fourth order Butterworth low pass filter will be

- (A) 80 dB per decade
- (B) 80 dB per octave
- (C) 24 dB per decade
- (D) 12 dB per octave

QUESTION 9.57

A student mistakenly configures a Sallen and Key filter as shown in figure. Transfer function of the filter is



- (A) $\frac{1}{1 + sR_1 C_2}$
- (B) $\frac{1}{1 - sR_1 C_2}$
- (C) $\frac{sC_2}{R_1 + sC_2}$
- (D) $\frac{sC_2}{R_1 - sC_2}$

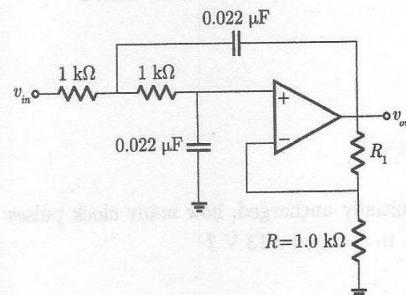
QUESTION 9.58

In previous question the designed circuit is not useful because

- (A) it has not a finite zero.
- (B) we can implement it with the passive components only, instead of op-amp.
- (C) it is only a simple high pass filter.
- (D) None of these

QUESTION 9.59

Consider the salien-key low pass filter shown below.

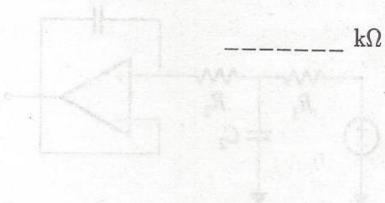


What is the value of 3-dB frequency?

kHz

QUESTION 9.60

In previous question what is value of R_1 for an approximate butter worth response ?



_____ k Ω

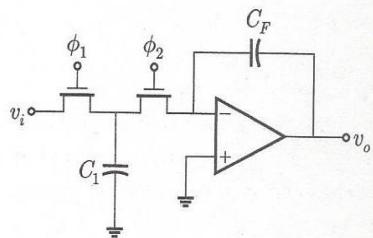
QUESTION 9.64

For sustaining oscillations in an oscillator

- (A) feedback factor should be unity
- (B) phase shift should be zero
- (C) feedback should be negative
- (D) both (A) and (B)

QUESTION 9.61

Consider a switched capacitor integrator shown in figure below



Let $C_F = 30 \text{ pF}$ and $C_1 = 5 \text{ pF}$, and assume the clock frequency is 100 kHz. Also, let $v_i = 1 \text{ V}$. What is the integrating RC time constant for the circuit ?

_____ μsec

QUESTION 9.62

In previous question the change in output voltage during each clock period will be ?

_____ Volt

QUESTION 9.65

The most important characteristic of a crystal oscillator is

- (A) its high efficiency
- (B) that it requires very low d.c. supply
- (C) that its output frequency is substantially constant
- (D) it has low cost

QUESTION 9.66

To generate 1 MHz frequency, the most suitable circuit is

- (A) phase-shift oscillator
- (B) Wein bridge oscillator
- (C) Colpitt's oscillator
- (D) none of the above

QUESTION 9.63

In Q 61 if C_F is initially uncharged, how many clock pulses are required for v_o to change by 13 V ?

QUESTION 9.67

For generating 1 kHz frequency, the most suitable circuit is

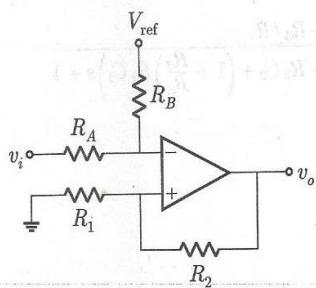
- (A) tuned collector oscillator
- (B) Hartley oscillator
- (C) Colpitt's oscillator
- (D) Wein bridge oscillator

QUESTION 9.68

- In R-C phase shift oscillator
- no need for feedback
 - feedback factor is less than unity
 - pure sine wave output is possible
 - square waves are produced

QUESTION 9.69

For the Schmitt trigger shown in figure below, assume $R_A = 10 \text{ k}\Omega$, $R_B = 20 \text{ k}\Omega$, $R_1 = 5 \text{ k}\Omega$, $R_2 = 20 \text{ k}\Omega$, $V_{\text{ref}} = 2 \text{ V}$ and the saturated output voltages are $\pm 10 \text{ V}$. What is the upper crossover voltage, V_{TH} ?

**QUESTION 9.70**

In previous question what is the lower crossover voltage, V_{TL} ?

----- Volt

QUESTION 9.71

A retriggerable monostable multivibrator is designed for an output pulse width of $400 \mu\text{s}$. If it were fed with 11 trigger pulses with successive trigger pulses separated by $10 \mu\text{s}$, the output pulse width would be

----- μs

QUESTION 9.72

In the basic clamper circuit, positive or negative, resistance R is always connected across the diode. If the forward-biased and reverse biased resistances of the diode were 10Ω and $10 \text{ M}\Omega$, respectively, the most optimum value of R would then be

- 10Ω
- $10 \text{ M}\Omega$
- $100 \text{ k}\Omega$
- $10 \text{ k}\Omega$

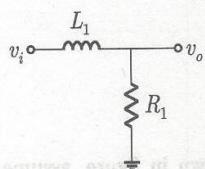
QUESTION 9.73

A Chebyshev filter must provide an attenuation of 25 dB at 5 MHz . If the order of the filter must not exceed 5, what is the minimum ripple that can be achieved across a bandwidth of 2 MHz ?

- $-0.42 \times 10^{-4} \text{ dB}$
- $-8.6 \times 10^{-4} \text{ dB}$
- $-4.3 \times 10^{-6} \text{ dB}$
- $1.97 \times 10^{-4} \text{ dB}$

QUESTION 9.74

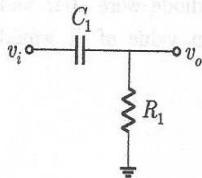
We wish to achieve a pole sensitivity of 5% in the given circuit below. If R_1 exhibits a variability of 3% , what is the maximum tolerance of L_1 ?



----- %

QUESTION 9.75

Consider the high-pass filter shown below :



(A) $\frac{1}{R_1 C_1}$

(B) $\frac{1}{R_1 C_1}, 0$

(C) $0, \frac{1}{R_1 C_1}$

- (D) $\frac{1}{R_1 C_1}, 0$

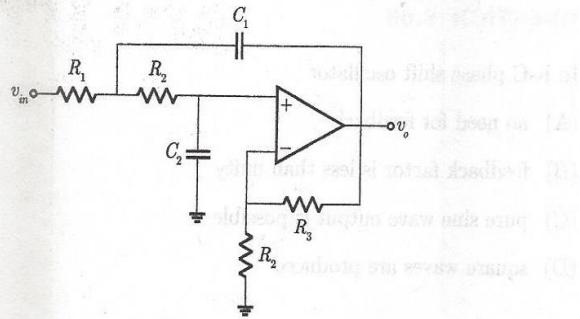
QUESTION 9.6

In previous question the sensitivities, $S_{R_1}^P$ and $S_{C_1}^P$ of the pole frequency with respect to R_1 and C_1 , respectively will be

- | | |
|-------------|-------------|
| $S_{R_1}^P$ | $S_{C_1}^P$ |
| (A) -1 | 1 |
| (B) 1 | 1 |
| (C) -1 | -1 |
| (D) 1 | -1 |

QUESTION 9.77

Consider a salien and key filter is shown in figure, assume op-amp is ideal.



The pole and zero of the transfer function are respectively

(A) $0, -\frac{1}{R_1 C_1}$

(B) $-\frac{1}{R_1 C_1}, 0$

(C) $0, \frac{1}{R_1 C_1}$

(D) $\frac{1}{R_1 C_1}, 0$

The transfer function of the filter.

(A) $\frac{1}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_2 + R_2 C_1)s + 1}$

(B) $\frac{1 + R_3/R_4}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_2 + R_2 C_1)s + 1}$

(C) $\frac{1 + R_3/R_4}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_2 + R_2 C_1 - R_1 \frac{R_3}{R_4} C_1)s + 1}$

(D) $\frac{-R_3/R_4}{R_1 R_2 C_1 C_2 s^2 + (R_1 C_2 + R_2 C_1 + (1 + \frac{R_3}{R_4}) R_1 C_1)s + 1}$

QUESTION 9.78

In previous question the circuit is a

- (A) low pass filter
 (B) High pass filter
 (C) Band-stop filter
 (D) All pass filter

QUESTION 9.79

In Q 77 the Pole frequency (ω_n) sensitivity with respect to R_1 , is

(A) -1

(B) $-1/2$

(C) +1

(D) $+1/2$

Answer

9.1	A
9.2	A
9.3	B
9.4	A
9.5	C
9.6	A
9.7	B
9.8	-7
9.9	B
9.10	B
9.11	B
9.12	-18.1
9.13	D
9.14	D
9.15	A
9.16	D
9.17	D
9.18	D
9.19	B
9.20	A
9.21	3.1
9.22	D
9.23	B
9.24	A
9.25	D
9.26	A
9.27	C
9.28	1.5
9.29	D
9.30	B
9.31	D
9.32	C
9.33	A
9.34	A
9.35	B
9.36	D
9.37	D
9.38	A
9.39	C
9.40	D

9.41	A
9.42	1.59
9.43	D
9.44	A
9.45	D
9.46	B
9.47	A
9.48	A
9.49	B
9.50	C
9.51	D
9.52	B
9.53	A
9.54	A
9.55	-21
9.56	A
9.57	A
9.58	B
9.59	7.23
9.60	586
9.61	60
9.62	0.167
9.63	78
9.64	D
9.65	C
9.66	C
9.67	D
9.68	C
9.69	2
9.70	-2
9.71	500 usec.
9.72	D
9.73	B
9.74	2
9.75	B
9.76	C
9.77	C
9.78	A
9.79	B

CHAPTER 10

FEEDBACK AMPLIFIER AND OSCILLATOR



QUESTION 10.1

A voltage amplifier has an open-loop gain of 100. If 10% negative feedback were introduced in the amplifier, then an 11% change in open-loop gain would cause

- (A) 1% change in closed-loop gain
- (B) 11% change in closed-loop gain
- (C) 1.1% change in closed-loop gain
- (D) 0.1% change in closed-loop gain

QUESTION 10.2

In the case of a negative-feedback amplifier, which of the following is true?

- (A) Closed-loop gain can be less than or more than the open-loop gain depending upon the type and amount of feedback.
- (B) Closed-loop gain is always less than the open-loop gain
- (C) Closed-loop gain is always more than the open-loop gain
- (D) Closed-loop gain and bandwidth are always less than the corresponding open-loop values.

QUESTION 10.3

In a negative-feedback amplifier with a high open-loop gain, doubling the feedback factor

- (A) doubles the closed-loop gain too.
- (B) has no effect on closed-loop gain
- (C) reduces the closed-loop gain to one-fourth
- (D) reduces the closed-loop gain to one-half

QUESTION 10.4

In a negative feedback amplifier, the phase difference between an input signal and a feedback signal is

- (A) 0°
- (B) 180°
- (C) 270°
- (D) 90°

QUESTION 10.5

Which one of the following effects is a result of application of negative feedback?

- (A) the bandwidth decreases
- (B) the harmonic distortion decreases
- (C) the harmonic distortion increases
- (D) the noise increases

QUESTION 10.6

Expression for distortion D' with negative feedback, with usual notation is $D' =$

- (A) $\frac{D}{1-\beta A}$
- (B) $D(1-bA)$
- (C) $\frac{D}{1+\beta A}$
- (D) $D(1+bA)$

QUESTION 10.7

An amplifier without feedback has a voltage gain of 50, input resistance of $1\text{ k}\Omega$ and output resistance of $2.5\text{ k}\Omega$. The input resistance of the current-shunt negative feedback amplifier using the above amplifier with a feedback factor of 0.2 is

- (A) $\frac{1}{11}\text{ k}\Omega$
- (B) $\frac{1}{5}\text{ k}\Omega$
- (C) $5\text{ k}\Omega$
- (D) $11\text{ k}\Omega$

QUESTION 10.8

A negative feedback amplifier has a closed loop gain of $A_f = 80$ and an open loop gain of $A = 10^5$. If the open loop gain decreases by 20% then the percent change in the closed loop gain and new value of close loop gain A_f will be respectively

- (A) 0.016%, 80.01
- (B) -0.016%, 79.99
- (C) 0.004%, 79.68
- (D) -0.004, 80.32

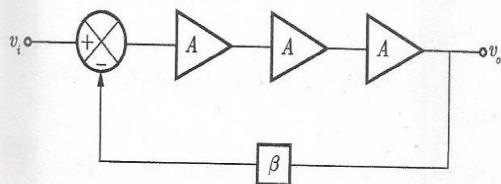
QUESTION 10.9

Consider a basic amplifier circuit having input resistance, $R_i = 10\text{ k}\Omega$ and output resistance, $R_o = 1\text{ k}\Omega$, and loop gain is $T = 10^4$. What are the maximum possible output resistance and minimum possible input resistance respectively.

- (A) $1\Omega, 10^4\text{ k}\Omega$
- (B) $\infty\Omega, 0\Omega$
- (C) $10^{-1}\Omega, 10\text{ M}\Omega$
- (D) $10^4\text{k}, 1\Omega$

QUESTION 10.10

A feedback amplifier shown in figure

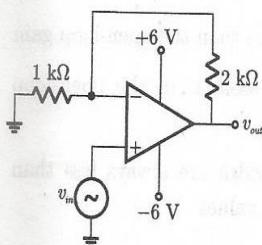


Each basic amplifier stage has an open loop gain of $A = 10$. The closed loop gain is $A_f = 100$. If the gain of each stage increased by 10%. What is the percent change in the closed loop voltage gain $\frac{v_o}{v_i}$ is

- (A) 2.55% increase
- (B) 2.55% decrease
- (C) 1% increase
- (D) 0.9 increase

QUESTION 10.11

The nature of feedback in the op-amp circuit shown is



- (A) Current-Current feedback
- (B) Voltage-Voltage feedback
- (C) Current-Voltage feedback
- (D) Voltage-Current feedback

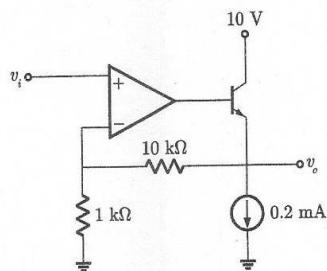
QUESTION 10.12

The common-collector bias and emitter-bias are examples of

- (A) voltage-series feedback
- (B) voltage-series feedback and voltage-shunt feedback, respectively.
- (C) voltage-series feedback and current-series feedback, respectively
- (D) current-series feedback and current-shunt feedback, respectively

QUESTION 10.13

Consider the circuit shown below.



This amplifier circuit will be

- (A) Series-Series
- (B) Series-shunt
- (C) Shunt-Series
- (D) Shunt-Shunt

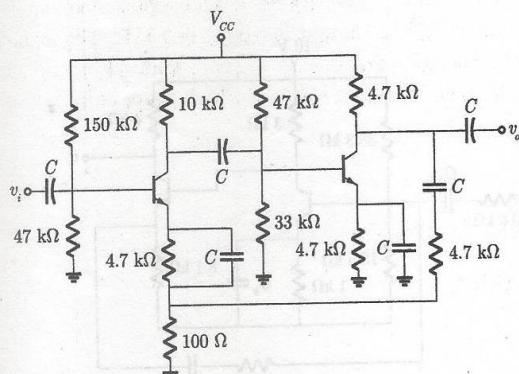
QUESTION 10.14

An op-amp has an open loop low frequency gain of $A = 10^5$ and an open loop 3 dB frequency $f_H = 4$ Hz. If an inverting amplifier with a closed loop low frequency gain of $|A_{vf}| = 50$ uses this op-amp. What is the value of the closed loop bandwidth?

_____ kHz

QUESTION 10.15

Consider the amplifier circuit shown below.



The type of amplifier circuit is

- (A) series-series
- (B) series-shunt
- (C) shunt-series
- (D) shunt-shunt

QUESTION 10.16

In which of the following feedback topologies, the input impedance decreases with introduction of feedback.

- (A) Voltage-shunt feedback
- (B) Current-series feedback
- (C) Voltage-series feedback
- (D) None of these

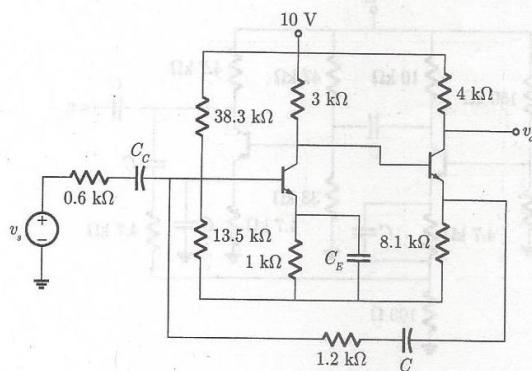
QUESTION 10.17

In which of the following feedback topologies, both input as well as output impedances decrease with introduction of feedback.

- (A) Voltage-shunt feedback
- (B) Current-shunt feedback
- (C) Voltage-series feedback
- (D) None of these

QUESTION 10.18

Consider the amplifier circuit shown below.

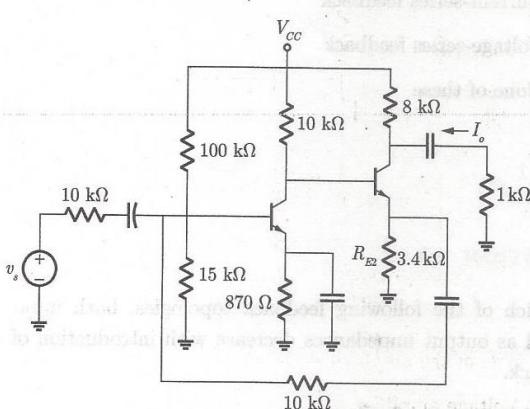


The type of the amplifier circuit will be

- (A) Series-Series
- (B) Series-Shunt
- (C) Shunt-Series
- (D) Shunt-Shunt

QUESTION 10.19

Consider the feedback amplifier circuit shown below. What is the feedback factor (β) of the circuit ?



QUESTION 10.20

It is desired to design a voltage controlled current source. What type of negative feedback should preferably be introduced to make it a stable source ?

- (A) Voltage-series feedback
- (B) Current-series feedback
- (C) Current-shunt feedback
- (D) Voltage-shunt feedback

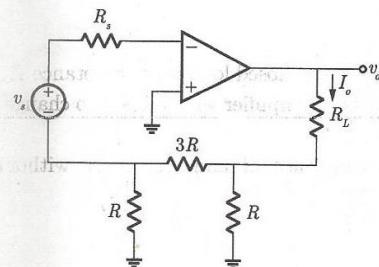
QUESTION 10.21

An amplifier with open-loop input resistance of $100\text{ k}\Omega$ has -20 dB of voltage-series feedback. Closed loop input resistance would be

- (A) $10\text{ k}\Omega$
- (B) $1000\text{ k}\Omega$
- (C) $2000\text{ k}\Omega$
- (D) $5\text{ k}\Omega$

QUESTION 10.22

Consider the circuit shown below.



The type of amplifier and feedback factor of the amplifier are

- (A) Series-Voltage, $\beta = -\frac{R}{5}$
- (B) Series-Current, $\beta = -\frac{R}{4}$
- (C) Shunt-current, $\beta = -\frac{R}{4}$
- (D) Series-Current, $\beta = -\frac{R}{5}$

QUESTION 10.23

A compound transconductance amplifier is to be designed by connecting two basic feedback amplifier in cascade. Which of the two amplifier should be connected in cascade to form the compound transconductance amplifier?

- (A) Series - Series Series - Series
- (B) Series - Series Shunt - Series
- (C) Series - Shunt Series - Series
- (D) (B) & (C)

Amplifier with shunt feedback should be used to obtain a feedforward to minimize the distortion in compound transconductance amplifier.

QUESTION 10.24

In which of the following feedback topologies, the input impedance increases with introduction of feedback.

- (A) Voltage-shunt feedback
- (B) Current-shunt feedback
- (C) Voltage-series feedback
- (D) None of these

QUESTION 10.25

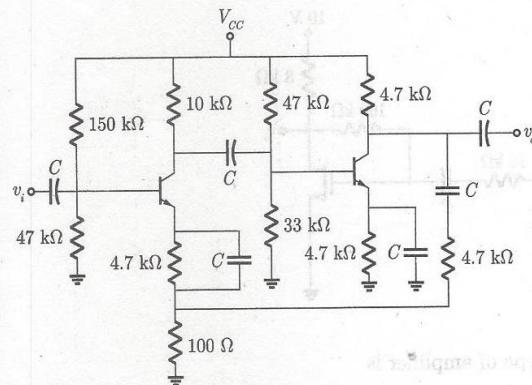
What is the sensitivity of the closed-loop input resistance R_{in} of the series-shunt feedback amplifier with respect to changes in open gain A ?

(assume that input resistance of amplifier is R without feedback and $A\beta \gg 1$)

- (A) 1
- (B) -1
- (C) 0
- (D) ∞

QUESTION 10.26

Consider the amplifier circuit shown below.

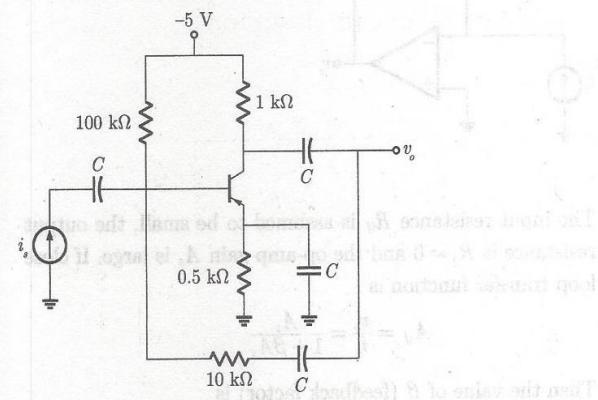


The type of amplifier circuit is

- (A) series-series
- (B) series-shunt
- (C) shunt-series
- (D) shunt-shunt

QUESTION 10.27

Consider the common-emitter amplifier circuit shown below.

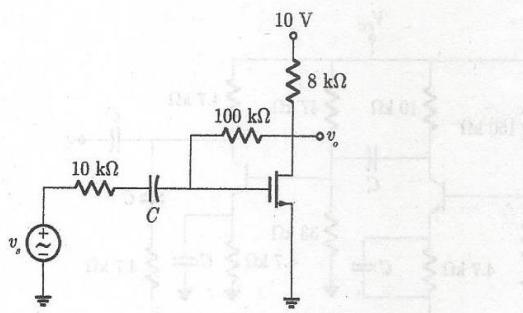


The type of the amplifier circuit is

- (A) Voltage amplifier
- (B) current amplifier
- (C) trans resistance amplifier
- (D) trans conductance amplifier

QUESTION 10.28

Consider the circuit shown below

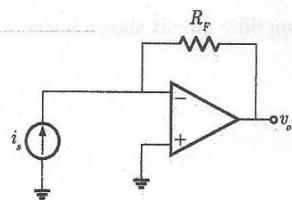


The type of amplifier is

- (A) Voltage amplifier
- (B) current amplifier
- (C) transconductance amplifier
- (D) transresistance amplifier

QUESTION 10.29

Consider the current to voltage convertor circuit shown below



The input resistance R_{if} is assumed to be small, the output resistance is $R_o = 0$ and the op-amp gain A_z is large. If close loop transfer function is

$$A_{zf} = \frac{v_o}{i_s} = \frac{A_z}{1 + \beta A_z}$$

Then the value of β (feedback factor) is

- (A) R_F
- (B) $\frac{1}{R_F}$
- (C) $\frac{R_F}{A_z}$
- (D) $\frac{A_z}{R_F}$

QUESTION 10.30

Voltage-shunt feedback stabilizes

- (A) voltage gain
- (B) current gain
- (C) transresistance
- (D) transconductance

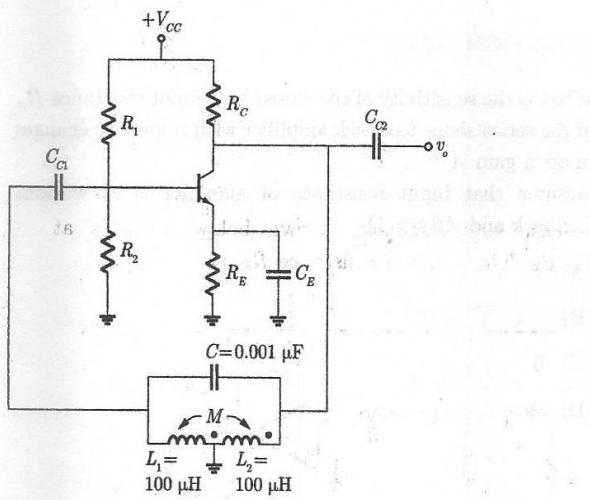
QUESTION 10.31

In which of the following feedback topologies, the output impedance increases with introduction of feedback.

- (A) Voltage-shunt feedback
- (B) Current-shunt feedback
- (C) Voltage-series feedback
- (D) None of these

QUESTION 10.32

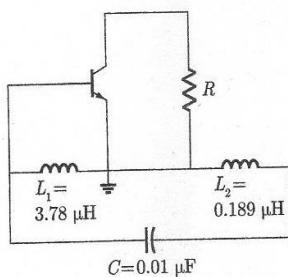
The Hartley oscillator shown in figure. The mutual inductance between L_1 and L_2 is $M = 20\text{ }\mu\text{H}$, what is the value of frequency for oscillations ?



kHz

QUESTION 10.33

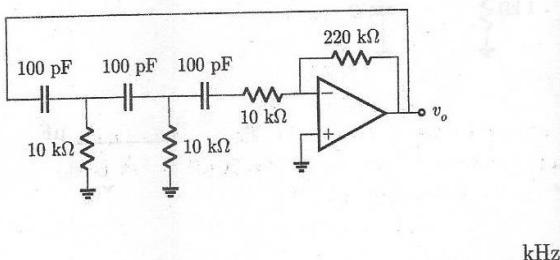
For the Hartley oscillator shown in figure, what is the value of oscillation frequency ?



$$\text{Frequency} = \frac{1}{2\pi\sqrt{L_1(L_1 + L_2)C}} \quad \text{kHz}$$

QUESTION 10.34

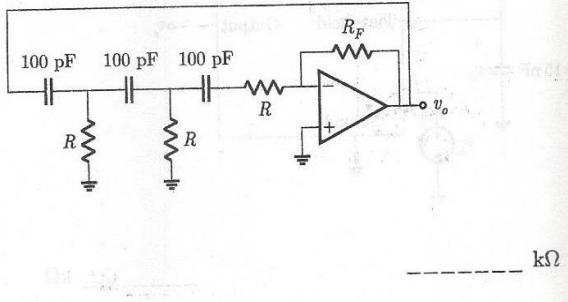
For the following phase-shift oscillator, frequency of oscillation is nearly equal to



$$\text{kHz}$$

QUESTION 10.35

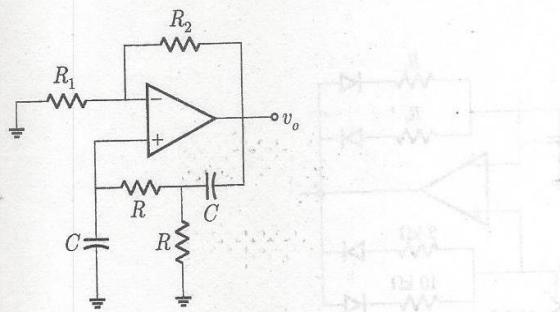
The phase shift oscillator shown below operates at $f = 80 \text{ kHz}$. The value of resistance R_F is



$$\text{k}\Omega$$

QUESTION 10.36

Consider the circuit shown in the figure below.

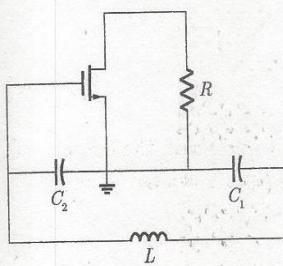


For sustained oscillation, the value of R_2/R_1 must be equal to

- (A) 2
- (B) 0.5
- (C) 3
- (D) 1

QUESTION 10.37

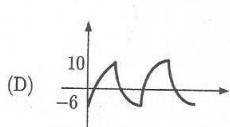
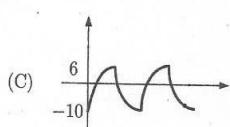
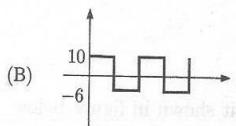
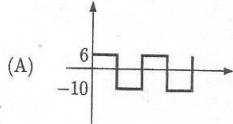
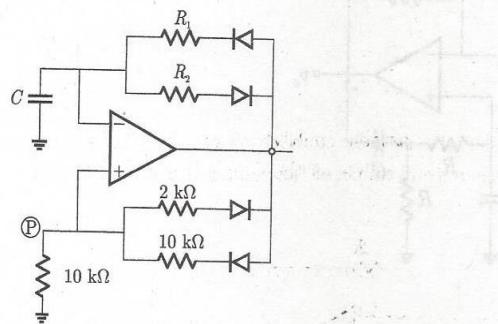
Consider the colpitts oscillator circuit shown in figure below with parameters $L = 1 \mu\text{H}$, $C_1 = 1 \text{nF}$, $C_2 = 1 \text{nF}$, $R = 4 \text{k}\Omega$. What is the oscillator frequency ?



$$\text{MHz}$$

QUESTION 10.36

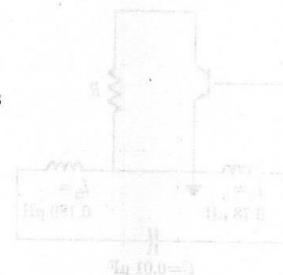
A relaxation oscillator is made using Op-amp as shown in figure. The supply voltages of the Op-amps are ± 12 V. The voltage waveform at point P will be



QUESTION 10.39

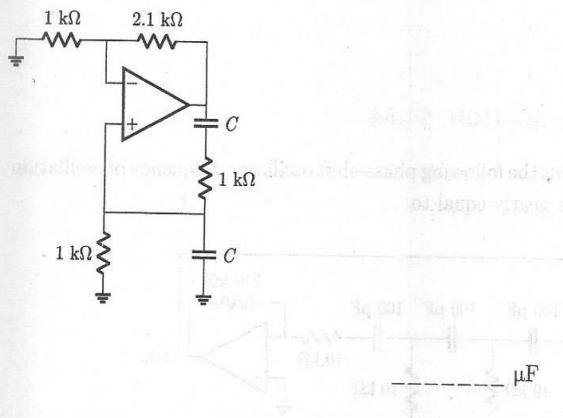
The phase-shift oscillator usually has

- (A) one lead-lag circuit
- (B) one lead or lag circuit
- (C) two lead or lag circuits
- (D) three lead or lag circuits



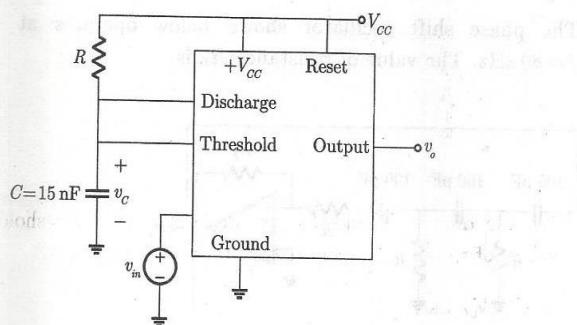
QUESTION 10.40

The value of C required for sinusoidal oscillation of frequency 1 kHz in the following circuit is



QUESTION 10.41

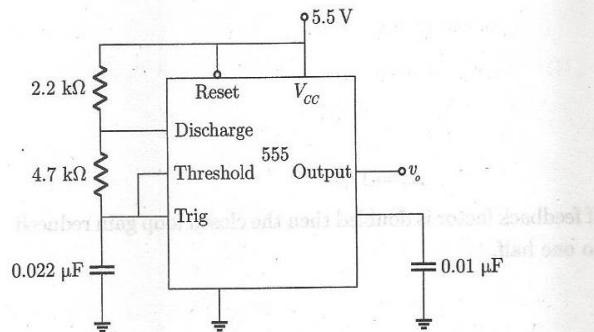
Consider the monostable multivibrator circuit shown below. If the monostable multivibrator with a $100\mu s$ output pulse then the value of R is



$k\Omega$

QUESTION 10.42

Consider the 555 time configured in the astable mode (oscillator) is shown below.

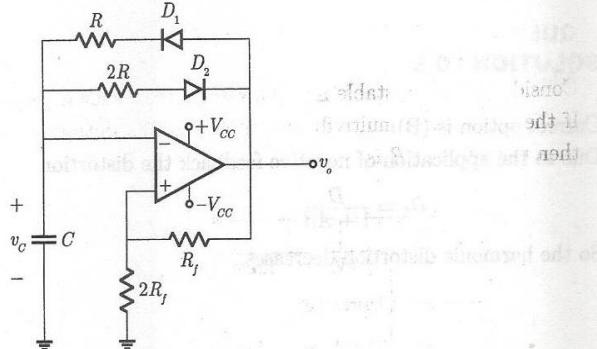


What is the frequency of output and duty cycle ?

- (A) $7.69 \text{ k}\Omega, 59.4\%$
- (B) $5.64 \text{ kHz}, 59.4\%$
- (C) $5.64 \text{ k}\Omega, 50\%$
- (D) $7.69 \text{ k}\Omega, 50\%$

QUESTION 10.43

Consider the modified astable multivibrator shown below.



Assume diodes D_1 and D_2 are ideal. For what threshold values of v_c does the schmitt trigger change state ?

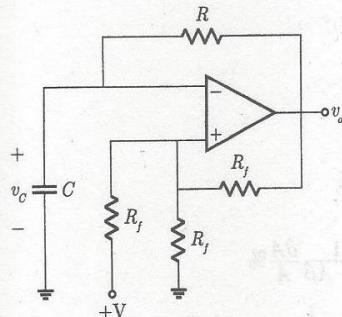
- (A) $\frac{2}{3} V_{cc}$ and $\frac{1}{3} V_{cc}$
- (B) $\frac{1}{3} V_{cc}$ and $-\frac{1}{3} V_{cc}$

- (C) $\frac{2}{3} V_{cc}$ and $-\frac{2}{3} V_{cc}$

- (D) V_{cc} and $-V_{cc}$

QUESTION 10.44

Consider the astable multivibrator shown below (Assume that the output values of the comparator are 0 and V)



For what threshold values of v_c does the schmitt trigger change state ?

- (A) $\frac{V}{2}$ and $-\frac{V}{2}$
- (B) $\frac{V}{2}$ and 0
- (C) $\frac{V}{3}$ and $\frac{2V}{3}$
- (D) $\frac{V}{3}$ and 0

Answer

10.1	A
10.2	B
10.3	D
10.4	B
10.5	B
10.6	C
10.7	A
10.8	B
10.9	D
10.10	A
10.11	B
10.12	C
10.13	B
10.14	8
10.15	B
10.16	A
10.17	A
10.18	C
10.19	-0.254
10.20	B
10.21	B
10.22	D

10.23	D
10.24	C
10.25	A
10.26	B
10.27	C
10.28	D
10.29	B
10.30	C
10.31	B
10.32	324.87
10.33	800
10.34	65
10.35	236
10.36	A
10.37	7.12
10.38	C
10.39	D
10.40	0.159
10.41	6.06
10.42	B
10.43	C
10.44	C