Gonzalez, Ilsia

CSE 140

Professor Jeon

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Homework #3

*MIPS Decoder:*

* *attached separate*

*Single-cycle MIPS Architecture:*

1. Assume that core components of single-cycle processor (shown below) have the following latencies:

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| I-Mem | Adder | Mux | ALU | Regs Rd/Wr | D-Mem | Sign-Extend | Shift-Left-2 |
| 40ps | 50ps | 20ps | 100ps | 80ps/60ps | 200ps | 20ps | 20ps |

Single-cycle processor data path:



Suppose that this data path executes only two types of instruction:

sub $rd, $rs, $rt & lw $rt, offset($rs)

What would be the clock period to correctly execute the two instructions on the above single-cycle processor? Assume that PC register doesn’t take any latency (i.e. Propagating a new PC value to I-Cache/I-Mem doesn’t take any cycle).

* For the instruction sub $rd, $rs, $rt we begin by fetching it from the I-Cache/I-MEM which has a latency of 40ps. Then it travels to the register file where we get read data 1 and 2. This is 80ps. This is then inputted to ALU which has a latency of 100ps. However, to get there it must go through a mux and with a latency of 20ps. Then its output is stored in register file with a 60ps. Also traveling through a mux (20ps). Now we add it together to get a total latency of 320ps
* As before lw $rt, offset($rs) is first gathered from the I-MEM. Then traveling to the register file. We get an output of read data 1. It travels through a mux and gets to ALU. It outputs a address that is given to D-Mem that then returns it back. Then the ALU is stored in the register file through a mux. Now we add the ps to get total latency which is 520ps
* So, in order for the processor to execute both of the instructions it will have a clock period of 520ps

*Single and Pipelined Datapaths*

2. Assume that the execution time of individual steps of an instruction execution are like below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| IF | ID | EX | MEM | WB |
| 100ps | 120ps | 220ps | 300ps | 120ps |

1. If you design a single-cycle processor with the above latency information, what is the clock latency?
   * For the total latency of this processor, we will add 100ps, 120ps, 220ps, 300ps, and 120ps. So, the clock latency is 860 ps.
2. If you design a five-stage pipelined processor with the above latency information, what is the clock latency?
   * In this instance a five stage pipelined processor is 300ps (MEM).