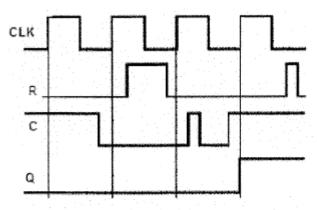
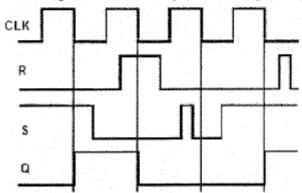


2.

Assuming that Q=0 initially (for the positive edge triggered S-C FF).

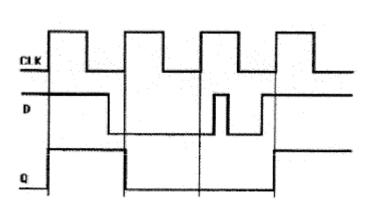


Assuming that Q=0 initially (for the negative edge triggered S-C FF).

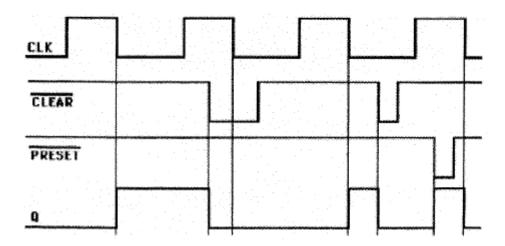


3.

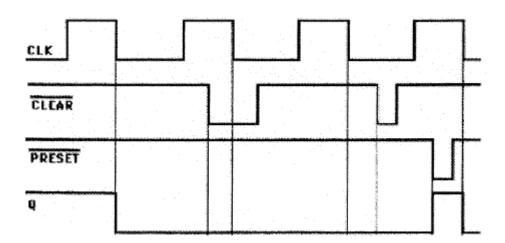
(a) Connect the J and K inputs permanently HIGH. The Q output will be a squarewave with a frequency of 5 KHz.



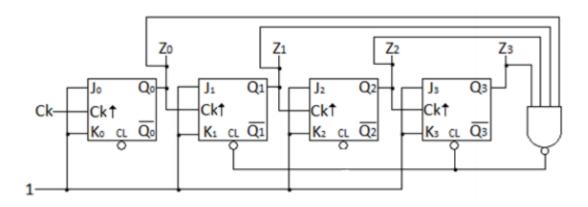
J=K=1 so FF will toggle on each CLK negative-going edge, unless either $\overline{\text{PRESET}}$ or $\overline{\text{CLEAR}}$ inputs is LOW.

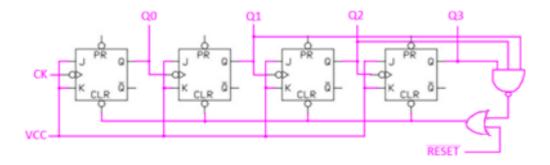


6.

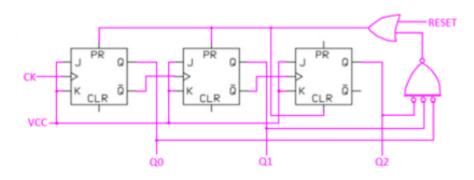


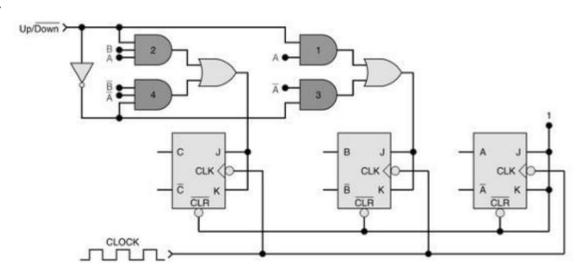
7. 10 FFs



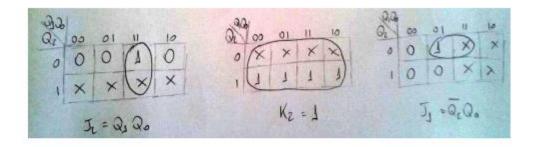


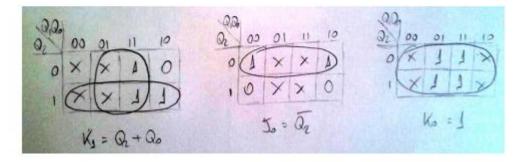
10.

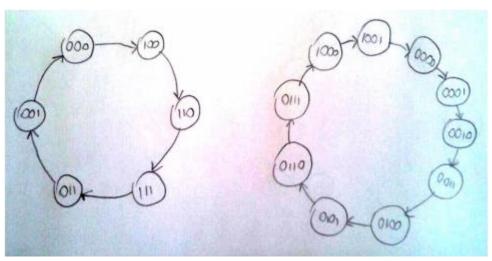




Qu	0,	Q.	72	Kz	J,	K	J.	Ko
0	0	0	0	×	0	×	1	×
0	0	1	0	×	1	X	×	1
0	1	0	0	×	×	0	Δ	×
0	1	1	7	X	×	7	X	7
7	0	0	×	1	0	X	0	X
1	0	1	×	1	0	X	×	7
1	1	0	×	7	×	1	0	X
1	1	1	X	1	X	7	×	1







14. a

CLOCK	LOAD	E.S	E.P.A	E.P.B	E.P.C	E.P.D	S.P.A	S.P.B	S.P.C	S.P.D	S.S
X	1	X	0	0	0	0	0	0	0	0	0
BD	0	1	X	X	X	X	1	0	0	0	0
BD	0	1	X	X	X	X	1	1	0	0	0
BD	0	0	X	X	X	X	0	1	1	0	0
BD	0	1	X	X	X	X	1	0	1	1	1
BD	0	1	X	X	X	X	1	1	0	1	1
BD	0	0	X	X	X	X	0	1	1	0	0
BD	0	0	X	X	X	X	0	0	1	1	1
BD	0	0	X	X	X	X	0	0	0	1	1
BD	0	0	X	X	X	X	0	0	0	0	0

b

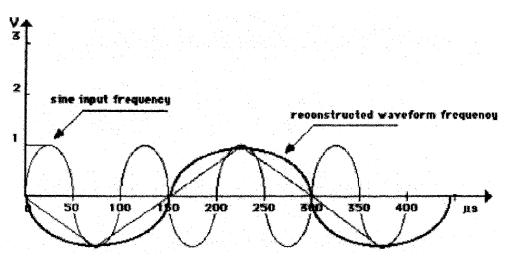
LOAD deve estar em nível baixo ALTO no momento do carregamento dos dados de entrada. Após isso, LOAD deve ir para nível BAIXO e devem ser aplicados 3 pulsos de clock para que os dados sejam apresentados de forma completa na saída serial.

FALSO. A resolução percentual só depende do número de bits! [1/((2^N)-1)]. Logo, a resolução percentual é a

mesma, independentemente do fundo de escala utilizado.

16. VERDADEIRO





- (a) Since the Flash ADC samples at intervals of 75μs, the sample frequency is 1/75μs =13.33 kHz.
- (b) The sine wave has a period of 100 μs or a F=10 kHz. Therefore, the difference between the sample frequency and the input sine wave frequency is 3.3 kHz.
- (c) The frequency of the reconstructed waveform is approximately 1/300 µs or 3.33 kHz.