Projeto Demonstrativo 6
Anexo - Descrição da CNN

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Na seguinte tabela, considere exp = “exped, dw = “depthwise”, exp = “expande”, proj = “project”.

Códigos:

- C1 = ZeroPadding2D
- C2 = Conv2D
- C3 = BatchNormalization
- C4 = Relu
- C5 = DepthwiseConvolution
- C6 = DepthCNN

Total params: 3,605,603
Trainable params: 3,571,491
Non-trainable params: 34,112

Layer (type)	Output Shape	Param	Connected to
input_1 (InputLayer)	(, 96, 96, 3)	0	
Conv1_pad C1	(, 97, 97, 3)	0	input_1[0][0]
Conv1 C2	(, 48, 48, 32)	864	Conv1_pad[0][0]
block_Conv1 C3	(, 48, 48, 32)	128	Conv1[0][0]
Conv1_relu C4	(, 48, 48, 32)	0	bn_Conv1[0][0]
exp_conv_dw C5	(, 48, 48, 32)	288	Conv1_relu[0][0]
exp_conv_dw_BN C3	(, 48, 48, 32)	128	exp_conv_dw[0][0]
exp_conv_dw_relu C4	(, 48, 48, 32)	0	exp_conv_dw_BN[0][0]
exp_conv_proj C2	(, 48, 48, 16)	512	exp_conv_dw_relu[0][0
exp_conv_proj_BN C3	(, 48, 48, 16)	64	exp_conv_proj[0][0]
block_1_exp C2	(, 48, 48, 96)	1536	exp_conv_proj_BN[0][0]
block_1_exp_BN C3	(, 48, 48, 96)	384	block_1_exp[0][0]
block_1_exp_relu C4	(, 48, 48, 96)	0	block_1_exp_BN[0][0]
block_1_pad C1	(, 49, 49, 96)	0	block_1_exp_relu[0][0]
block_1_dw C6	(, 24, 24, 96)	864	block_1_pad[0][0]
block_1_dw_BN C3	(, 24, 24, 96)	384	block_1_dw[0][0]
block_1_dw_relu C4	(, 24, 24, 96)	0	block_1_dw_BN[0][0]
block_1_proj C2	(, 24, 24, 24)	2304	block_1_dw_relu[0][0]
block_1_proj_BN C3	(, 24, 24, 24)	96	block_1_proj[0][0]
block_2_exp C2	(, 24, 24, 144)	3456	block_1_proj_BN[0][0]
block_2_exp_BN C3	(, 24, 24, 144)	576	block_2_exp[0][0]
block_2_exp_relu C4	(, 24, 24, 144)	0	block_2_exp_BN[0][0]
block_2_dw C6	(, 24, 24, 144)	1296	block_2_exp_relu[0][0]
block_2_dw_BN C3	(, 24, 24, 144)	576	block_2_dw[0][0]
block_2_dw_relu C4	(, 24, 24, 144)	0	block_2_dw_BN[0][0]
block_2_proj C2	(, 24, 24, 24)	3456	block_2_dw_relu[0][0]
block_2_proj_BN C3	(, 24, 24, 24)	96	block_2_proj[0][0]
block_2_add (Add)	(, 24, 24, 24)	0	block_1_proj_BN[0][0] block_2_proj_BN[0][0]
block_3_exp C2	(, 24, 24, 144)	3456	block_2_add[0][0]
block_3_exp_BN C3	(, 24, 24, 144)	576	block_3_exp[0][0]
block_3_exp_relu C4	(, 24, 24, 144)	0	block_3_exp_BN[0][0]
block_3_pad C1	(, 25, 25, 144)	0	block_3_exp_relu[0][0]
block_3_dw C6	(, 12, 12, 144)	1296	block_3_pad[0][0]
block_3_dw_BN C3	(, 12, 12, 144)	576	block_3_dw[0][0]
block_3_dw_relu C4	(, 12, 12, 144)	0	block_3_dw_BN[0][0]
block_3_proj C2	(, 12, 12, 32)	4608	block_3_dw_relu[0][0]
block_3_proj_BN C3	(, 12, 12, 32)	128	block_3_proj[0][0]
block_4_exp C2	(, 12, 12, 192)	6144	block_3_proj_BN[0][0]
block_4_exp_BN C3	(, 12, 12, 192)	768	block_4_exp[0][0]
block_4_exp_relu C4	(, 12, 12, 192)	0	block_4_exp_BN[0][0]

block_4_dw C6	(, 12, 12, 192)	1728	block_4_exp_relu[0][0]
block_4_dw_BN C3	(, 12, 12, 192)	768	block_4_dw[0][0]
block_4_dw_relu C4	(, 12, 12, 192)	0	block_4_dw_BN[0][0]
block_4_proj C2	(, 12, 12, 32)	6144	block_4_dw_relu[0][0]
block_4_proj_BN C3	(, 12, 12, 32)	128	block_4_proj[0][0]
block_4_add (Add)	(, 12, 12, 32)	0	block_3_proj_BN[0][0] block_4_proj_BN[0][0]
block_5_exp C2	(, 12, 12, 192)	6144	block_4_add[0][0]
block_5_exp_BN C3	(, 12, 12, 192)	768	block_5_exp[0][0]
block_5_exp_relu C4	(, 12, 12, 192)	0	block_5_exp_BN[0][0]
block_5_dw C6	(, 12, 12, 192)	1728	block_5_exp_relu[0][0]
block_5_dw_BN C3	(, 12, 12, 192)	768	block_5_dw[0][0]
block_5_dw_relu C4	(, 12, 12, 192)	0	block_5_dw_BN[0][0]
block_5_proj C2	(, 12, 12, 32)	6144	block_5_dw_relu[0][0]
block_5_proj_BN C3	(, 12, 12, 32)	128	block_5_proj[0][0]
block_5_add (Add)	(, 12, 12, 32)	0	block_4_add[0][0] block_5_proj_BN[0][0]
block_6_exp C2	(, 12, 12, 192)	6144	block_5_add[0][0]
block_6_exp_BN C3	(, 12, 12, 192)	768	block_6_exp[0][0]
block_6_exp_relu C4	(, 12, 12, 192)	0	block_6_exp_BN[0][0]
block_6_pad C1	(, 13, 13, 192)	0	block_6_exp_relu[0][0]
block_6_dw C6	(, 6, 6, 192)	1728	block_6_pad[0][0]
block_6_dw_BN C3	(, 6, 6, 192)	768	block_6_dw[0][0]
block_6_dw_relu C4	(, 6, 6, 192)	0	block_6_dw_BN[0][0]
block_6_proj C2	(, 6, 6, 64)	12288	block_6_dw_relu[0][0]
block_6_proj_BN C3	(, 6, 6, 64)	256	block_6_proj[0][0]
block_7_exp C2	(, 6, 6, 384)	24576	block_6_proj_BN[0][0]
block_7_exp_BN C3	(, 6, 6, 384)	1536	block_7_exp[0][0]
block_7_exp_relu C4	(, 6, 6, 384)	0	block_7_exp_BN[0][0]
block_7_dw C6	(, 6, 6, 384)	3456	block_7_exp_relu[0][0]
block_7_dw_BN C3	(, 6, 6, 384)	1536	block_7_dw[0][0]
block_7_dw_relu C4	(, 6, 6, 384)	0	block_7_dw_BN[0][0]
block_7_proj C2	(, 6, 6, 64)	24576	block_7_dw_relu[0][0]
block_7_proj_BN C3	(, 6, 6, 64)	256	block_7_proj[0][0]
block_7_add (Add)	(, 6, 6, 64)	0	block_6_proj_BN[0][0] block_7_proj_BN[0][0]
block_8_exp C2	(, 6, 6, 384)	24576	block_7_add[0][0]
block_8_exp_BN C3	(, 6, 6, 384)	1536	block_8_exp[0][0]
block_8_exp_relu C4	(, 6, 6, 384)	0	block_8_exp_BN[0][0]
block_8_dw C6	(, 6, 6, 384)	3456	block_8_exp_relu[0][0]
block_8_dw_BN C3	(, 6, 6, 384)	1536	block_8_dw[0][0]

block_8_dw_relu C4	(, 6, 6, 384)	0	block_8_dw_BN[0][0]
block_8_proj C2	(, 6, 6, 64)	24576	block_8_dw_relu[0][0]
block_8_proj_BN C3	(, 6, 6, 64)	256	block_8_proj[0][0]
block_8_add (Add)	(, 6, 6, 64)	0	block_7_add[0][0] block_8_proj_BN[0][0]
block_9_exp C2	(, 6, 6, 384)	24576	block_8_add[0][0]
block_9_exp_BN C3	(, 6, 6, 384)	1536	block_9_exp[0][0]
block_9_exp_relu C4	(, 6, 6, 384)	0	block_9_exp_BN[0][0]
block_9_dw C6	(, 6, 6, 384)	3456	block_9_exp_relu[0][0]
block_9_dw_BN C3	(, 6, 6, 384)	1536	block_9_dw[0][0]
block_9_dw_relu C4	(, 6, 6, 384)	0	block_9_dw_BN[0][0]
block_9_proj C2	(, 6, 6, 64)	24576	block_9_dw_relu[0][0]
block_9_proj_BN C3	(, 6, 6, 64)	256	block_9_proj[0][0]
block_9_add (Add)	(, 6, 6, 64)	0	block_8_add[0][0] block_9_proj_BN[0][0]
block_10_exp C2	(, 6, 6, 384)	24576	block_9_add[0][0]
block_10_exp_BN C3	(, 6, 6, 384)	1536	block_10_exp[0][0]
block_10_exp_relu C4	(, 6, 6, 384)	0	block_10_exp_BN[0][0]
block_10_dw C5	(, 6, 6, 384)	3456	block_10_exp_relu[0][0]
block_10_dw_BN C3	(, 6, 6, 384)	1536	block_10_dw[0][0]
block_10_dw_relu C4	(, 6, 6, 384)	0	block_10_dw_BN[0][0]
block_10_proj C2	(, 6, 6, 96)	36864	block_10_dw_relu[0][0]
block_10_proj_BN C3	(, 6, 6, 96)	384	block_10_proj[0][0]
block_11_exp C2	(, 6, 6, 576)	55296	block_10_proj_BN[0][0]
block_11_exp_BN C3	(, 6, 6, 576)	2304	block_11_exp[0][0]
block_11_exp_relu C4	(, 6, 6, 576)	0	block_11_exp_BN[0][0]
block_11_dw C5	(, 6, 6, 576)	5184	block_11_exp_relu[0][0]
block_11_dw_BN C3	(, 6, 6, 576)	2304	block_11_dw[0][0]
block_11_dw_relu C4	(, 6, 6, 576)	0	block_11_dw_BN[0][0]
block_11_proj C2	(, 6, 6, 96)	55296	block_11_dw_relu[0][0]
block_11_proj_BN C3	(, 6, 6, 96)	384	block_11_proj[0][0]
block_11_add (Add)	(, 6, 6, 96)	0	block_10_proj_BN[0][0] block_11_proj_BN[0][0]
block_12_exp C2	(, 6, 6, 576)	55296	block_11_add[0][0]
block_12_exp_BN C3	(, 6, 6, 576)	2304	block_12_exp[0][0]
block_12_exp_relu C4	(, 6, 6, 576)	0	block_12_exp_BN[0][0]
block_12_dw C5	(, 6, 6, 576)	5184	block_12_exp_relu[0][0]
block_12_dw_BN C3	(, 6, 6, 576)	2304	block_12_dw[0][0]
block_12_dw_relu C4	(, 6, 6, 576)	0	block_12_dw_BN[0][0]
block_12_proj C2	(, 6, 6, 96)	55296	block_12_dw_relu[0][0]
block_12_proj_BN C3	(, 6, 6, 96)	384	block_12_proj[0][0]

block_12_add (Add)	(, 6, 6, 96)	0	block_11_add[0][0] block_12_proj_BN[0][0]
block_13_exp C2	(, 6, 6, 576)	55296	block_12_add[0][0]
block_13_exp_BN C3	(, 6, 6, 576)	2304	block_13_exp[0][0]
block_13_exp_relu C4	(, 6, 6, 576)	0	block_13_exp_BN[0][0]
block_13_pad C1	(, 7, 7, 576)	0	block_13_exp_relu[0][0]
block_13_dw C5	(, 3, 3, 576)	5184	block_13_pad[0][0]
block_13_dw_BN C3	(, 3, 3, 576)	2304	block_13_dw[0][0]
block_13_dw_relu C4	(, 3, 3, 576)	0	block_13_dw_BN[0][0]
block_13_proj C2	(, 3, 3, 160)	92160	block_13_dw_relu[0][0]
block_13_proj_BN C3	(, 3, 3, 160)	640	block_13_proj[0][0]
block_14_exp C2	(, 3, 3, 960)	153600	block_13_proj_BN[0][0]
block_14_exp_BN C3	(, 3, 3, 960)	3840	block_14_exp[0][0]
block_14_exp_relu C4	(, 3, 3, 960)	0	block_14_exp_BN[0][0]
block_14_dw C5	(, 3, 3, 960)	8640	block_14_exp_relu[0][0]
block_14_dw_BN C3	(, 3, 3, 960)	3840	block_14_dw[0][0]
block_14_dw_relu C4	(, 3, 3, 960)	0	block_14_dw_BN[0][0]
block_14_proj C2	(, 3, 3, 160)	153600	block_14_dw_relu[0][0]
block_14_proj_BN C3	(, 3, 3, 160)	640	block_14_proj[0][0]
block_14_add (Add)	(, 3, 3, 160)	0	block_13_proj_BN[0][0] block_14_proj_BN[0][0]
block_15_exp C2	(, 3, 3, 960)	153600	block_14_add[0][0]
block_15_exp_BN C3	(, 3, 3, 960)	3840	block_15_exp[0][0]
block_15_exp_relu C4	(, 3, 3, 960)	0	block_15_exp_BN[0][0]
block_15_dw C5	(, 3, 3, 960)	8640	block_15_exp_relu[0][0]
block_15_dw_BN C3	(, 3, 3, 960)	3840	block_15_dw[0][0]
block_15_dw_relu C4	(, 3, 3, 960)	0	block_15_dw_BN[0][0]
block_15_proj C2	(, 3, 3, 160)	153600	block_15_dw_relu[0][0]
block_15_proj_BN C3	(, 3, 3, 160)	640	block_15_proj[0][0]
block_15_add (Add)	(, 3, 3, 160)	0	block_14_add[0][0] block_15_proj_BN[0][0]
block_16_exp C2	(, 3, 3, 960)	153600	block_15_add[0][0]
block_16_exp_BN C3	(, 3, 3, 960)	3840	block_16_exp[0][0]
block_16_exp_relu C4	(, 3, 3, 960)	0	block_16_exp_BN[0][0]
block_16_dw C5	(, 3, 3, 960)	8640	block_16_exp_relu[0][0]
block_16_dw_BN C3	(, 3, 3, 960)	3840	block_16_dw[0][0]
block_16_dw_relu C4	(, 3, 3, 960)	0	block_16_dw_BN[0][0]
block_16_proj C2	(, 3, 3, 320)	307200	block_16_dw_relu[0][0]
block_16_proj_BN C3	(, 3, 3, 320)	1280	block_16_proj[0][0]
Conv_1 C2	(, 3, 3, 1280)	409600	block_16_proj_BN[0][0]
Conv_1_bn C3zation)	(, 3, 3, 1280)	5120	Conv_1[0][0]
out_relu C4	(, 3, 3, 1280)	0	Conv_1_bn[0][0]
global_average	(, 1280)	0	out_relu[0][0]
dense_1 (Dense)	(, 1024)	1311744	global_average[0][0]
dense_2 (Dense)	(, 35)	35875	dense_1[0][0]