

Application Note No. 060

A High Third-Order Intercept Low Noise Amplifier
for 1900 MHz Application Using the Silicon-
Germanium BFP620 Transistor

RF & Protection Devices



Never stop thinking

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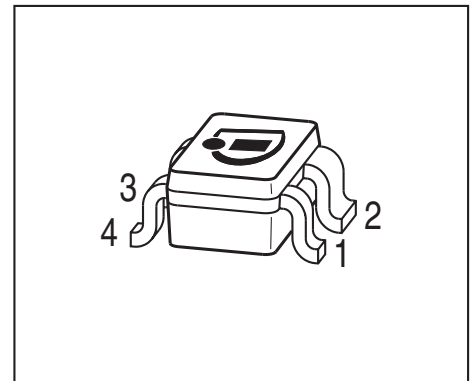
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A High Third-Order Intercept Low Noise Amplifier for 1900 MHz Application

1 A High Third-Order Intercept Low Noise Amplifier for 1900 MHz Application Using the Silicon-Germanium BFP 620 Transistor

- Gain = 14.7 dB
- Very Low Noise Figure = 1.05 dB
- High Input 3rd-Order Intercept Point = +10 dBm
- Low Power Consumption, 8.9 mA at 3.0 V
- Single Supply Voltage (no negative bias required), low parts count
- Applications: Cellular Handsets for CDMA, WCDMA, UMTS



1 = B, 2 = E, 3 = C, 4 = E

1.1 Description

Infineon's BFP620 is a high-performance, low-cost Silicon-Germanium bipolar transistor fabricated with Infineon's B7HF SiGe process. Housed in a 4-lead ultra-miniature SOT343 surface mount package and with a 70 GHz transition frequency (f_T), this device is ideal for high performance applications including Low Noise Amplifiers in portable telephones and other battery operated wireless communications devices. The BFP620 offers exceptionally low noise figure, high gain and high linearity at low power consumption levels. The BFP620 rivals more expensive GaAs MESFET and PHEMT devices in performance without requiring a negative supply voltage. This application note describes a low noise figure, high 3rd-order intercept 1900 MHz LNA targeted for CDMA applications and also provides guidelines for improving 3rd-order intercept performance in amplifiers using Infineon Transistors.

1.2 Overview of 1900 MHz High-Linearity LNA

The schematic diagram for the 1930 - 1990 MHz low noise amplifier (LNA) is shown in [Figure 1](#). The amplifier is intended for use in low-cost battery powered applications such as those found in PCS band or TriMode CDMA cellular handsets. Design goals include a gain of 15 dB, unconditional stability, a noise figure under 1.1 dB, an Input 3rd-Order Intercept Point (IIP_3) of +10 dBm, reduced parts count and low PCB area requirement. Input and output return loss values of better than 10 dB were sought in order to do easy integration with a duplexer and image-stripping filter. The Bill Of Material and a PC Board cross-section diagram are shown in [Table 2](#) and a more detailed description of the LNA follows in [Chapter 2](#). Measurement results are summarized in [Table 1](#). These are mean values taken from a sample lot of 10 application boards (please refer to Appendix C). The insertion losses of the connectors and microstrip lines are not backed out for these results - if the (input) transmission line and connector losses were subtracted, the noise figure results would be ≈ 0.2 dB lower.

A High Third-Order Intercept Low Noise Amplifier for 1900 MHz Application

Table 1 Typical Performance for BFP620 V4.3 Application at 1960 MHz, $T = 25\text{ }^{\circ}\text{C}$, $V = 3.0\text{ V}$

Parameter	Symbol	Value
Gain	$\text{dB}[s_{21}]^2$	14.7 dB
Noise Figure	NF	1.04 dB
Input 3 rd Order Intercept	IIP_3	+10.3 dBm
Output 3 rd Order Intercept	OIP_3	+25.0 dBm
Output 1dB compression	$OP_{1\text{dB}}$	+5.8 dBm
Input Return Loss	$\text{dB}[s_{11}]^2$	13.3 dB
Output Return Loss	$\text{dB}[s_{22}]^2$	14.6 dB
Collector-Emitter Voltage	V_{CE}	2.1 V
Supply Current	I	8.9 mA
LNA PC Board Area		$\approx 45\text{ mm}^2$
Number of external SMT Components ¹⁾		12

1) Includes bias resistors and DC blocks

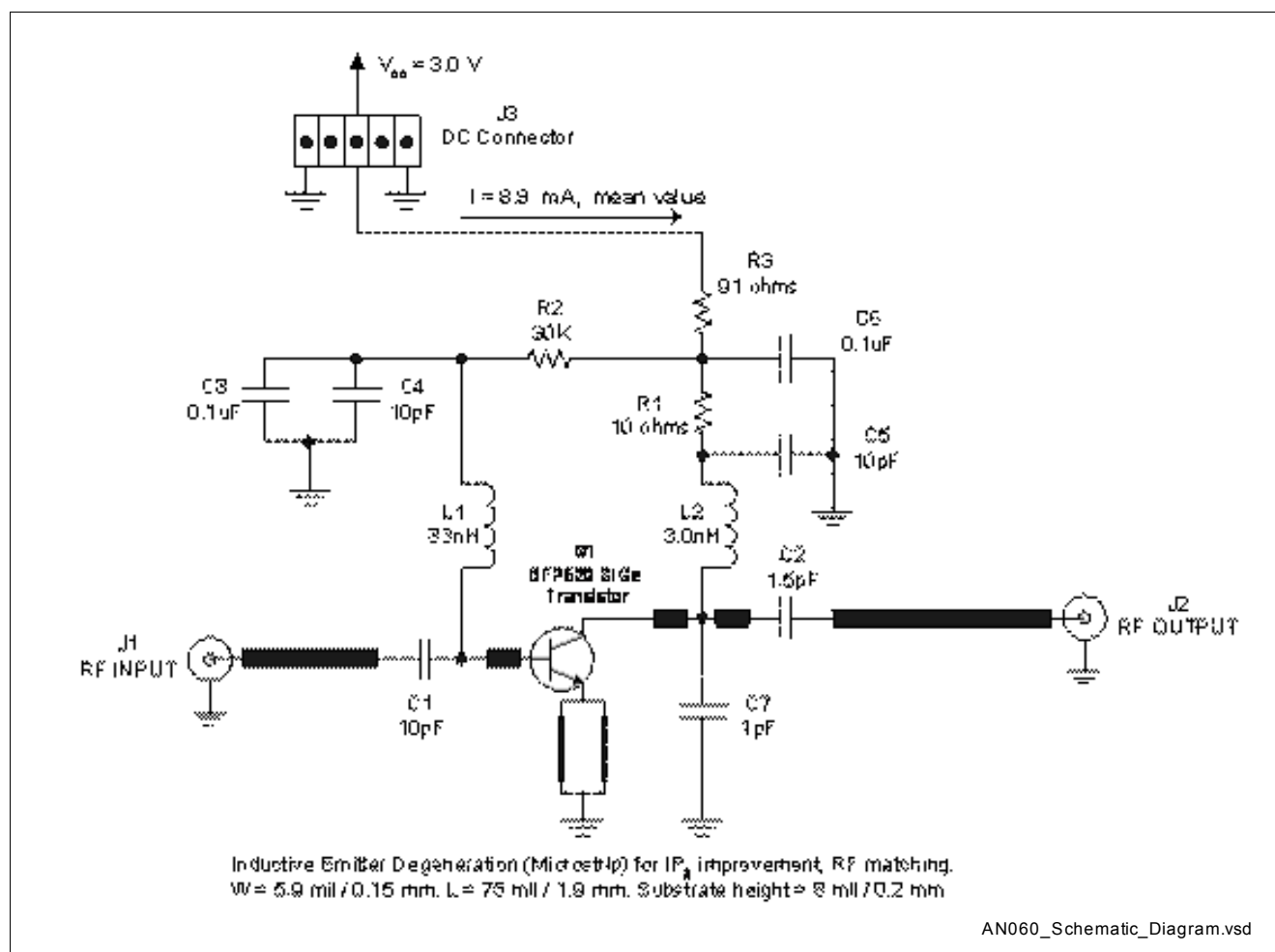
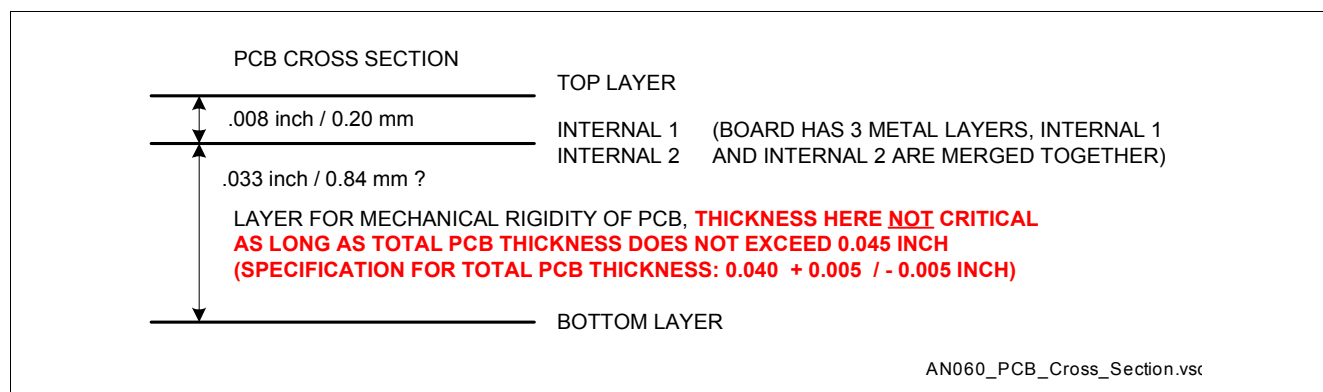


Figure 1 Schematic Diagram for PCS LNA, Printed Circuit Board Version 4.3

A High Third-Order Intercept Low Noise Amplifier for 1900 MHz Application

Table 2 Bill Of Material

Reference Designator	Value	Manufacturer / Type	Case Size	Function
C1	10 pF	Various	0402	Input DC block
C2	1.5 pF	Various	0402	Output DC block, output RF matching
C3	0.1 μ F	Various	0603	Low frequency ground at base (Input 3 rd Order Intercept improvement)
C4	10 pF	Various	0402	RF bypass / RF block
C5	10 pF	Various	0402	RF bypass / RF block
C6	0.1 μ F	Various	0603	Bypass / block
C7	0.5 pF	Various	0402	High freq. stability / kill gain > 8 GHz
L1	15 nH	Murata LQG10A (Low cost inductor)	0402	RF choke to DC bias on base
L2	3.3 nH	Murata LQG10A (Low cost inductor)	0402	Output RF match, DC feed to collector
R1	10 Ω	Various	0402	Stability (below 2 GHz)
R2	30 k Ω	Various	0402	DC bias for base
R3	91 Ω	Various	0402	DC bias / drop voltage for collector
Q1		Infineon Technologies	SOT343	BFP620 Silicon-Germanium transistor
J1		Johnson 142-0701-841		RF input connector
J2		Johnson 142-0701-841		RF output connector
J3		AMP 5 pin header, MTA-100 series 640456-5 (Standard pin plating) Or 641215-5 (gold plated pins)		DC connector Pins 1, 5 = grounded Pin 3 = V_{CC} Pins 2, 4 = no connection


Figure 2 PC Board Cross Section. Board material is standard FR4. Note spacing from top layer RF traces to internal ground plane is 0.008 inch / 0.20 mm

2 Low Noise Amplifier Design Considerations

In subsequent sections the various design considerations and trade-offs for this particular LNA will be described, including:

1. Linearity
2. Stability
3. Noise Figure
4. Input / Output Match
5. DC Bias

2.1 Linearity

The primary design goal for this Low Noise Amplifier (LNA) was to achieve an input 3rd-order intercept point of +10 dB, while consuming less than 10 mA of DC current. To this end, two techniques were employed: a) inductive emitter degeneration and b) use of additional charge storage across the base-emitter junction of the transistor.

2.1.1 Some Definitions

The usual method employed for measuring 3rd order intercept point (IP_3) involves injecting two equal amplitude sinusoidal signals at frequencies f_1 and f_2 into the amplifier input, and observing the relative levels of the test signals f_1 , f_2 and third-order products $2f_2 - f_1$ and $2f_1 - f_2$ at the amplifier output. The third-order products, as well as all other signals present at the amplifier output besides f_1 and f_2 constitute distortion and are the results of nonlinear behaviour within the transistor, most notably across the base-emitter junction. For the testing done on this particular LNA, each input test tone power level (P_{in} , input power for both f_1 and f_2) is set to -20 dBm, and the spacing between the tones is nominally 1 MHz. The input 3rd-order intercept point (IIP_3) is calculated as follows:

(1)

$$IIP3 = PIN + \frac{\Delta IM3}{2}$$

Where ΔIM_3 = the difference in amplitude between one of the two equal amplitude test tones present at the amplifier output, and the level of the highest 3rd-order distortion product. Please refer to [Figure 3](#).

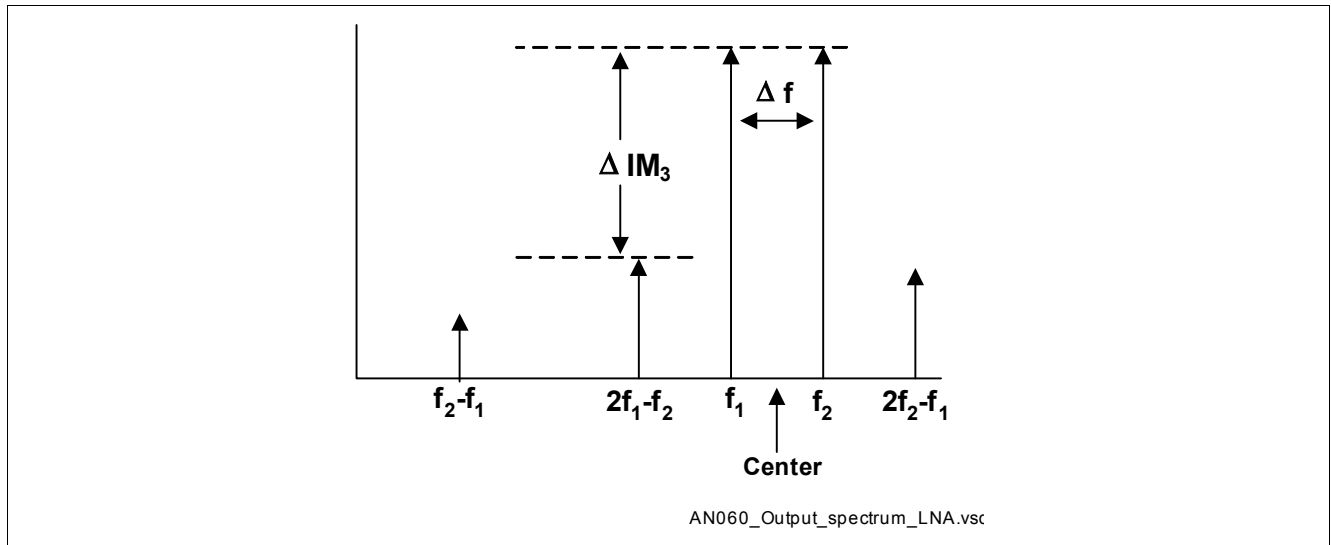


Figure 3 Partial presentation of output spectrum of the LNA; f_1 and f_2 are equal - amplitude input test tones. For this LNA, -20 dBm powered tone is used. Other signals besides f_1 and f_2 are generated as a result of non-linear device behavior

2.1.1.1 Inductive Emitter Degeneration

The process of intentionally inserting additional inductance between device emitter connections and RF ground is a commonly employed method used for influencing device input / output match, noise match, stability and linearity. Inductive degeneration does not seriously impact noise figure performance, as resistive degeneration does. In this design, two microstrip lines, each with dimensions of 0.15 mm x 1.9 mm, serve as inductors between each device emitter lead and PCB ground plane. This additional inductance provides “series-series” negative feedback, improving amplifier 3rd-order intercept and gain compression points, at the cost of reduced gain. For this LNA approximately 1.5 to 2 dB of gain is traded to attain improved linearity. In other words typical gain in a similar applications board with direct emitter grounding was 16 to 16.5 dB, and this gain was reduced to 14.7 dB by the use of inductive emitter degeneration.

2.1.1.2 Effect of Adding Additional Charge-Storage Across the Base-Emitter Junction

One of the spectral lines generated by device nonlinearity during a two-tone test is a low frequency product, (f_1-f_2) . For the case of a test tone spacing of 1 MHz, this 1 MHz product modulates the base-emitter and collector-emitter voltages of the LNA at a 1 MHz rate. Recalling that for a bipolar transistor, emitter current is an exponential function of the base-emitter voltage,

(2)

$$I_e \approx I_{es} \cdot e^{\left(\frac{qV_{BE}}{kT}\right)}$$

One can imagine this low frequency AC signal present at the device terminals varying the operating point of the transistor at the rate (f_2-f_1) , thus adversely impacting distortion product levels.

If a relatively large value capacitor is placed across the base-emitter junction in order to bypass this low frequency product (f_2-f_1) , the voltage fluctuation seen by the base-emitter junction of the transistor can be reduced, and the levels of the 3rd order products minimized. Please refer to the schematic diagram in [Figure 1](#). Capacitor C3, 0.1 μF, performs the low-frequency bypass function described here. An improvement in third-order intercept point

Low Noise Amplifier Design Considerations

of approximately 5 to 10 dB can be expected by using this “trick”. The same effect may be seen by using extra charge storage on the collector, but the results usually are not nearly as dramatic.

The closer together the two input test tones f_1 and f_2 are in frequency, the lower frequency the product or beat note ($f_2 - f_1$) is. Therefore as input test tones f_1 and f_2 come closer together, more capacitance is needed to achieve best possible bypassing of the low frequency product ($f_2 - f_1$). For a test tone separation of 1 MHz, 0.1 μ F was found to be more than adequate in this particular application circuit. A good physical or gut-level feeling for the efficacy of this trick can be had by testing the LNA with and without C3 in place, and by experimenting with different test tone spacing and capacitor values for C3.

For best results, the transistor should see a nice, low-impedance path at low frequencies between this additional charge storage and its terminals; for this reason a coil rather than a high-value resistor is used to bring in the base bias voltage and isolate the RF from the DC bias network. The 15 nH inductor used on the base to bring in the DC bias has negligible impedance up to tens of megahertz, but provides enough impedance at 1.9 GHz to nearly isolate the base of the transistor from the bias network within the LNA’s normal operating frequency range. For applications requiring operation over wide temperature ranges, the effect of temperature on capacitor dielectric and capacitor performance should be investigated.

It is important to note that bypassing the ($f_2 - f_1$) product as described here does not affect the compression level of the amplifier - only the third-order intercept point. As a result, if this bypassing technique is used, the general rule of thumb stating that there is approximately a 10 dB difference between third-order intercept and 1 dB compression points is not longer valid. In this application, the Input IP_3 is +10 dBm, and the Input P_{1dB} is typically -7.9 dBm, with a difference of 17.9 dB between these two points. A typical gain compression curve is shown in Figure 4.

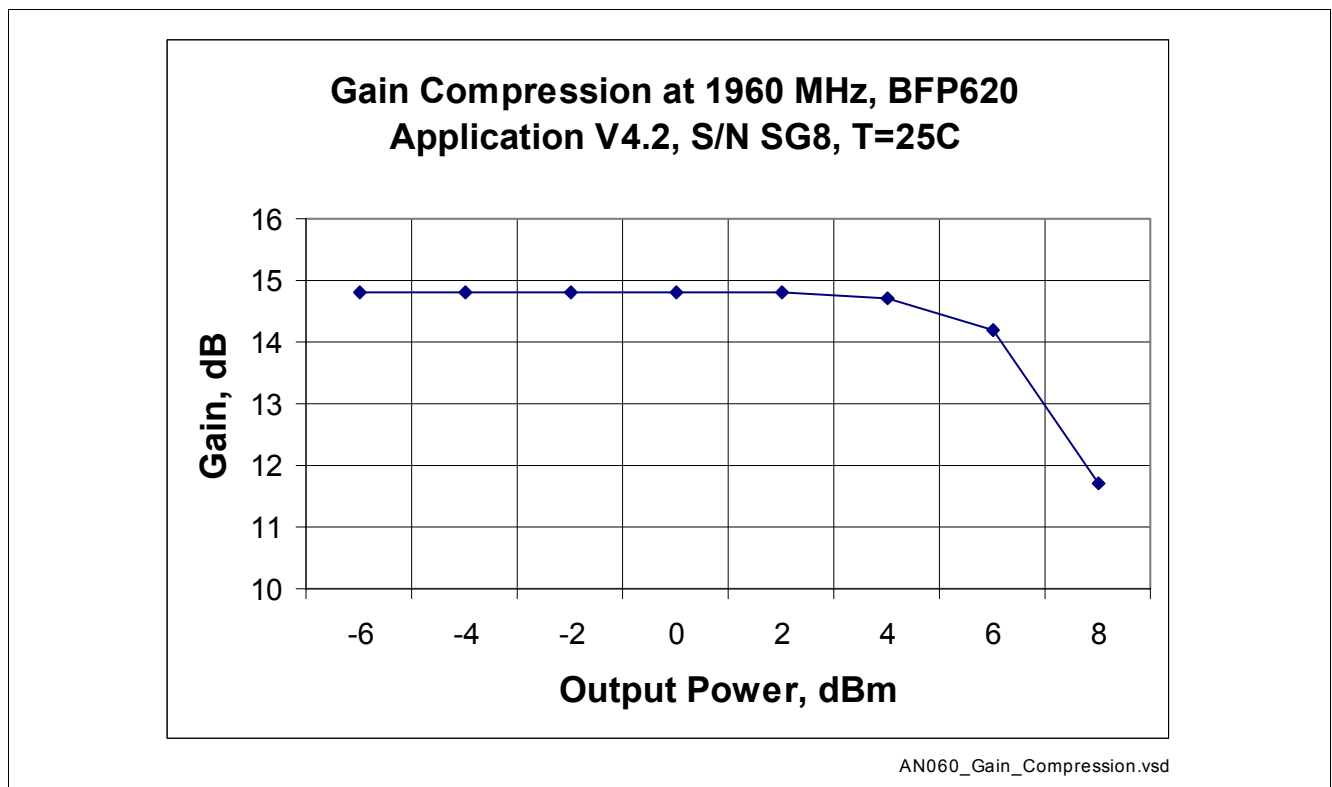


Figure 4 Typical Gain Compression Curve at 1960 MHz, $T = 25\text{ }^{\circ}\text{C}$, $V = 3.0\text{ V}$ for BFP620 Application Version 4.2., S/N SG8

2.1.1.3 Test Tone Spacing vs. IIP_3

The reader may wonder what happens to third-order product distortion levels at the two input test tone are “walked apart” in frequency. A BFP620 V4.2 Applications Board was tested for Input IP_3 over range of test tone spacing, from 20 kHz to 100 MHz. In each case the “center frequency” $(f_1+f_2) / 2$ was 1960 MHz. Results are tabulated in [Table 3](#) and plotted in [Figure 5](#).

As previously mentioned, one limiting factor at close tone spacing is the available charge storage (e.g. value of C3), or “how good of a low frequency ground” one has across the base-emitter junction (and also, to a lesser degree, at the collector). At wider tone spacing, the product (f_2-f_1) rises in frequency, and the impedance of the RF chokes which isolate the DC bias circuit from the transistor begin to play a role - and this undesired impedance begins to roll off or degrade IP_3 performance. Of course the selectivity of the matching circuits at LNA input and output also have some influence, particularly as the test tones are separated more and more widely and begin to fall out of the normal operating frequency range of the amplifier.

Table 3 Input 3rd Order Intercept versus Test Tone Spacing¹⁾

f_1 , MHz	f_2 , MHz	Δf	IIP_3 , dBm
1959.990	1960.010	20 kHz	+7.1
1959.975	1960.025	50 kHz	+8.1
1959.950	1960.050	100 kHz	+9.4
1959.900	1960.100	200 kHz	+9.6
1959.750	1960.250	500 kHz	+10.1
1959.500	1960.500	1 MHz	+10.1
1959.000	1961.000	2 MHz	+10.1
1957.500	1962.500	5 MHz	+10.0
1955.000	1965.000	10 MHz	+10.0
1950.000	1970.000	20 MHz	+9.8
1935.000	1985.000	50 MHz	+9.1
1910.000	2010.000	100 MHz	+9.0

1) For BFP620 V4.2 Application board, the “center” frequency - e.g. $(f_1+f_2)/2$ - is kept at 1960 MHz. Input power of each test tone, f_1 and f_2 , is -20 dBm each tone.

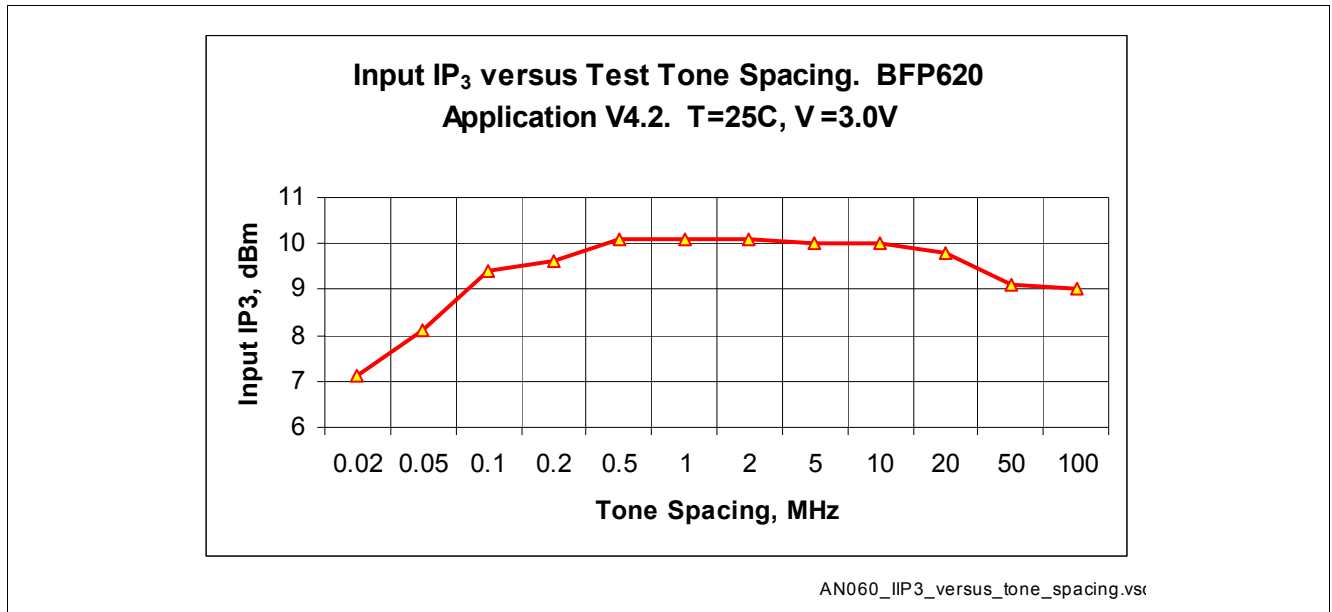


Figure 5 Input IP_3 versus test tone spacing, BFP620 Application V4.2. $V = 3\text{ V}$, Center Frequency = 1960 MHz, $T = 25\text{ }^{\circ}\text{C}$

2.1.1.4 Linearity - To Sum Up

For this LNA application, two methods are used to improve third-order intercept performance: 1) inductive emitter degeneration and 2) low-frequency bypassing of the $(f_2 - f_1)$ product at the base-emitter (and collector) junction.

Inductive emitter degeneration achieves linearity improvement at the cost of reduced gain. Other methods may be employed to achieve further reduction of third-order distortion levels, but these two simple methods are less likely to be influenced by temperature and LNA termination impedance than some of the more exotic techniques reported in the literature [1]. Additional information on linearity topics can be found in Infineon Application Note AN057 [4].

2.1.2 Stability Considerations

In general, for a linear two-port device characterized by S-parameters, the two necessary and sufficient conditions to guarantee unconditional stability (e.g. no possibility of oscillation when input and output of the device are both terminated in any passive real impedance) are

A) $K > 1$ and b) $|\Delta| < 1$ where

(3)

$$K = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12} \cdot s_{21}|}$$

(4)

$$|\Delta| = |s_{11} \cdot s_{22} - s_{12} \cdot s_{21}|$$

Low Noise Amplifier Design Considerations

In the literature one may encounter an alternative form for these two conditions as

a) $K > 1$ and b) $B_1 > 0$ where

(5)

$$B_1 = 1 + |s_{11}|^2 - |s_{22}|^2 - |\Delta|^2$$

A simulation tool is of great help when trying to optimize an amplifier for stability. The Ansoft Serenade® design environment was used for simulations in this LNA design, including evaluating the stability factors K and B_1 up to 6 GHz.

2.1.2.1 Stability Below 6 GHz

At the time of this writing s-parameter were available for the BFP620 from 10 MHz to 6 GHz. Initial simulations looked at stability factors K and B_1 . The use of inductive emitter degeneration for the purposes of linearity improvement also had a major impact on the stability of the amplifier. In brief: a small amount of emitter degeneration improves stability at lower frequencies, but as the amount of emitter inductance is increased, stability at higher frequencies, e.g. in the range of 5 to 12 GHz - is compromised. In simulations, and later confirmed with measurements, output resistive loading (see schematic, R_1 , 10 Ω) in conjunction with the additional emitter inductance helped to bring K to a value greater than 1, particularly in the range of 800 - 1200 MHz. The RF bypass capacitor C_5 , 10 pF, has less of an effect at lower frequencies as compared to at 2 GHz, hence the LNA output "sees" this lossy 10 Ω resistor below band, improving stability in that region. Having some stability margin in this range is especially important given that PCS band duplexers typically look very reflective in the 800 -1200 MHz range.

2.1.2.2 Stability above 6 GHz

As stated previously, a small amount of additional emitter inductance can help stabilize the BFP620 at lower frequencies, but larger amounts of added emitter inductance can jeopardize stability at higher frequencies - for this particular amplifier, in the region above about 8 GHz. As the BFP620 is a very high gain device with an extremely high transition frequency, the potential for high frequency instability exists, thus great care must be exercised.

A large amount of inductive emitter degeneration was required in order to meet the linearity requirement target - an input IP_3 of +10 dBm with less than 10 mA of current. Due to this large amount of required emitter inductance, it was found that the LNA could oscillate at 10 GHz if both LNA input and output were left open-circuited. The 10 GHz oscillation could be observed on a spectrum analyzer if the area near the LNA were "sniffed" with an RF probe while amplifier input and output were left open-circuited. (Even a cable with a PC Board mount SMA connector inserted into one end may be used as a makeshift RF probe, with the center pin of the SMA connector used as an "antenna". Be sure to DC block the spectrum analyzer input!)

Another observable symptom of the 10 GHz oscillation was a shift in DC operating current - as the input and output of the LNA were taken from being terminated in 50 Ω to being open circuited, the DC current would increase by 0.5 to 1.5 mA.

In a real application (e.g. with a duplexer LNA input and a ceramic image-stripping filter at LNA output) the LNA would not see a perfect open circuit at all frequencies, and a problem might not exist. Nevertheless, this situation with marginal stability with input and output open-circuited is undesirable. As s-parameters were only available to a 6 GHz, a careful analysis of K and B_1 was not possible at 10 GHz. A more empirical approach was taken to eliminate the potential 10 GHz oscillation.

Low Noise Amplifier Design Considerations

If it were possible to kill the gain of the LNA above 8 GHz or so, while leaving PCS band gain largely unaffected, it might be possible to eliminate the potential 10 GHz instability. To this end, a simple, crude, but effective fix was employed.

Please refer to the schematic diagram [Figure 1](#). Note the 0.5 pF capacitor C7. An approximate lumped-element model for this capacitor is shown in [Figure 6](#), including the short microstrip track leading to the capacitor's self-inductance and equivalent series resistance (ESR). (In general, for best simulation accuracy it is a good idea to try and model parasitic reactance in circuit elements, e.g. modeling the parasitic capacitance / self-resonant frequency of chip coils, or parasitic inductance and equivalent series resistance ("ESR") of chip capacitors.)

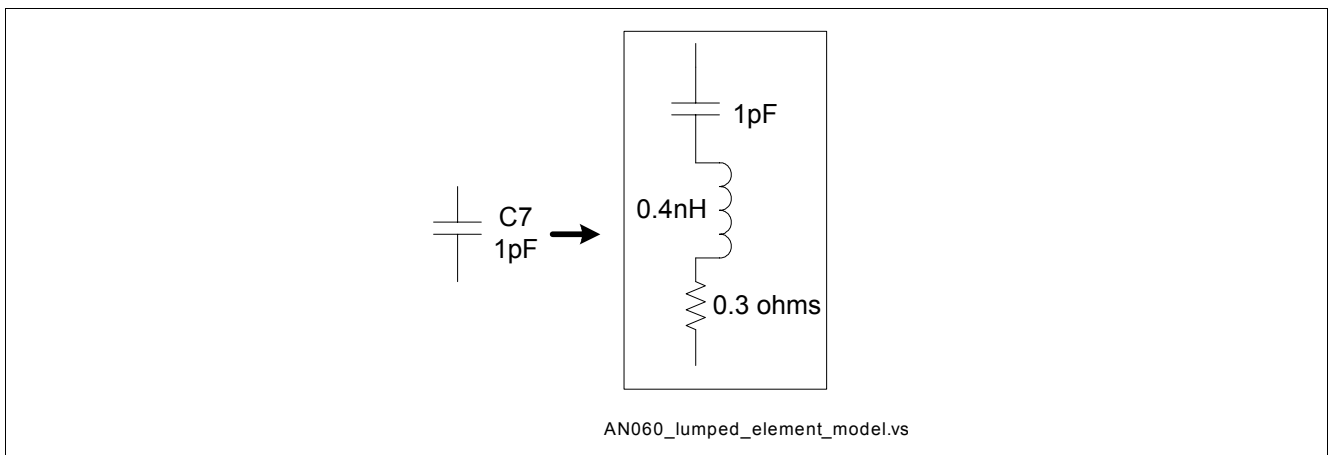


Figure 6 Approximate lumped-element model for Capacitor C7 in 0402 package. (PCB track, chip self-inductance and Equivalent Series Resistance are accounted for)

The 0.5 pF 0402-size chip capacitor C7 has its in-circuit self-resonance at approximately 9 GHz, given by

(6)

$$f_{res} = \frac{1}{2\pi\sqrt{LC}}$$

Being a series resonance, C7 tends toward a short-circuit condition near 9 GHz. The main idea: LNA gain in the vicinity of 8 to 11 GHz is reduced by "shorting-out" the LNA output in this frequency range with C7, hence killing the potential oscillation. The effect on gain in the 1900 MHz PCS band was minimal, with a loss in gain of around 0.2 dB. Despite s-parameters being available only to 6 GHz, the simulation plot in [Figure 7](#) gives a good qualitative idea of how this element affects the amplifier with respect to gain above 5 or 6 GHz (the simulator extrapolates s-parameters above 6 GHz.) In each case for the simulation, with C7 and without C7, the output is re-matched for optimum amplifier gain and return loss. Note the reduction in gain above about 6 GHz when C7 is added to the LNA output. This above-band gain reduction helped kill the potential 10 GHz oscillation.

Simulated and measured plots of the stability factors K and B_1 for up to 6 GHz appear in [Figure 8](#) and [Figure 9](#) for a BFP620 Version 4.3 PC board. For [Figure 9](#) measured s-parameter data taken from an actual BFP620 board is imported into the circuit simulator, which then calculates and plots K and B_1 .

Low Noise Amplifier Design Considerations

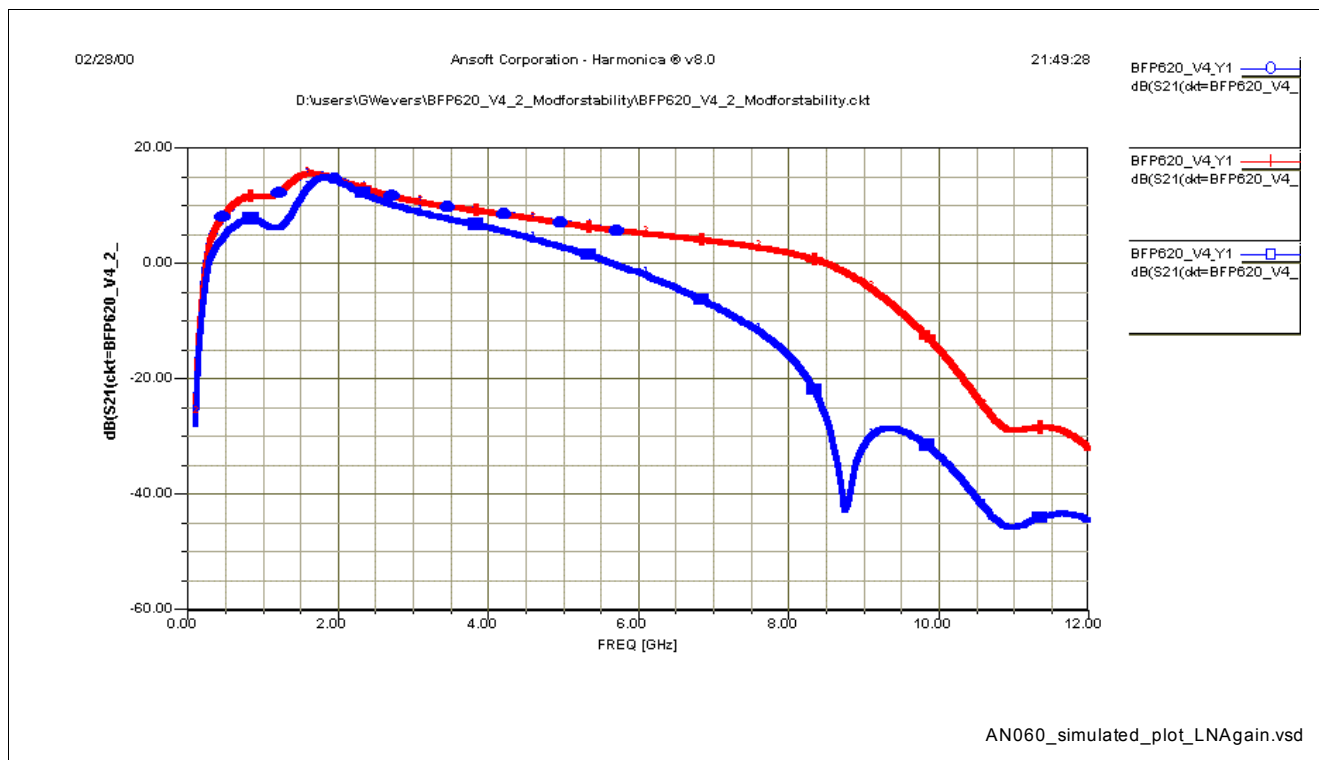


Figure 7 Simulated plot of LNA gain showing effect of capacitor C7 on high frequency gain of LNA. Note “suckout” or reduction in gain for 6 to 11 GHz region with C7 in the circuit. Gain reduction in this range helped to kill potential 10 GHz oscillation caused by large amount of emitter degeneration. (Sweep for this plot is from 100 MHz to 12 GHz.)

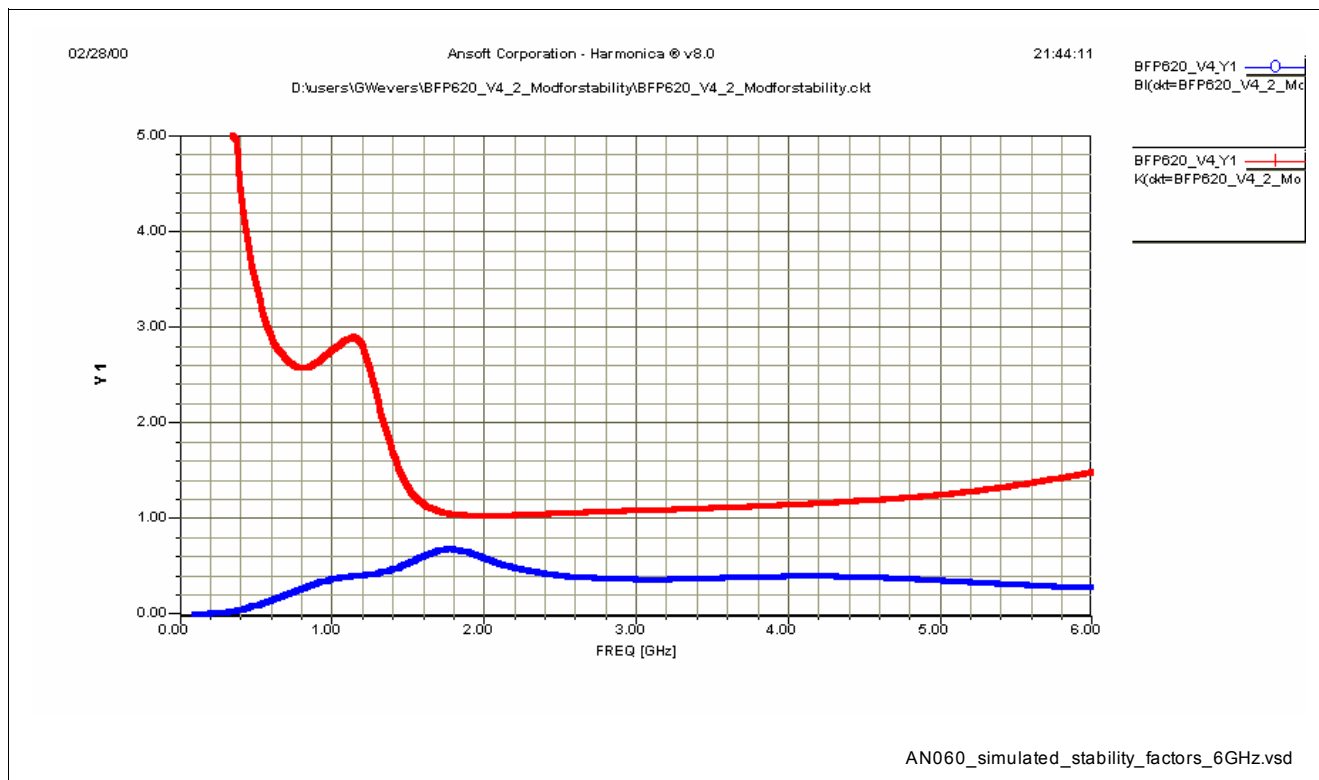


Figure 8 Simulation plot of stability factors K and B₁ up to 6 GHz. (Sweep is 100 MHz to 6 GHz). Note

$K > 1$ and $B_1 > 0$ for entire region. Minimum K value is 1.04 at 1850 MHz

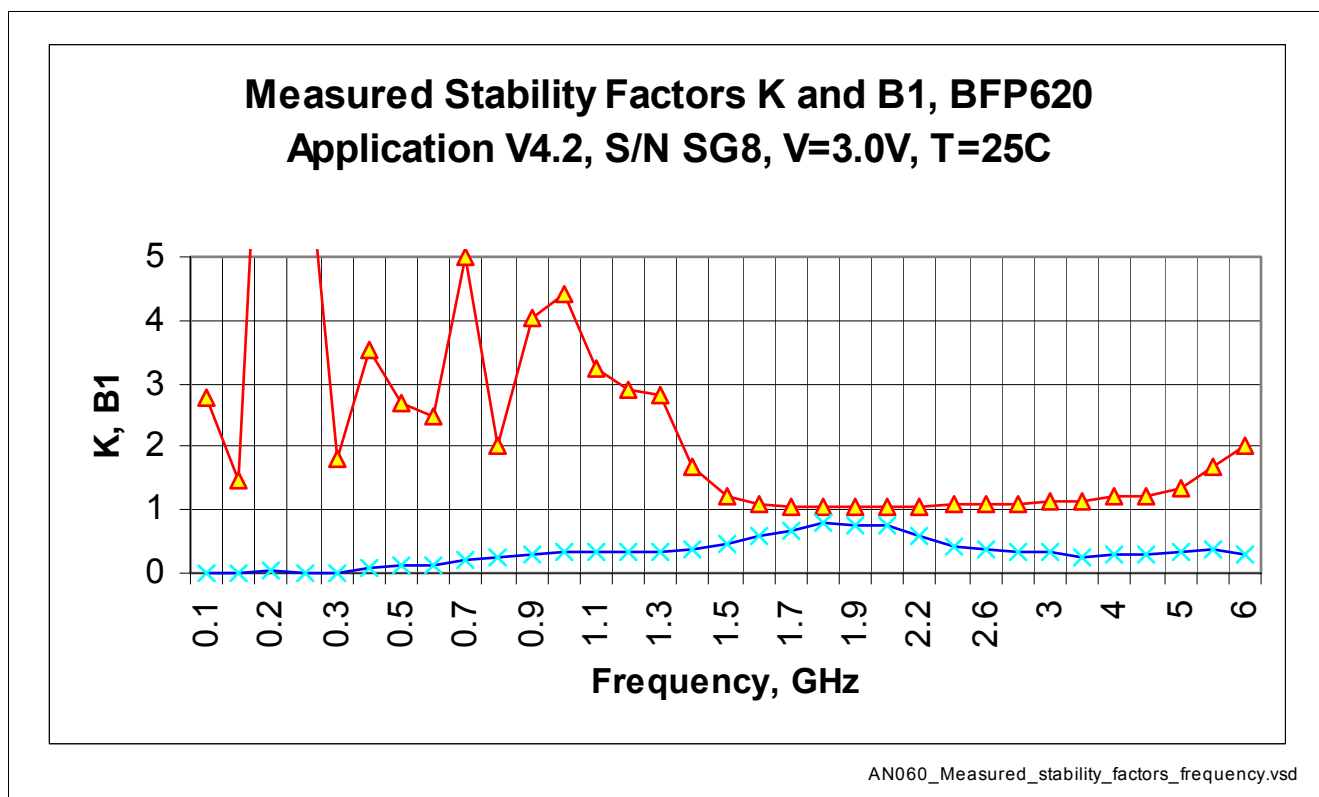


Figure 9 Measured stability factors K and B₁ and B₁ vs. frequency for a V4.3 BFP620 Applications Board. Compare to simulated results in Figure 8. Measurement range is 100 MHz to 6 GHz

2.2 Noise Figure

The BFP620 is capable of excellent noise figure performance up to 6 GHz, and offers noise figure values comparable to more expensive PHEMT and GaAs MESFET devices.

Near 2 GHz, the bias current for minimum noise figure is about 5 mA. However, the +10 dBm Input IP_3 requirement could not be met with only 5 mA of current, and for this particular application a minimum current of approximately 8 mA is required.

Table 4 gives noise parameters for the BFP620 at 1.8 GHz and a V_{CE} of 2 V at 5, 8 and 10 mA collector current. This should help the reader in understanding how bias current influenced noise figure in this design. If the +10 dBm IIP_3 requirement were dropped (e.g. as would be the case in a "low-desense requirement" LNA design), less current (and less emitter degeneration) could be used - and noise figure values of just under 1.0 dB in an application circuit should be possible.

Table 4 BFP620 Noise Parameters at 1.8 GHz for $V_{CE} = 2.0$ Volts

I_C mA	F_{min} dB	Γ_{opt} mag	Γ_{opt} ang	Rn/50
5	0.65	0.16	71	0.14
8	0.71	0.09	97	0.08
10	0.76	0.06	111	0.11

Low Noise Amplifier Design Considerations

The emitter degeneration used for linearity improvement also had the pleasant side-effect of moving the optimum noise match and return loss match at bit closer together in terms of impedance. A plot of noise figure for a BFP620 V4.2 Application Board is given in [Table 10](#).

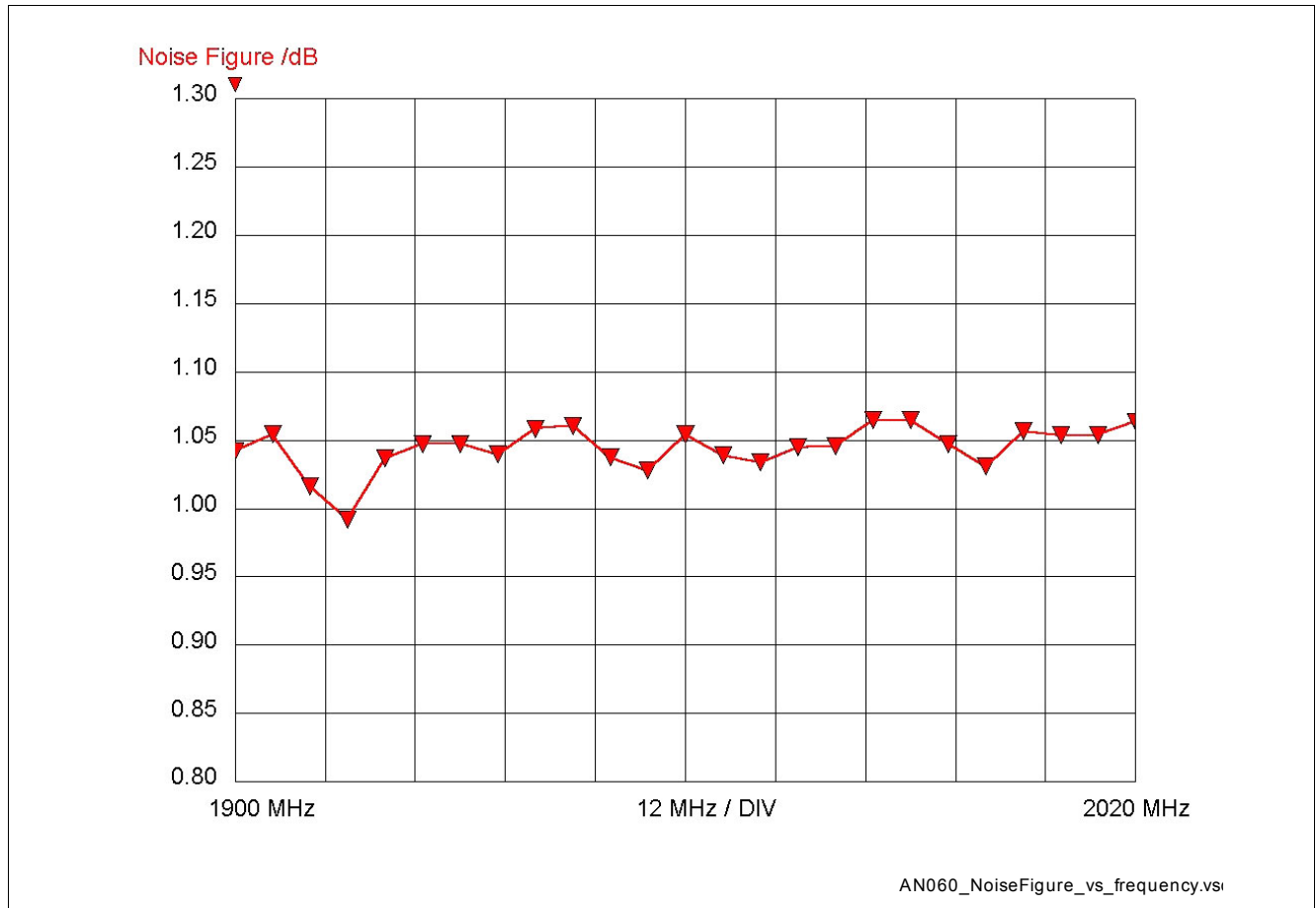


Figure 10 Plot of Noise Figure versus Frequency for BFP620 V4.2 Application, PC Board Serial Number SG8. Span is 1900 to 2010 MHz. Temperature = 25 °C

2.3 Input / Output Match

As stated in the previous section, the use of added emitter inductance helped to move the optimum noise match and optimum return-loss match closer together in terms of impedance.

The output matching circuit is a high-pass network consisting of L2 and C2. Due to the non-zero S12 of the device, the output matching circuit was used to favorably influence the input return loss.

The influence of the output matching circuit on the input return loss together with the positive effect of the added emitter inductance for both return loss and noise matching enabled the elimination of any RF matching elements at the device input. Only a 10 pF DC blocking capacitor (C1) and a coil to bring in DC bias voltage to the base (L1) were required at the input. This elimination of input tuning elements also permits optimizing the design for a balance of input return loss and noise figure with fewer iterations. A good linear RF simulation tool is very helpful in gaining insight into circuit behaviour and trends in this regard.

At the input, L1 presents a relatively high impedance at the 1900 MHz PCS band, and as such has minimal influences on the input match of the circuit. This coil has a minimum self-resonant frequency of 2300 MHz, which lies above the LNA's nominal frequency range.

The input and output return loss for a typical BFP620 Version 4.3 Application at the low, middle and upper edge of the PCS band is shown in [Table 5](#).

Table 5 Input and Output Return Loss for BFP620 V4.3 Application, S/N MS6

Frequency MHz	DB[s11] ²	DB[s22] ²
1930	12.2	19.5
1960	13.3	15.9
1990	14.9	13.7

2.4 DC Bias

In term of the chosen DC bias setting, a compromise of the various specification targets - gain, linearity, noise figure and power consumption - had to be made. Higher current improves linearity and gain, but as shown in an earlier section, noise figure increases with higher current levels. Linearity is also improved with increased collector-emitter voltage (more voltage swing available at the amplifier output) but as one nears the collector-emitter breakdown voltage (V_{CEO}) noise figure can begin to degrade due to the onset of voltage breakdown effects.

The BFP620's worst case collector-emitter breakdown voltage (V_{CEO}) is 2.3 V, but typically is higher. Balancing and trading off the various target specification goals resulted in a nominal bias point of 2.1 V for the collector-emitter voltage and 8.9 mA for device current.

Referring to the schematic diagram in [Figure 1](#), resistor R3 drops the supply voltage down from 3.0 volts to approximately 2.1 V. R2 supplies bias to the base of the transistor. R1 is present for LNA stability improvement, not for DC bias purposes.

This simple bias circuit offers a low to moderate amount of negative feedback to compensate for DC beta variation from device to device and over temperature. If the device current increases due to temperature or device-to-device variation in DC beta, the voltage drop across R3 increases, reducing the voltage seen by the base, thereby providing negative feedback. The DC current shift over the -40 to +85 °C range for a Version 4.3 BFP620 application board is shown in [Table 6](#), along with gain and input 3rd-order intercept variation over this same temperature range. Note that the current varies by only 7.5% from cold to hot in spite of the limitations of the bias circuit used on this application board. If a more stable bias scheme is required, an active bias circuit using either a PNP transistor or the Infineon BCR400W active bias controller is recommended [\[2\],\[3\]](#).

Table 6 Bias Current, Gain and IIP_3 ¹⁾

Parameter	Temperature			Variation, Δ% ²⁾ Cold to Hot
	-40 °C (Cold)	+25 °C (Room)	+85 °C (Hot)	
-	-	-	-	-
Bias Current, mA	8.8	9.3	9.5	7.5%↑
Gain, dB	15.1	14.7	14.1	6.8%↓
IIP_3 , dBm	+9.2	+10.2	+10.3	10.8%↑

1) Variation from -40 to +85 °C in a BFP620 V4.3 Applications Board, Serial Number MS11. Note that a simple resistive bias scheme is used ([Figure 1](#))

2) Variation is defined as the total swing in parameter value divided by the nominal (room temperature, 25 °C) value, with the result subsequently multiplied by 100.

3 Summary / Conclusions

Infineon's Silicon-Germanium BFP620 bipolar transistor offers a very high performance, power-efficient and cost-effective solution for high frequency low noise-amplifier (LNA) designs.

This application note describes a high-linearity LNA design for 1900 MHz PCS band applications. The BFP620 is also a good solution for low-noise amplifiers operating in the European and Asian UMTS / WCDMA frequency ranges. Evaluation boards for the LNA application depicted in this Application Note are available from Infineon Technologies.

References

- [1] Vladimir Aparin, Charles Persico, "Effect of Out-Of-Band Terminations on Intermodulation Distortion in Common-Emitter Circuits".
- [2] "Application Considerations for the Integrated Bias Control Circuits BCR400R and BCR400W" Application Note No. 014, Infineon Technologies, Silicon Discretes Group.
- [3] RF Design Guide, Systems, Circuits, and Equations. Peter Vizmuller, Artech House, 1995, ISBN 0-89006-754-6. (Pages 76-78 show active biasing of an RF bipolar transistor.)
- [4] "A 1.9 GHz Low Noise Amplifier optimised for high IP_3 using BFP540" Application Note No. 057, Infineon Technologies, Silicon Discretes Group. (Use of a large value capacitor across the base-emitter junction of a BFP540 transistor for IP_3 improvement is discussed).

4 Appendices

4.1 Appendix A. Scanned Images of BFP620 Application Board

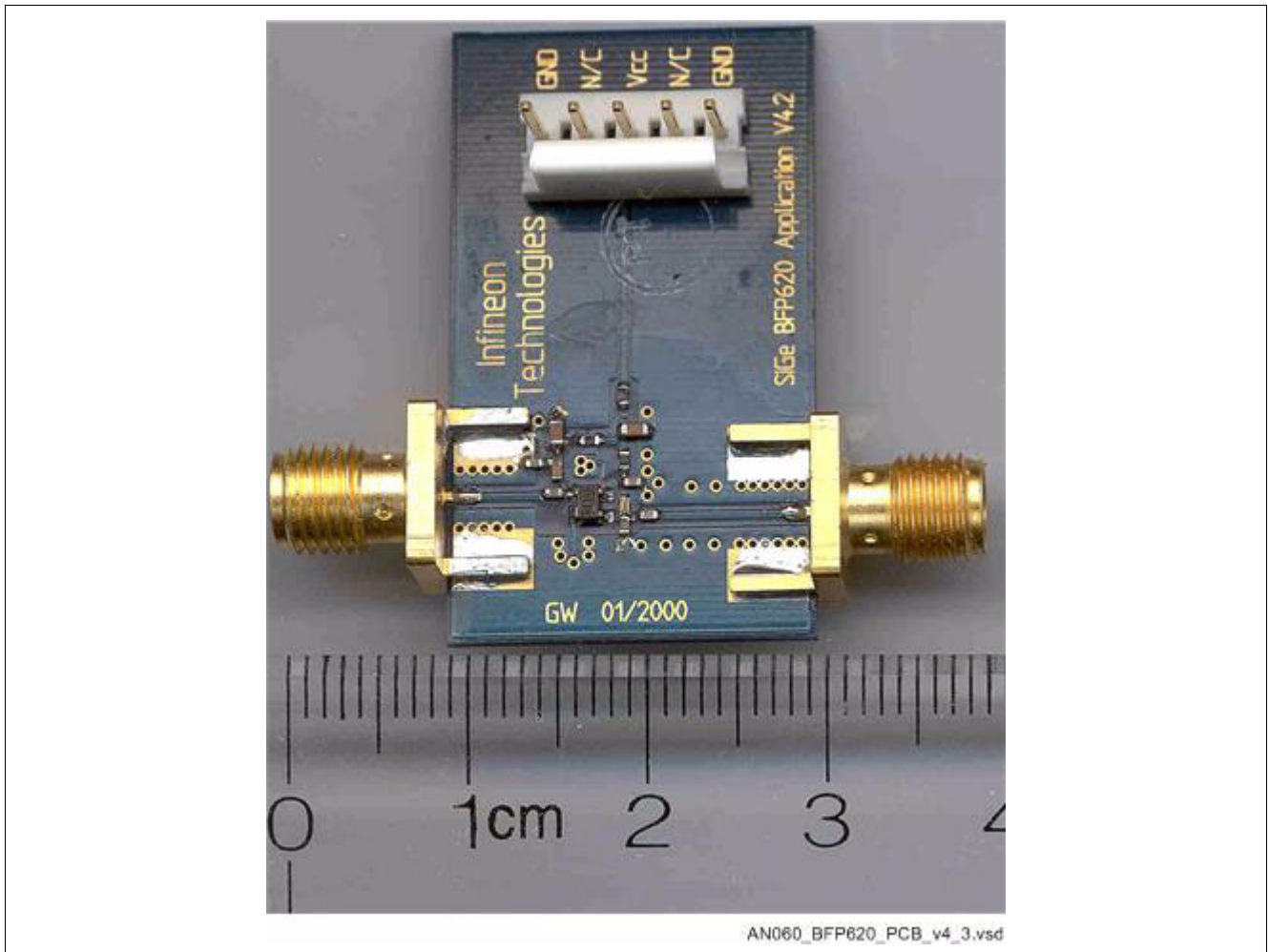


Figure 11 View of Version 4.3 Printed Circuit Board

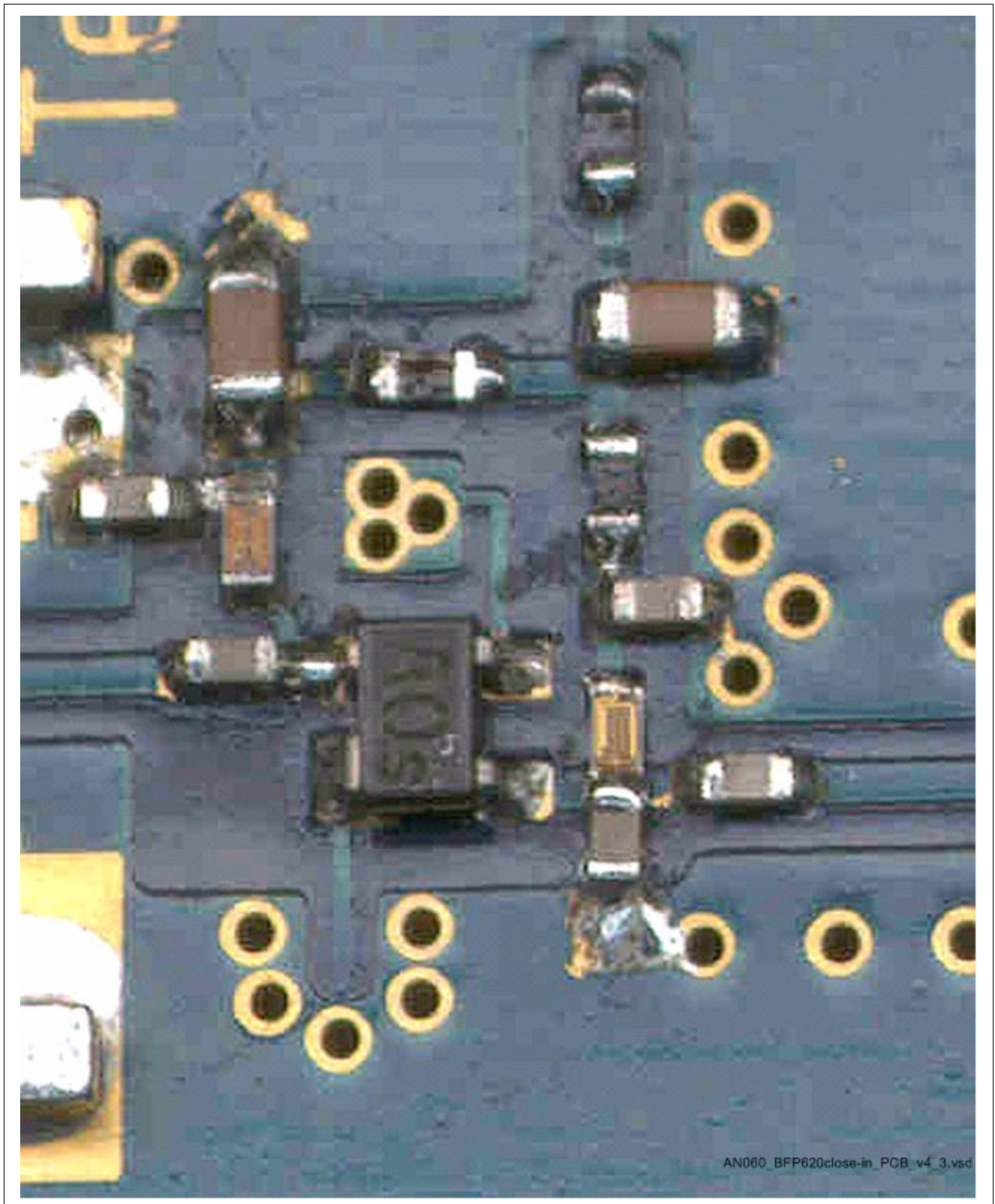


Figure 12 Close-in shot of BFP620 V4.3 PCB showing parts placement. Microstrip lines used for inductive emitter degeneration are visible between each of the two emitter leads and ground vias

4.2 Appendix B - Data Plots for a BFP620 Version 4.3 Application Board, Serial Number MS5

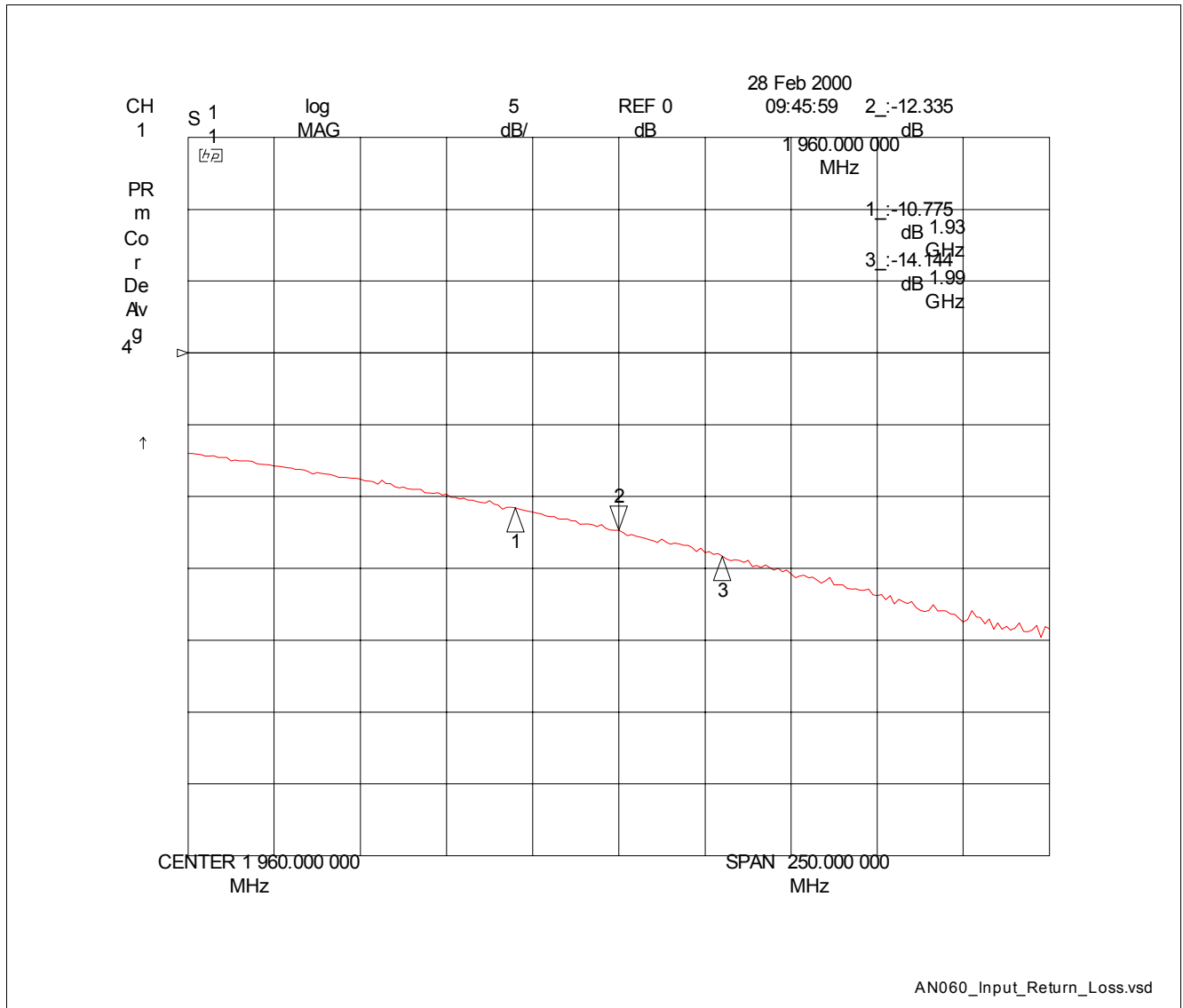


Figure 13 Input Return Loss, Log Mag

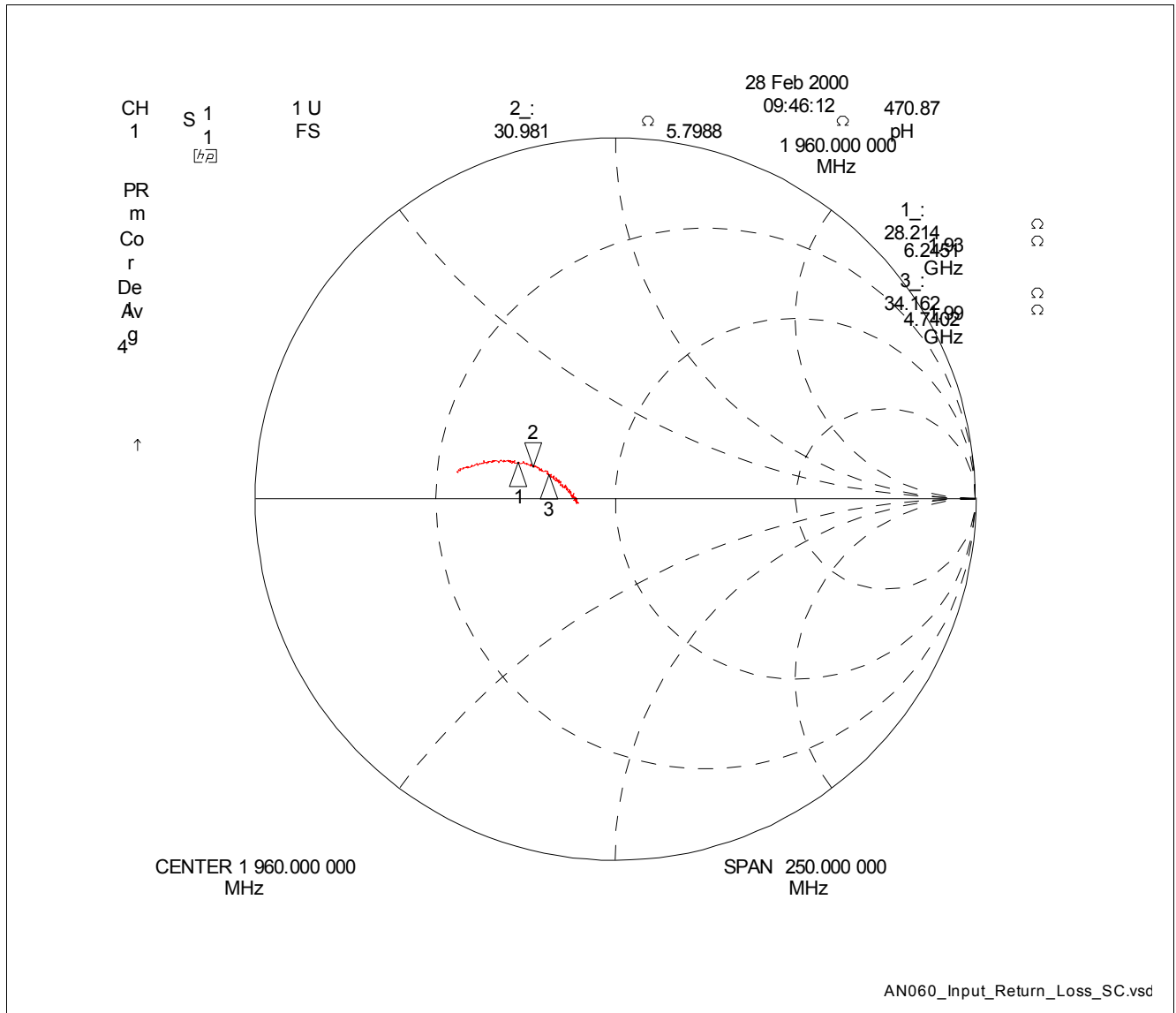


Figure 14 Input Return Loss, Smith Chart

Attention: The reference plane is normalized to the PC board RF Input Connector.

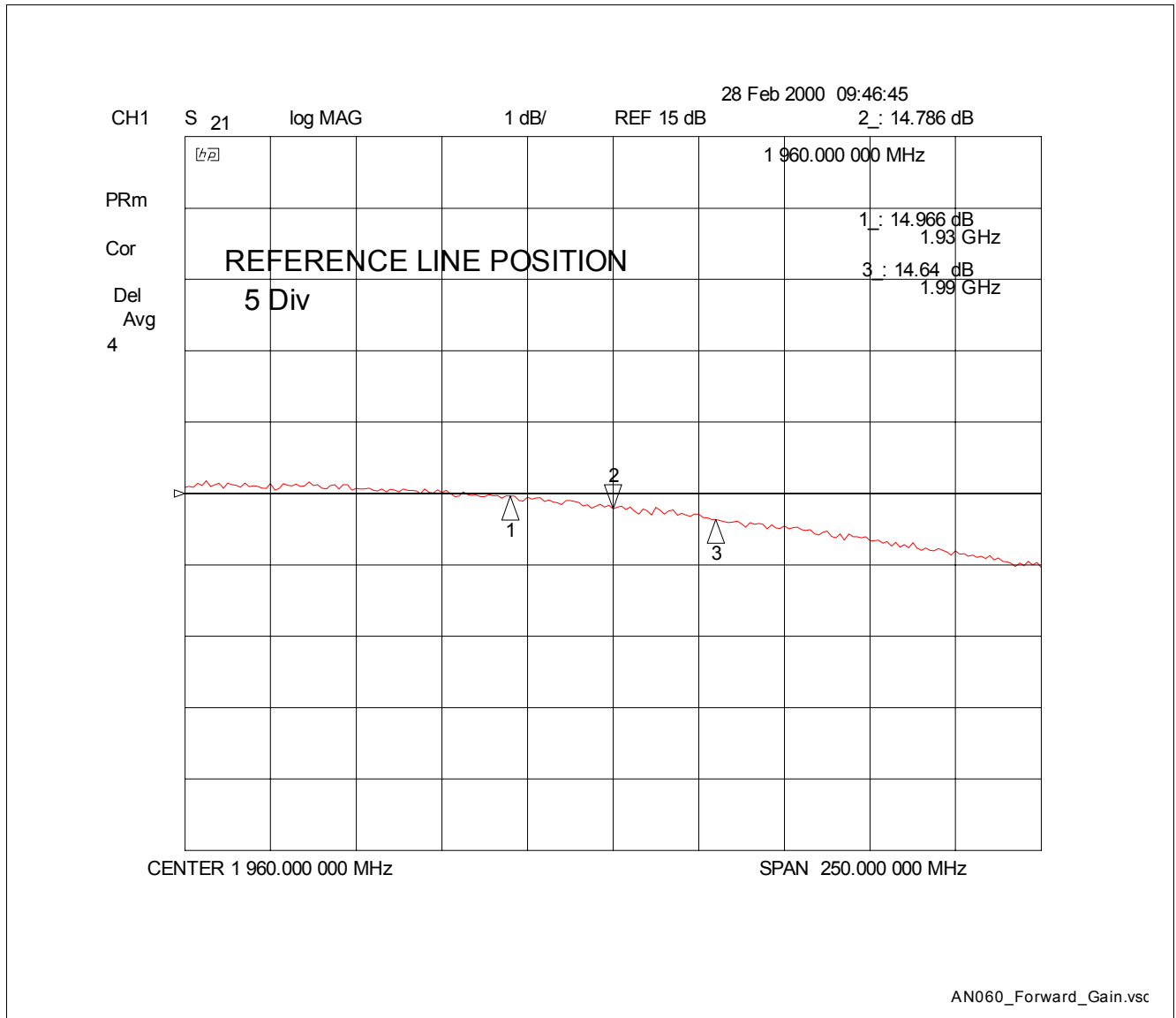


Figure 15 Forward Gain

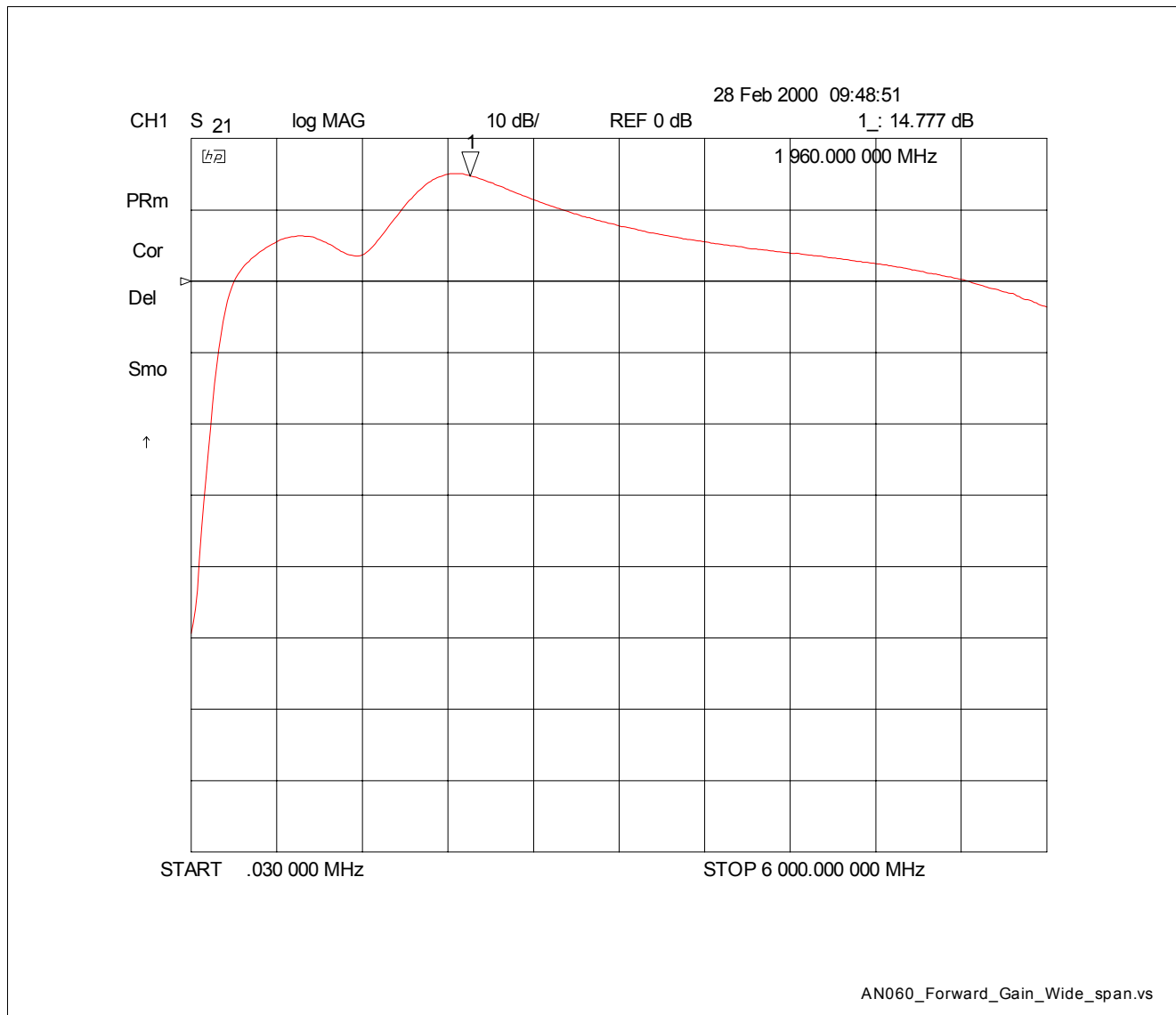


Figure 16 Forward Gain, Wide span (30 kHz - 6 GHz)

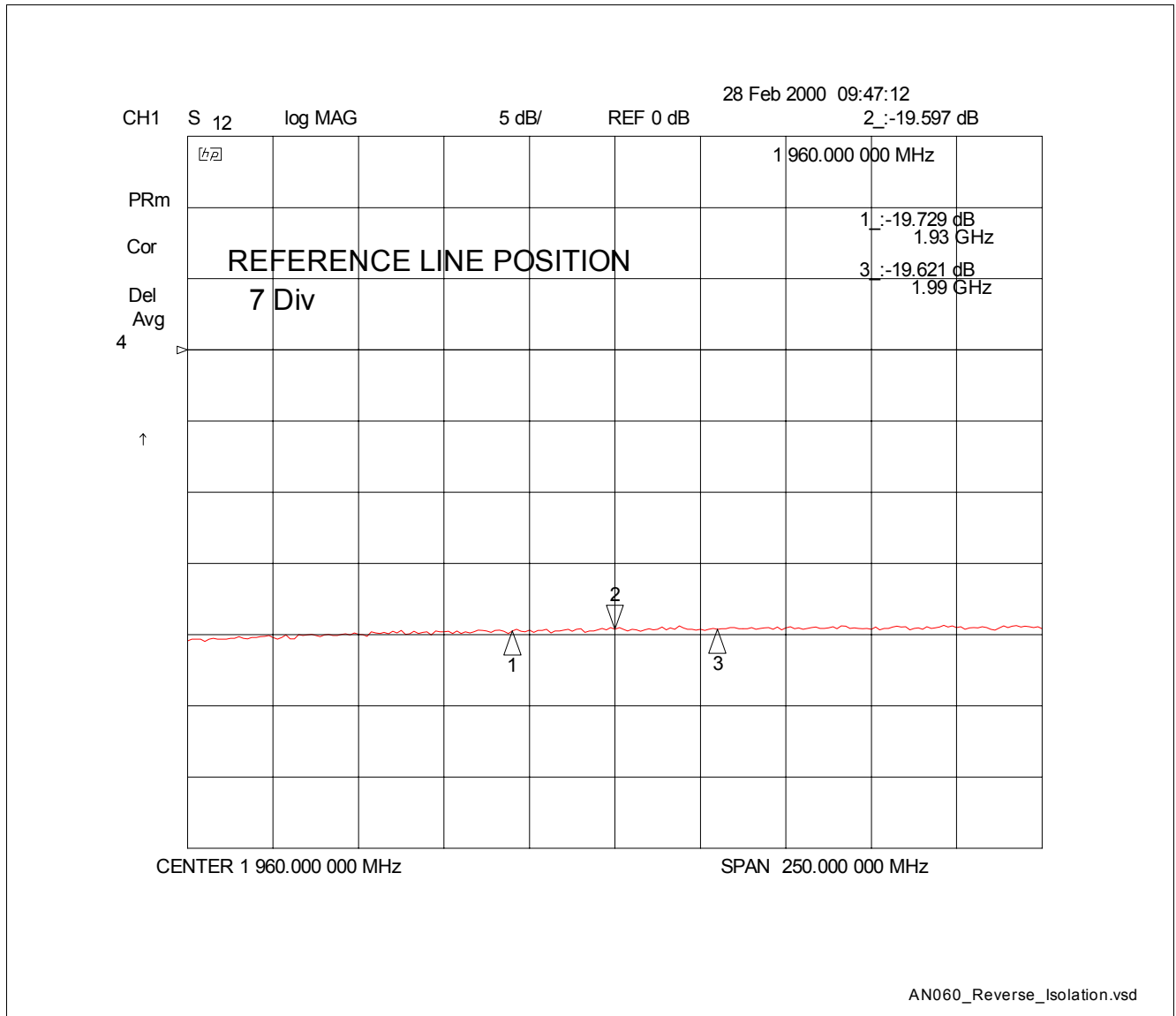


Figure 17 Reverse Isolation

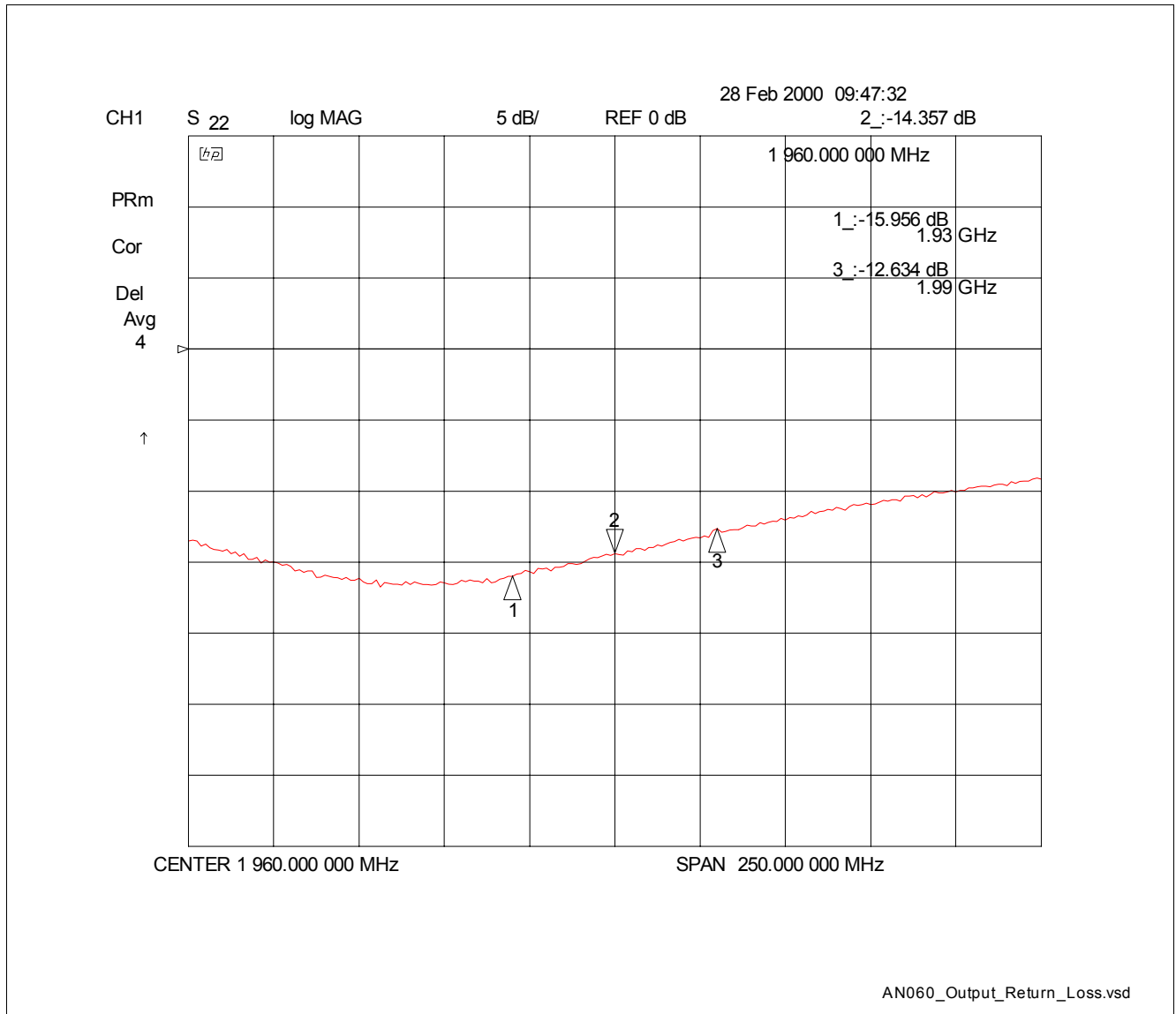
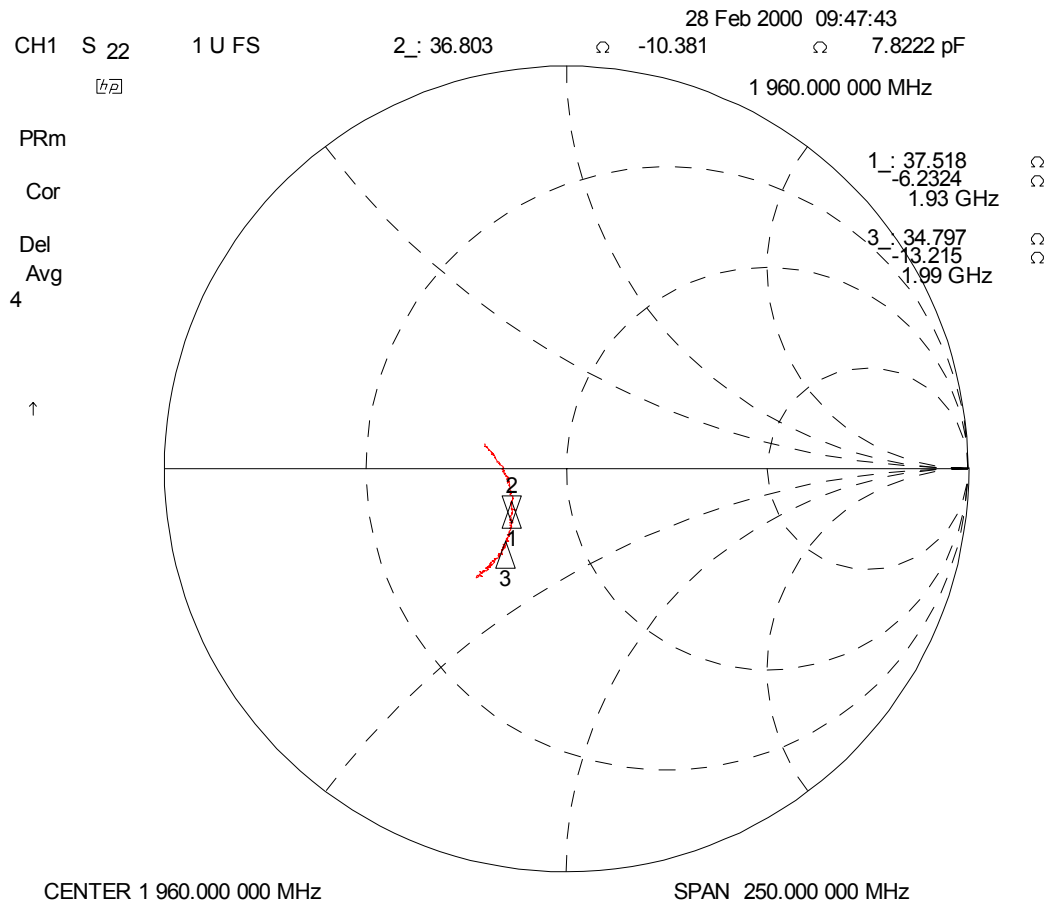


Figure 18 Output Return Loss, Log Mag



AN060_Output_Return_Loss_LM.vsd

Figure 19 Output Return Loss, Smith Chart

Attention: The reference plane is normalized to the PC board RF Output Connector.

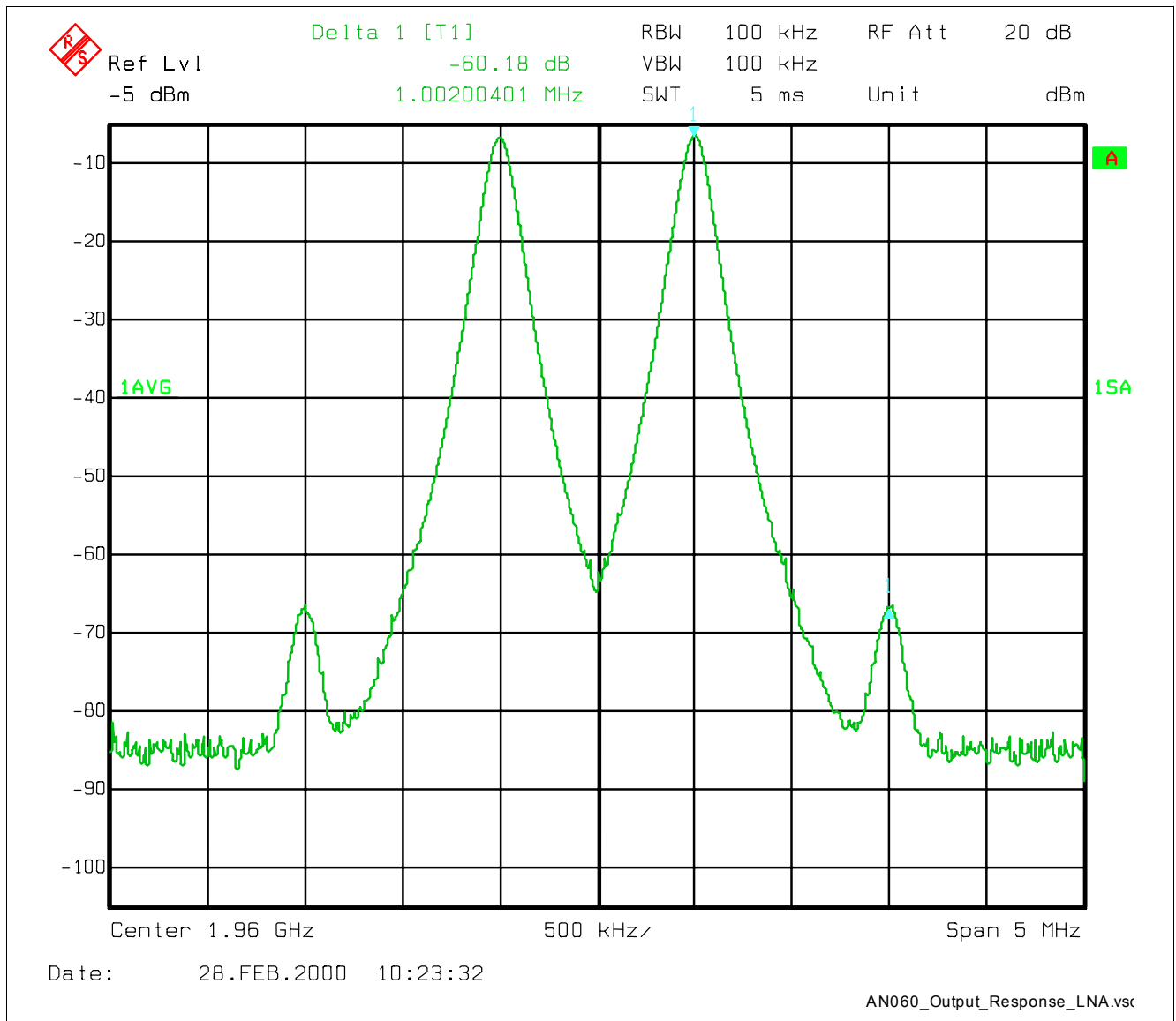


Figure 20 Output Response of LNA to Two-Tone IP_3 test. Input tones are $f_1 = 1959.5$ MHz, $f_2 = 1960.5$ MHz, tone power = -20 dBm each tone. Input $IP_3 = -20 + (60.98/2) = +10.5$ dBm. PC Board = V4.3, serial Number MS5

4.3 Appendix C. Data on 10 BFP620 Version 4.3 Printed Circuit Boards, taken randomly from a lot of 20 units. All Data taken a room temperature (25 °C)

Table 7

Board S/N	dB[s11] ²			dB[s21] ²			dB[s12] ²			dB[s22] ²		
	1960 MHz	1960 MHz	1990 MHz	1930 MHz	1960 MHz	1990 MHz	1930 MHz	1960 MHz	1990 MHz	1930 MHz	1960 MHz	1990 MHz
MS1	10.6	11.9	13.9	14.7	14.6	14.5	19.5	19.4	19.2	13.9	13.0	11.9
MS2	10.7	11.7	12.9	14.9	14.8	14.6	19.6	19.1	19.1	21.6	17.6	15.1
MS3	12.2	13.3	14.9	14.9	14.7	14.5	19.2	19.2	19.1	19.5	15.9	13.7
MS4	12.8	14.3	15.5	14.9	14.7	14.5	19.6	19.5	19.4	15.7	13.5	11.9
MS5	12.3	14.0	15.6	14.9	14.7	14.5	19.6	19.5	19.5	15.2	13.4	11.8
MS6	11.3	12.7	14.4	14.8	14.7	14.5	19.5	19.3	19.3	15.9	14.6	13.1
MS7	11.7	13.1	14.6	14.8	14.7	14.5	19.4	19.3	19.2	17.2	15.3	13.5
MS8	12.5	14.0	15.5	14.8	14.7	14.5	19.3	19.3	19.3	15.4	13.6	12.2
MS9	12.4	13.7	14.9	14.9	14.8	14.6	19.5	19.3	19.3	17.8	15.0	13.3
MS10	12.6	14.0	15.2	14.9	14.7	14.5	19.5	19.5	19.4	15.7	13.6	12.1

Table 8

Board S/N	Noise Figure DB			<i>IIP</i> ₃ DBm			Output <i>P</i> _{1dB} DBm	<i>V</i> _{CE} V	<i>I</i> MA
	1930 MHz	1960 MHz	1990 MHz	1930 MHz	1960 MHz	1990 MHz	1960 MHz		
MS1	1.04	1.06	1.07	+9.7	+9.8	+10.2	+6.5	2.09	8.8
MS2	1.08	1.08	1.09	+10.2	+10.3	+10.6	+5.0	2.19	8.1
MS3	1.04	1.04	1.04	+10.5	+10.7	+10.9	+5.4	2.12	8.7
MS4	1.05	1.03	1.05	+10.5	+10.4	+10.7	+5.8	2.06	9.4
MS5	1.00	1.01	1.01	+10.1	+10.1	+10.6	+6.4	2.08	9.3
MS6	0.96	0.99	0.96	+10.0	+10.2	+10.4	+6.3	2.09	9.0
MS7	1.00	1.01	1.03	+10.1	+10.4	+10.6	+6.1	2.11	8.8
MS8	1.03	1.05	1.05	+10.2	+10.3	+10.5	+6.1	2.09	9.1
MS9	1.04	1.05	1.03	+10.3	+10.5	+10.9	+4.8	2.17	8.3
MS10	1.04	1.05	1.05	+10.2	+10.4	+10.7	+5.4	2.11	9.0

“Statistics” for n = 10 BFP620 V4.3 PC Boards at the middle of band (1960 MHz). Some parameters follow directly from current variation (e.g. Output *P*_{1dB}). Note that Gain, Noise Figure and Input 3rd Order Intercept have reasonably “tight” distributions. Standard Deviation used is population standard deviation (σ_n), not sample standard deviation (σ_{n-1}).

Input Return Loss

- Mean value "x" = 13.3 dB
- Standard deviation " σ_n " = 0.87
- "Coefficient of variation "V"¹⁾ = 6.53

1) Coefficient of Variation "V" is defined as $V = (\sigma_n * 100) / x$

Output Return Loss

- Mean value = 14.6 dB
- Standard deviation = 1.36
- Coefficient of variation = 9.32

Gain

- Mean value = 14.7 dB
- Standard deviation = 0.05
- Coefficient of variation = 0.37

Noise Figure

- Mean value = 1.04 dB
- Standard deviation = 0.026
- Coefficient of variation = 2.47

Current Consumption

- Mean value = 8.9 dB
- Standard deviation = 0.39
- Coefficient of variation = 4.36

Input 3rd Order Intercept

- Mean value = +10.3 dB
- Standard deviation = 0.23
- Coefficient of variation = 2.23

Output 1 dB Compression Point (P_{1dBout})

- Mean value = +5.8 dB
- Standard deviation = 0.57
- Coefficient of variation = 9.81

4.4 Appendix D. Description and Photo of BFP620 AN060 Application Kit

The BFP620 AN060 Application Kit contains the following items:

1. Populated and tested BFP620 Version 4.3 Applications Board in anti-static bag
2. DC wire harness
3. BFP620 Datasheet
4. Copy of Application Note AN060
5. Test Data Sheet (1 page) with test results for the particular PC board in kit

The entire kit is packaged in a cardboard mailer box, the PC Board contained in the anti-static bag is sandwiched between two pieces of anti-static foam.

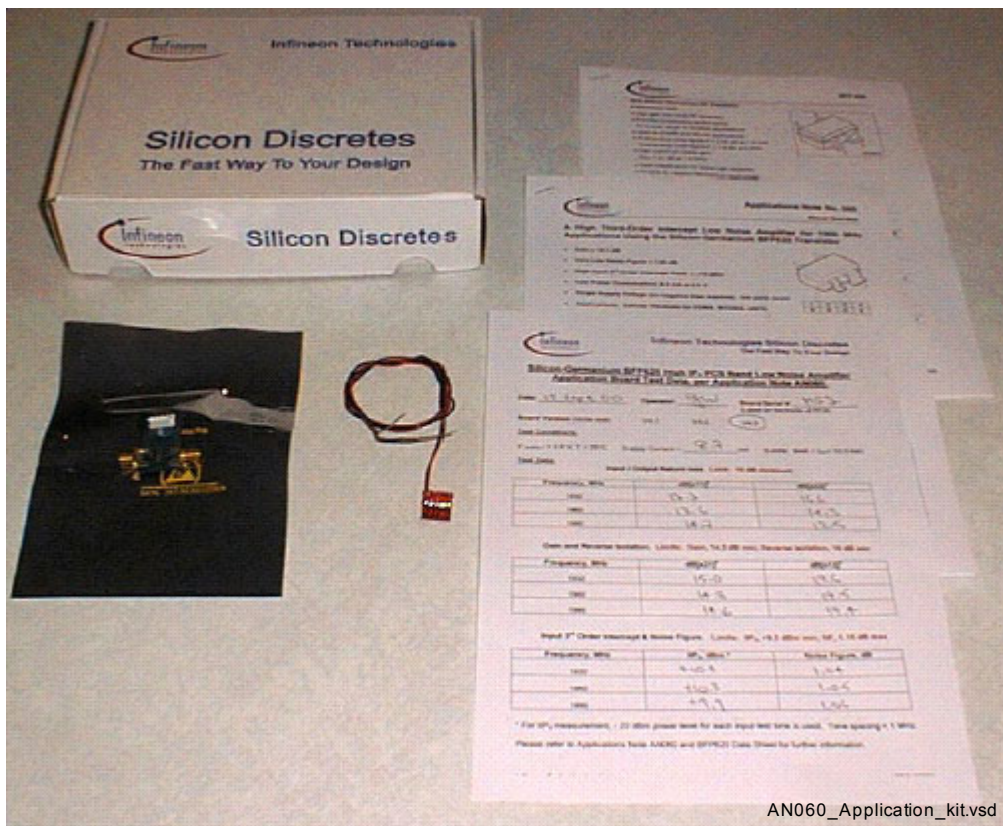


Figure 21 Photo of contents of BFT620 AN060 AN060 Application Kit