



# Tutorial 1: Step-by-Step Guide to Designing a Low Noise Amplifier for the ISM Band (2400MHz To 2500MHz)

## 1.1 Introduction

In this tutorial, we will learn the step-by-step guideline of a Low Noise Amplifier (LNA). For this tutorial, we will design an ISM band LNA for 2.4GHz to 2.5GHz applications. However, the technique presented here can be used to design LNA for any frequency band of interest.

Eight steps are involved in designing an LNA, which is given in Table 1.1. Firstly, a device will be selected. Secondly, the LNA impedances need to be obtained. Thirdly, impedance matching for the LNA should be done. The fourth step is the circuit design and simulation. As a fifth step, layout design should be done. Then Layout simulation should be conducted, followed by EM-circuit Co-simulation. Finally, simulation results will be analyzed. In this step, measurement and correlation between simulation and measurements are not included. Maybe in the future, we can include measurements and correlation analysis as well.

Table 1.1: Design Steps of a Low Noise Amplifier (LNA)

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Design
- Others

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## I) Device Selection

Remarks

### 2) Obtain LNA impedances

**SUBMIT**

### 3) Impedance matching

### RECENT POSTS

*Tutorial 4: Step-by-Step Guide in Designing and Optimization of a PCB 4G and 5G Antenna*

### 4) Circuit Simulation

*Tutorial 3: Step-by-Step Guide to Designing Balun*

### 5) Layout Design

*Tutorial 2: Step-by-Step Guide to Designing Reactively Matched Power Amplifier for the ISM Band (2400MHz to 2500MHz)*

### 6) Layout simulation

### 7) EM-Circuit Co-simulation

### 8) Results & Analysis

We will start by briefly introducing the LNA.

## 1.2 LNA Introduction

Let's start our tutorial with the LNA introduction.

Figure 1.1 shows the basic RF radio system contains a baseband processor, up-conversion Mixer, down-conversion Mixer, Voltage Controlled Oscillator (VCO), Local



coupler, antenna switch, harmonic filter, antenna, pre-driver, Low Noise Amplifier (LNA) and post-selector filter. Each radio component plays a unique and significant part in achieving the end goal of receiving and transmitting information wirelessly over a long distance.

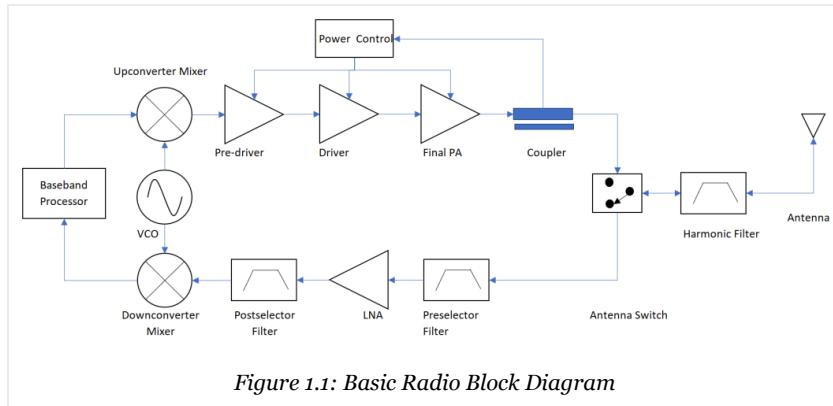


Figure 1.1: Basic Radio Block Diagram

The LNA is located at the receiver chain of the radio system. The receiver chain and LNA are shown in Figure 1.2. The signal received by the antenna will be routed to the receiver section by the antenna switch. The Preselector filter will filter out-of-band frequencies and route the received signal to the LNA. The LNA is responsible for amplifying weak received signals with the addition of minimal noise. Post-Selector Filter will further filter the received signal to be passed on to the downconverter mixer and then the baseband processor.

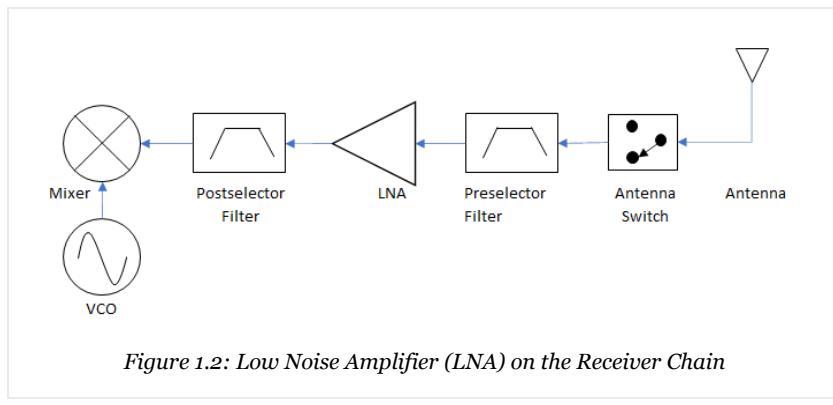
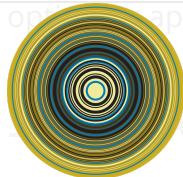


Figure 1.2: Low Noise Amplifier (LNA) on the Receiver Chain

The LNA is also responsible for providing additional isolation from the Mixer to the antenna. Since LNA



open source appropriate gain and efficiency.

## Discrete vs. Integrated Implementation

Two ways of implementing an LNA are Discrete and integrated Circuit Implementation. Each implementation has its advantages and disadvantages. Table 1.2 lists the characteristic of a Discrete LNA vs. an Integrated Circuit LNA, whereas Table 1.3 exhibits the characteristics of an Integrated LNA compared to Discrete LNA.

Table 1.2: Characteristics of a Discrete LNA vs. Integrated Circuit (IC) LNA

*Table 1.2: Characteristics of a Discrete LNA vs. Integrated Circuit (IC) LNA*

ADVANTAGE	DISADVANTAGE
Inexpensive implementation	Lower reliability compared to IC
Can be repaired if design not meeting goal during bench testing	Limited bandwidth compared to IC
Low transmission line loss compared to IC	Uncontrolled parasitics
Higher components Q	Large size
Wide variety of components / lumped elements	High assembly cost
	Limited to low frequency

Next, this table shows the characteristic of an Integrated Circuit LNA vs. Discrete LNA.



Size and Weight

## DISADVANTAGE

High cost compared to PCB

	Implementation in small quantities.
Broader bandwidth	No Tuning
Design Flexibility because we can design whatever value of lumped components we want.	Higher transmission line losses
Improved reliability	Undesired RF coupling
Good reproducibility	High Equipment cost
Lower cost in volume	Limited component values are available. Custom components can be designed but at a higher cost.
Very broad Frequency for MMIC	

Even though there are two ways of implementing LNA, both are relevant. The designer can choose one according to the product specification or application. For our application, we will be moving ahead with Discrete LNA implementation.

## 1.2.2 Cumulative Noise Figure by Friis's Equation

Friis's equation is an essential formula that enables us to calculate the receiver sensitivity. We can also calculate the IP3 and IP2 of a receiver chain. However, since we are focusing on LNA design only in this training I will stop at

components on the receiver chain are below that.

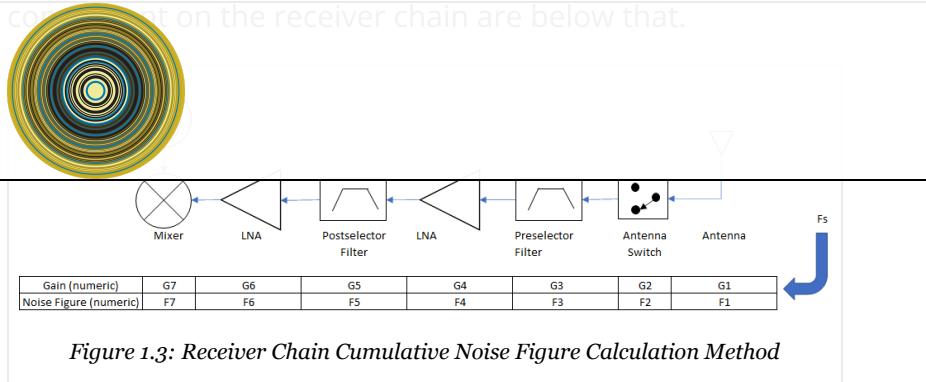


Figure 1.3: Receiver Chain Cumulative Noise Figure Calculation Method

$$F_s = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}}$$

Friis's formula calculates the total noise figure of a cascade of stages, each with its noise figure and power gain, assuming that the impedances are matched at each stage.

The Friis's Equation is given by Equation 1.1. The first term (F1) in the equation above is the most significant contributor to the cumulative noise figure because it's not divided by gain. Due to this, it's essential to minimize the noise figure of the 1st stage of the cascaded receiver system.

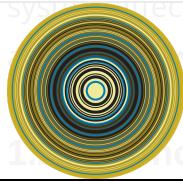
### 1.2.3 Type of Noise

In a receiver system, noise is the main obstacle. Both passive and active components generate noise. There are Six types of noise available.

#### 1.2.3.1 Thermal noise

Thermal noise, also called Johnson-Nyquist noise, is unavoidable. Its generated by the random thermal motion of charge carriers or electrons inside an electrical conductor, which happens regardless of any applied voltage.

Thermal noise is approximately white, meaning its power spectral density is nearly equal throughout the frequency



### 1.2.3.2 Shot noise

Short noise in electronic devices results from unavoidable random statistical fluctuations of the electric current when the charge carriers (such as electrons) traverse a gap. If electrons flow across a barrier, then they have discrete arrival times. Those discrete arrivals exhibit shot noise. Typically, the barrier in a diode is used. Shot noise is similar to the noise created by rain falling on a tin roof. The flow of rain may be relatively constant, but the individual raindrops arrive discretely.

The Schottky formula gives the root-mean-square value of the shot noise current  $i_n$ ;

$$i_n = \sqrt{2I_q\Delta B}$$

(1.2)

Where  $I$  is the DC,  $q$  is the charge of an electron, and  $\Delta B$  is the bandwidth in hertz.

Conductors and resistors typically do not exhibit shot noise because the electrons thermalize and move diffusively within the material; the electrons do not have discrete arrival times. Shot noise has been demonstrated in mesoscopic resistors when the size of the resistive element becomes shorter than the electron-phonon scattering length.

### 1.2.3.3 Flicker noise

Flicker noise, also known as  $1/f$  noise, is a signal or process with a frequency spectrum that falls off steadily into the higher frequencies, with a pink spectrum. It occurs in



When current divides between two (or more) paths, noise can random fluctuations during this division. For example, a transistor will have more noise than the combined shot noise from its two PN junctions.

### 1.2.3.5 Burst noise

Burst noise consists of sudden step-like transitions between two or more discrete voltage or current levels, as high as several hundred microvolts, at random and unpredictable times. Each shift in offset voltage or current lasts for several milliseconds to seconds. It is also known as popcorn noise for the popping or crackling sounds it produces in audio circuits.

### 1.2.3.6 Transit-time noise

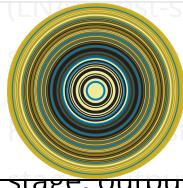
Sometimes, the time the electrons travel from emitter to collector in a transistor becomes comparable to the period the signal is amplified. In that case, at frequencies above VHF and beyond, the transit-time effect takes place, and the noise input impedance of the transistor decreases. From the frequency at which this effect becomes significant, it increases with frequency and quickly dominates other noise sources.

#### Sources:

- 1) <https://madpcb.com/glossary/noise/>
- 2) <http://eelabs.faculty.unlv.edu/docs/labs/ee460L/CommChannelModel.pdf>

## 1.2.4 LNA Stage Specs vs. nonlinear Receiver Line UP/System Specs

Nonlinear Receiver line-up specifications are usually done in Keysight SystemVue. Nonlinear receiver Line-up



(LNA, band-select filter, and mixer, and show the overall needed for the radio to operate well.

SystemVue simulates the input power to each

stage, output power from each stage, Gain, Noise Figure, efficiency, Linearity, receiver sensitivity, third-order intercept point (IP3), and second-order intercept point (IP2).

Nonlinear receiver line-up specifications need to be done for all the power modes that the radio support and consider the worst-case conditions such as lowest power and highest current drain.

## 1.2.5 LNA Parameters

These are the LNA parameters simulated using Keysight ADS.

**Pin\_RF** – is RF Input power into the LNA.

**S(2,1)** – is LNA Small Signal Gain.

**Noise Figure** – Measures how much noise the LNA introduces into the system. It will affect the sensitivity.

**OIP3** – Measures how linear the LNA is. It will affect IM performance.

**S(1,1) and S(2,2)** – is Input and Output Return Loss. It shows how well the Input and output matching is done.

**S(1,2)** – is Reverse Isolation. It shows how well LNA isolates the Input from the output.

**I<sub>ce</sub>** – is the DC drawn of the LNA

**RFfreq** – is the Frequency range of the LNA

**$\mu_{load}$ ,  $\mu_{source}$ , Real Part of Driving Point Admittance,**

**Bilateral (True Return Ratio) Loop Gain** – How stable is the PA to variations in load VSWR, Temperature, voltage, and input power?



and output. The stability can be solved by avoiding signals input from coupling in-phase with the Input. Stabilization can be checked in the design stage by simulating S-parameters for various load conditions. Stability factors such as  $|\mu_{load}|$  and  $|\mu_{source}|$  can be used to predict stability margins.

We will also study WS Probe stability analysis. WS Probe has many stability analyses within. We will analyze the “Real Part of Driving Point Admittance” and “Bilateral (True Return Ratio) Loop Gain” in the WS Probe.

Common Stability fixes are Collector and Base bypass capacitor, RC-feedback (sacrifices gain at low frequencies for stability), Input resistive loading (sacrifices noise figure), Output resistive loading (sacrifices gain, power, IIP3), and Emitter feedback resistor (sacrifices gain at high frequencies).

## 1.3 Step 1: Device Selection

The most important step but often undermined. The device must be selected based on the LNA stage specification derived from the transmitter line-up or system specifications.

### 1.3.1 Design Specification

To select a device, we need to have design requirements for the LNA. The LNA design requirement is derived from the transmitter line-up specification. Generally, a technical manager or team leader will handle transmitter line-up specifications, and engineers will be given specifications to design the LNA accordingly.

These are the specifications we would like to focus on for this tutorial. The frequency range of the LNA is 2.4GHz to 2.5GHz, and the gain is around 20dB. The design should be unconditionally stable across a wide frequency range. Input

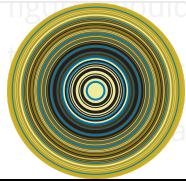


Table 1.4: Design Requirements of LNA

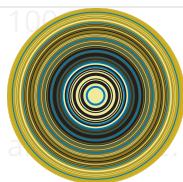
Table 1.4: Design Requirements of LNA

DESIGN PARAMETERS	DESIGN SPECIFICATION
Frequency range	2.4GHz – 2.5GHz
Gain	~20dB
Stability	$\mu_{\text{source}} & \mu_{\text{load}} > 1$ , $\text{Real}(1/C.H_0) &$ $\text{Real}(1/B.H_0) > 0$ , $\text{dB(LGC)}, \text{dB(LGB)} < 0$
Input Return Loss ( $S_{11}$ )	< -10dB
Output Return Loss ( $S_{22}$ )	< -10dB
Noise Figure	< 1dB
IP3	> 15 dBm

### 1.3.2 Understanding Device Technology

Device technology needs to be understood to select a suitable device effectively. The selection of a device is the most crucial step. The device must be chosen based on the LNA stage specification.

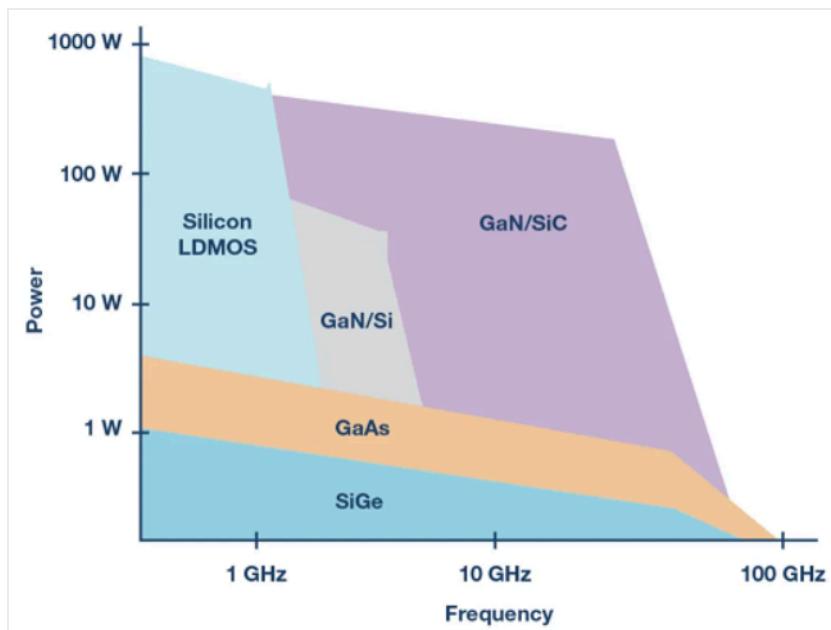
Device technology must be understood to effectively select a suitable device for our Driver LNA. Please take a look at the graph attached here. This graph is taken from the analog devices website. As you can see, device technology varies as we vary the power level and the frequency. For low power applications of less than 1W, SiGe is most



above 6W, Silicon LDMOS, GaN/Si, and GaN/SiC  
and SiGe. For high-power and low-frequency

applications, Silicon LDMOS is most suitable. For high-power and mid-frequency applications, GaN/Si devices will serve better. For high-power and high-frequency applications, GaN/SiC devices are the best.

Besides power and frequency, the supply voltage also dictates device selection because the device supply voltage varies from 2V to 50V.



*Figure 1.4: Process technology comparison of microwave frequency range power electronics.*

To learn more about device technology, please go to the link below.

Source: <https://www.analog.com/en/analog-dialogue/articles/rf-power-amplifiers-go-wide-and-high.html>

### 1.3.3 Parameters of selected devices

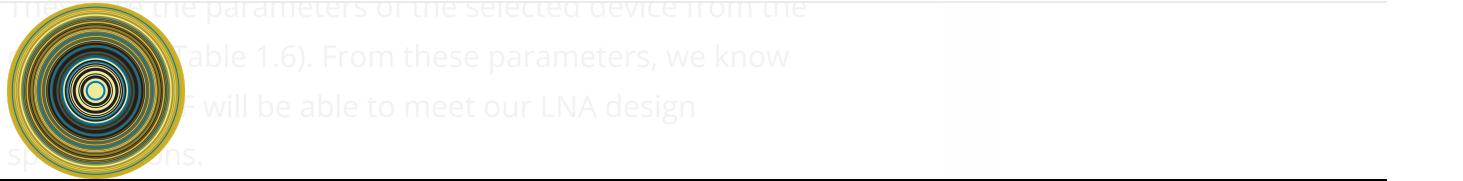


Table 1.5: The parameters of the selected device – BFU730F

*Table 1.5: The parameters of the selected device – BFU730F*

DESIGN PARAMETERS	SPECIFICATION
P1dB	12.5dBm
Noise Figure (NF)	0.55dB
IP3	26.5dBm@2.4GHz
Transition Frequency (fT)	55 GHz
Gain	21.5dB@2.4GHz
Vce (max)	2.8V
Vce (P1dB)	2.5V
Ic (P1dB)	15mA
Ic (max)	30mA
Veb (max)	1V
Ccbs (collector base capacitance)	55fF

### 1.3.4 Device Model Selection

The BFU730F supplier NXP has provided two device models: MEX and SPICE. There are two ways to select a suitable or most accurate device model. Those are comparing the



### 1.3.4.1 Compare the impedance with the s-parameters

Another way to select a device model is by comparing the simulation results of ADS models. Figure 1.5 shows the impedance simulation setup of s-parameter data.

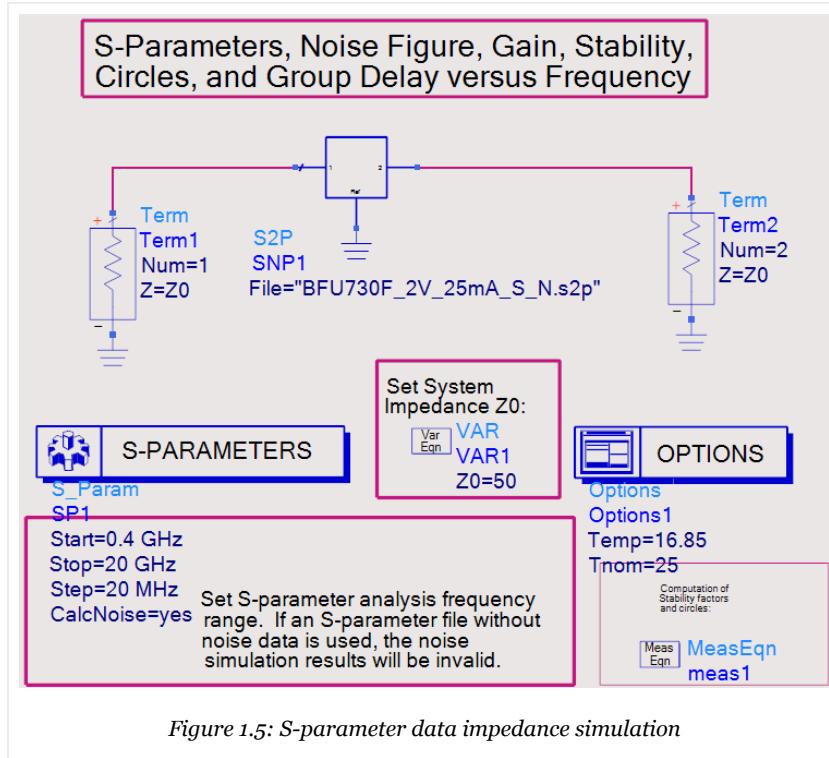
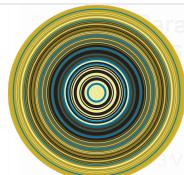


Figure 1.5: S-parameter data impedance simulation

Figure 1.6 shows the MEX model impedance simulation setup. Figure 1.7 shows the correlation between MEX model simulation and S-parameter data simulation. The MEX model correlates well with s-parameter data.



Parameters, Noise Figure, Gain, Stability, and Group Delay versus Frequency

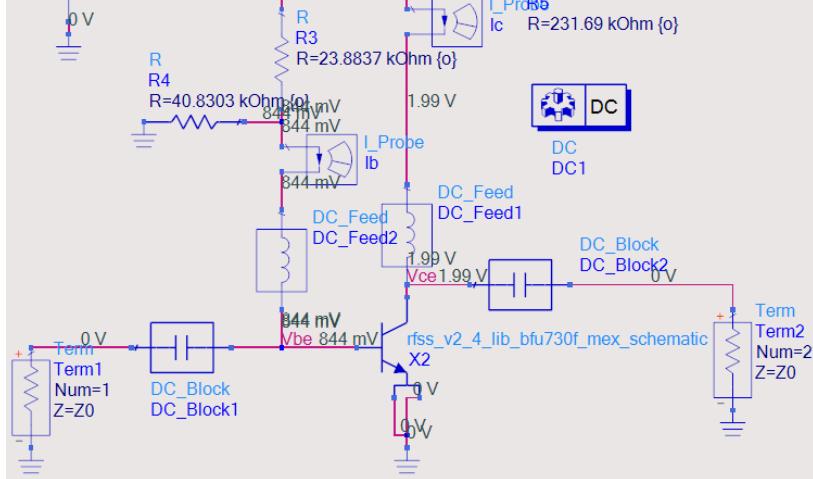


Figure 1.6: MEX model impedance simulation

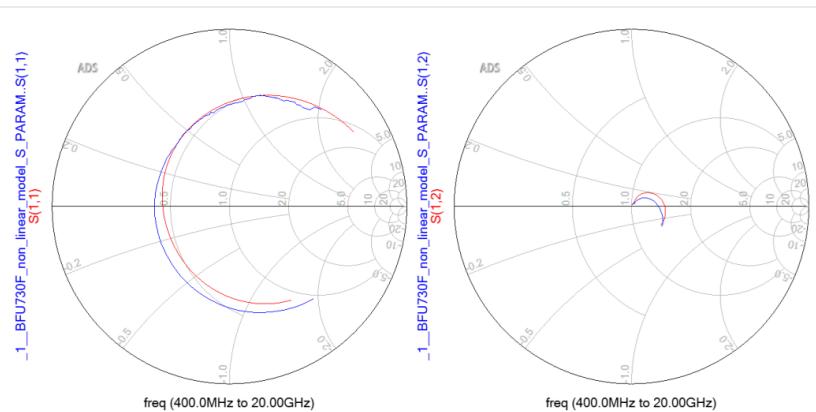
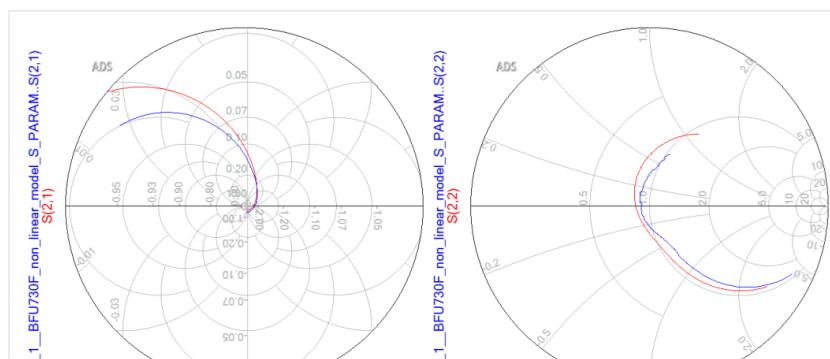


Figure 1.7: S11 and S12 of the MEX model compared to S-parameter data



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Figure 1.10 shows the correlation between the SPICE simulation and S-parameter data simulation. The plot correlates well with s-parameter data.

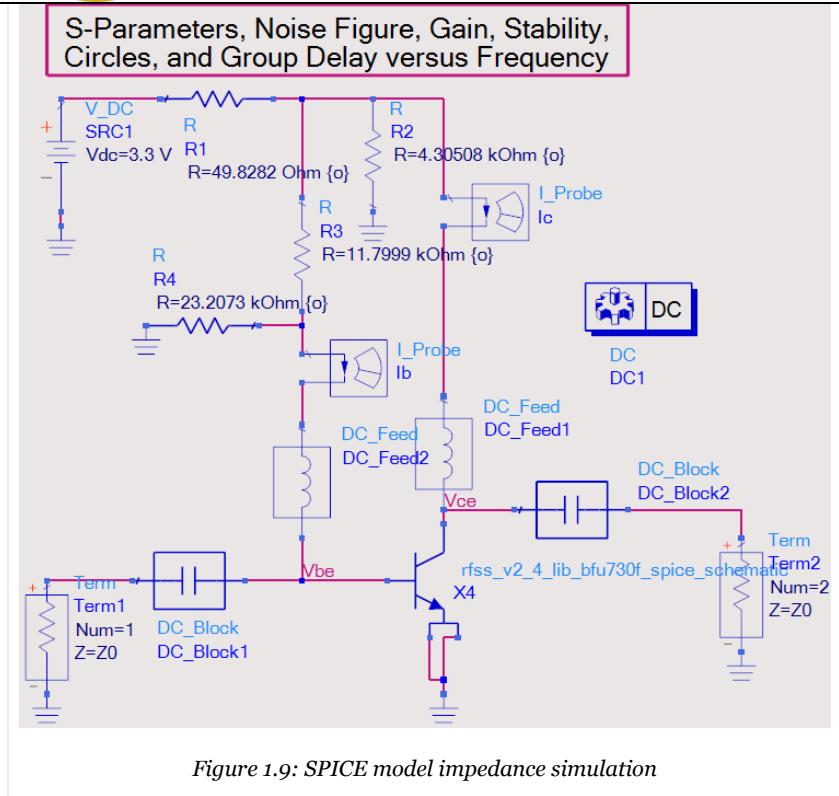


Figure 1.9: SPICE model impedance simulation

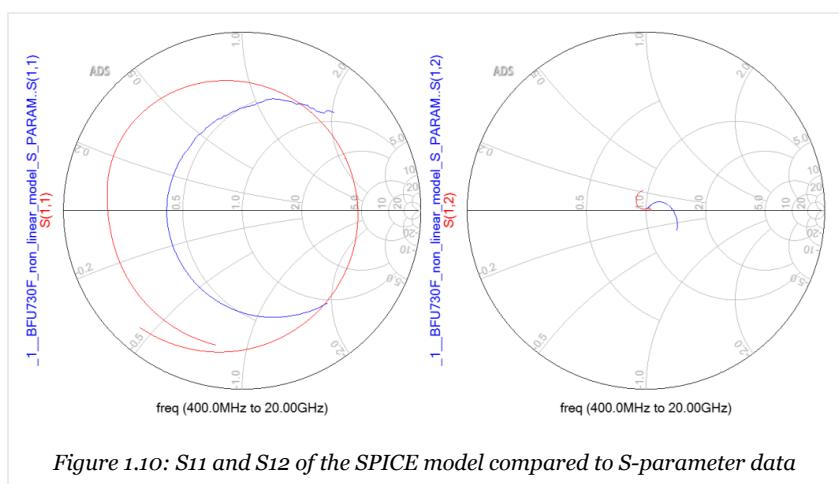


Figure 1.10:  $S_{11}$  and  $S_{12}$  of the SPICE model compared to S-parameter data

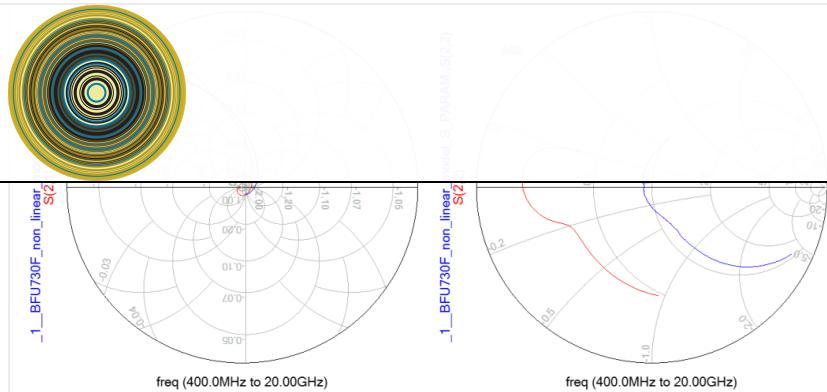
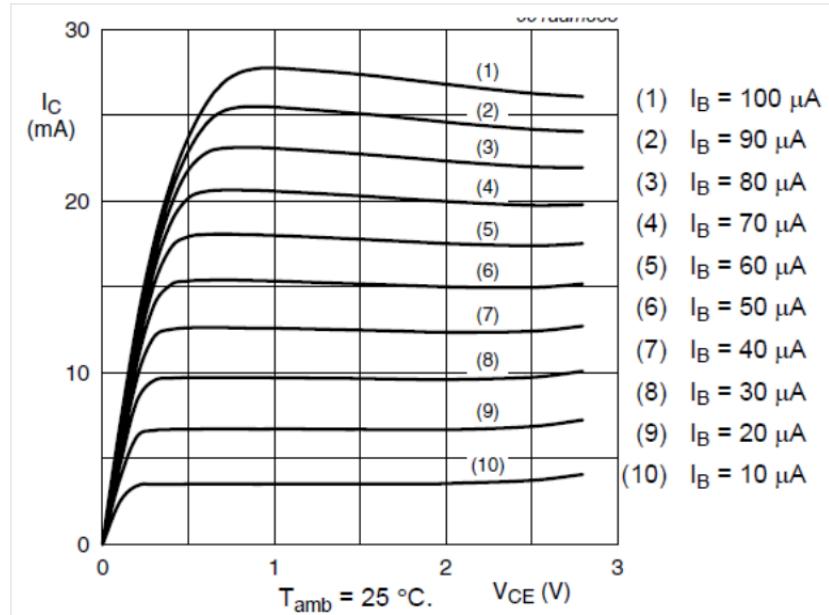


Figure 1.11:  $S_{21}$  and  $S_{22}$  of the SPICE model compared to S-parameter data

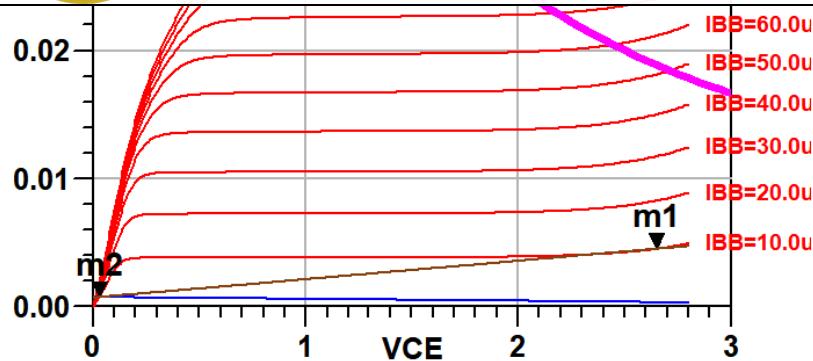
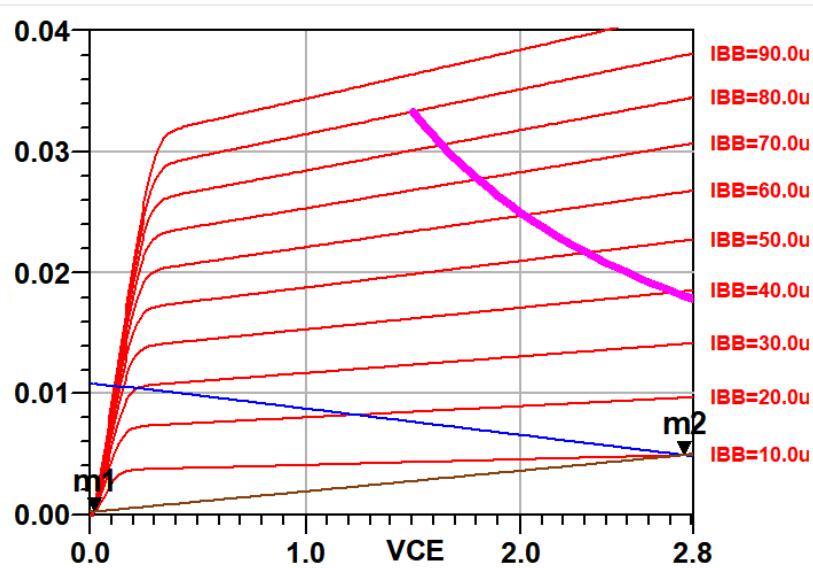
The MEX model is proven as the most accurate model for BFU730F. All the simulations in the following steps will use the BFU730F MEX model.

### 1.3.4.2 Compare the IV curve with the datasheet

Apart from the above-mentioned method, the DC Curve ( $I_C$  vs.  $V_{ce}$ ) can be used to select the most accurate device model. The  $I_C$  vs.  $V_{ce}$  from the datasheet can be compared with the  $I_C$  vs.  $V_{ce}$  plot of the MEX and SPICE model to choose the model which closely matches the datasheet.



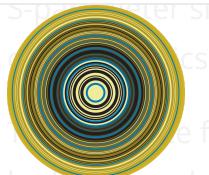
**Fig 2. Collector current as a function of collector-emitter voltage; typical values**

Figure 1.13: MEX model  $I_c$  vs  $V_{ce}$ Figure 1.14: SPICE model  $I_c$  vs.  $V_{ce}$ 

After comparing Figure 1.12 with 1.13 and 1.14, the MEX model is closely matched to the datasheet.

## 1.4 Step 2: Obtain the LNA impedances

The next step is to obtain the LNA input and output



3-parameter simulation for LNA because of the small signal.

Impedance.

for LNA impedance extraction simulation can

be found under DesignGuide > Amplifier > S-parameter

Simulations. The template's name is "S-param., Noise Fig., Gain, Stability, Circles, and Group delay versus Frequency", as shown in Figure 1.15. S-parameter data or the MEX model can be used for the impedance simulation. I have used the MEX model, as shown in Figure 1.16.

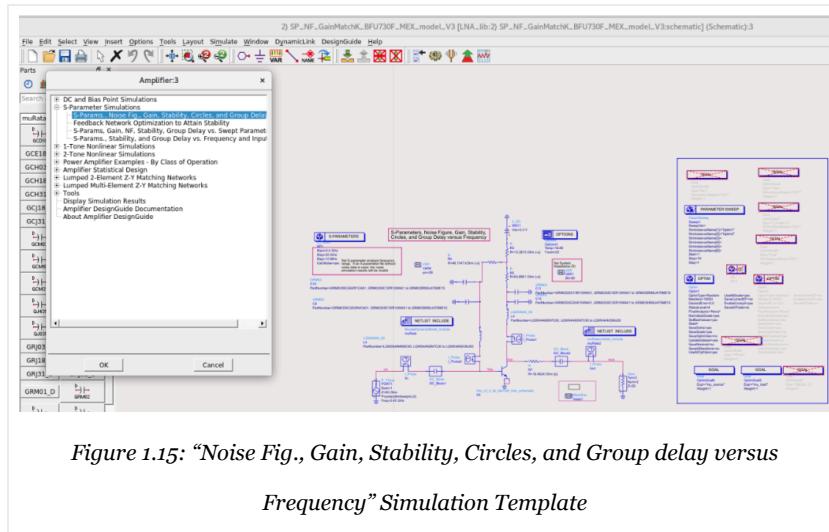


Figure 1.15: "Noise Fig., Gain, Stability, Circles, and Group delay versus Frequency" Simulation Template

We built the biasing circuit, which gives appropriate collector-emitter voltage ( $V_{ce}$ ) and base current ( $I_b$ ) according to the biasing condition of interest. The optimization setup shown on the left is done to obtain unconditional stability by optimizing RF choke, L3, and L4 and decoupling capacitors C10, C9, C11, and C12. Since these parameters are inadequate to provide unconditional stability to the LNA, we have used additional components, R7. The resistor R7 is used at the output match to trade gain for stability. With R7, we have obtained unconditional stability over a wide range of frequencies.

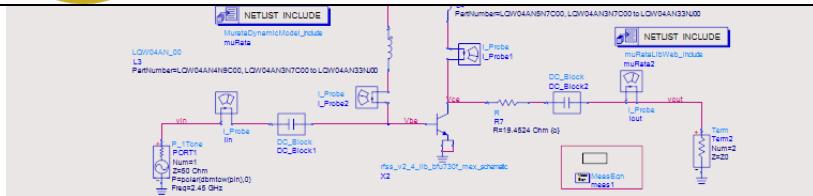


Figure 1.16: LNA impedances extraction schematic

In this Figure 1.17, we can move this RF Frequency selector marker to an appropriate frequency point, and all the boxes below show the parameters for the frequency point. We have set the frequency point at the center of our band of interest, 2.45GHz. The four boxes below the RF frequency selector show the s-parameter data.

We have two options here. The 1<sup>st</sup> one is to do matching for gain. If we select this option, we need to use these impedances to do impedance matching for our LNA, and we will get the highest gain of 22 dB.

The 2<sup>nd</sup> option is to do impedance matching for the noise figure. If we do impedance matching for our LNA using the impedances shown in the box below, we will achieve the best possible noise figure of 0.69dB. The gain is also more than 20dB, as shown in Figure 1.17. Since it will be able to meet both noise figure and gain specification, we will choose to match for noise figure, and impedances will follow as in this box.

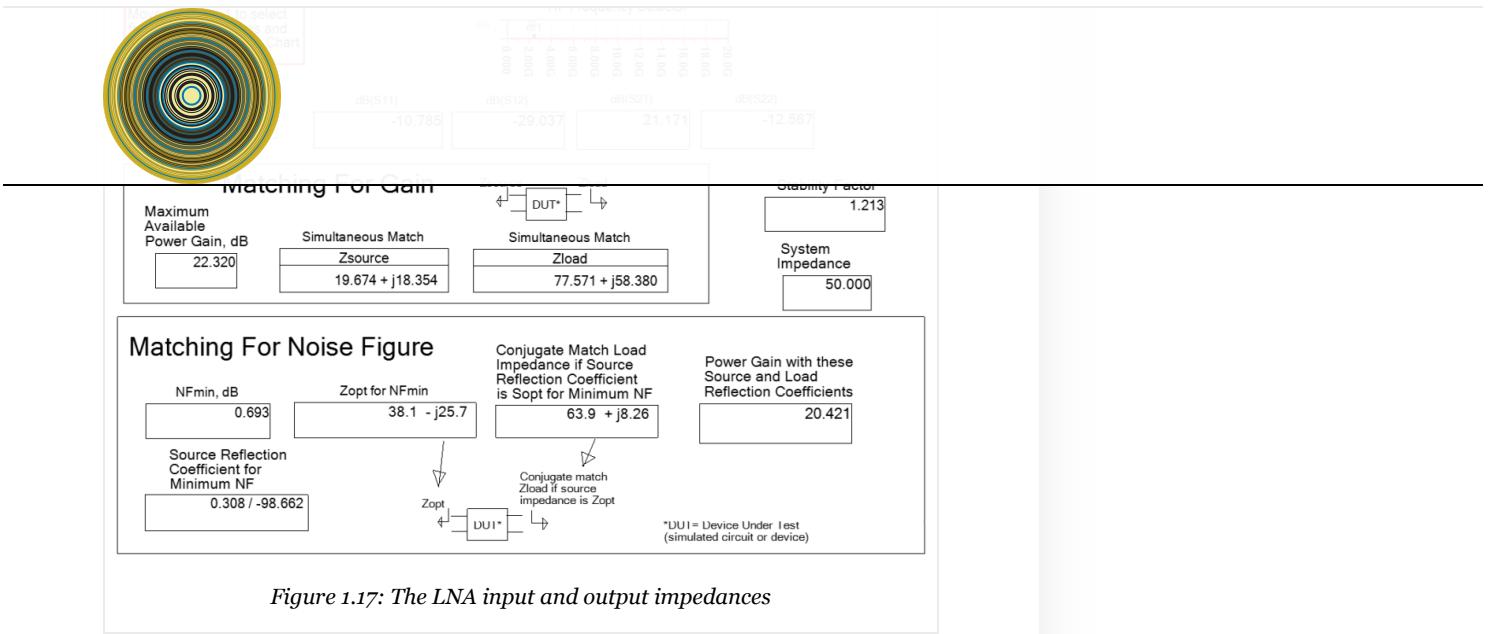


Figure 1.17: The LNA input and output impedances

## 1.5 Step 3: Impedance matching

After obtaining the impedances, we have to match the input and output impedance with 50 ohms. Impedance matching is done from LNA input and output impedance to 50 ohms. The impedance we obtained from the previous simulation is the complex conjugate LNA impedance. Its shown in figure 1.18 as  $Z_i^*$  and  $Z_o^*$ . Due to this, we need to reverse the sign of the imaginary part of these impedances to get the actual LNA impedances.

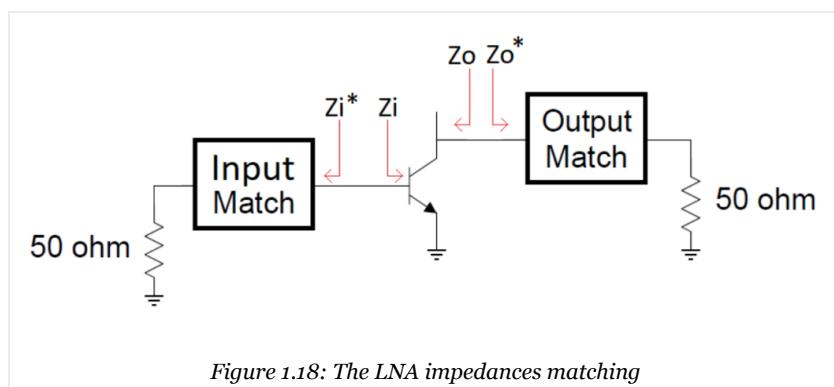


Figure 1.18: The LNA impedances matching

$Z_o^*$  – complex conjugate of output impedance

$Z_i^*$  – complex conjugate of input impedance

7 - Tutorial content index

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The next step is to do impedance matching. ADS has a brilliant impedance-matching tool called the Smith chart utility. We will be using this tool to do impedance matching.

The 1<sup>st</sup> step is to make sure the frequency is set to the center frequency of our band of interest and the characteristic impedance is set to 50 ohms. The next step is to insert the Q circle value. For our frequency band of interest, the calculated Q circle value is 8.

Next, we have to match the LNA output impedance to 50 ohms.

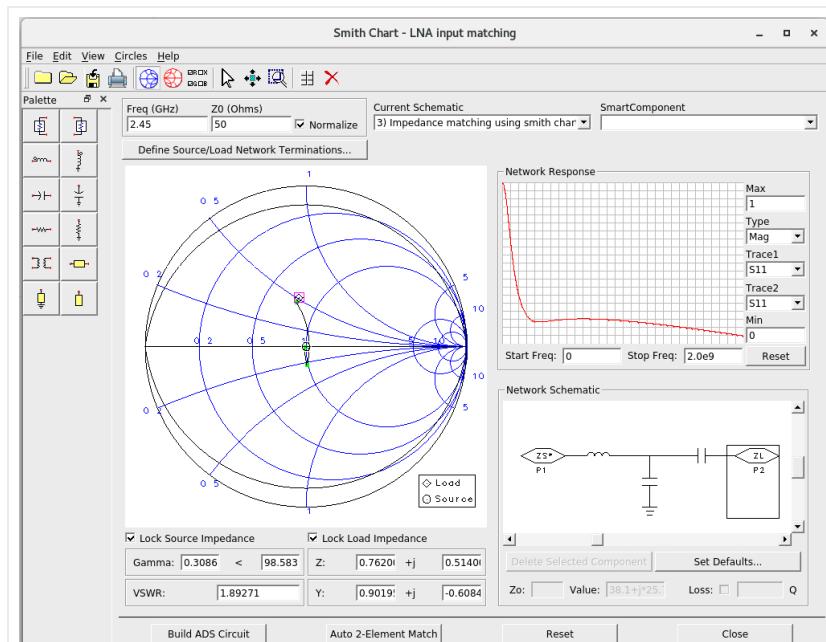
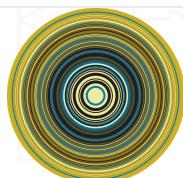
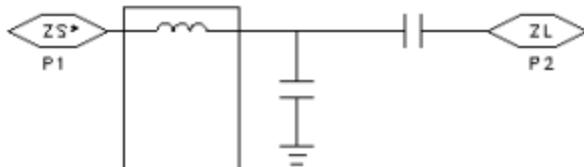


Figure 1.19: Input impedances matching using Smith chart utility



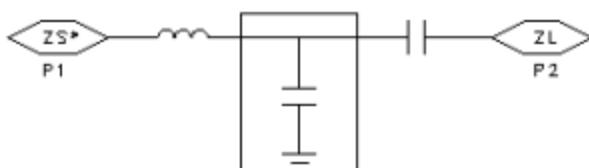
Delete Selected Component | Set Defaults...

$\text{ZS}$ :  Value:  Loss:



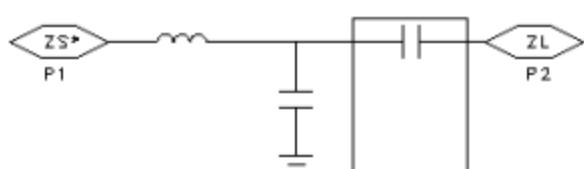
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$\text{C}$ :  Value:  pH Loss:



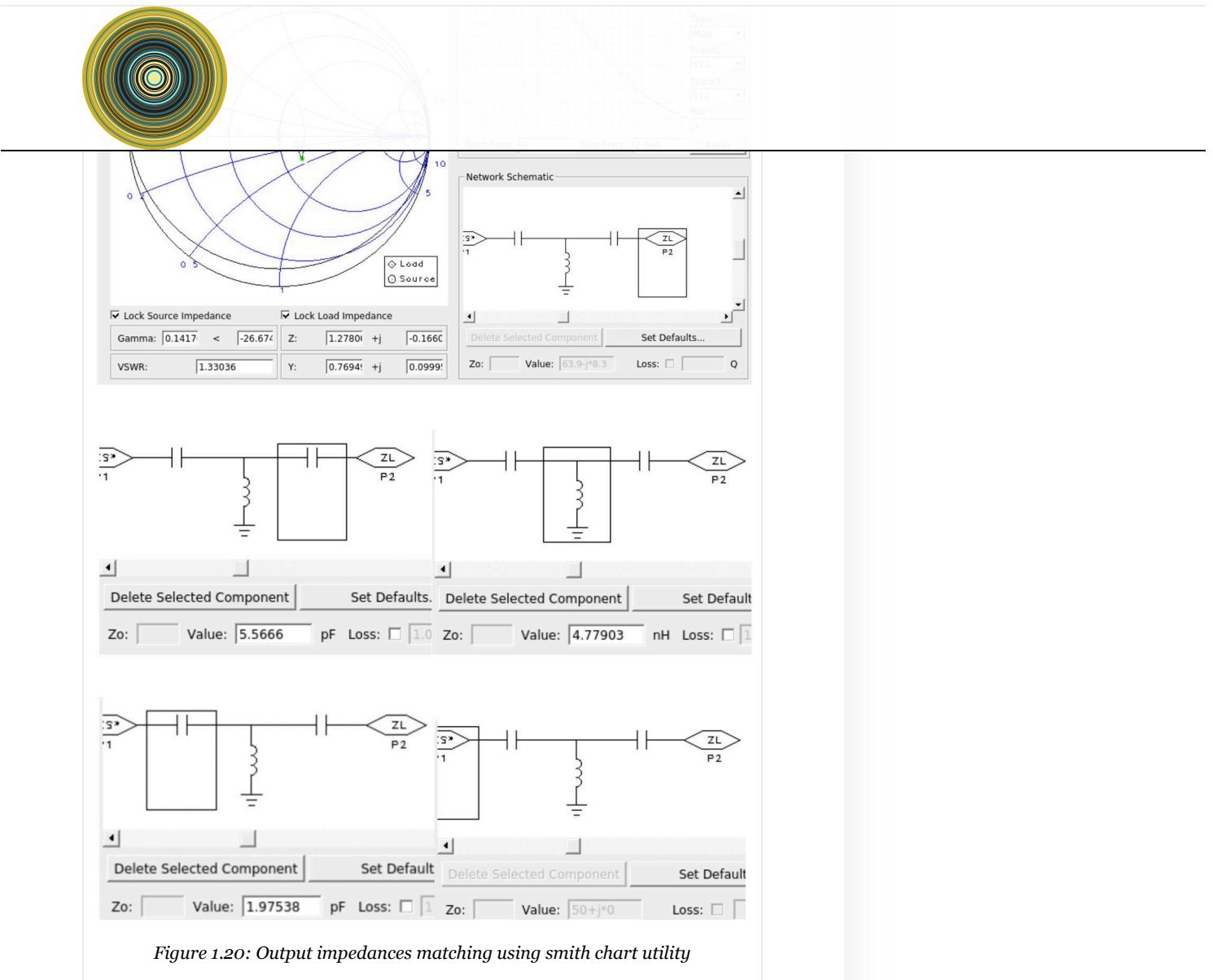
Delete Selected Component | Set Defaults...

$\text{C}$ :  Value:  pF Loss:



Delete Selected Component | Set Defaults...

$\text{C}$ :  Value:  pF Loss:



Impedance matching is accomplished for load and source impedance.

## 1.6 Step 4: Circuit Simulation

The next step is circuit simulation. Before we simulate, we need to build the circuit. Our LNA circuit is shown in Figure 1.21. The matching component values obtained from step 3 will be used in the schematic here. On top of that, the LNA circuit also contains biasing circuit. The biasing circuit

block DC from entering the RF path. I have incorporated capacitors in the Input and output matching to block the DC from entering the RF path. All these components are shown in Figure 1.21.

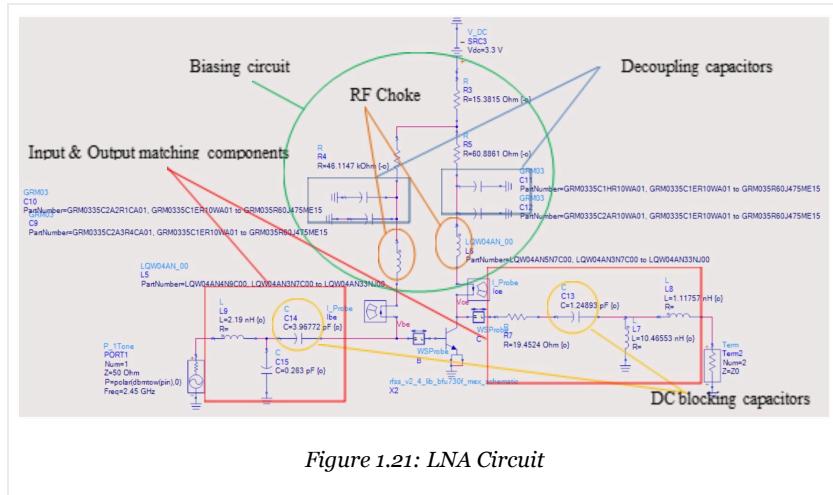
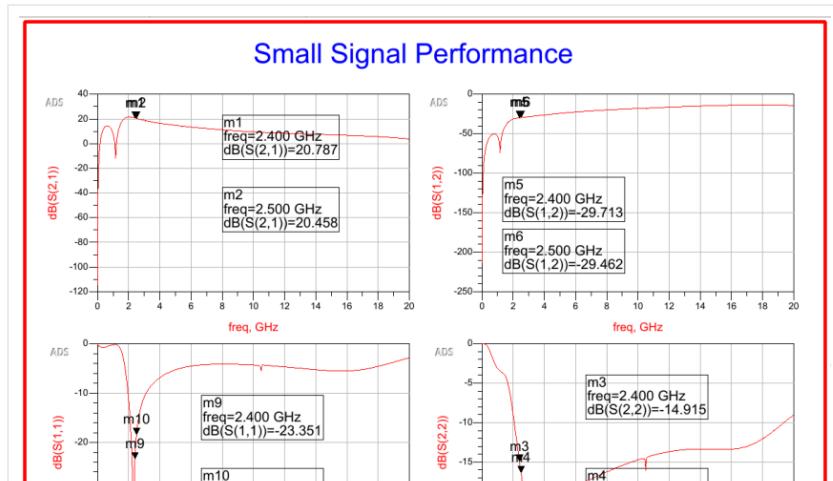


Figure 1.21: LNA Circuit

Let's move on to check our circuit simulation results. I create this data display server template. You can create a custom template like this and copy and paste it easily to recreate them, which saves a lot of time.

The s-parameter performance of the circuit simulation is shown in Figure 1.22. The LNA meets all the specifications, including gain and isolation and input and output return loss. The gain is more than 20dB which is excellent. The isolation is -29dB. The input return loss is less than -18dB, and the output return loss is less than -14.9 dB.



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This shows Noise Figure and DC simulation. The noise figure of 0.92dB to 0.95dB was obtained across 2.4GHz to 2.5GHz frequency range. The Collector

current ( $I_{ce}$ ) of 0.017mA is obtained, which is also the total current draw of the LNA. The base current ( $I_{be}$ ) is very small and negligible, but ADS allows you to plot this as well.

Figure 1.24 shows the small signal stability analysis.

Through the WS Probe, we have plotted the “Real Part of Driving Point Admittance” and “Bilateral (True Return Ratio) Loop Gain”. We also plotted  $\mu_{source}$  &  $\mu_{load}$ . The  $\mu_{source}$  &  $\mu_{load} > 1$  across 1kHz to 20GHz shows the LNA is unconditionally stable. Moreover, the “Real Part of Driving Point Admittance” is more than zero, and the “Bilateral (True Return Ratio) Loop Gain” is less than 0 validates the mentioned conclusion.

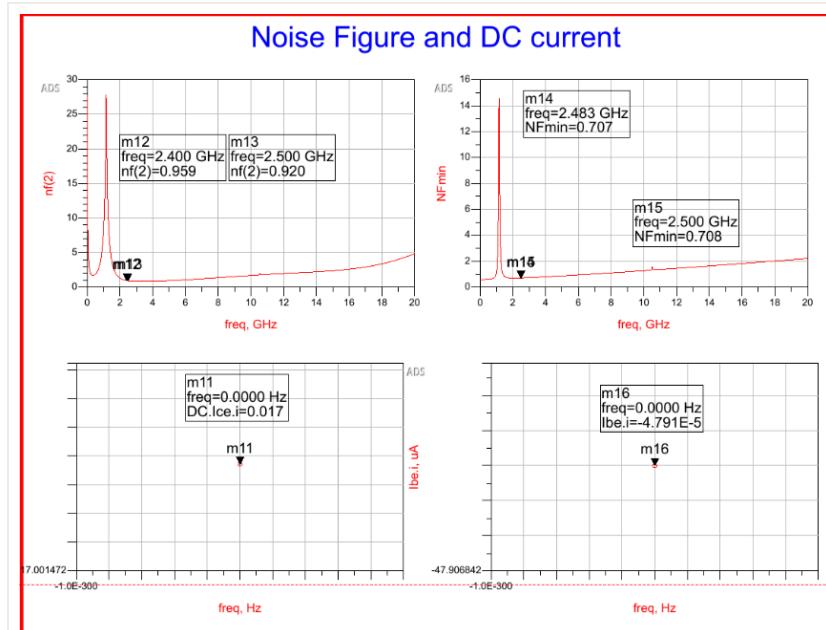


Figure 1.23: Noise Figure and DC simulation results



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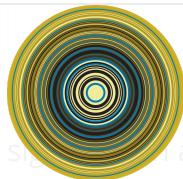


Figure 1.24: LNA small signal stability analysis

shows the LNA IP3 measurement setup. Two signals with an appropriate gap will be injected into our

DUT or LNA, and the output will be monitored by a spectrum analyzer. In our case, we are injecting 2.449GHz and 2.451GHz together, and the fundamental frequency is 2.45GHz and a gap of 1MHz. In the industry, sometimes this gap can be in kHz, depending upon the radio specification. The power level is -40dBm. The OIP3 can be calculated using this IP3out component in ADS. I have inserted two components because we have upper and lower-side OIP3 products.

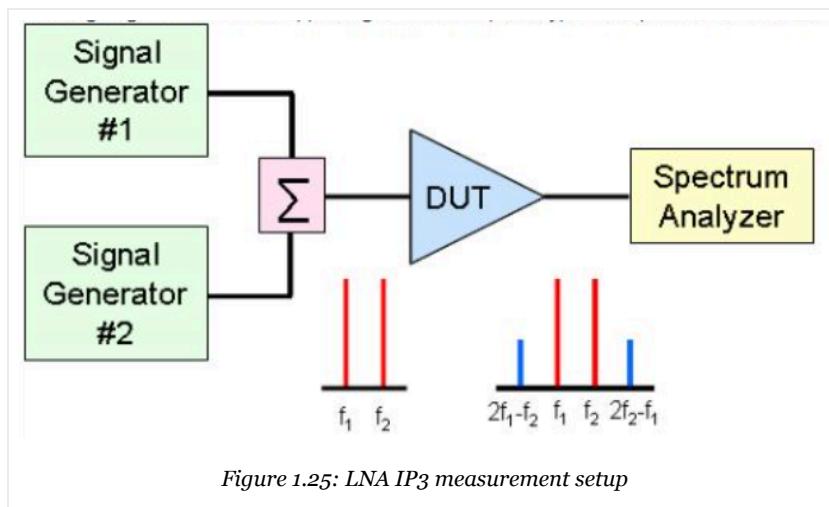


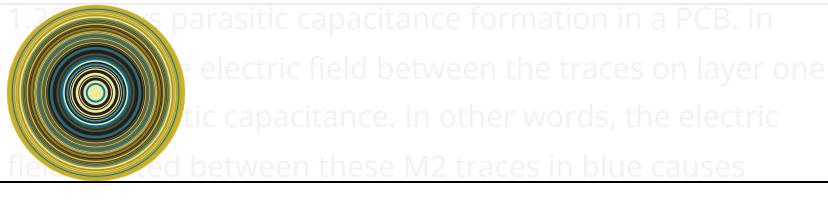
Figure 1.25: LNA IP3 measurement setup

We will do an IP3 simulation with the EM simulation model later.

For circuit simulation, we have met all the design goals set for the s-parameter, noise figure, and stability simulations.

## 1.7 Step 5: Layout Design

LNA layout must be carefully designed to minimize parasitic capacitance and parasitic inductance. The layout causes parasitic capacitance and parasitic inductance. As you already know, parasitic capacitance and inductance are



In case two, the electric field between a trace on layer one and metal on the neighboring layers forms parasitic capacitance. for example, the electric field formed between M2, M3, and M1 will also create parasitic capacitance.

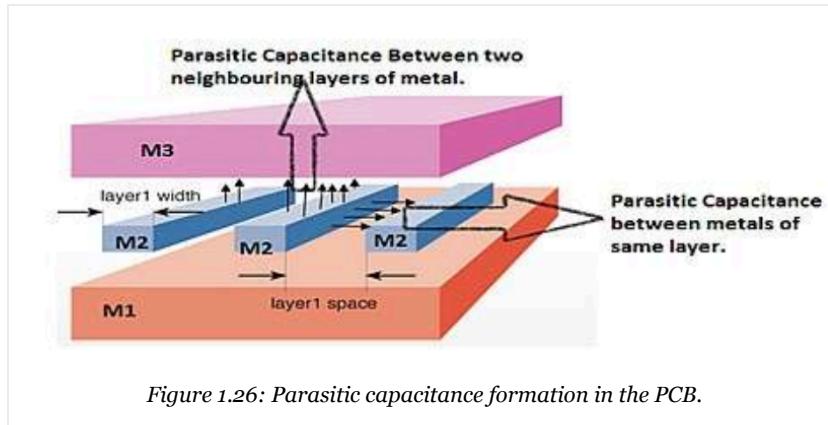
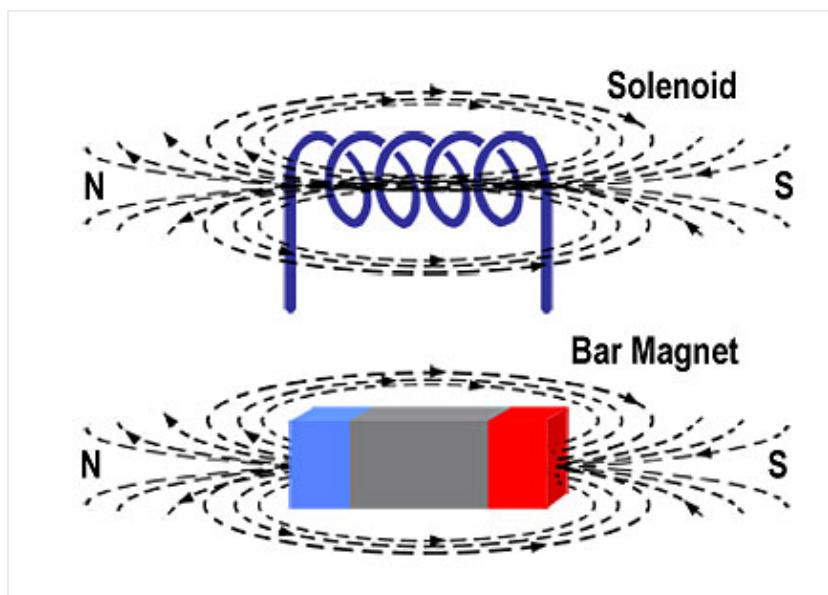


Figure 1.26: Parasitic capacitance formation in the PCB.

Now let's understand how parasitic inductance is formed. The magnetic field between two ends of a trace forms parasitic inductance, as shown in Figure 1.3. long traces will have huge parasitics inductance and wise versa.





RF engineers need to be aware of the parasitic capacitance and learn to minimize or control parasitics to avoid unwanted issues such as LNA low gain stability issues. Layout design needs to be done

carefully with complete awareness of parasitics. PCB layout is designed to minimize parasitic capacitance and parasitic inductance.

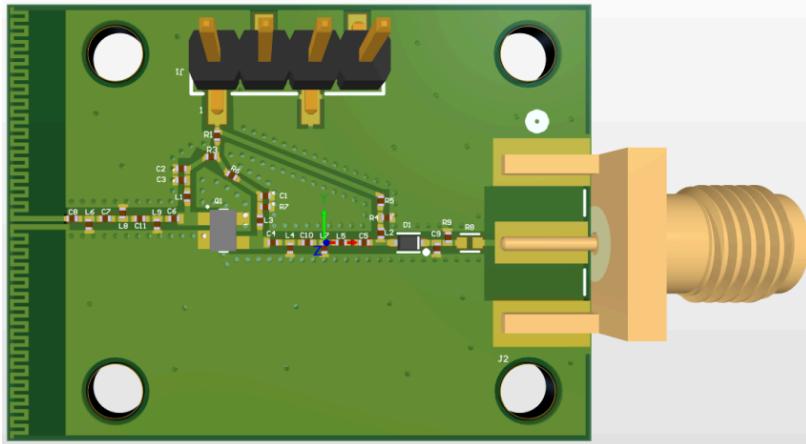


Figure 1.28: Parasitic inductance formation in the PCB.

## 1.8 Step 6: Layout Simulation

The sixth step is to do a layout simulation. Layout simulation needs to be done after designing the layout to ensure layout parasitics are not degrading the circuit performances such as gain, noise figure, stability, IP3, etc. Our youtube videos have a step-by-step guide on importing the layout into Keysight ADS in ODB++ format, setup the EM simulation, and Running it. Please check the videos on Innowave's youtube channel to learn more about the subjects mentioned above.

I have set the frequency range as 0 Hz to 10 GHz because of the stability simulation. Stability factors require simulation over a wide frequency band. The next frequency range is the ISM band low and high frequency, which is 2.4GHz and 2.5GHz, respectively. Finally, a single frequency is set at 2.45GHz. This is the center frequency of our band of



simulation. To do that, click "simulator" and select FEM.

The rest of the settings are standard.

This simulation is a large simulation and will take days on any

system. One can simplify the simulation complexity. To do that, click on "edit advanced simulator setup". Here, you can change generation to generation 2, mesh domain optimization to ON, and the refinement frequency to 2.5GHz, which is the high frequency of our band of interest. These setting changes reduce simulation time drastically. In my case, I'm willing to wait, so I didn't do that.

After doing all the setup, Run needs to be clicked to begin the RFPro simulation.

## 1.9 Step 7: EM-circuit co-simulation

Upon completing the EM simulation, the EM simulation model is created and placed onto the ADS schematic, so EM-Circuit Co-Simulation can be done by clicking "Results" à"Generate Sub Circuit mode."

As shown in Figure 1.29, we have built the circuit with our EM simulation model. I want to highlight that the same component values are used between the circuit and layout simulations except for the resistor R7. We have reduced the R7 value from 12.7 ohms to 6 ohms in order for the LNA to pass the gain specification. The same components value for both the circuit simulation and layout simulation is possible because we have minimized the parasitics.

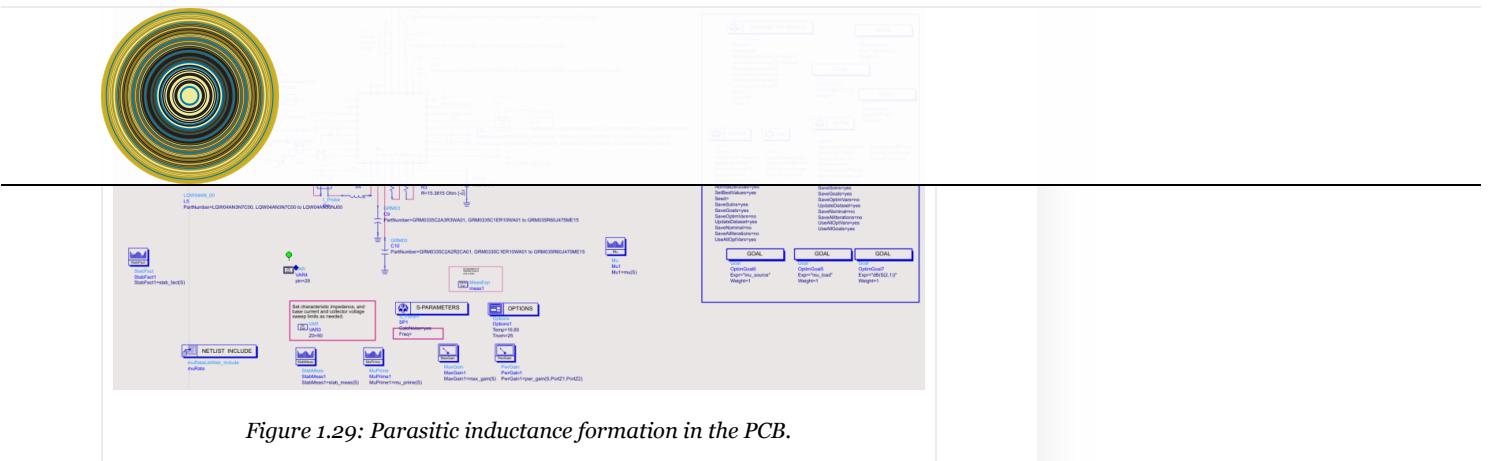
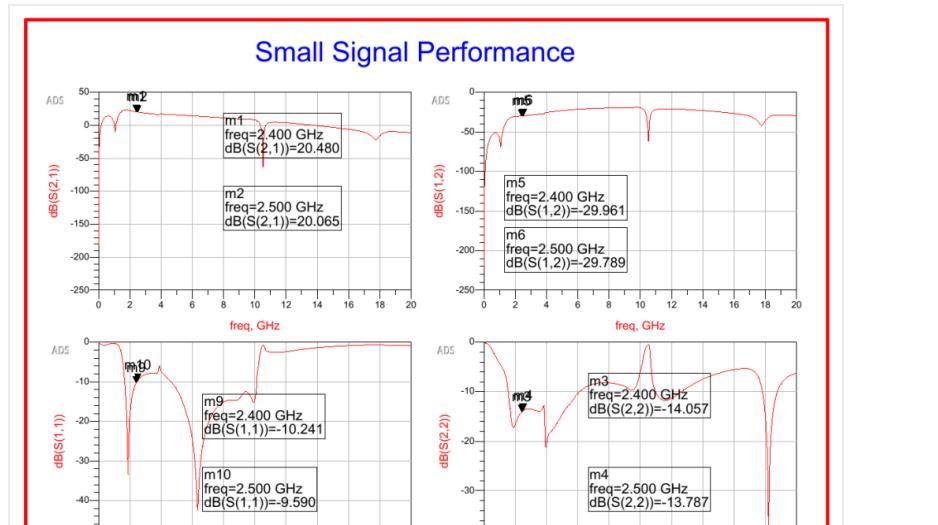


Figure 1.29: Parasitic inductance formation in the PCB.

## 1.10 Step 8: Results and Analysis

The s-parameter performance of the circuit simulation is shown in Figure 1.30. 20dB gain was obtained across the band of interest, 2.4GHz to 2.5GHz. Isolation of -29dB is achieved in the band of the LNA operation. Input return loss is less than -9.5dB, whereas output return loss is less than -13.7 dB.

In conclusion, the LNA meets gain and reverses isolation and output return loss specifications, but Input return loss. Input return loss is failing by 0.5dB. However, we can live with this because the most critical parameters, such as gain and isolation, meet the spec.



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This shows the Noise Figure and DC simulation. The noise figure of 0.78dB was obtained across the band. Collector current ( $I_{ce}$ ) of 0.017mA is obtained,

which is also the total current draw of the LNA.

Figure 1.32 shows the small signal stability analysis.

Through the WS Probe, we have plotted the “Real Part of Driving Point Admittance” and “Bilateral (True Return Ratio) Loop Gain.” We also plotted  $\mu_{source}$  &  $\mu_{load}$ . The  $\mu_{source}$  &  $\mu_{load} > 1$  shows the LNA is unconditionally stable.

Moreover, the “Real Part of Driving Point Admittance” is more than zero, and the “Bilateral (True Return Ratio) Loop Gain” is less than 0 validates the mentioned conclusion.

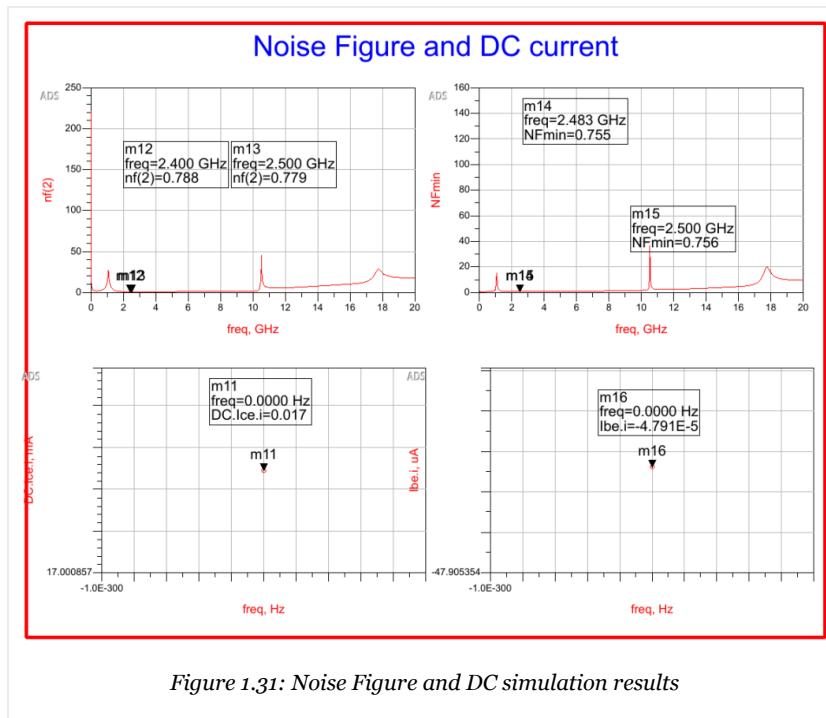
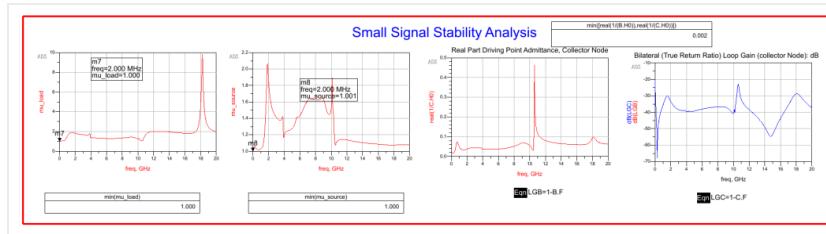
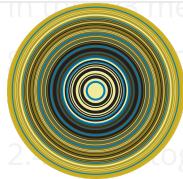


Figure 1.31: Noise Figure and DC simulation results





In this measurement, two signals with an appropriate frequency gap are injected into the LNA, and a spectrum analyzer measures the output. In our case, we inject 2.449GHz and 2.453GHz together. The fundamental frequency is 2.45GHz,

and the gap is 1MHz between the two mentioned signals. In the industry, sometimes this gap can be in kHz, depending upon the radio specification. The power level is -40dBm. The OIP3 can be calculated using this IP3out component in ADS. I have inserted two components because we have upper and lower-side OIP3 products.

The rest of the setup in the schematic is standard or similar compared to our previous schematic for the s-parameter and noise figure simulation. Figure 1.33 shows the OIP3 simulated values. OIP3 is more than 15dBm, which also meets our design specifications.

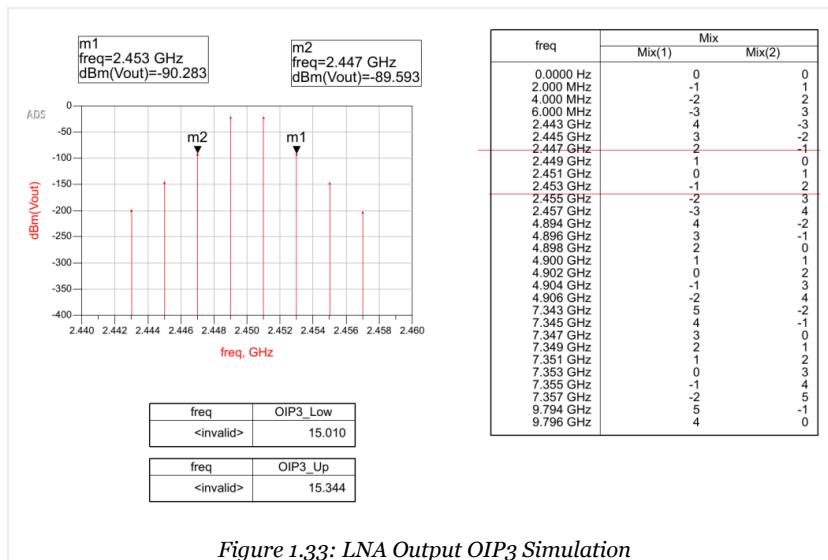


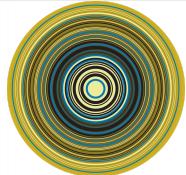
Figure 1.33: LNA Output OIP3 Simulation

Table 1.6: LNA Design Specification vs. Simulated Results

DESIGN PARAMETERS	DESIGN SPECIFICATION	SIMULATED RESULTS
Frequency range	2.4GHz – 2.5GHz	2.4GHz – 2.5GHz
Gain	> 20dB	> 20dB

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1,  
Real(1/C.H0) &  
Real(1/B.H0) > 0,  
Real(1/B.H0) > 0,

	$\text{dB}(\text{LGC}), \text{dB}(\text{LGB})$	$\text{dB}(\text{LGC}), \text{dB}(\text{LGB})$
	< 0	< 0
Input Return Loss (S11)	< -10dB	< -9.5dB to -10.2dB
Output Return Loss (S22)	< -10dB	< -13.7dB
Noise Figure	< 1dB	0.779dB to 0.788dB
OIP3	> 15 dBm	15 to 15.3

This table summarizes the LNA performance and compares it to the design specifications. LNA meets design goals for gain, stability, output return loss, noise figure, and OIP3. As mentioned earlier, input return loss is marginal, but we assume it should be fine.

The video links of the LNA design Tutorial is given below.

### Tutorial 12: Step-by-Step Guide to Designi...





Tutorial 13: Step-by-Step Guide to Designi...



Tutorial 14: Step-by-Step Guide to Designi...



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