LNA design for CDMA front end by Jarek Lucek Market Application Engineer and
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Abstract: This article will step the reader through a practical design of a front end 900 MHz and 1.9 GHz CDMA Low Noise Amplifier. The main emphasis will be put on Noise Figure, IP3, Gain and power dissipation trade offs.

The main topics of the article will include the following:

- Bias design
- Circuit stabilization
- Noise optimization
- Linearity optimization
- Load pull for gain and IP3 trade off improvement
- Complete circuit characterization

The LNA design will be carried out with a discrete, 5th generation silicon transistor from Philips Semiconductors. A circuit solution will be presented along with complete measured performance that is required by 900MHz and 1.9 GHz CDMA systems. Although the article will be based on LNA design with a specific transistor, this general LNA design method can be used for other transistors and applications.

Introduction:

LNA function in today's communication system provides first level of amplification of the signal received at the system's antenna. The smallest possible signal that can be received by the receiver defines the receiver's sensitivity. The largest signal that can be received by the receiver establishes an upper power level limit that can be handled by the system while preserving voice or data quality. The dynamic range of the receiver, which is the difference between the largest possible received signal and the smallest possible received signal, defines the quality of the receiver chain. The LNA function plays an undisputed importance in the receiver design. Its main function is to amplify extremely low signals without adding noise, thus preserving required signal to noise ratio of the system at extremely low power levels. Additionally, for large signal levels, the LNA amplifies the received signal without introducing any distortions, hence eliminating

channel interference. Proper LNA design is crucial in today's communication solutions. Due to complexity of the signals in today's digital communications, additional design considerations need to be addressed during a LNA design procedure.

Typical trade offs in LNA design:

A LNA design presents considerable challenge due to its simultaneous requirement for high gain, low noise figure, good input and output matching and unconditional stability at the lowest possible current draw from the amplifier. CDMA system adds to the challenge because of its high linearity or high IP3 (3rd order intercept point) requirement. While gain, noise figure, stability, linearity and input and output match are all equally important, they are interdependent and not always work in each others favor. Typically, the CDMA LNA has the following requirements:

- Low supply voltage, Vce=2Volts
- Low current consumption, Ic≤10mA
- High gain≥15dB
- High Input IP3≥5dBm
- Low Noise Figure≤2dB
- Unconditionally stable
- Input Return Loss≥10dB
- High Isolation
- Small dimension/low part count
- Low cost

Most of the conditions listed above can be met with a careful selection of a transistor and good understanding of parameter tradeoffs. Low noise figure and good input match is almost never simultaneously obtained without using novel feedback arrangments[1]. Unconditional stability will always require a certain gain reduction due to either shunt or series resistive loading of the collector. High IP3 requires higher current draw, while lowest possible noise figure is usually achieved at lower current levels. Envelope termination technique can be used in order to improve IP3 performance while operating LNA at low current levels. Additional improvement of IP3 can also be achieved by means of proper power output matching (P1dB match). The P1dB match, being different from conjugate gain match, reduces the gain while improving IP3 performance.

Transistor selections:

Transistor selection is the first and most important step in a LNA design. The designer should carefully review the transistor selection keeping the most important LNA design tradeoffs in mind. The transistor should exhibit high gain, low noise figure, high IP3 performance at the lowest possible current consumption, while preserving relatively easy matching at frequency of operation. Philips Semiconductors' 5th generation BFG425W has been chosen for CDMA LNA application because it delivers high RF performance at low supply voltages (below 3Volts) and low collector currents (below 10mA). Its f_T

exceeds 20GHz and its low feedback capacitance ensures high isolations. BFG425W is also easy to match while maintaining a good noise behavior.

Examination of a datasheet is a good starting point in a transistor evaluation for LNA design. The transistor's S-parameters should be published at different collector/emitter voltages and different current levels for frequencies ranging from low to high values. The data sheet should also contain noise parameters, which are essential for low noise design. Spice models for the transistor and its package are also useful for IP3 and P1dB simulations.

The designer should first look at three main design parameters: noise, gain, IP3 and decide what Vce and Ic levels will produce the most optimal performance. A closer examination of NF vs. collector current shown in Figure 1, indicates that the minimum noise figure can be achieved at around 4 mA at both 900MHz and 1.9 GHz.

(1) $V_{CE} = 2$ V; f = 2 GHz.
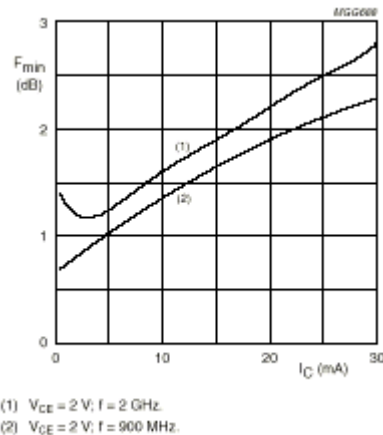(2) $V_{CE} = 2$ V; f = 900 MHz.

Figure1.   BFG425W minimum noise figure as a function of the collector current

Gain available from the transistor vs. collector current is shown in Figure 2 and reveals another important aspect in LNA design: the forward transducer power gain of 18dB remains constant at 1.9 GHz for current levels above 10mA (24dB for 900MHz). Small gain degradation is expected at low current operation, below 10mA.

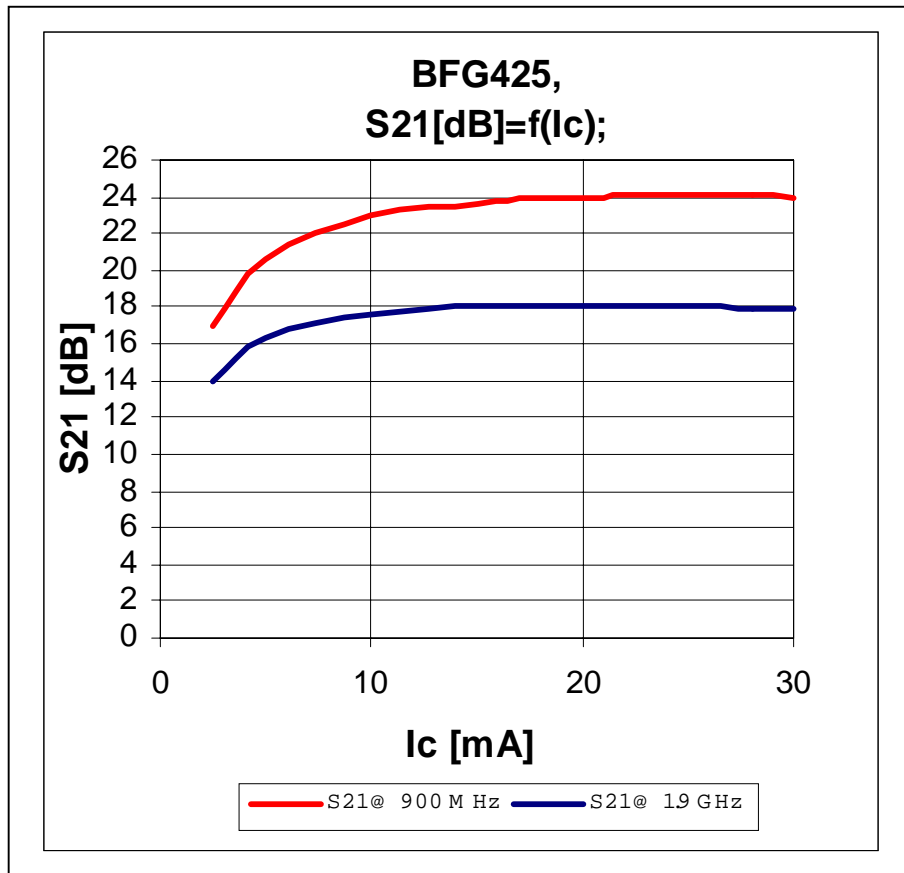**BFG425,**
S21[dB]=f(Ic);

Figure 2.   Forward transducer power gain of BFG425W

The forward transducer power gain represents the gain from the transistor itself with its input and output presented with 50Ω impedance. The $|S_{21}|$ values are provided by the manufacturer of the transistor at multiple frequencies and different Vce and current levels. Additional gain can be obtained from source and load matching circuits[2,3,4]. Maximum stable gain (MSG) and Maximum power gain (Gmax) are good indicators of additional obtainable gain from the LNA circuit.

LNA linearity is another important CDMA LNA parameter. A figure of merit for linearity is Third Order Intercept Point, IP3. A two tone test is used for derivation of IP3[5]. As a rule of thumb for BJT transistors, the output-IP3 can be estimated from the following formula:

$$OIP3 = 10*\log(Vce*Ic*5) \quad [dBm]$$

where Vce is in volts and Ic is in mA.

The graph of OIP3 vs. collector current can be derived. Figure 3 shows the result.
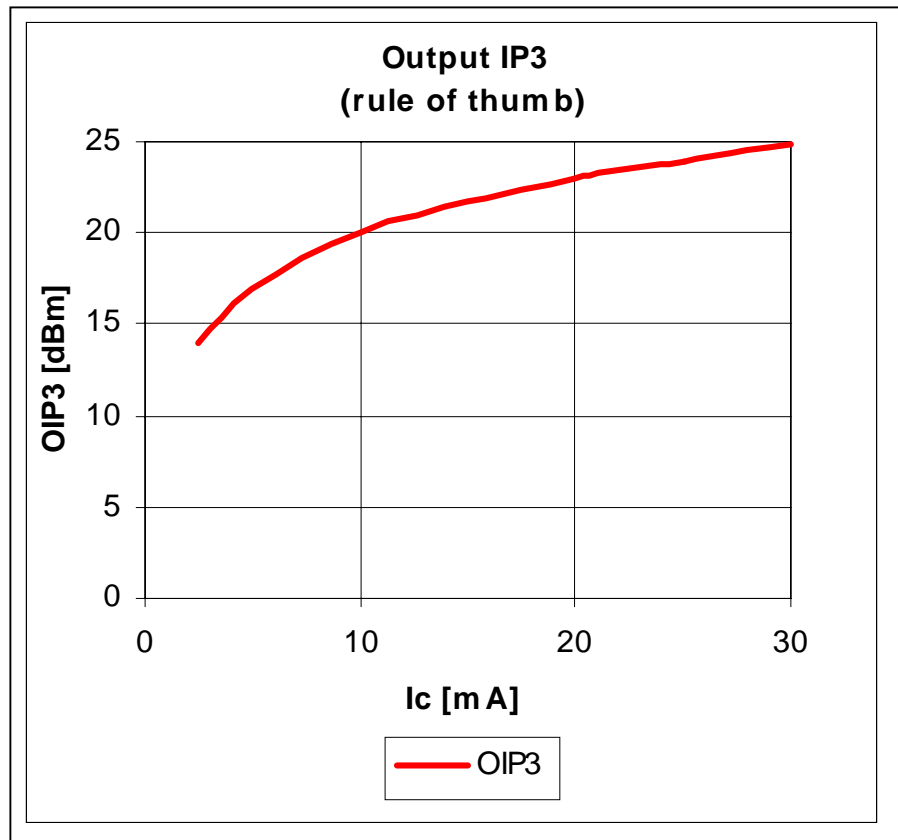
Figure 3. OIP3 vs collector current BFG425W

The relation between Input IP3 (IIP3) and the Output IP3 (OIP3) is defined as:

$$IIP3 = OIP3 - Gain \ \text{[dBm]}$$

Using 15 dB for our target gain and by examining the graph of Figure 3, one can determine that BFG425W will need to be operated at at least 10mA in order to produce 5 dBm of IIP3 without any margins. Additional IIP3 enhancement techniques will be needed in order to produce IIP3 of at least 5dBm at 10mA of collector current.

Vce=2V and Ic of 10mA is the point where BFG425W will produce an acceptable gain of at least 15dB with a Noise Figure below 2dB at both 900MHz and 1.9 GHz. IIP3 will also be above 5dBm with a collector current level of 10mA.

LNA Design.

I.   DC biasing.

DC biasing represents the first step in LNA design. The chosen DC bias circuit should exhibit stable thermal performance and reduce the influence of h_{FE} spread. It also should be a cost effective and simple solution, one that does not increase complexity of the design and preserves smallest possible size for the overall LNA. Resistive feedback arrangement shown in Figure 4 is the simplest form of DC biasing that fulfills all the major requirements.
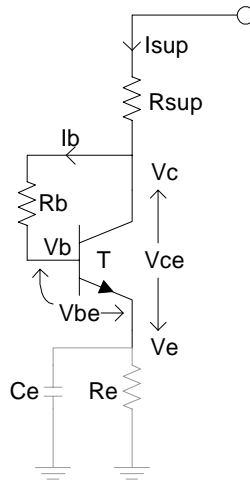

Figure 4. Typical LNA biasing circuit.

Two bias feedback arrangements are possible. One with a combination of Rsup and Rb and second one with a simple Re and Ce combination. The operation of the Rsup and Rb is as follows: Rsup and Rb will establish a biasing point. Since the operation of the LNA is going to be class A (constant current draw for dynamic range of power levels), we want to have a stable biasing point (for BFG425W at 10mA) over different temperatures and for different lot codes of transistors, where a small variation in h_{fe} can be expected. Vc in terms of Vsup and Isup can be expressed as follows:

$$Vc = V\text{sup} - I\text{sup} * R\text{sup}$$

As Isup decreases, which could be the case with a part with lower h_{fe}, Vc will increase at the same time. With an increase of Vc, higher Ib will result. With higher Ib, increase in Ic (~Isup) will take place up to a stable level set by Rsup and Rb. The same circuit handles thermal variations well. With a temperature increase, Isup will increase, which

will lower Vc. Lower Vc will result in lower Ib and lower Ib will lower Ic (~Isup). This circuit is inexpensive, simple and takes very little real-estate, while its performance is well behaved and understood. In order for Rb to have very little influence on source matching, which is crucial for noise performance, the feedback network should be decoupled with an inductor (making biasing invisible at RF band of operation).

Another possible bias feedback can be realized with emitter resistor and capacitor, shown in shaded colors in Figure 4. With Isup (~Ie) decreasing, Ve will decrease. Vbe will increase with a decrease in Ve. With increase in Vbe, Isup will increase, while keeping a stable biasing point. Ce should be selected carefully, since Re will also have a direct effect on RF gain of LNA. Ce should present a short at frequency of operation in order to limit its influence on gain and noise performance of the circuit.

Other biasing methods are suitable for class A networks. These are usually closed feedback arrangements with dynamic bias control provided by active components[6]. Although suitable for LNA application, these active feedback bias networks increase complexity of the LNA network, introduce additional components and increase the real-estate area of the solution.

II.   Stability design

Stability analysis should be the next step in LNA design. Unconditional stability of the circuit is the goal of the LNA designer. Unconditional stability means that with any load presented to the input or output of the device, the circuit will not become unstable – will not oscillate. Instabilities are primarily caused by three phenomena: internal feedback of the transistor, external feedback around the transistor caused by external circuit, or excess of gain at frequencies outside of the band of operation. S-parameters provided by the manufacturer of the transistor will aid in stability analysis of the LNA circuit. Two main methods exist in S-parameter stability analysis: numerical and graphical. Numerical analysis consists of calculating a term called Rollett Stability Factor K[2,3,4]. An intermitted quantity called delta (Δ) should be calculated first in order to simplify the final equation for the K-factor.

$$\Delta = S_{11} * S_{22} - S_{21} * S_{12}$$

then

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 * |S_{21}| * |S_{12}|}$$

When the K factor is greater than unity, the circuit will be unconditionally stable for any combination of source and load impedance. When K is less than unity, the circuit is potentially unstable and oscillation may occur with a certain combination of source and/or load impedance presented to the transistor. The K factor represents a quick check for stability at given frequency and given bias condition. A sweep of the K-factor over frequency for a given biasing point should be performed in order to assure unconditional

stability outside of the band of operation. Figure 5 shows two stability factor curves: for the transistor itself and for the complete LNA circuit. The designer's goal is to design a LNA circuit that is unconditionally stable for the complete range of frequencies where the device has a substantial gain.

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K factor
  2.0 ┌─────────────────────┐
      │                     │
      │              ╱╲     │── output resistor
      │         ____╱  ╲    │
      │       ╱         ╲   │
      │      ╱     ___    │  │
      │     ╱   ╱╱   ╲╲   │  │
      │    ╱  ╱        ╲  ╲ │
      │   ╱ ╱           ╲ │ │── bare device
      │  ╱╱              ╲  │
      │ ╱                │  │
      │▫                 │  │
  0.0 │                  │  │
      └─────────────────────┘
    200.0 MHz    freq   6.0 GHz
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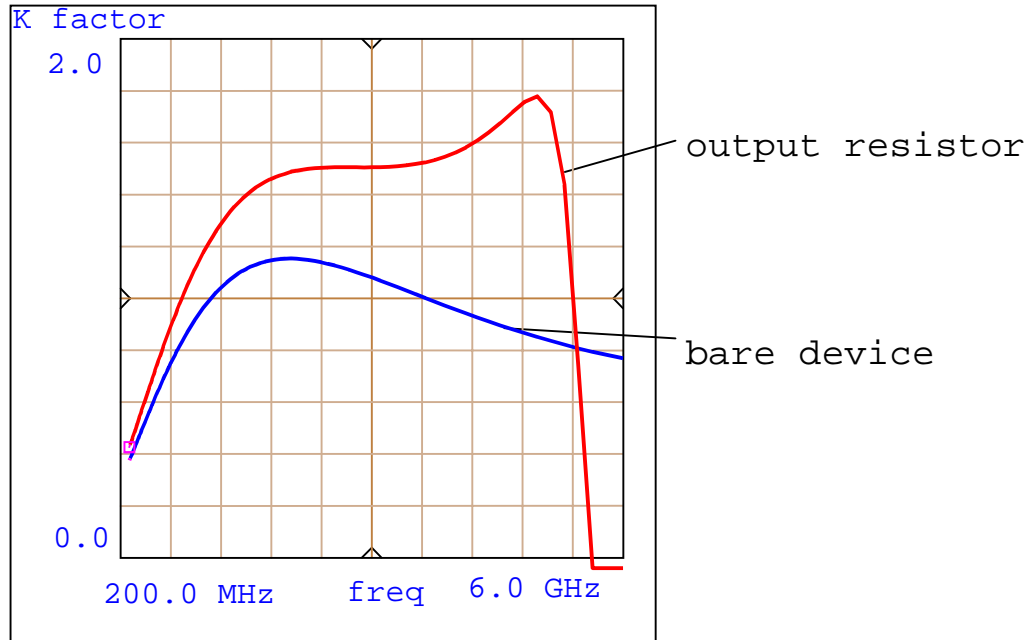
Figure 5. Stability Factor over Frequency

LNA designer can use at least five methods for circuit stabilization. The first one consists of resistive loading of the input. This method, although capable of improving the stability of the circuit, also degrades the noise of the LNA and is almost never used. Output resistive loading is a preferred method of circuit stabilization. This method should be carefully used because its effects are lower gain and lower P1dB point (thus lower IP3 point). The third method uses collector to base R-L-C (resistor-inductor-capacitor) feedback in order to lower the gain at the lower frequencies and hence improve the stability of the circuit. The forth method consist of filter matching, usually used at the output of the transistor, in order to decrease the gain at a specific narrow bandwidth frequency. This method is usually used for eliminating gain at high frequencies, much above the band of operation. Short circuit quarter wave lines design for problematic frequencies, or simple capacitors with the same resonant frequency as the frequency of oscillation (or excessive gain) can be employed to stabilize the circuit. The final stabilization method can be realized with a simple emitter feedback inductor. A small emitter inductor can make the circuit more stable at higher frequencies.

III.   Noise matching.

The next step in LNA design consists of noise and input return loss (IRL defines how well the circuit is matched to 50 Ω) matching of the source. A typical approach in LNA

design is to design an input matching circuit that terminates the transistor with a Γopt, which represents the terminating impedance of the transistor for the best noise match. In many cases this means that the input return loss of LNA will be sacrificed. The optimal IRL can be achieved only when the input matching network terminates the device with a conjugate of S11, which in many cases is different from conjugate of Γopt. An emitter inductor feedback can rotate S11 closer to Γopt, which can help with obtaining close to minimum noise figure and respectable IRL simultaneously. This additional inductance at the emitter of the transistor will also reduce the overall available gain of the network and can be used in balancing trade offs between the gain, IIP3 and stability in LNA design. A typical method used in designing input matching network is to display noise circles and gain/loss circles of the input network on the same smith chart. This provides a visual tool in establishing an input matching network for the best IRL and noise trade off. This method is widely used and it is also well published[7].

A slightly different design approach will be followed in our CDMA LNA example due to a special case described below. Figure 6 shows noise figure circles for BFG425W at 2V, 10mA and 1.9 GHz. The input match is exclusively used for obtaining optimal noise performance of the LNA while preserving good IRL. A closer examination of Figure 6 reveals that Γopt coincides with the 50 Ω point. This means that almost no matching is required with the input network of the transistor (simple 50 Ω line along with the self resonating at frequency of operation coupling capacitor will be sufficient) in order to obtain minimum specified noise figure at the given frequency of operation and given operating point. For the 900 MHz circuit, a small emitter inductance will be used in order to bring S11 point and Γopt point closer together, thus preserving respectable IRL. This inductance will be achieved with small strip lines connected directly to the emitters of the transistor.
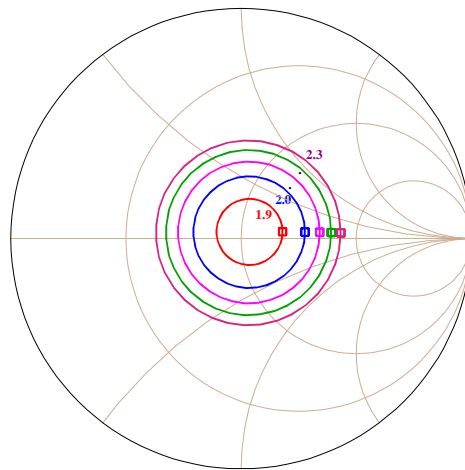

Figure 6. BFG425W 1.9 GHz, 2V, 10mA Noise Circles

IV. Loadpull matching.

The last step in LNA design involves output matching of the transistor. Traditionally, this step used to be relatively simple. An additional resistor, in either series or parallel,

has been placed on the collector of the transistor for circuit stabilization. Conjugate matching has been exclusively used for narrow band LNA design in order to maximize the gain out of the circuit. With additional IP3 requirement forced on the LNA, the trade off between IP3 and gain has to be considered. Linearity matching is widely known by high power amplifier designers, especially those who deal with linear systems, but is relatively unknown for a small signal designer. The so-called load-pulling is used in order to establish IP3 and gain impedance contours. The load-pulling can be realized by using nonlinear Spice model of the transistor with simulation software like HP's MDS. Harmonic balance can be used for establishing two tone environment. The load-pulling method sweeps impedance of the whole Smith chart and plots contours of constant gain and IP3 numbers. Figure 7. Shows gain contours for BFG425W at 1.9 GHz and Figure 8 shows IIP3 contours. The optimal gain impedance point does not match the optimal IIP3 point, which means that the design will have to be realized by means of a trade off. Typically, the designer should design the LNA circuit at the point where the gain does not degrade as much and the IP3 is still respectable. If one were to draw a line between the two optimal gain and IIP3 impedance points, every point on that straight line will represent a good area of trade off, with the ends representing the two optimal points.
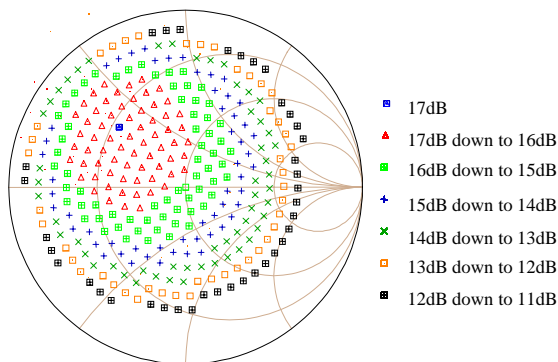

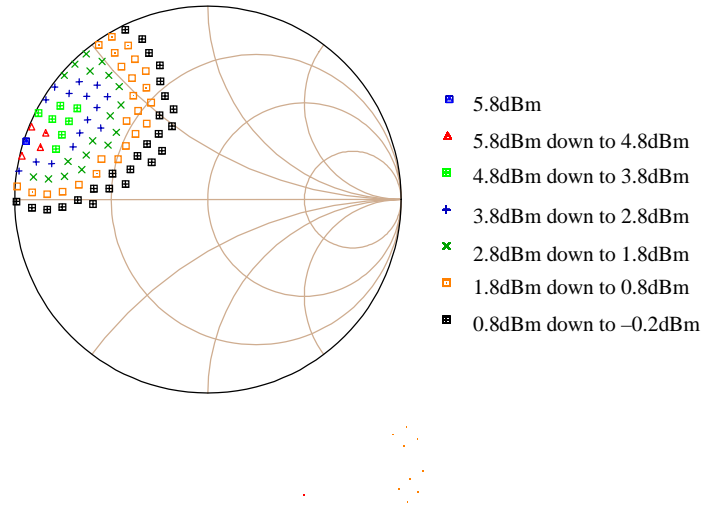|	
⊡	17dB
▲	17dB down to 16dB
▪	16dB down to 15dB
+	15dB down to 14dB
✕	14dB down to 13dB
▫	13dB down to 12dB
▦	12dB down to 11dB

Figure 7. Gain contours for 1.9 GHz LNA

Figure 8. IIP3 contours for 1.9 GHz LNA

The rule of thumb for P1dB and IP3 is shown blow:

$$IP3 = P_{1dB} + 10 \text{ in dBm}$$

This means that by knowing the P1dB point one can estimate the IP3 levels. The 10 dB rule can further be improved with appropriate bypassing of the base and collector[8]. As previously indicated, the third order intercept point is established by injecting two equal in magnitude signals with small frequency offset into an active circuit. As the active circuit approaches non-linear region, close to P1dB, the two carries will generate distortion products, both in and out of band, see figure 9.

Figure 9. Two tones with in and out of band distortions

The low frequency products, f2-f1, can modulate the base emitter and collector emitter LNA supply voltages. For improved linearity the fluctuation of the base and collector voltages should be eliminated by means of proper by-passing, hence presenting the base and the collector with very low impedance at so called video frequencies (between DC and usually up to 40 MHz depending on the bandwidth of the signal that is being presented to the LNA). In the case of CDMA system, the video bandwidth should extend well beyond 1.25 MHz or at least 5 MHz. The designer should exhibit caution during by-

passing design. A poor selection of the by-pass capacitors could also degrade IP3 performance as shown in Figure 10.
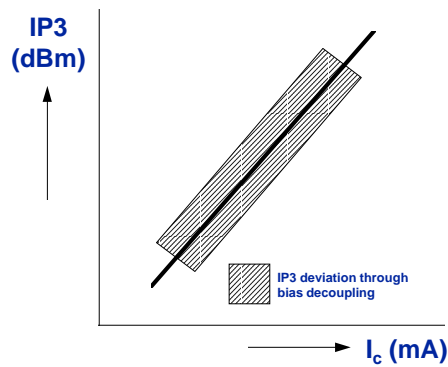

Figure 10. IP3 deviation through by-pass enhancement.

Figure 11. shows 1.9 GHz LNA with BFG425W. Capacitor C2 and C5 will resonate at frequency of operation. C3 and C4 combination will work at video frequencies, thus making sure that both collector and base bias are not modulated with the distortion signals. As a rule of thumb, the impedance of by-passing circuit should be lower than 25% of the input impedance of the transistor at particular frequency spacing. In the case of BFG425W the following is valid:
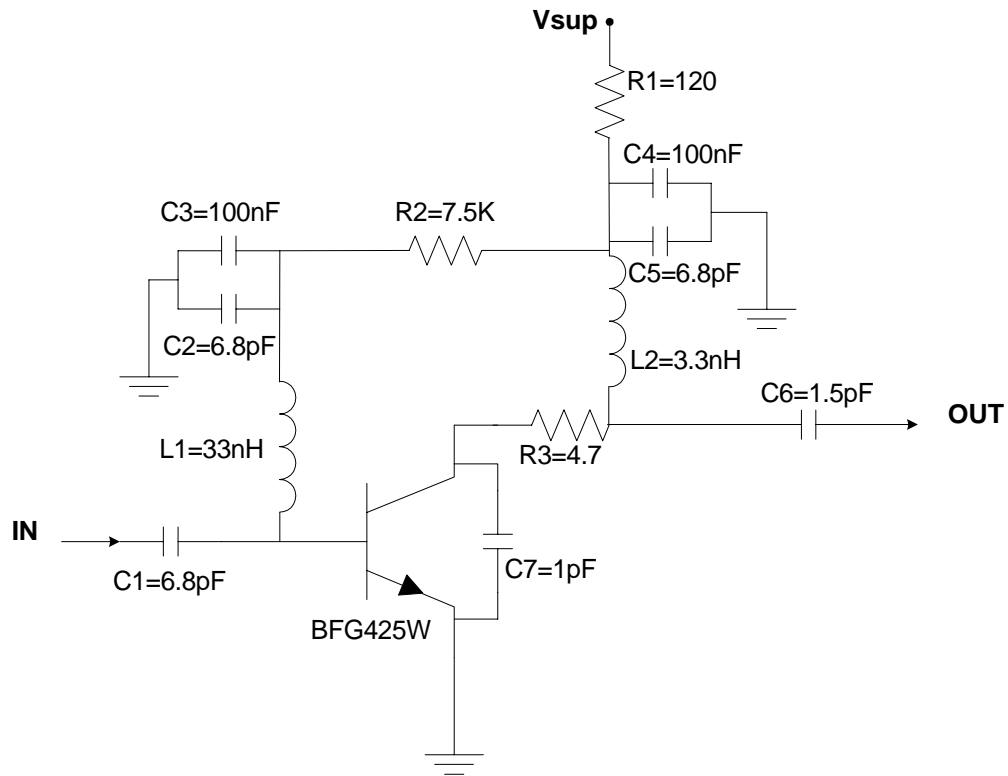
Figure 11. 1.9 GHz LNA with BFG425W

The impedance of the BFG425W transistor is:

$$Zin(5MHz) \approx \frac{h_{fe}}{g_m} = \frac{h_{fe}}{Ic/V_T} = \frac{70}{10/25} = 175\,\Omega$$

Cd should be 25% less than 175 Ω: Cd<0.25 * 175 Ω ≈ 44 Ω

At 5MHz spacing, the Cd should be at least:

$$Cd \geq \frac{1}{2*\Pi*f*44} \geq \frac{1}{2*3.14*5E6*44} \geq 1\,nF$$

While preserving the gain performance of the LNA, the by-passing method, also known as an envelope termination technique, can improve LNA's IIP3 performance without increasing current consumption. Figure 12 shows IIP3 contours after implementation of video frequency decoupling. Comparison of Figure 12 and Figure 8 reveals substantial improvement in IIP3 trade off. Since the gain contours for IIP3 improved circuit will remain the same, the main improvement in IIP3 performance is achieved by extending the available IIP3 impedance points closer to the optimal gain impedance levels.
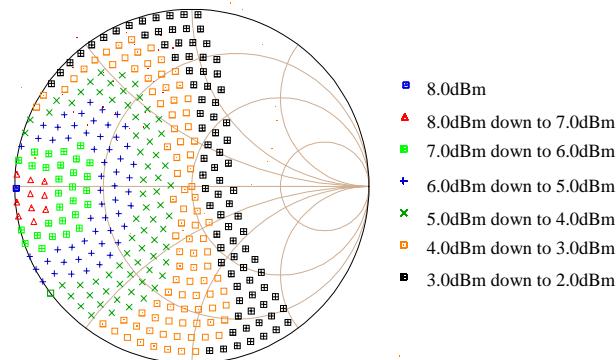

▣	8.0dBm
▲	8.0dBm down to 7.0dBm
▣	7.0dBm down to 6.0dBm
+	6.0dBm down to 5.0dBm
✕	5.0dBm down to 4.0dBm
▫	4.0dBm down to 3.0dBm
▣	3.0dBm down to 2.0dBm

Figure 12. IIP3 contours for decoupling corrected LNA circuit, 1.9 GHz LNA.

LNA circuit realization.

Figure 11 shows 1.9 GHz high IP3 CDMA LNA circuit with BFG425W and figure 13 demonstrates a typical 900 MHz LNA.
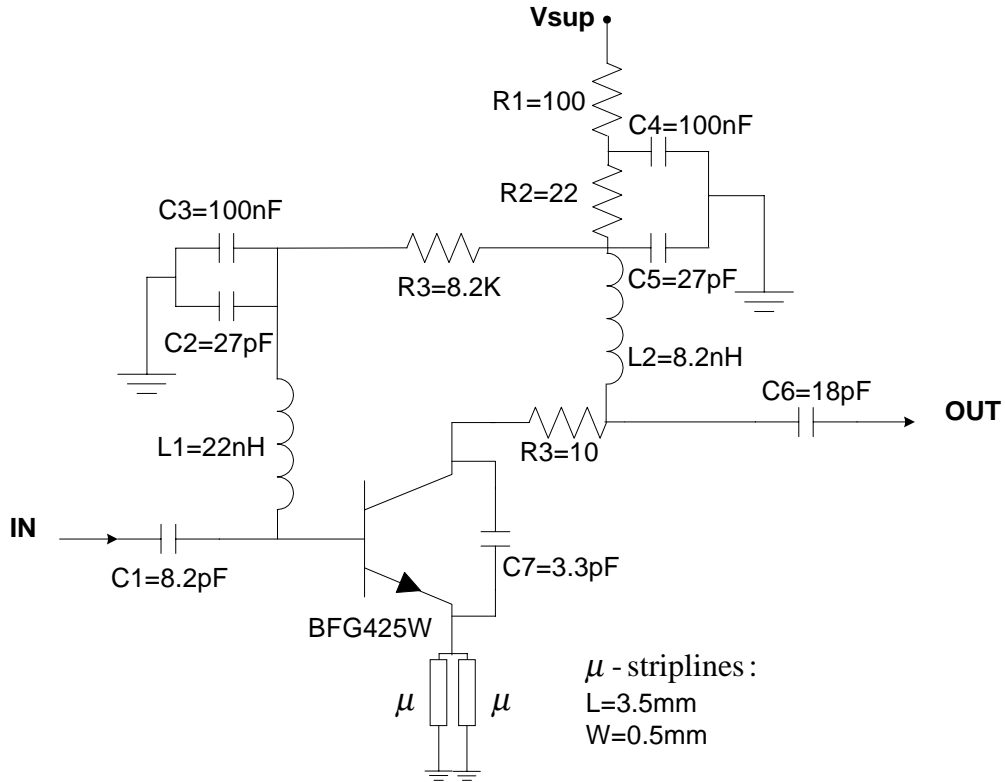
Figure 13. 900 MHz LNA circuit with BFG425W

Both circuits were realized with design methods described in this article.

Table 1 summarizes the measured performance of 1.9 GHz LNA circuit. Table 2
summarizes the performance of 900 MHz version of LNA.

Parameters	Units	Measured performance with IIP3 by-pass improvement	Measured Performance without IIP3 by-pass improvement
Vsuply	Volts	3.3	3.3
Vce	Volts	2	2
Ic	mA	10.3	10.3
Gain	dB	16.8	16.8
NF	dB	1.9	1.9
IIP3	dBm	+5 (at 1.25MHz spacing)	-2.5 (at 1.25MHz spacing)
IRL	dB	13	14
ORL	dB	11	10
Isolation	dB	27	27

Table1. 1.9 GHz LNA performance

Parameters	Units	Measured performance with IIP3 by-pass improvement	Measured Performance without IIP3 by-pass improvement
Vsuply	Volts	3.3	3.3

Vce	Volts	2	2
Ic	mA	10	10
Gain	dB	16.9	17
NF	dB	1.8	1.85
IIP3	dBm	+5 (at 1.25MHz spacing)	-4 (at 1.25MHz spacing)
IRL	dB	7	7
ORL	dB	11	11
Isolation	dB	28.5	28.5

Table2. 900MHz LNA performance

Acknowledgment:

[1] . S. Mercer, "An introduction to low-noise amplifier design," RF *Design,* July1998, pp. 44-56.

[2] . S. Liao, *Microwave Circuit Analysis and Amplifier Design,* Prentice-Hall, 1988, pp. 123-160.

[3] . G. Gonzalez, *Microwave Transistor Amplifiers,* Prentice-Hall, 1984, pp. 139-193

[4] . N. Dye, H. Granberg, *Radio Frequency Transistors Principles and Practical Applications,* Butterworth-Heinemann, 1993, pp. 204-231.

[5] . N. Dye, H. Granberg, *Radio Frequency Transistors Principles and Practical Applications,* Butterworth-Heinemann, 1993, pp. 18-23.

[6] . N. Dixit, "Design and Performance of a Low Voltage, Low Noise 900 MHz Amplifier", *RF Design,* March 1994.

[7] . S. Liao, *Microwave Circuit Analysis and Amplifier Design,* Prentice-Hall, 1988, pp. 145-149.

[8] . K. Vennema, "Ultra Low Noise Amplifiers for 900 and 2000 MHz with High IP3", Philips Semiconductors 1998 SC14 Wideband transistors databook.