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Current Mode Control

Detailed Implementation & Control Loop Design

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Material to Cover in this Section

- Problems with standard voltage mode control and how to improve them
- Peak current mode control
  - Subharmonic oscillation & slope compensation
  - Leading edge blanking
  - Current gain and current measurement
  - Right-hand plane zero and its impact on phase margin
  - Peak current mode control loop design
  - Loop design with transconductance amplifiers
- Labs

Fixed Frequency Power Supply Control Methods Recap

- Standard Voltage Mode (Vmode)
  - Buck/Forward topologies
  - Fixed Frequency - one control loop
  - Measure Vout and compare with Vref and then compensate to get new value of PWM
- Voltage Mode with *Input* Voltage Feedforward (Vmode+VFF)
  - Buck/Forward topologies
  - Measure input voltage and incorporate it in the control loop
  - Gives better line regulation
- Current Mode → Boost/Flyback/SEPIC/Cuk…. and Buck
  - Fixed Frequency + two control loops
    - Outer loop controls the voltage and the inner loop controls peak (most commonly) inductor current
  - Has advantages over Voltage mode
  - Also has headaches such as sub-harmonic oscillations, needs ramp compensation

There are 2 main sub-categories:

1 - Peak Current Mode Control for DC/DC PSUs
&
2 - Average Current Mode Control for PFCs

Today we will cover Peak CMC
We will cover Average CMC during the PFC day

So What Was Wrong with Voltage Mode?

- There are several issues but here are the main ones:
  - 1 - Although our control loop knows exactly what is happening on the output, it doesn't "directly" know what is happening on the input
    - i.e. standard voltage mode is very slow to react to changes Vin → it has poor line regulation
  - 2 - Please recall that PWM gain of $\frac{V_{in}}{V_{RAMP}}$ appears in the transfer function of the standard Vmode PSU

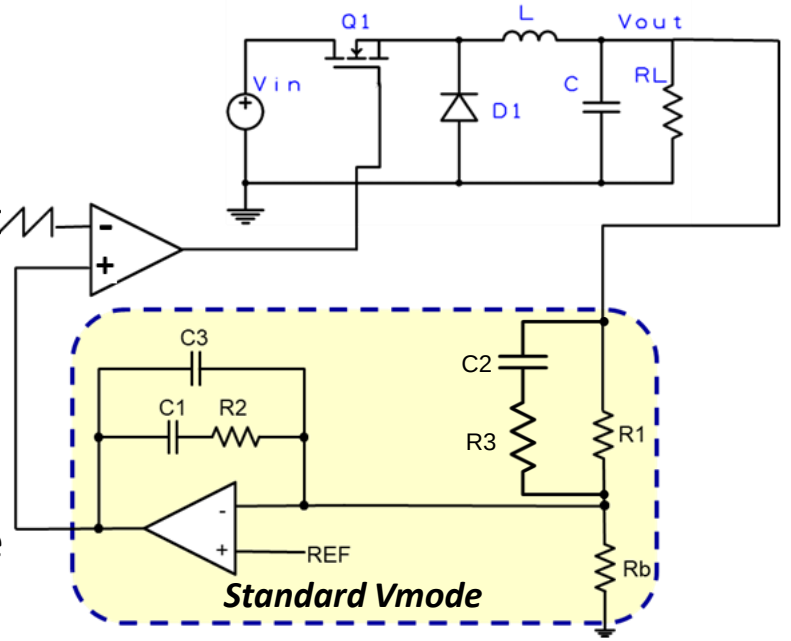
Standard Vmode

We talked about these yesterday and solved them with Vmode+VFF…

but there are other issues that Vmode+VFF cannot solve

So What More Is Wrong with Voltage Mode?

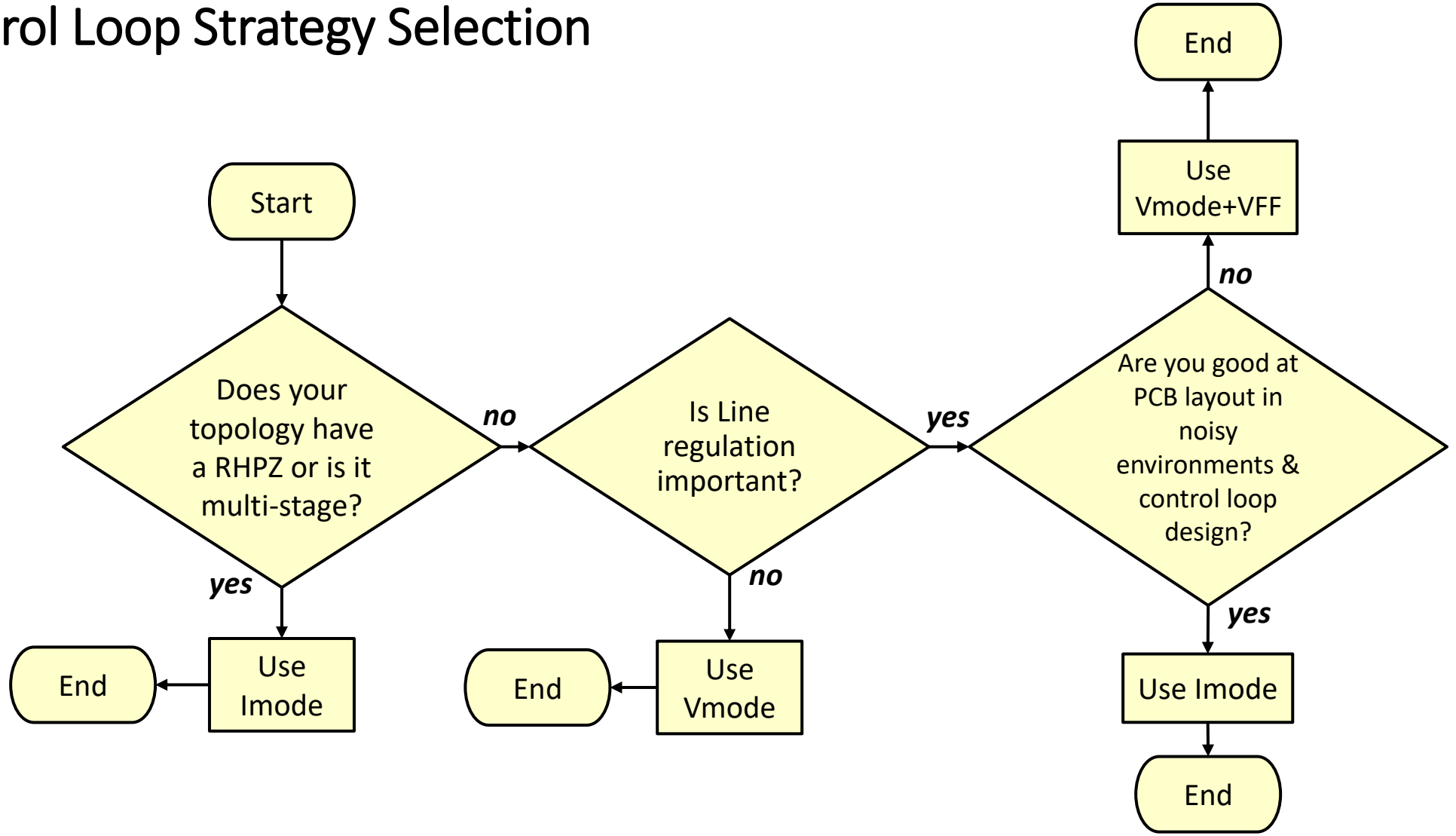
- 3 - We are not measuring the current → no information about current means no current limiting
  - If we have to measure the current anyway for safety, why not use it in the control loop?
  - Note that current measurement for safety is much simpler than current measurement for control loop stability and often is done internally in the PWM controller → so this is not a big deal
- 4 - Can not use Vmode with any topology that has a Right Hand Plane Zero (RHPZ)
  - We will talk about RHPZ soon
- 5 - Can't current share in multi-stage/interleaved PSUs with Vmode
  - In Vmode there will be conflict between the control loop of each stage as to which one controls Vout
  - If we have one global loop for Vout and a local current loop per stage we solve this problem



How Do We Solve the Problems with Standard Vmode?

- To solve problems 1 & 2 we clearly need to take a measure of our input and somehow incorporate it in our control loop
- Engineers invented 2 methods to do this:
  - Voltage Mode with Input Voltage Feedforward (Vmode+VFF)
    - Measures Vin and incorporates into the control loop
  - Current Mode Control (Imode)
    - Measures the inductor current and incorporates into the control loop
    - Peak current mode → DC/DC PSUs
    - Average current mode → PFCs
- As we yesterday Vmode+VFF solves the first 2 problems
  - You still can not use it for topologies with a RHPZ
  - You still can not current share in multi-stage converters
  - You still have a current limiting issue → easy to solve
- Current mode solves all of the 5 issues identified in the previous slides
  - But, as with anything else in engineering, it has its drawbacks
    - In particular, clean current measurement, subharmonic oscillations and slope compensation is a real pain!

Control Loop Strategy Selection

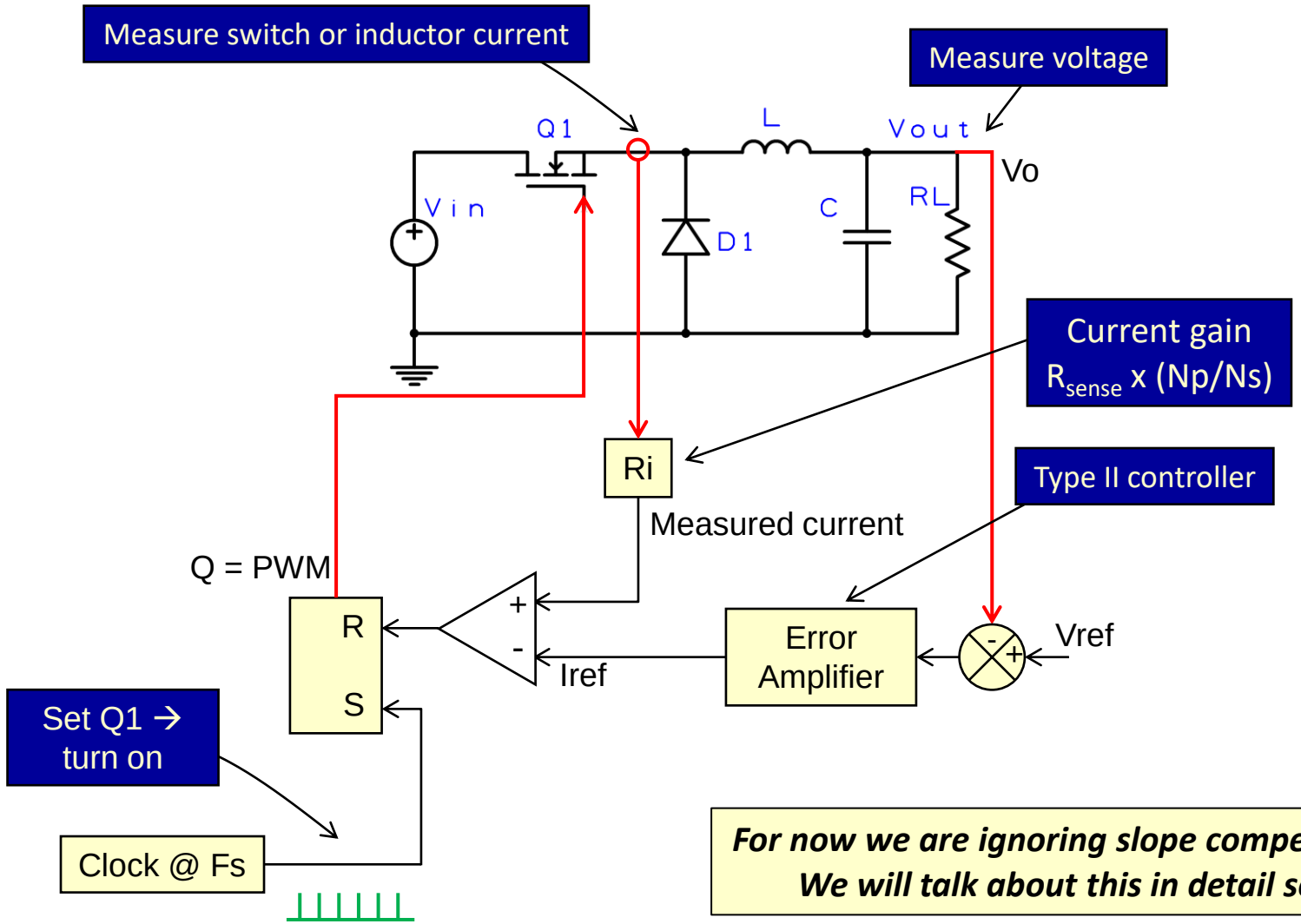


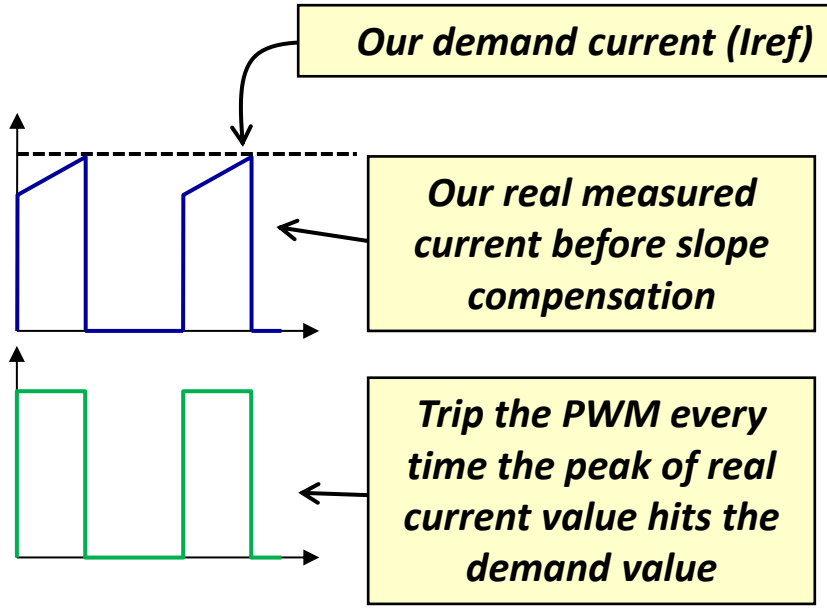
Analog Peak Current Mode

- We control the peak of the inductor current
  - We have two loops
  - An outer voltage loop regulating Vout and an inner current loop controlling the peak of the inductor current → a change in Vin will very quickly change this current
- Advantages vs Voltage Mode:
  - Better line regulation
  - Easier to parallel
  - Much better transition between Discontinuous Conduction Mode (DCM) and Continuous Conduction (CCM)
  - Can deal with topologies with right-hand plane zero (e.g. CCM Flyback, Boost, etc.)
  - Current limiting comes free
  - Maintains flux balance in push-pull converters → not very common these days
- Disadvantages
  - Plant model is complex
  - Current sensing is difficult, sensitive to layout, noisy, expensive, needs more circuitry, can be inaccurate or lossy
  - Needs leading edge blanking → there is a minimum duty limit due to this
  - Under continuous conduction mode (CCM), can have sub-harmonic oscillations and must add a compensating ramp

Current mode address all 5 problems that we discussed earlier … but it has some headaches!

Analog Peak Current Mode Operation

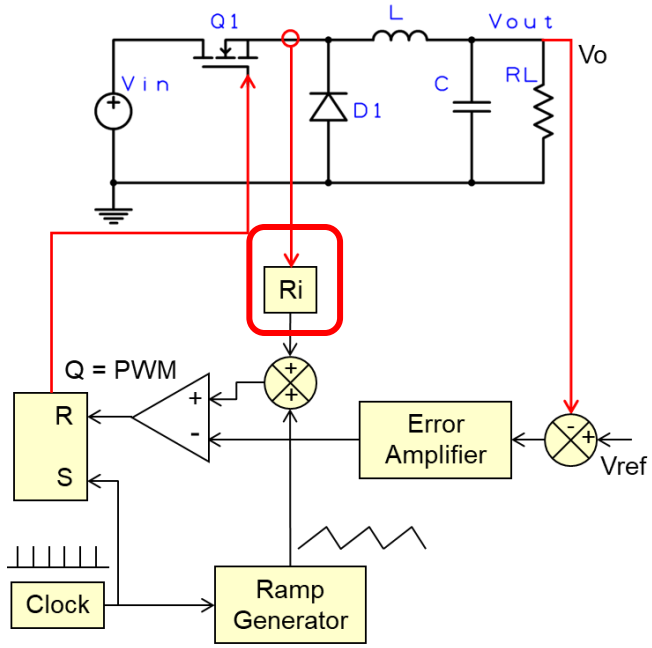


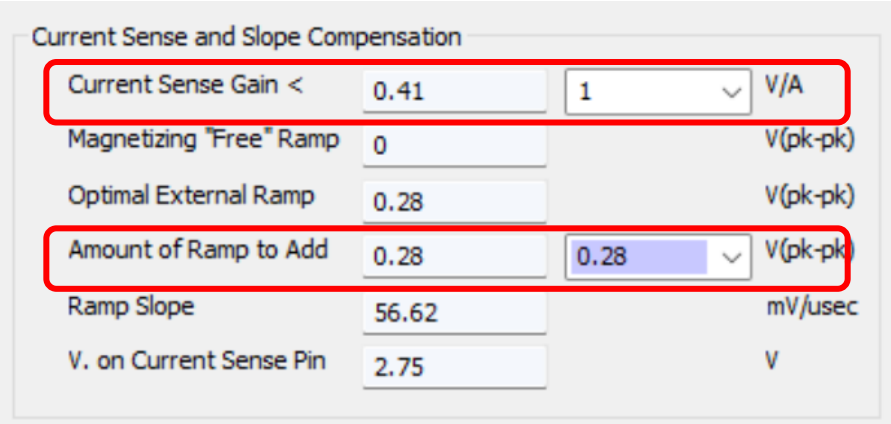


For now we are ignoring slope compensation
We will talk about this in detail soon

Current Gain Ri

- In most cases at some point we have to sense our current and convert our measured current from Amps to Volts
  - So that we can feed it into our chip
- This is the process that adds the gain term on our transfer function called Current Gain (Ri) → usually specified in V/A (not ohms! ☺)
  - Most design software including WDS need Ri to make their calculations
- Let us assume that we measure our current with a simple 1ohm sense resistor (Rsns)
  - In other words when 1A flows though our 1ohm sense resistor 1V will appear across it
  - For every Amp we will get 1V ∴ Our Current Gain Ri = 1V/A
  - This is the value that we need to type into WDS → WDS will then calculate everything else including the amount of ramp that we need





We will talk about Rsns selection, power dissipation and current sense transformers soon

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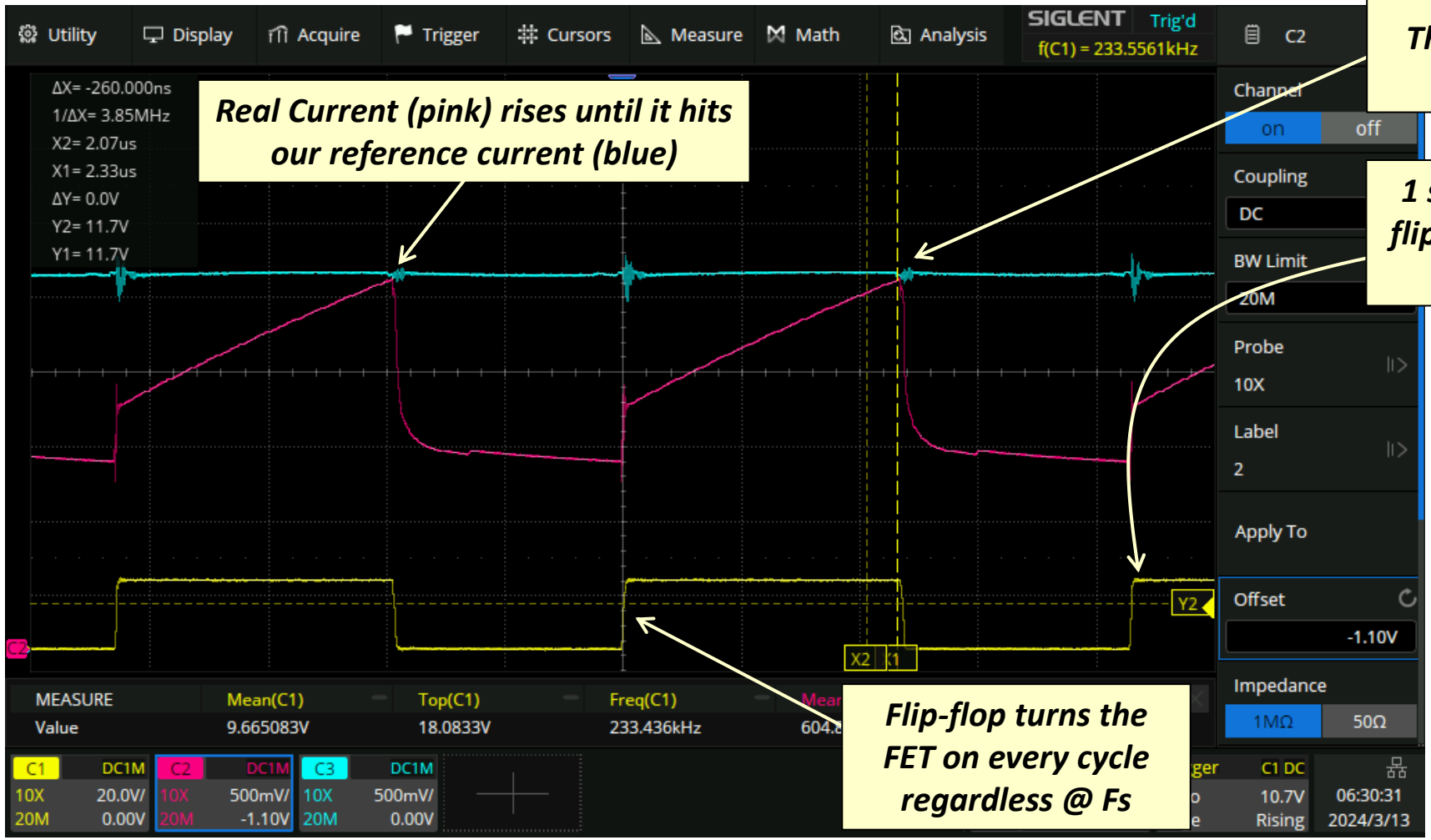
Analog Peak Current Mode Operation



When our real current is equal to our reference current, the flip-flop resets and turns FET off

Therefore we are controlling the peak of the inductor current*

1 switching cycle later, the flip-flop will turn on the FET again

Flip-flop turns the FET on every cycle regardless @ Fs

* Note there is some propagation delay and an internal 1.1 to 1.4V off-set – please see device datasheet here:
https://www.ti.com/lit/ds/symlink/uc3825a.pdf?ts=1710244414189&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FUC3825A%253FkeyMatch%253D3825

Subharmonic Oscillations in Real Life

- Peak Current mode can suffer from subharmonic oscillations which can be described as a form of instability
- The PWM will have a series of long a short pulses as shown
- The voltage loop continues to regulate, but the ripple increases
  - And there may be audible noise
- We fix this with what is called slope compensation

Why Do We Get Subharmonic Oscillations?

- To understand subharmonic oscillations please bear mind the following important points under current mode:
  - We turn the switch on at fixed times using a clock regardless of the value of the inductor current
  - We turn the switch off *whenever* the peak of the inductor current hits our demand value that we calculated in the previous cycle
  - In other words:
    - We are not allowing the inductor current freely settle to a natural steady state value
    - We are in fact forcing the inductor to act like as a controlled current source, whose peak current we are controlling
- This is not the case under voltage mode:
  - We only measure the output voltage and control the duty
  - We are not forcing the current to be a specific value and therefore its can change to whatever value it naturally needs to be
- What is “Perturbation”?
  - If you have been reading about subharmonic oscillations you will have probably heard about “perturbing” the inductor current or a small perturbation signal being injected…
  - Let us explain this term before going any further as it causes a lot of confusion

Perturbation Signal as Applied to Current Mode

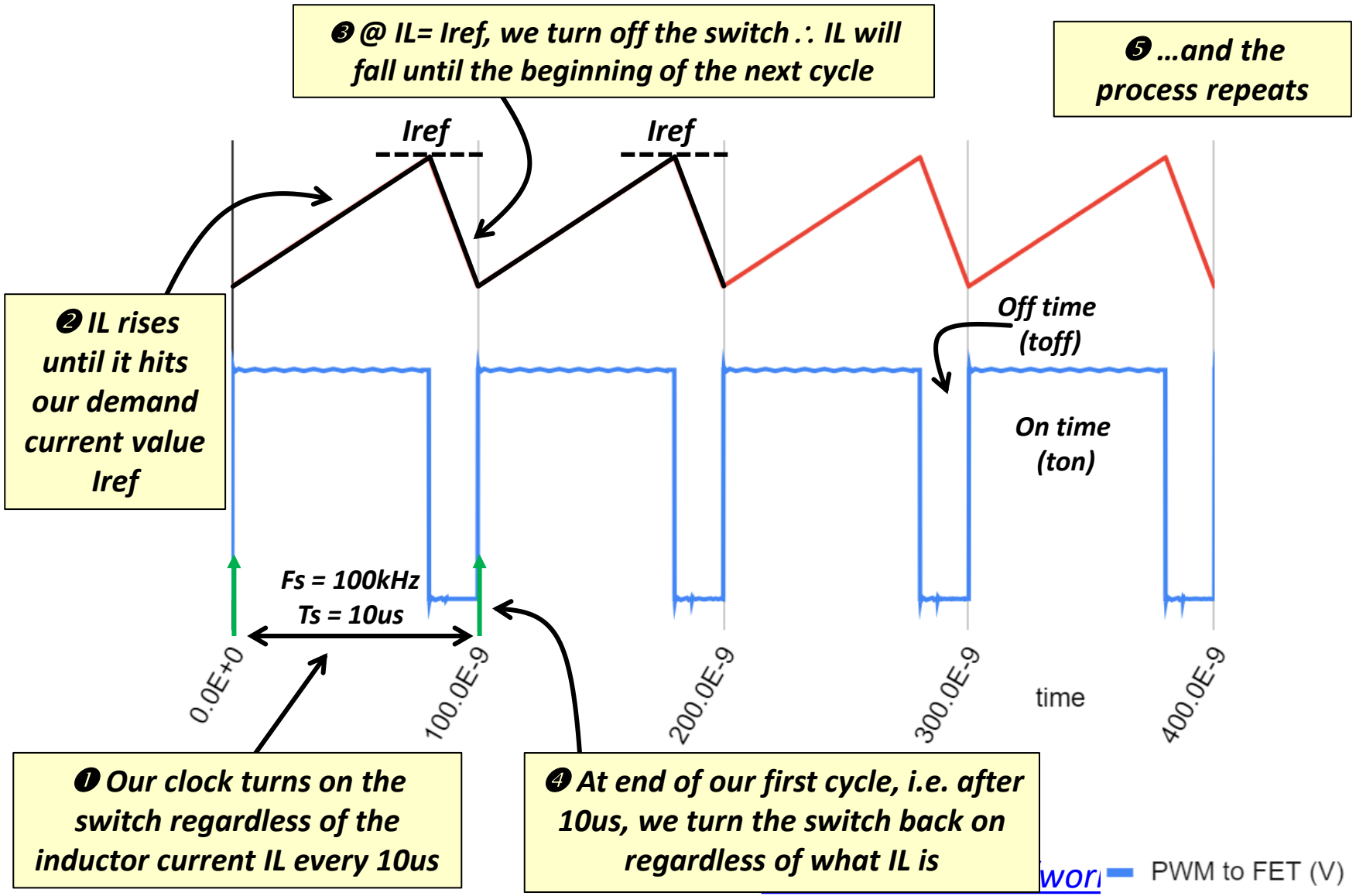
- Large signal analysis
  - Our control system is disturbed with a large change and its behavior is studied
  - e.g. our power supply is given a 50% load step
  - Works great for linear systems, e.g. resistor + linear voltage source
- Deriving large signal mathematical models for nonlinear systems such as power supplies is complex
  - We can give our power supply a large load step (large signal) and look at its behavior with a scope, but deriving a mathematical equation for it is difficult
- To make analysis of non-linear systems easier, mathematicians invented *small signal analysis*
  - The assumption is that even non-linear systems behave relatively linearly provided that our injected signal is small → hence the name *"Small"* Signal Analysis ☺
- So if we keep our injected signal so small that our system still behaves linearly then our analysis becomes easier → we call this a small *"perturbation"*
  - We can use straight line equations instead of differential equations

So when we say we "perturb" the inductor current we mean*:

We "disturb/perturb/cause" a change the inductor current, small enough for us to see a change but not large enough to get the control loop to act in a nonlinear manner

* Within the context of subharmonic oscillation analysis in current mode power supplies

Current Mode with No Perturbation → Stable Regardless of Duty



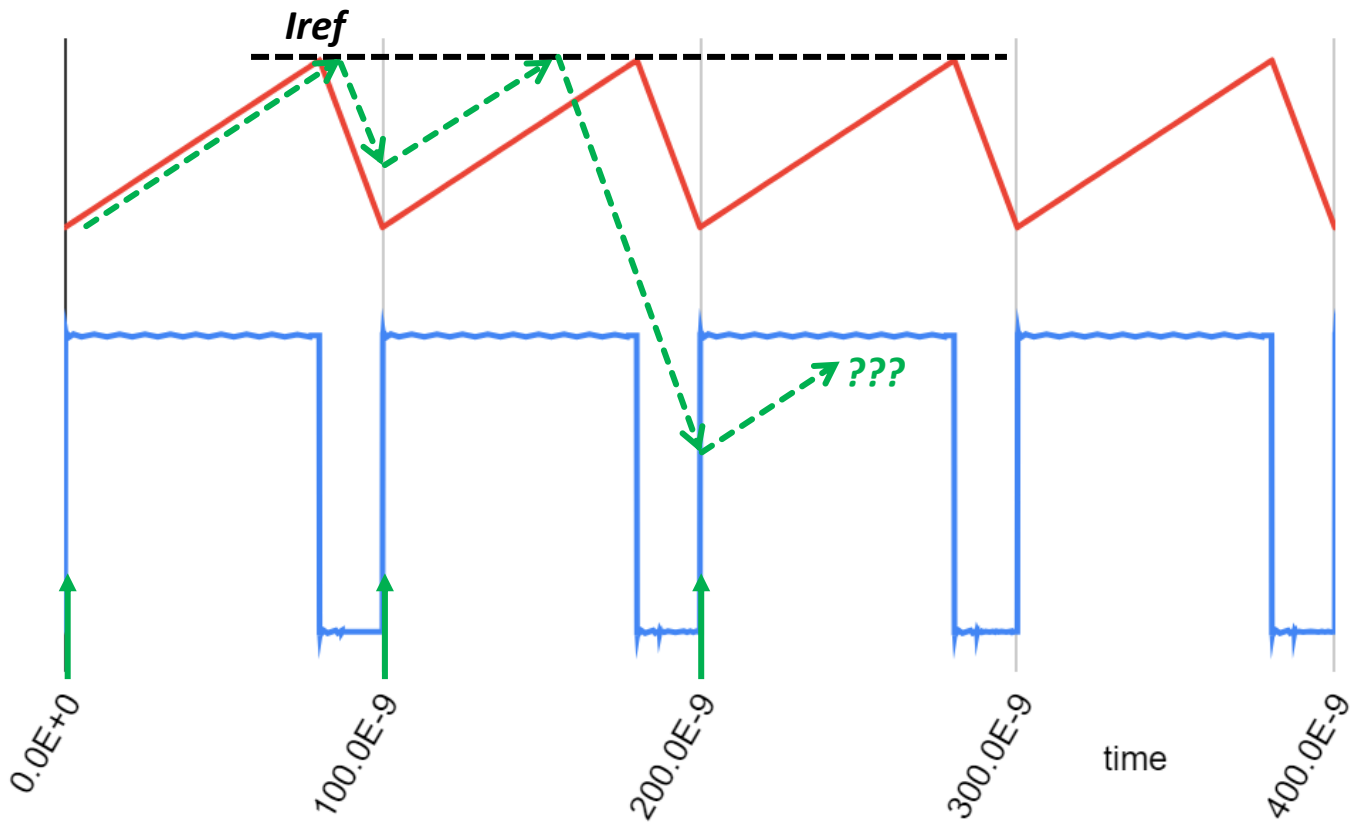
- For simplicity let us assume that Fs = 100kHz, so the clock will turn the switch on every 10us regardless of current

This is theoretical and for teaching purposes only!

In real life there is ALWAYS some perturbation

Current Mode with Perturbation (Duty >= 50%)

- Under peak current mode with D >=50%, the smallest of perturbations would result in big changes in duty, increased current ripple and undamped oscillations



This drawing is grossly exaggerated for demonstration/teaching purposes

Let us now show a real simulation …

Small Perturbation in Current with D > 50%

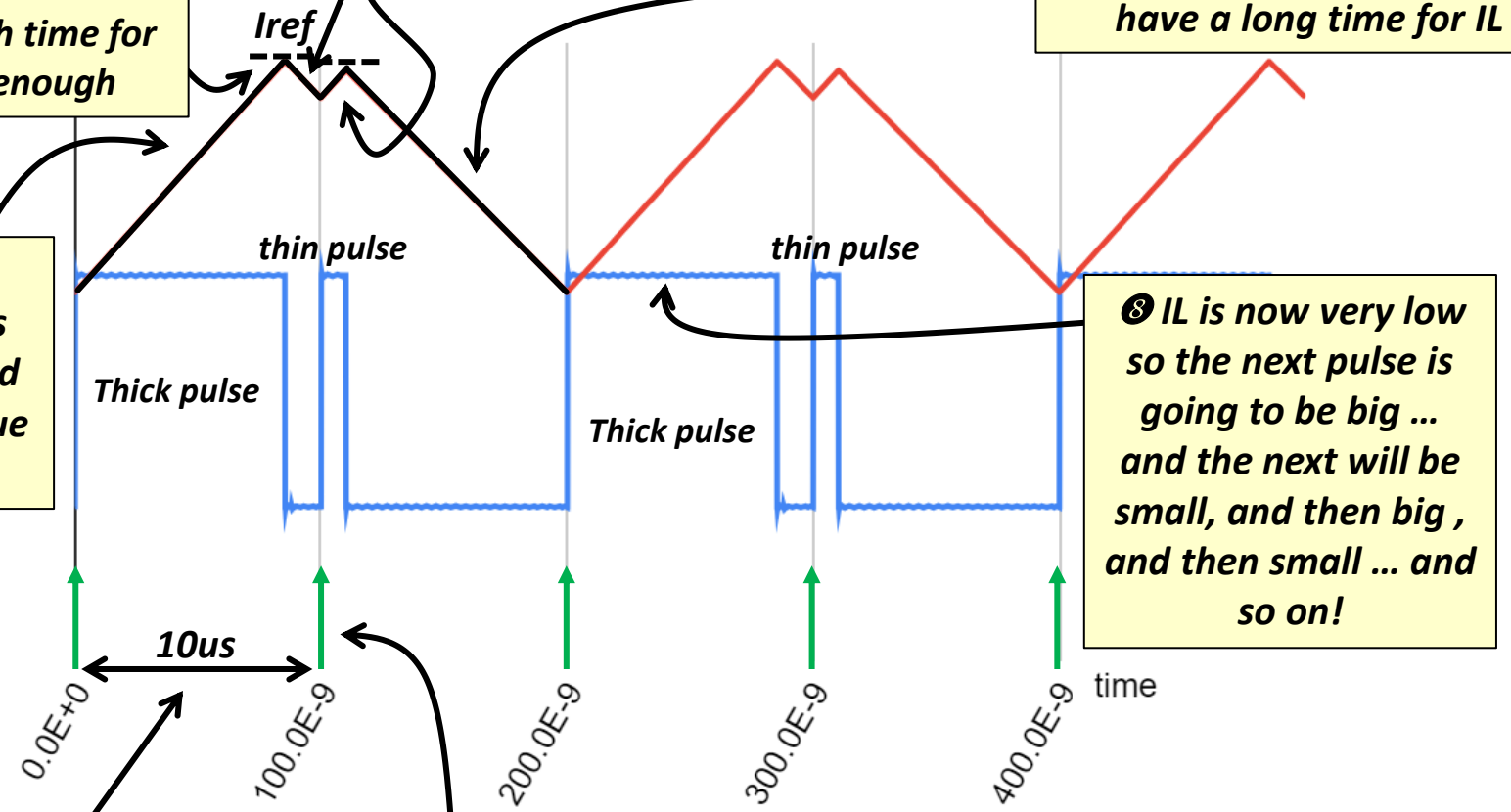
❸ IL= Iref so we turn off the switch but duty is big → there isn't enough time for IL to fall enough

❹ IL starts to fall …but time's up!

❻ IL starts to rise from an already high value and very quickly hits the new value of Iref, so the switch turns off early and we end up with a thin pulse

❼ But because of the small duty of the last pulse, we now have a long time for IL to fall until the next clock cycle

As duty approaches 50%, any oscillations will not naturally decay … so we end up with subharmonic oscillations



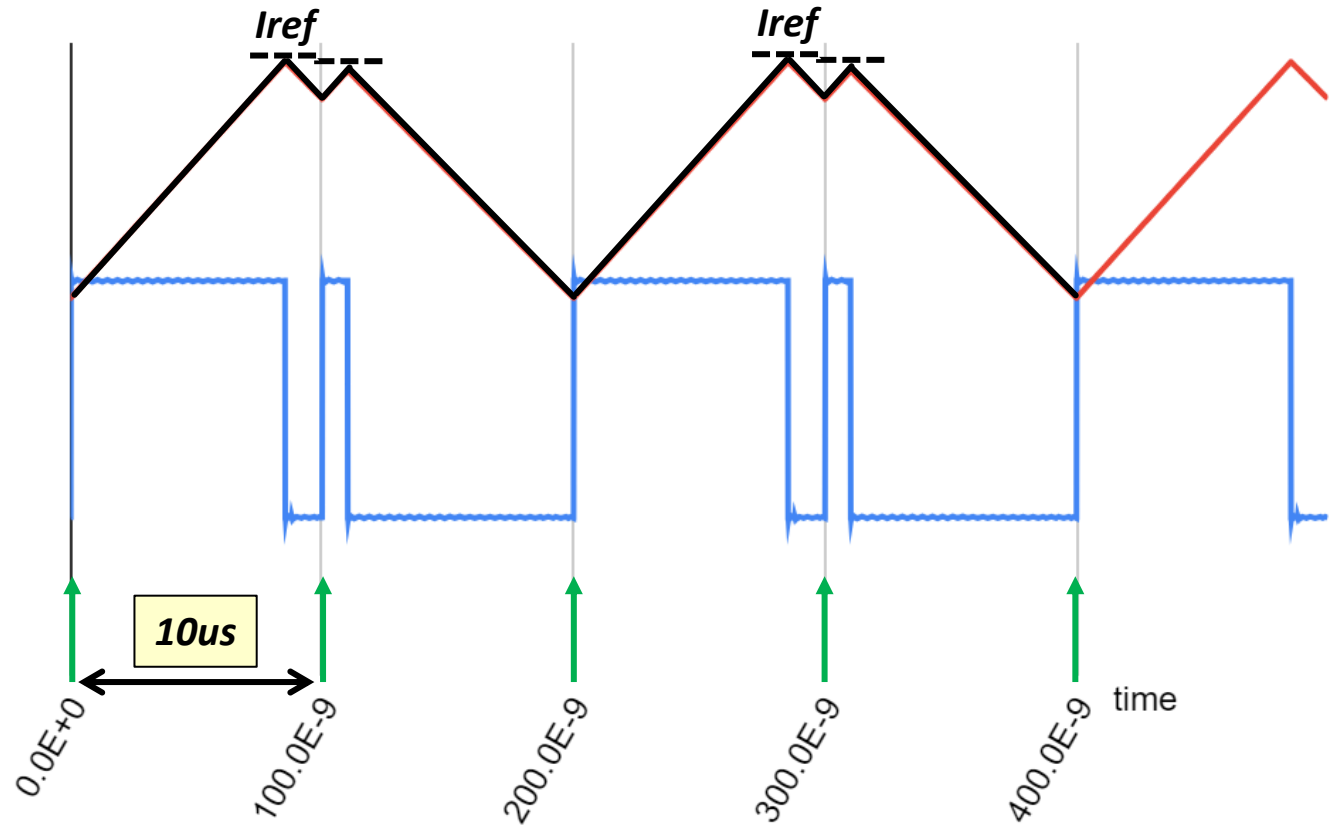
❷ IL rises until it hits our demand current value Iref

❽ IL is now very low so the next pulse is going to be big … and the next will be small, and then big , and then small … and so on!

❶ Again our clock turns on the switch regardless of the IL every 10us

❺ At end of our first cycle, i.e. after 10us, we turn the switch back on regardless IL … but IL has not fallen very much

Current Mode in Real Life (D >= 50%)



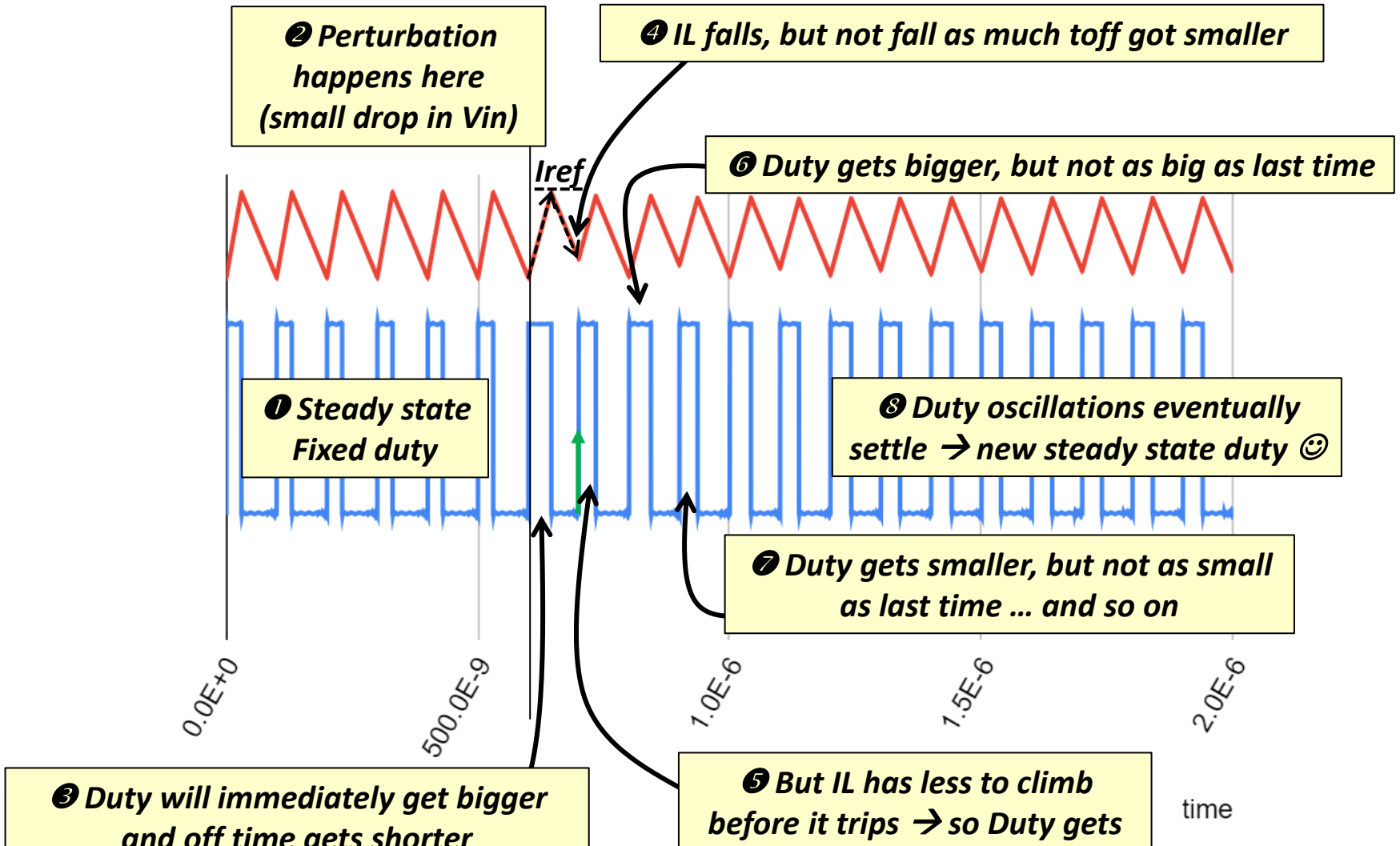
- The last slide was too busy, so let's go through it again without all the text!

We can remove subharmonic oscillations by adding slope compensation

Important: As duty approaches 50%, any oscillations will not naturally decay … so we end up with subharmonic oscillations

If our duty is smaller than 50%, subharmonic oscillations will naturally decay

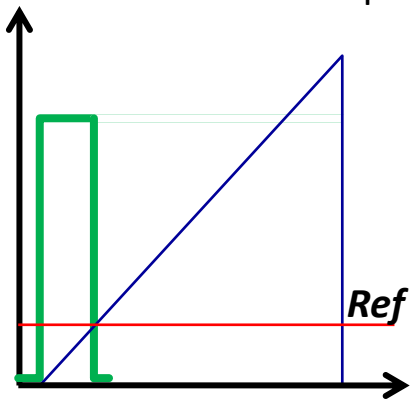
Current Mode in Real Life (D < 50%)



Provided our D < 50%, after a perturbation any undesired oscillations in IL will naturally decay and go away … this is not the case for D>50% so we need to fix it → with Slope Compensation

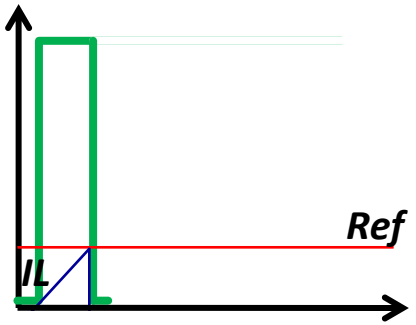
Slope Compensation

- The root cause of subharmonic oscillations is the way in which our PWM is generated in current mode
  - After all these subharmonics do not happen in voltage mode
- Under voltage mode, we generate our PWM by comparing a "*variable*" reference with a "*fixed amplitude*" ramp
  - This ramp is often generated by the clock
  - Some texts call this an "artificial ramp"
- But in current mode both the reference *and* the ramp are varying
  - Because our ramp is being generated using IL



PWM generation in voltage mode

If we add a little bit of fixed ramp to our IL, we will make a hybrid system… this is called slope compensation



PWM generation in current mode

If 100% of our ramp is artificial/fixed (i.e. Vmode) we do not have a subharmonic oscillations problem

If 100% of our ramp is varying (i.e. IL in Imode) we do have subharmonic a oscillations problem

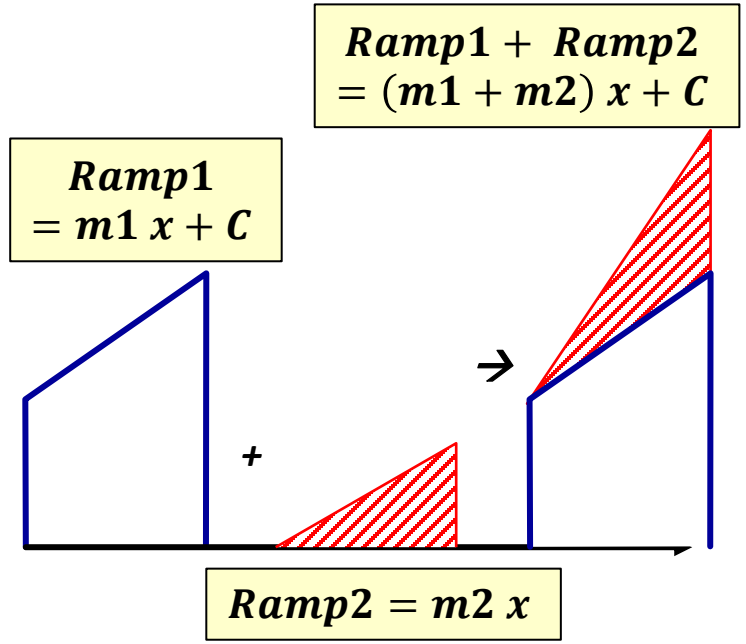
What if we make a hybrid system whose ramp, let us say, is 50%* fixed/artificial and 50% IL?

* 50% for simplicity of teaching only; we will soon explain how to calculate the size of this artificial ramp

www.

Slope Compensation

- Mathematically, if add a ramp with a positive slope to another ramp with a positive slope, the result will another ramp with and even sharper slope
- And that is why it is called slope compensation ☺
- If we add a certain amount of fixed/artificial ramp to our current, subharmonic oscillations will naturally decay
  - Essentially we are adding a bit of voltage mode control into our current mode controller*
- The more ramp we add, the larger the duty before which we get oscillations → but obviously there is a limit:
  - If we add too much ramp the system starts to behave like voltage mode
    - With all its disadvantages, it may even go unstable → more on this later
  - If we add too little ramp, we may get oscillations
- Obviously we have to find a sweet spot
  - Luckily most IC add the ramp automatically
  - They very rarely add too little ramp, but sometimes they may add too much → more on this soon

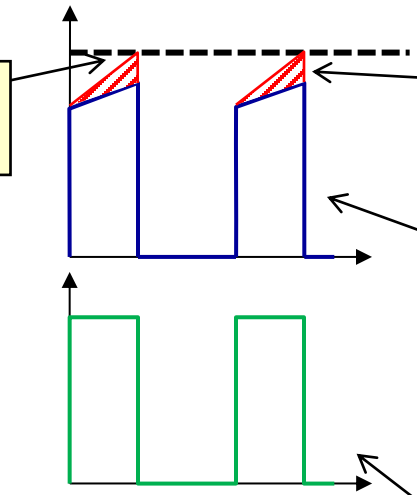


* Maniktala, ISBN 978-0123865335

Slope Compensation

- The subharmonic oscillations can be removed by adding slope compensation → we add a ramp to the inductor current during "on" period
- We *increase the slope* of our current during the on time (up-slope) a little bit by adding an extra ramp
  - This has the effect of damping the oscillations such that they gradually decay
- In fact, we are damping the Q of the double pole (resonant peak) @ Fs/2 in frequency domain
  - What we would like to do is this:

In most modern analog chips slope compensation is now done internally so we no longer need to worry (too much ☺) about the implementation



This is our demand current Iref

Red trace is our measured current <u>plus</u> the added the compensating ramp

Blue trace is our real measured current <u>before</u> slope compensation

Finally we trip the PWM every time the peak of real current + slope value hits the demand value

Analog Peak Current Mode Operation