# AT6558R

## BDS/GNSS satellite positioning SOC chip

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|---|---|---|
| Hangzhou Zhongke Microelectronics Co., Ltd. | title | AT6558R<br>BDS/GNSSSatellite positioningSOCchip |
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| | Document Number | DS-AT6558-R |
| | Version Number | 1.0 |
| Document Summary | | |
| This manual provides the chip's functional features, chip overview, and usage instructions. | | |

Table of contents

# 1 Chip Overview

## 1.1 Chip Introduction

AT6558RIs a high performanceBDS/GNSSMulti-mode satellite navigation receiverSOCSingle chip, integrated RF front end, Digital baseband processor,32PositionRISC CPU, power management function.

The chip supports multiple satellite navigation systems, including China's BeiDou satellite navigation systemBDS, the United StatesGPS,Russia ofGLONASS, and realize multi-system joint positioning.

## 1.2 Main features

- Functional Specifications

  -supportBDS/GPS/GLONASSMulti-system joint positioning and single-system independent positioning.

- Sensitivity
  - Cold Start Capture Sensitivity: -148dBm.
  - Tracking sensitivity: -162dBm.
- Power Management
  - support2.7~3.6VSingle power supply, typical3.3Vpowered by.
  - RTCand backup circuit power can be as low as1.4V.
  - BDS/GPSDual-mode continuous operation:23mA(@3.3V).
  - Standby:8uA(@3.3V)
- Antenna detection and protection
  - Supports active antenna detection.
  - Supports active antenna short-circuit protection.
- Package and size

  -QFN40Package, chip size:5mm×5mm×0.9mm.

1.3 Performance indicators

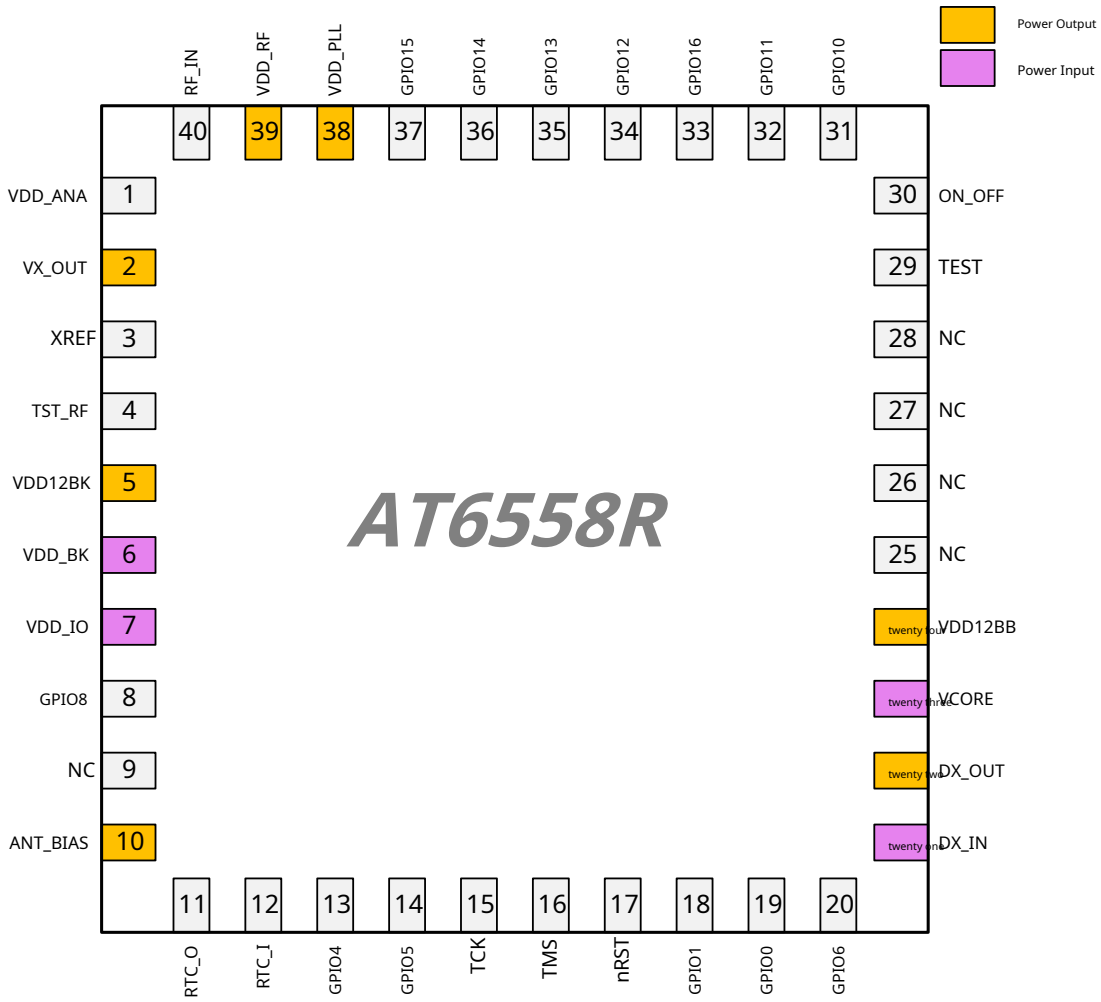
| Technical Parameters | index |
|---|---|
| Signal reception | supportBDS/GPS/GLONASSParallel reception and joint positioning |
| Cold StartTTFF | ⩽32s |
| Hot StartTTFF | ⩽1s |
| RecaptureTTFF | ⩽1s |
| Cold start capture sensitivity | - 148dBm |
| Hot start capture sensitivity | - 156dBm |
| Recapture sensitivity | - 160dBm |
| Tracking sensitivity | - 162dBm |
| Positioning accuracy | <2m（1σ） |
| Speed measurement accuracy | <0.1m/s（1σ） |
| Timing accuracy | <30ns（1σ） |
| Positioning update rate | maximum5Hz |

## 1.4 Chip Application

- Vehicle positioning and navigation
- Timing
- Wearable devices
- Portable devices such as mobile phones and tablets

## 2 Pin Description

### 2.1 Pin Arrangement




picture2-1Chip package pin arrangement

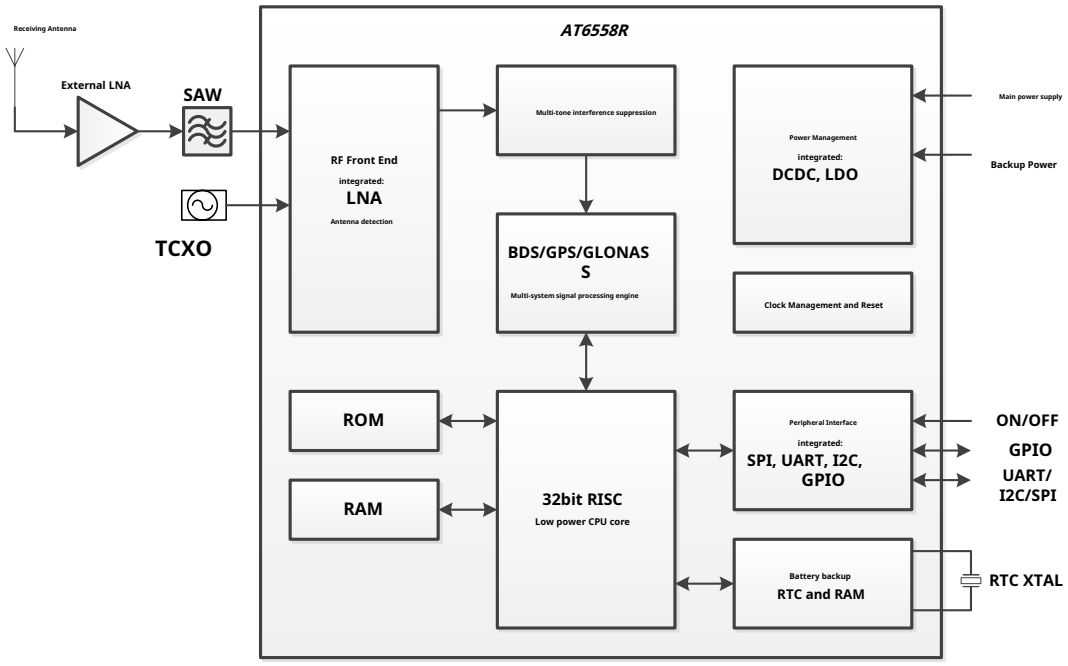
### 2.2 Pin Description

| Serial number | name | I/Otype | Functional Description |
|---|---|---|---|
| 1 | VDD_ANA | Analog Power Supply | simulationLDOOutput,1.08~1.32V,1uFCapacitor grounding |
| 2 | VX_OUT | simulationIO | Output toTCXOPower supply,2.7~3.6V,0.1uFCapacitor grounding |
| 3 | XREF | simulationIO | Clock input terminal, externalTCXO |
| 4 | TST_RF | simulationIO | RF test port. Default output3.3VVoltage |
| 5 | VDD12BK | simulationIO | BackupLDOThe output,1.08~1.32V |
| 6 | VDD_BK | Analog Power Supply | Backup power input,1.4~3.6V |
| 7 | VDD_IO | Digital Power | numberIOPower input,2.7~3.6V |

| | | | |
|---|---|---|---|
| 8 | GPIO8 | Digital two-way | GeneralGPIO, the default mode configuration, should be left floating when used |
| 9 | NC | | |
| 10 | ANT_BIAS | simulationIO | Active antenna powering and detection,2.7~3.6V |
| 11 | RTC_O | simulationIO | RTC OSCOutput |
| 12 | RTC_I | simulationIO | RTC OSCInput |
| 13 | GPIO4 | Digital two-way | GeneralGPIO, the default isUART1ofTXD |
| 14 | GPIO5 | Digital two-way | GeneralGPIO, the default isUART1ofRxD |
| 15 | TCK | Digital Input | SWDDebug interface clock line |
| 16 | TMS | Digital two-way | SWDDebug interface data line |
| 17 | nRST | simulationIO | External reset input, with internal pull-up, must be left floating if not used |
| 18 | GPIO1 | Digital two-way | GeneralGPIO, the default isUART0ofRxD |
| 19 | GPIO0 | Digital two-way | GeneralGPIO, the default isUART0ofTXD |
| 20 | GPIO6 | Digital two-way | GeneralGPIO, default input |
| twenty one | DX_IN | Analog Power Supply | DCDCenter,2.7~3.6V |
| twenty two | DX_OUT | simulationIO | DCDCOutput,1.35~1.75V |
| twenty three | Vcore | Analog Power Supply | Chip main power input,1.4~3.6V |
| twenty four | VDD12BB | Digital Power | Digital CoreLDOOutput,1.08~1.32V |
| 25 | NC | Digital two-way | NC |
| 26 | NC | Digital two-way | NC |
| 27 | NC | Digital two-way | NC |
| 28 | NC | Digital two-way | NC |
| 29 | TEST | Digital Input | Mode control, keep low level for normal operation; internal pull-down |
| 30 | ON_OFF | Digital Input | Shutdown control, keep high level for normal operation; internal pull-up |
| 31 | GPIO10 | Digital two-way | GeneralGPIO,defaultI2CofSCLClock Line |
| 32 | GPIO11 | Digital two-way | GeneralGPIO,defaultI2CofSDAData cable |
| 33 | GPIO16 | Digital two-way | GeneralGPIO, must be left unconnected by default |
| 34 | GPIO12 | Digital two-way | GeneralGPIO, default input |
| 35 | GPIO13 | Digital two-way | GeneralGPIO,default1PPSOutput |
| 36 | GPIO14 | Digital two-way | GeneralGPIO, default input |
| 37 | GPIO15 | Digital two-way | GeneralGPIO, default input |
| 38 | VDD_PLL | simulationIO | Phase-locked loopLDOOutput,1.08~1.32V |
| 39 | VDD_RF | simulationIO | Radio FrequencyLDOOutput,1.08~1.32V |
| 40 | RF_IN | Radio FrequencyIO | RFenter |
| EP | GND | Bottom Metal | Public grounding point must be well grounded |

## 3 Chip Architecture

### 3.1 Chip Block Diagram




picture3-1chipblock diagram

3.2 Power supply solution

3.2.1 Chip low power supply connection solution

As shown3-2As shown, the main power supplyVDD_3.3Vsupply3.3VPower supply, which provides power to the entire chip.

VDD_3.3VConnect toVDD_IOFor chipsIO PADPower supply; also to the internalPORPowered by a two

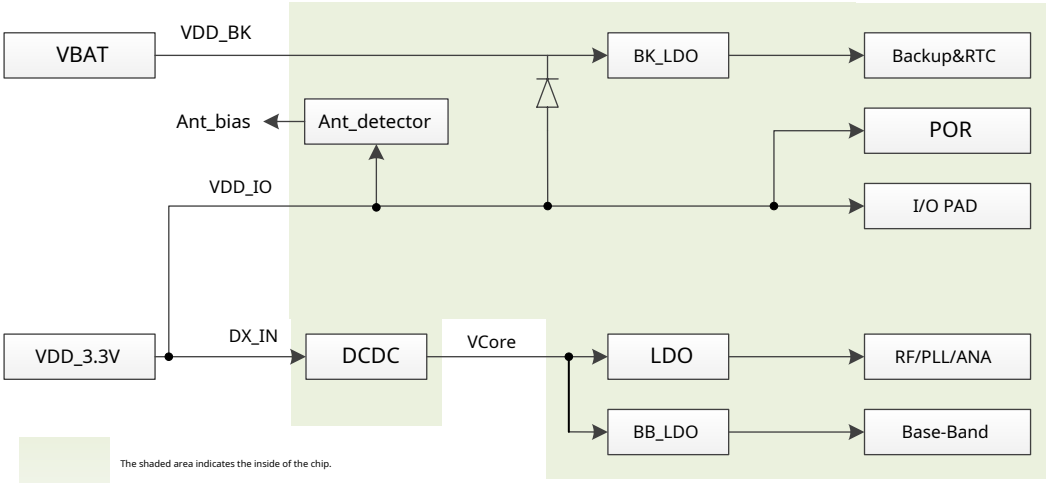
The diode supplies power to the backup area; it also supplies power to the antenna detection and active antenna parts.

VDD_3.3VConnect toDCDCInputDX_INrightDCDCPower supply, useDCDCOutput as internalLDOlose

In, from the insideLDOProvides power to the RF front-end, analog and digital parts of the chip.

External button battery as backup power supply (VBAT) to supply power to the backup area of the chip, which can be used when the main power fails

Provides power to backup circuits.




picture3-2Chip low power supply connection solution (using chip internalDCDC)

3.2.2 Power connection scheme without DCDC

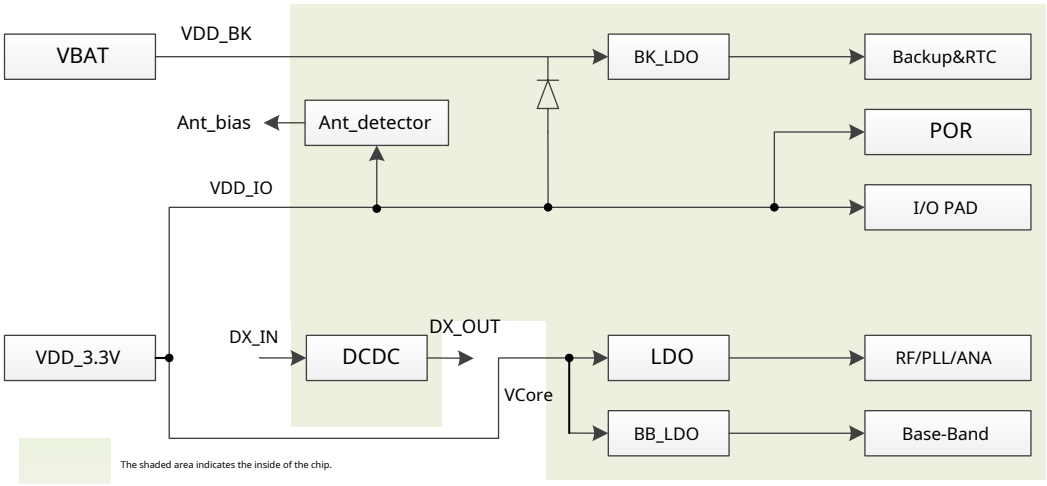
In the externalPMUOr if you are not sensitive to power consumption, you can choose not to use the internal chipDCDC. Can be omittedDCDCoutside

The inductor and capacitor components of the part; at the same time, the performance is better than usingDCDCThere is a certain improvement.

External button battery as backup power supply (VBAT) to supply power to the backup area of the chip, which can be used in case of a main power failure

The backup circuit is powered.

Note: Do not useDCDChour,DX_INandDX_OUTIt is recommended to leave the pin floating.




picture3-3No chip insideDCDCPower connection scheme

## 3.3 Working Mode

The chip has multiple working modes: full working mode, sleep mode and battery backup mode.

Full working mode: All power supplies are working normally, andON_OFFWhen the pin is high, the chip is in full working mode.

Perform normal signal reception and resolution.

Sleep mode: All power supplies are normal.ON_OFFPulling the pin low will turn offDCDCandLDO, RF circuits and

The baseband circuit stops working and enters a low-power sleep state.ON_OFFAfter the pin is pulled high, the chip will automatically resume full operation

mode (equivalent to a hot start).

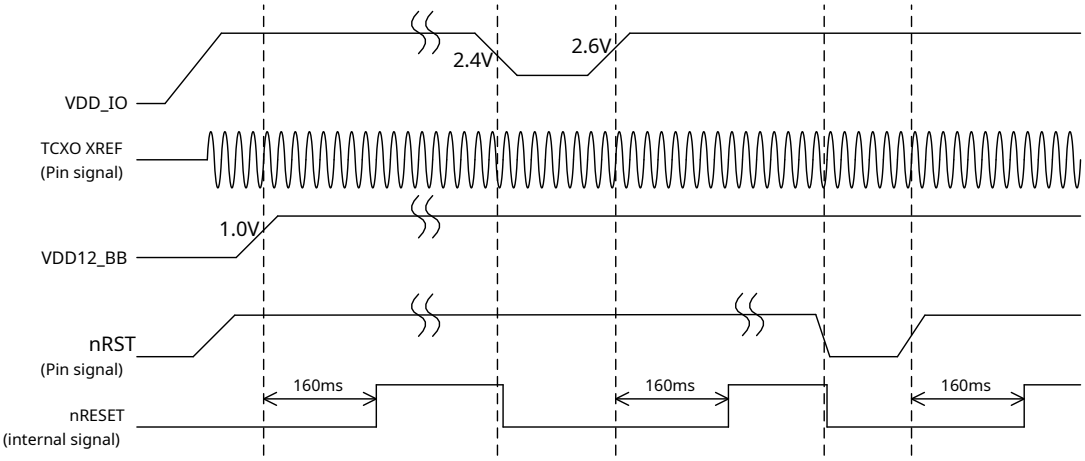
Battery backup mode: Turn offVDD_BKAll power sources except for theRTCclock

and backupRAMAfter power is restored, the navigation program can be restored from the backupRAMRecovery for a fast warm start.

| model | RF Front End | Baseband Core | IO/POR | RTC/**BackupRAM** |
|---|---|---|---|---|
| Full working mode | √ | √ | √ | √ |
| Sleep Mode | × | × | √ | √ |
| Battery backup mode | × | × | × | √ |

## 3.4 Chip Reset

The chip integrates a power-on reset circuit and supports external reset. The reset sequence is as follows:

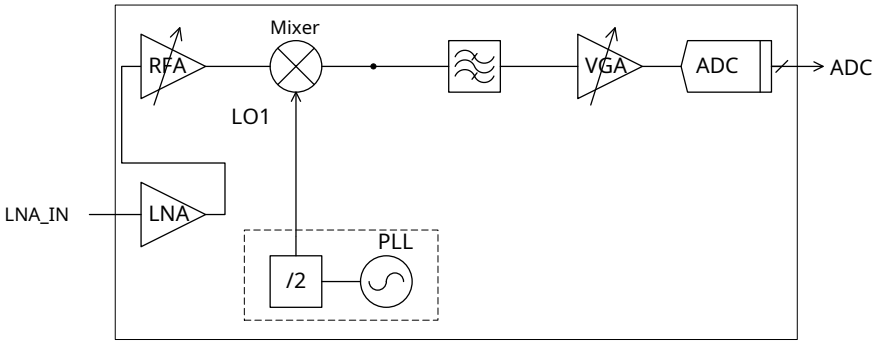



picture3-5Chip reset timing diagram

# 4 RF front end

## 4.1 RF Front-end Architecture

The RF front end supports satellite signal frequencies of the entire constellation:BDS B1,GPS L1,GLONASS L1. Data channel sharing LNA/RFAandPLL, supports multiple reference frequencies. Integrated active antenna detection circuit, integrated clock multiplication circuit,ADCPick The sampling frequency is configurable.




picture4-1Chip RF front-end block diagram

## 4.2 Active Antenna Detection

The chip integrates active antenna detection circuit, which can feed the external active antenna. The active antenna detection circuit also provides short circuit protection by limiting the current feeding the active antenna. Protect the chip and active antenna from damage.

The detection circuit defines three states. When the current is less than the set value, it indicates that the antenna is open; when the current is greater than the set value, Indicates that the antenna is normal; when the current is too large or a short circuit occurs, it indicates that the antenna is overcurrent.

# 5 Baseband Processor

## 5.1 Multi-system satellite processing engine

The chip integrates the latest multi-system satellite processing engine, supportingBDS,GPS,GLONASSThe system signal and The joint positioning can significantly improve the positioning accuracy and positioning availability, especially in complex environments such as urban canyons. The improvement is more significant.

## 5.2 Real-time clock backup area

Real-time clock (RTC) is located in the battery powered area and is equipped with a backupRAM. Use independent low powerLDO Provide power supply.RTCIt can work normally in case of loss of main power supply, while ensuring backupRAMThe data in Lost.

## 5.3 UART

Contains two independent full-duplexUARTModule, realizes the conversion between serial and parallel data, the baud rate is supported hold256000bps, and has automatic baud rate detection function.

# 6 Electrical characteristics

### 6.1 Limiting characteristics

| parameter | Maximum swing | unit |
|---|---|---|
| Power supply to ground voltage (analog core power supply, digital core power supply) | - 0.3~1.8 | V |
| Power supply to ground voltage (digitalIORear drive power supply,LDOInput Power) | - 0.3~4.1 | V |
| Analog pin voltage | - 0.3~1.8 | V |
| Other pin voltages | - 0.3~4.1 | V |
| Maximum RF input power | 5 | dBm |
| Operating temperature | - 40~85 | ℃ |
| Junction temperature | 150 | ℃ |
| Storage temperature | - 50~125 | ℃ |

### 6.2 DC Characteristics

#### 6.2.1 Power pins

| parameter | Minimum | Typical Value | Maximum | unit |
|---|---|---|---|---|
| VDD12BB | 1.08 | 1.2 | 1.32 | V |
| VDD12BK | 1.08 | 1.2 | 1.32 | V |
| VDD_ANA | 1.08 | 1.2 | 1.32 | V |
| VDD_PLL | 1.08 | 1.2 | 1.32 | V |
| VDD_RF | 1.08 | 1.2 | 1.32 | V |
| VDD_IO | 2.7 | 3.3 | 3.6 | V |
| VDD_BK | 1.4 | 3.3 | 3.6 | V |
| VCore | 1.4 | 1.5 | 3.6 | V |
| DX_IN | 2.7 | 3.3 | 3.6 | V |
| DX_OUT | 1.4 | 1.5 | 1.75 | V |

#### 6.2.2 Digital IO Pins

| parameter | illustrate | Minimum | Typical Value | Maximum | unit |
|---|---|---|---|---|---|
| Ileak | Leakage current input pin | --- | <1 | --- | uA |
| Vil | Low level input voltage | - 0.3 | 0 | VDD_IO*0.2 | V |
| Vih | High level input voltage | VDD_IO*0.8 | --- | VDD_IO+0.3 | V |

| | | | | | |
|---|---|---|---|---|---|
| Vol | Low level output voltage | - - - | 0 | 0.4 | V |
| Voh | High level output voltage | VDD_IO-0.4 | - - - | | V |
| R | Pull-up resistor | | 40 | | kΩ |
| R | Pull-down resistor | | 40 | | kΩ |

6.3 Simulation-related characteristics

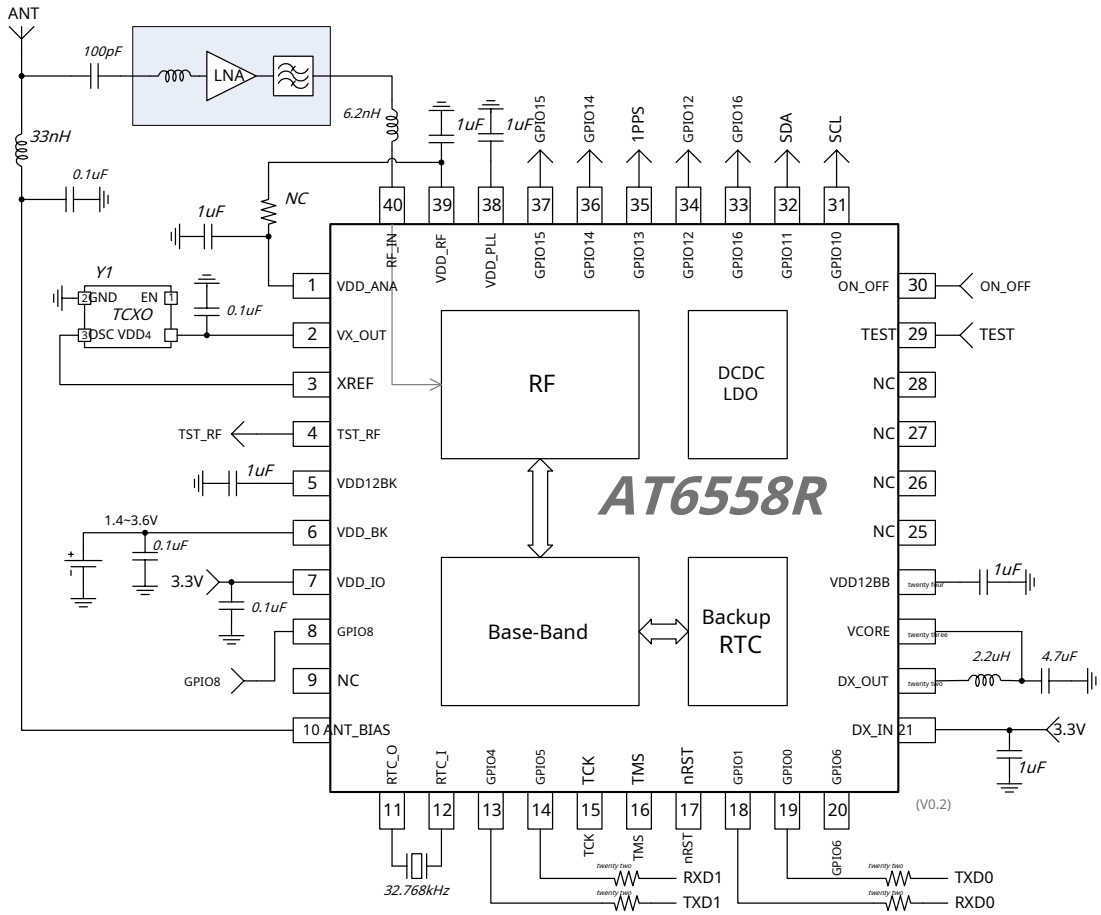
| Serial number | parameter | condition | Parameters | | | unit |
|---|---|---|---|---|---|---|
| | | | Minimum | Typical Value | Maximum | |
| 1 | Reset voltage | @VDD_IO | 2.35 | 2.45 | 2.6 | V |
| 2 | Reset time | Crystal frequency 26.000MHz | | 160 | | ms |
| 3 | TCXOCrystal frequency] | | | 26.000000 | | MHz |
| 4 | TCXOAmplitude | | 0.5 | 1.5 | | Vpp |
| 5 | Active Antenna Detection current | | 2.5 | | | mA |
| 6 | Active Antenna Short circuit protection current | | 45 | 50 | 60 | mA |
| 7 | Antenna detection circuit voltage drop | enter3.3V,50mAload | | | 0.3 | V |
| 8 | Working current | @3.3V BDS+GPS | | twenty three | | mA |
| 9 | Battery backup current | | | 8 | | uA |
| 10 | Sleep mode current | ON_OFF=0 | | 20 | | uA |
| 11 | RTC Crystalfrequency | | | 32.768 | | kHz |
| 12 | RTC CrystalEquivalence Series resistance*Rs* | | | | 80 | KΩ |
| 13 | RTC CrystalSeries Capacitor | | | 8 | | pF |

6.4 RF-related characteristics

| sequence Number | parameter | condition | Parameters | | | unit |
|---|---|---|---|---|---|---|
| | | | Minimum | Typical Value | Maximum | |
| 1 | Input frequency $F_{in}$ | GPS | | 1575.42 | | MHz |
| | | Galileo | | 1575.42 | | MHz |
| | | BDS | | 1561.098 | | MHz |
| | | GLONASS | 1597.78 | 1602 | 1605.66 | MHz |
| 2 | Input signal level $P_{IN}$ | | - 110 | | - 65 | dBm |
| 3 | Input reflection coefficientS11 | | | | - 10 | dB |
| 4 | Noise FigureNF | | | 2.5 | | dB |
| 5 | 1dBCompression Point | | | - 75 | | dBm |
| 6 | Image Rejection Ratio | | 16 | 26 | | dB |
| 7 | Phase-locked loop lock time | | | | 100 | us |
| 8 | AGCStabilization time | | | | 100 | us |

## 7 Reference Design

### 7.1 Reference Solution




picture7-1Chip reference design

The application solution can use passive antenna or active antenna, and the total external gain of the chip is recommended to be greater than18dB, less than35dB.

Active antenna throughANT_BIASPower supply to provide antenna detection and short circuit protection.

The capacitor should be close to the RF inlet.

Notice,RF_INThe DC voltage of the pin shall not exceed1.2VIf the externalLNAThe output is DC and must be powered

Capacity for direct isolation.

Positioning information is output through the serial port. The output port isUART0, corresponding toGPIO0（TXD0)andGPIO1（RXD0).

Materials list: Please refer to "*Main peripheral devicesBOMSelection Table*"

7.2 Device Selection

Main peripheral devicesBOMSelection Table

| Device Name | parameter | Encapsulation | Specification | factory | model |
|---|---|---|---|---|---|
| DC/DCPower Inductors | 2.2uH | 0603 | ±20%,620mA,0.5Europe | SAMSUNG | CIG10W4R7MNC |
| | | | | MURATA | LQM18PN4R7MFR |
| High frequency inductor | 4.3nH | 0402 | ±0.2nH,750mA,0.07Europe | MURATA | LQW15AN4N3C00D |
| | | | ±0.3nH,300mA,0.21Europe | | LQG15HN4N3S02 |
| | 6.2nH | | ±3%,570mA,0.13Europe | | LQW15AN6N8H00D |
| | | | ±5%,300mA,0.29Europe | | LQG15HN6N8J02 |
| | 33nH/47nH | | ±3%,260mA,0.63Europe | | LQW15AN33NH00D |
| | | | ±5%,200mA,0.67Europe | | LQG15HN33NJ02 |
| RTCCrystal | 32.768K | SMD3215 | 20ppm,CL=8pF | EPSON | FC-135 |
| | | | | KDS | DST310S |
| TCXOCrystal Oscillator | 26M | SMD2520 | 3.3V,<br>0.5ppm@-30℃to +85℃ or<br>0.5ppm@-40℃to +85℃ | EPSON | TG-5035CG |
| | | | | | TG-5006CG |
| | | | | KDS | DSB221SDN |
| | | | | KYOCERA | KT2520K26000ACW33T |
| | | | | NDK | NT2520SB |
| | | | | TXC | 7L26003 |
| | | | | SIWARD | STO-2520A |
| Low Noise Amplifier | LNA | 6UDFN | Gain=21.5dB,NF=0.8dB | Hangzhou Zhongkewei | AT2659 |

| | | | | | |
|---|---|---|---|---|---|
| filter | SAW | SMD1411 | Insertion Loss= 0.9dB@1575.42M<br>impedance=50Europe | TDK EPCOS | B39162B9416K610 |
| | | | nsertion Loss =1.3dB@1561.098M<br>0.9dB@1575.42M , 1.4dB@1602M<br>impedance=50Ω | MURATA | SAFFB1G56KB0F0A |
| | | | Insertion Loss = 0.95dB@1575.42M<br>impedance=50Europe | | SAFEB1G57KE0F00 |
| | | | Insertion Loss = 0.9dB@1575.42M<br>1.3dB@1602M, impedance=50Europe | | SAFEA1G58KA0F00 |
| | | | Insertion Loss = 1.0dB@1575.42M<br>1.3dB@1602M, impedance=50Europe | WISOL | SFHG89DQ102 |

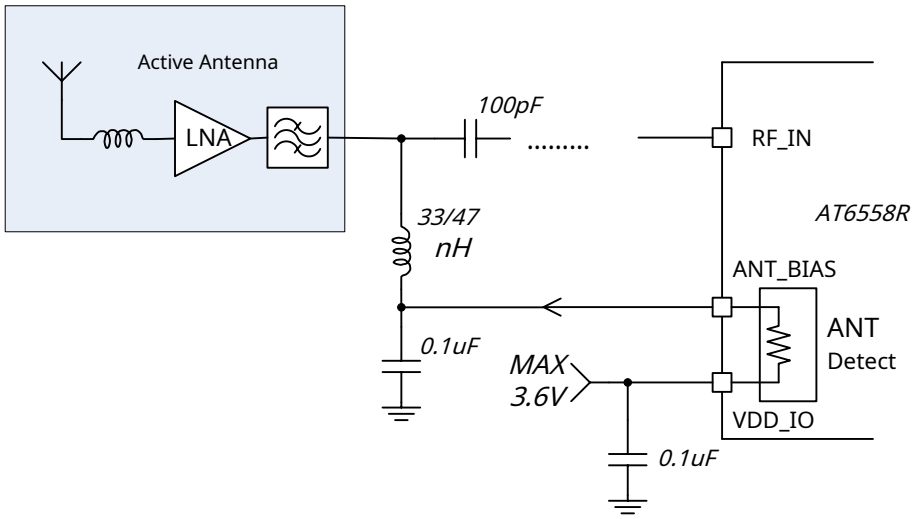
## 8 Application Schemes

### 8.1 Active Antenna Feeding and Detection

As shown in the figure below, the chip's active antenna detection circuit can detect the state of the active antenna, and the input is the systemIOPower supply, most High Voltage3.6V.ANT_BIASFeed the active antenna and connect one33nHor47nHThe inductance and0.1uFCapacitor filtering The inductor and capacitor are used to block AC signals.PCBIt should be close to the RF input terminal.

Note: Even if AC signal blocking is addedLCfilter, low frequency AC large signals may still feed through to ANT_BIASport, causing the detection circuit to misjudge. Especially in strong interference environments or near high-power transmitters, The probability of misjudgment will increase.

The default minimum detection current for antenna access is2.5mA, the short-circuit protection current limit default is50mA.




picture8.1Active Antenna Detection and Protection

## 8.2 RF Input Gain

The RF signal fromRF_ININput, external antenna unit (passive dielectric +LNA, or active antenna) is recommended to have a gain of 18~35dB.

### 8.3 Lightning Protection and ESD

The RF interface of the device is usually exposed, although this chip has beenHBM2000V ESDTesting, but in testing and using During use, strong impact may still cause chip damage; so please be careful during chip testing and use.ESDProtection, And add appropriateESDProtective design.

When the navigation antenna is placed outdoors, lightning protection design is also required.

### 8.4 Reference Clock Crystal

The frequency stability of the reference clock will greatly affect the performance of the receiver, including sensitivity, positioning accuracy, and timing.

Therefore, in order to obtain the best performance, it is recommended that users use a high-stability crystal oscillator.

It is the clock reference source of the navigation chip. It is recommended to select a frequency with an initial error less than2ppm,temperature-40℃~85Stability in °C range

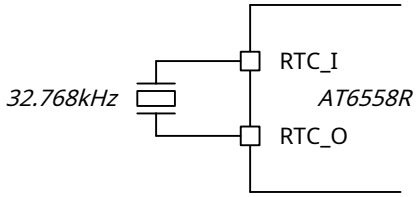
Less than0.5ppm, and a temperature compensated crystal oscillator that is insensitive to temperature and environmental vibrationTCXO.

## 9.5 RTC Clock

Real-time clock (RTC) is located in the backup battery power supply area to ensure backup after the main power supply failsRAMThe data in the

It can be quickly repositioned when the main power is restored.RTC OSCUse passive crystal, connected to the chipRTC_IandRTC_O

Pins, no external capacitors and feedback resistors are required, as shown below:

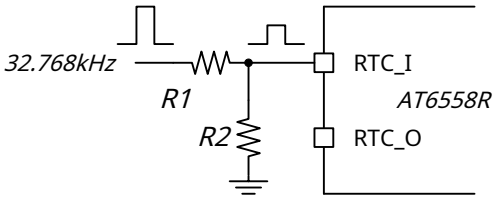



picture8.2 32k RTCPassive Crystal

The chip also supports direct clock input.***Note that the signal must be fromRTC_Ienter***, and ensure***RTC_I***The voltage on

Pass1.5VAs shown in the figure below, the clock signal is added to the***RTC_I***On, adjustR1andR2ratio,***RTC_I***Last time

The clock high level is1.2V.




picture8.3 32kDirect clock input (resistor voltage divider)

### 8.6 Power Management

Chip has2Ways to enter low power mode:

1) Close exceptBDD_BKAll power supplies except

2)WillON_OFFThe pin is set to low level. The chip enters a low-power sleep state and consumes very little current.

| Power Mode | | Kernel | IO/POR | LNA | TCXO | antenna | RTC | Main power supply |
|---|---|---|---|---|---|---|---|---|
| Full working mode | | √ | √ | √ | √ | √ | √ | ON |
| Low power consumption model | Power off | × | × | × | × | × | √ | OFF |
| | ON_OFFPull down | × | √ | × | × | × | √ | ON |

## 8.7 DCDC

If the system is not sensitive to power consumption, or to save the cost of inductors and capacitors, it can be omitted.DCDC.at this timeDCDClose It is recommended to leave the input and output pins floating.VCOREThe power supply can be1.4~3.6V.

On-chipDCDCIt can effectively reduce chip power consumption.

To reduceDCDCThe impact of switching noise on chip performance should be minimizedDCDCInductors and capacitors and pins DCDC_OUTThe connection length should be short and the device should be away from the RF signal input port and RF related components.

DCDCPower supply filtering at the input is very important and should be used2.2uFThe above capacitors, and filter capacitors as close as possible DX_INPin.

All filter capacitors should be well grounded.DCDCThe input filter capacitor is grounded, the output capacitor is grounded, and the chip bottom All metal parts must be fully and well grounded.PCBTrace width and number of vias.

## 8.8 LDO

Chip internal integrationLDO.

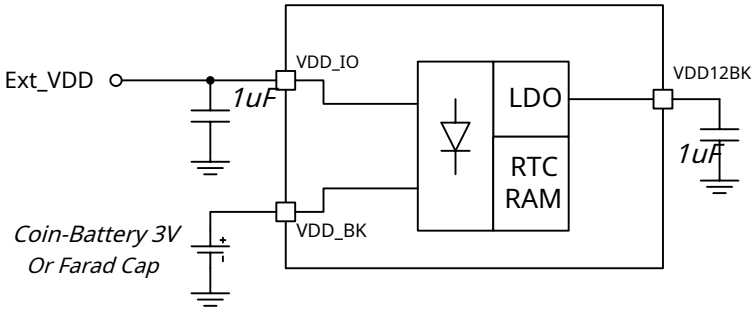
RF analog partLDOOutput likeVDD_ANA,VDD_RF,VDD_PLLThe bypass filter has high requirements.PCB When designing, please try to shorten the trace length between the bypass capacitor and the corresponding pin, and pay attention to the good grounding of the bypass capacitor.

### 8.9 Backup Power Supply

It is recommended to connect a rechargeable3VButton cell battery or Farad capacitor, provideRTCand backupRAMBackup power supply, To support hot start positioning. The chip has built-in trickle charging circuit and anti-reverse charging circuit. Note the maximum The charging voltage should be greater thanVDD_IO+0.3V.

If the system does not require hot start function,VDD_BKThe pin can be left floating; when the system is powered off,RTCand backupRAMDepend on If there is no power supply, it will stop working, the positioning information cannot be saved, and the hot start function will be invalid.

Note: Whether or not to add backup power supply,VDD12BKon1uFThe capacitors cannot be removed.




picture8.4Backup power connection diagram

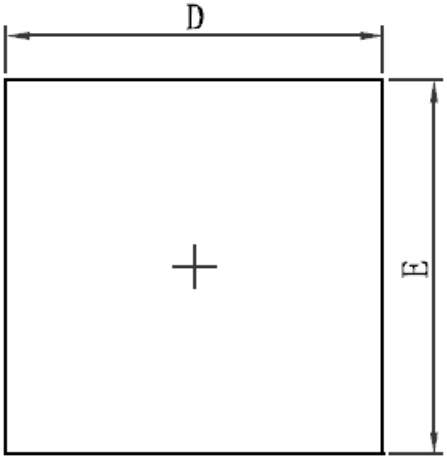
## 9 Chip packaging

9.1 Chip Identification Rules

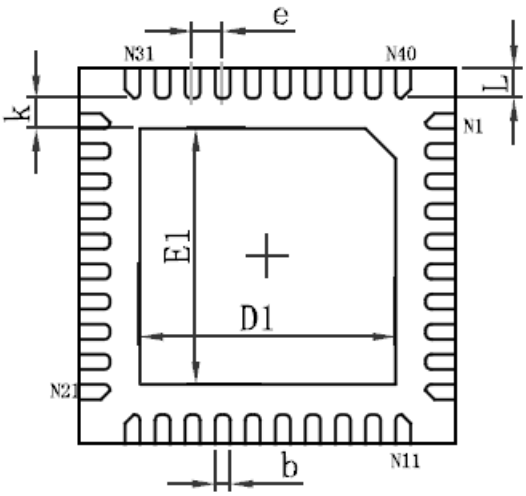

| coding | illustrate |
|---|---|
| AT6558R | Chip Model |
| LLLLLLLLLLL | Chip serial number |

10.2 Packaging Specifications

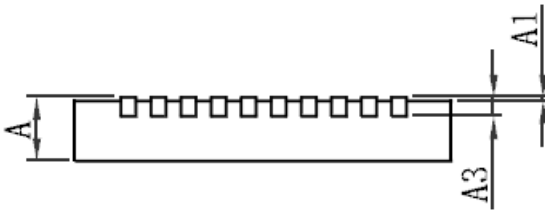
Chip AdoptionQFN5×5-40L（P0.4T0.8) package, and below are the package dimensions.




Top View




Bottom View




Side View

Package size

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.700/0.800 | 0.800/0.900 | 0.028/0.031 | 0.031/0.035 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.203REF. | | 0.008REF. | |
| D | 4.924 | 5.076 | 0.194 | 0.200 |
| E | 4.924 | 5.076 | 0.194 | 0.200 |
| D1 | 3.300 | 3.500 | 0.130 | 0.138 |
| E1 | 3.300 | 3.500 | 0.130 | 0.138 |
| k | 0.200MIN. | | 0.008MIN. | |
| b | 0.150 | 0.250 | 0.006 | 0.010 |
| e | 0.400TYP. | | 0.016TYP. | |
| L | 0.324 | 0.476 | 0.013 | 0.019 |

## 10 Chip welding and storage

10.1 Moisture resistance level:

Moisture Sensitivity Level (MSL):3class

MSLPlease refer toIPC/JEDEC J-STD-020standard.

### 10.2 Reflow Oven Curve:

**!Notice**

Adjust the equilibration time to ensure proper gas handling when the solder paste is melted.PCBThere are too many gaps on the board, you can increase

Balance time.

Considering that the product is placed in the welding area for a long time (temperature180℃ or above), in order to prevent damage to components and the base plate,

Keep placement time as short as possible.

**! Important features of the curve:**

Ascending speed =1~4°C /sec, 25°C to150°Caverage

Preheat temperature =140°C to 150°C, 60sec~90sec

Temperature Fluctuation =225°C to 250°C,About30sec

Falling speed =2~6°C/sec, to 183°C,About15sec

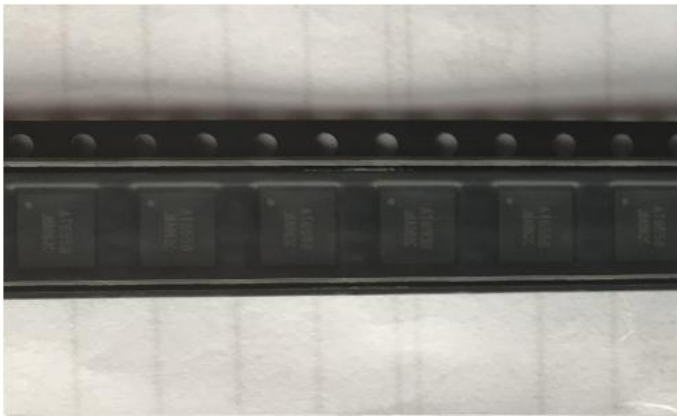
Total time = approx.300sec

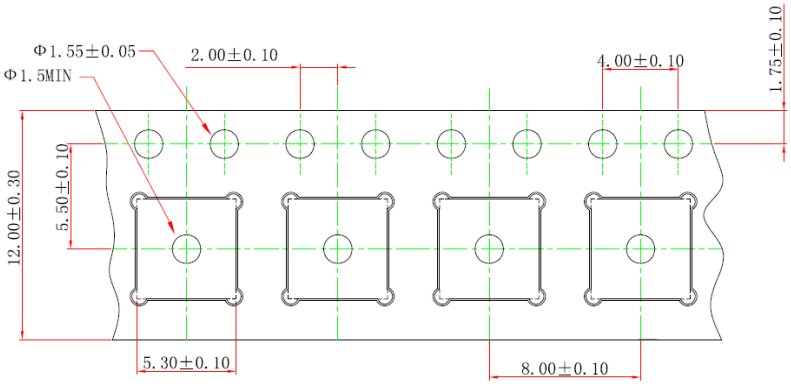
## 11 Packaging and Transportation

### 11.1 Packaging

The chip is packaged in vacuum tape and has moisture-proof and anti-static properties. The use process is compatible with major chip placement machines in the industry.

Minimum packaging1000Pieces/reel. Specific tape dimensions are as follows:






### 11.2 ESD Protection

Please pay attention to anti-static and moisture-proof during chip transportation and production.

**CAUTION!**ESD SENSITIVE DEVICE!

**Please pay attention to static electricity protection during use, packaging and transportation!**

## 12 Document update history

| date | Version | illustrate |
|---|---|---|
| 2018.03.29 | V0.1 | Document Drafting |
| 2018.08.22 | V1.0 | |
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