Application Note:

PCB Design Guidelines

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Introduction

This application note describes the main steps necessary to ensure correct PCB layout and design optimization. This is explained for each functional block of the RF integrated circuit architecture. Following these design principles will help achieve a correct first-time design with optimal radio performance that will pass the regulatory certification process.

This manual is split into two parts:

1. RF Design Guide:
    - Section 1 is a Quick Reference, which concisely illustrates the layout best practice.
    - Sections 2 and 3 give details about everything that is in the Quick Reference.
2. PCB Design Checklist: Section 4 is a checklist, to help the designer perform a sanity check prior to building the PCB.

The examples in this guide apply to all LoRa® radio and PCB radio layouts.

PART 1: RF Design Guide

1 Synopsys

1.1 RF Chain Overview

The schematic below describes the basic functionality of an RF chain. Most Semtech products have the same topology and have common blocks.

This example is an SX1261 EVK with an Xtal and DC/DC supply. Please refer to your reference design for the exact implementation.

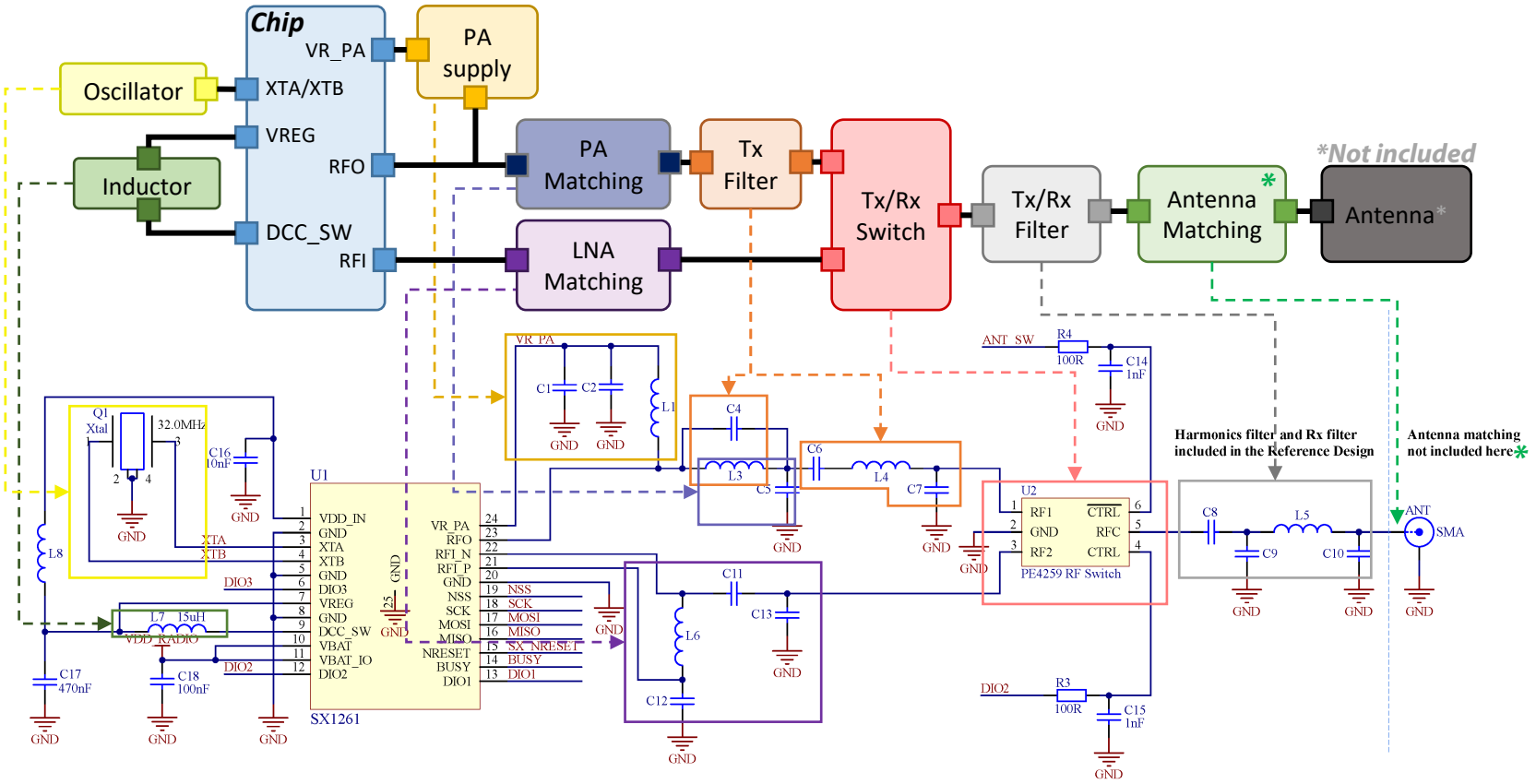
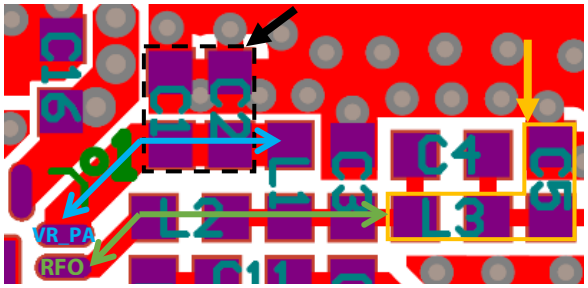


Figure 1: SX1261 Schematic Block Description

1.2 RF Components and Matching

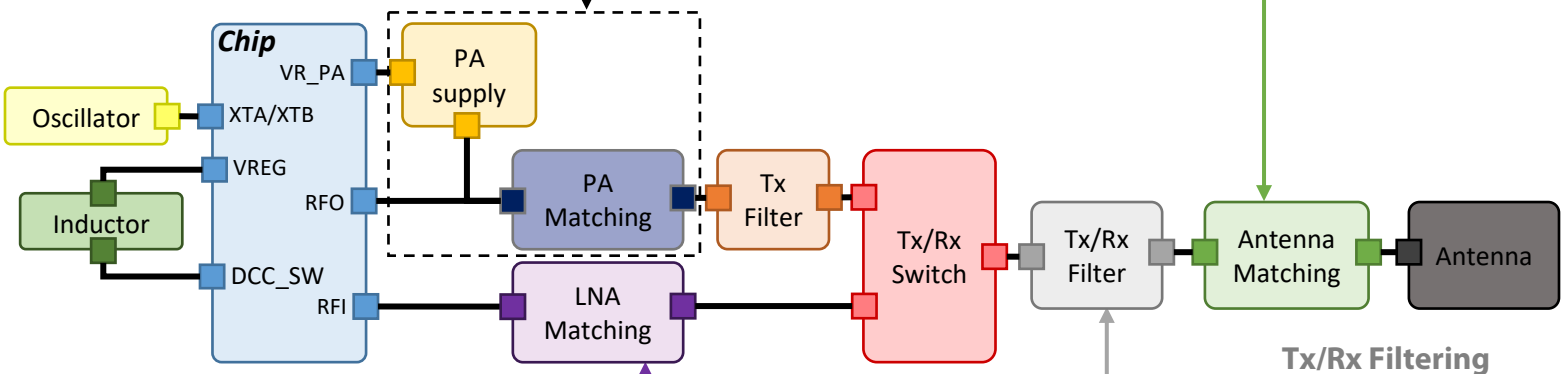
Tx PA matching and Supply



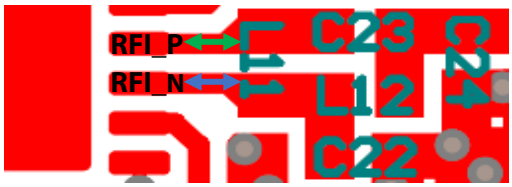
- The **PA supply path** VR_PA to the choke inductor L1 should be as short as possible.
- The PA Matching **L3/C5** should have the **shortest length** to the RF output possible.
- For **C1 and C2** refer to the reference design for implementation.

Antenna matching

- Add **footprints** for antenna matching, recommended.
- Add a **TVS diode** for ESD protection, if required.
- If possible, add an antenna connector for conducted measurements (UFL connectors are good in this role but must not create a stub when placed).



Rx Matching and differential input



- The whole RX balun must be placed close to the transceiver.
- The differential paths **RFI_N** and **RFI_P** should be as symmetrical as possible.

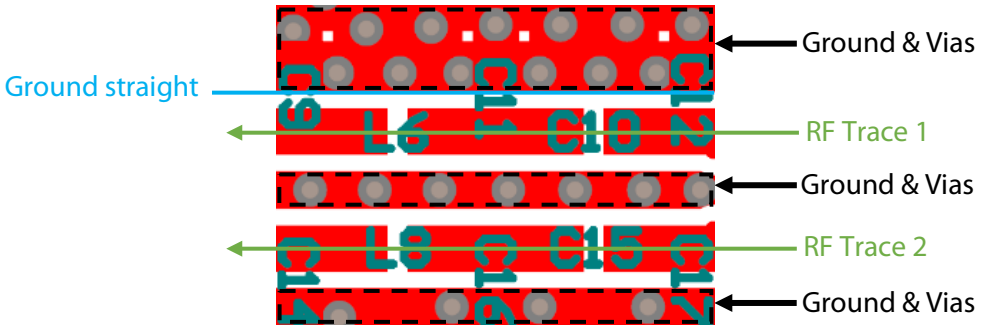
Tx/Rx Filtering

- Include a PI filter after the RF switch for the LR11xx and SX1261/2/8.

Figure 2: RF Components and Matching Layout

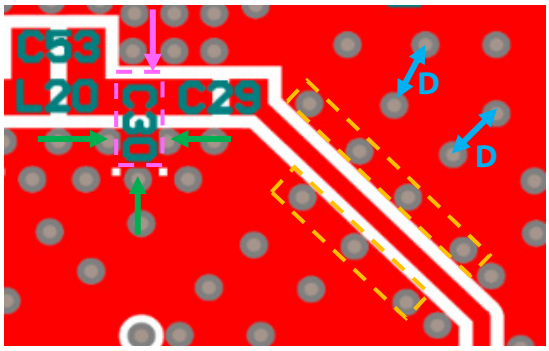
1.3 Vias, RF Line and Reference Oscillator

Ground shielding & RF line



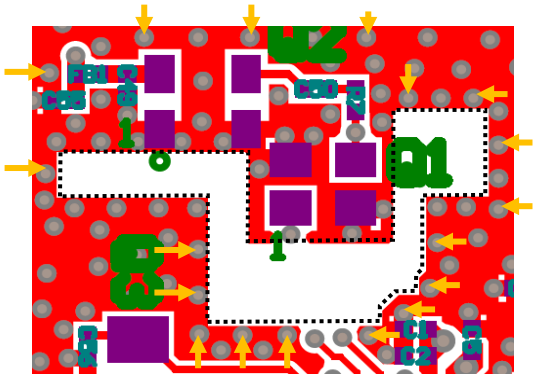
- **Ground plane with vias** should be added between separate RF paths.
- Ground plane should be present all along each side of the transmission line.
- The whole RF path should be on the same layer. Avoid vias in the RF path.
- The ground plane edge along all transmission lines must be **straight and without discontinuities**.
- RF lines must be as short as possible.
- Use 50 Ω line characteristic impedance to connect antenna.

Vias & RF lines



- All **shunt components** should have one pad directly connected to the RF line, and the other connected to the ground with ideally **3 ground vias** placed as close as possible to the shunt's pads.
- Vias must be stitched at a distance of at least **D = λ /20** on the ground plane.
- Vias must be added **close to the RF path**.
- Vias must also be implemented around the DC signal and the edge of the PCB.

Reference oscillator

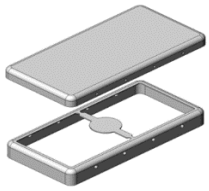


- If a crystal oscillator is used, **thermal reliefs** must be implemented.
- Ground and **vias** should be implemented around the crystal or TCXO, especially near Chip supply and VR_PA.
- For crystal or TCXO, refer to the reference design for implementation.

Figure 3: Vias, RF Line and Oscillator Layout

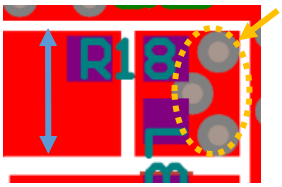
1.4 Miscellaneous

RF shield



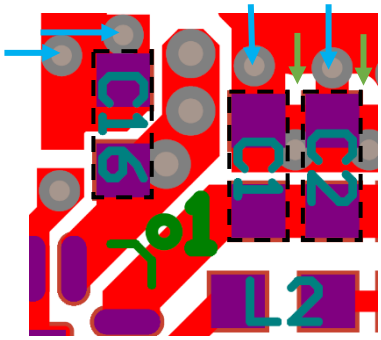
- Plan to add a shield on the RF area to prevent unwanted radiated emissions and to help pass RF certification testing.

Supply lines

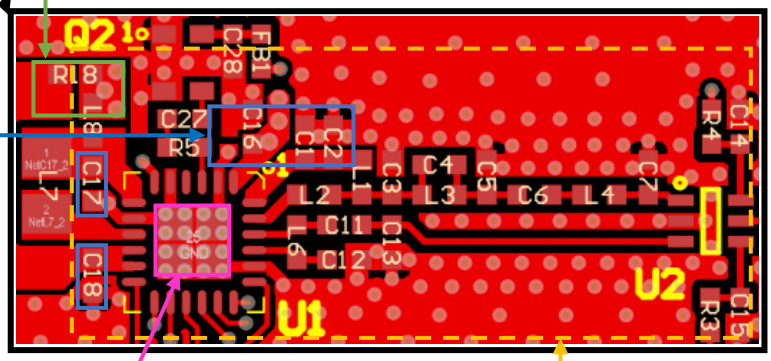


- Increase the **width** of VDD/GND lines when possible.
- Add several **vias** when changing layers.

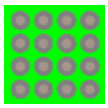
Decoupling capacitors



- Each **decoupling capacitor** for VDD/VBAT must be placed close to the chip.
- Each decoupling capacitor should have at least one or more **vias** to the ground.
- Decoupling capacitors and other components must have **thermal reliefs** for easy soldering.



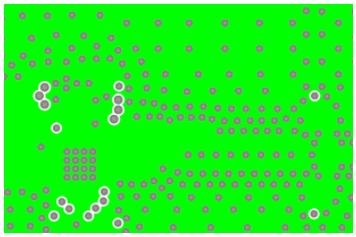
Exposed pads



- Refer to the reference design recommended package footprint to see how many vias there should be under the exposed pad of the chip.

Ground planes under RF

Layer below RF: Clear ground



- The layer below the RF shall be a clean ground plane.
- No trace routing is allowed under the RF path.
- Do not put any vias just below the RF path and ensure clean current return path.

Figure 4: Miscellaneous Layouts

1.5 Layers

PCB Stack-up

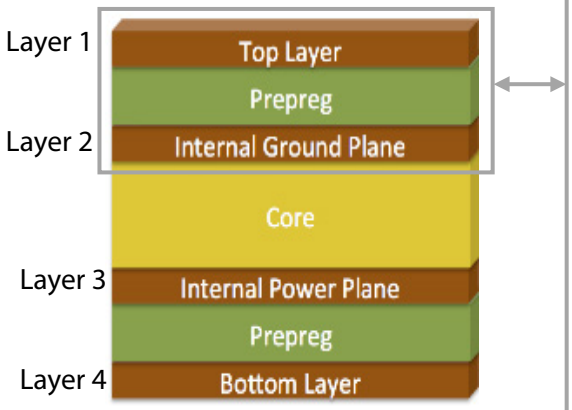


Figure 6: PCB Stack-Up

- Use of a 4-layer PCB is preferable to optimize RF PCB layout, especially if there is dense routing.
- For 4-layer PCBs, use one full layer for a clean ground plane below the RF.
- For 2-layer PCBs, do not cut the ground plane under the entire RF area.

50 Ω Characteristic Impedance for the RF Transmission Line

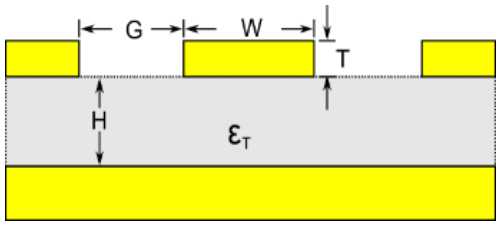


Figure 5: Coplanar Line Model

- *G, W, T, H* and *εr* must be determined to ensure 50 Ω with coplanar waveguide with ground - RF line.
- *W* line width parameter must be constant all along the RF path.
- If possible, W parameter should be the same width as your components' pads (not always possible).
- Free calculator software is available to define 50 Ω line characteristic impedance for the RF path of PCB designs.
  Free calculator software examples:
  - *leleivre.com/rf_coplanar_gb.html* (simple)
  - *wcalc.sourceforge.net/cgi-bin/coplanar.cgi* (advanced)
- *εr* is dependent on the substrate selected (e.g., FR4).

2 Good Layout Practice

The following sections describe in detail the best practices a PCB designer should follow for every design. Most of the recommendations are RF related, as this is the most critical aspect in ensuring the design objectives are met, but they impact the whole board design [1][2].

The goal of a low power radio PCB layout is to optimize the energy efficiency and maximize the RF performance of the device. At the PCB level this translates to minimizing RF path losses whilst preventing parasitic emissions (such as harmonics) to ensure radio regulatory compliance.

RF designers should follow a certain order of priority for the placement of components and PCB layout, as listed below:

1. Determine the necessary antenna gain, radiation pattern and product size needed by your application.
2. Choose your antennas with criteria above. The antennas choice and specifications determine the minimum size of your ground plane/PCB.
3. Start your PCB layout by placing the antennas first (GNSS antenna is the priority for the LR11xx), and then the antenna matching at the feed point.
4. Place the Semtech radio device.
5. Place all necessary decoupling capacitors close to the Semtech radio device.
6. Route all RF trace from the device to the antenna. Keep the ground plane under the RF full, without openings.
7. Route all other critical lines away from the RF, for example high-speed digital lines and reference high frequency clocks (32.0 MHz or 52.0 MHz).
8. Route all DC supply lines on a specific power plane, if possible.
9. Route all other analog or digital lines on the PCB.

2.1 Antennas

Antennas are often neglected during the PCB design phase, sometimes resulting in them being placed in unsuitable locations at the end of the design process [3]. This results in poor antenna characteristics and disappointing performance in the final application.

If an antenna is integrated in the product (PCB or ceramic antenna), most antenna manufacturers provide reference designs for their products, and you should follow their guidance.

Some external antennas (with a physical connector like an SMA) do not need a matching network. However, most antenna manufacturers still provide guidance on how to use their antenna.

Whether the antenna is external with a connector or integrated on the PCB (see Figure 7), a Pi or T section for antenna matching must be implemented at the antenna feed point (example below L18, C35, and L19). Even if the antenna is already matched to 50 Ω, its impedance is very likely to be detuned due to the actual PCB dimensions. Indeed, compared to the antenna reference design, the final product has some different ground/power planes shapes, product case or mechanical parts, etc.

This Pi or T section can thus be used to tune the antenna.

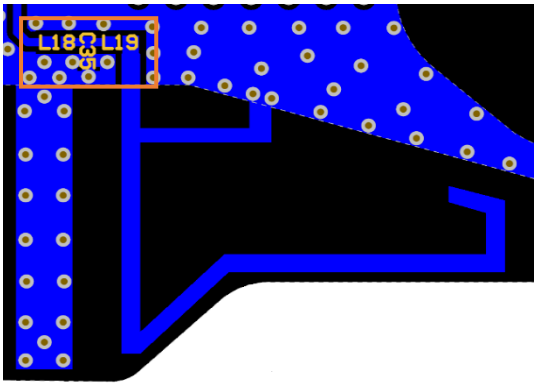


Figure 7: Antenna Integrated on PCB

For PCB prototyping with an integrated antenna, the designer should leave enough space, if possible, for a UFL or SMA connector close to the antenna feed point. This allows easier validation of the whole RF Tx or Rx chain with conducted measurements using a Spectrum Analyzer or an RF Generator. Furthermore, regulatory testing for some countries like Japan or Korea require conducted measurements.

Note for GNSS: Specific attention must be given to GNSS antennas whatever the antenna type with the LR11xx and LoRa Edge™ product families. GNSS path design is more sensitive than LoRa path design, therefore GNSS antennas should be placed in priority on the PCB and the maximum lobe of the radiation pattern should point at the sky [4].

2.2 Impedance Matching and Filtering

The whole RF path can be split into different blocks [5] . The goal of this section is to explain how to better integrate and understand these blocks.

Example: EVK LR11xx – LoRa RF Path: TX High power (HP) / TX Low power (LP)* / RX

* *As functionality is almost the same between HP and LP paths, blocks in the LP path are not represented.*

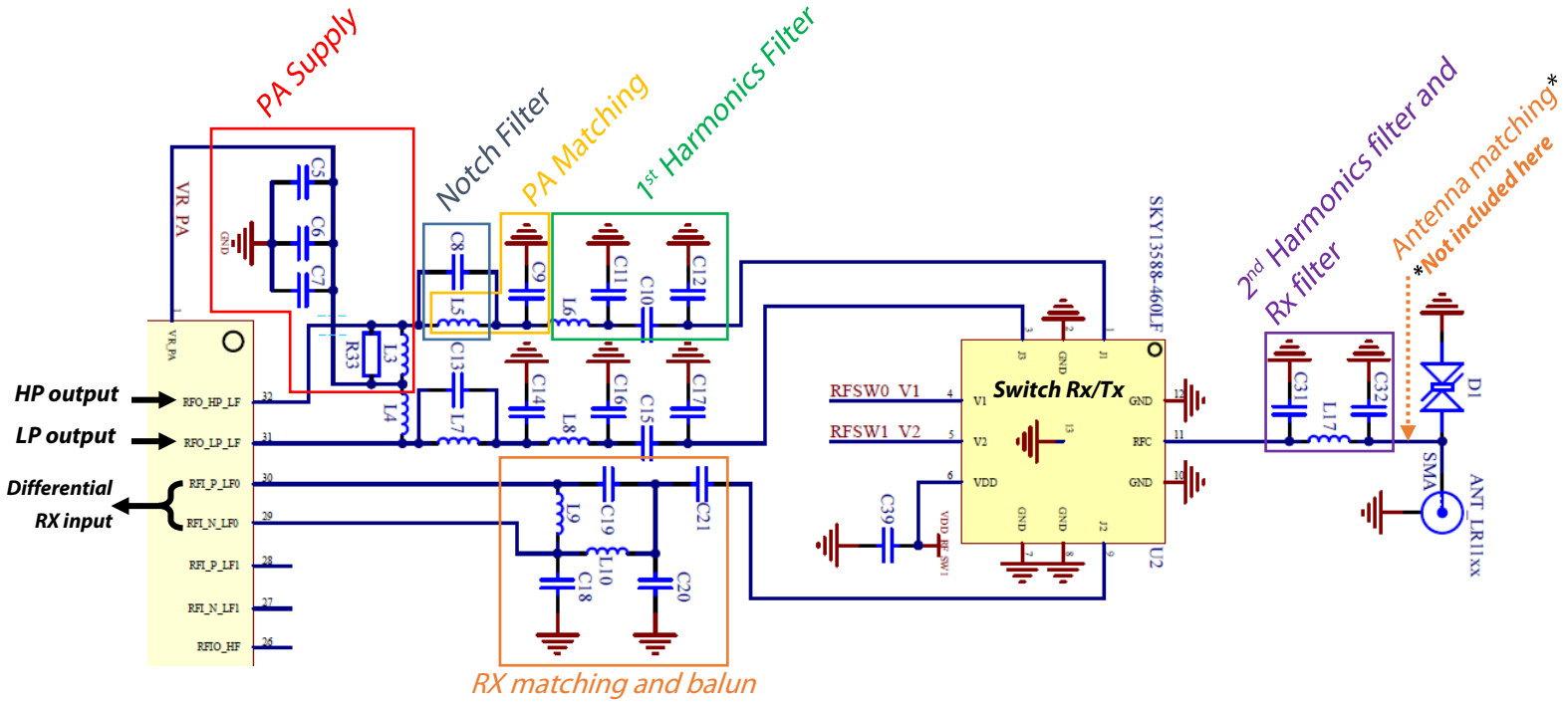


Figure 8: EVK LR11xx – LoRa RF Paths

- **PA Supply** (regulated): The DC power supply of the PA. Composed of decoupling capacitors for VR_PA and a choke inductor for each PA (High-Power and Low-Power PAs). For the LR11xx, it is advised to add a 200 Ω resistor footprint (R33) in parallel to the High-Power PA choke inductor L3.
- **Notch Filter**: Composed of a parallel L/C notch to reduce the H2 or H3 harmonic level (for the US or EU designs respectively).
- **PA Matching**: All RF components influence the global impedance present at the input of the PA, but these 2 components (L5 and C9 for HP PA) are the main influence for PA matching network.
- **1st Harmonic Filter**: Composed of a low pass filter and DC block, for harmonic attenuation and to protect the LR11xx DC bias.
- **2nd Harmonic Filter and Rx Filter**: This Pi section acts as a 2nd harmonics filter and as an Rx filter, to increase blocking immunity (mandatory for LR11xx & SX1261/2/8).
- **Rx Matching and Balun**: This cell makes a transformation from single-ended to differential transmission line and acts as the matching network for the LNA.
- **Antenna Matching**: Semtech does not give BOM values for this block, and they are not represented on the schematic above. Antenna matching network values should be optimized for each different frequency band and design. It is necessary to leave at least enough space for at least one T or Pi section. Between the antenna matching network and the antenna feed point, an additional TVS diode can be used to clamp to a safe voltage for ESD protection.
- **Power Modes**: Two power modes are available (not represented on Figure 8)
    - DCDC for low power applications, better efficiency for output power up to +14 dBm. The cost and space for two external inductors shall be included.
    - LDO for high power applications up to +22 dBm. The cost and space for two external inductors are spared.

2.2.1 PA Matching

This section introduces the PA matching good practice. In order to make a complete overview of Semtech products, two references are used for the demonstration: the SX126x and the LR11xx.

2.2.1.1 PA Matching SX126x

The SX126x family have the simplest integration of Semtech products.

The **PA matching** is performed mainly by L3 and C5 (see Figure 9). The **PCB trace length** between these two components and the PA output should be as short as possible.

A VR_PA regulated supply powers the PA. The choke inductor (L1) isolates the RF to VR_PA and must have a current rating >130 mA for SX1262 (+22 dBm) and >30 mA for SX1261 (+14 dBm) and shall have a voltage drop <100 mV. This choke inductor must be placed perpendicularly to the RF PA trace to avoid coupling. See the reference design and BOM for more details.

For SX126x devices, VR_PA line has two decoupling capacitors of **47 pF** (C1) and **47 nF** (C2). Even if VR_PA is a DC output, it is sensitive to the nearby environment (Oscillator, Radio RF output). The **VR_PA line** especially should be shielded with a ground plane and have vias around it. The VR_PA line at the output of the device to L1 should be routed on the 2nd internal layer below the Ground plane to improve immunity.

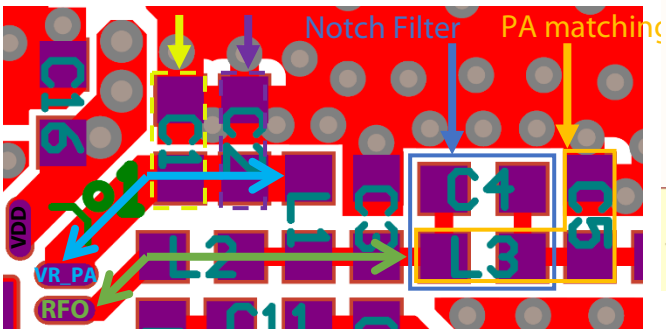


Figure 9: EVK SX126x - PA Matching PCB Layout

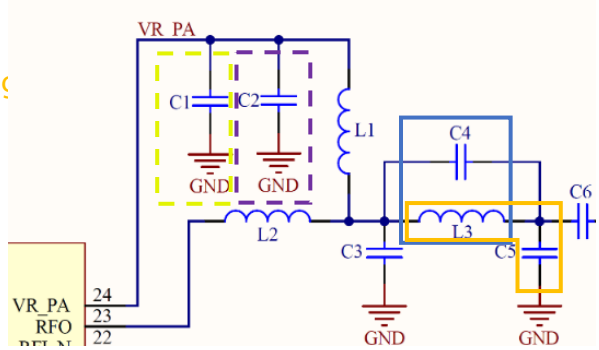


Figure 10: EVK SX126x - PA Matching Schematic

2.2.1.2 PA Matching LR11xx

The LR11xx has two PA outputs, one high power (HP) +22 dBm and one Low power (LP) +14 dBm. Most of the Semtech EVK reference designs implement both solutions in the same layout. For this reason, the RF output is quite busy near PA output. If the customer plans to use only one output power, it is recommended to put the whole RF matching as close to the device as possible.

The **PA matching** is performed mainly by L5 and C9 (see Figure 11). The **PCB trace length** between these two components and the PA output should be as short as possible.

A VR_PA regulated supply powers the PA. The choke inductor (L3) isolates the RF to VR_PA and must have a current rating >130 mA for high-power configuration (+22 dBm) and shall have a voltage drop <100 mV. This choke inductor must be placed perpendicular to the RF PA trace to avoid coupling. See the reference design and BOM for more details. To improve LR11xx PA stability, add a 200 Ω resistor footprint (R33) in parallel to the high-power PA choke inductor (L3).

For LR11xx devices, VR_PA line has two decoupling capacitors, a **47 pF** (C6) (68 pF for 490 MHz design) close to the choke inductor (C7 in the case of LP path) and a **2.2 nF** (C5) close to VR_PA output.

Even if VR_PA is a DC output, it is sensitive to the nearby environment (Oscillator, Radio RF output). The **VR_PA line** especially should be shielded with a ground plane and have vias around it. The VR_PA line at the output of the device to L3 can be routed on the 2nd internal layer below the Ground plane to improve immunity.

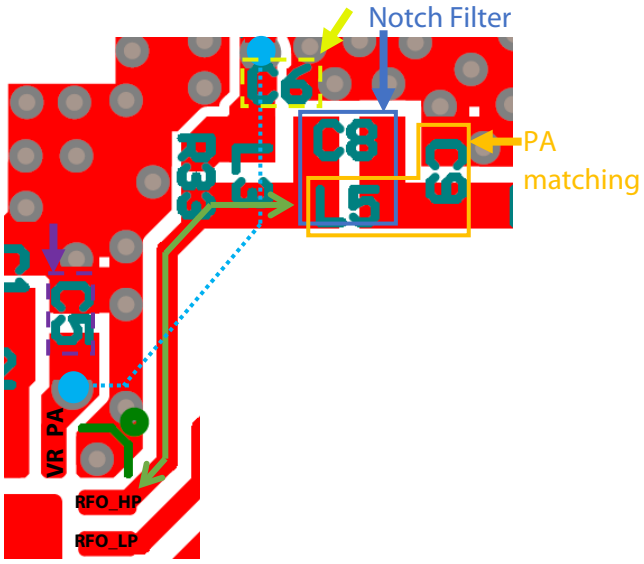


Figure 11: EVK LR11xx - PCB PA Matching

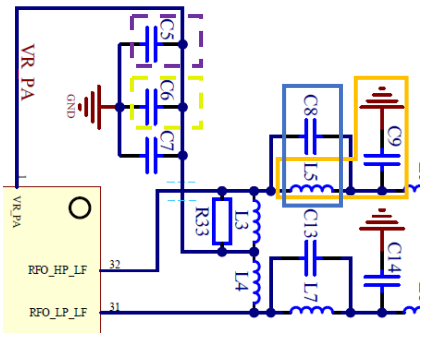


Figure 12: EVK LR11xx - PA Matching Schematic

2.2.2 RX Balun and Matching

Depending on the Semtech product, the RX input can be single ended or differential. C22, C23, C24, L11 and L12 (see Figure 14) act as an RX matching with a balun for the transformation from single to differential. The inductor L12 helps to improve the differentiability. Having L11 and L12 with high Q increase the matching gain.

Keeping a layout as symmetrical as possible helps to have a 180 ° phase shift between **RFI_P** and **RFI_N**.

All the discrete components of this Rx balun and matching should be integrated close to each other and close to the chip, in order to reduce mismatch, losses and parasitic capacitance, which reduce the overall matching gain.

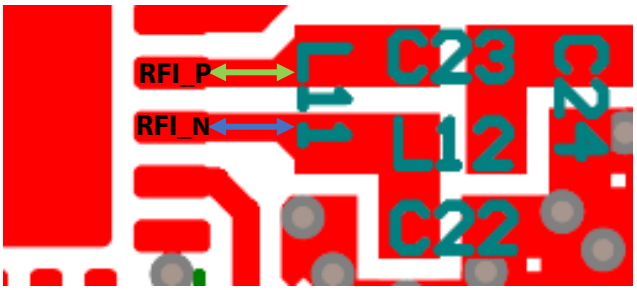


Figure 13: RX Input PCB Layout

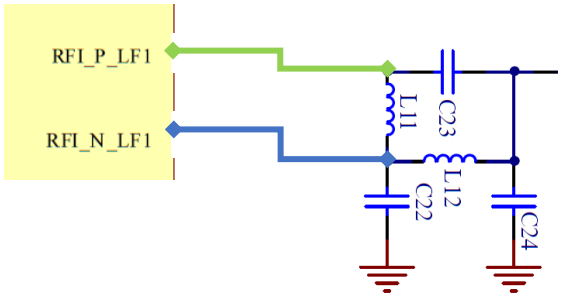


Figure 14: RX Input Schematic

2.2.3 Rx/Tx Filtering

There are three main filters on Semtech designs:

- A Tx filter between the device and the switch Tx/Rx.
- An Rx filter between the device and the switch Tx/Rx.
- A **common Tx/Rx** filter (mandatory for LR11xx & SX1261/2/8) between the **Tx/Rx switch** and the **antenna matching**.

Filters on the Tx path are necessary to reduce harmonic levels in order to be compliant with local radio regulation and certification (ex. FCC, ETSI). As the chip is using a switching PA, it generates a high level of spurious harmonic emissions. Some PA settings can reduce the harmonic levels [6], but filtering cells are necessary to lower harmonics below the mandatory level.

The common Rx/Tx filter is used in Tx to reduce high frequency harmonics (higher than harmonic 3), and used in Rx to increase blocking immunity. This filter is 50 Ω and symmetrical.

The common Rx/Tx filter must be implemented in addition to the antenna matching. As this filter is useful in Tx and Rx, it should be placed between the antenna matching and the output of the **Tx/Rx switch**.

Each Semtech product has a different BOM depending on the device and frequency used. Follow exactly the same BOM as the reference design, and keep the layout as similar as possible to the reference design layout.

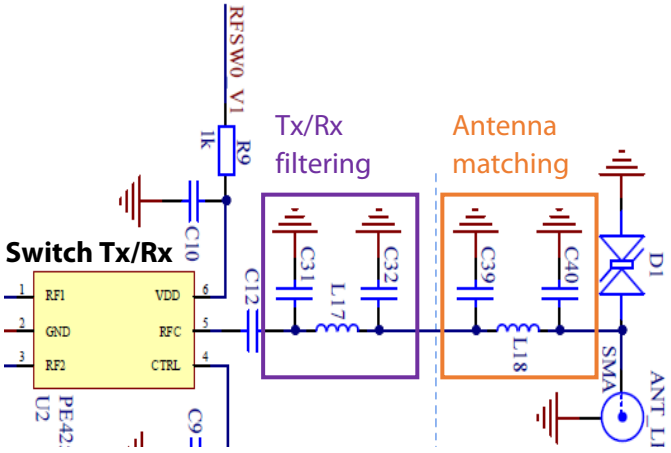


Figure 15: Rx/Tx Filter and Antenna Matching Schematic

2.3 RF Line Layout

Any RF line can potentially radiate or receive interfering signals. The section below describes all the best layout practices for a 50 Ω RF line to minimize EMC problems.

2.3.1 Theory

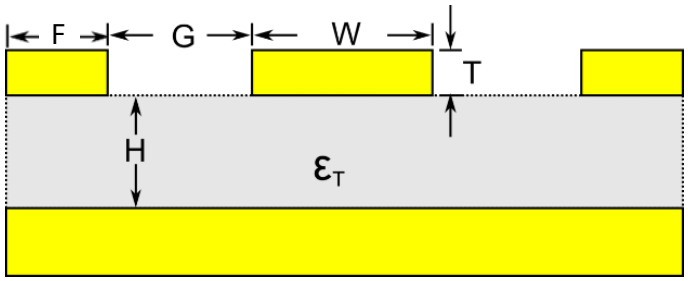


Figure 16: RF Line Layout

The RF trace between the antenna and the matching network should be designed using a grounded coplanar waveguide (GCPW) structure as shown Figure 16. The GCPW should be dimensioned to have a characteristic impedance equal to the antenna impedance, typically 50 Ω. However, it does not have to be 50 Ω inside a filtering cell or inside the PA matching network.

The parameters *G*, *W*, *T*, *B* and *H* determine the characteristic impedance of the GCPW, which can be calculated using many on-line tools. Examples of free tools can be found here:

- leleivre.com/rf_coplanar_gb.html (simplified model)
- wcalc.sourceforge.net/cgi-bin/coplanar.cgi (advanced model)

A perfect RF line without perturbation is a straight line; with static *G, W, T, H, F* and εr. Due to PCB limitations and RF components integration, *G* and *W* parameters will inevitably change and create some mismatch. The goal of the PCB designer is to keep these parameters as static as possible during the layout.

For GCPW, the width of the ground on each side of the RF line *F* must be larger than the width of the RF line *W* plus the gap *G* (*F* > *W* + *G*).

2.3.2 Ground and Via Stitching

Vias must be stitched **all along the RF path**, with a maximum distance of **D ≈ λ /20** between them, and as close as possible to the ground plane on the TOP layer.

Via stitching is also useful over the whole PCB near the DC supply and analog/digital sensitive lines. It is also vitally important that the edges of the PCB are stitched with a ground plane to help prevent the creation of inadvertent antennas.

A clean ground plane, in addition to via ground stitching, greatly reduces unwanted emissions and crosstalk between lines.

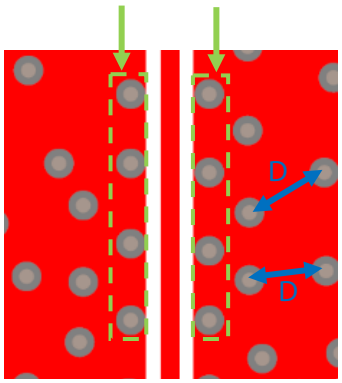


Figure 17: Vias around RF Path

Even if two RF lines are close to each other, they should be separated by some **ground** to avoid coupling, especially between **Tx** and **Rx** lines.

All other traces, like a power supply line, must not be used as a ground trace.

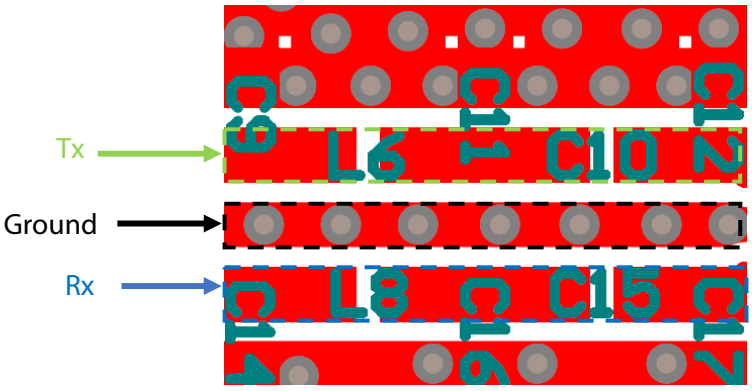


Figure 18: Ground Separation between 2 RF Lines

2.3.3 Shunt Components on the RF Path

All **shunt** components should have one pad directly connected to the RF line and the other connected to ground, with at least 1 via connected very closely to the ground. Ideally, a ground connection with **3 vias** is a good practice for clean current flow. Do not put a via directly in the center of a pad, to avoid surface-mount device assembly and soldering issues.

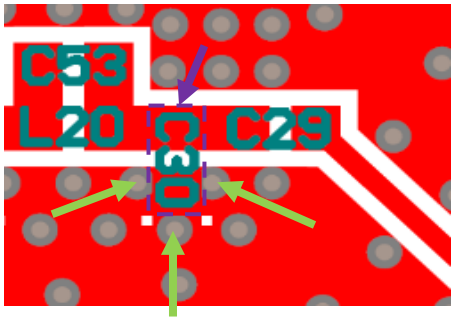


Figure 19: Shunt Component Vias

Each PCB trace that is perpendicular to the RF path, to connect a shunt component, acts as a transmission line stub and creates a mismatch. All shunt components on the RF path should be placed in-line with the RF path as illustrated below:

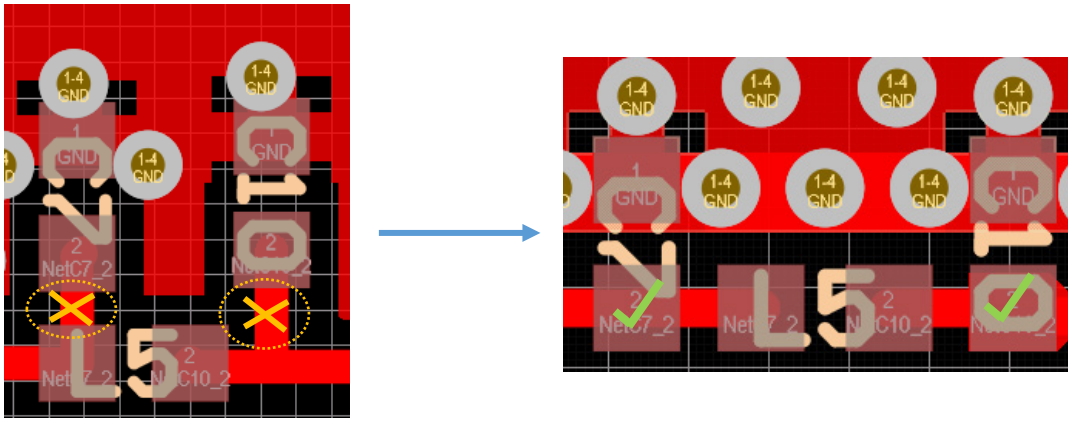


Figure 20: Incorrect (left) and Correct Way (right) to Connect a Shunt to Ground

2.3.4 RF Length and Direction

Corners on RF traces should be avoided if possible, and corners should be rounded (refer to Figure 21).

A smooth RF path is advisable to avoid RF signal radiation from right angles, and therefore may avoid radiated spurious emissions. All RF lines should be as short as possible to minimize insertion losses throughout the RF line and to reduce the impedance phase shift in the case of impedance mismatch.

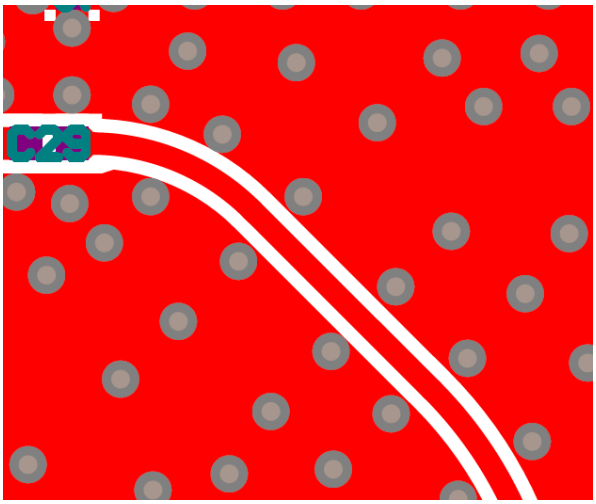


Figure 21: Curved RF Trace

2.3.5 PCB Ground

Ideally, a PCB of 4 or more layers should be used, with the RF signal routed on the top layer. The second layer should be reserved for ground, the third and fourth layers can be used for power and signal routing.

4-layer example:

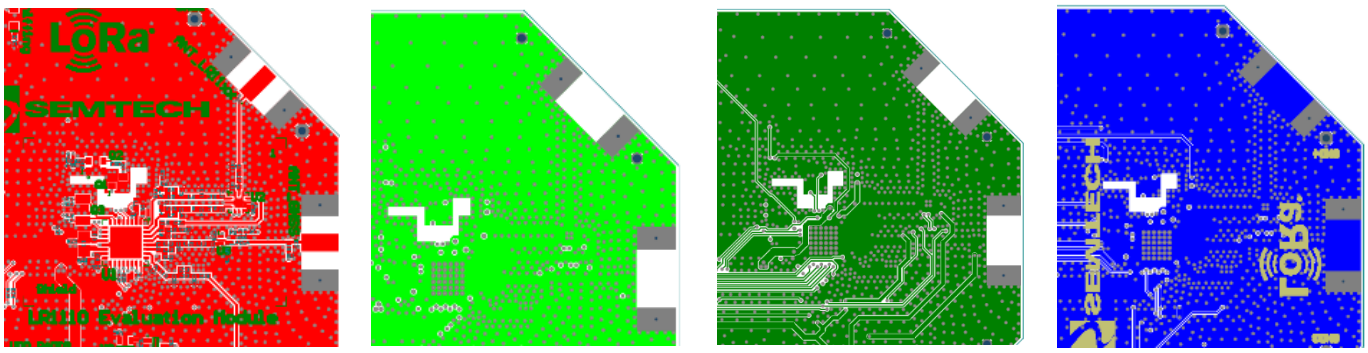


Figure 22: 1 RF (priority); 2 Clear Ground Below RF Portions; 3 and 4: Analog/Digital Line/DC Supply

A 4 (or more) layer PCB is recommended to optimize RF PCB layout, with more layers added if the routing is too dense.

Extra costs are not always significant compared to 4 layers, taking into account the benefits of obtaining a cleaner RF layout, avoiding the risk of failing regulatory certifications and thus reducing the regulatory testing costs, and ultimately ensuring a shorter time to market. In any case, whether it is a 2-layer or a 4-layer PCB, the ground under the RF section should not be cut or made into islands

In multi-layer PCBs, placing noisy signals like clock traces between two ground layers can avoid many radiation problems. Avoid overlapping power planes in multi-layer boards because noise easily couples between the different supply domains.

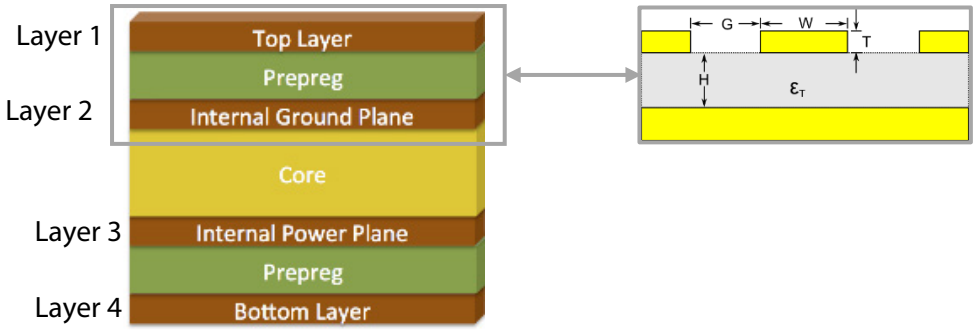


Figure 23: 4-Layer Example

2.4 DC Line and Decoupling Capacitors

Place decoupling capacitors as close as possible to the DC supply pad of the device, with at least one or more **vias** connected to the ground, which should also be close to the pad. Vias shall not be shared between pins or pads (avoid soldering issues during assembly).

Implement **thermal relief** close to decoupling capacitors, to facilitate assembly and soldering.

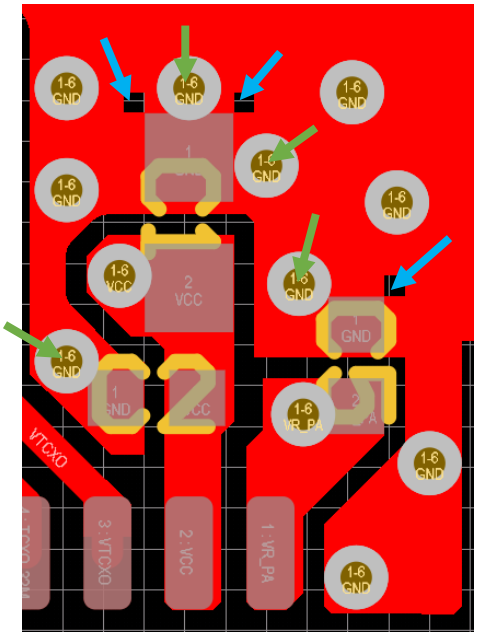


Figure 24: DC Line Vias and Thermal Relief

For DC lines with a high current rating, like power supply, serial impedance can be reduced by increasing the **width** of the line and adding **several vias** when changing layers.

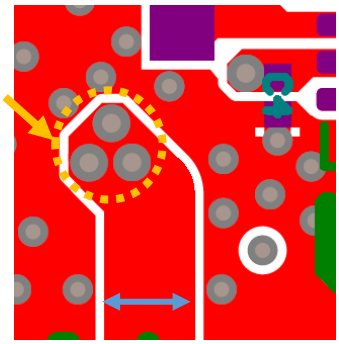


Figure 25: DC Line Width and Vias

2.5 Reference Oscillator

Semtech provides various Application Notes to help the RF designer choose between a crystal and a TCXO [7][8][9].

The crystal/TCXO needs to be isolated from the RF path. The 32 MHz may disturb other analog/digital lines, so the crystal/TCXO must be shielded with ground and vias all around it. Special attention is needed to protect VR_PA/VDD_IN (pin device close to C1, C2, C5 in the image below) which must be correctly grounded with **vias**.

In the image below, the footprint gives a free choice to use either TCXO or crystal.

If a crystal is used, a **thermal relief** is mandatory to protect the crystal against heat and to reduce frequency drift:

- The XTA and XTB lines to the crystal should be routed in an inner layer of the PCB, and with the minimum allowed width. Those two lines should not be routed too close to each other (respect XTA to XTB pitch of the device package).
- The total length of those lines needs to be at least 2.5 mm (increase thermal isolation).
- The ground cut opening between the device and the crystal should be at least 2 mm, and at least 1 mm further away from the device.
- The perimeter of the ground cut should be equivalent or larger than that proposed in Semtech's reference design.

Refer to the respective reference design for implementation examples. It is important to respect the overall perimeter of the thermal relief to reduce heat propagation from the device to the crystal.

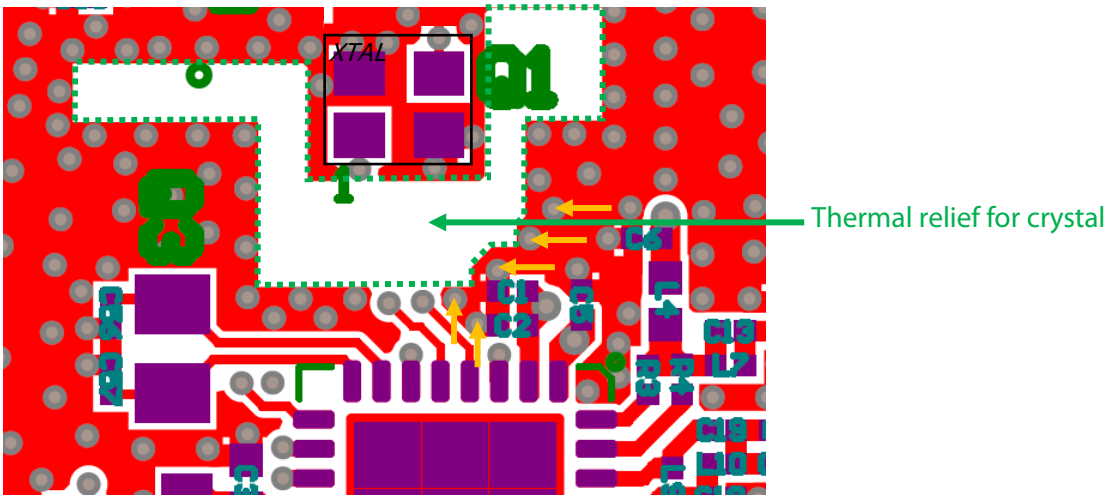


Figure 26: XTAL Implementation

- If a TCXO is used, no thermal relief is required. However:
    - A **ferrite bead** is needed on the supply to the TCXO.
    - A **serial capacitor** and a **serial resistor** are mandatory on the XTA output, in order to lower the TCXO amplitude and make it compliant with the Semtech device (only for the LR11xx & SX1261/2/8 & SX1250). Refer to Semtech reference design for exact values.

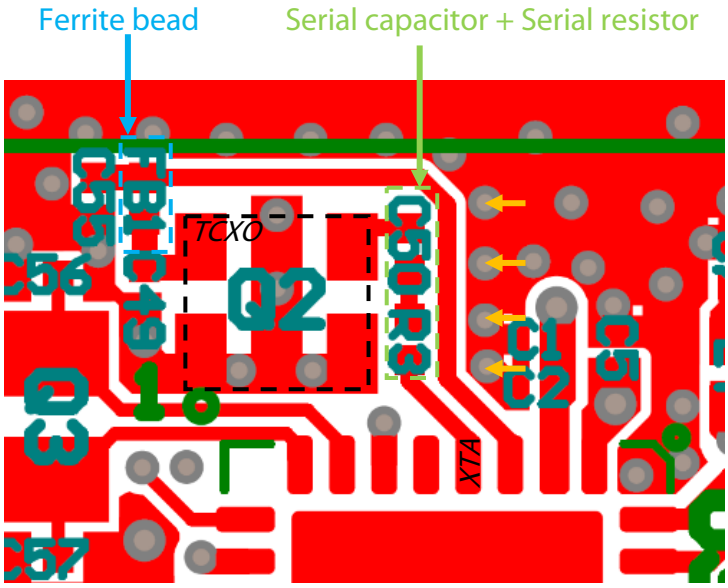


Figure 27: TCXO Implementation

2.6 External GNSS LNA

Reference designs provided by Semtech can have two different implementations on the GNSS path:

- **Active antenna**: Since an active antenna already integrates a GNSS LNA, there is no need to implement an external LNA. However, the RF line of the GNSS path requires an external power supply.
- **Passive antenna**: An external LNA Infineon BGA52N6, shown in Figure 28, is present on the GNSS RF to allow optimum sensitivity in passive antenna implementations.
  The LNA supply must have a decoupling capacitor **C58** (>10nF) close to the VCC pin.
  An Input matching **L14** and **C54** must be implemented close to the LNA.
  The LNA is controlled by the host or the LR11xx itself. However, Semtech recommend driving the LNA thru a MOS between VBAT and LNA VCC to guarantee a clean and stable supply.
  The LNA control and LNA supply line must be routed away from any noise source.

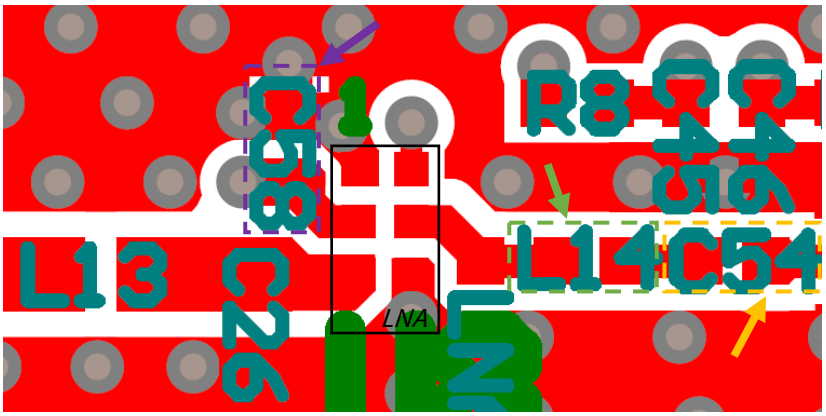


Figure 28: External LNA Implementation

3 EMC

Electromagnetic compatibility is the propensity of a circuit to not cause interference to other electronic systems and the immunity of that device from electronic noise [10][11]. Many points regarding EMC were already raised in previous sections; however, please consider the following additional advice.

3.1 Current Loop

Current flowing in a loop in digital or RF lines generates unwanted emissions and can disrupt nearby lines. This kind of behavior is like that of a wire-wound inductor, which is why two inductors that are close together should be placed at 90° relative to each other to avoid coupling between them.

This loop behaves like an antenna, whose radiating efficiency increases up to 1/4 wavelength of the frequency of interest. As soon as the length of one of the loops reaches 1/4 wavelength, more radiation is emitted.

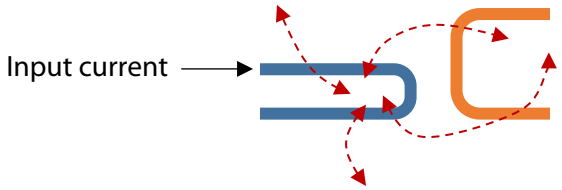


Figure 29: Current Loop

At 915 MHz, 1/4 wavelength is about 8 cm.

3.2 Connectors

Do not populate anything in the area close to the connectors, except protection components. High coupling phenomena build up in this area because the connector lines are so close to each other.

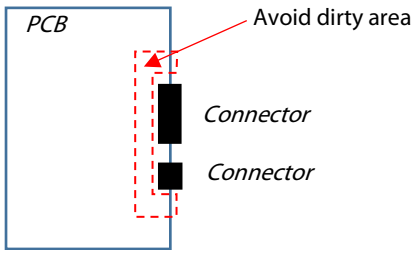


Figure 30: Connectors

Group connectors by function, and separate the analog, digital and RF connectors.

Improve cable immunity by adding more ferrites and decoupling capacitors. Make them short and fixed. Twist power/signal cables with the corresponding GND cable to compensate both electromagnetic fields.

3.3 Return Path

Via stitching is very often used to stop unwanted radiated emissions and to immunize against local radiated environments. However, vias should be placed with care; messy vias could be an issue for current return paths.

When creating a trace for DC and RF signals, you must make a clean return path and avoid areas of high impedance (groups of vias, gaps).

The trace should be as close as possible to the ground trace. The best choice is to design them in parallel on two different layers.

Figure 31: Incorrect (left) and Correct (right) Return Current Paths

PART 2: PCB Design Checklist

4 PCB Design Checklist

This chapter helps the designer to self-evaluate his own design. As the design progresses, the lists in these sections need to be ticked off.

Test number	Test description	Validate
X	[…]	☐

It is not necessary to have 100 % of conditions met. Indeed, due to final product integration, some points cannot be integrated. However, getting as close as possible to ticking all these points ensures you have the best possible performance.

In complement to this checklist, Semtech also provides a free PCB review service to help obtaining the right design first time.

4.1 Application Form

Semtech can provide a design review for customers. When the PCB review is submitted, the following information must be provided:

- Project Name
- Date
- Reviewers
- Chip and Frequency used

Customers must imperatively provide the following documentation:

- Schematic
- Layout (PDF or Gerber)
- PCB stack up layers
- BOM
- Design check list filled
- Final product overview (Battery type and position, Antennas type, Case, final environment usage)

4.2 Transmission Line

1	Transmission lines are microstrip or coplanar. The 50 Ω characteristic impedance is respected all along the RF path (confirmed with an impedance calculator).	☐
2	The 50 Ω impedance is constant throughout the trace (Filtering cellule and PA matching are not concerned).	☐
3	The RF trace width is constant. For a coplanar line, the gap between the RF trace and the adjacent ground is constant.	☐
4	For coplanar waveguide, the width of the ground on each side of the RF line *F* must be larger than the width of the RF line *W* plus the gap *G* (*F* > *W* + *G*).	☐
5	RF traces are short as possible (the traces and the substrate below attenuate the RF signal proportionally to the length).	☐
6	RF traces have no stubs or branching (no test points forming a stub on the RF trace).	☐
7	RF traces all on the same layer (avoid vias on RF lines).	☐
8	RF traces close to each other are separated by ground and vias (avoid mutual coupling of the signals between traces).	☐

4.3 Ground Plane

1	Except for the crystal thermal cut, the ground beneath the RF is full ground plane, uninterrupted and without any other traces or vias crossing the RF trace (to allow a proper return path for the RF currents, and reduce coupling).	☐
2	Unused areas in the top and bottom layers are filled with ground.	☐
3	All ground areas of different layers are connected with many vias (spaced at not more than λ/20).	☐
4	Full and solid ground planes (not split), except in the thermal cut zone.	☐
5	Noisy traces are well shielded (surrounded by ground + vias).	☐
6	Corners of the power plane are covered with vias to ground.	☐

4.4 Decoupling Capacitor

1	All decoupling capacitors are as close as possible to the supply pin.	☐
2	Smallest-value capacitors are closest to the supply pin. (Does not apply for PA power supply VR_PA)	☐
3	Decoupling capacitors are on the same layer as the IC.	☐
4	Each decoupling capacitor has its own via to ground	☐

4.5 Inductors

1	Inductors are not placed in parallel and not close to each other (reduce mutual inductance).	☐
2	Inductors or unrelated sections are placed orthogonal to each other.	☐
3	Inductors are only high-Q.	☐

4.6 Vias

1	Vias for ground are not spaced by more than λ/20.	☐
2	Shunt elements to the ground have ideally 3 vias placed immediately next to pins/pads.	☐
3	Multiple vias are used on DC line with high current rating (reduce serial inductance).	☐
4	Vias are not shared between pins or pads (avoid soldering issues during assembly).	☐
5	There is the good number of vias below the IC (improve heat dissipation).	☐
6	Vias stitching is very close to the RF section.	☐

4.7 Oscillator

1	Capacitors are only C0G/NP0 series.	☐
2	Oscillator and clock signal are shielded with vias and ground all around, except in the thermal cut zone (for crystal oscillator only).	☐
3	In the case of crystal oscillator, clock signal XTA/XTB are not too close from each other. The clock signal length is more than 2.5mm.	☐
4	In the case of a crystal oscillator, a thermal relief of the same size as the reference design is implemented.	☐
5	In the case of TCXO, there is a serial capacitor and a serial resistor in the TCXO output.	☐

4.8 Matching Network

1	RF Capacitors are C0G/NP0 series.	☐
2	RF Capacitors operate well below their series resonant frequency (SRF).	☐
3	RF Capacitors have high-Q.	☐
4	Small components (0402 or 0201) used (to have less parasitic reactance).	☐
5	For a DC block on an RF trace that is already matched, the capacitor has an SRF close to the frequency of operation and a low Equivalent Series Resistance (ESR).	☐
6	Inductors are only high-Q with a SRF well above the operating frequency.	☐
7	In TX, the Matching network is placed close to the chip (long length between the chip and matching network is equivalent to add a serial inductor).	☐
8	In RX (differential), the length between RFI_N and the inductor is the same as the length of RFI_P and the inductor (as short as possible).	☐
9	All the BOM is identical to the reference design	☐

4.9 Power Supply Filtering

1	In case of need, inductors are used with an SRF close to the noise frequency.	☐

4.10 Product Specific

4.10.1 LR1110

1	The GNSS LNA is placed as close as possible to the antenna (reduce NF).	☐
2	VR_PA line has two decoupling capacitors, a 47 pF (68 pF for 490 MHz design) close to the choke inductor (C7 in the case of LP path) and a 2.2 nF close to VR_PA output.	☐
3	If HP PA is used (+22 dBm), a 200 Ω resistor is in parallel with the choke inductor (improve PA stability).	☐
4	A 32 kHz crystal or signal line is present (mandatory for Basics Modem-E)	☐

4.10.2 LR1120

1	The GNSS LNA is placed as close as possible to the antenna (reduce NF).	☐
2	VR_PA line has two decoupling capacitors, a 47 pF (68 pF for 490 MHz design) close to the choke inductor (C7 in the case of LP path) and a 2.2 nF close to VR_PA output.	☐
3	If HP PA is used (+22 dBm), a 200 Ω resistor is in parallel with the choke inductor (improve PA stability).	☐

4.10.3 SX126x

1	VR_PA line has two decoupling capacitors of 47 pF and 47 nF	☐

4.10.4 SX1280

1	There is provision of serial footprint on the SX1280 SPI line. If there is high level of unwanted radiated emission, several kilo ohms are used to reduce signal edge and so unwanted emission	☐

5 References

[1] **Bowick** - RF Circuit Design Paperback – 21 November. 2007

[2] **Henry W. Ott** – Noise reduction techniques in electronic systems – 1988

[3] **Linx** --AN-00501 - Understanding Antenna Specifications and Operation – 20 August 2012

[4] **Semtech** – AN 1200.69 GNSS Antenna Performance Optimization

[5] **Semtech** - AN 1200.40 Reference Design Explanation – May 2018

[6] **Semtech** - AN 1200.32 designing for high efficiency and low harmonic emissions – July 2017

[7] **Semtech** - AN1200.59 Selecting the Optimal Reference Clock – April 2022

[8] **Semtech** - AN 1200.14 LoRa Modulation crystal oscillator guidance – July 2017

[9] **Semtech** - AN 1200.37 Recommendations for best Performance – January 2018

[10] **Mark I. Montrose** - EMC and the Printed Circuit Board: Design, Theory, and Layout Made Simple – 1999.

[11] **Mark I. Montrose** - Printed circuit board design techniques for EMC compliance: a handbook for designers - 2000.

6 Revision History

Version	ECO	Date	Changes and/or Modifications
1.0	060217	January 2022	Initial Version
1.1	063557	September 2022	Add “External GNSS LNA” section

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