

# PCA9557 Remote 8-Bit I<sup>2</sup>C and SMBus Low-Power I/O Expander With Reset and Configuration Registers

## 1 Features

- Low standby current consumption of 1µA maximum
- I<sup>2</sup>C to parallel port expander
- Operating power-supply voltage range of 2.3V to 5.5V
- 5V Tolerant I/O ports
- 400kHz Fast I<sup>2</sup>C bus
- Three hardware address pins allow for use of up to eight devices on I<sup>2</sup>C/SMBus
- Lower-voltage higher-performance migration path for PCA9556
- Input and output configuration register
- Polarity inversion register
- Active-low reset input
- Internal power-on reset
- High-impedance open drain on P0
- Power up with all channels configured as inputs
- No glitch on power up
- Noise filter on SCL or SDA inputs
- Latched outputs with high current drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22
  - 2000V Human-body model (A114-A)
  - 200V Machine model (A115-A)
  - 1000V Charged-device model (C101)

## 2 Applications

- Telecom shelters: filter units
- Servers
- Routers (telecom switching equipment)
- [Personal computers](#)
- [Personal electronics](#)
- [Industrial automation](#)
- Products with GPIO-limited

## 3 Description

This 8-bit I/O expander for the two-line bidirectional bus (I<sup>2</sup>C) is designed for 2.3V to 5.5V V<sub>CC</sub> operation.

The device provides general-purpose remote I/O expansion for most microcontroller families through the I<sup>2</sup>C interface [serial clock (SCL) and serial data (SDA)].

The PCA9557 consists of one 8-bit configuration (input or output selection), input port, output port, and polarity inversion (active-high) registers. At power on, the I/Os are configured as inputs. However, the system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. All registers can be read by the system controller.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

The system controller can reset the PCA9557 in the event of a timeout or other improper operation by asserting a low in the active-low reset (RESET) input. The power-on reset puts the registers in their default state and initializes the I<sup>2</sup>C/SMBus state machine. Asserting RESET causes the same reset/initialization to occur without depowering the part.

Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I<sup>2</sup>C address, allowing up to eight devices to share the same I<sup>2</sup>C bus or SMBus.

### Package Information

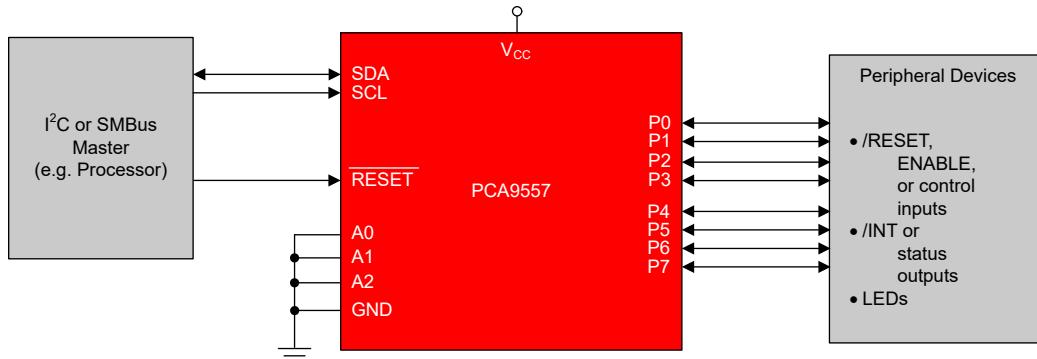
| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> |
|-------------|------------------------|-----------------------------|
| PCA9557     | D (SOIC, 16)           | 9.9mm × 6mm                 |
|             | DB (SSOP, 16)          | 6.2mm × 7.8mm               |
|             | DGV (TSSOP, 16)        | 3.6mm × 6.4mm               |
|             | PW (TQFP, 16)          | 5mm × 6.4mm                 |
|             | RGY (VQFN, 16)         | 4mm × 3.5mm                 |
|             | RGV (VQFN, 16)         | 4mm × 4mm                   |

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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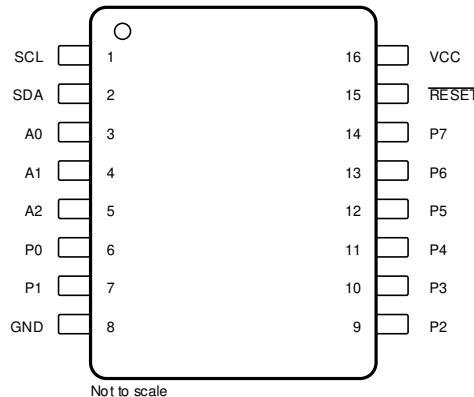


Logic Diagram

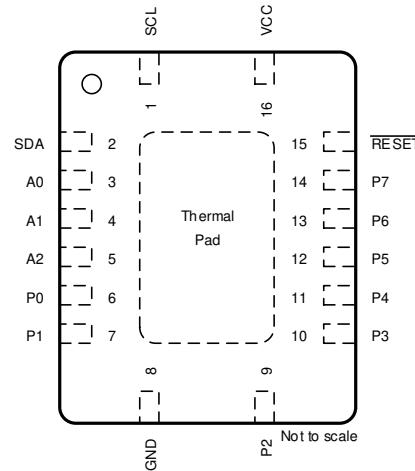
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## 4 Pin Configuration and Functions



**Figure 4-1. D, DB, DGV, PW Package, 16-Pin SOIC, SSOP, TVSOP, or TSSOP (Top View)**

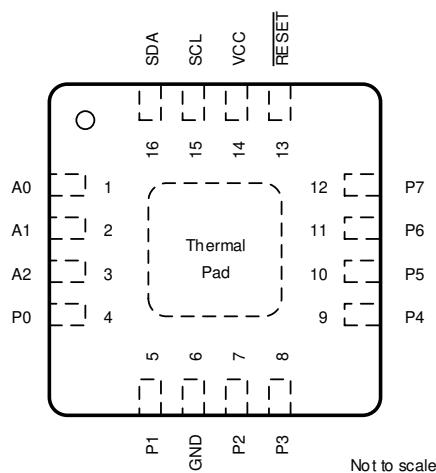


**Figure 4-2. RGY or RGV Package, 16-Pin VQFN or VQFN (Top View)**

**Table 4-1. Pin Functions**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----------------|-----|---------------------|--|
| NAME            | NO. |                     |  |
| SCL             | 1   | I                   | Serial clock bus. Connect to V <sub>CC</sub> through a pullup resistor.  |
| SDA             | 2   | I/O                 | Serial data bus. Connect to V <sub>CC</sub> through a pullup resistor.   |
| A0              | 3   | I                   | Address input. Connect directly to V <sub>CC</sub> or ground.  |
| A1              | 4   | I                   | Address input. Connect directly to V <sub>CC</sub> or ground.  |
| A2              | 5   | I                   | Address input. Connect directly to V <sub>CC</sub> or ground.  |
| P0              | 6   | I/O                 | P-port input/output. High impedance open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| P1              | 7   | I/O                 | P-port input/output. Push-pull design structure  |
| GND             | 8   | G                   | Ground   |
| P2              | 9   | I/O                 | P-port input/output. Push-pull design structure  |
| P3              | 10  | I/O                 | P-port input/output. Push-pull design structure  |
| P4              | 11  | I/O                 | P-port input/output. Push-pull design structure  |
| P5              | 12  | I/O                 | P-port input/output. Push-pull design structure  |
| P6              | 13  | I/O                 | P-port input/output. Push-pull design structure  |
| P7              | 14  | I/O                 | P-port input/output. Push-pull design structure  |
| RESET           | 15  | I                   | Active-low reset input. Connect to V <sub>CC</sub> through a pullup resistor if no active connection is used.          |
| V <sub>CC</sub> | 16  | P                   | Supply voltage   |

(1) I = input, O = output, P = power, G = Ground



**Figure 4-3. RGV Package, 16-Pin QFN (Top View)**

**Table 4-2. Pin Functions, RGV**

| PIN             |     | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----------------|-----|---------------------|--|
| NAME            | NO. |                     |  |
| A0              | 1   | I                   | Address input. Connect directly to V <sub>CC</sub> or ground.  |
| A1              | 2   | I                   | Address input. Connect directly to V <sub>CC</sub> or ground.  |
| A2              | 3   | I                   | Address input. Connect directly to V <sub>CC</sub> or ground.  |
| P0              | 4   | I/O                 | P-port input/output. High impedance open-drain design structure. Connect to V <sub>CC</sub> through a pullup resistor. |
| P1              | 5   | I/O                 | P-port input/output. Push-pull design structure  |
| GND             | 6   | G                   | Ground   |
| P2              | 7   | I/O                 | P-port input/output. Push-pull design structure  |
| P3              | 8   | I/O                 | P-port input/output. Push-pull design structure  |
| P4              | 9   | I/O                 | P-port input/output. Push-pull design structure  |
| P5              | 10  | I/O                 | P-port input/output. Push-pull design structure  |
| P6              | 11  | I/O                 | P-port input/output. Push-pull design structure  |
| P7              | 12  | I/O                 | P-port input/output. Push-pull design structure  |
| RESET           | 13  | I                   | Active-low reset input. Connect to V <sub>CC</sub> through a pullup resistor if no active connection is used.          |
| V <sub>CC</sub> | 14  | P                   | Supply voltage   |
| SCL             | 15  | I                   | Serial clock bus. Connect to V <sub>CC</sub> through a pullup resistor.  |
| SDA             | 16  | I/O                 | Serial data bus. Connect to V <sub>CC</sub> through a pullup resistor.   |

(1) I = input, O = output, P = power, G = Ground

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) see (1)

|                  |  |  | MIN  | MAX  | UNIT |
|------------------|--|--|------|------|------|
| V <sub>CC</sub>  | Supply voltage                             |  | -0.5 | 6    | V    |
| V <sub>I</sub>   | Input voltage (2)                          |  | -0.5 | 6    | V    |
| V <sub>O</sub>   | Output voltage (2)                         |  | -0.5 | 6    | V    |
| I <sub>IK</sub>  | Input clamp current                        | V <sub>I</sub> < 0                                     |      | -20  | mA   |
| I <sub>OK</sub>  | Output clamp current                       | V <sub>O</sub> < 0                                     |      | -20  | mA   |
| I <sub>IOK</sub> | Input/output clamp current                 | V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> |      | -20  | μA   |
| I <sub>OL</sub>  | Continuous output low current              | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |      | 50   | mA   |
| I <sub>OH</sub>  | Continuous output high current             | V <sub>O</sub> = 0 to V <sub>CC</sub>                  |      | -50  | mA   |
| I <sub>CC</sub>  | Continuous current through GND             |  |      | -250 | mA   |
|                  | Continuous current through V <sub>CC</sub> |  |      | 160  |      |
| T <sub>stg</sub> | Storage temperature                        |  | -65  | 150  | °C   |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommend Operating Conditions*. If briefly operating outside the *Recommend Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)              | ±2000 | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2) | ±1000 |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

|                 |                                |  | MIN                   | MAX                   | UNIT |
|-----------------|--------------------------------|--|-----------------------|-----------------------|------|
| V <sub>CC</sub> | Supply voltage                 |  | 2.3                   | 5.5                   | V    |
| V <sub>IH</sub> | High-level input voltage       | SCL, SDA                                     | 0.7 × V <sub>CC</sub> | 5.5                   | V    |
|                 |                                | A2–A0, P7–P0, RESET                          | 2.2                   | 5.5                   |      |
| V <sub>IL</sub> | Low-level input voltage        | SCL, SDA                                     | -0.5                  | 0.3 × V <sub>CC</sub> | V    |
|                 |                                | A2–A0, P7–P0, (RESET V <sub>CC</sub> > 2.4V) | -0.5                  | 0.8                   |      |
|                 |                                | RESET V <sub>CC</sub> ≤ 2.4V                 | -0.5                  | 0.75                  |      |
| I <sub>OH</sub> | High-level output current      | P7–P1  |                       | -10                   | mA   |
| I <sub>OL</sub> | Low-level output current       | P7–P0  |                       | 25                    | mA   |
| T <sub>A</sub>  | Operating free-air temperature |  | -40                   | 85                    | °C   |

## 5.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

| THERMAL METRIC <sup>(1)</sup> |  | PCA9557  |           |            |           |            |            | UNIT |
|-------------------------------|--|----------|-----------|------------|-----------|------------|------------|------|
|                               |  | D (SSOP) | DB (SSOP) | DGV (SSOP) | PW (SSOP) | RGV (VQFN) | RGY (VQFN) |      |
|                               |  | 16 PINS  | 16 PINS   | 16 PINS    | 16 PINS   | 16 PINS    | 16 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 77.2     | 82        | 120        | 98.0      | 44.5       | 47         | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 40.0     |           |            | 30.7      | 40.1       |            | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 39.2     |           |            | 52.7      | 20.2       |            | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 6.5      |           |            | 1.0       | 0.9        |            | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 38.8     |           |            | 52.1      | 20.2       |            | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A      |           |            | N/A       | 5.7        |            | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        |   | TEST CONDITIONS   | V <sub>CC</sub>  | MIN  | TYP <sup>(1)</sup> | MAX | UNIT |
|------------------|---|---|------------------|------|--------------------|-----|------|
| V <sub>IK</sub>  | Input diode clamp voltage                       | I <sub>I</sub> = -18mA  | 2.3V to 5.5V     | -1.2 |                    |     | V    |
| V <sub>POR</sub> | Power-on reset voltage                          | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0   | V <sub>POR</sub> |      | 1.65               | 2.1 | V    |
| V <sub>OH</sub>  | P-port high-level output voltage <sup>(3)</sup> | I <sub>OH</sub> = -8mA  | 2.3V             | 1.8  |                    |     | V    |
|                  |   |   | 3V               | 2.6  |                    |     |      |
|                  |   |   | 4.5V             | 3    |                    |     |      |
|                  |   |   | 4.75V            | 4.1  |                    |     |      |
|                  |   | I <sub>OH</sub> = -10mA   | 2.3V             | 1.5  |                    |     |      |
|                  |   |   | 3V               | 2.5  |                    |     |      |
|                  |   |   | 4.5V             | 3    |                    |     |      |
|                  |   |   | 4.75V            | 4    |                    |     |      |
| I <sub>OL</sub>  | SDA   | V <sub>OL</sub> = 0.4V  | 2.3V to 5.5V     | 3    |                    |     | mA   |
|                  | P port <sup>(2)</sup>                           | V <sub>OL</sub> = 0.5V  |                  |      | 8                  | 20  |      |
|                  |   | V <sub>OL</sub> = 0.55V   | 2.3V to 5.5V     | 8    | 20                 |     |      |
|                  |   | V <sub>OL</sub> = 0.7V  |                  | 10   | 24                 |     |      |
| I <sub>OH</sub>  | P port, except for P0 <sup>(2)</sup>            | V <sub>OH</sub> = 2.3V  | 2.3V to 5.5V     | -4   |                    |     | mA   |
|                  | P0 <sup>(2)</sup>                               | V <sub>OH</sub> = 4.6V  | 4.6V to 5.5V     |      |                    | 1   | μA   |
|                  |   | V <sub>OH</sub> = 3.3V  | 3.3V to 5.5V     |      |                    | 1   |      |
| I <sub>I</sub>   | SCL, SDA  | V <sub>I</sub> = V <sub>CC</sub> or GND   | 2.3V to 5.5V     |      |                    | ±1  | μA   |
|                  | A2-A0, RESET                                    |   |                  |      |                    | ±1  |      |
| I <sub>IH</sub>  | P port  | V <sub>I</sub> = V <sub>CC</sub>  | 2.3V to 5.5V     |      |                    | 1   | μA   |
| I <sub>IL</sub>  | P port  | V <sub>I</sub> = GND  | 2.3V to 5.5V     |      |                    | 1   | μA   |
| I <sub>CC</sub>  | Operating mode                                  | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 400 kHz | 5.5V             |      | 19                 | 25  | μA   |
|                  |   |   | 3.6V             |      | 12                 | 22  |      |
|                  |   |   | 2.7V             |      | 8                  | 20  |      |
|                  |   | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 100 kHz | 5.5V             |      | 1.5                | 5   |      |
|                  |   |   | 3.6V             |      | 1                  | 4   |      |
|                  |   |   | 2.7V             |      | 0.6                | 3   |      |
|                  | Standby mode                                    | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0, I/O = inputs, f <sub>SCL</sub> = 0 kHz   | 5.5V             |      | 0.25               | 1   |      |
|                  |   |   | 3.6V             |      | 0.25               | 0.9 |      |
|                  |   |   | 2.7V             |      | 0.2                | 0.8 |      |

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER       |                                    | TEST CONDITIONS  | VCC           | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|-----------------|------------------------------------|--|---------------|-----|--------------------|-----|------|
| $\Delta I_{CC}$ | Additional current in standby mode | One input at $V_{CC} - 0.6$ V, Other inputs at $V_{CC}$ or GND | 2.3V to 5.5V  |     | 0.2                |     | mA   |
|                 |                                    | Every LED I/O at $V_I = 4.3$ V, $f_{SCL} = 0$ kHz              | 5.5V          |     | 0.4                |     |      |
| $C_I$           | SCL                                | $V_I = V_{CC}$ or GND  | 2.3V to 5.5 V |     | 4                  | 6   | pF   |
| $C_{io}$        | SDA                                | $V_{IO} = V_{CC}$ or GND                                       | 2.3V to 5.5V  |     | 5.5                | 8   | pF   |
|                 | P port                             |  |               |     | 7.5                | 9.5 |      |

(1) All typical values are at nominal supply voltage (2.5, 3.3, or 5V  $V_{CC}$ ) and  $T_A = 25^\circ\text{C}$ .

(2) Each I/O must be externally limited to a maximum of 25mA, and the P port (P7–P0) must be limited to a maximum current of 200mA.

(3) The total current sourced by all I/Os must be limited to 85mA per bit.

## 5.6 I<sup>2</sup>C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

|                      |  | MIN                           | MAX  | UNIT          |
|----------------------|--|-------------------------------|------|---------------|
| <b>STANDARD MODE</b> |  |                               |      |               |
| $f_{SCL}$            | I <sup>2</sup> C clock frequency   | 100                           |      | kHz           |
| $t_{sch}$            | I <sup>2</sup> C clock high time   | 4                             |      | $\mu\text{s}$ |
| $t_{scl}$            | I <sup>2</sup> C clock low time  | 4.7                           |      | $\mu\text{s}$ |
| $t_{sp}$             | I <sup>2</sup> C spike time  | 50                            |      | ns            |
| $t_{sds}$            | I <sup>2</sup> C serial data setup time                                    | 250                           |      | ns            |
| $t_{sdh}$            | I <sup>2</sup> C serial data hold time                                     | 0                             |      | ns            |
| $t_{icr}$            | I <sup>2</sup> C input rise time   |                               | 1000 | ns            |
| $t_{icf}$            | I <sup>2</sup> C input fall time   |                               | 300  | ns            |
| $t_{ocf}$            | I <sup>2</sup> C output fall time, 10-pF to 400-pF bus                     |                               | 300  | ns            |
| $t_{buf}$            | I <sup>2</sup> C bus free time between stop and start                      |                               | 4.7  | $\mu\text{s}$ |
| $t_{sts}$            | I <sup>2</sup> C start or repeated start condition setup time              |                               | 4.7  | $\mu\text{s}$ |
| $t_{sth}$            | I <sup>2</sup> C start or repeated start condition hold time               |                               | 4    | $\mu\text{s}$ |
| $t_{sps}$            | I <sup>2</sup> C stop condition setup time                                 |                               | 4    | $\mu\text{s}$ |
| $t_{vd(data)}$       | Valid data time, SCL low to SDA output valid                               | 1                             |      | $\mu\text{s}$ |
| $t_{vd(ack)}$        | Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low |                               | 1    | $\mu\text{s}$ |
| $C_b$                | I <sup>2</sup> C bus capacitive load                                       |                               | 400  | pF            |
| <b>FAST MODE</b>     |  |                               |      |               |
| $f_{SCL}$            | I <sup>2</sup> C clock frequency   | 400                           |      | kHz           |
| $t_{sch}$            | I <sup>2</sup> C clock high time   | 0.6                           |      | $\mu\text{s}$ |
| $t_{scl}$            | I <sup>2</sup> C clock low time  | 1.3                           |      | $\mu\text{s}$ |
| $t_{sp}$             | I <sup>2</sup> C spike time  | 50                            |      | ns            |
| $t_{sds}$            | I <sup>2</sup> C serial data setup time                                    | 100                           |      | ns            |
| $t_{sdh}$            | I <sup>2</sup> C serial data hold time                                     | 0                             |      | ns            |
| $t_{icr}$            | I <sup>2</sup> C input rise time   | 20 + 0.1 $C_b$ <sup>(1)</sup> | 300  | ns            |
| $t_{icf}$            | I <sup>2</sup> C input fall time   | 20 + 0.1 $C_b$ <sup>(1)</sup> | 300  | ns            |
| $t_{ocf}$            | I <sup>2</sup> C output fall time, 10-pF to 400-pF bus                     | 20 + 0.1 $C_b$ <sup>(1)</sup> | 300  | ns            |
| $t_{buf}$            | I <sup>2</sup> C bus free time between Stop and Start                      |                               | 1.3  | $\mu\text{s}$ |
| $t_{sts}$            | I <sup>2</sup> C start or repeated start condition setup time              |                               | 0.6  | $\mu\text{s}$ |
| $t_{sth}$            | I <sup>2</sup> C start or repeated start condition hold time               |                               | 0.6  | $\mu\text{s}$ |
| $t_{sps}$            | I <sup>2</sup> C stop condition setup time                                 |                               | 0.6  | $\mu\text{s}$ |
| $t_{vd(data)}$       | Valid data time, SCL low to SDA output valid                               | 0.9                           |      | $\mu\text{s}$ |
| $t_{vd(ack)}$        | Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low |                               | 0.9  | $\mu\text{s}$ |
| $C_b$                | I <sup>2</sup> C bus capacitive load                                       |                               | 400  | pF            |

(1)  $C_b$  = total capacitance of one bus line in pF

## 5.7 Reset Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-3](#))

|                                    |   | MIN | MAX | UNIT |
|------------------------------------|---|-----|-----|------|
| <b>STANDARD MODE and FAST MODE</b> |   |     |     |      |
| $t_W$                              | Reset pulse duration $V_{CC} \leq 2.5V^{(2)}$ |     | 20  | ns   |
|                                    | Reset pulse duration $V_{CC} > 2.5V^{(2)}$    |     | 16  | ns   |
| $t_{REC}$                          | Reset recovery time                           |     | 0   | ns   |
| $t_{RESET}$                        | Time to reset <sup>(1)</sup>                  |     | 400 | ns   |

(1) The PCA9557 requires a minimum of 400 ns to be reset

(2) A pulse duration of 16 ns minimum must be applied to RESET to return the PCA9557 to its default state.

## 5.8 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 6-1](#))

| PARAMETER                          | FROM                  | TO     | MIN   | MAX | UNIT |
|------------------------------------|-----------------------|--------|-------|-----|------|
| <b>STANDARD MODE and FAST MODE</b> |                       |        |       |     |      |
| $t_{pv}$                           | Output data valid     | SCL    | P0    | 250 | ns   |
|                                    |                       | SCL    | P1–P7 | 200 |      |
| $t_{ps}$                           | Input data setup time | P port | SCL   | 0   | ns   |
| $t_{ph}$                           | Input data hold time  | P port | SCL   | 200 | ns   |

## 5.9 Typical Characteristics

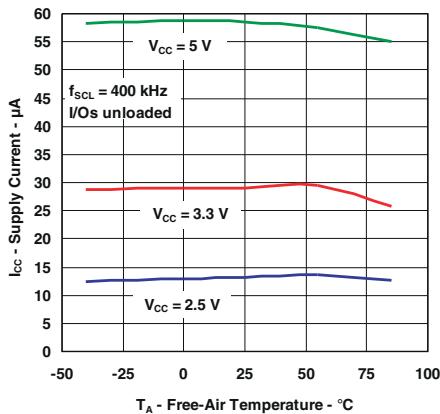


Figure 5-1. Supply Current vs Temperature

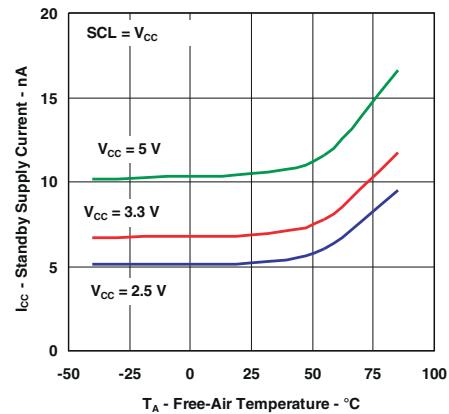


Figure 5-2. Standby Supply Current vs Temperature

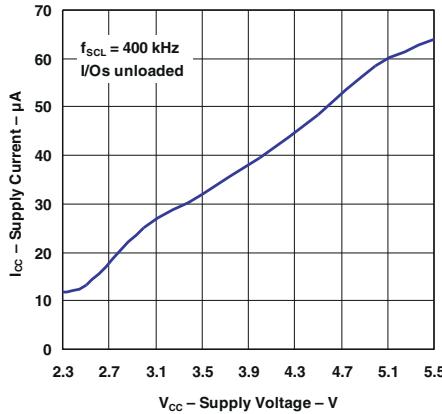


Figure 5-3. Supply Current vs Supply Voltage

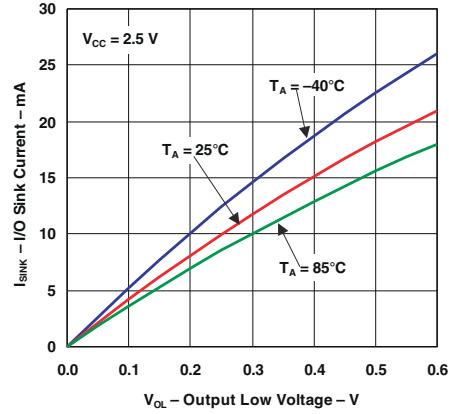


Figure 5-4. I/O Sink Current vs Output Low Voltage

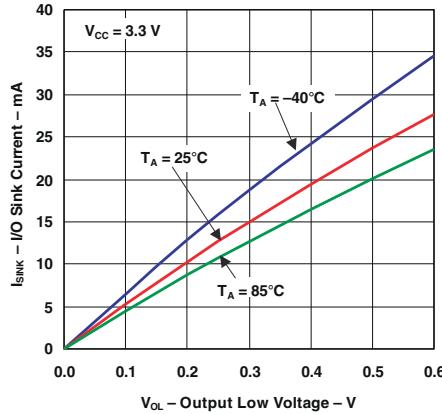


Figure 5-5. I/O Sink Current vs Output Low Voltage

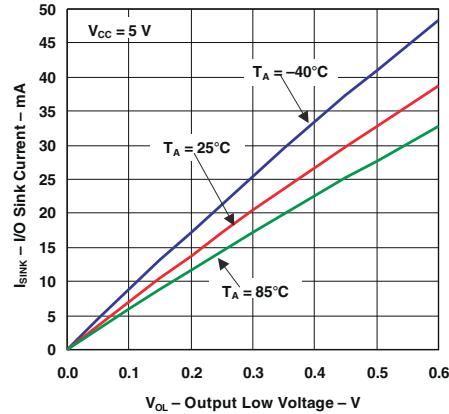


Figure 5-6. I/O Sink Current vs Output Low Voltage

## 5.9 Typical Characteristics (continued)

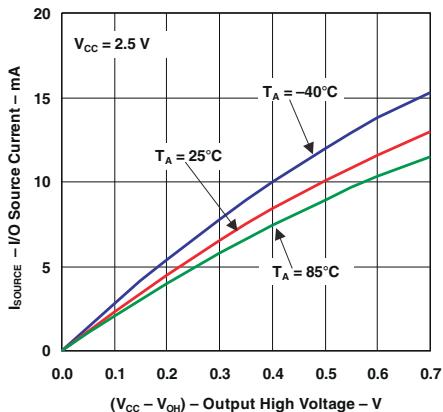


Figure 5-7. I/O Source Current vs Output High Voltage (P7–P1)

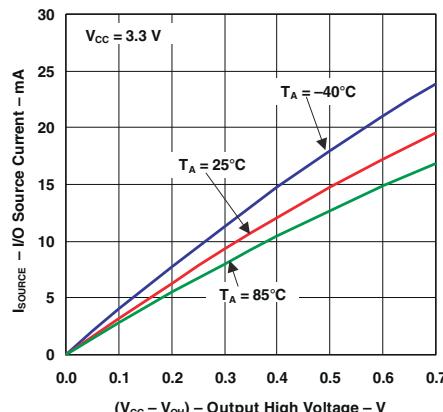


Figure 5-8. I/O Source Current vs Output High Voltage (P7–P1)

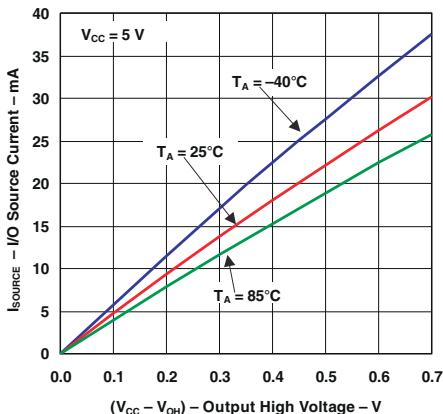


Figure 5-9. I/O Source Current vs Output High Voltage (P7–P1)

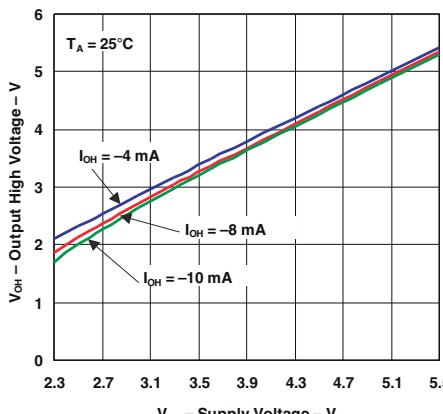


Figure 5-10. Output High Voltage vs Supply Voltage (P7–P1)

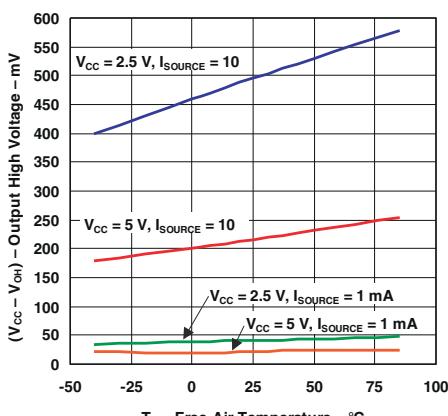


Figure 5-11. Output High Voltage vs Temperature (P7–P1)

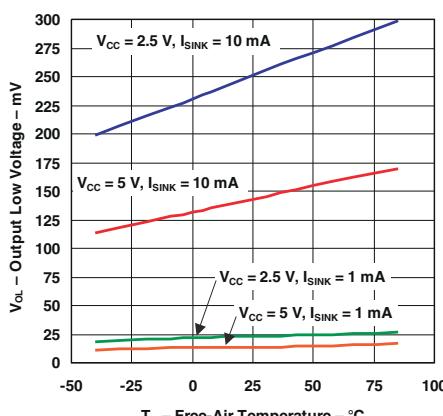
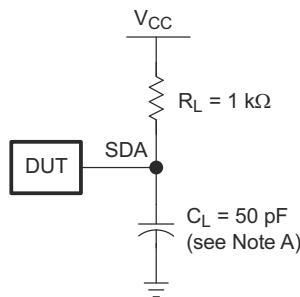
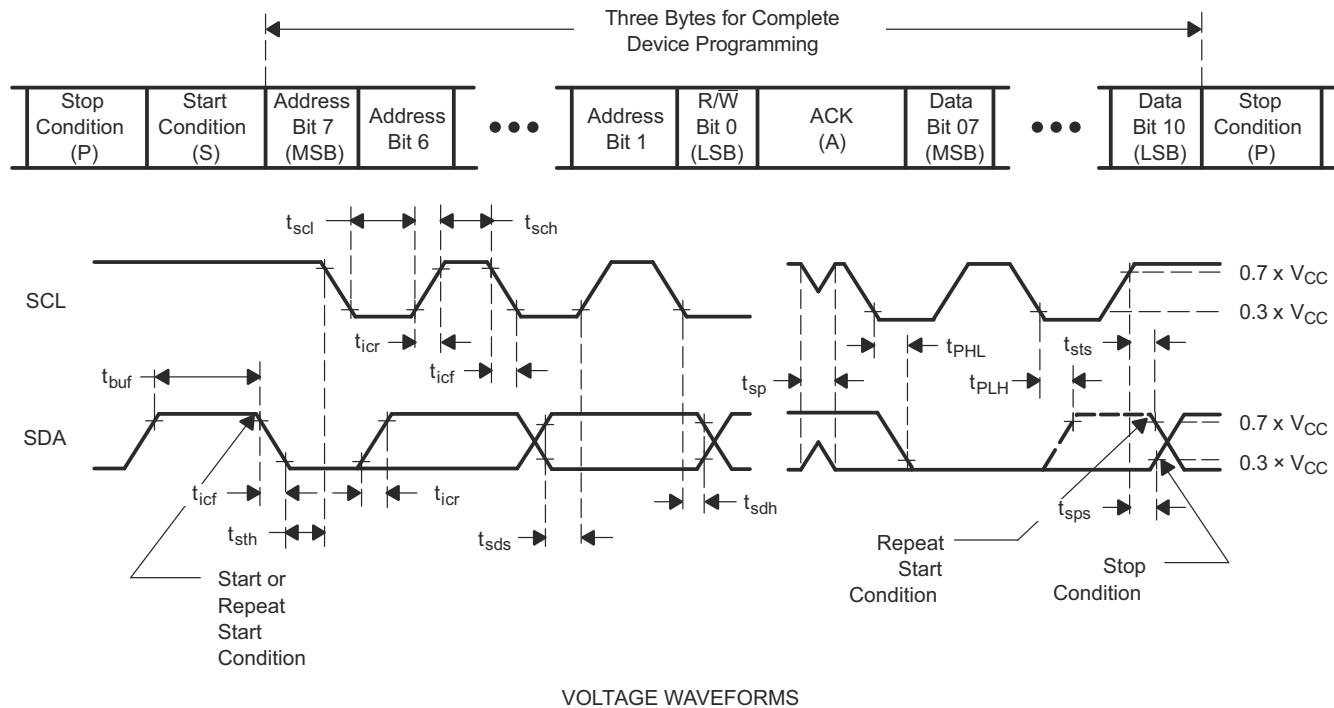


Figure 5-12. Output Low Voltage vs Temperature

## 6 Parameter Measurement Information

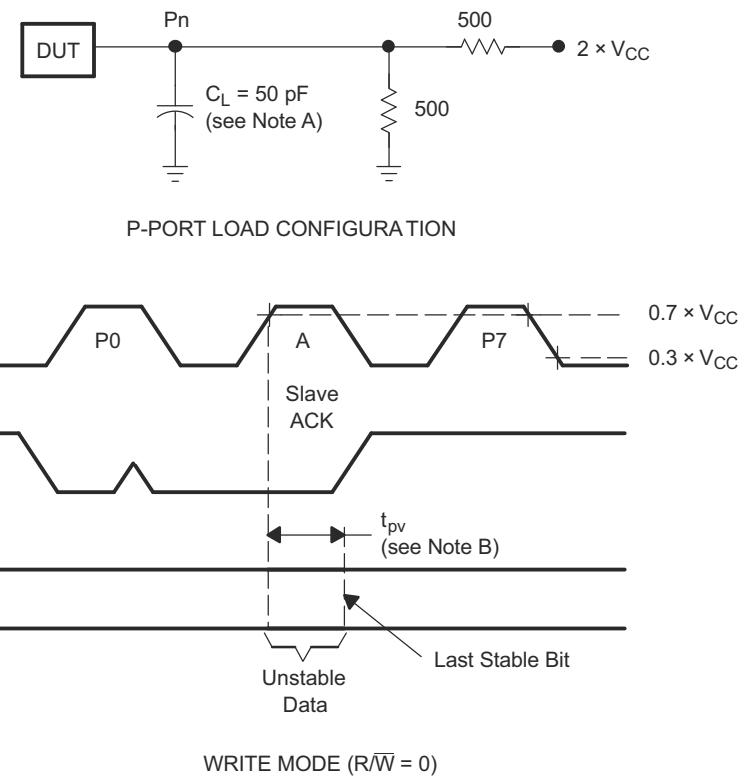


SDA LOAD CONFIGURATION



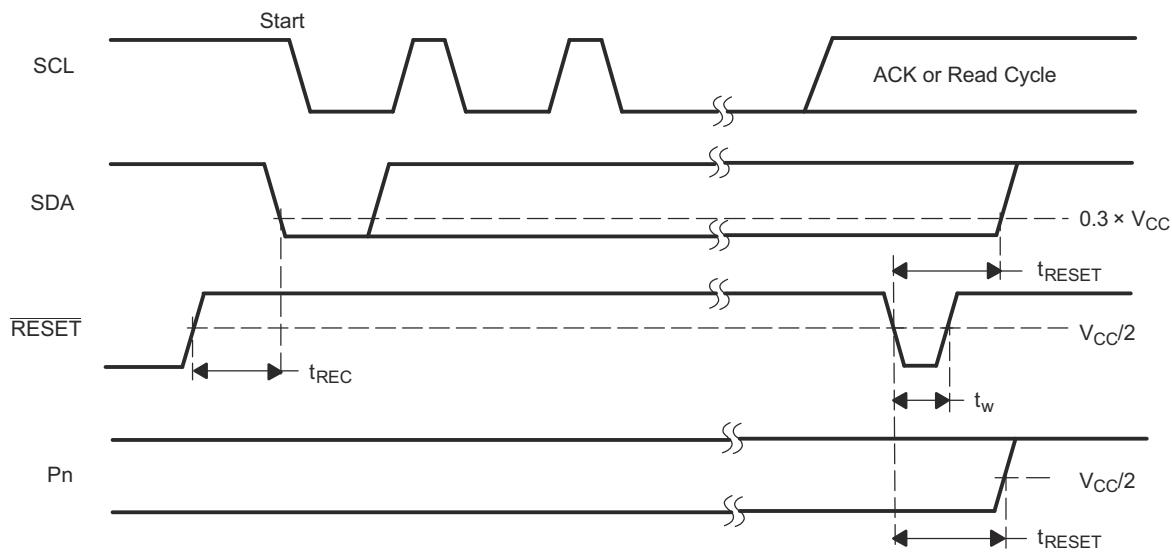
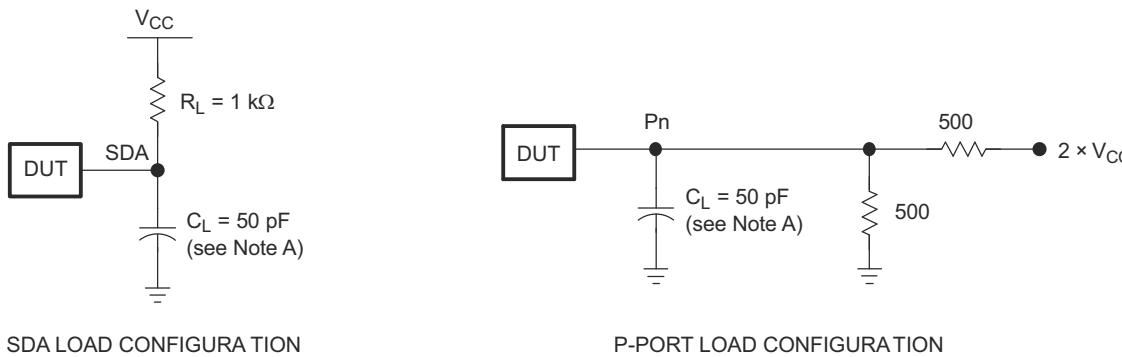
- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30 \text{ ns}$ .
- C. All parameters and waveforms are not applicable to all devices.

**Figure 6-1. I<sup>2</sup>C Interface Load Circuit and Voltage Waveforms**



- A.  $C_L$  includes probe and jig capacitance.
- B.  $t_{pv}$  is measured from  $0.7 \times V_{CC}$  on SCL to 50% I/O (Pn) output.
- C. All inputs are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

**Figure 6-2. P-Port Load Circuit and Voltage Waveforms**

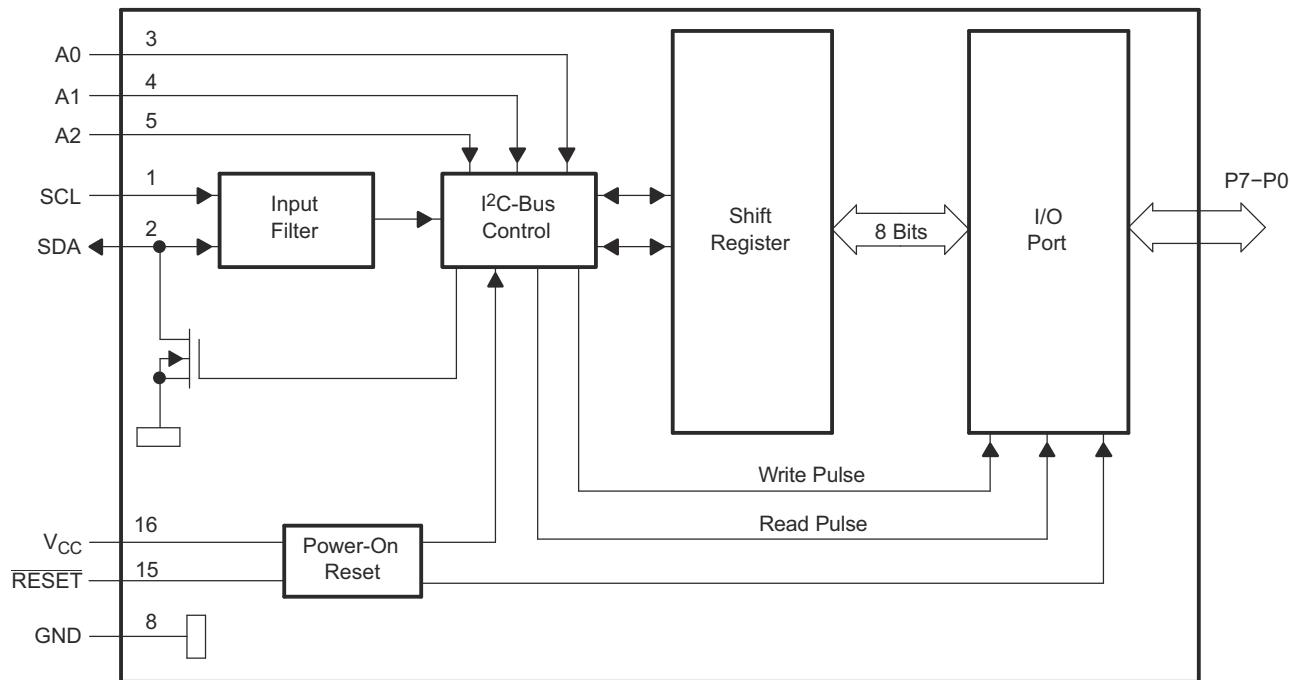


- A.  $C_L$  includes probe and jig capacitance.
- B. All inputs are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r/t_f \leq 30 \text{ ns}$ .
- C. I/Os are configured as inputs.
- D. All parameters and waveforms are not applicable to all devices.

**Figure 6-3. Reset Load Circuits and Voltage Waveforms**

## 7 Detailed Description

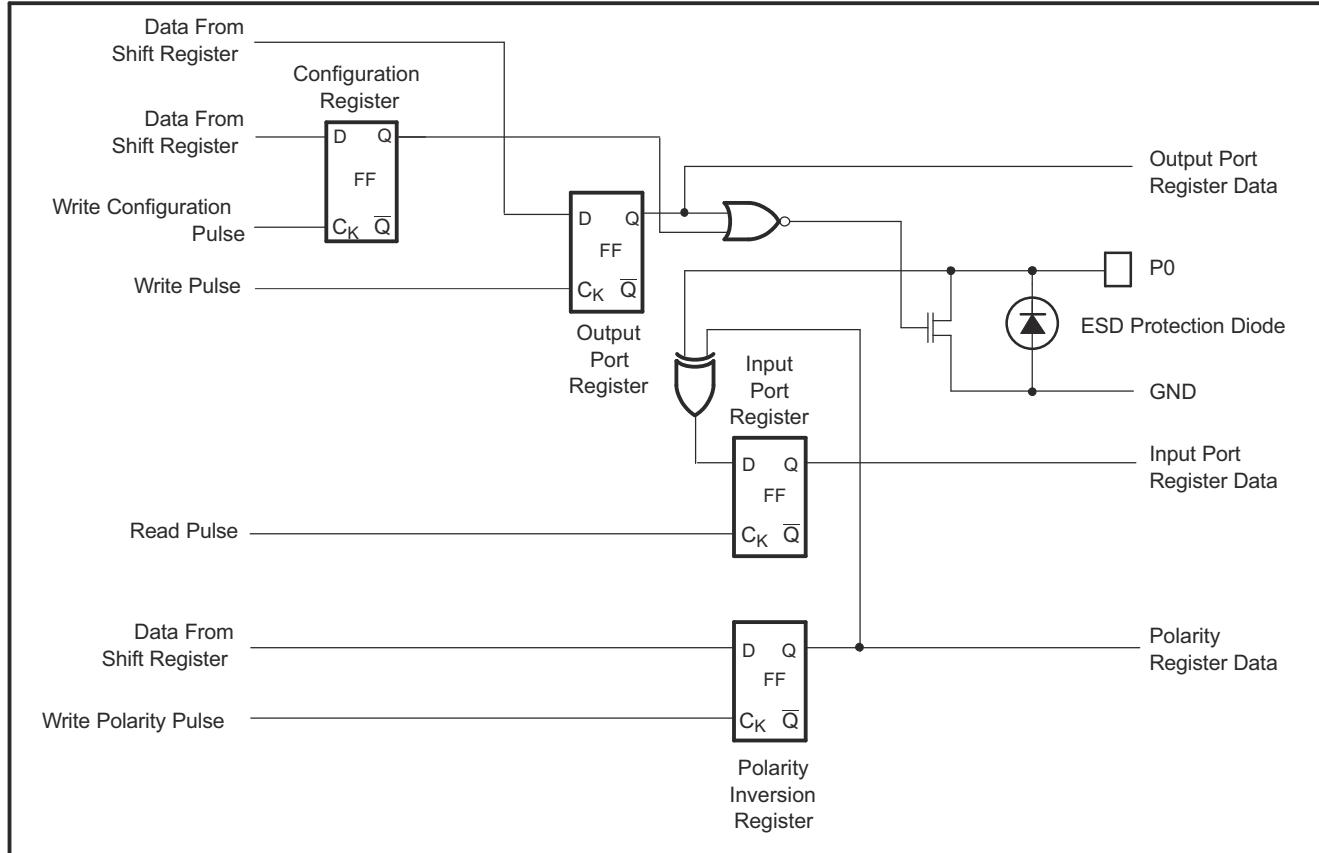
### 7.1 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.

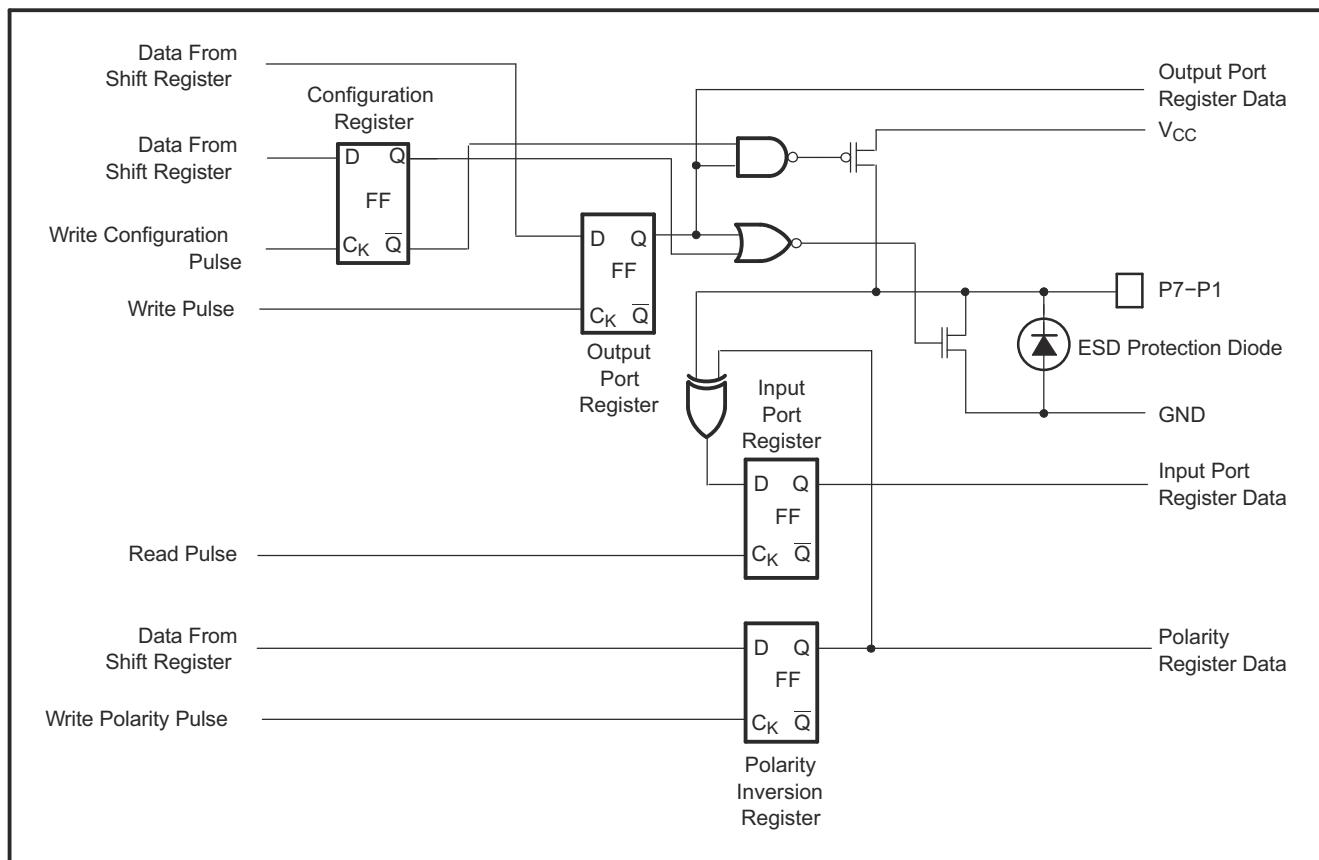
All I/Os are set to inputs at reset.

**Figure 7-1. Logic Diagram (Positive Logic)**



On power up or reset, all registers return to default values.

**Figure 7-2. Simplified Schematic Diagram of P0**



On power up or reset, all registers return to default values.

**Figure 7-3. Simplified Schematic Diagram of P7–P1**

## 7.2 Feature Description

### 7.2.1 RESET

A reset can be accomplished by holding the **RESET** pin low for a minimum of  $t_W$ . The PCA9557 registers and I<sup>2</sup>C/SMBus state machine are held in their default states until **RESET** again is high. This input requires a pullup resistor to V<sub>CC</sub> if no active connection is used.

#### 7.2.1.1 RESET Errata

If **RESET** voltage set higher than V<sub>CC</sub>, current will flow from **RESET** pin to V<sub>CC</sub> pin.

##### 7.2.1.1.1 System Impact

V<sub>CC</sub> will be pulled above its regular voltage level.

##### 7.2.1.1.2 System Workaround

Design such that **RESET** voltage is same or lower than V<sub>CC</sub>.

### 7.2.2 Power-On Reset

When power (from 0 V) is applied to V<sub>CC</sub>, an internal power-on reset holds the PCA9557 in a reset condition until V<sub>CC</sub> has reached V<sub>POR</sub>. At that time, the reset condition is released, and the PCA9557 registers and I<sup>2</sup>C/SMBus state machine initialize to their default states. After that, V<sub>CC</sub> must be lowered to below 0.2 V and back up to the operating voltage for a power-reset cycle. The **RESET** input can be asserted to reset the system, while keeping the V<sub>CC</sub> at its operating level.

See the [Power-On Reset Errata](#) section.

## 7.3 Programming

### 7.3.1 I<sup>2</sup>C Interface

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I<sup>2</sup>C communication with this device is initiated by a controller sending a start condition, a high-to-low transition on the SDA input and output while the SCL input is high (see [Figure 7-4](#)). After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/ W).

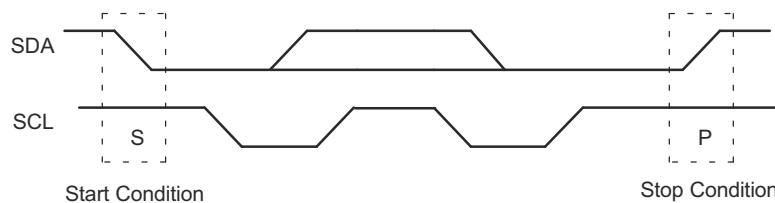
After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address (A<sub>2</sub>-A<sub>0</sub>) inputs of the target device must not be changed between the start and the stop conditions.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see [Figure 7-5](#)).

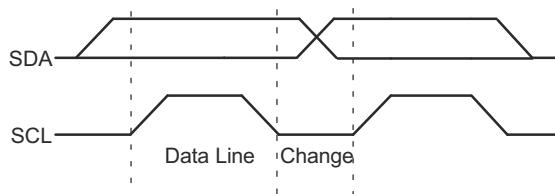
A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller (see [Figure 7-4](#)).

Any number of data bytes can be transferred from the transmitter to the receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period (see [Figure 7-6](#)). When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met to ensure proper operation.

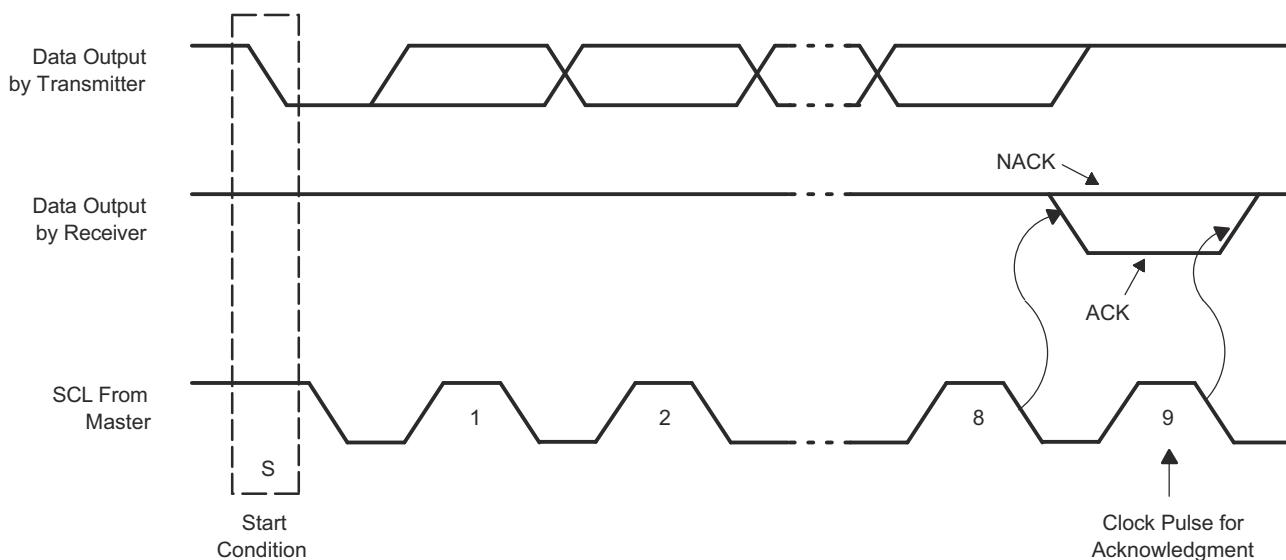
A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a stop condition.



**Figure 7-4. Definition of Start and Stop Conditions**



**Figure 7-5. Bit Transfer**



**Figure 7-6. Acknowledgment on the I<sup>2</sup>C Bus**

## 7.4 Register Maps

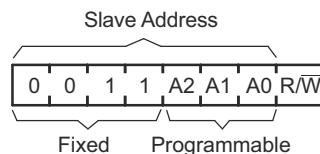
Table 7-1 shows the PCA9557 interface definition.

**Table 7-1. Interface Definition**

| <b>BYTE</b>                    | <b>BIT</b>     |          |          |          |          |          |          |                |
|--------------------------------|----------------|----------|----------|----------|----------|----------|----------|----------------|
|                                | <b>7 (MSB)</b> | <b>6</b> | <b>5</b> | <b>4</b> | <b>3</b> | <b>2</b> | <b>1</b> | <b>0 (LSB)</b> |
| I <sup>2</sup> C slave address | L              | L        | H        | H        | A2       | A1       | A0       | R/W            |
| Px I/O data bus                | P7             | P6       | P5       | P4       | P3       | P2       | P1       | P0             |

### 7.4.1 Device Address

The address of the PCA9557 is shown in Figure 7-7.



**Figure 7-7. PCA9557 Address**

The address reference of the PCA9557 is shown in Table 7-2.

**Table 7-2. Address Reference**

| <b>INPUTS</b> |           |           | <b>I<sup>2</sup>C BUS TARGET ADDRESS</b> |
|---------------|-----------|-----------|--|
| <b>A2</b>     | <b>A1</b> | <b>A0</b> |  |
| L             | L         | L         | 24 (decimal), 18 (hexadecimal)           |
| L             | L         | H         | 25 (decimal), 19 (hexadecimal)           |
| L             | H         | L         | 26 (decimal), 1A (hexadecimal)           |
| L             | H         | H         | 27 (decimal), 1B (hexadecimal)           |
| H             | L         | L         | 28 (decimal), 1C (hexadecimal)           |
| H             | L         | H         | 29 (decimal), 1D (hexadecimal)           |
| H             | H         | L         | 30 (decimal), 1E (hexadecimal)           |
| H             | H         | H         | 31 (decimal), 1F (hexadecimal)           |

The last bit of the target address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

#### 7.4.2 Control Register And Command Byte

Following the successful acknowledgment of the address byte, the bus controller sends a command byte that is stored in the control register in the PCA9557. Two bits of this data byte state the operation (read or write) and the internal registers (input, output, polarity inversion or configuration) that is affected. This register is written or read through the I<sup>2</sup>C bus. The command byte is sent only during a write transmission.

Once a new command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent. [Figure 7-8](#) shows the PCA9557 control register bits.



**Figure 7-8. Control Register Bits**

[Table 7-3](#) shows the PCA9557 command byte.

**Table 7-3. Command Byte**

| <b>CONTROL REGISTER BITS</b> |           | <b>COMMAND BYTE<br/>(HEX)</b> | <b>REGISTER</b>    | <b>PROTOCOL</b> | <b>POWER-UP<br/>DEFAULT</b> |
|------------------------------|-----------|-------------------------------|--------------------|-----------------|-----------------------------|
| <b>B1</b>                    | <b>B0</b> |                               |                    |                 |                             |
| 0                            | 0         | 0x00                          | Input Port         | Read byte       | xxxx xxxx                   |
| 0                            | 1         | 0x01                          | Output Port        | Read/write byte | 0000 0000                   |
| 1                            | 0         | 0x02                          | Polarity Inversion | Read/write byte | 1111 0000                   |
| 1                            | 1         | 0x03                          | Configuration      | Read/write byte | 1111 1111                   |

### 7.4.3 Register Descriptions

The input port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to signal the I<sup>2</sup>C device that the input port register will be accessed next. See [Table 7-4](#).

**Table 7-4. Register 0 (Input Port Register)**

| BIT     | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | X  | X  | X  | X  | X  | X  | X  | X  |

The output port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See [Table 7-5](#).

**Table 7-5. Register 1 (Output Port Register)**

| BIT     | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

The polarity inversion register (register 2) allows polarity inversion of pins defined as inputs by the configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained. See [Table 7-6](#).

**Table 7-6. Register 2 (Polarity Inversion Register)**

| BIT     | N7 | N6 | N5 | N4 | N3 | N2 | N1 | N0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  |

The configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with high impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See [Table 7-7](#).

**Table 7-7. Register 3 (Configuration Register)**

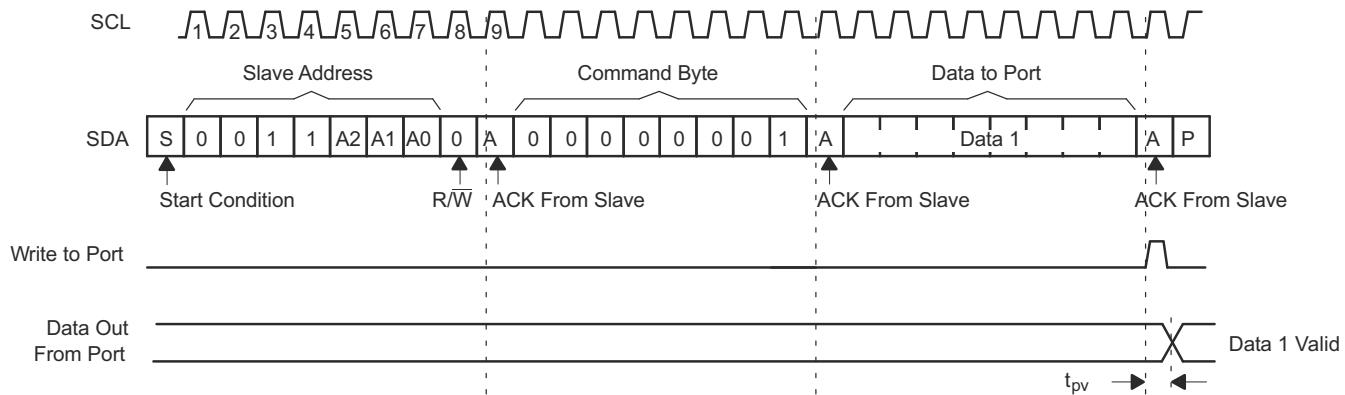
| BIT     | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---------|----|----|----|----|----|----|----|----|
| DEFAULT | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  |

#### 7.4.3.1 Bus Transactions

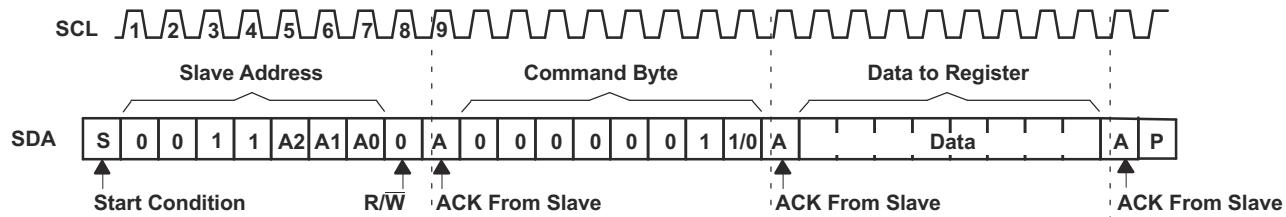
Data is exchanged between the master and PCA9557 through write and read commands.

##### 7.4.3.1.1 Writes

Data is transmitted to the PCA9557 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see [Figure 7-7](#) for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. There is no limitation on the number of data bytes sent in one write transmission (see [Figure 7-9](#) and [Figure 7-10](#)).



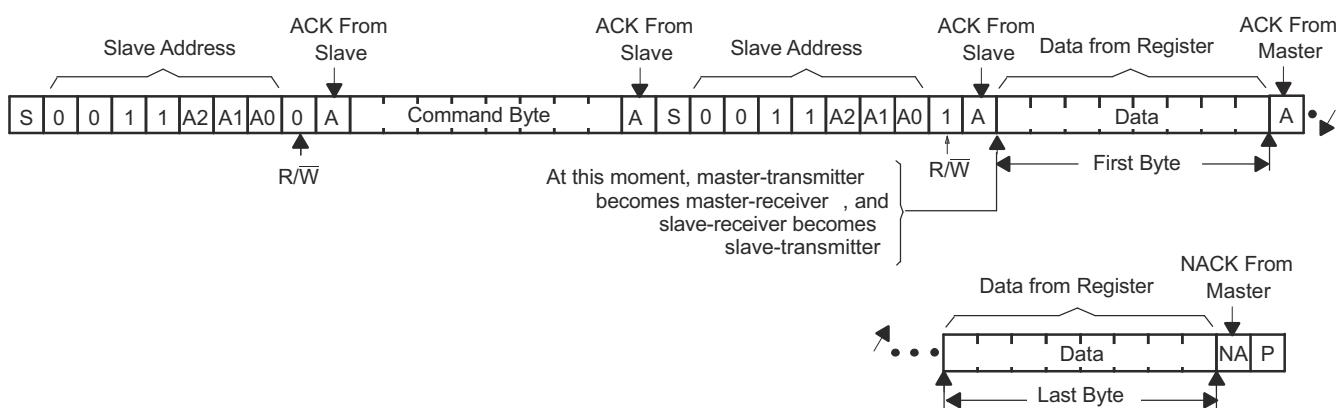
**Figure 7-9. Write to Output Port Register**



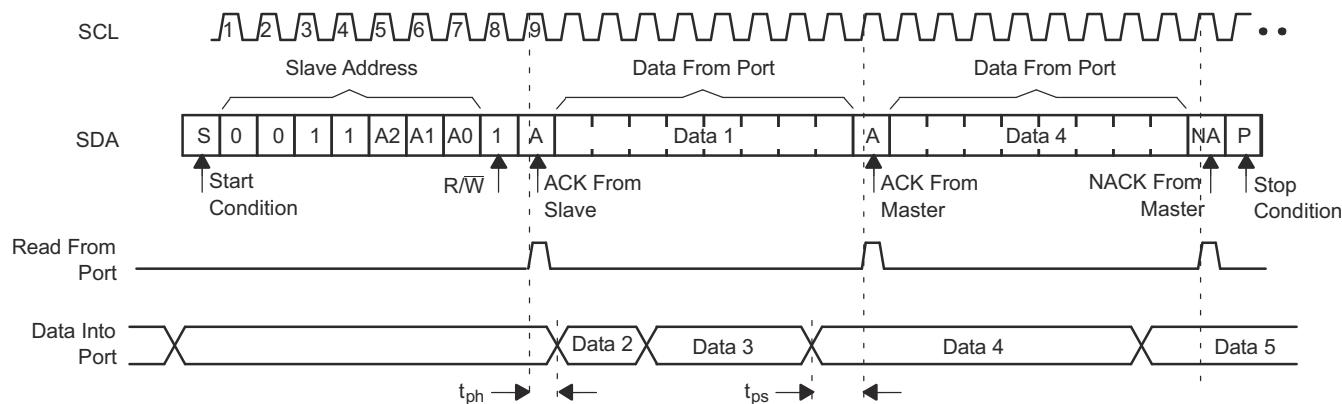
**Figure 7-10. Write to Configuration or Polarity Inversion Registers**

#### 7.4.3.1.2 Reads

The bus master first must send the PCA9557 address with the LSB set to a logic 0 (see [Figure 7-7](#) for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9557 (see [Figure 7-11](#) and [Figure 7-12](#)). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.



**Figure 7-11. Read From Register**



- This figure assumes the command byte has been previously programmed with 00h.
- Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.
- This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see [Figure 7-11](#)).

**Figure 7-12. Read Input Port Register**

## 8 Application and Implementation

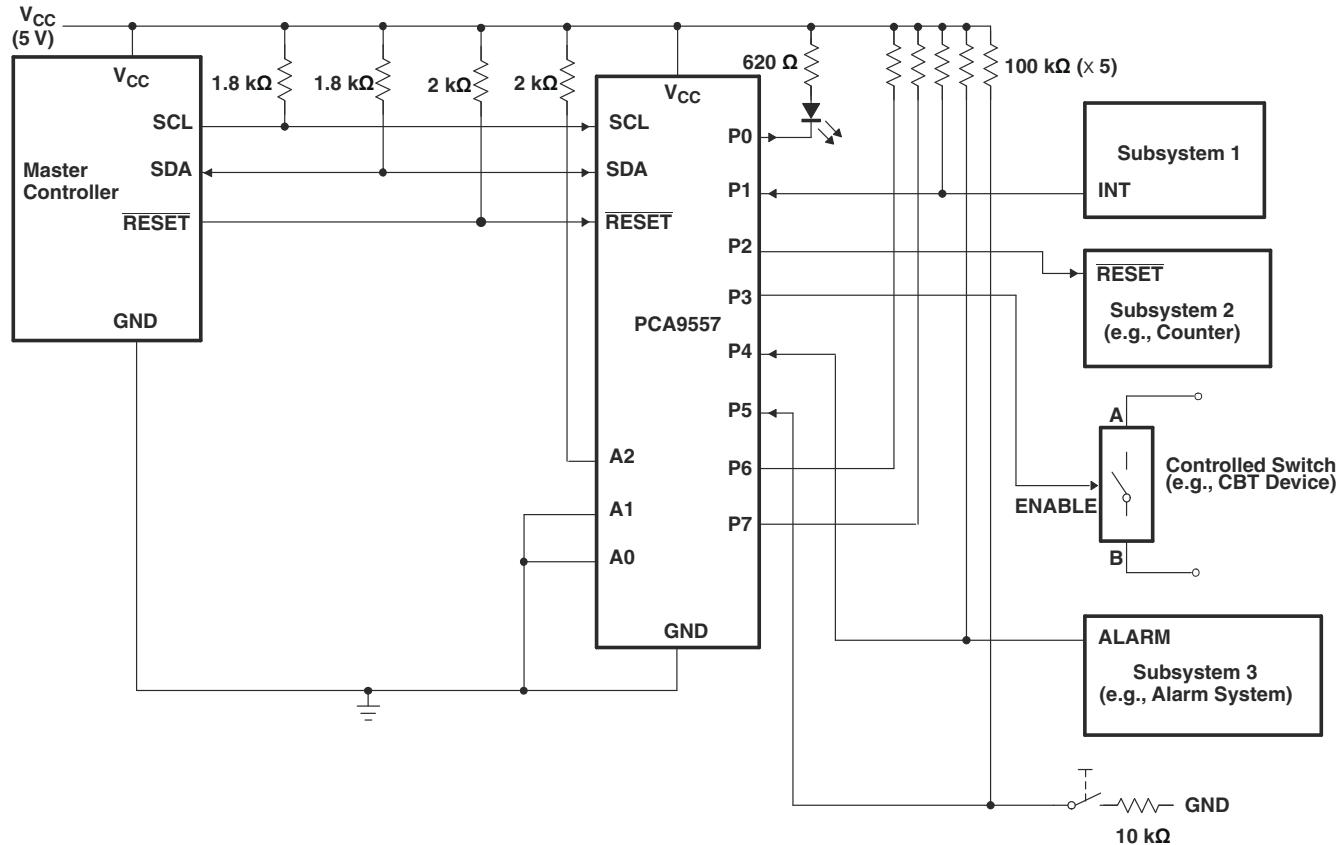
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

Figure 8-1 shows an application in which the PCA9557 can be used.

### 8.2 Typical Application



- Device address is configured as 0011100 for this example.
- P1, P4, and P5 are configured as inputs.
- P0, P2, and P3 are configured as outputs.
- P6 and P7 are not used and must be configured as outputs.

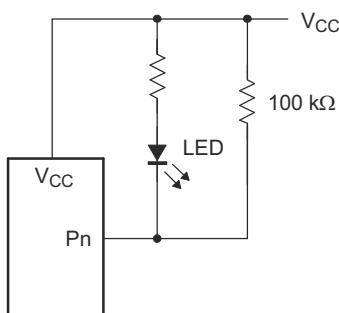
**Figure 8-1. Typical Application**

#### 8.2.1 Detailed Design Procedure

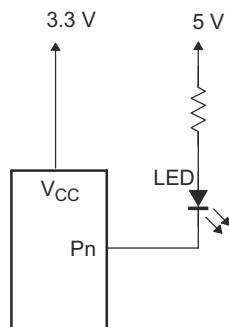
##### 8.2.1.1 Minimizing $I_{CC}$ when I/O is Used to Control LED

When an I/O is used to control an LED, normally it is connected to  $V_{CC}$  through a resistor as shown in Figure 8-1. The LED acts as a diode so, when the LED is off, the I/O  $V_{IN}$  is about 1.2 V less than  $V_{CC}$ . The  $\Delta I_{CC}$  parameter in the Section 5.5 table shows how  $I_{CC}$  increases as  $V_{IN}$  becomes lower than  $V_{CC}$ . Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to  $V_{CC}$  when the LED is off.

Figure 8-2 shows a high-value resistor in parallel with the LED. Figure 8-3 shows  $V_{CC}$  less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O  $V_{IN}$  at or above  $V_{CC}$  and prevent additional supply-current consumption when the LED is off.



**Figure 8-2. High-Value Resistor in Parallel with the LED**

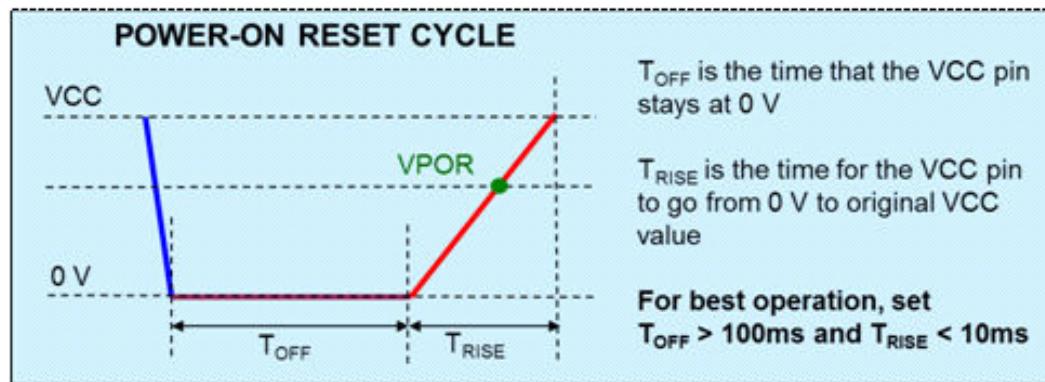


**Figure 8-3. Device Supplied by a Low Voltage**

## 8.3 Power Supply Recommendations

### 8.3.1 Power-On Reset Errata

A power-on reset condition can be missed if the  $V_{CC}$  ramps are outside specification listed in Figure 8-4.



**Figure 8-4. Power-On Reset**

#### 8.3.1.1 System Impact

As shown in the previous figure, if ramp conditions are outside timing allowance, then POR condition can be missed causing the device to lock up.

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [I<sup>2</sup>C Bus Pull-Up Resistor Calculation](#)
- Texas Instruments, [Maximum Clock Frequency of I<sup>2</sup>C Bus Using Repeaters](#)
- Texas Instruments, [Introduction to Logic](#)
- Texas Instruments, [Understanding the I<sup>2</sup>C Bus](#)
- Texas Instruments, [Choosing the Correct I<sup>2</sup>C Device for New Designs](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on [ti.com](http://ti.com). In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision J (May 2014) to Revision K (December 2024)   | Page |
|--|------|
| • Changed the numbering format for tables, figures, and cross-references throughout the document.....                                    | 1    |
| • Moved Storage Temperature Range row from <i>ESD Ratings</i> table to <i>Absolute Maximum Ratings</i> table.....                        | 6    |
| • Updated V <sub>IH</sub> from 2.0V to 2.2V.....   | 6    |
| • Add V <sub>IL</sub> parameter for RESET .....  | 6    |
| • Updated <i>Thermal Information</i> values for D, PW and RGV packages.....  | 7    |
| • Updated <i>I<sup>2</sup>C Timing Requirements</i> table.....   | 8    |
| • Add t <sub>W</sub> parameter for 2.5V voltage condition.....   | 9    |
| • Changed the Command Byte From: 00000001/0 To: 00000011/0 in the <i>Write Configuration or Polarity Inversion Registers</i> figure..... | 22   |

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| Changes from Revision I (June 2008) to Revision J (May 2014) | Page |
|--|------|
| • Added <u>RESET</u> Errata section.....                     | 17   |
| • Added Power-On Reset Errata section.....                   | 25   |

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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| PCA9557D              | Obsolete      | Production           | SOIC (D)   16    | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | PCA9557             |
| PCA9557DB             | Active        | Production           | SSOP (DB)   16   | 80   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557DB.A           | Active        | Production           | SSOP (DB)   16   | 80   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557DBR            | Active        | Production           | SSOP (DB)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557DBR.A          | Active        | Production           | SSOP (DB)   16   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557DGVR           | Active        | Production           | TVSOP (DGV)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557DGVR.A         | Active        | Production           | TVSOP (DGV)   16 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557DR             | Active        | Production           | SOIC (D)   16    | 2500   LARGE T&R      | Yes         | NIPDAU   NIPDAU                      | Level-1-260C-UNLIM                | -40 to 85    | PCA9557             |
| PCA9557DR.A           | Active        | Production           | SOIC (D)   16    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PCA9557             |
| PCA9557PWR            | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557PWR.A          | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557PWRG4          | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557PWRG4.A        | Active        | Production           | TSSOP (PW)   16  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | PD557               |
| PCA9557RGVR           | Active        | Production           | VQFN (RGV)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | PD557               |
| PCA9557RGVR.A         | Active        | Production           | VQFN (RGV)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | PD557               |
| PCA9557RGVRG4         | Active        | Production           | VQFN (RGV)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | PD557               |
| PCA9557RGVRG4.A       | Active        | Production           | VQFN (RGV)   16  | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | PD557               |
| PCA9557RGYR           | Active        | Production           | VQFN (RGY)   16  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | PD557               |
| PCA9557RGYR.A         | Active        | Production           | VQFN (RGY)   16  | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 85    | PD557               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

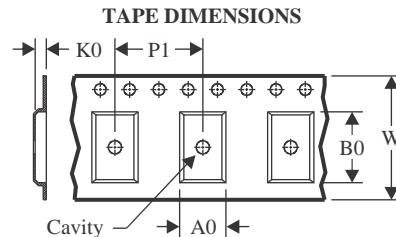
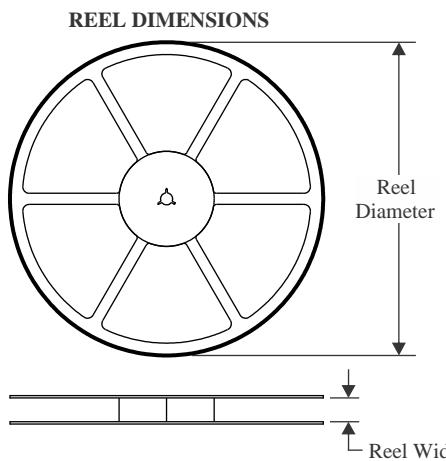
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

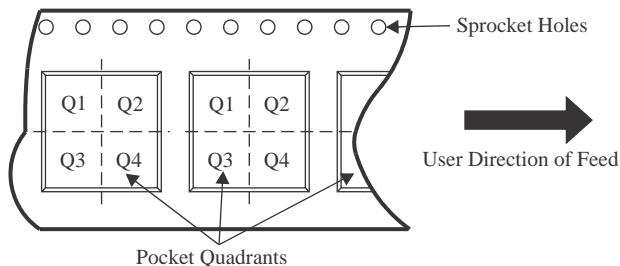
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

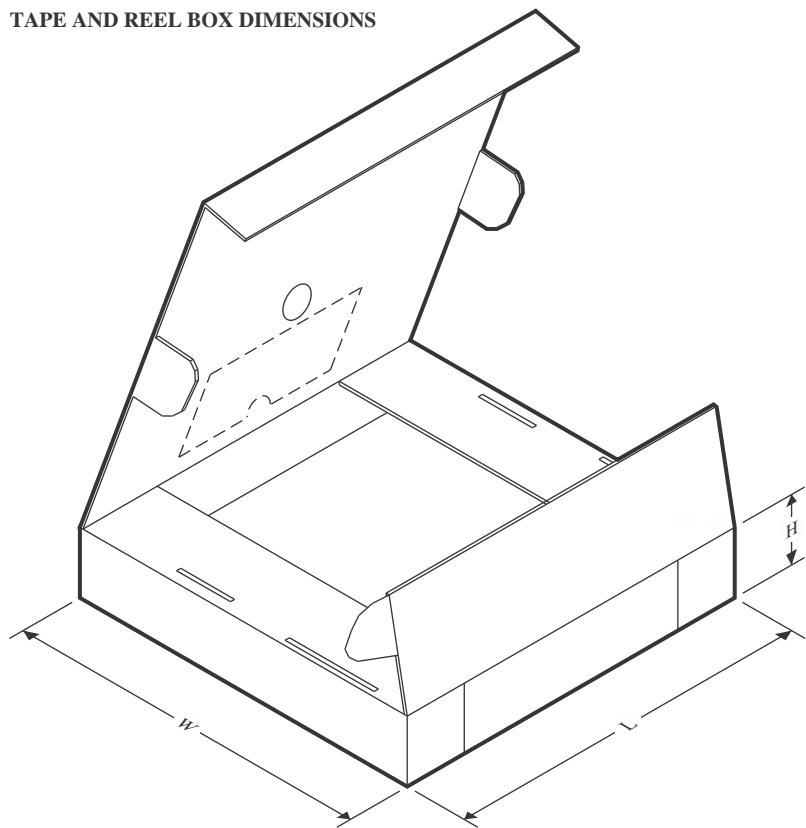
**TAPE AND REEL INFORMATION**

|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

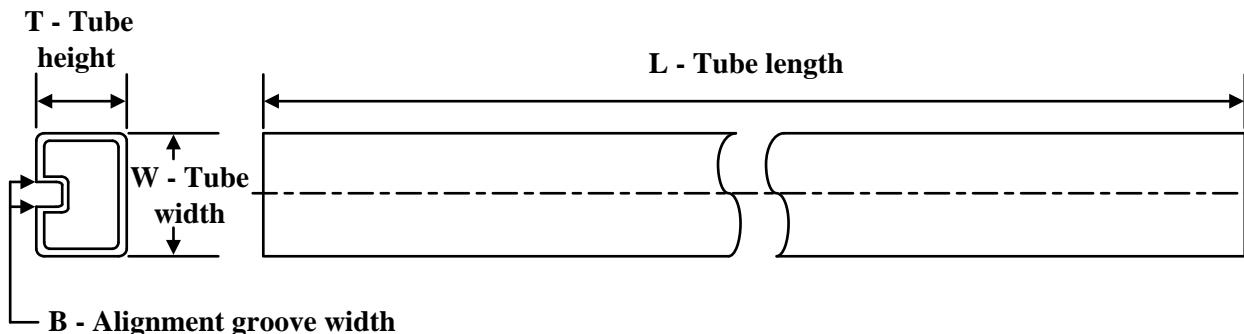
\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCA9557DBR    | SSOP         | DB              | 16   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| PCA9557DGVR   | TVSOP        | DGV             | 16   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| PCA9557DR     | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |
| PCA9557DR     | SOIC         | D               | 16   | 2500 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |
| PCA9557PWR    | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| PCA9557PWR    | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| PCA9557PWRG4  | TSSOP        | PW              | 16   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| PCA9557RGVR   | VQFN         | RGV             | 16   | 2500 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| PCA9557RGVRG4 | VQFN         | RGV             | 16   | 2500 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| PCA9557RGYR   | VQFN         | RGY             | 16   | 3000 | 330.0              | 12.4               | 3.8     | 4.3     | 1.5     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCA9557DBR    | SSOP         | DB              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| PCA9557DGVR   | TVSOP        | DGV             | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| PCA9557DR     | SOIC         | D               | 16   | 2500 | 333.2       | 345.9      | 28.6        |
| PCA9557DR     | SOIC         | D               | 16   | 2500 | 340.5       | 336.1      | 32.0        |
| PCA9557PWR    | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| PCA9557PWR    | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| PCA9557PWRG4  | TSSOP        | PW              | 16   | 2000 | 353.0       | 353.0      | 32.0        |
| PCA9557RGVR   | VQFN         | RGV             | 16   | 2500 | 367.0       | 367.0      | 35.0        |
| PCA9557RGVRG4 | VQFN         | RGV             | 16   | 2500 | 353.0       | 353.0      | 32.0        |
| PCA9557RGYR   | VQFN         | RGY             | 16   | 3000 | 353.0       | 353.0      | 32.0        |

**TUBE**


\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T ( $\mu$ m) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------------|--------|
| PCA9557DB   | DB           | SSOP         | 16   | 80  | 530    | 10.5   | 4000         | 4.1    |
| PCA9557DB.A | DB           | SSOP         | 16   | 80  | 530    | 10.5   | 4000         | 4.1    |

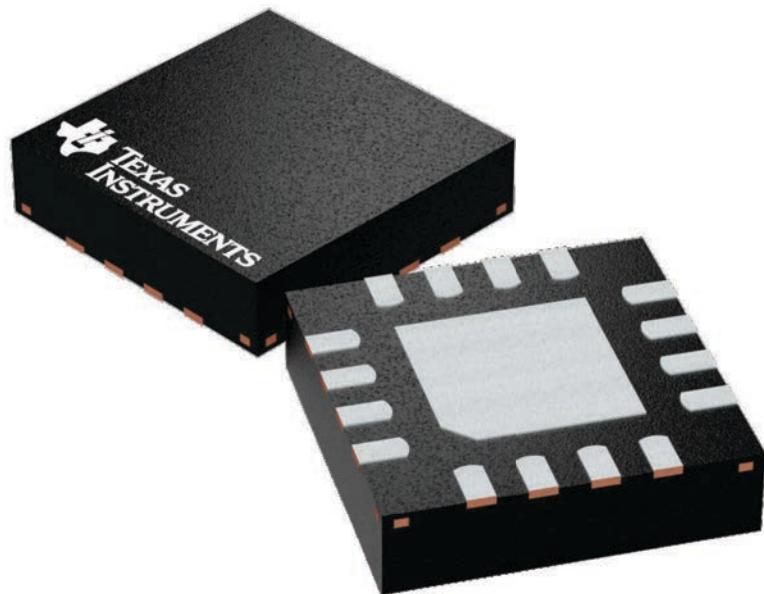
## GENERIC PACKAGE VIEW

**RGV 16**

**VQFN - 1 mm max height**

4 x 4, 0.65 mm pitch

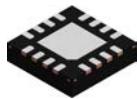
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224748/A

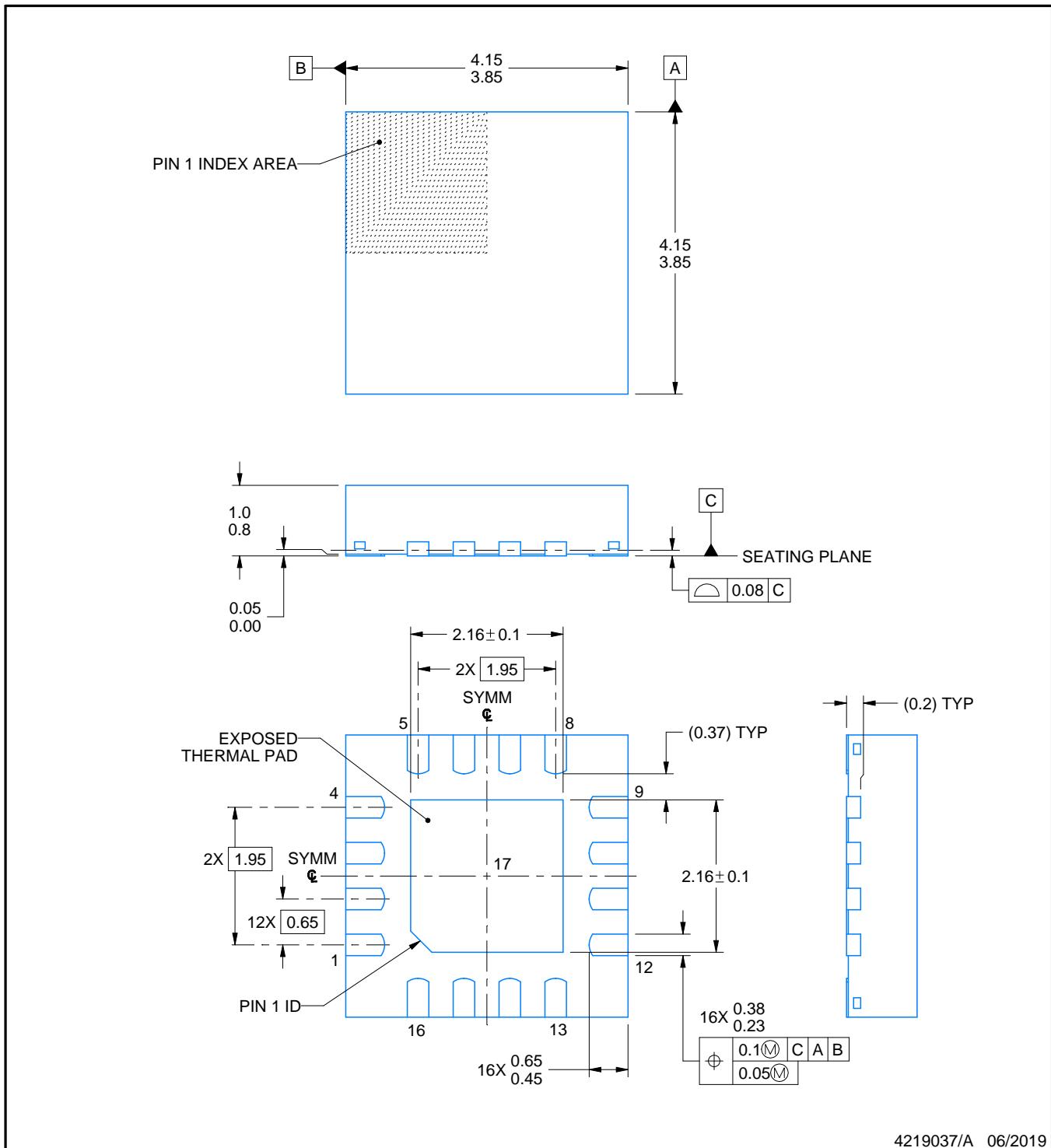
**RGV0016A**



## PACKAGE OUTLINE

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

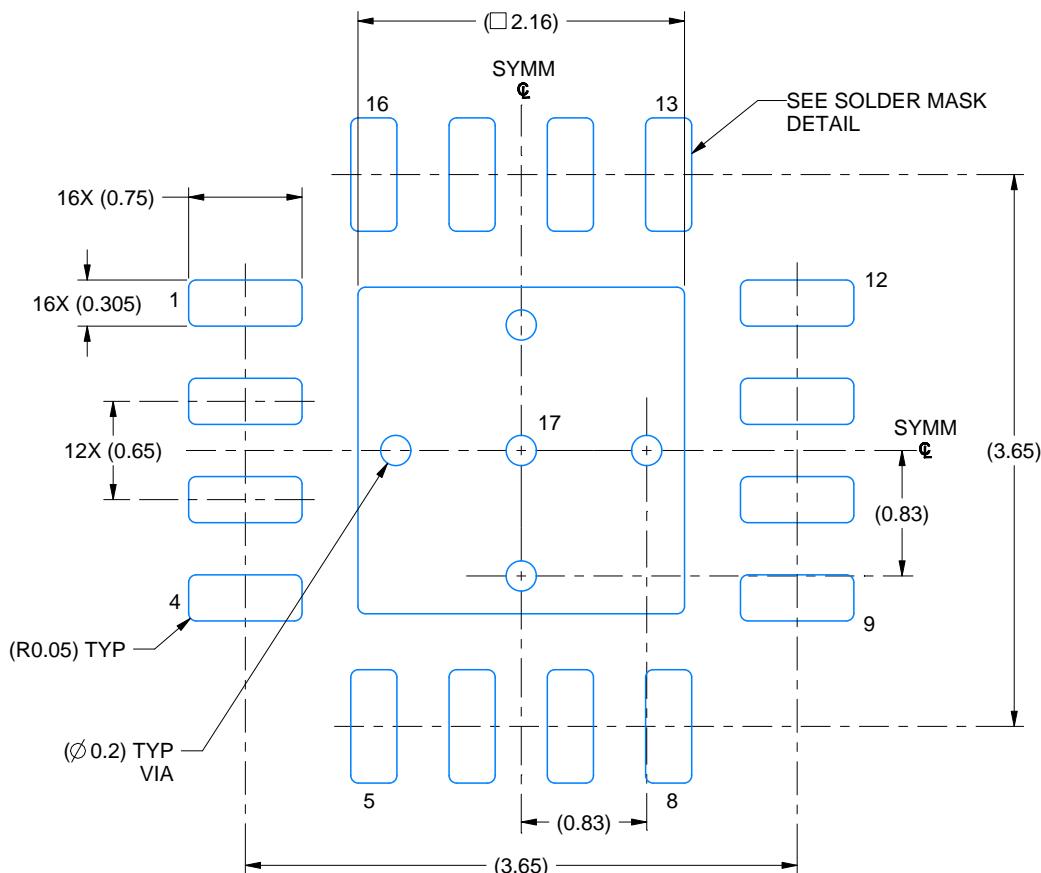
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

**RGV0016A**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4219037/A 06/2019

NOTES: (continued)

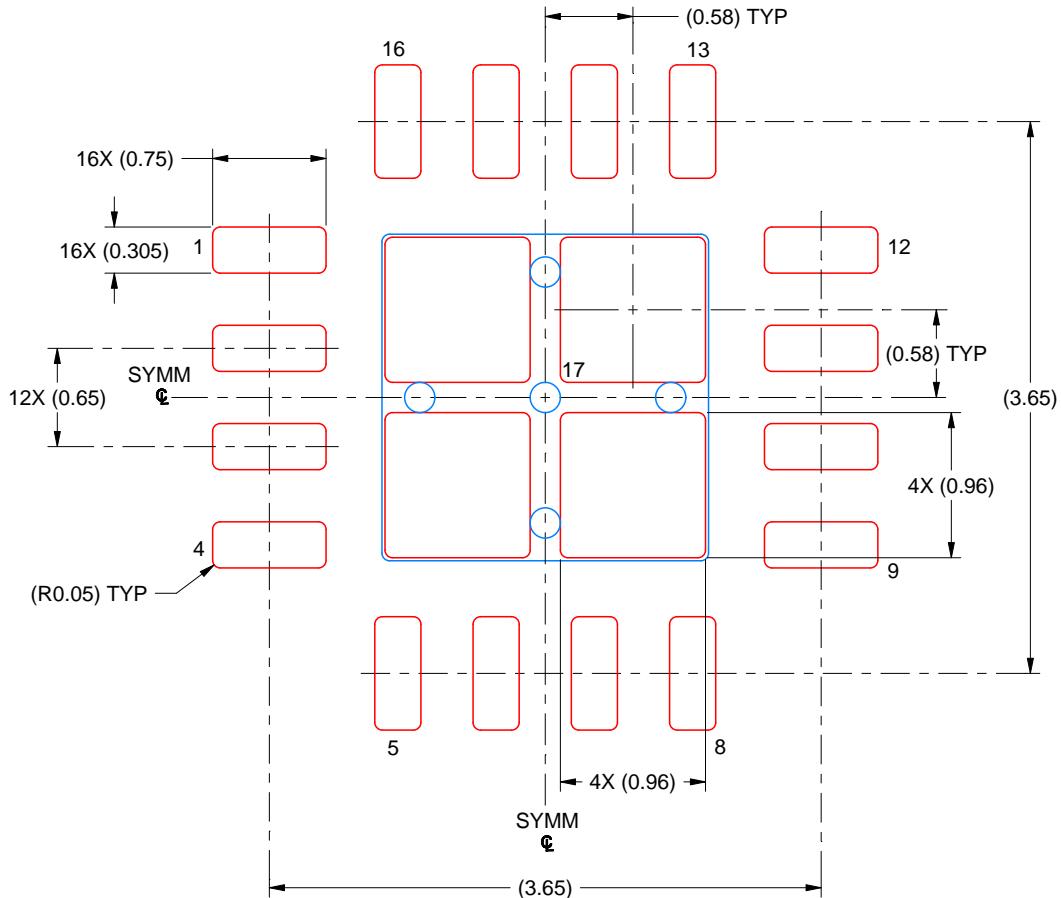
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGV0016A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 17  
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

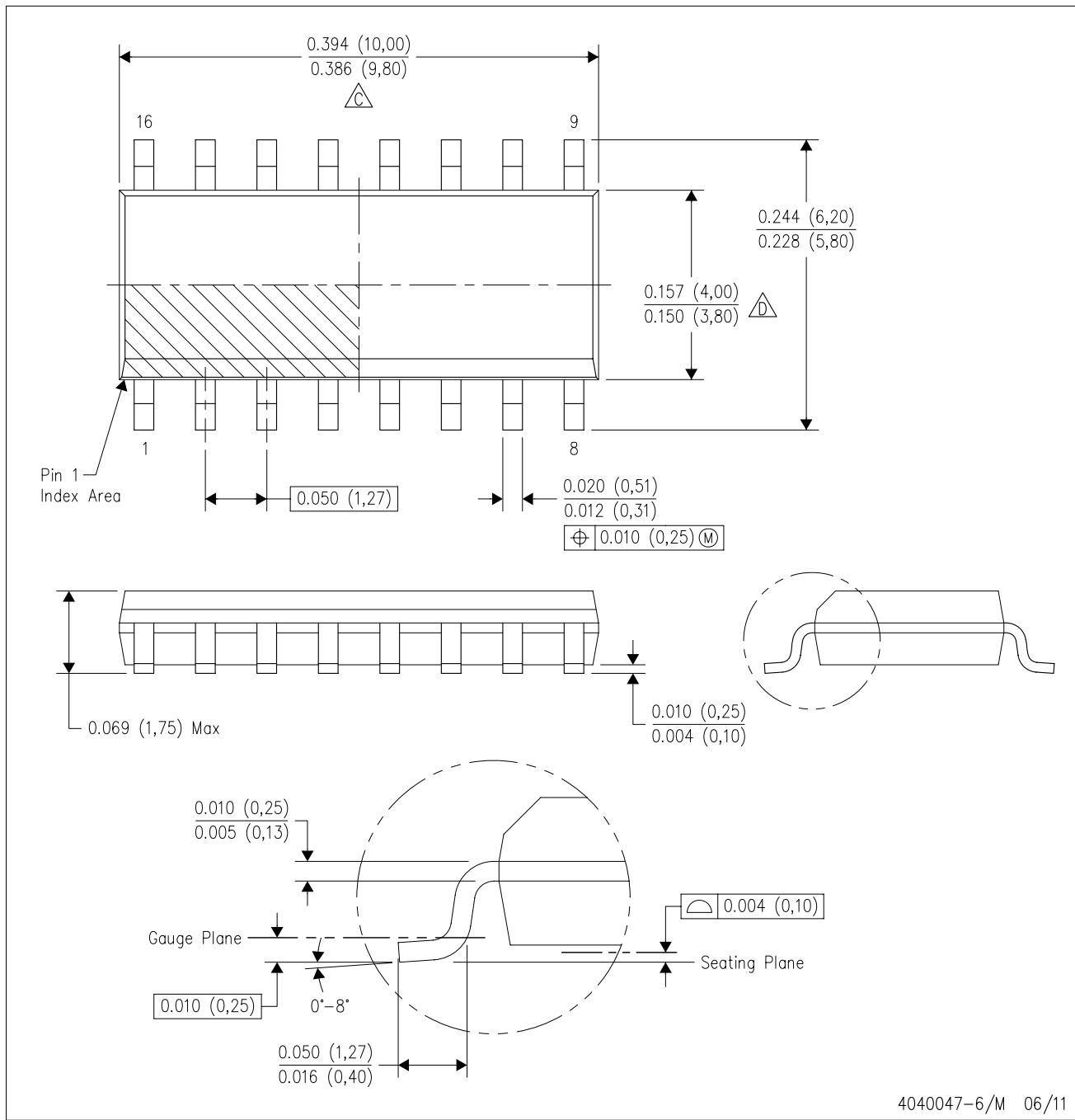
4219037/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

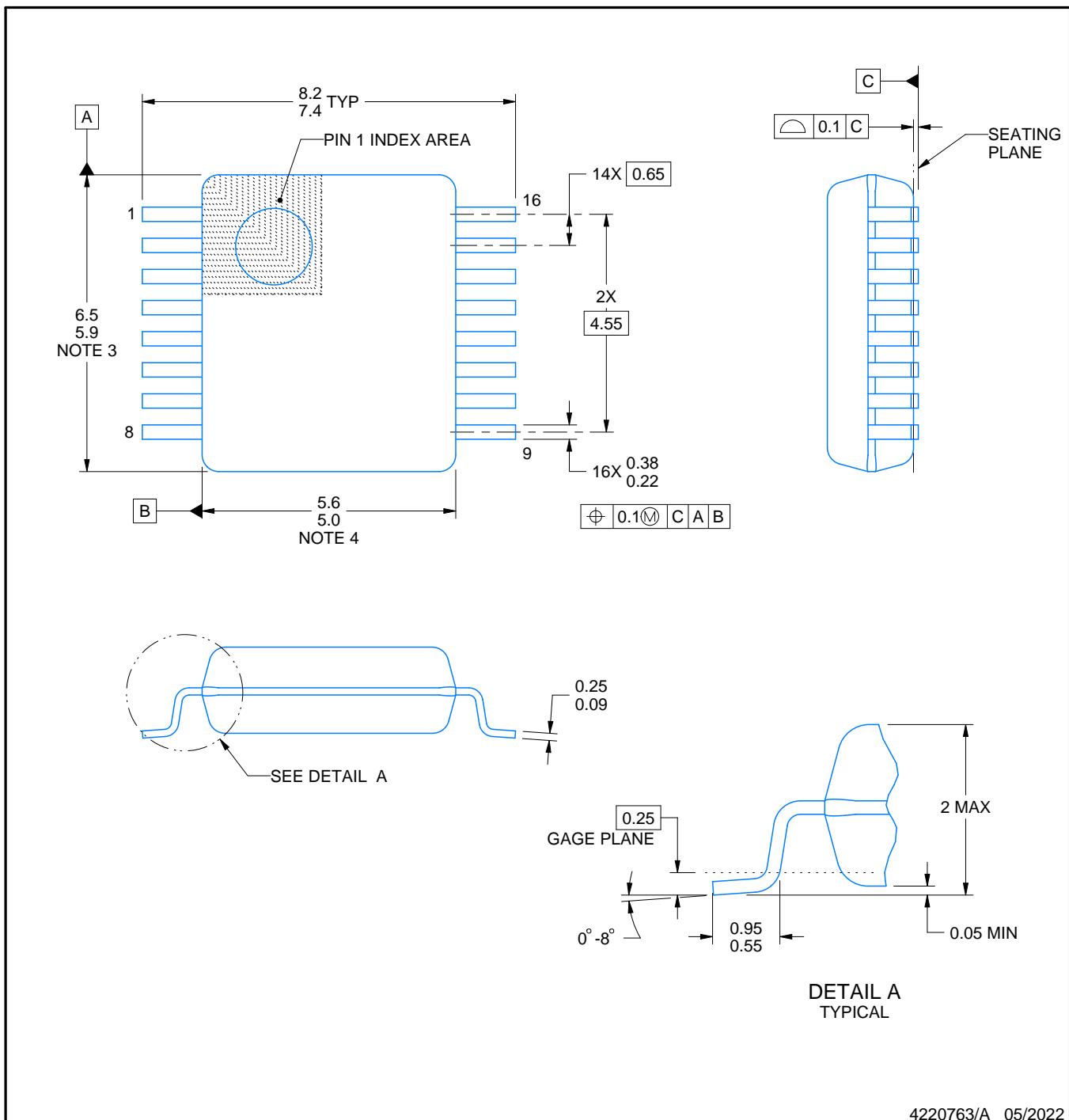
E. Reference JEDEC MS-012 variation AC.

4040047-6/M 06/11

# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

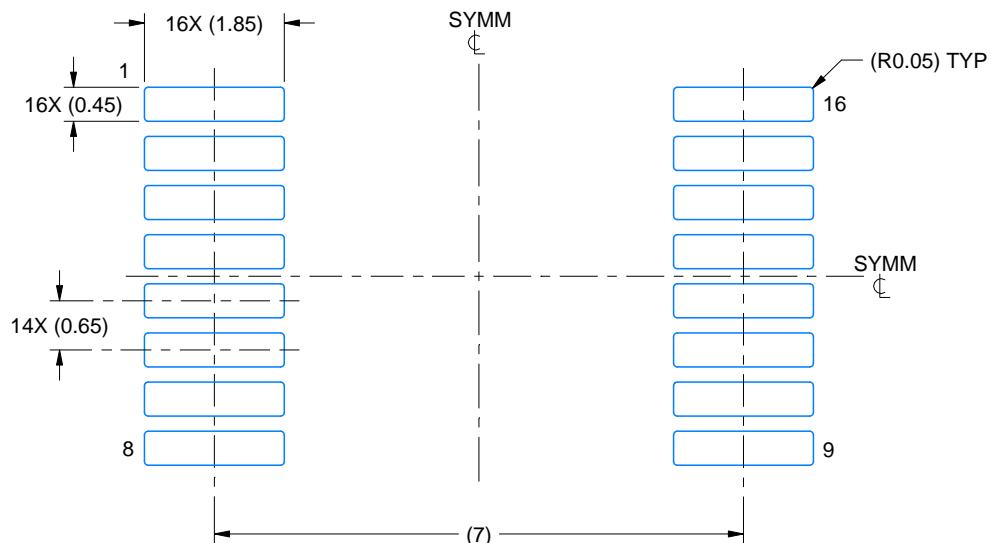
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

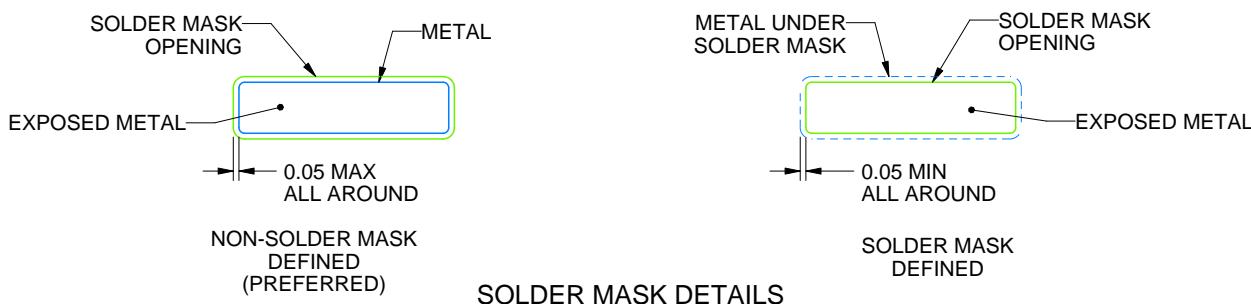
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

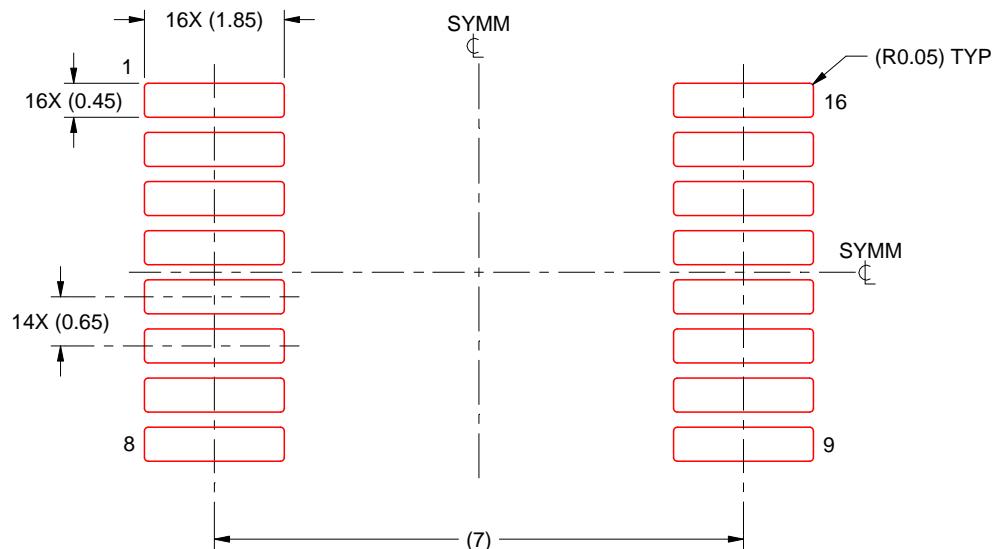
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

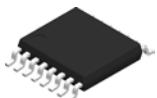
4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

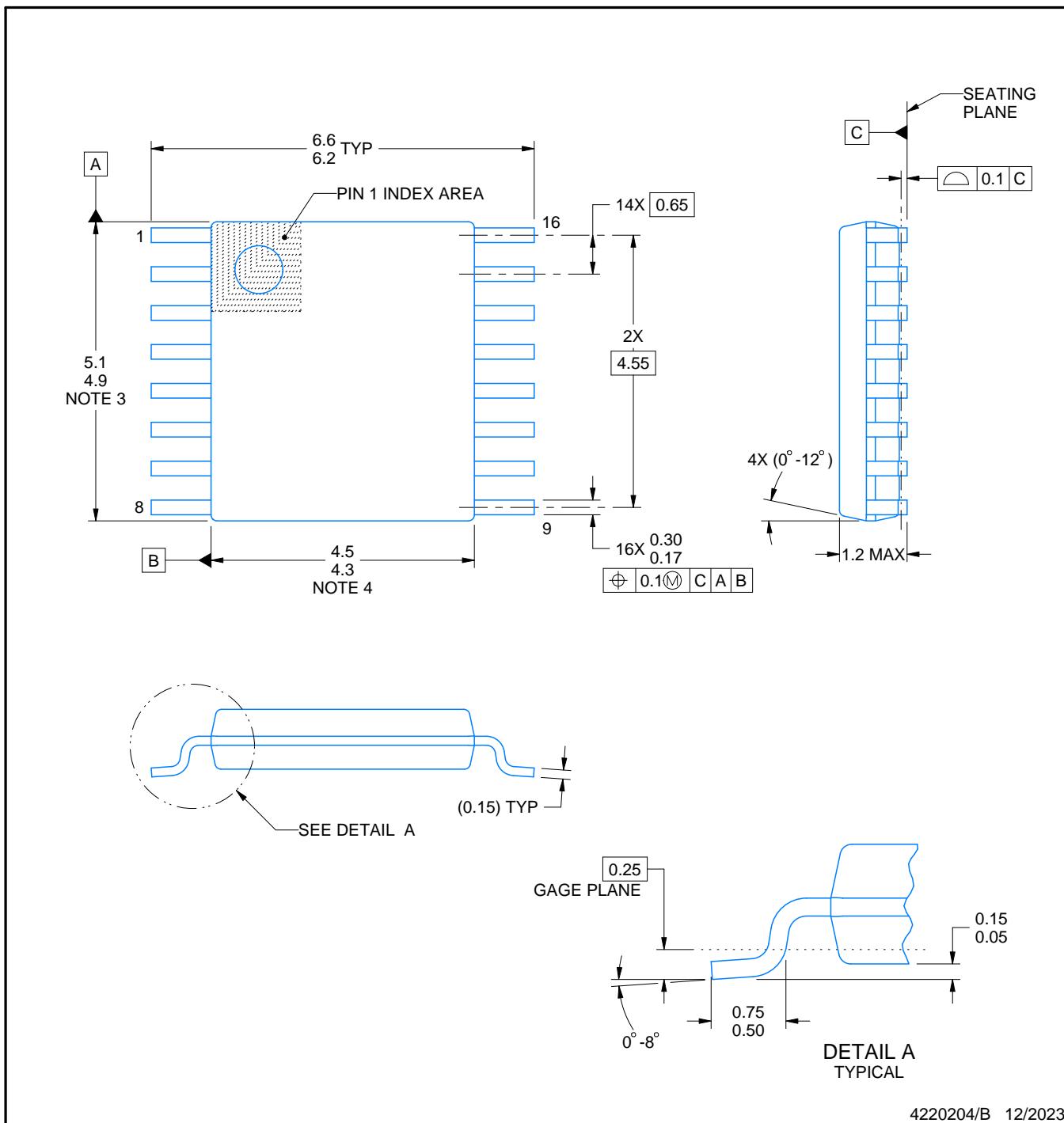
# PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



## NOTES:

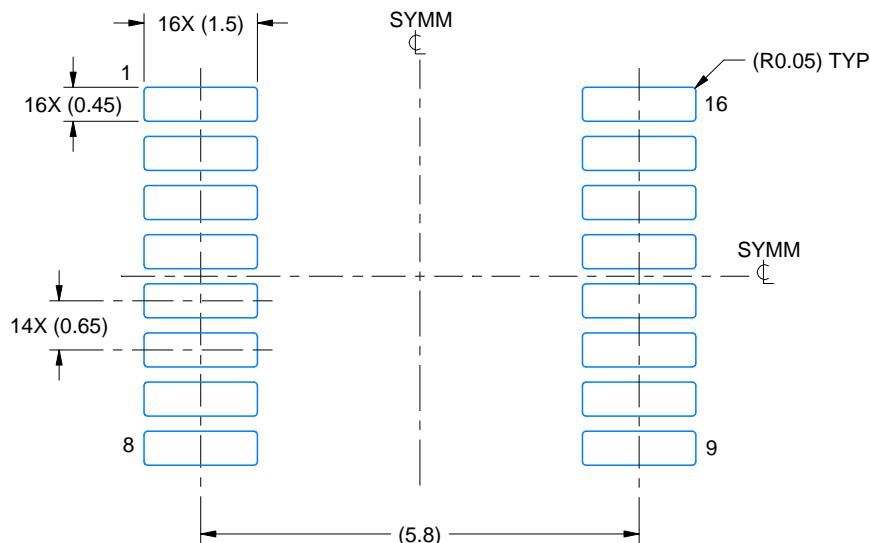
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

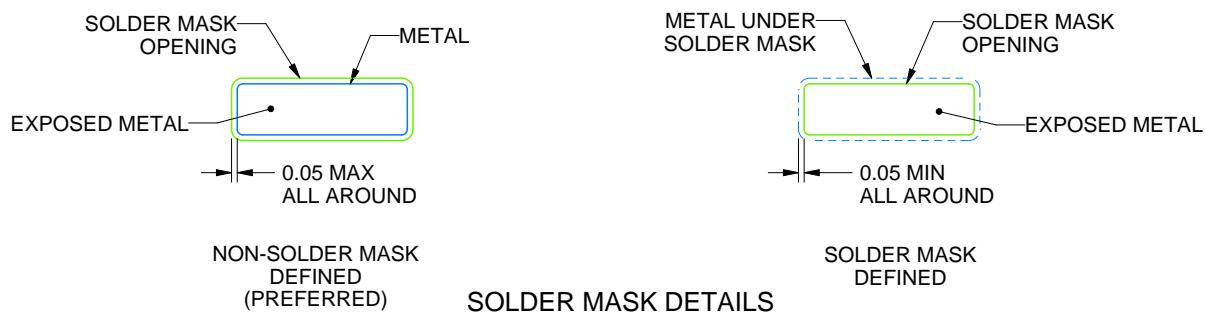
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

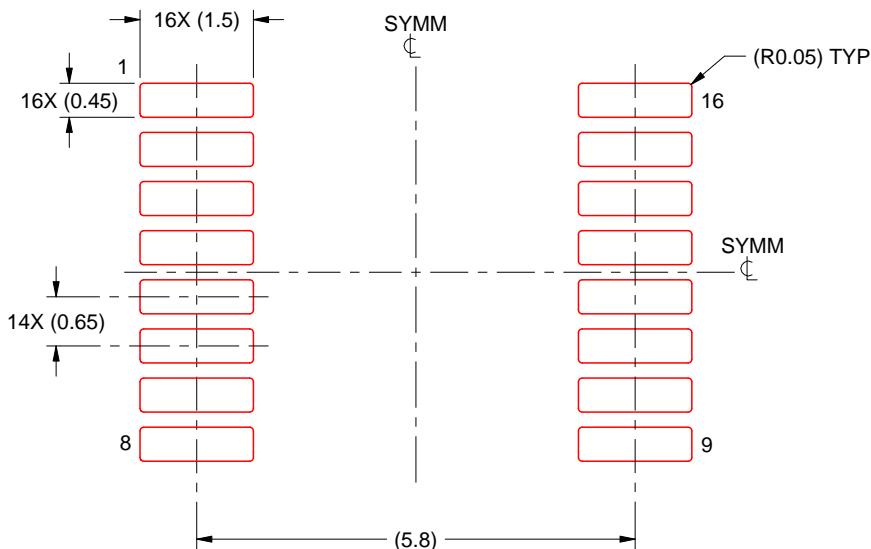
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

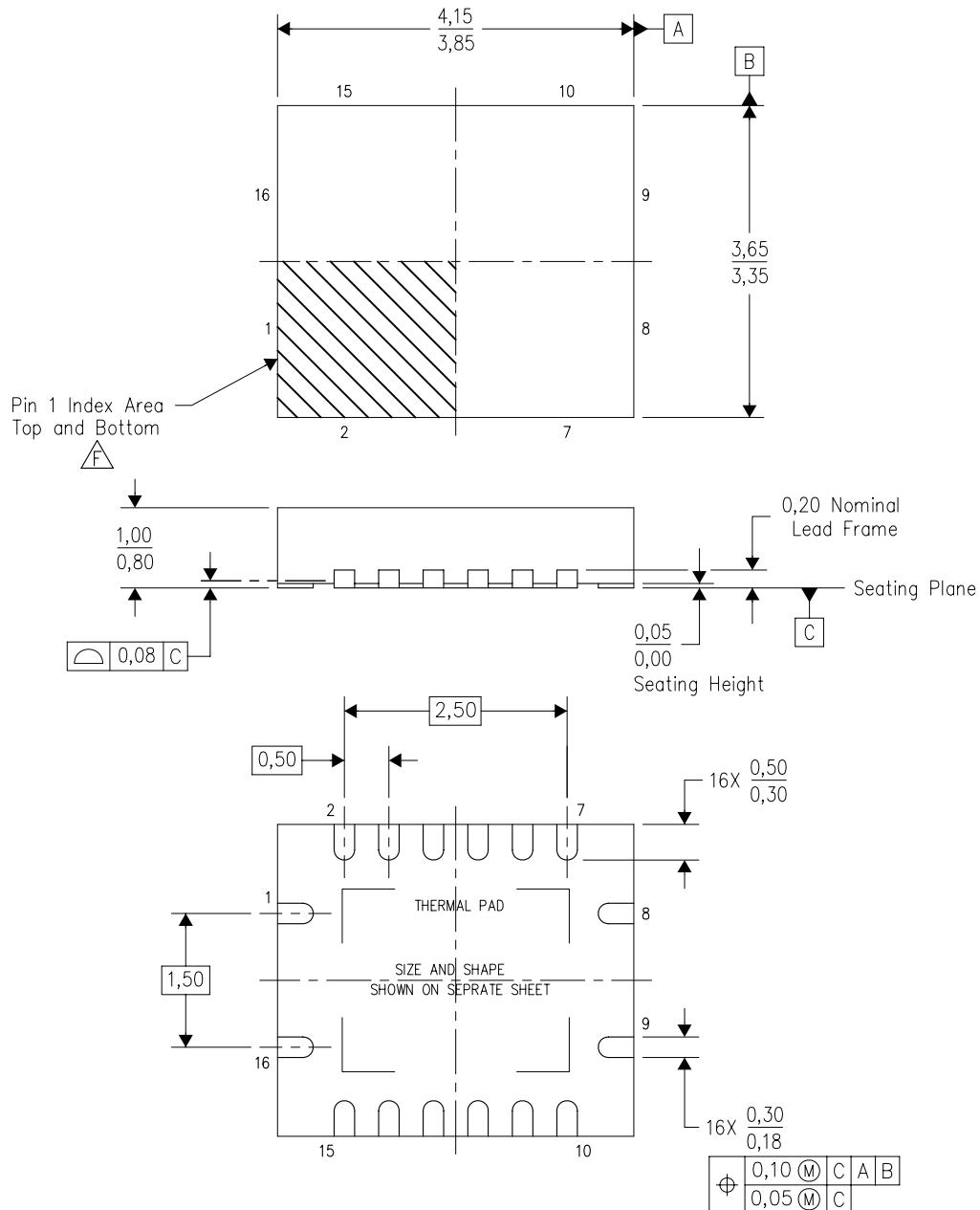
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

# THERMAL PAD MECHANICAL DATA

RGY (R-PVQFN-N16)

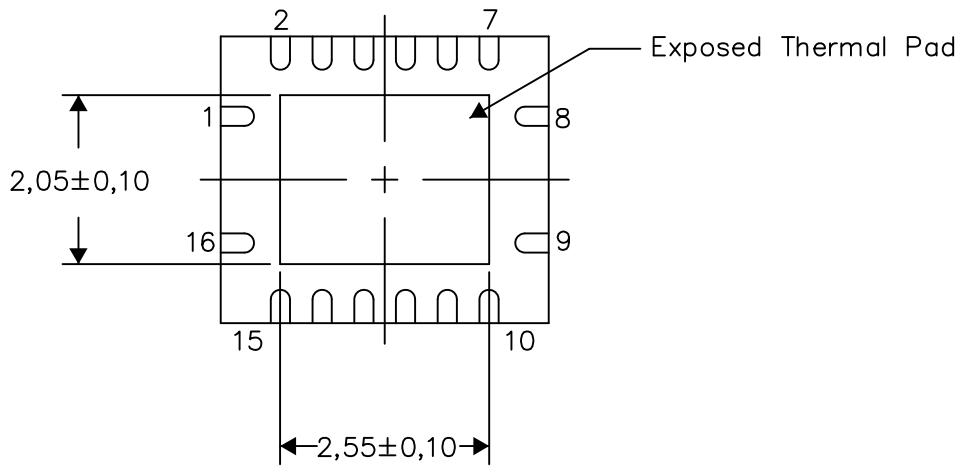
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

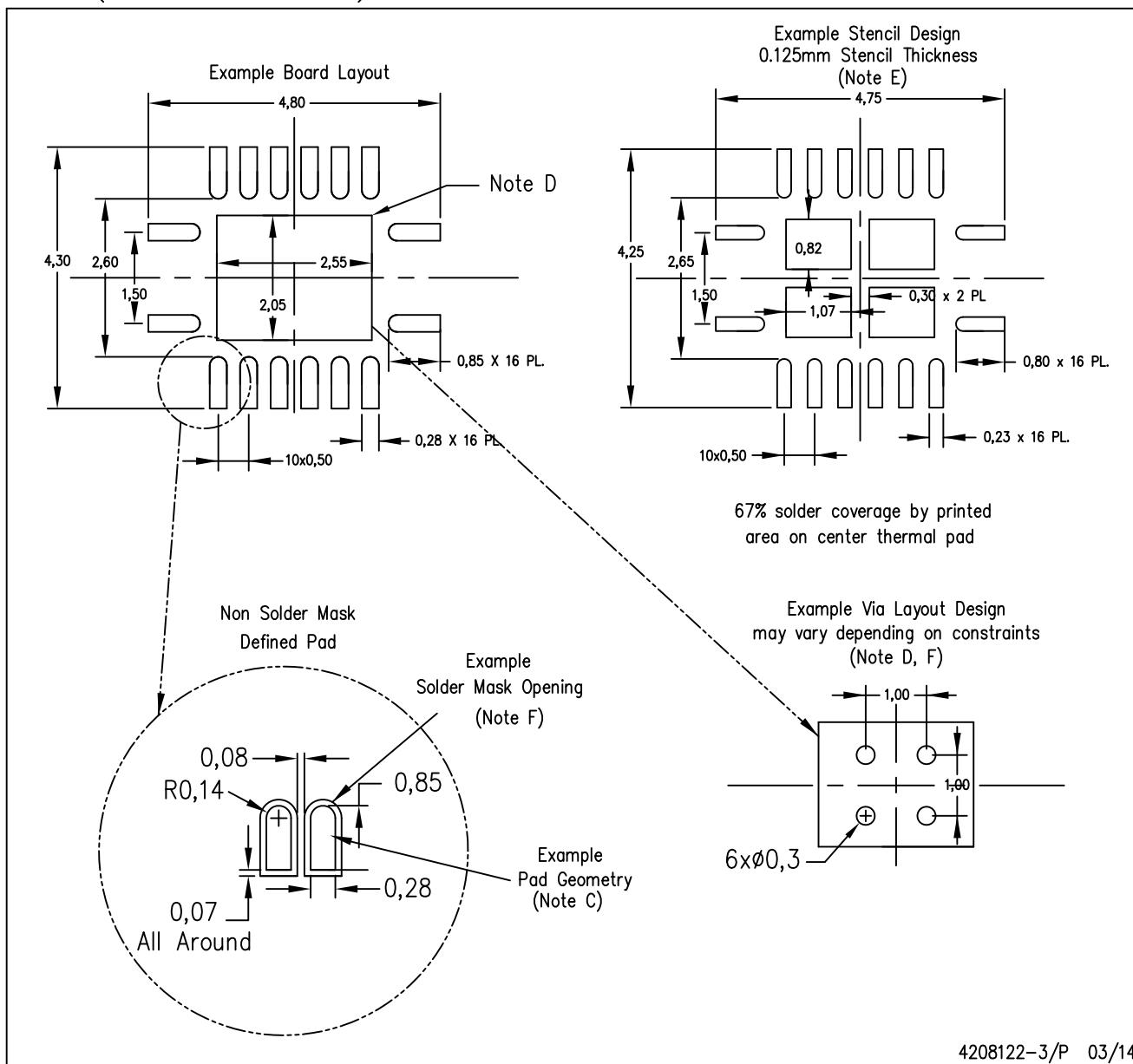
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NOTE: All linear dimensions are in millimeters

## LAND PATTERN DATA

RGY (R-PVQFN-N16)

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- NOTES:**
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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