Operational Amplifier Design

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***Abstract*—Operational amplifiers are used to create large gains with minimal distortions. The have high input impedance and low output impedance. An operational amplifier was tested with a gain of 511, a DC offset of less than 0.01V, an input resistance of 17kΩ, an output resistance of less than 27Ω, a -3dB cutoff frequency of 50Hz, an output swing of 2.1V. This amplifier was designed for a load of 200Ω.**

I. Introduction

THE objective of this experiment was to design a Operational Amplifier (Op-Amp) with $400 \leq A_V \leq 500$, $|V_{offset}|$ $\leq$0.01V, $R_{id} \geq$ 20kΩ, $R_o \leq$ 200Ω, R_L = 200Ω, $f_{L,3db} \leq$ 100Hz, and $V_{op-p} \geq$ 1.8V using standard resistors and capacitors available in the laboratory kit. The amplifier design should satisfy the presented specifications 9V maximum V_{cc}, and -9V maximum V_{ee}. [1]

Operational Amplifiers are important to create large gains with large maximum output swing. This ensures that the Op-Amp will not distort given a small input. The first stage is a differential amplifier, which helps reduce the noise from the circuit and has a high input resistance which is beneficial for Op-Amp designs. A Darlington pair is often used for its high value to improve the gain. A emitter-follower is the last stage of the Op-Amp to have a small the output resistance. High input resistance and low output resistance are important for Op-Amps as they do not disturb other circuit components if placed into a circuit.

II. System Description

The circuit in Fig. 1 was designed. It is composed of four stages and a current mirror. The first stage is a differential amplifier using Q1 and Q2. This first stage was designed initially for a gain of 100, but do to lab limitations the designed gain is 70. After the first stage was designed, the current mirror was designed to produce the necessary emitter current for Q1 and Q2. The output of the differential amplifier is cascaded into a common-emitter amplifier utilizing a Darlington pair, shown in Fig. 1 by Q3 and Q4. The second stage was designed to produce a gain of 7. The output of the second stage is cascaded into the base of Q5. This portion of the circuit removes the DC voltage offset of the output. Finally, a common-emitter amplifier is used to reduce the output resistance.

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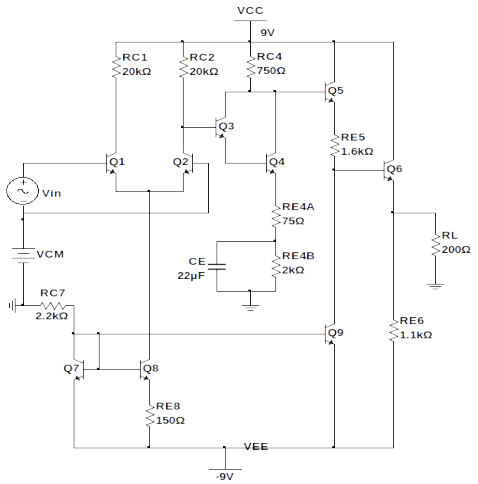

Fig. 1. Multi-Stage Amplifier Design

III. Experimental Evaluation

A. Performance Metrics

The performance of the designed amplifier is measured by its gain, input resistance, output resistance, symmetrical output swing, and DC voltage offset of the output. Additionally, this circuit's -3dB cutoff frequency was to be 100Hz. Gain was to be greater than 400 and less than 500 and is calculated by (1). Output resistance was to be less than 200Ω and is calculated by (2). Input resistance was to be greater than 20kΩ. Symmetric output swing was to be greater than 1.8V. The absolute value of the DC offset was to be less than 0.01V.

$$A_v = \frac{V_o}{V_(in)} \tag{1}$$

$$R_o = \frac{V_o - V_L}{I_L} = \frac{V_o - V_L}{\frac{V_L}{R_L}} \tag{2}$$

B. List of Materials

The required hardware and software to replicate this lab are the following: [1]

- Hardware
  - Analog Discovery 2 USB Oscilloscope (AD2)
  - Micro-USB cable
  - DC power supply
  - 1 medium β Darlington pair (MPSA-13)
  - 2 medium β NPN transistor array chips (CA3046)
  - Digilent Multimeter (DMM)
  - NI Elvis II Series Prototyping Board
- Resistors and Capacitors
  - Two 20kΩ resistors

  - 2.2kΩ resistor
  - 750Ω resistor
  - 75Ω resistor
  - 2kΩ resistor
  - 1.1kΩ resistor
  - 150Ω resistor
  - 200Ω resistor
  - Two 20kΩ resistor
  - 22μF capacitors
  - 10kΩ potentiometer
- Software
  - Digilent WaveForms

C. Experimental Procedure

The amplifier shown in Fig. 1 was constructed. The amplifier's DC operating point values were measured and recorded. Currents were found by Ohm's law, using the measured voltages and measured resistances.

To find the maximum output peak-to-peak swing, the input peak voltage was set to a high value where the output was distorted. It was set to a frequency of 1kHz. The input peak voltage was decreased until the output waveform displayed no distortion. The output peak-to-peak voltage was found by analyzing the waves and estimating peak voltages.

The input peak voltage was then set lower than the input swing and the frequency was set to 1kHz. The gain was found by measuring the output voltage, V_o, and the input voltage, V_{in}, using the AD2 oscilloscope, and (1) was employed to calculate gain. A Bode plot was found for the amplifier using the Digilent Network Analyzer tool. The gain was confirmed by the Bode plot by comparing the calculated gain with the magnitude of the Bode plot at 10kHz. The -3dB cutoff frequency was found by finding the frequency at which the gain was 3dB below the maximum gain.

The input resistance was found by placing a 10kΩ potentiometer in series with the input voltage. The voltage of the input and the voltage across the potentiometer was measured. The resistance of the potentiometer was modified and additional 20kΩ resistors were added in series to the potentiometer until the voltage across the potentiometer was half of the input voltage. The resistance of the potentiometer was then recorded as the input resistance.

The output resistance was measured by finding the open-load voltage for a given input. A resistor was then placed as a load and the voltage across the resistor was measured. The resistance of the load resistor was measured, and (2) was used to find the output resistance.

The DC offset voltage was found using the DMM to measure DC voltage across the load.

D. Results

Table 1 tabulates the DC operating conditions of the amplifier as designed, simulated, and measured in the experiment.

Table 2 tabulates the network parameters of the amplifier. The -3dB cutoff frequency was found using the Bode plot in Fig. 2.

Fig. 2 shows the Bode plot of the amplifier operating with a small load.

TABLE I
DC VOLTAGE MEASUREMENTS FROM AMPLIFIER IN FIG. 1

Circuit Component	Measured	Simulated	Designed
V_{RC1} (V)	4.34	3.8	4
V_{RC2} (V)	4.2	3.8	4
V_{RC7} (V)	8.46	8.19	8.8
V_{RE8} (V)	0.706	0.879	0.6
V_{RC4} (V)	3.08	2.96	1.35
V_{RE4A} (V)	0.311	0.22	0.2
V_{RE4B} (V)	3.45	5.82	4.8
V_{RE5} (V)	4.79	5.09	5.92
V_{RE6} (V)	9.42	8.41	8.8

TABLE II
NETWORK PARAMETERS OF AMPLIFIER IN FIG. 1

Circuit Component	Measured	Simulated	Designed
R_{in} (kΩ)	17.9	29.9	20
R_o (Ω)	27	19.0	20
Gain @ 1kHz	511.8	450	450
$\Delta V_{o,p-p}$ (V)	2.1	2	2.8
—V-Offset— (mV)	0.00	24.5	0.0
-3dB Cutoff (Hz)	52	75.1	100
Common-mode gain	0	0	0

E. Discussion of Results

Most DC measured values match designed and simulated results.

Gain and the -3dB cutoff frequency deviate from expectations. The gain is higher than expected. Because the DC bias points were within expectations, the likely cause of this AC gain deviation is differences in the values of the transistors. For the design and simulation, an approximate value of of 110 was used; however, real values of often vary significantly.

The large difference in -3dB cutoff frequency is likely a combination of experimental error and effects of limited lab equipment. The network analyzer tool used to produce this Bode plot was unable to create input voltages within the input swing range, distorting the output and thus changing the gain.

The ideal results of common-mode gain are likely the result of imprecision in measurements. The common-mode gain could not be measured as it was indistinguishable from noise. Similarly, the DC offset voltage was likely non-zero, but it was small enough that the DMM was unable to measure it.

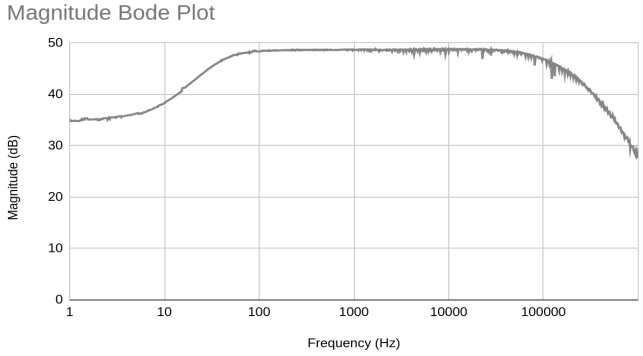

Fig. 2. Bode Plot of designed amplifier in Fig. 1

F. Limitations

This experiment was limited by the imprecision of the available instruments. For example, the AD2 oscilloscope was unable to distinguish the common-mode gain from background noise, and the AD2 waveform generator was unable to produce signals below 1mV. Moreover, the network analyzer tool of the AD2 was unable to produce inputs within the maximum input swing, distorting the Bode plot.

The power supply changed the V_{CC} and V_{EE} values by as much as 0.3V. The power supplied oscillated, adding AC noise to the circuit which was amplified by the circuit. Additionally, shielding of the circuit was impossible and the at-home nature of the lab ensures there is a high amount of background noise from wireless devices, which could be amplified by the circuit. These all contributed to variations in measured values.

Many designed values were unavailable because of the limited lab kit. This required changing the values to sub-optimal choices, which affected every stage of the design process and the implementation of the circuit. For example, no capacitance was available to produce a theoretical -3dB cutoff of 100Hz.

IV. Conclusion

The amplifier designed had a gain of 511 at 1kHz, an input resistance of 17.9kΩ, an output resistance of 27Ω, an output swing of 2.1V, a DC bias of 0V, a common-mode gain of 0, and a -3dB cutoff frequency of 50Hz.

References

[1] G. Vejarano, "Experiment #9," Loyola Marymount University, Los Angeles, CA, USA, Apr 2021.

Ian Green was born in Las Vegas, NV, USA in 2000. He is currently pursuing a B.S. in electrical engineering and computer science with a minor in mathematics, from Loyola Marymount University, with an expected graduation in 2022.

Since 2020, Ian has worked in the Bioinformatics Laboratory under Dr. John Dionisio. His research interests include bioinformatics, free-space optical communication, and computational biomedicine.

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In the summer of 2019, Jacob was an Engineering Intern with CJ Technical Solutions. Since 2020, he has been a Teaching Assistant with the Electrical Engineering Department and Mathematics Department, Loyola Marymount University in five different class sections over the last four semesters. Jacob was a recipient of the Dean's List twice for Loyola Marymount University.