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Lab Assignment 6: Overall planning and design explanation

1. Down Counter:
   Initially, we set the zero signal to be asserted only when all of the second and minute components are equal to 0, meaning that our countdown timer has finished counting down. The logic behind implementing this operation is a basic approach as the following: If the ***RST*** button is pressed, load 0 to all the second and minute components of the egg timer. But if the *load* button is pressed, then whatever the user has loaded gets forwarded to the egg timer. After these checks, our controller has sent a countdown signal to inform us whether to count down. This is achieved by a couple of if-else statements to check the states of the digits and to decrement the n_th digit if all the digits before it are equal to 0.

2. Counter
   Counter module acts as a clock divider from 1000 Hz to 1 Hz. It basically counts from 0 to 999 in 1 second. The counting starts after *start* input is detected, and at the end of the counting positive *endd* output is given.

3. Controller
   Controller module is used to connect user inputs, counter module, and down counter module together. It sends a *load* signal when input from **PRESET** is detected. When the **START** button is pressed, it starts the counter module for the first time. Each time after receiving *endd* signal from counter, it starts another counter. And each time after receiving *endd* signal, it sends *countdown* signal to down counter module to count down. When *zero* input is received from the downcounter, meaning that the number on the timer is 00:00, the controller stops sending *countdown* signals.