POSTAL Study Course 2018

Computer Science & IT

Objective Practice Sets

Digital Logic

Contents

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1 CHAPTER

Basics of Digital Logic

Q.1 Let $a_n a_{n-1} \ldots a_1 a_0$ be the binary representation of an integer b. The integer b is divisible by 3 if

(a) The difference of alternates sums, i.e. $(a_0 + a_2 + \ldots) - (a_1 + a_3 + \ldots)$ is divisible by 3

(b) The number of ones is divisible by 3

(c) The number of ones is divisible by 3, but not by 9

(d) The number of zeros is divisible by 3

Q.2 Convert $(3121.121)_4$ to base 3?

(a) 10022.100 (b) 22001.100

(c) 22001.101 (d) 10022.110

Q.3 $(10110011100011110000)_2$ in base 32 are

(a) 2214716 (b) 1192331

(c) 11976 (d) 11142316

Q.4 $(22)_4 + (101)_3 - (20)_5 = (x)_4 + (4)_{x-1}$ where $x > 4$. The value of x is:

(a) 6 (b) 4

(c) 12 (d) 8

Q.5 The hexadecimal representation of $(657)_8$ is

(a) $(1AF)_H$ (b) $(D78)_H$

(c) $(D71)_H$ (d) $(32F)_H$

Q.6 Convert 10010011 (BCD code) into binary. The value of obtained in binary will be equal to_____ in decimal

Q.7 In a particular number system having base B. $(\sqrt{41})_B = 5_{10}$. The value of 'B' is _____.

Q.8 The number of 1s in the binary representation of (3 * 4096 + 15 * 256 + 5 * 16 + 3) are

(a) 8 (b) 9

(c) 10 (d) 12

Q.9 The decimal value 0.25

(a) is equivalent to the binary value 0.1

(b) is equivalent to the binary value 0.01

(c) is equivalent to the binary value 0.00111...

(d) cannot be represented precisely in binary

Q.10 The binary equivalent of the decimal number 0.4375 is

(a) 0.0111 (b) 0.1011

(c) 0.1100 (d) 0.1010

Q.11 Two numbers –48 and –23 are added using 2's complement. The 2's complement of the result using 8 bit representation is _____

(a) 10111001 (b) 01000111

(c) 01101010 (d) 11100111

Q.12 A number N is stored in a 4-bit 2's complement representation as

a_3	a_2	a_1	a_0

it is copied into a 6-bit register and after a few operations, the final bit pattern is

a_3	a_3	a_2	a_1	a_0	1

The value of this bit pattern in 2's complement representation is given in terms of the original number in N as

(a) $32a_3 + 2N + 1$ (b) $32a_3 - 2N - 1$

(c) $2N - 1$ (d) $2N + 1$

Q.13 A number in 4-bit two's complement representation is $X_3 X_2 X_1 X_0$. This number when stored using 8-bits will be

(a) $0\,0\,0\,0\,X_3 X_2 X_1 X_0$

(b) $1\,1\,1\,1\,X_3 X_2 X_1 X_0$

(c) $X_3 X_3 X_3 X_3 X_3 X_2 X_1 X_0$

(d) $\bar{X}_3 \bar{X}_3 \bar{X}_3 \bar{X}_3 \bar{X}_3 X_2 X_1 X_0$

Q.14 What range of decimal integers can be represented by n-bit two's complement representation?

(a) $-(2^{n-1})$ to $+(2^{n-1}-1)$
(b) $-(2^{n-1}+1)$ to $+(2^{n-1}-1)$
(c) $-(2^{n})$ to $+(2^{n-1}-1)$
(d) $-(2^{n-1})$ to $+(2^{n-1})$

Q.15 The greatest negative number which can be stored in computer that has 8-bit word length and uses 2's complement arithmetic is
(a) –256 (b) –255
(c) –128 (d) –127

Q.16 Result of the subtraction with the following unsigned decimal numbers by taking the 10's complement of the subtrahend. 1753 – 8640
(a) 3113 (b) 10393
(c) –6887 (d) –3113

Q.17 Number $(+46.5)_{10}$ can be represented as a floating point binary number with 24 bits. The normalized fraction mantissa has 1 bits and the exponent has 8 bits. The mantissa of the number is
(a) 0101110100000000
(b) 1001110100000000
(c) 0000011000000000
(d) 0000000001011101

Q.18 Given that $(EOB)_H - (ABF)_H = Y$. The radix 8's compliment of Y is
(a) 844 (b) 1514
(c) 6264 (d) 3251

Q.19 4-bit 2's complement representation of a decimal number is 1000. The number is

Q.20 Which of the following statement is **incorrect** for the range of n bits binary numbers?
(a) Range of unsigned numbers is 0 to $2^n - 1$.
(b) Range of signed numbers is $-2^{n-1} + 1$ to $2^{n-1} - 1$
(c) Range of signed 1's compliment numbers is $-2^{n-1} + 1$ to 2^{n-1}
(d) Range of signed 2's compliment numbers is -2^{n-1} to $2^{n-1} - 1$

Q.21 Let A = 1111 1010 and B = 0000 1010 be two 8-bit 2's complement numbers. Their product in 2's complement is
(a) 1100 0100
(b) 1001 1100
(c) 1010 0101
(d) 1101 0101

■■■■

Answers Basics of Digital Logic

1.	(a)	2.	(c)	3.	(a)	4.	(a)	5.	(a)	8.	(c)	9.	(b)	10.	(a)	11.	(b)	12.	(d)
13.	(c)	14.	(a)	15.	(c)	16.	(c)	17.	(c)	18.	(a)	20.	(c)	21.	(a)				

Explanations Basics of Digital Logic

1. (a)

Consider 1 0 1 0 1 0 1 1

a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0

Number of 1 in even places = 1

Number of 1 in odd places = 4

The difference (4 – 1) is dividable by 3

binary number 10101011 = 171 (decimal no. is divisible by 3)

2. (c)

$3121 = 3 \times 4^3 + 1 \times 4^2 + 2 \times 4^1 + 1 \times 4^0 = 217$

$0.121 = 1 \times 4^{-1} + 2 \times 4^{-2} + 1 \times 4^{-3} = 0.390$

3	217		
3	72	—	1
3	24	—	0
3	8	—	0
3	2	—	2
	2		

$= (22001)_3$

$0.390 \times 3 = 1.17$

$0.17 \times 3 = 0.51$

$0.51 \times 3 = 1.53$

$= (0.101)^3$

So $(217.390)_{10} = (22001.101)_3$

3. (a)

To convert to base 8, we group in 3's, because $2^3 = 8$.

To convert to base 16, we group in 4's because $2^4 = 16$.

To convert to base 32, we group in 5's because $2^5 = 32$.

Grouping in 5's, from the right we get the answer.

So $\underset{22}{\underline{10110}}$ $\underset{14}{\underline{01110}}$ $\underset{7}{\underline{00111}}$ $\underset{16}{\underline{10000}}$

4. (a)

$(22)_4 + (101)_3 - (20)_5 = (x)_4 + (4)_{x-1}$

$\Rightarrow 4 \times 2 + 2 \times 4^0 + 1 \times 3^2 + 0 + 1 \times 3^0 - [5 \times 2 + 0] = 4^0 + x + (x-1)^0 \times 4$

$\Rightarrow 8 + 2 + 9 + 1 - [10] = x + 4$

$\Rightarrow 10 + 10 - 10 = x + 4$

$\Rightarrow 10 = x + 4$

$\Rightarrow x = 6$

5. (a)

Octal number 657_8

Binary representation of 657_8

$\underline{0\,0\,0\,1}$ $\underline{1\,0\,1\,0}$ $\underline{1\,1\,1\,1}$

Hexadecimal representation of $(657)_8$

$= (1\,AF)_H$

6. (93)

As $10010011 \rightarrow \underbrace{01011101}_{\text{binary}} = (93)_{10}$

7. (6)

squaring both side, $(\sqrt{41})^2 = (5)^2$

$(41)_B = (25)_{10}$

$(4B + 1)_{10} = (25)_{10}$

$\Rightarrow B = 6$

8. (c)

3*4096 + 15*256 + 5*16 + 3

As we can see that

$4096 = 2^{12}$ have one 1

$256 = 2^8$ have one 1

$16 = 2^4$ have one 1

Hence, they only remain as same in number of 1's and when any other number is multiplied by themselves, the number of 1's is only the count of the number of 1's in other multiplicant.

$\left.\begin{array}{l} 3 - 011 \\ 15 - 1111 \\ 5 - 0101 \\ 3 - 011 \end{array}\right]$ 10 1's

∴ Correct option is (c)

9. (b)

$(0.25)_{10} \Rightarrow$

0.25	0.5
×2	×2
0.50	1.0
↓	↓
0	1

$\therefore (0.25)_{10} = (0.01)_2$

10. (a)

$(0.4375)_{10}$

(i)		(ii)		(iii)	
0.4375		0.8750		0.75	
×2		×2		×2	
0.8750	↗	1.7500	↗	1.50	
↓		↓		↓	
0		1		1	

(iv) 0.50
×2
1.0
↓
1

$\therefore (0.4375)_{10} = (0.0111)_2$

Hence, (a) is correct option

11. (b)

$(-48)_{10} + (-23)_{10}$

–48	11010000
–23	(+)11101001
–71	10111001

2's complement of a 2's complement number is the number itself.

Here answer –71 is in 2's complement.

2's complement of 10111001 is 01000111

12. (d)

Given number is $\boxed{a_3 \mid a_2 \mid a_1 \mid a_0}$ in 2's complement form.

We know that in 2's complement form. If we copy MSB any number of times the number remains unchanged.

So, $a_3\, a_2\, a_1\, a_0 = a_3\, a_3\, a_2\, a_1\, a_0 = N$

When we left shift a number by 1 bit then it is multipled by 2, so, $a_3\, a_3\, a_2\, a_1\, a_0 0 = 2N$

Now, $a_3\, a_3\, a_2\, a_1\, a_0 0 + 1 = a_3\, a_3\, a_2\, a_1\, a_0 1 = 2N + 1$

13. (c)

Suppose we have to represent a number +5 and –5 in 2's complement representation using 8-bits

+5 = 0 0 0 0 0 1 0 1

–5 = 11111011 (Using 2's complement)

From the above example we conclude that when $X_3\, X_2\, X_1\, X_0$ number will be stored in 2's complement method using 8-bit will be $X_3\, X_3\, X_3\, X_3\, X_3\, X_2\, X_1\, X_0$.

16. (c)

$$\begin{array}{r} 1753 \\ +\ 1360 \\ \hline 3113 \end{array} \longrightarrow \text{10's complement } -6887$$

17. (a)

As $46.5 = (101110.1)_2$

$$\underbrace{0101110100000000}_{\text{mantissa}} \quad \underbrace{00000110}_{\text{exponent}}$$

18. (c)

$(EOB)_H - (ABF)_H = (34C)_H$

$(34C)_H = (001101001100)_2$

$= (1514)_8$

7's compliment $= (6263)_8$

8's compliment $= (6263)_8 + 1 = (6264)_8$

19. (–8)

1000

MSB is 1 so, –ve number

Take 2's complement for magnitude.

$$\begin{array}{r} 0111 \\ +\ \ 1 \\ \hline 1000 \end{array} = -8$$

20. (c)

Range of signed 1's compliment number is $-2^{n-1} + 1$ to $2^{n-1} - 1$.

21. (a)

A = 11111010

Since MSB is 1 hence no. is negative i.e. –(00000110)

$= -(00000110)$

$A = -6$

$B = 00001010,$

there is no. 2's complement representation for positive no. $B = +10$

$A \times B = 10 \times (-6) = -60$

Binary representation of – 60 = 00111100

Now take 2's complement = 11000100

■■■

2 CHAPTER

Boolean Algebra and Minimization Techniques

Q.1 A Boolean expression $f(A, B, C)$ is represented in its pictorial form as shown below. The function $f(A, B, C)$ is

AB \ C	0	1
00	0	1
01	1	1
10	1	0
11	1	1

(a) $(\bar{A}C + A\bar{C} + \bar{B})'$

(b) $[\bar{B}(\bar{A} + C)(A + \bar{C})]'$

(c) $[(A + B + C)(\bar{A} + B + \bar{C})]'$

(d) $(ABC + \bar{A}B\bar{C})'$

Q.2 The maximum number of Boolean expressions that can be formed for the function $f(x, y, z)$ satisfying the relation $f(\bar{x}, y, \bar{z}) = f(x, y, z)$ is

(a) 16 (b) 256
(c) 8 (d) 12

Q.3 Match **column-I** with **column-II**

Column-I	Column-II
(a) $(A \oplus B) \oplus (B \oplus C)$	**1.** $(A \odot C)$
(b) $AB \oplus \bar{A}C + BC$	**2.** $(A + B) \odot (A + C)$
(c) $(A \odot B) \odot (B \odot C)$	**3.** $AB \oplus \bar{A}C$
(d) $A + (B \odot C)$	**4.** $(A \oplus C)$
	5. $\bar{A}C \oplus AC$

Codes

	A	B	C	D
(a)	4	3	1	2
(b)	3	4	1	2
(c)	2	3	1	2
(d)	4	3	5	2

Q.4 Which of the following functions implement the *K*-map shown below?

AB \ CD	00	01	11	10
00	0	x	1	0
01	x	1	0	1
11	1	1	0	x
10	0	1	1	0

(a) $BC' + BD + BD'$ (b) $BD + A'B + C'D$
(c) $B'D + BD' + C'D$ (d) $B'D + BD' + CD$

Q.5 The switching expression corresponding to $f(A, B, C, D) = \Sigma(0,3,4,7,8)$ and $\sum_d(10, 11, 12, 14, 15)$ where d : don't care

(a) $\bar{C}\bar{D} + B\bar{C}$ (b) $C \odot D$
(c) $C \oplus D$ (d) CD

Q.6 For the following Boolean equation, the value of A, B and C will be $AB + \bar{A}C = 1$, $AC + B = 0$

(a) 1, 1, 1 (b) 1, 1, 0
(c) 0, 0, 1 (d) 0, 0, 0

Q.7 The k-map for the boolean function F of 4 boolean variables is given below where A, B, C are don't care conditions. What values of A, B, C will result in the minimal expression?

WX \ YZ	00	01	11	10
00	0	0	A	0
01	0	1	1	0
11	1	B	C	0
10	0	0	1	0

(a) $A = B = C = 1$ (b) $B = C = 1$; $A = 0$
(c) $A = C = 1$; $B = 0$ (d) $A = B = 1$; $C = 0$

Q.8 The well known fibonacci numbers are 1 1 2 3 5 8 13... Let the boolean variables a, b and c together represent a 3-bit non-negative binary number (that is, not in 2's compliment representation).

Let c be the least significant bit (that is, write the number as abc). Let F be a boolean variable that indicates whether the number represented by a, b, c is a Fibonacci number. (F=1 if it is fibonacci number and 0 otherwise). Determine the minimized sum of product formula for F.

(a) $F = a'c + b'c$ (b) $F = a'b + b'c$
(c) $F = a'b + a'c$ (d) none of these

Q.9 The Boolean Expression $\overline{B \oplus E}$ is a simplified version of expression:

$\bar{A}BE + BCDE + B\bar{C}\bar{D}E + \bar{A}\bar{B}D\bar{E} + \bar{B}\bar{C}D\bar{E} + \bar{A}\bar{B}\bar{D}\bar{E}$

then which of the following choice is correct:

1. don't care conditions don't exist
2. don't care conditions exist
3. d(16, 18, 20, 23, 27, 29) is the set of don't care conditions
4. d(16, 20, 22, 27, 29) is the set of don't care conditions

(a) 1 only (b) 2 and 3 only
(c) 2 and 4 only (d) Data insufficient

Q.10 Boolean expression $\overline{A+\bar{B}+C} + \overline{\bar{A}+\bar{B}+C} + \overline{A+\bar{B}+\bar{C}} + ABC$ reduces to

(a) A (b) B
(c) C (d) $A+B+C$

Q.11 The minimized expression for the given K-map (X: don't care) is

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	X	X	1
11	X	X	1	X
10	1	0	1	1

(a) $A + \bar{B}C$ (b) $B + AC$
(c) $C + AB$ (d) ABC

Q.12 The black box in the below figure consists of a minimum complexity circuit that uses only AND, OR and NOT gates.

The function $f(x, y, z) = 1$ whenever x, y are different and 0 otherwise. In addition the 3 inputs x, y, z never contain the same value. Which one of the following equations leads to the correct design for the minimum complexity circuit?

(a) $x'y + xy'$ (b) $x + y'z$
(c) $x'y'z' + xy'z$ (d) $xy + y'z + z'$

Q.13 Find the correct function for the following k-map

DE \ BC	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	0	0	1	0
10	1	0	0	1

$A = 0$

DE \ BC	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	0	0	1	0
10	1	0	0	1

$A = 1$

(a) $\bar{A}CE + BCE + AC\bar{D}E$
(b) $\bar{C}\bar{E} + BCE + C\bar{D}E$
(c) $AE + \bar{C}\bar{E} + BCE$
(d) $\bar{C}\bar{E} + C\bar{D}E + BCD$

Q.14 Minimal POS obtained from $Y = \Sigma m(0, 2, 3, 6, 7) + \Sigma d(8, 10, 11, 15)$

(a) $\bar{A}C + \bar{B}\bar{D}$ (b) $\bar{A}(C + \bar{D})(\bar{B} + C)$
(c) $(AC + \bar{B}\bar{D})$ (d) None of these

Q.15 If $Y = \overline{ABC + \bar{A}\bar{B}} + BC$ then dual and compliment of Y are respectively

(a) $(ABC + \bar{A}\bar{B}) \cdot (B + C)$ and $\left[(\overline{A+B+C}) + (\bar{A}+\bar{B})\right] \cdot BC$

(b) $\left[(A + B + C + \bar{A} \cdot \bar{B})\right] \cdot \overline{BC}$ and $\left[ABC + (\overline{A+B})\right] \cdot \overline{BC}$

(c) $\left[(\overline{A+B+C}) + (\overline{\bar{A} \cdot \bar{B}})\right] \cdot (B + C)$ and $(ABC + \bar{A}\bar{B}) \cdot \overline{BC}$

(d) $\left[\overline{ABC} + \overline{\bar{A}+B}\right] \cdot \overline{BC}$ and $\left[(A + B + C) + \overline{\bar{A}\bar{B}}\right] \cdot BC$

Q.16 The logic function $f = \overline{(x \cdot \bar{y}) + (\bar{x} \cdot y)}$ is the same as

(a) $f = x \oplus y$ (b) $f = x \odot y$
(c) $f = x + y$ (d) None of these

Q.17 The boolean expression A + BC equals

(a) $(\bar{A}+\bar{B})(A+C)$ (b) $(A+B)(A+C)$

(c) $(A+B)(\bar{A}+C)$ (d) None of these

Q.18 The SOP form of given function

$y = \overline{(A+\bar{B}+\bar{C}+D)\cdot(\bar{A}+B)}$ is

(a) $y = A\bar{B}\bar{C}D + \bar{A}B$

(b) $y = \overline{A\bar{B}\bar{C}D + \bar{A}B}$

(c) $y = \overline{\bar{A}BC\bar{D} + A\bar{B}}$

(d) $y = \bar{A}BC\bar{D} + A\bar{B}$

Q.19 Which of the following functions implements the Karnaugh map shown below?

AB \ CD	00	01	11	10
00	0	0	1	0
01	×	×	1	×
11	0	1	1	0
10	0	1	1	0

(a) $\bar{A}B + CD$ (b) $D(C+A)$

(c) $AD + \bar{A}B$ (d) $(C+D)(\bar{C}+D)(A+B)$

Q.20 Consider a four variable K-map shown below:

AB \ CD	00	01	11	10
00	1	1		1
01		1	1	
11	1		1	1
10	1			1

The total number of all possible Non Essential-Prime Implicants (NEPIs) is

(a) 6 (b) 5

(c) 4 (d) 3

Q.21 Consider a 3 variable function $f(P, Q, R)$ having min terms representation as,

$f(P, Q, R) = \Sigma m(3, 5, 6, 7)$

How many minimum NAND gates required to implement above expression?

(a) 2 (b) 3

(c) 5 (d) 6

■■■

Answers Logic Functions

1.	(b)	2.	(a)	3.	(a)	4.	(c)	5.	(b)	6.	(c)	7.	(a)	8.	(b)	9.	(c)
10.	(b)	11.	(a)	12.	(a)	13.	(b)	14.	(b)	15.	(c)	16.	(b)	17.	(b)	18.	(d)
19.	(b)	20.	(b)	21.	(d)												

Explanations Logic Functions

1. (b)

Representing the graph in K-map

$f(A, B, C) = B + A\bar{C} + \bar{A}C$

$f(A, B, C) = \overline{\left(B + A\bar{C} + \bar{A}C\right)}$

$f(A, B, C) = \overline{\left[\bar{B}(\bar{A}+C)(A+\bar{C})\right]}$

AB \ C	0	1
00	0	1
01	1	1
11	1	1
10	1	0

2. (a)

For every combination of x, y, z the function value remains same for input $\bar{x}, y, \bar{z}$.

x y z	$f(x, y, z) = f(\bar{x}, y, \bar{z})$
0 0 0 1 0 1	either 0 or 1
0 0 1 1 0 0	either 0 or 1
0 1 0 1 1 1	either 0 or 1
0 1 1 1 1 0	either 0 or 1

Effectively there are only four rows for the truth table of the function $f(x, y, z)$.

∴ Total Boolean expressions possible is $2^4 = 16$.

3. (a)

$(A \oplus B) \oplus (B \oplus C)$

$\Rightarrow (\overline{A \oplus B})(B \oplus C) + (A \oplus B)(\overline{B \oplus C})$

$\Rightarrow (AB + \bar{A}\bar{B})(A\bar{B}C + B\bar{C}) + (\bar{A}B + A\bar{B})(BC + \bar{B}\bar{C})$

$\Rightarrow AB\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C}$

$\Rightarrow \bar{A}C(B + \bar{B}) + A\bar{C}(B + \bar{B})$

$(\bar{A}C + A\bar{C}) = A \oplus C$

(a) matches with (4)

$AB \oplus AC + BC = AB \oplus \bar{A}C$

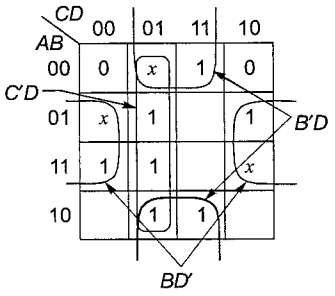
This is concensus law in XOR algebra.

(b) matches with (3)

$A + (B \odot C) = \underbrace{(A + B) \odot (A + C)}_{\text{Follows distributive law}}$

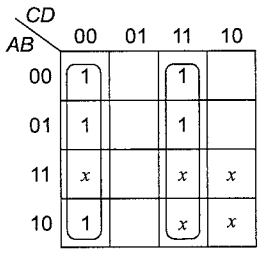
Option (d) matches with (2).

4. (c)



So, $B'D + BD' + C'D$

5. (b)



$\Rightarrow \bar{C}\bar{D} + CD = C \odot D$

6. (c)

From $AC + B = 0 \Rightarrow B = 0$

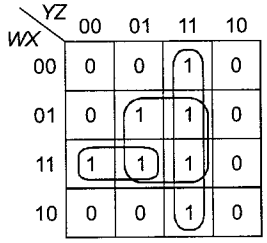
from $AB + \bar{A}C = 1$ and $B = 0$

$\Rightarrow \bar{A}C = 1 \Rightarrow A = 0$ and $C = 1$

Thus$(A, B, C) = (0, 0, 1)$

7. (a)

For minimal expression



For $A = B = C = 1$

It will give the minimal expression.

8. (b)

Fibonacci numbers are: 1, 1, 2, 3, 5, 8...

Fibonacci numbers with 3 digits in its binary representation are

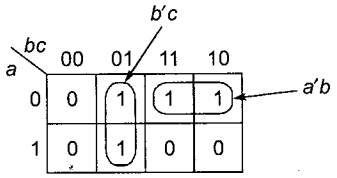
1 0 0 1

2 0 1 0

3 0 1 1

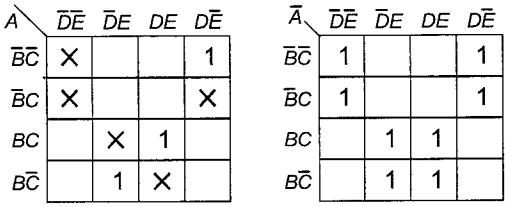
5 1 0 1

using K-map we can get minimized SOP formula for it



$\Rightarrow \quad F = \bar{a}b + \bar{b}c$

9. (c)



Only (c) option satisfies the required condition.

10. (b)

$\overline{A + \bar{B} + C} + \overline{\bar{A} + \bar{B} + C} + \overline{A + \bar{B} + \bar{C}} + ABC$

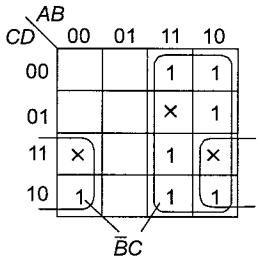
$= \bar{A} \cdot B \cdot \bar{C} + AB\bar{C} + \bar{A}BC + ABC$

$= \bar{A}B(\bar{C} + C) + AB(\bar{C} + C)$

$= \bar{A}B + AB$

$= B(\bar{A} + A) = B \qquad [\text{using } x + \bar{x} = 1]$

11. (a)



The expression is $Y = A + \bar{B}C$

12. (a)

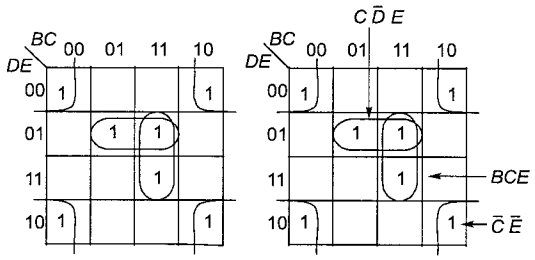
x	y	z	$f(x,y,z)$
0	1	0 or 1	1
1	0	0 or 1	1

So, $F(x,y,z) = \bar{x}y\bar{z} + \bar{x}yz + x\bar{y}\,\bar{z} + x\bar{y}z$

$= \bar{x}y(\bar{z} + z) + x\bar{y}(\bar{z} + z)$

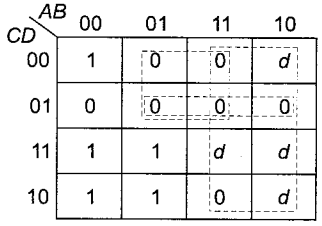
$= \bar{x}y + x\bar{y}$

13. (b)



$F = \bar{C}\bar{E} + C\bar{D}E + BCE$

14. (b)



$\Rightarrow \quad \bar{A}(C + \bar{D})(\bar{B} + C)$

15. (c)

$Y = \overline{ABC + \bar{A}\bar{B}} + BC$

Dual of Y

$Y_d = \overline{(A + B + C)\cdot(\bar{A} + \bar{B})}\cdot(B + C)$

$= \left[\overline{(A + B + C)}\cdot\overline{(\bar{A} + \bar{B})}\right]\cdot(B + C)$

Compliment of Y

$Y_c = \overline{\overline{(ABC + \bar{A}\bar{B})} + BC}$

$= \overline{\overline{(ABC + \bar{A}\bar{B})}}\cdot\overline{BC}$

$= (ABC + \bar{A}\bar{B})\cdot\overline{BC}$

16. (b)

$f = \overline{(x\cdot\bar{y}) + (\bar{x}\cdot y)}$

$= \overline{(x\cdot\bar{y})}\cdot\overline{(\bar{x}\cdot y)}$

$= (\bar{x} + y)\cdot(x + \bar{y})$

$= xy + \bar{x}\,\bar{y} = x \odot y$

or $(x\cdot\bar{y}) + (\bar{x}\cdot y) = \oplus$, complement of $\oplus$ is $\odot$.

17. (b)

$A + BC$ represents the distributive law which can be expanded as

$A + BC = (A + B)\cdot(A + C)$

18. (d)

$y = \overline{(A + \bar{B} + \bar{C} + D)\cdot(\bar{A} + B)}$

$= \overline{(A + \bar{B} + \bar{C} + D)} + \overline{(\bar{A} + B)}$

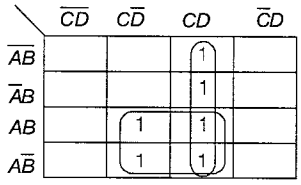
$= (\bar{A}\cdot\bar{\bar{B}}\cdot\bar{\bar{C}}\cdot\bar{D}) + (\bar{\bar{A}}\cdot\bar{B}) = \bar{A}BC\bar{D} + A\bar{B}$

19. (b)

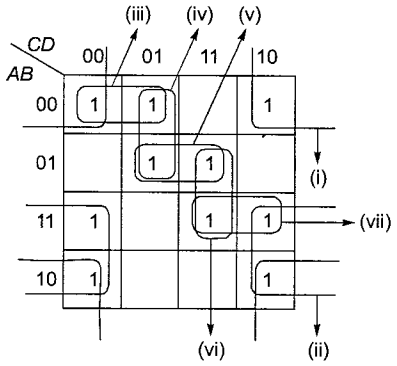
Solving the given k-map we have

$f = AD + CD$

$f = D(C + A)$



20. (b)



Group-(i) → NEPI → $\bar{B}\bar{D}$

Group-(ii) → NEPI → $A\bar{D}$

Group-(iii) → NEPI → $\bar{A}\bar{B}\bar{C}$

Group-(iv) → NEPI → $\bar{A}\bar{C}D$

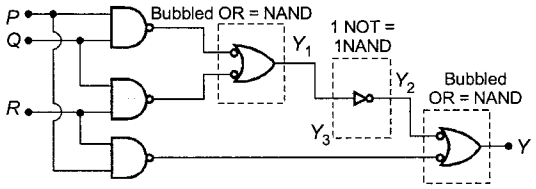
Group-(v) → NEPI → $\bar{A}BD$

Group-(vi) → NEPI → BCD

Group-(vii) → NEPI → ABC

21. (d)

Realization of 'Y' by using only NAND gates is given as below:



$$Y = \overline{Y_3 \cdot Y_2} = \overline{(\overline{PR})(\overline{Y_1})}$$

$$= \overline{(\overline{PR})(\overline{PQ+QR})}$$

$$= \overline{\overline{PR}} + \overline{\overline{PQ+QR}}$$

$$= PR + PQ + QR$$

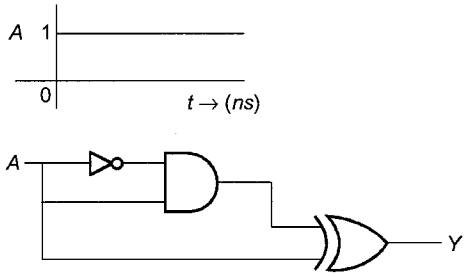
∴ Minimum # NAND gates required = 6.

■■■

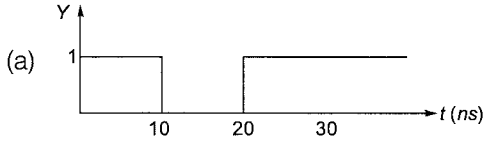
3 CHAPTER

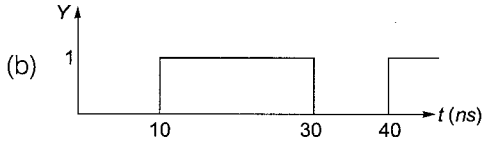
Logic Gates and Switching Circuits

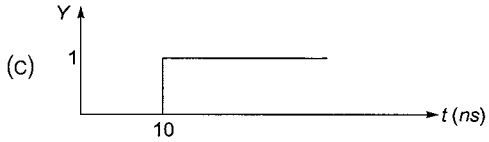
Q.1 Consider the circuit shown in figure below

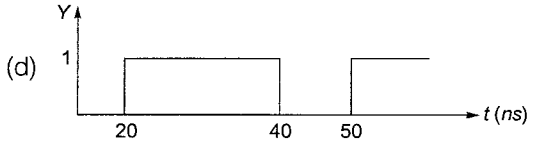


If propagation delay of NOT gate is 10 nsec, AND gate is 20 nsec and *X-OR* gate is 10 nsec. If *A* is connected to V_{CC} at t = 0, then waveform for output *Y* is

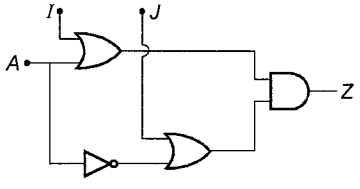
(a)


(b)


(c)


(d)


Q.2 The circuit shown below is to be used to implement the function $Z = f(A, B) = \overline{A} + B$. The values of *I* and *J* are



(a) $I = 0$ and $J = B$ (b) $I = 1$ and $J = B$
(c) $I = B$ and $J = 1$ (d) $I = B$ and $J = 0$

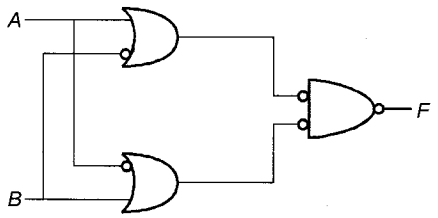
Q.3 $Y = f(A, B) = \Pi M\,(0, 1, 2, 3)$ represents (*M* is Maxterm)

(a) NOR gate
(b) NAND gate
(c) OR gate
(d) a situation where output is independent of input

Q.4 The minimum number of NAND gates required to implement the boolean function *ABCDE* + *ABCD* + *ABC* + *AC* + *C* is

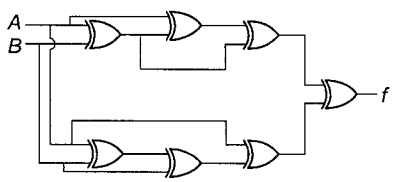
(a) 0 (b) 1
(c) 4 (d) 7

Q.5 The Boolean expression corresponding to the given circuit



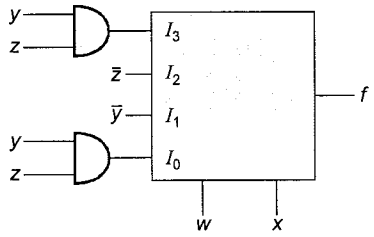
(a) is independent of *A*
(b) is an inconsistency
(c) is a tautology
(d) none of these

Q.6 The output '*f*' of the given circuit is _____.

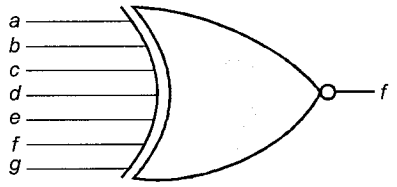


(a) 0 (b) 1
(c) *A* (d) *B*

Q.7 The given multiplexer diagram can be expressed in canonical SOP form. If a function is defined as $f(w, x, y, z)$ then what will be the number of minterms in canonical SOP form?



Q.8 Consider a 7 input EXNOR gate shown in the Figure below



The seven input EXNOR gate acts as

(a) Odd function (b) Even function
(c) Identity function (d) Both (b) and (c)

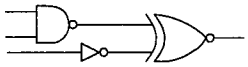
Q.9 Minimum number of 2-input NOR Gates required to implement the function.

$$f = \bar{A} + \overline{\left[B + \bar{C}(AB + A\bar{C})\right]}$$

Q.10 Which of the following expressions is not equivalent to $\bar{x}$?

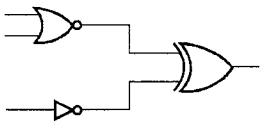
(a) x NAND x (b) x NOR x
(c) x NAND 1 (d) x NOR 1

Q.11 A positive level logic digital circuit is shown below

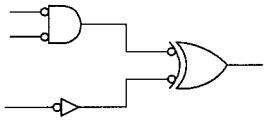


The negative level logic digital circuit for the given circuit is

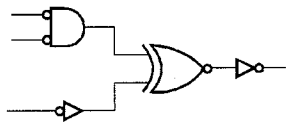
(a)



(b)



(c)

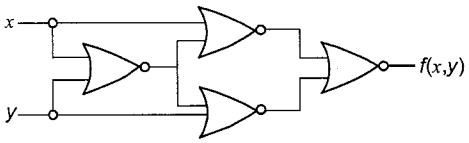


(d) All of these

Q.12 Consider $Y = A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A \oplus \bar{A} \oplus \bar{A} \oplus A \oplus A$ then Y is equivalent to:

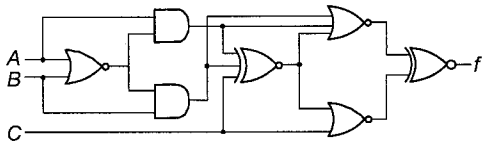
(a) 1 OR A (b) A EXOR 0
(c) 1 NOR $\bar{A}$ (d) A AND A

Q.13 Identify the logic function performed by the circuit shown in the given figure



(a) exclusive OR (b) exclusive NOR
(c) NAND (d) NOR

Q.14 The following circuit

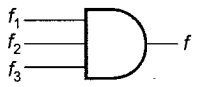


can be represented as:

(a) C
(b) $f(A, B, C) = \Sigma(0, 1, 2, 3, 4, 5, 6, 7)$
(c) $(A \oplus B)C$
(d) 1

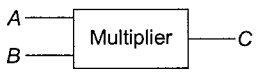
Q.15 Consider the logical functions given below.

$f_1(A, B, C) = \Sigma(2, 3, 4)$
$f_2(A, B, C) = \pi(0, 1, 3, 6, 7)$

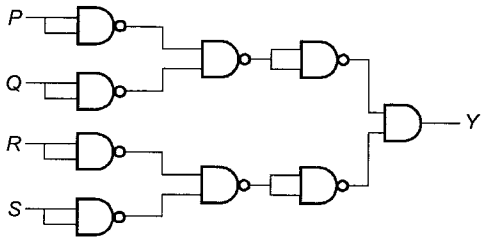


If f is logic zero, then maximum number of possible minterms in function f_3 are _____.

Q.16 Consider a 3-bit number A and 2 bit number B are given to a multiplier. The output of multiplier is realized using AND gate and one bit full adders. If minimum number of AND gates required are X and one bit full adders required are Y, then $X + Y =$ _____.



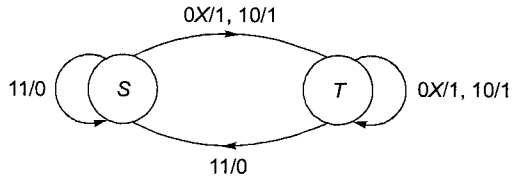
Q.17 For the circuit shown in figure the Boolean expression for the output Y in terms of inputs P, Q, R and S is



(a) $\overline{P}+\overline{Q}+\overline{R}+\overline{S}$ (b) $\overline{P}\,\overline{Q}\,\overline{R}\,\overline{S}$

(c) $(\overline{P}+\overline{Q})+(\overline{R}+\overline{S})$ (d) $(P+Q)(R+S)$

Q.18 A state diagram of a logic which exhibits a delay in the output is shown in the figure, where X is the do not care condition.

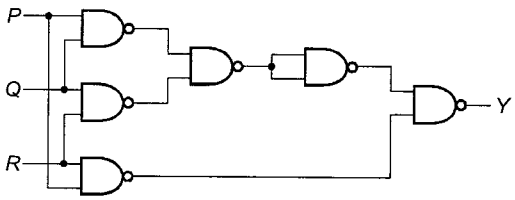


The logic gate represented by the state diagram is

(a) XOR (b) OR

(c) AND (d) NAND

Q.19 The output Y in the circuit below is always "1" when



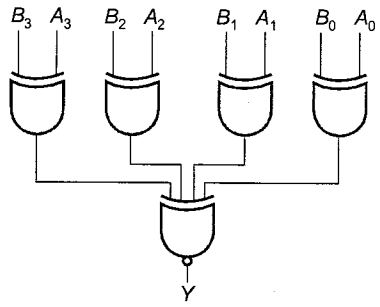
(a) two or more of the inputs, P, Q, R are "0"

(b) two or more of the inputs P, Q, R are "1"

(c) any odd number of the inputs P, Q, R is "0"

(d) any odd number of the inputs P, Q, R is "1"

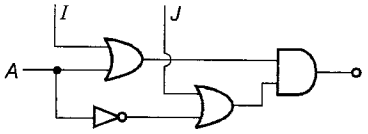
Q.20 A digital circuit which compares two numbers $A_3\,A_2\,A_1\,A_0$, $B_3\,B_2\,B_1\,B_0$ is shown in figure. To get output $Y=0$, choose one pair of correct input numbers.



(a) 1010, 1010 (b) 0101, 0101

(c) 0010, 0010 (d) 1010, 1011

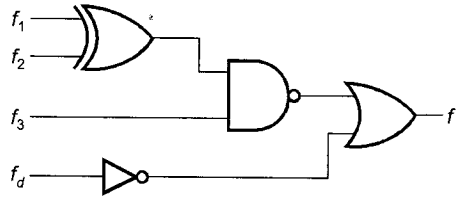
Q.21 The circuit given in figure is to be used to implement the function $Z=f(A,B)=\overline{A}+B$. What are the values that should be selected for I and J?



(a) $I=0, J=B$ (b) $I=1, J=B$

(c) $I=B, J=1$ (d) $I=\overline{B}, J=0$

Q.22 Consider the circuit diagram given below



Given $f_1=\Sigma m(1,2,4,6,7)$

$f_2=\Sigma m(2,3,4,5)$

$f_3=\Sigma m(0,1,2,3)$

$f_4=\Sigma m(0,2,4,6)$

If the boolean function f_d is dual of f_4, then the boolean function 'f' is _____.

(a) $\Sigma m(0,1,2,3,4,5,6,7)$

(b) $\Sigma m(0,1,2,3,6,7)$

(c) $\Sigma m(0,1,2,3,7)$

(d) None of these

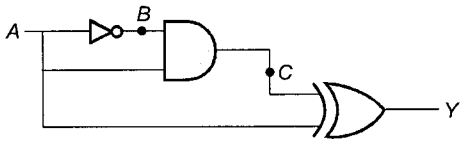
■■■■

Answers Logic Gates and Switching Circuits

1.	(b)	2.	(b)	3.	(d)	4.	(a)	5.	(c)	6.	(c)	7.	(8)	8.	(a)	10.	(d)		
11.	(d)	12.	(b)	13.	(b)	14.	(d)	17.	(b)	18.	(d)	19.	(b)	20.	(d)	21.	(b)		
22.	(a)																		

Explanations Logic Gates and Switching Circuits

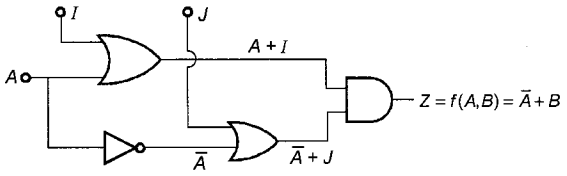
1. (b)



	A	B	C	Y
$t < 10$ ns	1	1	0	0
10 ns $< t <$ 20 ns	1	0	0	1
20 ns $< t <$ 30 ns	1	0	1	1
30 ns $< t <$ 40 ns	1	0	0	0
40 ns $< t$	1	0	0	1

$\Rightarrow$ Option (b) is correct.

2. (b)



$Z = (A + I)(\bar{A} + J)$

Put, $I = 1; J = B$

$Z = (A + 1)(\bar{A} + B)$

$Z = (\bar{A} + B)$

3. (d)

$Y = f(A, B) = \Pi M(0, 1, 2, 3)$

K-map for Y:

$Y = 1$ which represents a situation where output is independent of input.

B \ A	0	1
0	0	0
1	0	0

4. (a)

$ABCDE + ABCD + ABC + AC + C$

$= ABCD(1 + E) + AC(B + 1) + C$

$= ABCD + AC + C$

$= ABCD + (A + 1)C$

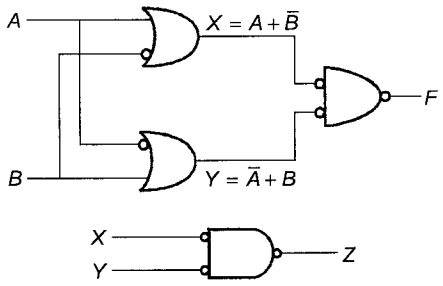
$= ABCD + C$

$= C(1 + ABD)$

$= C(1 + A)(1 + B)(1 + D)$

$= C$

5. (c)

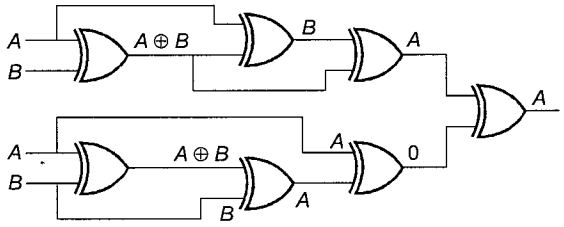


$Z = \overline{\bar{X} \cdot \bar{Y}} = X + Y$

$\Rightarrow \quad F = A + \bar{B} + \bar{A} + B = 1$

So F is a tautology.

6. (c)



7. (8)

$f = \bar{w}\bar{x}(y + z) + \bar{w}x\bar{y} + w\bar{x}\bar{z} + wxyz$

$= \bar{w}\bar{x}y(z + \bar{z}) + \bar{w}\bar{x}\bar{z}(y + \bar{y})$
$+\bar{w}x\bar{y}(z + \bar{z}) + w\bar{x}\bar{z}(y + \bar{y}) + wxyz$

$= \bar{w}\bar{x}yz + \bar{w}\bar{x}y\bar{z} + \bar{w}\bar{x}yz$
$+\bar{w}\bar{x}z\bar{y} + \bar{w}x\bar{y}z + \bar{w}x\bar{y}\bar{z}$
$+w\bar{x}\bar{z}y + w\bar{x}\bar{z}\bar{y} + wxyz$

$= \Sigma m(1, 2, 3, 4, 5, 8, 10, 15)$

$\therefore$ Number of minterms = 8

8. (a)

EXNOR gate with even number of inputs acts as even function.

EXNOR gate with odd number of inputs acts as odd function.

Here the EXNOR gate has seven inputs

$\therefore$ EXNOR gate acts as odd function.

9. (3)

$$f = \overline{\bar{A} + \overline{\left[B + \bar{C}(\overline{AB + A\bar{C}})\right]}}$$

$$= A \cdot \left[B + \bar{C}(\overline{AB + A\bar{C}})\right]$$

[Demorgan's Law]

$$= A \cdot \left[B + \bar{C}(\overline{AB} \cdot \overline{A\bar{C}})\right]$$

[Demorgan's Law]

$$= A \cdot \left[B + \bar{C}(\bar{A} + \bar{B})(\bar{A} + C)\right]$$

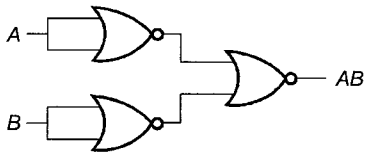
[Demorgan's Law]

$$= A\left[B + \bar{C}(\bar{A} + \bar{B}C)\right]$$

[Distributive property]

$$= A\left[B + \bar{A}\bar{C}\right] = AB + A\bar{A}\bar{C}$$

$= AB$ (AND gate to be implemented)



$\Rightarrow$ Minimum number of NOR gate required = 3

10. (d)

Let $x = 0$

then 0 NOR 1 = $0 \neq \bar{x}$

Let $x = 1$

then 1 NOR 1 = $0 \neq \bar{x}$

Hence, (d) is the required option.

11. (d)

The negative level logic circuit is a dual circuit of positive level logic circuit.

Using dual logic gates, it can be shown that the circuits in option (a), (b) and (c) are all same in operation.

12. (b)

$y = A \oplus (\bar{A} \oplus \bar{A}) \oplus (A \oplus A) \oplus (\bar{A} \oplus \bar{A}) \oplus (A \oplus A)$

Note: $A \oplus A = 0$

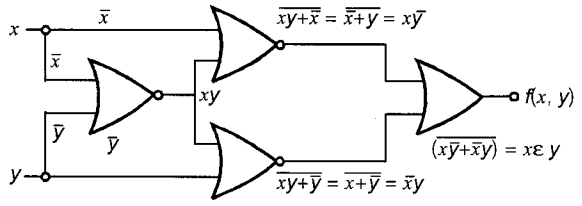
$A \oplus \bar{A} = 1$

$\therefore \quad Y = A \oplus 0 \oplus 0 \oplus 0 \oplus 0 = A \oplus 0$

Hence $Y = A$ EXOR 0

Hence (b) is correct option.

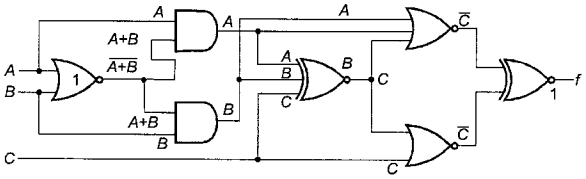
13. (b)



Therefore the above circuit performed exclusive NOR gate.

14. (d)

From the given diagram we can see that



Property : $CC \overset{*}{=} C \odot C = 1$.

15. (6)

$f_1(A, B, C) = \Sigma(2, 3, 4)$

$f_2(A, B, C) = \pi(0, 1, 3, 6, 7) = \Sigma(2, 4, 5)$

For function f to be zero:

$$f_3(A, B, C) = \overline{[f_1(A, B, C) \cap f_2(A, B, C)]}$$

$$= \Sigma(0, 1, 3, 5, 6, 7)$$

Maximum minterms possible are 6.

16. (9)

$$\begin{array}{lcccc} A = & & a_2 & a_1 & a_0 \\ B = & & & b_1 & b_0 \\ \hline A \times B = & & a_2b_0 & a_1b_0 & a_0b_0 \\ & b_1a_2 & b_1a_1 & b_1a_0 & \downarrow \\ \hline & b_1a_2 & (a_2b_0 + a_1b_1) & (a_1b_0 + b_1a_0) & a_0b_0 \\ & C_3 & C_2 & C_1 & C_0 \end{array}$$

Number of AND gates required (X) = 6
Number of one bit full adders required (Y) = 3

$$X + Y = 6 + 3 = 9$$

17. (b)

$$Y = \overline{\overline{(\bar{P}\cdot\bar{Q})}\cdot\overline{(\bar{R}\cdot\bar{S})}} = \bar{P}\bar{Q}\bar{R}\bar{S}$$

[by demorgan's law]

18. (d)

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

If any one of the input is zero, output is logic '1'. Otherwise output is logic '0', which represents the NAND gate.

19. (b)

Take two or three input '1' then we always get '1'

or

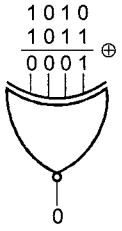
Take two or three input zero then we always get '0' hence option '*b*' is true and output

$$Y = PQ + PR + RQ$$

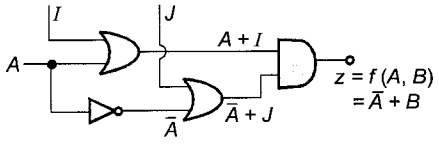
20. (d)

In EX-NOR gate, if odd number of inputs are 1

then output is zero.



21. (b)



As we can see clearly output must be $\bar{A}+B$ which can be obtained only by making $J = B$ and $I = 1$

So, that $J + \bar{A} = 1$ and $f = (\bar{A} + B)\,1 = \bar{A} + B$.
Hence (b) is correct option.

22. (a)

$$f = (\bar{f}_d) + \overline{(f_3)\cdot(f_1 \oplus f_2)}$$

$$= \bar{f}_d + \bar{f}_3 + (f_1 \odot f_2)$$

$$f = \bar{f}_d + \bar{f}_3 + f_1 f_2 + \bar{f}_1 \bar{f}_2$$

$$f_d = f_4 d$$

$$f_d = \Sigma m\,(0, 2, 4, 6)$$

$$\bar{f}_d = \Sigma m\,(1, 3, 5, 7)$$

$$f = \Sigma m\,(1, 3, 5, 7) + \Sigma m\,(4, 5, 6, 7) + \Sigma m\,(0, 2, 4)$$

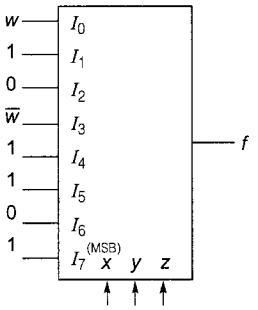
$$f = \Sigma m\,(0,1, 2, 3, 4, 5, 6, 7) = 1$$

■■■■

4 CHAPTER

Combinational Logic Circuits

Q.1 Find the simplified boolean expression $f(x,y,z,w)$ for the below 8 : 1 MUX



(a) $\overline{x}y + xz + \overline{z}w + \overline{y}w$

(b) $x\overline{y} + \overline{y}w + \overline{x}z + xz$

(c) $\overline{x}y + xz + z\overline{w} + \overline{y}w$

(d) $x\overline{y} + xz + z\overline{w} + \overline{y}w$

Q.2 If x number of 4 × 1 multiplexers, y number of 2 × 1 multiplexers and z number of 16 × 1 multiplexers are needed to impliment a 128 × 1 multiplexer, then which of the following can be value of $(x + y + z)$?

[**Hint:** Use exactly two16 × 1 multiplexers i.e., $z = 2$]

(a) 35 (b) 10

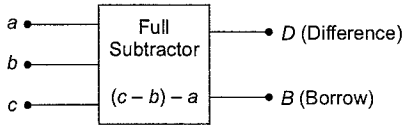
(c) 80 (d) All of these

Q.3 For a n-bit carry look ahead adder the gate count is

(a) $\frac{(n^2 + 8n)}{2}$ (b) $\frac{(n^2 + 9n)}{2}$

(c) $\frac{n^2 + 5n}{2}$ (d) $\frac{(n^2 + 6n)}{2}$

Q.4 Find the boolean expression B in the digital circuit given below



(a) $\overline{a}b + bc + \overline{a}c$ (b) $a\overline{b} + \overline{b}c + ca$

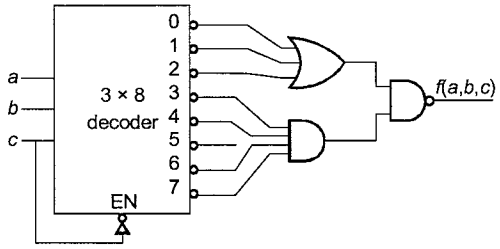
(c) $ab + b\overline{c} + \overline{c}a$ (d) $ab + bc + ca$

Q.5 A 1-bit full adder takes 20 ns to generate carryout bit and 40 ns for the sum bit. What is the maximum rate of addition per second when four 1-bit full adders are cascaded?

(a) 10^7 (b) 1.25×10^7

(c) 6.25×10^6 (d) 10^5

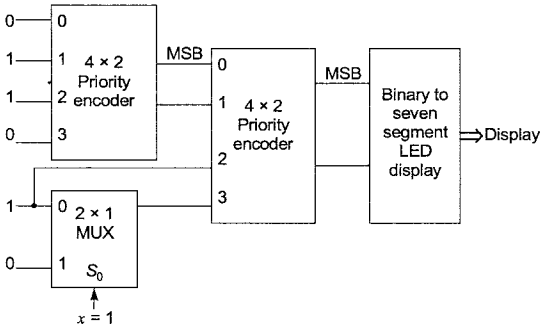
Q.6 The Boolean expression $f(a, b, c)$ in its canonical form for the decoder circuit shown below is



(a) $\Pi M(4, 6)$ (b) $\Sigma m(0, 1, 2, 3, 5, 7)$

(c) $\Sigma m(4, 6)$ (d) $\Pi M(0, 1, 2, 3, 5)$

Q.7 Consider the combinational circuit below



The output of the combinational circuit is_____.

Q.8 How many half adders are required to realize the following 4 functions?

$f_1 = A \oplus B \oplus C$

$f_2 = \overline{A}BC + A\overline{B}C$

$f_3 = AB\bar{C} + (\bar{A} + \bar{B})C$

$f_4 = ABC$

(a) 2 (b) 4
(c) 3 (d) 5

Q.9 Let x_s, y_s and z_s are the sign bits of a number x, y and result z. The overflow condition if C_{n-2} be the carry into sign bit

(a) $\bar{x}_s\bar{y}_s c_{n-2} + x_s\bar{y}_s\bar{c}_{n-2}$

(b) $\bar{x}_s y_s c_{n-2} + x_s\bar{y}_s c_{n-2}$

(c) $\bar{x}_s\bar{y}_s c_{n-2} + x_s y_s\bar{c}_{n-2}$

(d) none of these

Q.10 A combinational circuit outputs a digit in the form of 4 bits. 0 is represented as 0000, 1 by 0001... 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and output 1 if the digit ≥ 5 and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

(a) 2 (b) 3
(c) 4 (d) 5

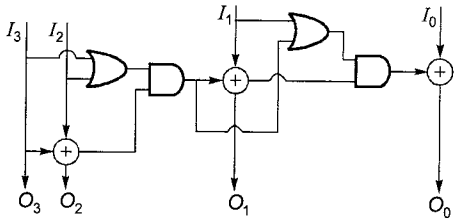
Q.11 Minimum number of 2 × 1 multiplexers required to realize the following function

$$f = \bar{A}\bar{B}C + \bar{A}B\bar{C}$$

Assume that inputs are available only in true and boolean constants 1 and 0 are available.

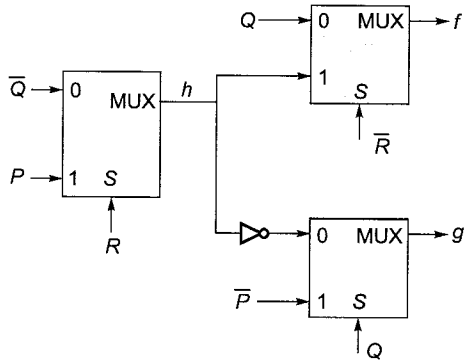
(a) 1 (b) 2
(c) 3 (d) 7

Q.12 The circuit shown below converts (Here ⊕ is XOR)



(a) Binary to gray
(b) Binary to excess 3
(c) Excess 3 to gray
(d) Gray to binary

Q.13 Consider the following multiplexer:



The value of output function 'g' is

(a) $P'Q + P'R$
(b) $PQ + PR$
(c) $PR + P'Q'$
(d) None of these

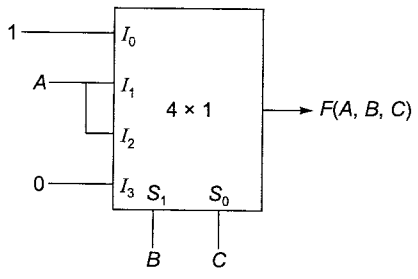
Q.14 Minimum number of NAND gates required to implement Sum in half-adder circuit is:

(a) 2 (b) 3
(c) 4 (d) 5

Q.15 The number of full and half-adder required to add 16 - bit numbers is

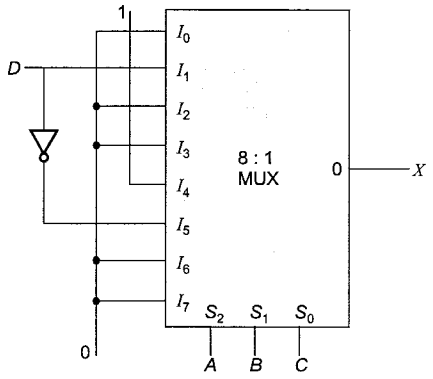
(a) 8 half-adders, 8 full-adders
(b) 1 half-adder, 15 full-adders
(c) 16 half-adders, 0 full-adders
(d) 4 half-adders, 12 full-adders

Q.16 A 4 × 1 multiplexer is used to implement 3 input boolean function as shown in the below figure. The $F(A, B, C)$ is_____



(a) $\Sigma(0, 4, 5, 6)$ (b) $\Sigma(3, 4, 5, 6)$
(c) $\pi(0, 4, 5, 6)$ (d) $\pi(3, 4, 5, 6)$

Q.17 The circuit below represents function $X(A, B, C, D)$ as:

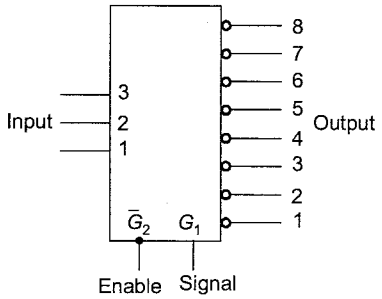


(a) $\Sigma(3, 8, 9, 10)$
(b) $\Sigma(3, 8, 10, 14)$
(c) $\Pi(0, 1, 2, 4, 5, 6, 7, 11, 12, 13, 15)$
(d) $\Pi(0, 1, 2, 4, 5, 6, 7, 10, 12, 13, 15)$

Q.18 Consider the following statements:
A 4 : 16 decoder can be constructed (with enable input) by:
1. using four 2 : 4 decoders (each with an enable input) only.
2. using five 2 : 4 decoders (each with an enable input) only.
3. using two 3 : 8 decoders (each with an enable input) only.
4. using two 3 : 8 decoders (each with an enable input) and an inverter.

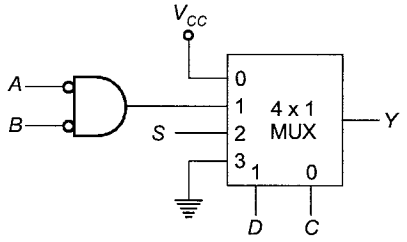
Which of the statements given above is/are correct
(a) 2 and 3 (b) 1 only
(c) 2 and 4 (d) None of these

Q.19 A 3-to-8 decorder is shown below:



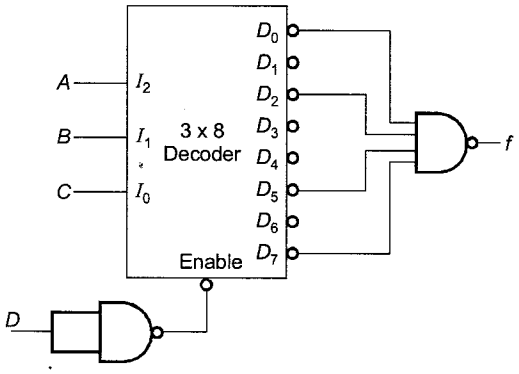
All the output lines of the chip will be high, when all the inputs 1, 2 and 3
(a) are high; and G_1, G_2 are low
(b) are high; and G_1 is low, G_2 is high
(c) are high; and G_1, G_2 are high
(d) are high; and G_1 is high, G_2 is low

Q.20 Consider the circuit given below



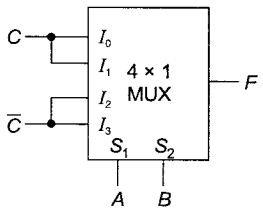
Which of the following statements is true for Y.
(a) $Y = \bar{C}\bar{D} + \bar{D}C(\bar{A} + \bar{B}) + \bar{C}DS$
(b) $Y = CD + D\bar{C}(\overline{A + B}) + CDS$
(c) $Y = \bar{C}\bar{D} + (\overline{\bar{D} + C})(\overline{A + B}) + \overline{C + \bar{D} + \bar{S}}$
(d) $Y = \bar{C}\bar{D} + (\overline{D + \bar{C}})(\overline{A + B}) + \overline{C + \bar{D} + \bar{S}}$

Q.21 The logic function $f(A, B, C, D)$ implemented by the circuit shown below is



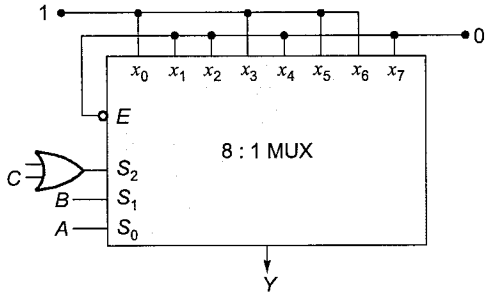
(a) $\bar{D}(A \oplus C)$ (b) $D(A \odot C)$
(c) $\bar{D}(A \oplus B)$ (d) $D(A \odot B)$

Q.22 The function realized by the circuit shown in figure is



(a) $F = A \odot C$ (b) $F = A \oplus C$
(c) $F = B \odot C$ (d) $F = B \oplus C$

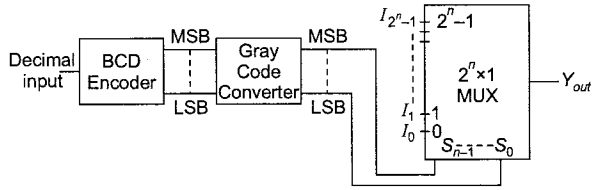
Q.23 In the following circuit, S_2, S_1 and S_0 are select lines and X_7 to X_0 are input lines. S_0 and X_0 are LSBs. The output Y is _____.



(a) indeterminate (b) $A \oplus B$

(c) $\overline{A \oplus B}$ (d) $\overline{C}(\overline{A \oplus B}) + C(A \oplus B)$

Q.24 Consider the circuit given below.



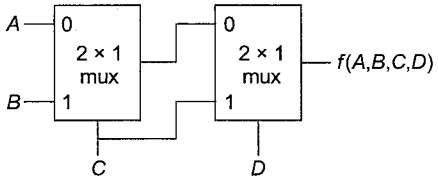
If the decimal input is 92 then Y_{out} corresponds to I_m, then value of m is _____.

Q.25 Minimum 4 line to 16 line decoders required to realize 8 line to 256 line decoder are

(a) 8 (b) 9

(c) 17 (d) 16

Q.26 Consider the logic circuit given below. The minterms in $f(A,B,C,D)$ are _____.



(a) $\Sigma m\,(1, 3, 5, 6, 7, 11, 14)$

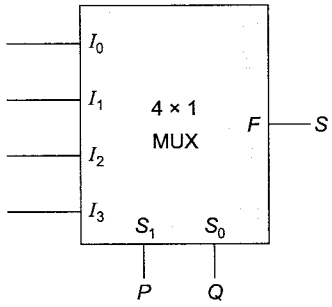
(b) $\Sigma m\,(6, 7, 8, 12, 14, 15)$

(c) $\Sigma m\,(3, 6, 7, 8, 11, 12, 14, 15)$

(d) $\Sigma m\,(3, 6, 7, 9, 11, 12, 14, 15)$

Q.27 Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in}.

Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S?



(a) $I_0 = I_1 = C_{in}$; $I_2 = I_3 = \overline{C}_{in}$

(b) $I_0 = I_1 = \overline{C}_{in}$; $I_2 = I_3 = C_{in}$

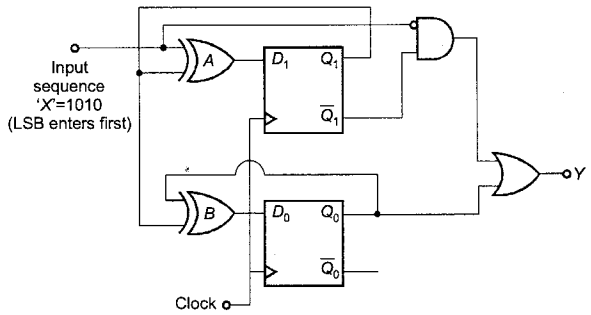
(c) $I_0 = I_3 = C_{in}$; $I_1 = I_2 = \overline{C}_{in}$

(d) $I_0 = I_3 = \overline{C}_{in}$; $I_1 = I_2 = C_{in}$

Q.28 Consider a clocked sequential circuit as shown in the figure below. Assuming initial state to be

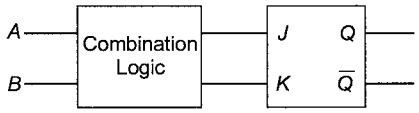
$Q_1\ Q_0 = 00$

For an input sequence $X = 1010$, the respective output sequence will be _____.

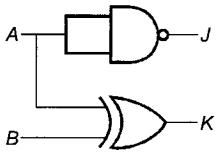


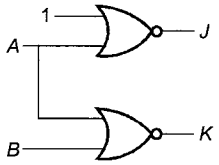
Q.29 A new two input flip flop is designed as shown in figure. The table shows the characteristic table of the A-B flip-flop.

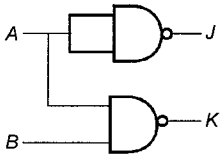
A	B	Q_{n+1}
0	0	$\overline{Q}_n$
0	1	1
1	0	Q_n
1	1	0

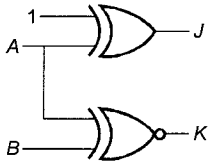


The combination logic is

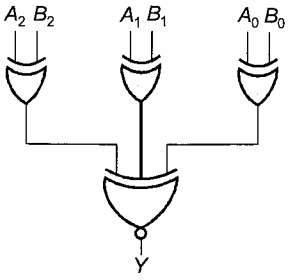
(a)


(b)


(c)


(d)


Q.30 A digital circuit which compares two numbers $A_2\ A_1\ A_0$ and $B_2\ B_1\ B_0$ is shown in figure

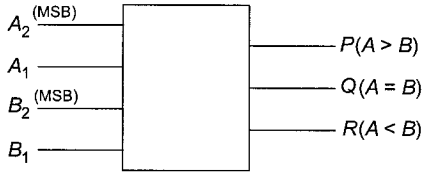


To obtain output $Y = 1$, the valid combination is_____.

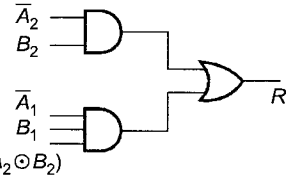
(a) 010, 111 (b) 010, 101

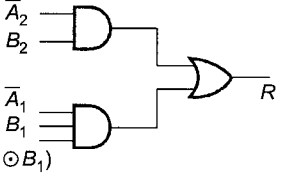
(c) 101, 110 (d) 101, 011

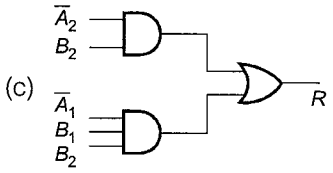
Q.31 A two bit magnitude comparator circuit is shown below.

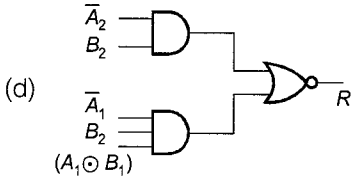


The logic circuit for r is

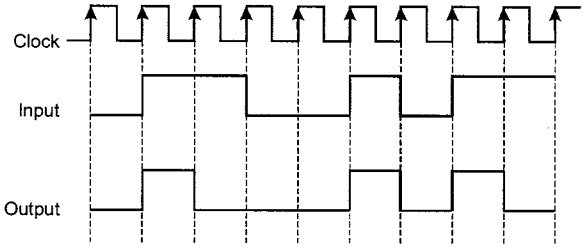
(a)


(b)


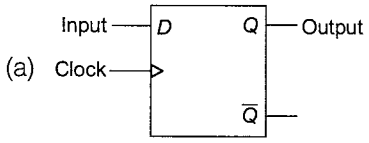
(c)


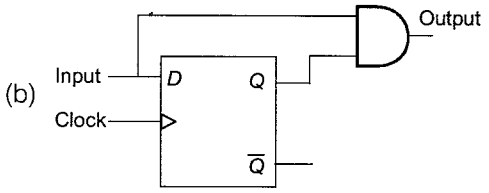
(d)


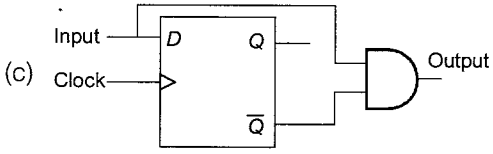
Q.32 Consider the waveforms given below:

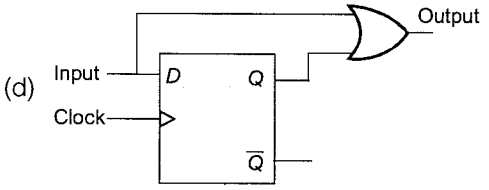


The output can be obtained from the circuit

(a)


(b)


(c)


(d)


■■■

Answers Combinational Logic Circuits

1.	(d)	2.	(a)	3.	(b)	4.	(c)	5.	(a)	6.	(c)	8.	(c)	9.	(c)	10.	(b)
11.	(b)	12.	(d)	13.	(a)	14.	(c)	15.	(b)	16.	(a)	17.	(a)	18.	(c)	19.	(b)
20.	(d)	21.	(b)	22.	(b)	23.	(b)	25.	(c)	26.	(c)	27.	(c)	29.	(d)	30.	(b)
31.	(a)	32.	(c)																

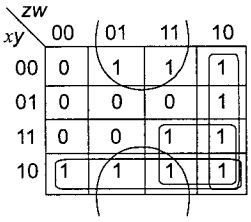
Explanations Combinational Logic Circuits

1. (d)

Function table for multiplexer is

x	y	z	f
0	0	0	w
0	0	1	1
0	1	0	0
0	1	1	$\bar{w}$
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Forming four-variable K-map



Total Four Quads

$f(x, y, z, w) = x\bar{y} + xz + z\bar{w} + \bar{y}w$

2. (a)

$x = \frac{128}{4} = 32 \rightarrow 4 \times 1$ Multiplexers

$z = \frac{32}{16} = 2 \rightarrow 16 \times 1$ Multiplexers

$y = \frac{2}{2} = 1 \rightarrow 2 \times 1$ Multiplexers

$\therefore \quad x + y + z = 32 + 1 + 2 = 35$

Option (b) and (c) not possible.

[**Note:** Many values can exist for $x + y + z$]

3. (b)

For n-bit carry look ahead adder

Total #AND gates = $\frac{n(n+1)}{2} + n$

Total #OR gates = n

Total #XOR gates = $n + n$

$\therefore$ Total gate count = $\frac{n(n+1)}{2} + n + n + n + n$

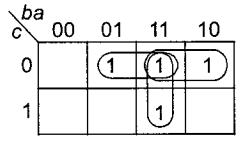
$= \frac{(n^2 + 9n)}{2}$

4. (c)

Order of subtraction is $(c - b) - a$

c	b	a	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Borrow $(B) = \bar{c}\bar{b}a + \bar{c}ba + \bar{c}ba + cba$



$B = \bar{c}a + \bar{c}b + ba$

5. (a)

Given, $T_{ci} = 20$ ns

$T_{si} = 40$ ns

$T_{S_0} = 40\ ns$
$T_{S_1} = (40+20)\ ns = 60\ ns$
$T_{S_2} = (60+20)\ ns = 80\ ns$
$T_{S_3} = (80+20)\ ns = 100\ ns$
} 4 full adders are cascaded

$\because$ Final sum result will take 100 ns

$\therefore$ Rate of addition $= \dfrac{1}{100\ ns} = 10^7$

6. (c)

The given 3 × 8 decoder is a active low output. Each output represents a maximum term when activated with enable.

If $c = 0$, then $EN = 1$

The outputs D_0, D_2, D_4 and D_6 are active and outputs D_1, D_3, D_5 and D_7 are inactive.

$\therefore$ Output of OR gate is $(M_0 + 1 + M_2) = 1$

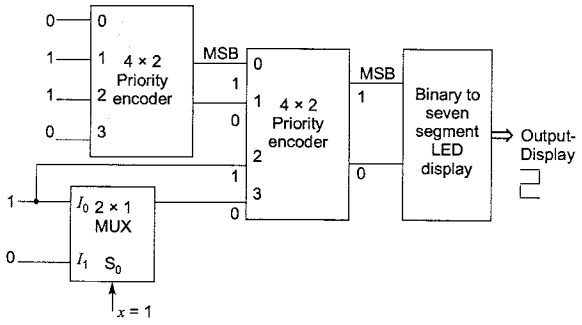
Output of AND gate is $(M_4\ M_6) = \Pi M(4, 6)$

$f(a, b, c) = \Pi M(4, 6)$

$f(a, b, c) = \Pi M(0, 1, 2, 3, 5, 7)$

$f(a, b, c) = \Sigma m(4, 6)$

7. (2)



8. (c)

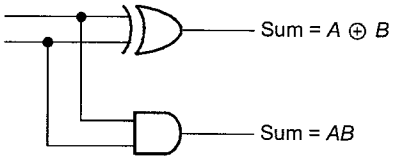
$f_2 = \bar{A}BC + A\bar{B}C = (\bar{A}B + A\bar{B})C$

$= (A \oplus B)C$

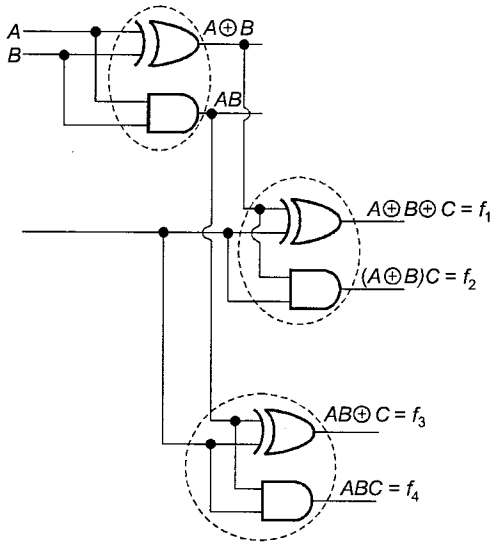
$f_3 = AB\bar{C} + (\bar{A} + \bar{B})C = AB\bar{C} + \overline{AB}C$

$= AB \oplus C$

Single Half Adder →



To realize the four given equations :



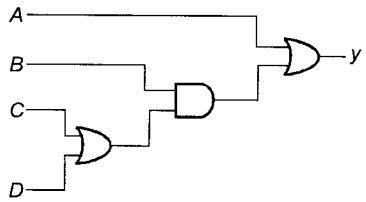
10. (b)

We need output 1 when input ≥ 5, the required boolean expression can be obtained using K-map

AB \ CD	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	1	1	1	1
10	1	1	1	1

$\Rightarrow \quad y = A + BD + BC$

$= A + B(C + D)$

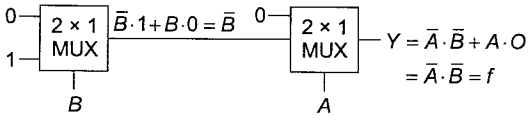


$\Rightarrow$ 3 gates are required.

11. (b)

$f = \bar{A}\bar{B}C + \bar{A}B\bar{C} = \bar{A}\bar{B}(C + \bar{C}) = \bar{A}\bar{B}$

with 2 × 1 multiplexer



13. (a)

$$g = \bar{Q}\bar{h} + Q\bar{P}$$
$$= \bar{Q}(\overline{\bar{R}\bar{Q} + RP}) + Q\bar{P}$$
$$= \bar{Q}((R+Q)(\bar{R}+\bar{P})) + Q\bar{P}$$
$$= \bar{Q}(R\bar{R} + Q\bar{R} + R\bar{P} + Q\bar{P}) + Q\bar{P}$$
$$= \bar{Q}R\bar{P} + Q\bar{P}$$
$$= (\bar{Q}R + Q)\bar{P} \quad (\because Q + \bar{Q}R)$$
$$= (Q+\bar{Q})(Q+R) = Q + R)$$
$$= (Q+R)\bar{P} = \bar{P}Q + \bar{P}R$$

14. (c)

Expression for sum in half adder is $\bar{A}B + A\bar{B} = A \oplus B$ and minimum number of NAND gates required for EX-OR Gate are '4'. Hence correct option is (c).

16. (a)

$$Y = \bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$
$$= A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$$
$$= 000, 100, 101, 110$$
$$= 0, 4, 5, 6$$

17. (a)

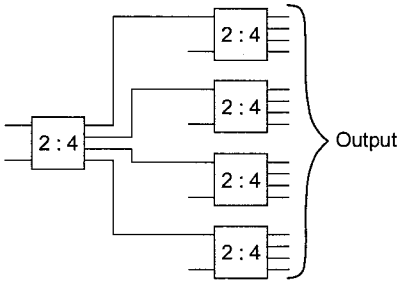
The given circuit represents the implementation of four variable function using 8 : 1 MUX here. D as taken as the fourth i/p and A, B, C act as select lines.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{D}$	0	2	4	6	⑧	⑩	12	14
D	1	③	5	7	⑨	11	13	15
Given →	0	D	0	0	1	$\bar{D}$	0	0

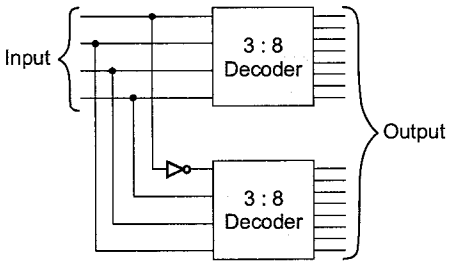
Σm (3, 8, 9, 10).

18. (c)

4 : 16 decoder using only 2 : 4 decoders:



4:16 decoder using two 3:8 decoders and an inverter:



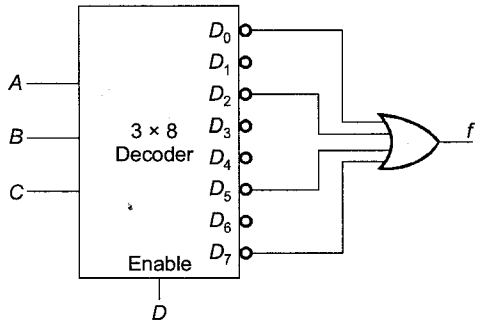
19. (b)

Outputs are active low, so all the output lines of the chip will be high, when chip will be disabled i.e., $G_1 = 0$ and $\bar{G}_2 = 1$.

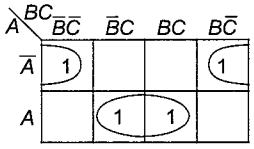
20. (d)

$$Y = \bar{C}\bar{D} + (\bar{A}\cdot\bar{B})(\bar{D}C) + \bar{C}DS$$
$$= Y = \bar{C}\bar{D} + \overline{(\overline{D+\bar{C}})(\overline{A+B})} + \overline{C+\bar{D}+\bar{S}}$$

21. (b)



A	B	C	D	f
X	X	X	0	0
0	0	0	1	1
0	0	1	1	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1



$$f = D(\bar{A}\bar{C} + AC)$$

22. (b)

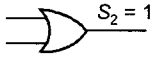
$$F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$$
$$F = \bar{A}C(\bar{B}+B) + A\bar{C}(\bar{B}+B)$$
$$F = \bar{A}C + A\bar{C}$$
$$F = A \oplus C$$

23. (b)

Floating input is accepted by GATE logic gate as logic 1.

Hence $S_2 = 1$

S_2 1	S_1 B	S_0 A	Y
1	0	1	1
1	0	1	1
1	1	0	1
1	1	1	0



$$Y = A \oplus B$$

24. (219)

Decimal input = 92

BCD = 10010010

Output of Gray code converter

= 11011011

Y_0 corresponds to I_m with $(S_n....S_0)$ is

$= (11011011)_2$

$m = 219$

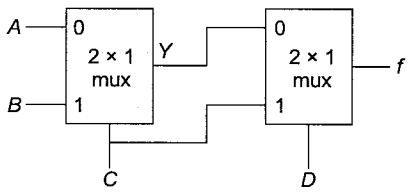
25. (c)

Numbers of 4 × 16 decoders required

$$\frac{256}{16} = 16$$

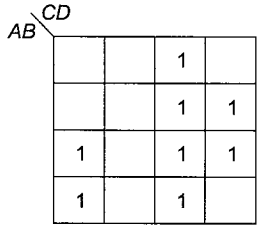
$$\frac{16}{16} = 1 \Rightarrow 16 + 1 = 17$$

26. (c)



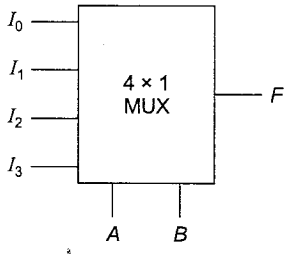
$$Y = A\bar{C} + BC$$
$$f = Y\bar{D} + CD$$
$$f = (A\bar{C} + BC)\bar{D} + CD$$
$$= A\bar{C}\bar{D} + BC\bar{D} + CD$$
$$= A(B+\bar{B})\bar{C}\bar{D} + (A+\bar{A})CB\bar{C}\bar{D} + CD(A+\bar{A})(B+\bar{B})$$
$$= AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + ABC\bar{D} + \bar{A}BC\bar{D} + ABCD + A\bar{B}CD + \bar{A}BCD + \bar{A}\bar{B}CD$$

$f(A,B,C,D) = \Sigma m(3, 6, 7, 8, 11, 12, 14, 15)$

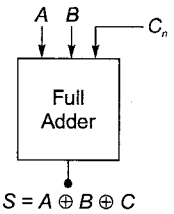


27. (c)

For a 4 : 1 mux



$$F = I_0\bar{A}\bar{B} + I_1\bar{A}B + I_2A\bar{B} + I_3AB$$



where sum of full adder is = $A \oplus B \oplus C$

Truth table of Full adder

	$S_1(A)$	$S_0(B)$	Carry(C_{in})	Sum	
I_0	0	0	0	0	$I_0 = C_{in}$
	0	0	1	1	
I_1	0	1	0	1	$I_1 = \overline{C_{in}}$
	0	1	1	0	
I_2	1	0	0	1	$I_2 = \overline{C_{in}}$
	1	0	1	0	
I_3	1	1	0	0	$I_3 = C_{in}$
	1	1	1	1	

28. (0011)

$Q_1(t+1) = D_1$

$Q_1(t+1) = Q_1(t) \oplus X$ ...(1)

$Q_0(t+1) = D_0$

$Q_0(t+1) = Q1(t) \oplus Q_0(t)$ ...(2)

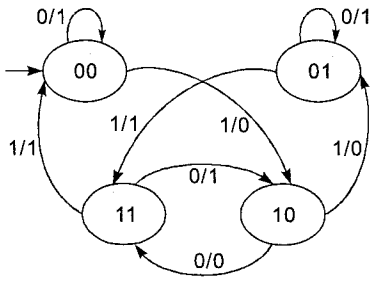
$$Y(t) = Q_0(t) + \left(\overline{Q}_1(t) \cdot \overline{X}\right)$$

$$Y(t) = Q_0(t) + \overline{(Q_1(t) + X)} \quad \ldots(3)$$

State table:

X	Present State		Next State		Y
	Q_1	Q_0	Q_1	Q_0	
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	1	0	0	1

State diagram:

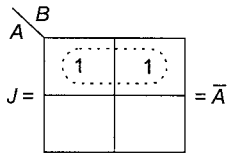


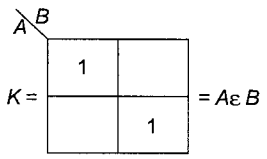
From state diagram output sequence is 0011 for input sequence 1010.

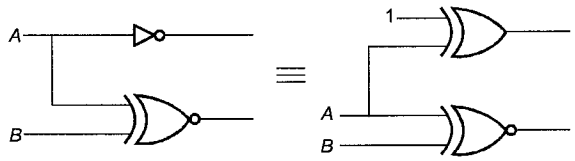
29. (d)

A	B	Q_{n+1}	J	K
0	0	$\overline{Q}_n$	1	1
0	1	1	1	0
1	0	Q_n	0	0
1	1	0	0	1

State Table

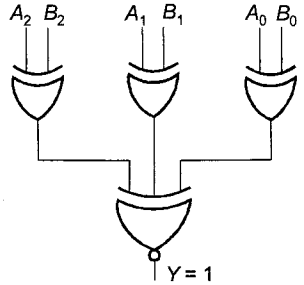






30. (b)

Redrawing the circuit



A 3-input XNOR gate acts as an odd function

$Y = A_0 \oplus B_0 \oplus A_1 \oplus B_1 \oplus A_2 \oplus B_2 = 1$

using definition of XOR the valid combination is

$A_2 A_1 A_0 = 010$ and $B_2 B_1 B_0 = 101$

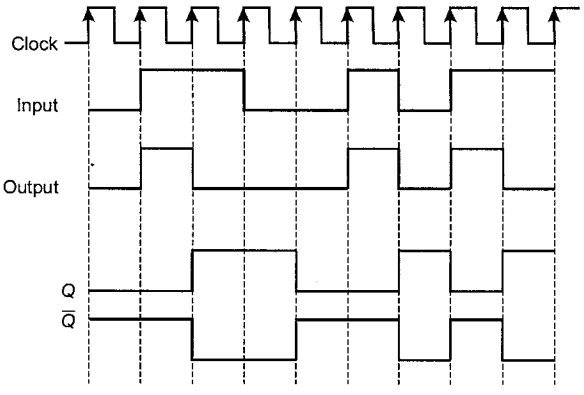
31. (a)

Expression of 'R' from logical deduction is

$$R = \overline{A}_2 B_2 + (A_2 \odot B_2)\overline{A}_1 B_1$$

R can be implemented by AND-OR logic.

32. (c)



By checking all the options.

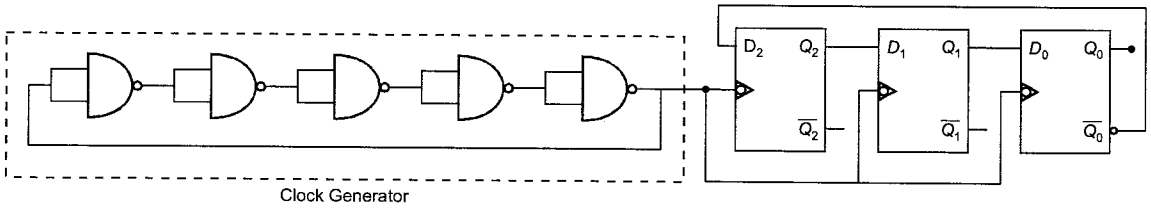
Option (c) correctly matches.

■■■

5 CHAPTER

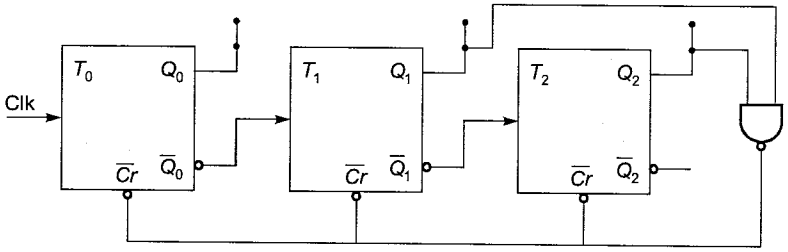
Sequential Logic Circuits

Q.1 Consider the digital circuit shown in below figure.



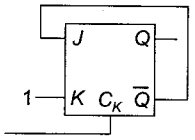
The average propagation delay of each NAND gate in the clock generator circuit is 10 ns. The frequency of the clock signal is _____ MHz.

Q.2 Consider the counter shown below



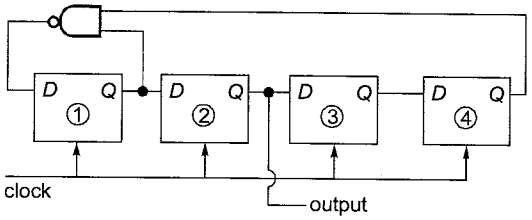
If the initial state of the counter is 001, then after how many minimum number of clock pulses the initial state is reached?

Q.3 In the following figure consisting of *J-K* flip flop assume the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be



(a) 010000
(b) 011001
(c) 010010
(d) 010101

Q.4 Consider the following circuit consisting of *D* flip flops.

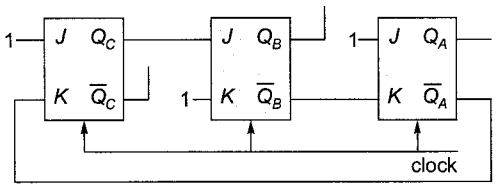


The circuit generates a sequence. Initially all flip flops are cleared. The generated sequence after all the flip flops have been changed from their initial value is

(a) 0011110 (b) 111010

(c) 001111 (d) 11010

Q.5



If the initial state $Q_A Q_B Q_C$ = 110, after how many clocks it get back same value?

(a) 5 (b) 6

(c) 7 (d) 3

Q.6 An *X*-*Y* flip-flop, whose characteristic table is given below, is to be implemented using a JK flip-flop. This can be done by making

X	Y	Q_{n+1}
0	0	1
0	1	Q_1
1	0	$\overline{Q}_n$
1	1	0

(a) $J = X, K = \overline{Y}$ (b) $J = \overline{X}, K = Y$

(c) $J = Y, K = \overline{X}$ (d) $J = \overline{Y}, K = X$

Q.7 **Assertion (A):** D-Flip-Flops are used as buffer register.

Reason (R): D-Flip-Flops are free from "race-around" condition.

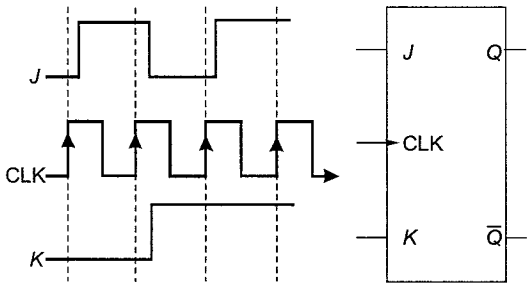
(a) Both A and R are individually true and R is the correct explanation of A

(b) Both A and R are individually true but R is not the correct explanation of A

(c) A is true but R is false

(d) A is false but R is true

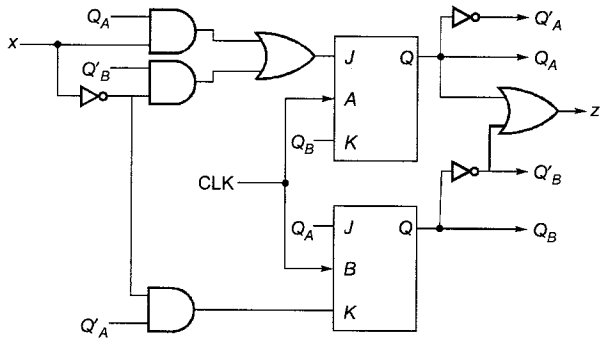
Q.8 The J-K flip-flop shown below is initially reset, so that $Q = 0$. If a sequence of four clock pulses is then applied, with the *J* and *K* inputs as given in the figure, the resulting sequence of values that appear at the output *Q* starting with its initial state, is given by



(a) 01011 (b) 01010

(c) 00110 (d) 00101

Q.9 Analyse the sequential circuit shown below in figure. Assuming that initial state is 00, determine what input sequence would lead to state 11?



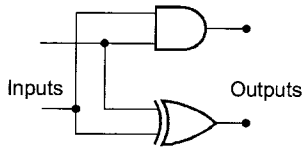
(a) 1 – 1
(b) 1 – 0
(c) 0 – 0
(d) State 11 is unreachable

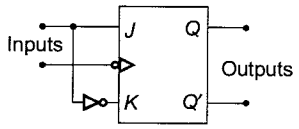
Q.10 Match **List-I** (Logic circuit/function) with **List-II** (Circuit realization) and select the correct answer using the code given below the lists:

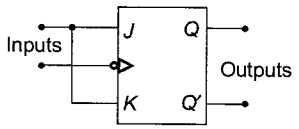
List-I

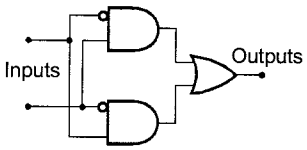
A. *D* flip-flop
B. *T* flip-flop
C. Exclusive OR
D. Half-adder

List-II

1.


2.


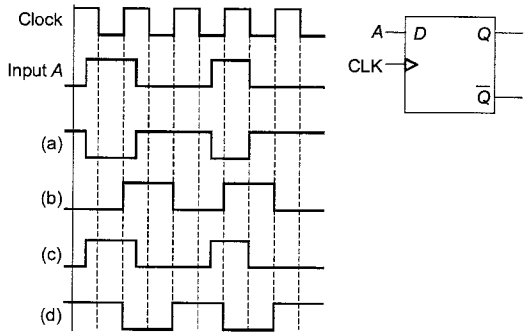
3.


4.


Codes:

	A	B	C	D
(a)	3	2	4	1
(b)	2	3	4	1
(c)	1	3	4	2
(d)	2	4	3	1

Q.11 The input A and clock applied to the *D* flip-flop are shown in figure below. The output $\overline{Q}$ is



Q.12 An *X-Y* flip flop, whose Characteristic Table is given below is to be implemented using a *J-K* flip flop

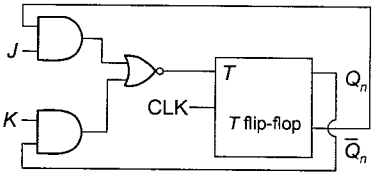
X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q_n}$
1	1	0

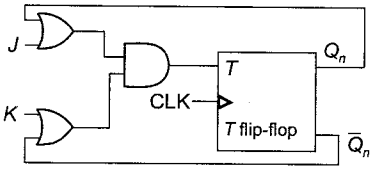
This can be done by making

(a) $J = X, K = \overline{Y}$ (b) $J = \overline{X}, K = Y$

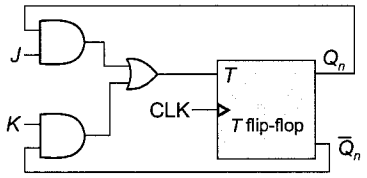
(c) $J = Y, K = \overline{X}$ (d) $J = \overline{Y}, K = X$

Q.13 A J-K flip-flop can be implemented by *T* flip-flop. Identify the correct implementation.

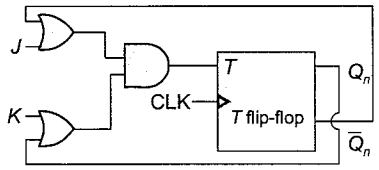
(a)


(b)


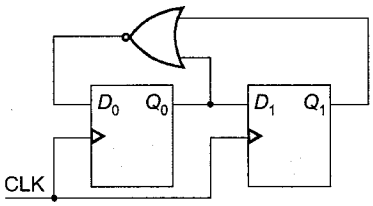
(c)



(d)

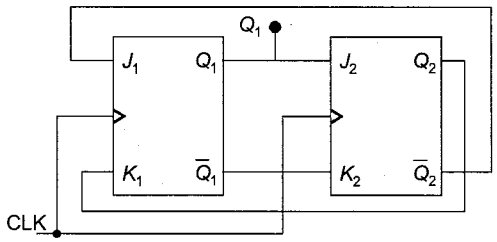


Q.14 For the circuit shown below, the counter state (Q_1Q_0) follows the sequence



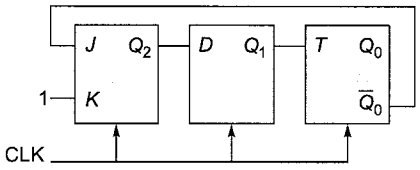
(a) 00, 01, 10, 11, 00 ...
(b) 00, 01, 10, 00, 01 ...
(c) 00, 01, 11, 00, 01 ...
(d) 00, 10, 11, 00, 10 ...

Q.15 The outputs of both the flip-flops Q_1 and Q_2 in the figure shown below are initialized to 0. The sequence generated at Q_1 upon application of clock signal is



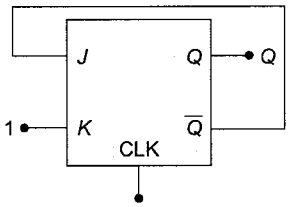
(a) 01110...
(b) 01010...
(c) 00110...
(d) 01100...

Q.16 Consider the following synchronous counter made up of *JK*, *D* and *T* Flip-Flops.



Find the modulus value of the counter.

Q.17 In the following *J-K* flip-flop we have $J = \overline{Q}$ and $K = 1$. Assuming the flip-flop was initially cleared and then clocked for 6 pulses, the sequence at the *Q* output will be



(a) 010000
(b) 011001
(c) 010010
(d) 010101

Q.18 The initial state of MOD-16 down counter is 0110. After 37 clock pulses, the state of the counter will be

Q.19 In clocked RS flip-flop, the output remains as previous output until
(a) $R = 0, S = 1$
(b) $CP = 0$
(c) $R = 1, S = 0$
(d) $R = 1, S = 1$

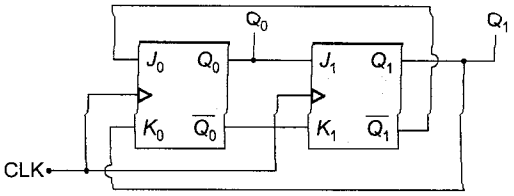
Q.20 An *X-Y* flip-flop, whose characteristic table is given below, is to be implemented using a *JK* flip-flop.

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q}_n$
1	1	0

This can be done by making
(a) $J = X, K =$
(b) $J = \overline{X}, K = Y$
(c) $J = Y, K = \overline{X}$
(d) $J = \overline{Y}, K = X$

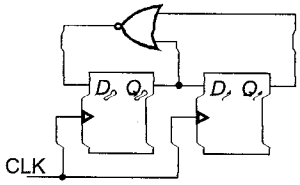
Q.21 A mod-2 counter followed by a mod-5 counter is
(a) same as a mode-5 counter followed by a mod-2 counter
(b) a decade counter
(c) a mod-7 counter
(d) none of these

Q.22 In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1Q_0 = 00$. The state (Q_1Q_0), immediately after the 333rd clock pulse is



(a) 00 (b) 01
(c) 10 (d) 11

Q.23 For the circuit shown below, the counter state (Q_1Q_0) follows the sequence



(a) 00, 01, 10, 11, 00...
(b) 00, 01, 10, 00, 01 ...
(c) 00, 01, 11, 00, 01 ...
(d) 00, 10, 11, 00, 10 ...

Q.24 For the following characteristic table using *XY* flip-flop, the characteristic equation $Q(t+1)$ = _____.

X	Y	$Q(t+1)$
0	0	1
1	0	$Q(t)$
0	1	$\overline{Q}(t)$
1	1	0

(a) $Y\overline{Q}(t)+\overline{X}\overline{Q}(t)$ (b) $\overline{Y}Q(t)+X\overline{Q}(t)$
(c) $\overline{Y}Q(t)+\overline{X}\overline{Q}(t)$ (d) $YQ(t)+X\overline{Q}(t)$

■■■

Answers Sequential Logic Circuits

3.	(d)	4.	(d)	5.	(a)	6.	(d)	7.	(b)	8.	(c)	9.	(b)	10.	(d)	11.	(d)
12.	(b)	13.	(b)	14.	(d)	16.	(d)	18.	(b)	19.	(d)	20.	(a)	21.	(b)	22.	(b)
23.	(c)																

Explanations Sequential Logic Circuits

1. (10)

Here the clock generator is a ring oscillator circuit.

$\therefore$ $f_{CLK} = 1/2Nt_{pd}$

N = number of logic gates

t_{pd} = propagation delay of each logic gate

$N = 5$; $t_{pd} = 10\ ns$

$$f_{CLK} = \frac{1}{2\times5\times10n} = 10MHz$$

2. (6)

The given digital circuit is a asynchronous up-counter.

CLK	Q_2	Q_1	Q_0
–	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0

The modulus value of the counter is six.
So, after six clock pulses the counter reaches its initial state.

3. (d)

For *J-K* flip flop

$$Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

because $K = 1$ always (given)

$\Rightarrow$ in this case, $Q_{n+1} = J\overline{Q}_n$

further given $Q_1 = 0$ and $J = \overline{Q}_1 = 1$

$\Rightarrow Q_2 = J\overline{Q}_1 = 1\,\overline{0} = 1$ and now $J = \overline{Q}_2 = 0$

$Q_3 = J\overline{Q}_2 = 0\,\overline{1} = 0$ and now $J = \overline{Q}_3 = 1$

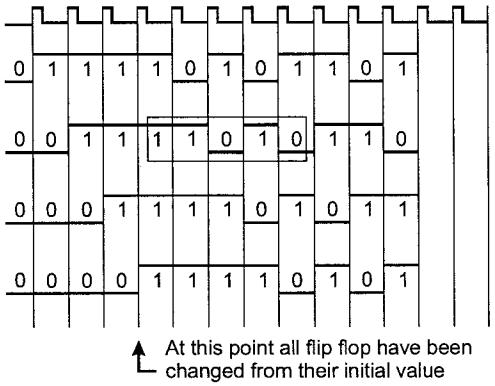
$Q_4 = J\overline{Q}_3 = 1\,\overline{0} = 1$ and now $J = \overline{Q}_4 = 0$

$Q_5 = J\overline{Q}_4 = 0\,\overline{1} = 0$ and now $J = \overline{Q}_5 = 1$

$Q_6 = J\overline{Q}_5 = 1\,\overline{0} = 1$

Thus the sequence of output will be = 010101.

4. (d)



The generated sequence is 1 1 0 1 0 .

5. (a)

For *J-K* flip flop

$$Q^{n+1} = J\overline{Q^n} + \overline{K}Q^n$$

$$Q_A^{n+1} = 1.\overline{Q_A^n} + \overline{Q_B^n}Q_A^n = \overline{Q_A^n} + Q_B^nQ_A^n$$

$$Q_B^{n+1} = Q_C^n \cdot \overline{Q_B^n} + 0 \cdot Q_B^n = Q_C^n \cdot \overline{Q_B^n}$$

$$Q_C^{n+1} = 1 \cdot \overline{Q_C^n} + \overline{Q_A^n} \cdot Q_C^n = \overline{Q_C^n} + Q_A^nQ_C^n$$

Now

$Q_A^0Q_B^0Q_C^0 = 110$

$Q_A^1Q_B^1Q_C^1 = (0+1.1)\,(0.0)\,(1+1.0) = 101$

$Q_A^2Q_B^2Q_C^2 = (0+0.1)\,(1.1)\,(0+1.1) = 011$

$Q_A^3Q_B^3Q_C^3 = (1+1.0)\,(1.0)\,(0+0.1) = 100$

$Q_A^4Q_B^4Q_C^4 = (0+0.1)\,(0.1)\,(1+1.0) = 001$

$Q_A^5Q_B^5Q_C^5 = (1+0.0)\,(1.1)\,(0+0.1) = 110$

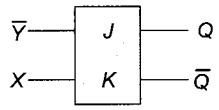
After 5 clocks, it will get back same value.

6. (d)

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q}_n$
1	1	0

The JK flip-flop can be implemented by making

$J = \overline{y},\ K = x$



x	y	$J=\overline{Y}$	$K=X$	Q_{n+1}
0	0	1	0	1
0	1	0	0	Q_n
1	0	1	1	$\overline{Q}_n$
1	1	0	1	0

which is true

Hence (d) is correct option.

8. (c)

Given,

$Q_A\,Q_B = 0\,0$

Then, $z = \overline{x}$

If $x = 0$; we will get

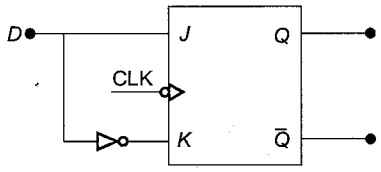
$z = 1$

$x = 0$ is only in option (c). Similarily for next state we need input $x = 0$.

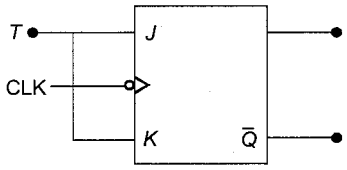
Hence for output state 1 1; input is 0 0.

9. (b)

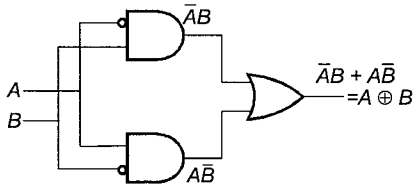
1. *D* flip flop



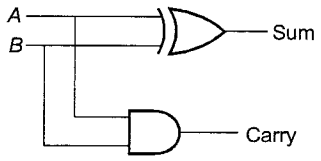
2. *T* flip flop



3. Exclusive OR



4. Half adder



So option is 2, 3, 4, 1 is right.

10. (d)

D flip-flop changes its output according to input and clock pulse applied to it. The flip flop shown in figure is positive edge triggered so the output modifies at every positive edge of clock according to the input.

11. (d)

X - *Y* truth table

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q_n}$
1	1	0

J-K truth table

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

Excitation table

$Q(t)$	$Q(t+1)$	J	K	X	Y
0	0	0	×	×	1
0	1	1	×	×	0
1	0	×	1	1	×
1	1	×	0	0	×

To make (*X* – *Y*) *FF* using (*J* – *K*) *FF*, (*J*) should be ($\overline{Y}$) and (*K*) should be (*X*).

12. (b)

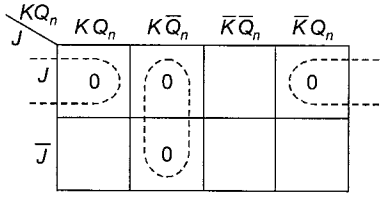
To obtain a JK flip-flop from a *T* flip-flop, we first construct the characteristic table of JK flip-flop; and then obtain the excitation values for the *T* flip-flop as shown below:

J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Characteristic table of JK flip flop → Excitation values for T flip-flop

Now, assuming *T* to be an output, we solve it in terms of *J*, *K*, Q_n inputs. This gives the definition of the logic to be applied on the *T* input.

Also, observing the given options, we solve for *T* using a maxterms map instead of using a minterms map, as shown below:



$$T = (J + Q_n) \cdot (K + \overline{Q}_n)$$

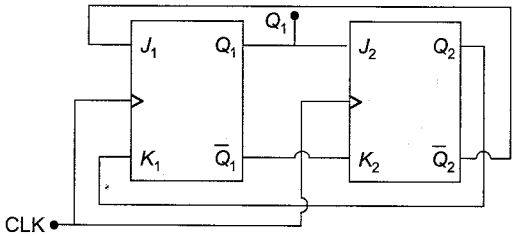
The circuit corresponding to this expression is given option (b).

13. (b)

$$D_1 = Q_0,\ D_0 = Q_0 \odot Q_1$$

$$\Rightarrow (Q_1\ Q_0)\ 00 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow 01...$$

14. (d)



Initially $Q_1 = Q_2 = 0$

Truth table of JK:

J	K	Q_n
0	0	Previous state
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Case-1: 1st clock pulse

$$Q_1 = 0,\ \overline{Q}_1 = 1, Q_2 = 0, \overline{Q}_2 = 1$$

So, $J_1 = 1,\ K_1 = 0$ and $J_2 = 0,\ K_2 = 1$

So $Q_1^+ = 1,\ Q_2^+ = 0$

(new values of Q_1 and Q_2)

Case-2:

$$Q_1 = 1,\ Q_2 = 0$$

$$\overline{Q}_1 = 0,\ \overline{Q}_2 = 1$$

So, $J_1 = 1,\ J_2 = 1$

$K_1 = 0\ \ K_2 = 0$

So, $Q_1^+ = 1,\ Q_2^+ = 1$

(new values of Q_1 and Q_2)

Case-2:

$Q_1 = 1,\ \bar{Q}_1 = 0, Q_2 = 1, \bar{Q}_2 = 0$

$J_1 = 0, K_1 = 1, J_2 = 1, K_2 = 0$

$Q_1^+ = 0,\quad Q_2^+ = 1$

(new values of Q_1 and Q_2)

So, the sequence will be 01100.

15. (5)

Consider characteristic equation of *J-K* Flip-Flop:

$$Q_{2N+1} = J\bar{Q}_{2N} + \bar{K}Q_{2N}$$

$$J = \bar{Q}_0;\ K = 1$$

$$\Rightarrow\quad Q_{2N+1} = \bar{Q}_0\,\bar{Q}_{2N} \qquad ...(i)$$

if $\quad Q_0 = 1 \Rightarrow Q_{2N+1} = 0$

if $\quad Q_0 = 0 \Rightarrow Q_{2N+1} = \bar{Q}_{2N}$

Consider characteristic equation of D – Flip-Flop:

$$Q_{N+1} = D$$

$$Q_{N+1} = Q_2 \qquad ...(ii)$$

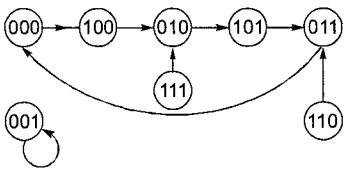
Consider characteristic equation of *T* – Flip-Flop:

$$Q_{N+1} = T \oplus Q_N$$

$$Q_{N+1} = Q_1 \oplus Q_0 \qquad ...(iii)$$

Using equations (*i*), (*ii*) and (*iii*)

Present State			Present State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	0



The number of used states = 5

∴ Modulus value of the counter = 5

16. (d)

When $\quad Q = 0 \Rightarrow \bar{Q} = 1$

So, $\quad J = K = 1$

$\Rightarrow \quad Q_{n+1} = \bar{Q}_n = 1$

When $\quad Q = 1$

$\Rightarrow \quad \bar{Q} = 0$

$J = 0, K = 1$

$\Rightarrow \quad Q_{n+1} = 0$

So, the sequence at the Q output will be 010101.

17. (0001)

$37 = 16 \times 2 + 5$

After 37 clock pulses, the state of MOD-16 DOWN counter will be five states below the present state.

$$\begin{array}{r} 0110\,(6) \\ -0101\,(-5) \\ \hline 0001 \end{array}$$

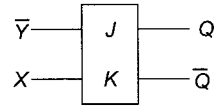
18. (b)

Truth table of clocked RS flip-flop is:

CP	*S*	*R*	Q_n
0	0	0	Q_{n-1}
0	0	1	Q_{n-1}
0	1	0	Q_{n-1}
0	1	1	Q_{n-1}
1	0	0	Q_{n-1}
1	0	1	Reset (i.e. 0)
1	1	0	Set (i.e. 1)
1	1	1	Invalid

19. (d)

X	*Y*	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\bar{Q}_n$
1	1	0



The JK flip-flop can be implemented by making $J = \bar{y},\ K = x$.

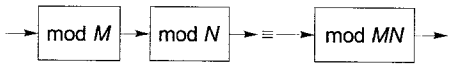
x	y	$J = \bar{Y}$	$K = X$	Q_{n+1}
0	0	1	0	1
0	1	0	0	Q_n
1	0	1	1	$\bar{Q}_n$
1	1	0	1	0

which is true

Hence (d) is correct option.

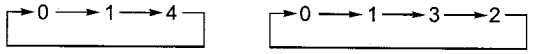
20. (a)

We can replace the positions of counters as shown in Figure.



21. (b)

Clk	Q_1	Q_1	FF1		FF0	
			$J_1 = Q_1$	$K_1 = \bar{Q}_0$	$J_0 = \bar{Q}_1$	$K_0 = Q_1$
	0	0	0	1	1	1
1	0	1	1	0	1	0
2	1	1	1	0	0	1
3	1	0	0	1	0	1
4	0	0				



$N = 4$

$K = 333$

$K \% N = 1 = (01)_2$

22. (b)

$$D_1 = Q_0,\ D_0 = Q_0 \odot Q_1$$

$$\Rightarrow (Q_1 Q_0)\ 00 \rightarrow 01 \rightarrow 10 \rightarrow 00 \rightarrow 01...$$

23. (c)

Using K-map

XY \ $Q(t)$	0	1
00	1	1
01	1	0
11	0	0
10	0	1

$$Q(t+1) = \bar{Y}Q(t) + \bar{X}\bar{Q}(t)$$

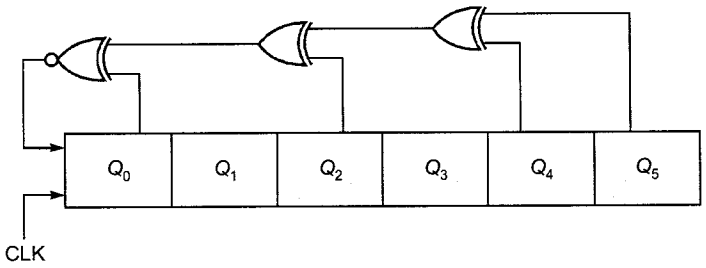
■■■

6 CHAPTER

Computer Science & IT

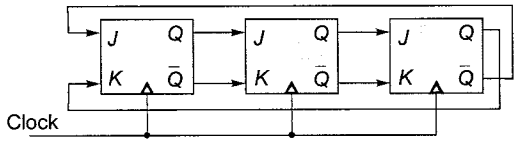
Registers

Q.1 A six bit right shift register is initialized to a value of 100000. Minimum number of clock pulses needed to produce 101101 from the given initial value is _____



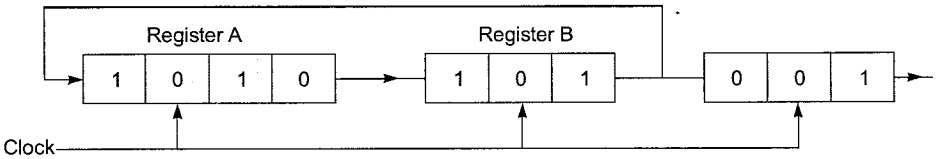
(a) 3
(b) 4
(c) 5
(d) 6

Q.2 For the initial state of 000, the function performed by the arrangement of the *J-K* flip-flop in the given figure is

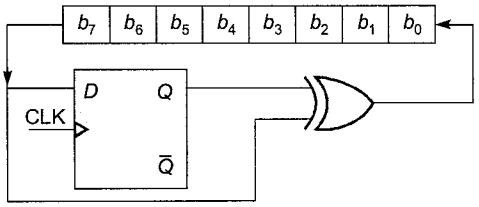


(a) Shift Register
(b) Mod-3 Counter
(c) Mod-6 Counter
(d) Mod-2 Counter

Q.3 Three shift registers are initialized and are connected as shown below, having a common clock. The contents of register-A after 10 clock pulses is _____

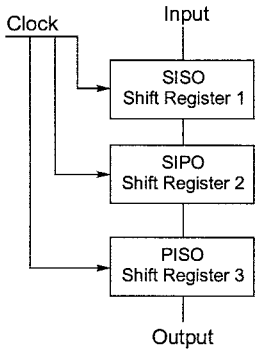


Q.4 A 8-bit shift-left shift register and a *D* flip-flop is shown in the figure are synchronized with the same clock. The *D* flip-flop is initially cleared. The circuit acts as



(a) Binary to 2's complement converter
(b) Binary to Gray code converter
(c) Binary to 1's complement converter
(d) Gray to binary converter

Q.5 Three 4 bit shift registers are connected in cascade as shown in figure below. Each register is applied with



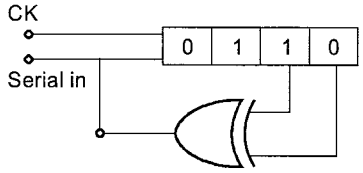
A 4 bit data 1011 is applied to the shift register 1. What is the minimum number of clock pulses required to get same input data at output are with same clock?

(a) 11 (b) 12
(c) 13 (d) 14

Q.6 A decimal number '58' is stored in a register. After performing one right shift operation on this, the content of the register is_____

(a) 0011 1010 (b) 0001 1101
(c) 0111 0100 (d) 1100 0101

Q.7 The initial contents of the 4 bit serial-in-parallel-out right-shift Register shown in figure below, is 0110. After three clock pulses are applied, the contents of the shift Register will be



(a) 0000 (b) 0101
(c) 1010 (d) 1111

Q.8 Consider the following statements regarding registers and latches:

1. Registers are made of edge-triggered FFs, whereas latches are made from level-triggered FFs.
2. Registers are temporary storage devices whereas latches are not.
3. A latch employs cross-coupled feedback connections.
4. A register stores a binary word whereas a latch does not.

Which of the statements given above are correct?

(a) 1 and 2 (b) 1 and 3
(c) 2 and 3 (d) 3 and 4

Q.9 Which of the following capabilities are available in a Universal Shift Register?

1. Shift left 2. Shift right
3. Parallel load 4. Serial add

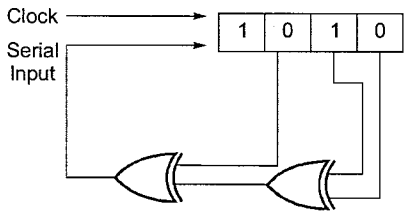
Select the correct answer from the codes given below :

(a) 2 and 4 only (b) 1, 2 and 3
(c) 1, 2 and 4 (d) 1, 3 and 4

Q.10 The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of register after six shifts.

(a) 1101 (b) 1011
(c) 1001 (d) 1110

Q.11 The shift register shown in figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register become 1010 again?



Q.12 Match List-I with List-II and select the correct answer using the codes given below the lists:

List-I
A. Shift register
B. Counter
C. Decoder

List-II
1. Frequency division
2. Addressing in memory chips
3. Serial to parallel data conversion

Codes:

	A	B	C
(a)	3	2	1
(b)	3	1	2
(c)	2	1	3
(d)	1	2	2

Q.13 A 3-bit ripple counter uses J-K flipflops. If the propagation delay of each flipflop is 50 n sec, then what will be the maximum clock frequency that can be used in megahertz?

Q.14 An n stage ripple counter can count up to
(a) 2^n (b) $2^n - 1$
(c) n (d) 2^{n-1}

■■■

Answers Registers

1. (c) 2. (c) 4. (b) 5. (b) 6. (b) 7. (c) 8. (b) 9. (b) 10. (b)
12. (b) 14. (b)

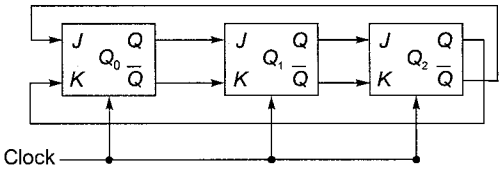
Explanations Registers

1. (c)
Let the output of XNOR gate is Y

CLK	Y	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5
–	0	1	0	0	0	0	0
1	1	0	1	0	0	0	0
2	1	1	0	1	0	0	0
3	0	1	1	0	1	0	0
4	1	0	1	1	0	1	0
5		1	0	1	1	0	1

Minimum five clock pulses are required to get the sequence 101101.

2. (c)
Given figure is a Jhonson counter, so maximum possible states in output will be $2n$, where n is the number of flip-flops.



Initial state = 000

Present state			Next state		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	1	1	1
1	1	1	1	1	0
1	1	0	1	0	0
1	0	0	0	0	0

6 different states.

Hence, option (c) is correct.

3. (1011)

Register-A and Register-B are taken together to form a cyclic register. So, contents in Register-A reappears after 7-clock pulses.

Clock Pulse	Register-A Contents
7	1 0 1 0
8	1 1 0 1
9	0 1 1 0
10	1 0 1 1

4. (b)

The output of XOR gate is $z = b_{i+1} \oplus b_i$ and this output shift the register to left, initially $z = 0$.

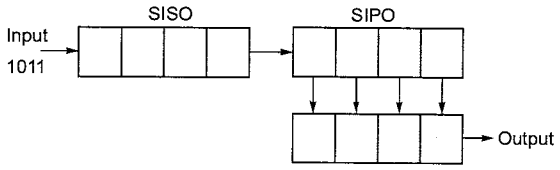
After 1st clock $z = b_7 \oplus 0 = b_7$

After 2nd clock $z = b_7 \oplus b_6$

After 3rd clock $z = b_6 \oplus b_5$

After 4th clock $z = b_5 \oplus b_4$

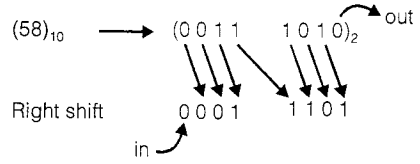
5. (b)



	SISO	SIPO	PISO
Initially	0 0 0 0	0 0 0 0	0 0 0 0
1.	1 0 0 0	0 0 0 0	0 0 0 0
2.	1 1 0 0	0 0 0 0	0 0 0 0
3.	0 1 1 0	0 0 0 0	0 0 0 0
4.	1 0 1 1	0 0 0 0	0 0 0 0
5.		1 0 0 0	0 0 0 0
6.		1 1 0 0	1 0 0 0
7.		0 1 1 0	1 1 0 0
8.		1 0 1 1	0 1 1 0
9.			1 0 1 1
10.			× 1 0 1
11.			× × 1 0
12.			× × × 1

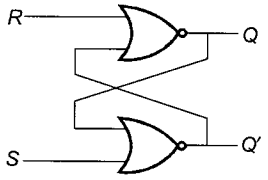
Minimum no. of clock pulses required = 12.

6. (b)



8. (b)

(*i*) SR latch is shown below:



A latch employs cross-coupled feedback connections.

(*ii*) Registers are made of edge-triggered FFs, whereas latches are made from level triggered FFs.

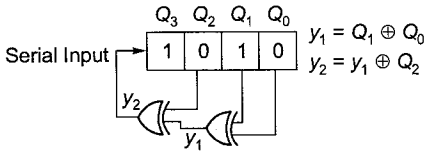
9. (b)

Universal shift register features parallel inputs, parallel outputs. It performs both functions shift left and shift right.

10. (b)

Input bits	4 bit register
	1101
1	→ 1110
0	→ 0111
1	→ 1011
1	→ 1101
0	→ 0110
1	→ 1011

11. (7)



CLK pulse	Q_3	Q_2	Q_1	Q_0
1 → 0	1	0	1	0
2 → 1	1	1	0	1
3 → 2	0	1	1	0
4 → 3	0	0	1	1
5 → 4	0	0	0	1
6 → 5	1	0	0	0
7 → 6	0	1	0	0
	1	0	1	0
7				

$Q_3(t+1) = Q_0(t) \oplus Q_1(t) \oplus Q_2(t)$

12. (b)

Shift register: Serial to parallel data conversion
Counter: Frequency division
Decoder: Addressing in memory chips

13. (6.67)

$$T \geq 3 \times 50 \text{ n sec}$$
$$T \geq 150 \text{ n sec}$$
$$T_{min} = 150 \text{ nsec}$$
$$f_{max} = \frac{1 \times 10^9}{150} = 6.67 \text{ MHz}$$

14. (b)

An n stage ripple counter can count up to the binary value represented by the n-bits.

■■■■

7 CHAPTER

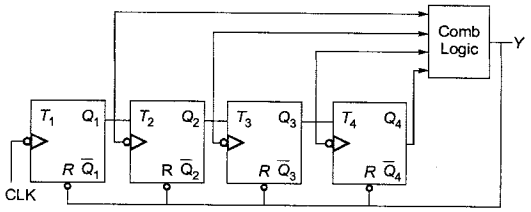
Counters

Q.1 Counter is a
(a) Combinational Circuit
(b) Sequential Circuit
(c) Both (a) and (b)
(d) None of these

Q.2 If a counter having 10 flip flops is initially at 0, what count will it hold after 2060 pulses.
(a) 0000001000 (b) 0000001110
(c) 0000011100 (d) 0000001100

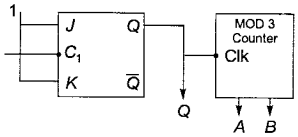
Q.3 How many decade counters are necessary to implement a devide by 1000 counter and divide by 10,000 counter?
(a) 10 (b) 1000
(c) 100 (d) 3

Q.4 The counter shown in figure is built with 4-T flipflops. The flipflops can be reset asynchronous when $R = 0$. The logic required to realize a modulo-14 counter is

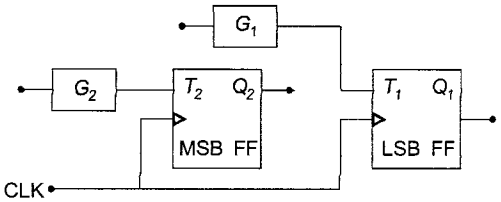


(a) $Y = \overline{Q_4} + \overline{Q_3} + \overline{Q_2} + Q_1$
(b) $Y = Q_4 Q_3 Q_2 \overline{Q_1}$
(c) $Y = Q_4 + Q_3 + Q_2 + \overline{Q_1}$
(d) $Y = \overline{Q_4}\ \overline{Q_3}\ \overline{Q_2}\ Q_1$

Q.5 In figure, initially $Q = A = B = 0$. After three clock triggers, the states of Q, A and B will be respectively is _____.



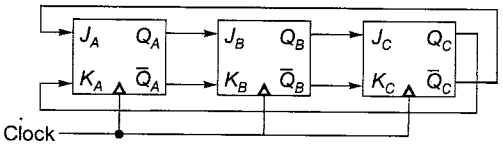
Q.6 By using two T-flip-flops we wish to design a synchronous counter having 2-bit random sequence are : $00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00$



For the design of counter, involved logic gates G_1 and G_2 respectively are:
(a) Ex-OR and NOT gate
(b) Ex-OR and Ex-NOR
(c) NOT and Ex-NOR
(d) NOT and AND

Q.7 Number of flip-flops that would be required to build Mod-19 counter is _____.

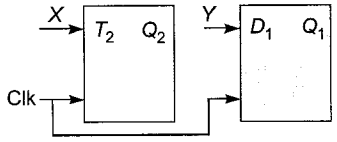
Q.8 For the initial state of 000, the function performed by the arrangement of the J-K flip-flop in the given figure is



(a) Shift Register
(b) Mod-3 Counter
(c) Mod-6 Counter
(d) Mod-2 Counter

Q.9 A 4-bit synchronous UP counter is holding a state 0101. What will be the count after 27^{th} clock pulse?
(a) 0101 (b) 0001
(c) 1111 (d) 0000

Q.10 Consider a two bit counter which implements the sequence 0–2–3–1–0, then



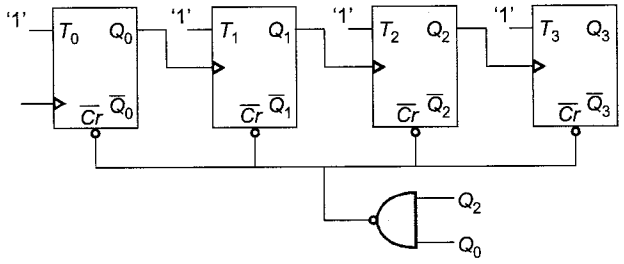
(a) $X = \overline{(Q_1 \oplus Q_2)}$, $Y = Q_2$

(b) $X = Q_1 \oplus Q_2$, $Y = Q_2\overline{Q_1}$

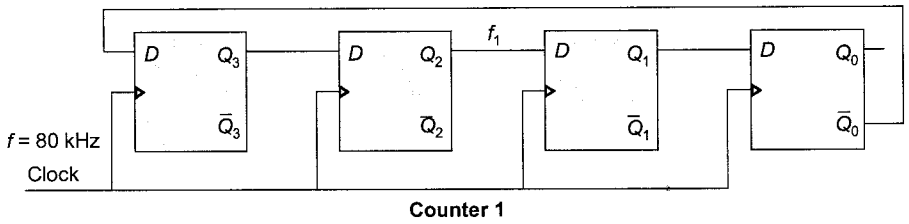
(c) $X = Q_1 + Q_2$, $Y = Q_2$

(d) $X = Q_1 \odot Q_2$, $Y = \overline{Q_2}Q_1$

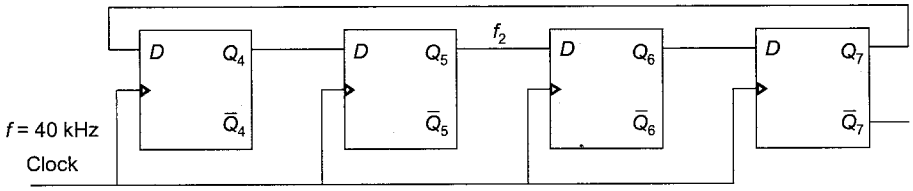
Q.11 A counter made up of *T* flipflops with a feedback circuit is shown below. What is the modulus value of the counter? [Counter is initialy with state 0000]



Q.12 Two counter circuits, counter-1 and counter-2 are shown below with their clock frequencies as 80kHz and 40kHz respectively



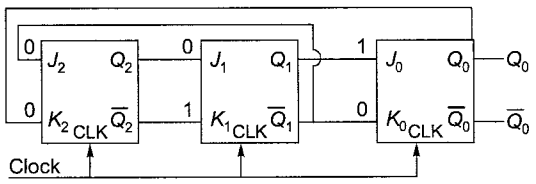
Counter 1



Counter 2

If f_1 and f_2 are frequencies at outputs Q_2 and Q_5 respectively, then what is the value of (f_1 / f_2)?

Q.13 The divide by *N* counter as shown in figure. If initially $Q_0 = 0$, $Q_1 = 1$, $Q_2 = 0$. What is the value of *N*?



(a) 5

(b) 6

(c) 3

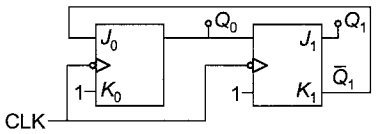
(d) 4

Q.14 A 3-bit ripple counter uses J-K flip-flops. If the propagation delay of each flipflop is 50 n sec, then what will be the maximum clock frequency that can be used in megahertz?

Q.15 A pulse train with a frequency of 1 MHz is counted using a module 1024 ripple counter built with J-K flip-flops. For proper operation of the counter, the maximum permissible propagation delay per flip flop stage is

(a) 10 n sec (b) 100 n sec
(c) 1000 n sec (d) 100 μ sec

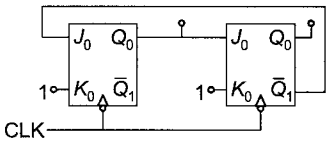
Q.16 The following counter has _____ number of states.



Q.17 A switch-tail ring counter consisting of 5-FFs. If this counter has P-states and it counts maximum decimal number Q the correct values of P and Q respectively are

(a) $P = 32, Q = 32$ (b) $P = 32, Q = 31$
(c) $P = 10, Q = 31$ (d) $P = 5, Q = 16$

Q.18 Figure shows a mod-K counter, Here K is equal to



Q.19 The initial state of MOD-16 down counter is 0110. After 37 clock pulses, the state of the counter will be

Q.20 Match List-I with List-II and select the correct answer using the codes given below the lists:

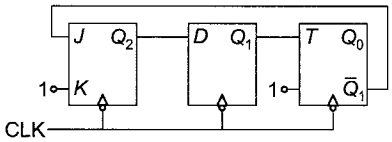
List-I		List-II
A.	Shift register	1. Frequency division
B.	Counter	2. Addressing in memory chips
C.	Decoder	3. Serial to parallel data conversion

Codes:

	A	B	C
(a)	3	2	1
(b)	3	1	2
(c)	2	1	3
(d)	1	2	2

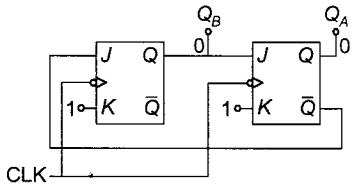
Q.21 A 3-bit ripple counter uses J-K flipflops. If the propagation delay of each flipflop is 50 n sec, then what will be the maximum clock frequency that can be used in megahertz?

Q.22 Consider the following synchronous counter made up of JK, D and T Flip-Flops.



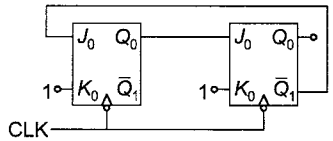
Find the modulus value of the counter.

Q.23 If Q_A is output and initial state is $Q_AQ_B = 00$, the circuit is



(a) Divide by two counter
(b) Divide by three counter
(c) Divide by four counter
(d) No division happens

Q.24 The below figure shows a mod-N counter. The value of N is _____.



(a) 1 (b) 2
(c) 3 (d) 4

■■■

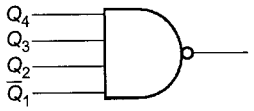
Answers Counters

1. (b) 2. (d) 3. (d) 4. (a) 6. (b) 8. (c) 9. (d) 10. (a) 13. (a)
15. (b) 17. (c) 20. (b) 23. (b) 24. (c)

Explanations Counters

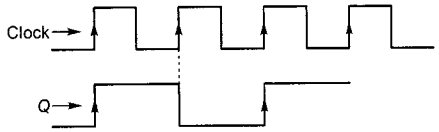
2. (d)
It completes one cycle in 1024 pulses and two cycles in 2048 pulses and 2060 – 2048 = 12.
Binary representation of 12 is 0000001100.

4. (a)
Here in given counter circuit R is preset and 'Q' output is connected as clock. So, a NAND-gate is used as combinational logic circuit.
Mod-14 = 1110
The logic required is $Y = Q_4 Q_3 Q_2 \overline{Q_1}$



$$Y = \overline{Q_4 Q_3 Q_2 \overline{Q_1}} = \overline{Q_4} + \overline{Q_3} + \overline{Q_2} + Q_1$$

5. (110)
J-K flip-flop is in toggle mode so after every clock pulse output Q toggles. So output Q will be as



and Q is input to MOD-3 counter then

after 3 clock pulses of input clock there are 2 +ve edge of clock input Q so output of counter goes to 2 = $(10)_2$
So, AB = 10
So, Q, A and B respectively is 110.

6. (b)
The given random sequence is
(Q_2 Q_1 = 00 → 10 → 11 → 01 → 00 ...)

First of all we write a state table as:

Present State		Next State	
G_{2n}	G_{1n}	G_{2n+1}	G_{1n+1}
0	0	1	0
1	0	1	1
1	1	0	1
0	1	0	0
0	0		

Excitation Table	
T_2	T_1
1	0
0	1
1	0
0	1

From the above state table and excitation table we get,

$$T_2 = \overline{Q_2 \overline{Q_1} + \overline{Q_2} Q_1} = \overline{Q_2 \oplus Q_1} = Q_2 \odot Q_1$$

$\therefore$ $T_2 = Q_2$ (Ex-NOR) Q_1 ...(*i*)

Again, $T_1 = Q_2 \overline{Q_1} + Q_1 \overline{Q_2} = Q_2 \oplus Q_1$

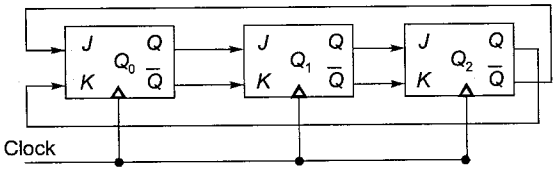
$\therefore$ $T_1 = Q_2$(Ex-OR)Q_1 ...(*ii*)

Since, $T_1 \rightarrow \boxed{G_1} \rightarrow$ Ex-OR gate

and $T_2 \rightarrow \boxed{G_2} \rightarrow$ Ex-NOR gate

7. (5)
As $2^5 = 32$.

8. (c)
Given figure is a Jhonson counter, so maximum possible states in output will be 2 n, where n is the number of flip-flops.



Initial state = 000

Present state			Next state		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	1	1	1
6 different states.					
1	1	1	1	1	0
1	1	0	1	0	0
1	0	0	0	0	0

Hence, option (c) is correct.

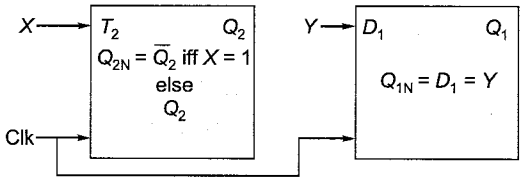
9. (d)

After every modulus the initial state will repeat hence after 16 clock pulses the counter holds the same state i.e., decimal 5.

The remaining clock pulses 27 – 16 = 11, so the final state is 11 + 5 = 16.

For this counter 16 means 0000

10. (a)



Present State		Next State	
Q_2	Q_1	$Q_{2N}(X = Q_1 e\, Q_2)$	$Q_{1N} = Q_2$
0	0	1	0
0	1	0	0
1	0	1	1
1	1	0	1

$00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00$

11. (2)

$$\overline{\overline{Q_2}\,\overline{Q_0}} = \overline{\overline{Q_2}} + \overline{\overline{Q_0}} = Q_0 + Q_2$$

Clk	Q_3	Q_2	Q_1	Q_0	Feedback ckt
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1

So, only 1 state ⇒ It is mod – 2 counter

12. (1)

Counter1 is a twisted ring counter

$$f_1 = \frac{80\,\text{kHz}}{2 \times 4} = 10\,\text{kHz}$$

Counter 2 is a ring counter

$$f_2 = \frac{40\,\text{kHz}}{4} = 10\,\text{kHz}$$

$$\therefore \quad \frac{f_1}{f_2} = \frac{10\,\text{kHz}}{10\,\text{kHz}} = 1$$

13. (a)

$$Q_0^{n+1} = J_0\overline{Q_0^n} + \overline{K_0}Q_0^n = Q_1^n\overline{Q_0^n} + Q_1^nQ_0^n = Q_1^n$$

$$Q_1^{n+1} = J_1\overline{Q_1^n} + \overline{K_1}Q_1^n = Q_2^n\overline{Q_1^n} + Q_2^nQ_1^n = Q_2^n$$

$$Q_2^{n+1} = J_2\overline{Q_2^n} + \overline{K_2}Q_2^n = \overline{Q_1^n}\,\overline{Q_2^n} + \overline{Q_0^n}\,Q_2^n$$

Initial state	Q_2	Q_1	Q_0	decimal
	0	1	0	
clock pulse1 →	0	0	1	1
clock pulse2 →	1	0	0	4
clock pulse3 →	1	1	0	6
clock pulse4 →	1	1	1	7
clock pulse5 →	0	1	1	3
clock pulse6 →	0	0	1	axis of system
clock pulse7 →	1	0	0	4

Here 5 states appeared so the value of $N = 5$.

14. (6.67)

$$T \geq 3 \times 50\ \text{n sec}$$

or $$T \geq 150\ \text{n sec}$$

$$T_{min} = 150\ \text{nsec}$$

$$f_{max} = \frac{1 \times 10^9}{150} = 6.67\ \text{MHz}$$

Since loading is synchronous type, for every nibble to load, one clock pulse is needed.

No. of clock pulses	Operation
1	LSB nibble written
4	LSB nibble read
1	MSB nibble written
4	MSB nibble read

Total clock pulses = 1 + 4 + 1 + 4 = 10

15. (b)

Pulse train frequency = 1 MHz = 10^6 cycles/sec

⇒ 1 pulse takes = 10^{-6} sec

And so, maximum propagation delay permissible through all stages = 10^{-6} sec. Now because the ripple counter in question is modulo 1024 ripple

counter ⇒ it will be n bit ripple counter with $2^n = 1024$, i.e. $n = 10$, so there will be 10 stages in the counter.

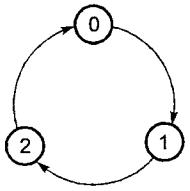
So the maximum permissible propagation delay per flip flop stage

$$= \frac{10^{-6}}{10} = 100 \times 10^{-9} \text{ sec} = 100 \text{ n sec.}$$

16. (3)

CLK	J_0	K_0	Q_0	J_1	K_1	Q_1	$\overline{Q}_1$
0	1	1	0 (let)	0	1	0 (let)	1
1	1	1	1	1	1	0	1
2	0	1	0	0	1	1	0
3	1	1	0	0	1	0	1
4	1	1	1	1	1	0	1

So, state diagram of the counter will be



∴ It has 3-states.

17. (c)

The switch-tail ring conter is nothing but a twisted ring counter or Johnson counter.

With n-FFs, the total number of possible states $= 2n = 2 \times 5 = 10$

∴ $P = 10$

Also with n-FFs the maximum count by this counter is $= (2^n - 1)_{10} = (2^5 - 1)_{10} = (31)_{10}$

$Q = 31$

18. (3)

Let initial $Q_1 = Q_0 = 0$

J_0	K_0	J_1	K_1	Q_1	Q_0
				0	0
1	1	0	1	0	1
1	1	1	1	1	0
0	1	0	1	0	0

It is a mod-3 counter (00 → 01 → 10 → 00)

So, $K = 3$

19. (0001)

$$37 = 16 \times 2 + 5$$

After 37 clock pulses, the state of MOD-16 DOWN counter will be five states below the present state.

$$\begin{array}{r} 0110\,(6) \\ -0101\,(-5) \\ \hline 0001 \end{array}$$

20. (b)

Shift register: Serial to parallel data conversion

Counter: Frequency division

Decoder: Addressing in memory chips

21. (6.67)

$$T \geq 3 \times 50 \text{ n sec} = 150 \text{ nsec}$$

$$T_{min} = 150 \text{ nsec}$$

$$f_{max} = \frac{1 \times 10^9}{150} = 6.67 \text{ MHz}$$

22. (5)

Consider characteristic equation of J-K Flip-Flop: $Q_{2N+1} = J\overline{Q}_{2N} + \overline{K}Q_{2N}$

$J = \overline{Q}_0; K = 1 \Rightarrow Q_{2N+1} = \overline{Q}_0 \overline{Q}_{2N}$ ...(i)

if $Q_0 = 1 \Rightarrow Q_{2N+1} = 0$

if $Q_0 = 0 \Rightarrow Q_{2N+1} = \overline{Q}_{2N}$

Consider characteristic equation of D-Flip-Flop:

$Q_{N+1} = D$

$Q_{N+1} = Q_2$ ...(ii)

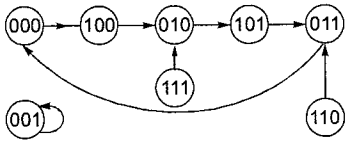
Consider characteristic equation of T-Flip-Flop:

$Q_{N+1} = T \oplus Q_N$

$Q_{N+1} = T_1 \oplus Q_0$ ...(iii)

Using equations (i), (ii) and (iii)

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	1	0	1
0	1	1	0	0	0
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	0	1	0



The number of used states = 5

∴ Modulus value of the counter = 5

23. (b)

CLK	Q_A	$Q_B = J_2$	$J_1 = \overline{Q}_A$
0	0	0	1
⎍ 1	0	1	1
⎍ 2	1	0	0
⎍ 3	0	0	1
⎍ 4	0	1	1
⎍ 5	1	0	0

From the above for every 3 clk pulses. Q_A giving 1 cycle. So, divide by 3 counter.

24. (c)

$J_1 = Q_0$, $K_1 = 1$ and $J_0 = \overline{Q}_1$, $K_0 = 1$

J_1	K_1	J_0	K_0	Q_1	Q_0
–	1	–	1	0	0
0	1	1	1	0	1
1	1	1	1	1	0
0	1	0	1	0	0