Mobile용 PMIC 설계

2010년도 AIPRC Power IC 설계 기술 Workshop

2010년 12월 9일

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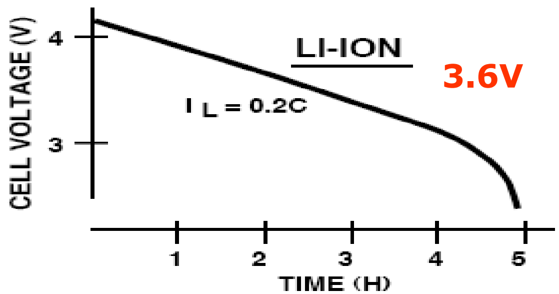
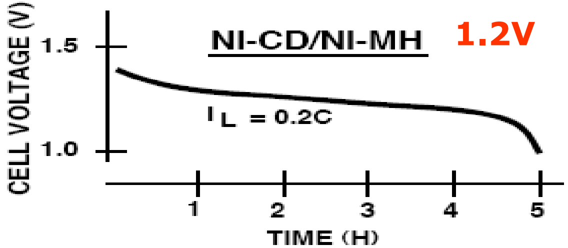
Power Sources for Mobile Devices

● Typical Battery Characteristics





✓ One Cell Enough

✓ Regulation Required

✓ Multiple Cells Required

● Various Power Supply Voltages for ICs

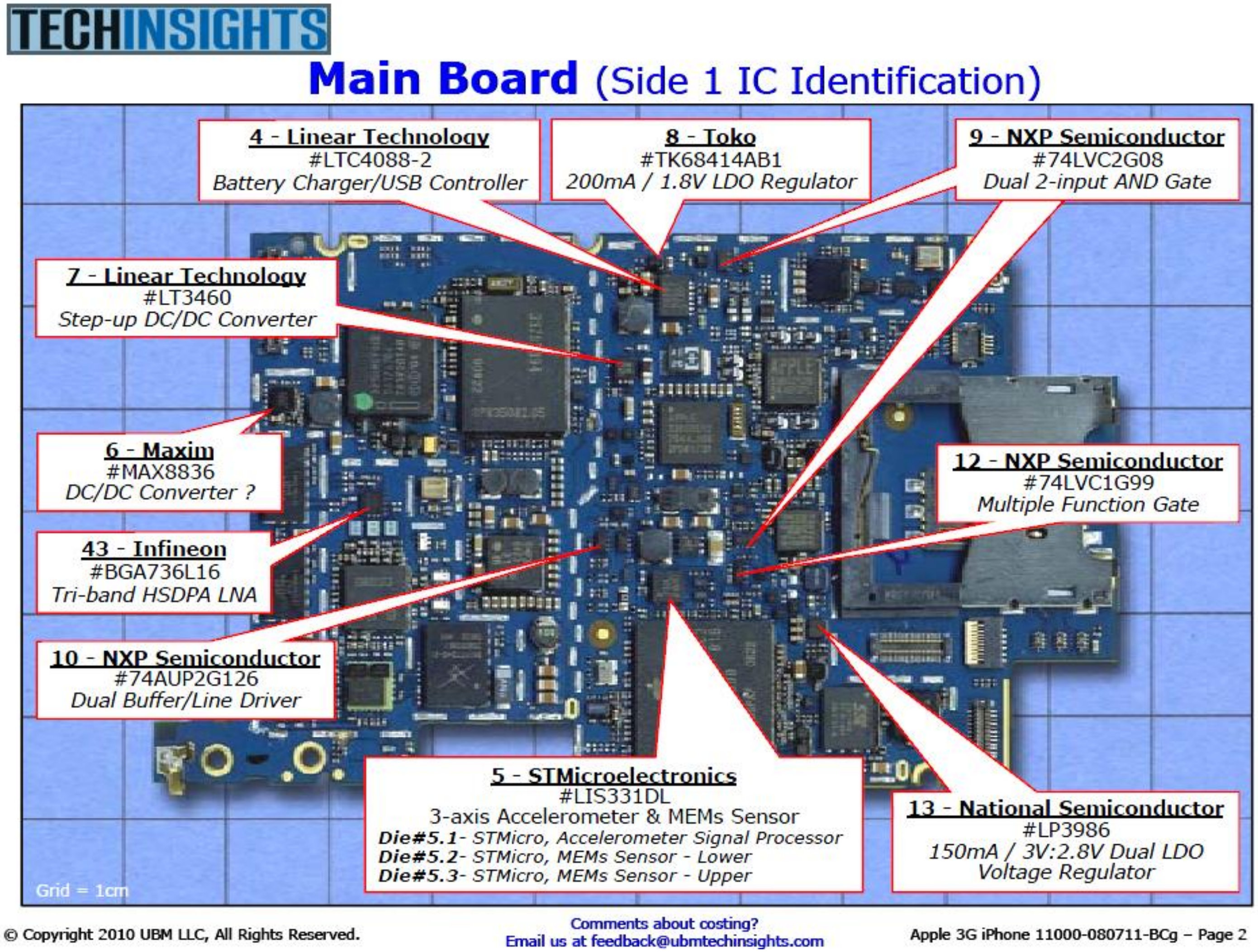
- Supply Voltage Values (Even Negative Polarity)
- Load Current Amount to be Used
- Noise Immunity
- Sensitivity to Load and Line Variations
- For Different Functional Blocks

PMIC for Mobile Applications

- Small Form-Factor
  - ➔ External Inductors, Capacitors, Resistors …
  - ➔ Increased Operating Frequency & Bandwidth
- Reducing The Number of External Off-Chip Components
  - ➔ Proper Topology to be Adopted
  - ➔ New Techniques to be Studied
- Integration of Various Power Sources into Single Chip
  - ➔ Complexity & Interference
  - ➔ Proper IC Fabrication Technology
- Longer Battery Time : Low-Power Design
- Multi-Channel Application : Matching Important
- Multi-Functions Available Through Digital Control

Difficulties in IP Integration

Apple iPhone 3G Example

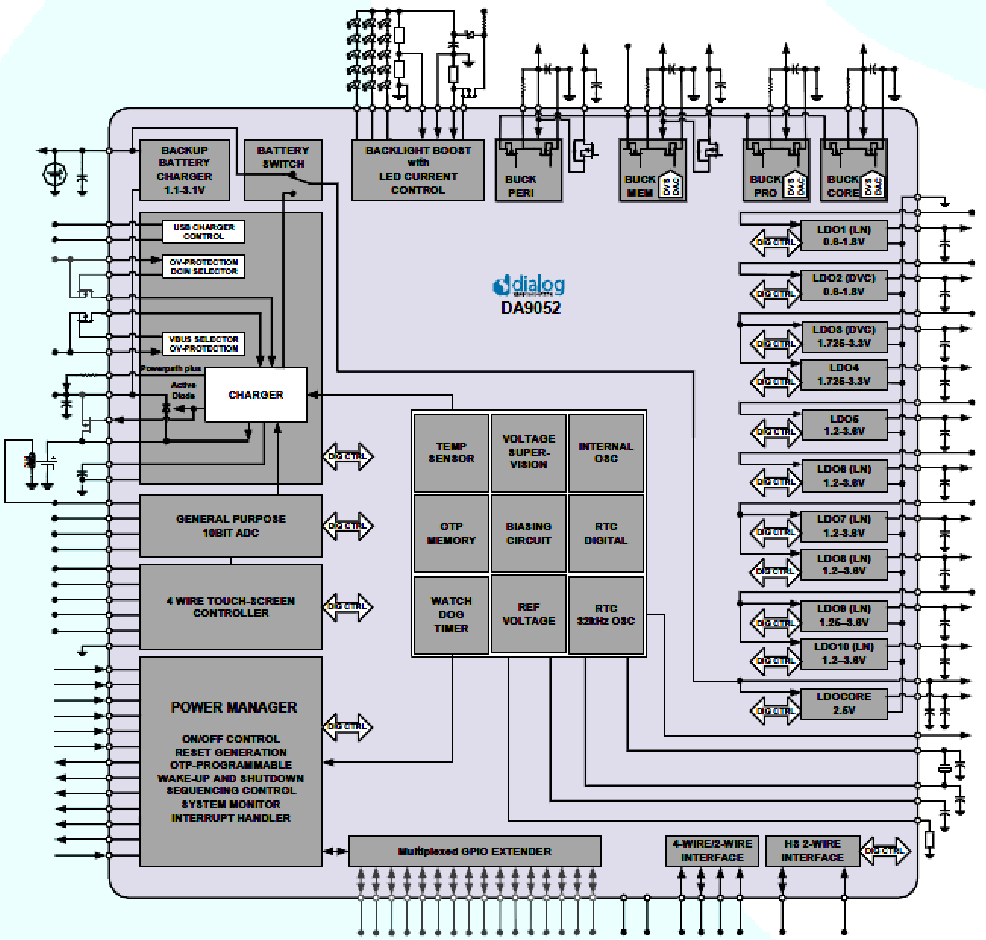


http://www.umbtechinsights.com

Apple iPhone 4 Example

http://www.umbtechinsights.com

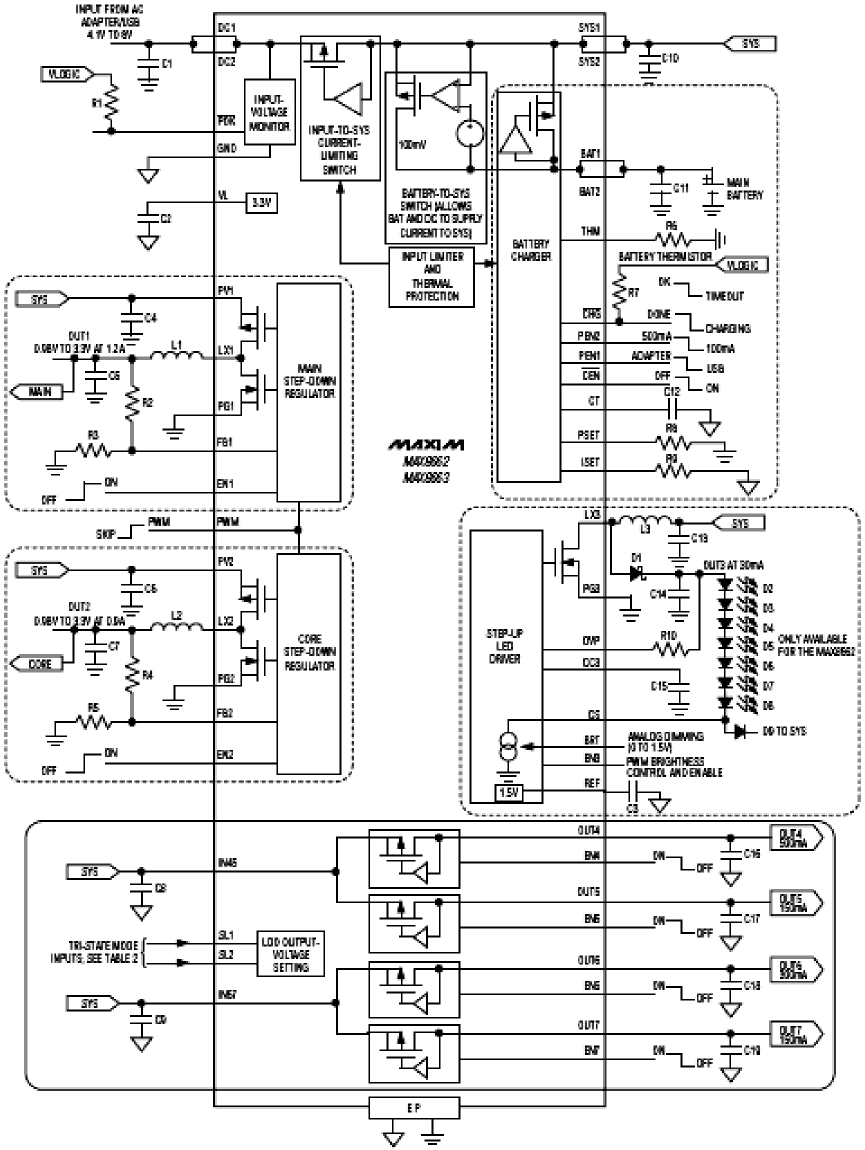
DA9502 (Dialog-Semi) Example



Features

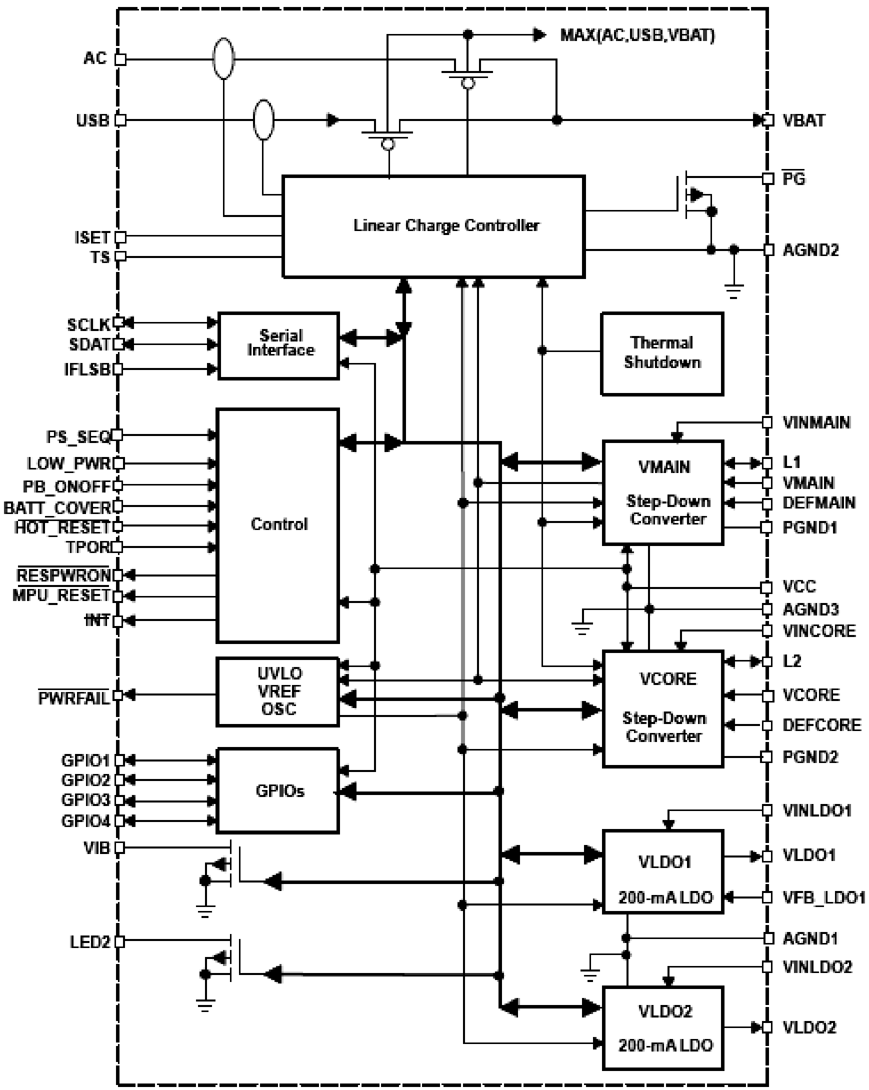
- Switched DC/USB Charger with power path management
- 4 DVS Buck Converters 0.5V-3.6V up to 1Amp
- 10 Programmable LDO's High PSRR, 1% accuracy.
- Low power Backup Charger 1.1-3.1V up to 6mA
- 32kHz RTC Oscillator
- General Purpose ADC with touch screen interface
- High voltage White LED driver 24V/ 50Ma Boost, 3 strings
- 16 bit GPIO bus for enhanced wakeup and peripheral control
- Dual serial control interfaces
- Unique ID code capability with OTP memory

MAX8662 (Maxim) Example



- **Two 95%-Efficient 1MHz DC-DC Buck Converters**
  - Main: 0.98V to VIN at 1200mA
  - Core: 0.98V to VIN at 900mA
- **1MHz Boost WLED Driver**
  - Up to 7 White LEDs at 30mA (max)
  - PWM and Analog Dimming Control
- **Four Low-Dropout Linear Regulators**
  - 1.7V to 5.5V Input Range
  - 15μA Quiescent Current
- **Single-Cell Li+ Charger**
  - Adapter or USB Input
  - Thermal-Overload Protection
- **Smart Power Selector (SPS)**
  - AC Adapter/USB or Battery Source
  - Charger-Current and System-Load Sharing

TPS65011 (TI) Example



- Linear Charger Management for Single Li-Ion or Li-Polymer Cells
- Dual Input Ports for Charging From USB or Wall Plug, (100/500-mA USB Req.)
- 1-A, 95% Efficient Step-Down Converter for I/O and Peripheral Components (VMAIN)
- 400-mA, 90% Efficient Step-Down Converter for Processor Core
- 2x 200-mA LDOs for I/O and Peripheral Components
- Serial Interface Compatible w/ I^{2}C
- 100-kHz, 400-kHz Operation
- 70-μA Quiescent Current
- 1% Reference Voltage
- Thermal Shutdown Protection

Typical Power Source Options

	Applications	Efficiency	Cost	Noise
LDO* Linear Regulator	$V_{OUT} < V_{IN}$	C	A	A
Charge Pump Converter**	$V_{OUT} >< V_{IN}$	B	C	C
DC-DC Boost Converter	$V_{OUT} > V_{IN}$	A	C-	C-
DC-DC Buck Converter	$V_{OUT} < V_{IN}$	A	C-	C-
DC-DC Buck/Boost Converter	$V_{OUT} >< V_{IN}$	A-	C-	C-

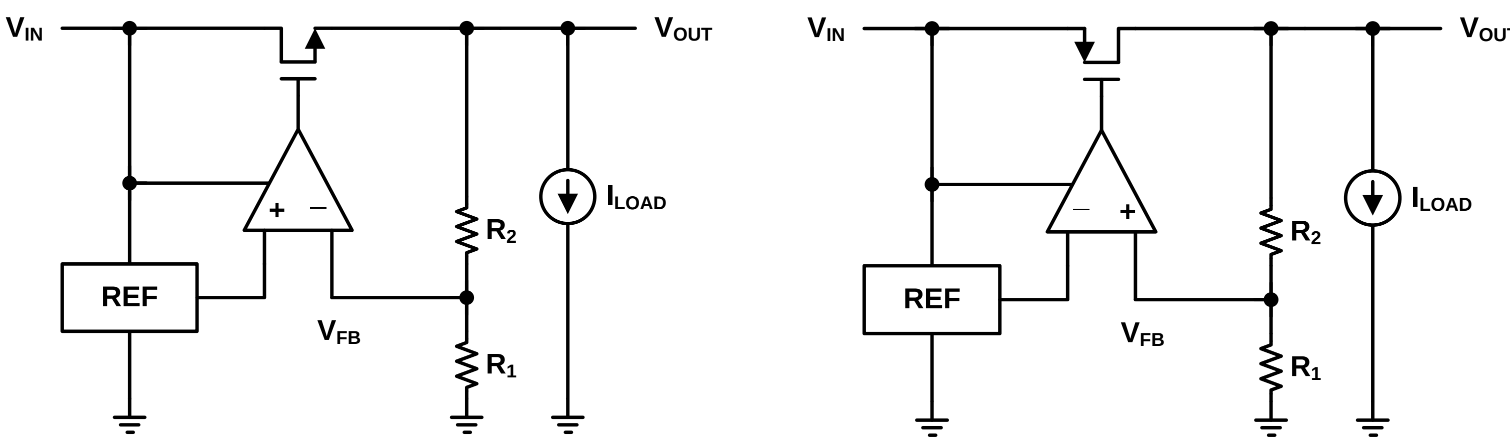
* LDO : Low-Drop Out

** Limited Output Voltage Values & Load Current

- **Optimum Power Management Required**

LDO Linear Regulator

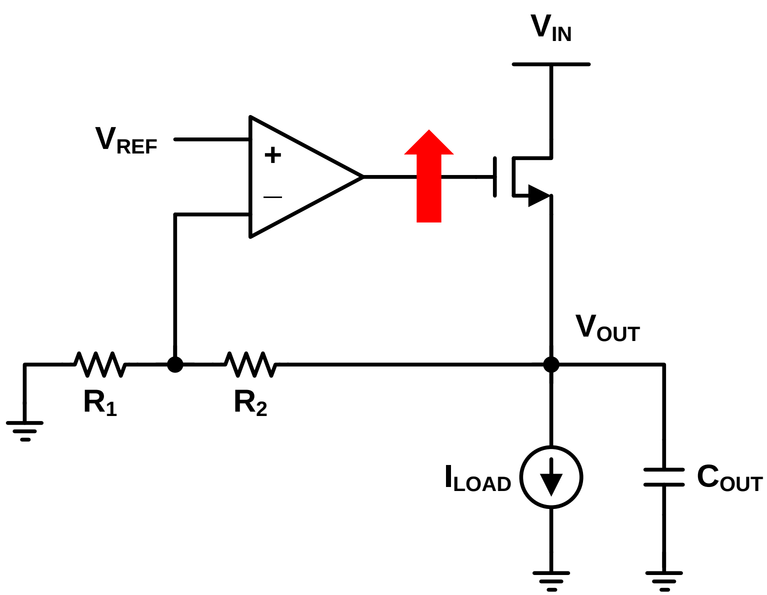
Linear Regulator Basic Principle



- Error Amplifier, Pass Transistor (Output Transistor), Voltage Reference, Feedback Network
- V_{GS} of Pass Transistor Controlled by Error Amplifier for Defined V_{DS}
- Output Voltage Regulated w.r.t. Varying V_{IN} and I_{LOAD}
- Stable Operation Required
- Efficiency η (ideal) = $(V_{IN}-V_{OUT})/V_{IN}$

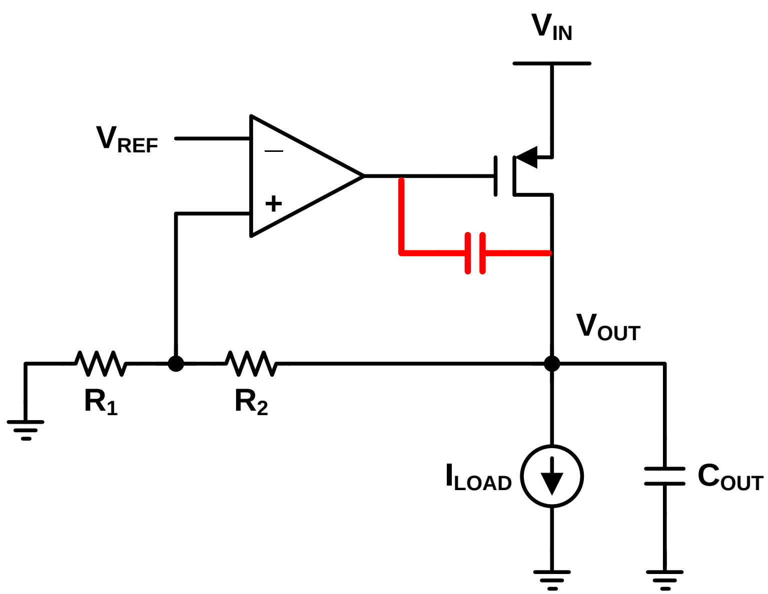
Low-Drop Out Design Restriction

■ OUTPUT NMOSFET



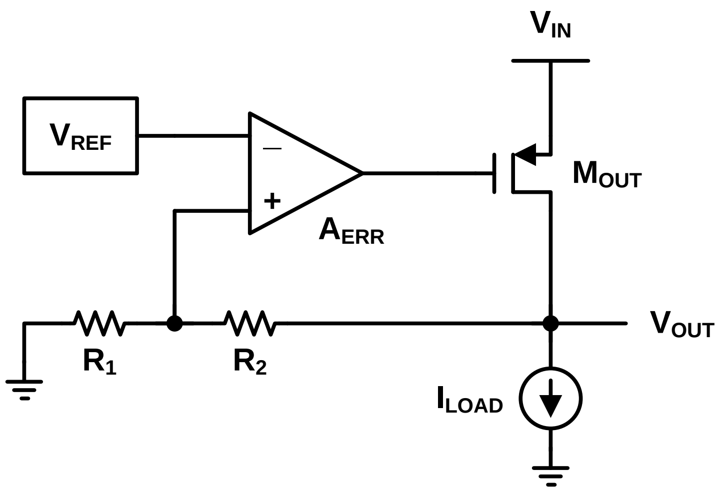
- More Stable Operation
- Difficult for LDO Design

■ OUTPUT PMOSFET



- Easy for LDO Design
- Less Stable Operation

Static Performance



- Feedback Gain

$$\beta \equiv \frac{R_1}{R_1 + R_2}$$

- Loop Gain

$$A_{LG} = A_{ERR} \cdot A_{M_{OUT}} \cdot \beta$$

- **Transfer Function**

$$\frac{V_{OUT}}{V_{REF}} = \frac{A_{ERR} \cdot A_{M_{OUT}}}{1 + A_{LG}} \approx \frac{1}{\beta} = 1 + \frac{R_2}{R_1}$$

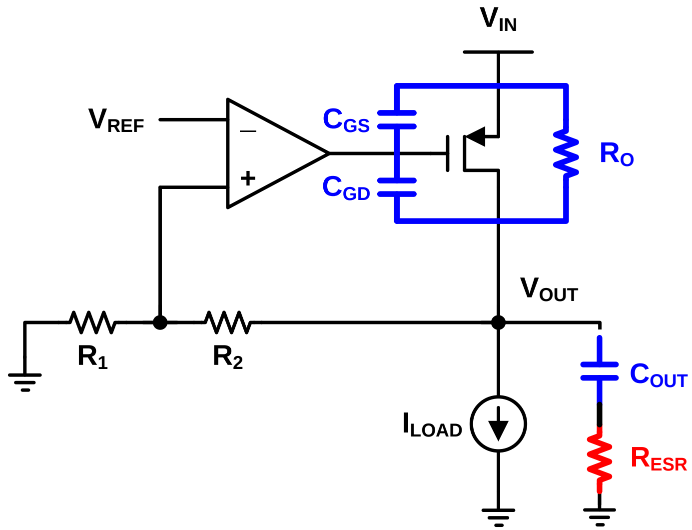
- **Load Regulation**

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = R_{OUT} = \frac{r_{out}|_{M_{OUT}}}{1 + A_{LG}} \approx \frac{1}{A_{ERR} \cdot g_m|_{M_{OUT}} \cdot \beta}$$

- **Line Regulation**

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} = g_m|_{M_{OUT}} \cdot R_{OUT} = g_m|_{M_{OUT}} \cdot \frac{r_{out}|_{M_{OUT}}}{1 + A_{LG}} \approx \frac{1}{A_{ERR} \cdot \beta}$$

Poles of LDO Regulator



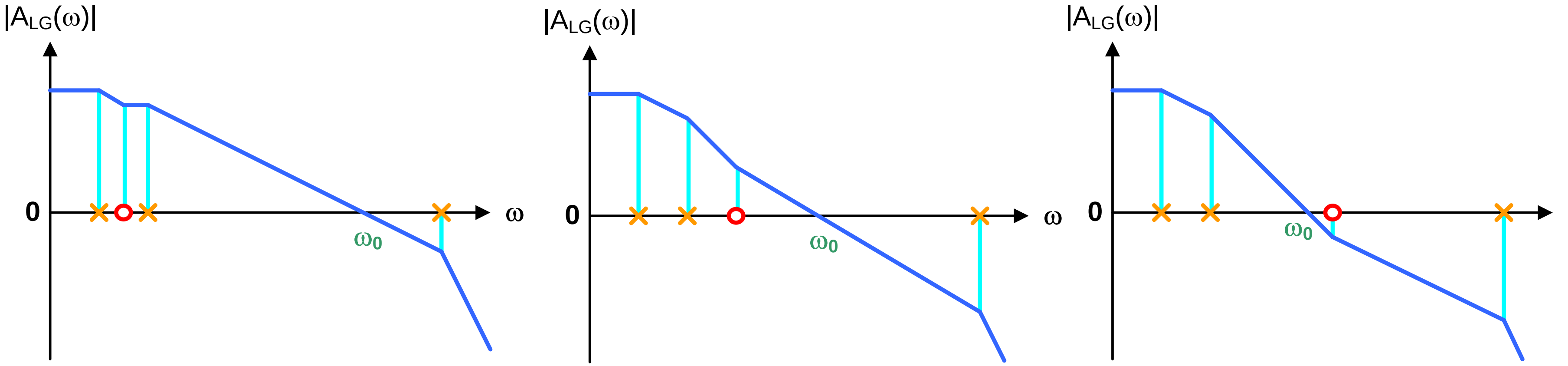
- Error Amp Output ➔ Related w/ Large C_{GS} & C_{GD}
- Output Node ➔ Related w/ Varied R_O & Very Large C_{OUT}
- Other Parasitic Capacitance Related Poles (High-Frequency)

- For Easiest Frequency Compensation,

  Use the Capacitor ESR (Equivalent Series Resistance)

$$\omega_{ZERO} = \frac{1}{R_{ESR} C_{OUT}}$$

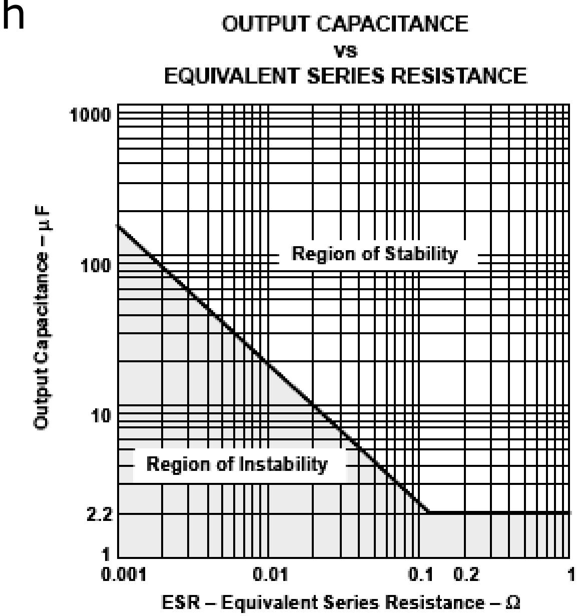
Limited Usage of ESR



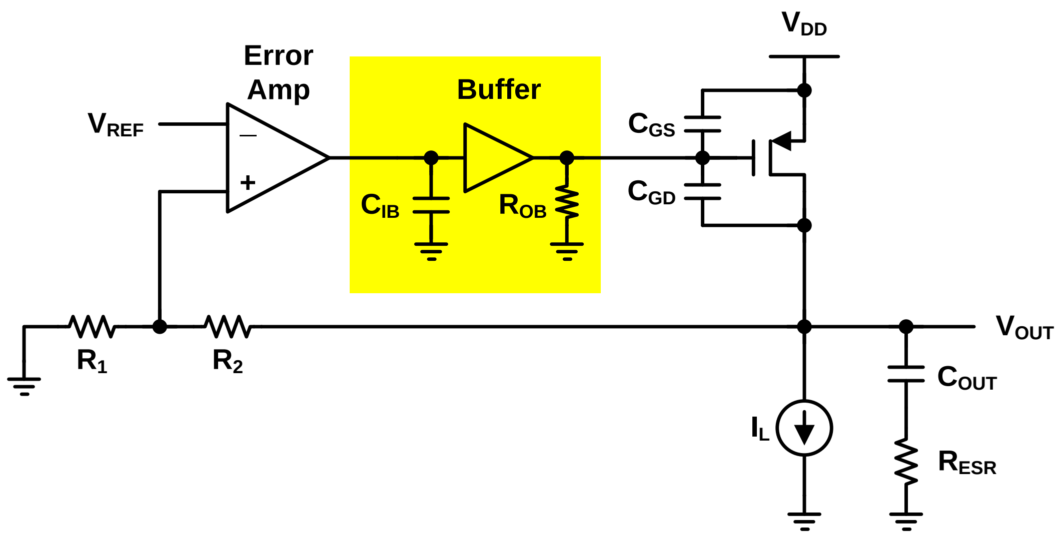
☑ Stable but
Reduced Bandwidth

☑ Unstable

- As R_{ESR} Smaller (Zero Increased)
  ➔ Unstable
- Limited Value of R_{ESR} for Fixed C_{OUT}
- As R_{ESR} Increased
  ➔ Larger Perturbation during Transient



3-Stage LDO Regulator

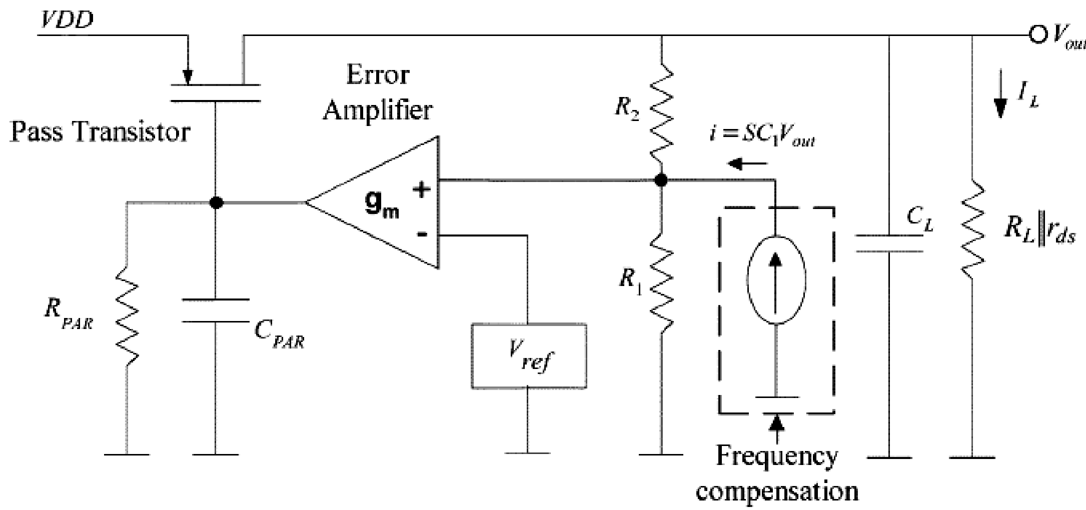


- Pole @ Error Amp Output $1/(r_{oERR}C_{IB}) > 1/(r_{oERR}C_{MOUT})$

  ➔ Helpful for Large Zero (Smaller R_{ESR})

- Pole @ Buffer Output $1/(R_{OB}C_{MOUT})$ ➔ Large Enough
- Pole @ LDO Output $1/(R_{OUT}C_{OUT})$
- Parasitic Pole

Compensation w/ Differentiator



$$\omega_{Z1} = \frac{1}{R_2 C_1}$$

$$\omega_{P1} \approx \left[\left\{ r_{ds} \| (R_1 + R_2) \| R_L \right\} \left\{ C_L - \frac{C_1}{1 + R_2 / R_1} \right\} \right]^{-1}$$

$$\omega_{P2} \approx \left[R_{par} \left\{ C_{par} + g_{mpass} \left(r_{ds} \| (R_1 + R_2) \| R_L \right) C_{gdpass} \right\} \right]^{-1}$$

📖 *IEEE TCAS-I*, pp.1041-1050, 2004 (Texas A&M Univ.)

Design Considerations

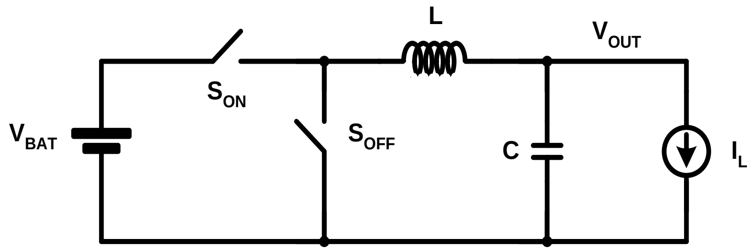
- Non-Idealities
  - Limited Loop Gain for Stability
  - Accuracy of Reference Voltage
  - Offset Voltage of Error Amplifier ➔ Severe for Low V_{REF}
  - Temperature Variation

- High-Performance Required
  - Reduced Standby Current Consumption
  - Fast Transient Operation
  - Improved Line/Load Regulation
  - Large Output Transistor for Higher Current Capability
  - Handling of Large Dynamic Switching Load Current
  - Possible Lack of External Capacitor

DC-DC Converter

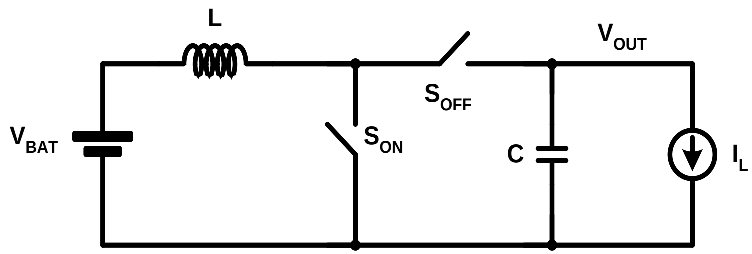
DC-DC Converter Basic

- **Buck (Step-Down) Converter**



$$V_{OUT} = D \cdot V_{BAT} = \frac{T_{ON}}{T} V_{BAT}$$

- **Boost (Step-Up) Converter**



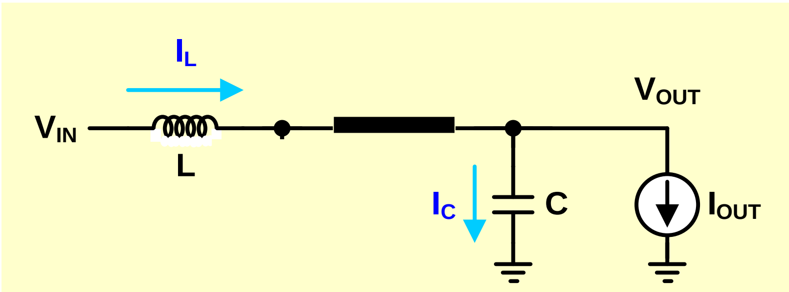
$$V_{OUT} = \frac{1}{1-D} V_{BAT} = \frac{T}{T_{OFF}} V_{BAT}$$

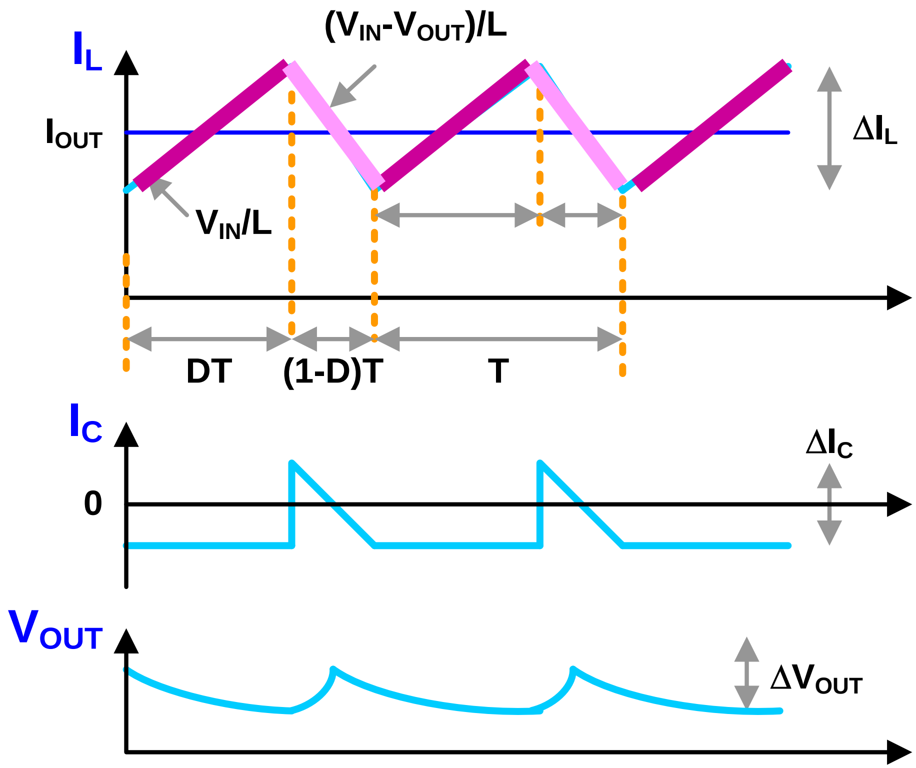
- **Buck/Boost Converter**

Buck + Boost

$$V_{OUT} = \frac{D}{1-D} V_{BAT} = \frac{T_{ON}}{T_{OFF}} V_{BAT}$$

Boost Converter Basic





- On-Time : DT

$$\Delta I_L\big|_{ON} = \frac{1}{L}\int_{DT} V_L(t)dt = \frac{V_{IN}}{L}DT$$

➔ Store Energy in Inductor

- Off-Time : (1-D)T

$$\Delta I_L\big|_{OFF} = \frac{1}{L}\int_{(1-D)T} V_L(t)dt = \frac{V_{IN}-V_{OUT}}{L}(1-D)T$$

➔ Provide I_{OUT}

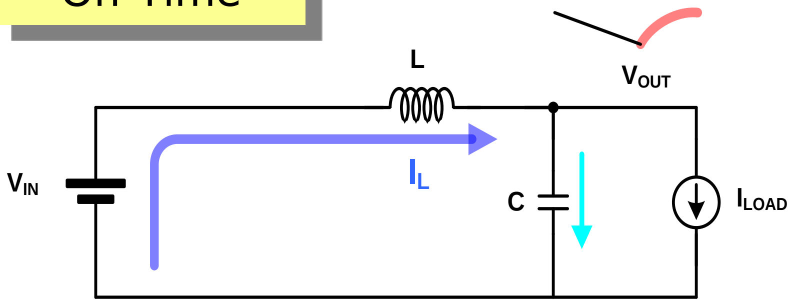
➔ Maintain V_{OUT}

- @ Steady Stage

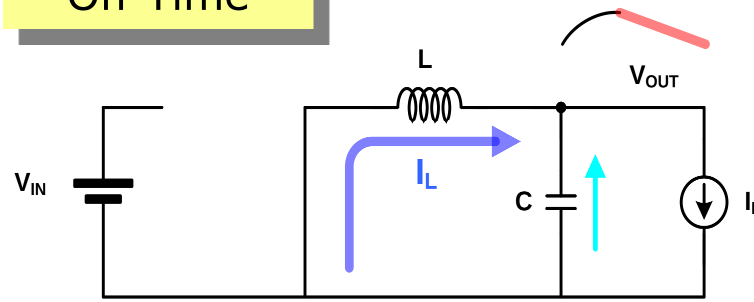
$$V_{OUT} = \frac{1}{1-D}V_{IN}$$

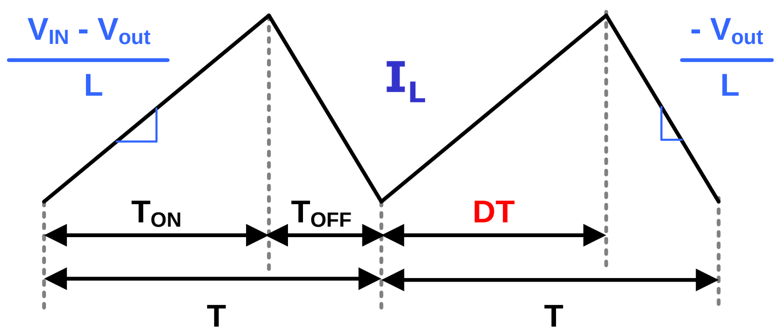
Buck Converter @ Steady State

On-Time



Off-Time

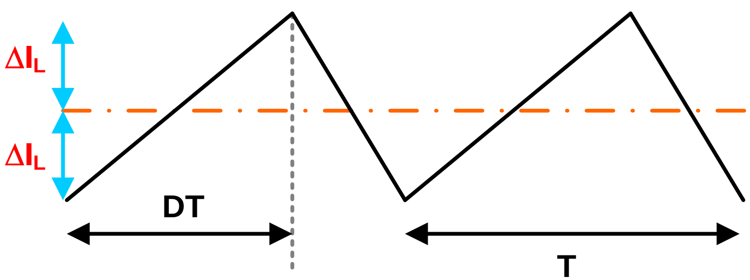




$$\frac{1}{L}\int_T V_L(t)dt = 0$$

$$\frac{1}{L}\cdot(V_{IN}-V_{OUT})\cdot T_{ON} + \frac{1}{L}(0-V_{OUT})T_{OFF} = 0$$

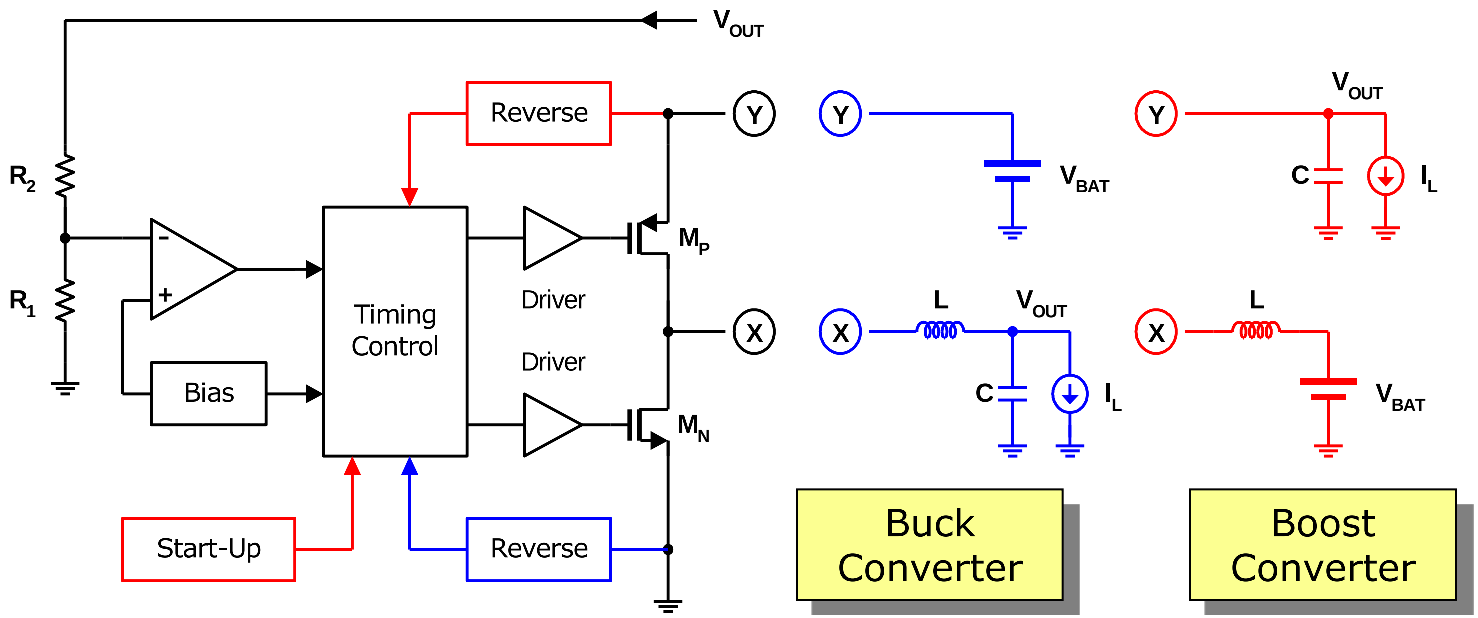
$$\boxed{\therefore \frac{V_{OUT}}{V_{IN}} = \frac{T_{on}}{T} = D}$$



$$2\Delta I_L = \frac{V_{IN}-V_{OUT}}{L}\cdot T_{ON} = \frac{V_{IN}-V_{OUT}}{L}\cdot DT$$

$$\therefore \Delta I_L = \frac{V_{IN}-V_{OUT}}{2L}\cdot DT$$

Architecture



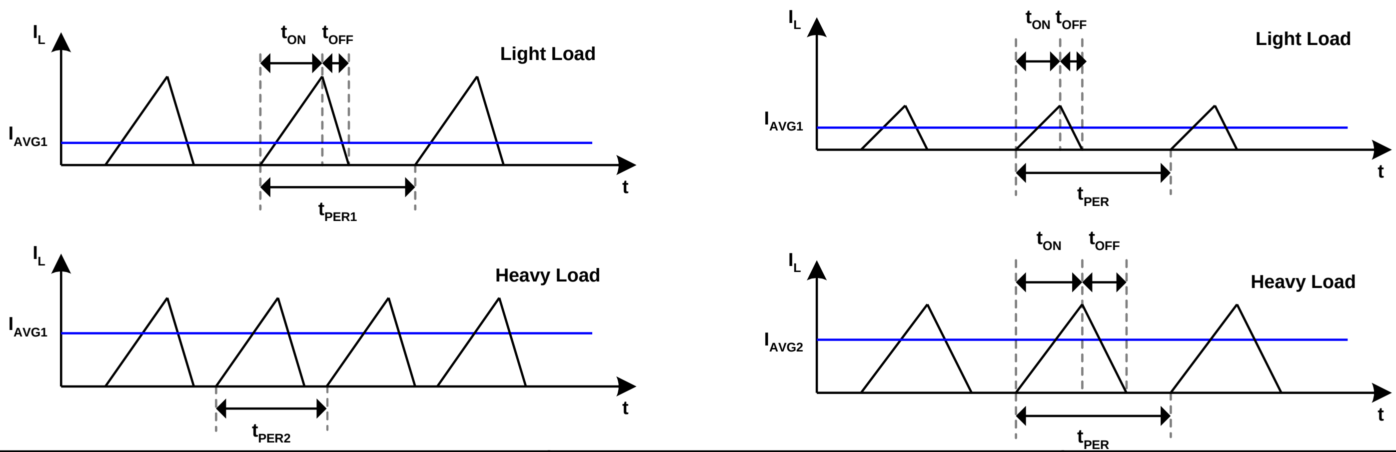
- Large MOSFET Switches ➔ R_{ON} << 100mΩ
- **Timing Control Circuit** for Frequency / Duty-Cycle Programming
- **Negative Feedback Circuit** to Maintain a Output Voltage
- Frequency Compensation for Stable Operation
- Driver Circuits for Driving Large MOSFET Switches
- Protection & Start Up Circuitry

Efficiency η

- **Efficiency η** : P_{output} / $P_{battery}$ = ($P_{battery}$-P_{loss}) / $P_{battery}$

- **Power Loss**
  - ✓ **Conduction Loss**
    - ➔ Load Current Dependent
    - ➔ On-Switch Resistance, DCR of Inductor, ESR of Capacitor
    - ➔ Large MOSFET Switches, Good External Components
  - ✓ **Switching Loss**
    - ➔ Frequency Dependent
    - ➔ Switching Active Devices, Charging Capacitors
    - ➔ Low-Frequency Desirable (Limited by I_{PEAK})
  - ✓ **Fixed Loss**
    - ➔ Bias Current, Leakage Current
    - ➔ Low-Power Design

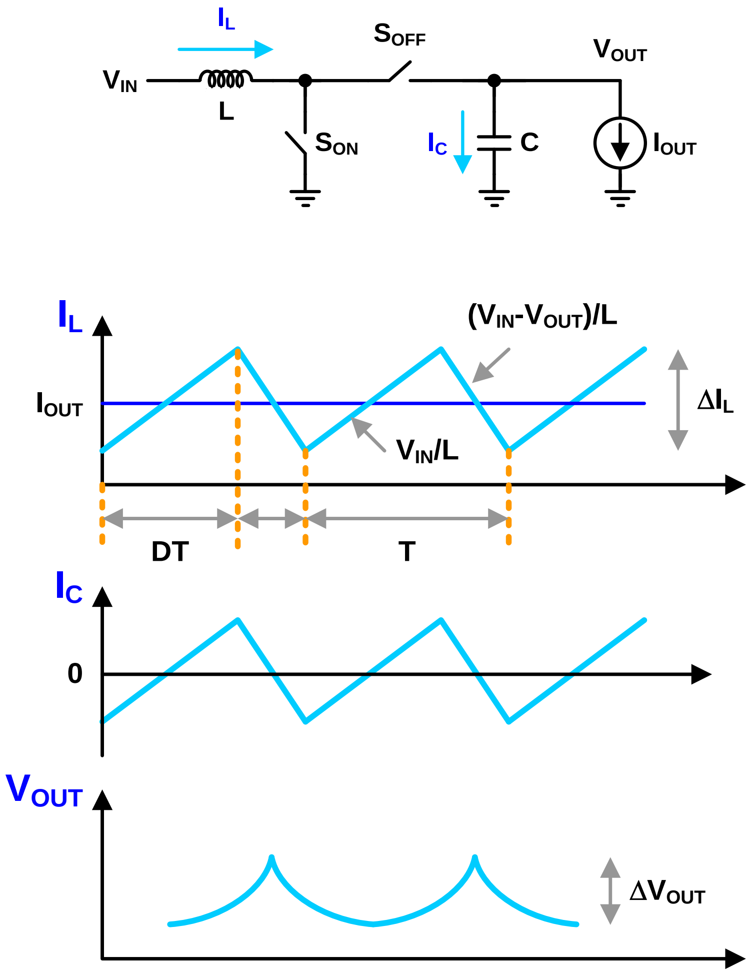
PWM vs. PFM



		PFM	PWM
Average Current		∝ Switching Frequency	∝ Duty Ratio (On-Time)
Peak Current		Constant	Variable
Switching Loss	Light Load Condition	< Conduction	Nearly Constant
	Heavy Load Condition	> Conduction	Nearly Constant
Output Ripple		Possibly Large	Small
Noise Spectrum		Variable	Constant
External L, C Values		Choose to Difficult	Easier

Preferred Approach of Combining Both Modulations

Switching Frequency



- Inductor Current Ripple

$$\Delta I_L = \frac{V_{IN}}{L} DT = \frac{V_{IN} - V_{OUT}}{L}(1-D)T$$

- For CCM Operation

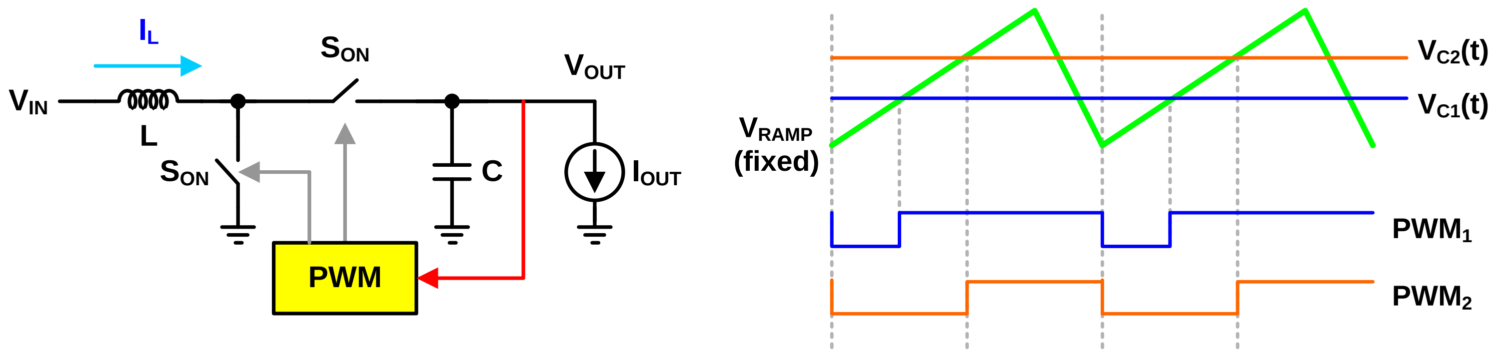
$$I_{OUT} > \frac{\Delta I_L}{2} \Rightarrow L > \frac{1}{2}\frac{R_{OUT}}{f} D(1-D)$$

- Output Voltage Ripple

$$\Delta V_{OUT} \cong \frac{D(1-D)V_{OUT}}{8LC}\frac{1}{f^2}$$

- **Higher Switching Frequency**
  - ➔ Smaller L & C Needed
  - ➔ Preferred for Mobile
  - ➔ High-Speed Switching FETs ?

Voltage-Mode PWM Controller (1)



- Output Voltage Used for Generating PWM Signal
- Advantage : Simplicity
- Control-to-Output Transfer Function (Boost)

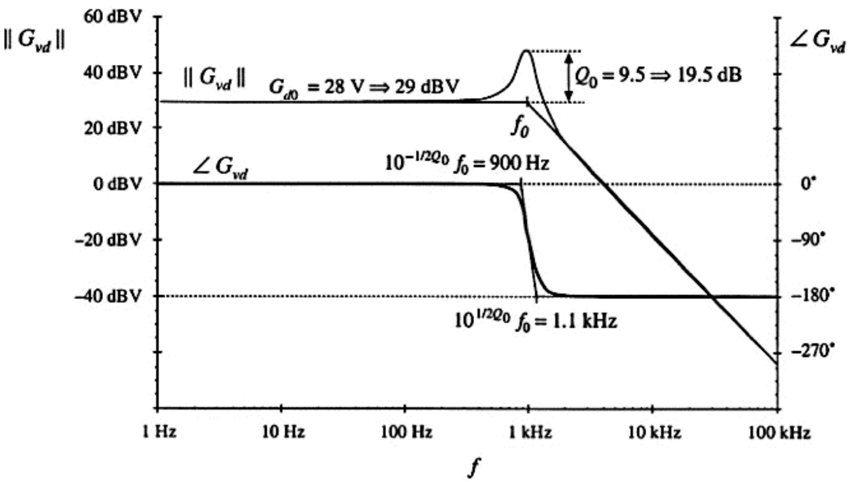
$$H_C(s) = \left(\frac{V_{OUT}}{1-D}\right) \frac{1 - \dfrac{L}{(1-D)^2 R} s}{1 + \dfrac{L}{(1-D)^2 R} s + \dfrac{(1-D)^2}{LC} s^2}$$

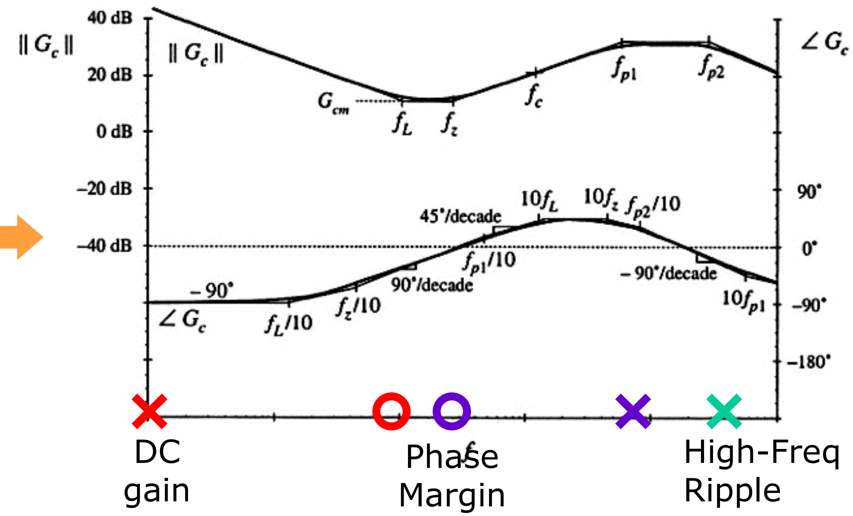
- Unstable When Used in Feedback

→ Elaborate Frequency Compensation Required

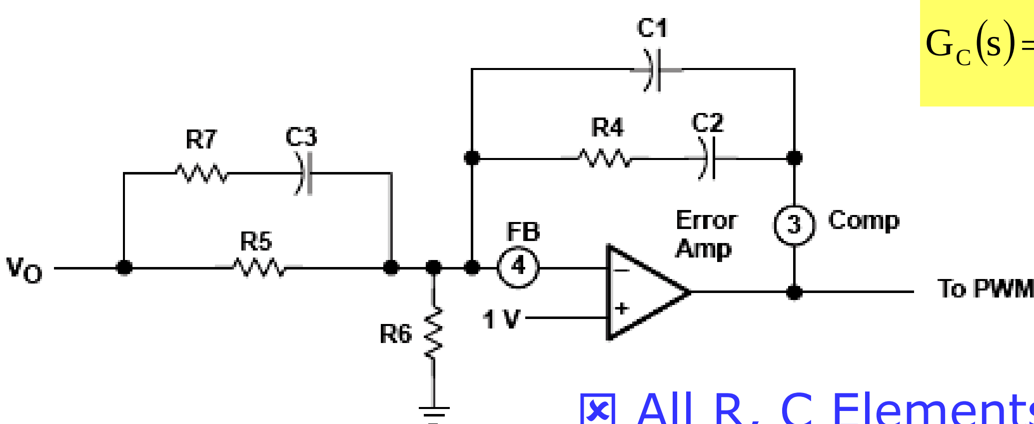
Voltage-Mode PWM Controller (2)

● PID Frequency Compensation



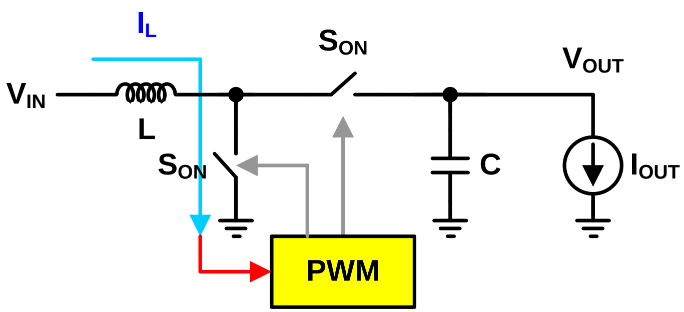


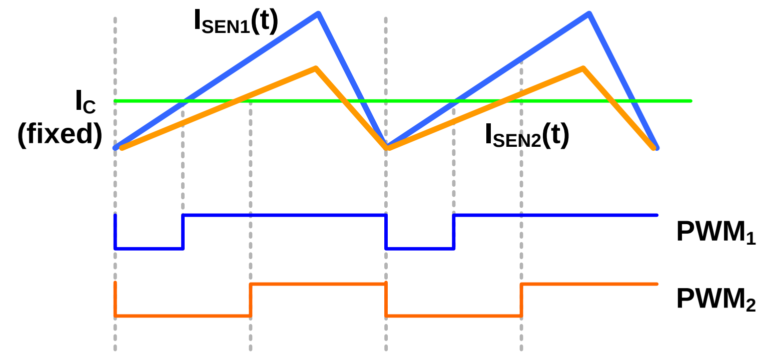
$$G_C(s) = G_{CM}\frac{(1+s/\omega_L)}{s}\frac{(1+s/\omega_z)}{(1+s/\omega_{p1})}\frac{1}{(1+s/\omega_{p2})}$$



⊠ All R, C Elements Off-Chip

Current-Mode PWM Controller (1)

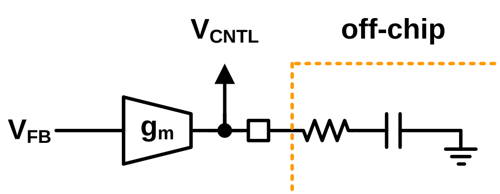




- Inductor Current Used for Generating PWM Signal
- Control-to-Output Transfer Function (Boost)

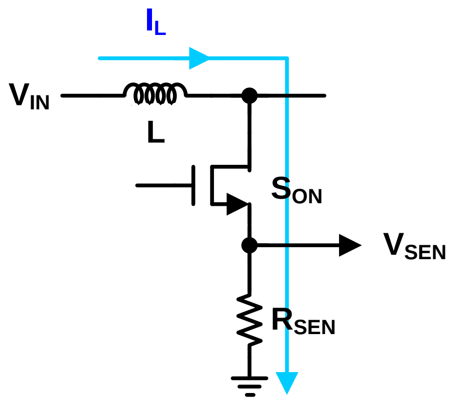
$$H_C(s) \approx \frac{(1-D)R}{2} \frac{1 - \frac{L}{(1-D)^2 R} s}{1 + \frac{RC}{2} s}$$

- **Simple Compensation ➔ Useful for Mobile Application**

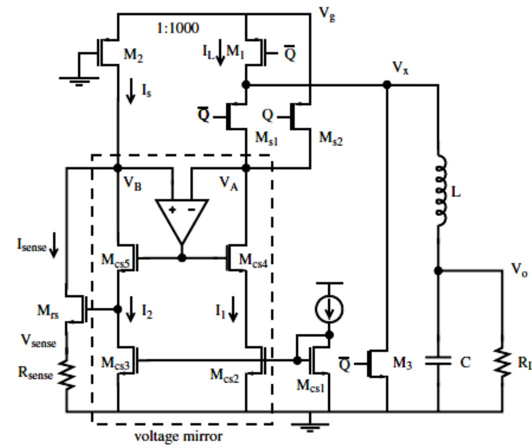


$$H_{COMP}(s) = g_m \frac{1 + sRC}{sC}$$

Current-Mode PWM Controller (2)

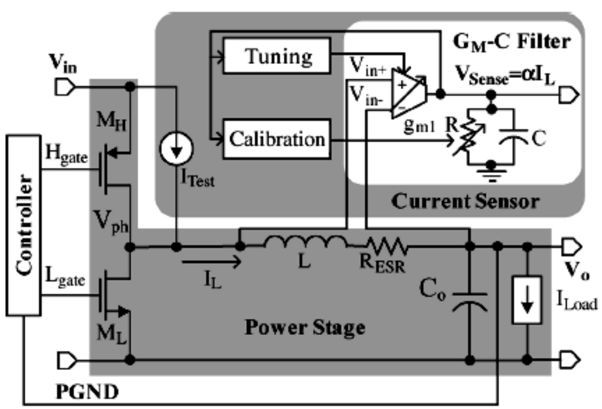


- Simple
- Degraded Efficiency
- Off-Chip Resistor



- Current-Mirroring
- On-Chip Current Sensing
- Mismatch Problem ?

📖 *IEEE JSSC*, 2004

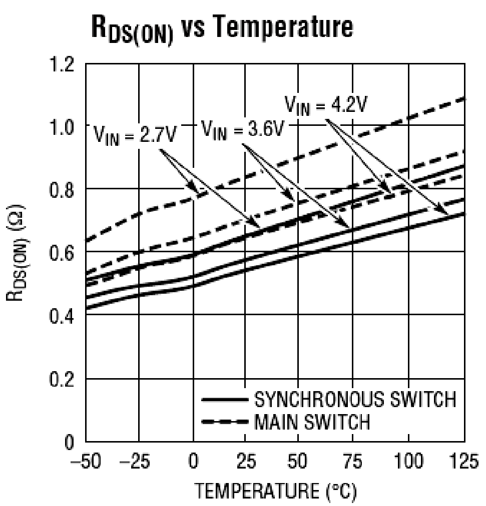


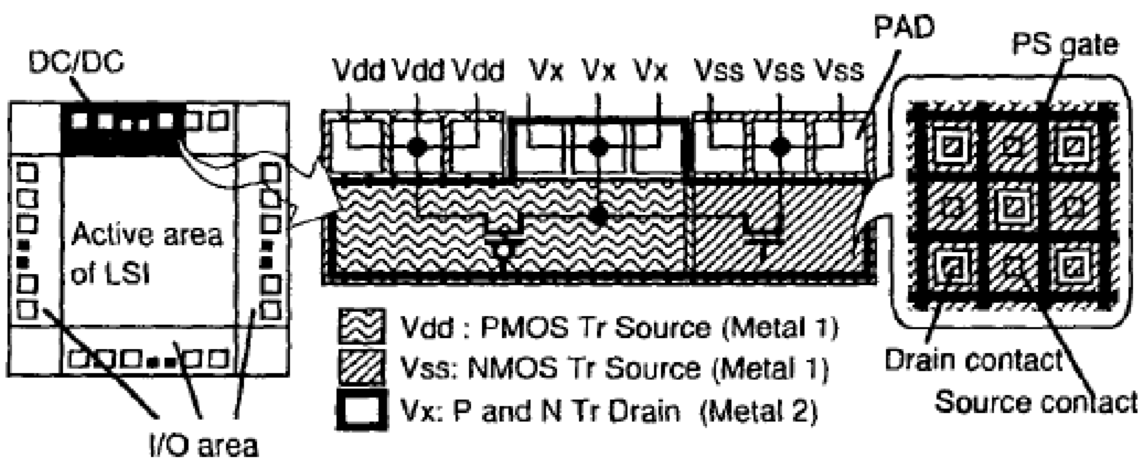
- Inductor Current Simulation
- On-Chip Current Sensing
- Tuning & Calibration ?

📖 *IEEE JSSC*, 2007

Integrated Power Switch Transistors

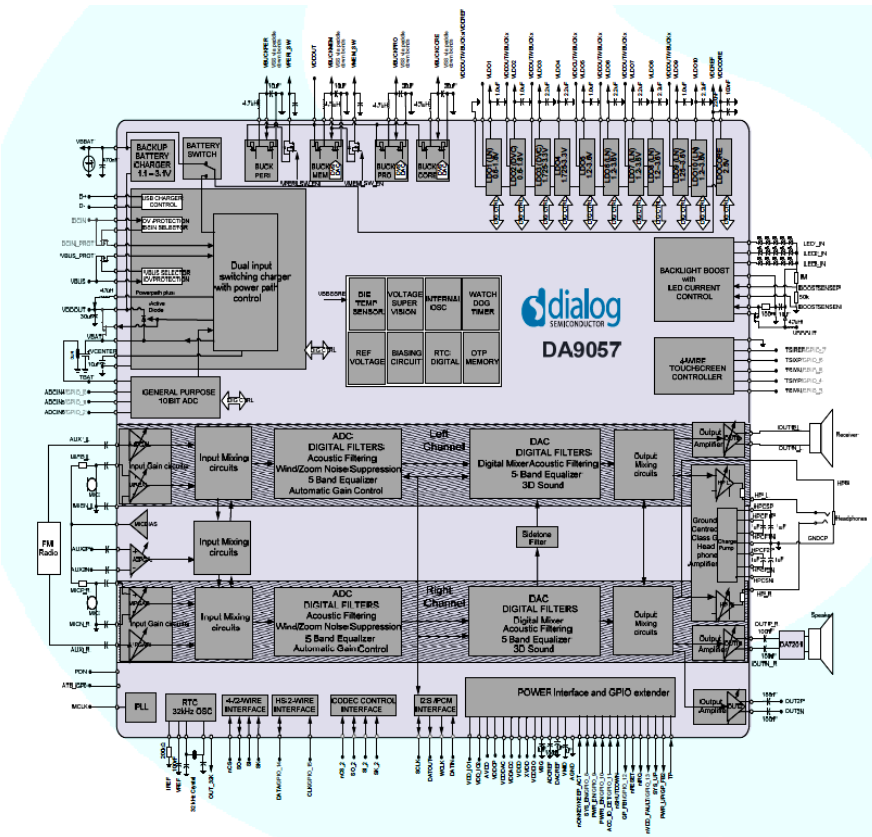
- Conduction Power Loss → P = I^2**R**
- If Possible, Synchronous Two Switches to be Integrated
- R_{ON} : Transistor ON Resistance
  - → Large Size : W>100,000μm for Several 10mΩ
  - → Preferred Structure : **High Width-to-Area Ratio**





PMIC + α

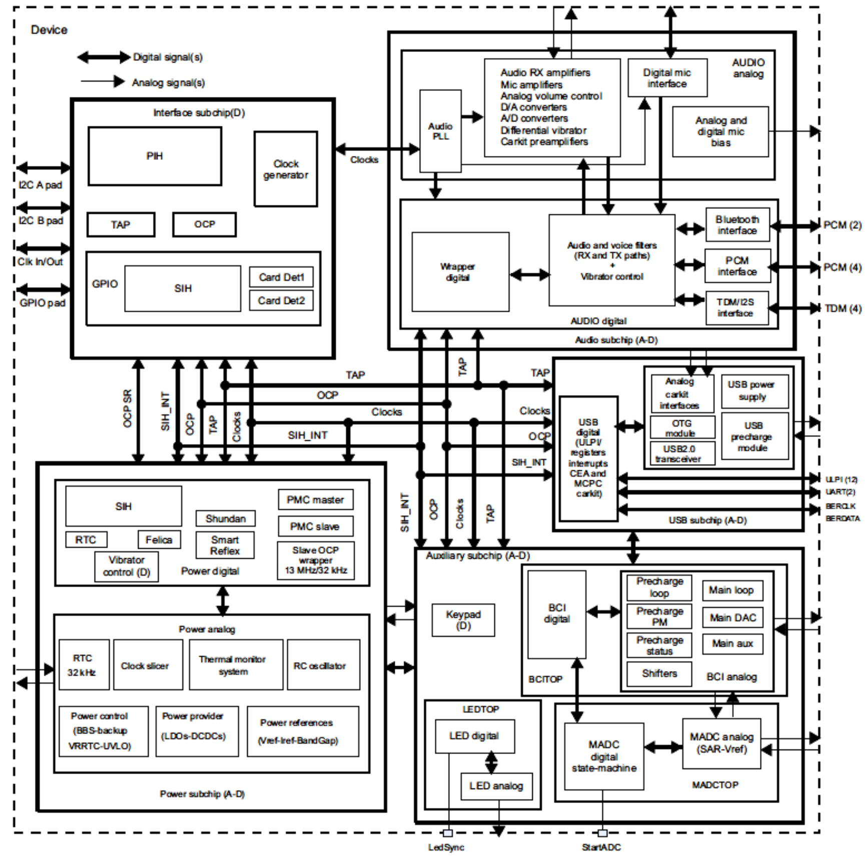
❐ DA9057



DA9057 Block Diagram

DC/USB Chrg, 4 Bucks, 10 LDOs, w-LED, 16-b Stereo CODEC, 5-band EQ

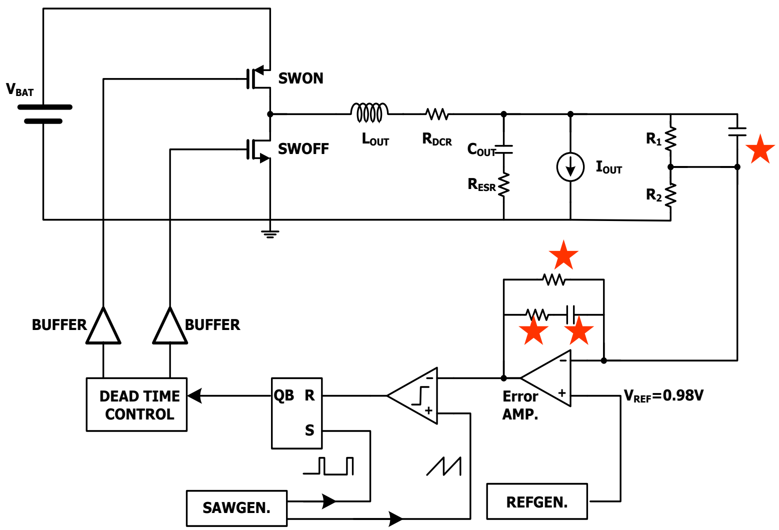
❐ TPS65950



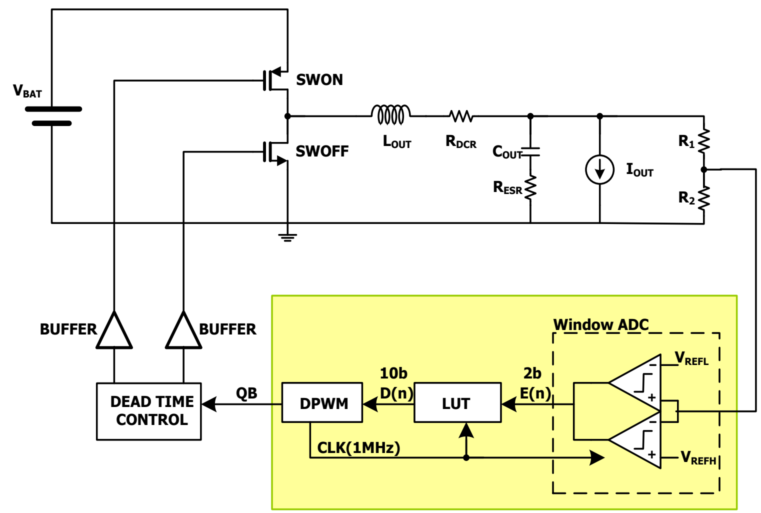
DC/USB Chrg, 3 Bucks, 10 LDOs, w-LED, Voice/Linear CODECs, 16-b ADC/DAC, Audio I/O, USB Tx/Rx

Digital PWM Controller Approach

Analog Control



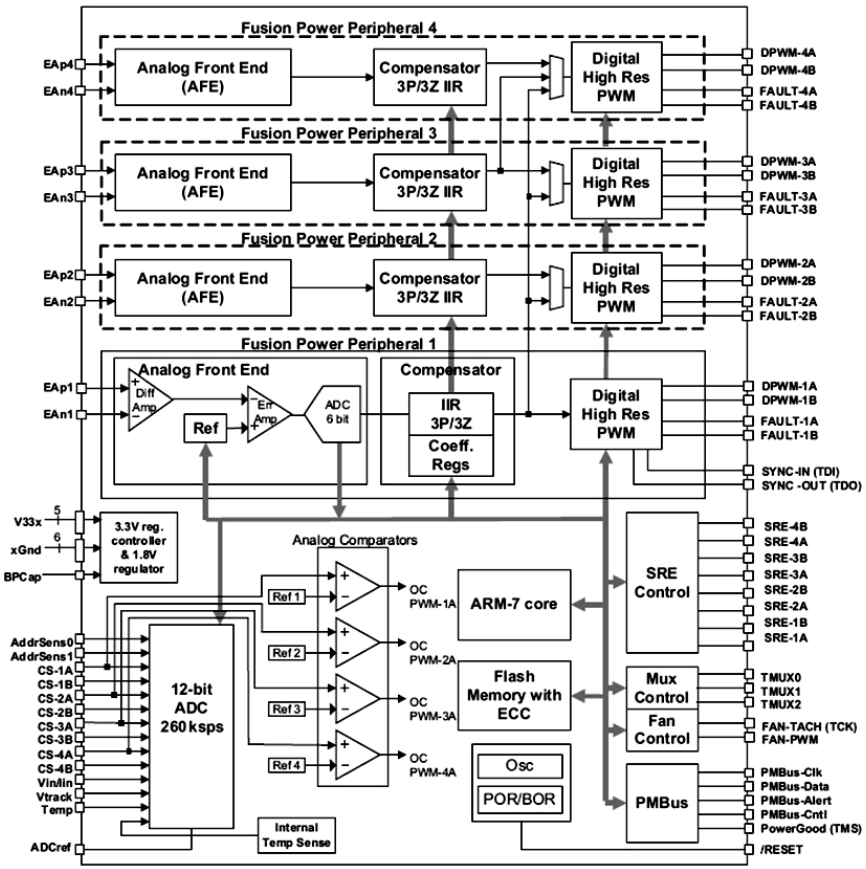
Digital Control



- Digital Controller to Simulate Analog Frequency Compensator
  ➔ External R & C Components to be Removed
- Hardware Minimization ➔ 2-bit ADC, Look-Up Table Approach
  Digital PWM w/ Error Feedback Loop
- Digital Versatility?

Digital PMIC Example

❒ UCD9240 of TI



- Digital Power Control/Management
- Digital Power Control
  - Reference Setting
  - Compensation Algorithm
  - DPWM Control
- DPWM w/ Various Operating Modes
- V/I/Temp Sensing w/ ADCs
- V/I/Temp Protection
- PMBus for External Interfacing

감 사 합 니 다.

Q & A