Innovus analysis command

setAnalysisMode

Sets global analysis modes for timing analysis. The software uses these modes for all timing analysis commands unless you specify specific modes in the reporting commands. The modes that you specify in the reporting commands override these modes.

-analysisType {single | bcwc | onChipVariation}

Sets the timing analysis type to single, best case worst case, or on-chip variation.

Default:

If you read in one library and do not specify any timing analysis type, the software uses single by default.

If you read in two libraries and do not specify any timing analysis type, the software uses bcwc by default.

single: Scales the delay values based on one operating condition.

bcwc: Checks the design for two extreme operating conditions.

The software uses the maximum delays for all paths during setup checks and

minimum delays for all paths during hold checks.

onChipVariation: Calculates the delay for one path based on maximum operating condition while calculating the delay for another path based on minimum operating condition for setup or hold checks.

-checkType {setup | hold}

Checks the design for setup or hold violations in the current analysis.

Default: setup

Note: When simultaneous setup/hold mode analysis is on, this parameter does not have any impact. You can use the report_timing -late/-early parameter to report setup/hold timing reports.

-cppr {none | both | setup | hold}

Removes pessimism from clock paths that have a portion of the clock network in common between the clock source and clock destination paths.

The pessimism is introduced when the timing analysis tools assume that the common path has different delay values for two different paths in case of on-chip variation. The pessimism can also be because of clock reconvergence in the clock network. The pessimism effects all analysis modes including single, best case-worst case (bcwc), and on-chip variation.

Default: none

Disables removal of clock reconvergence pessimism.

both:

Enables removal of clock reconvergence pessimism for both setup and hold modes.

Note:

When setAnalysisMode -cppr is specified (without any arguments), the value is set to both.

setup:

Enables removal of clock reconvergence pessimism in setup mode only.

hold:

Enables removal of clock reconvergence pessimism in hold mode only.

report_clock_timing

Generates a clock skew report for the current design. The software generates a separate report for each specified clock or pair of clocks. You specify the clocks using the -clock parameter, and clock pairs using the -from_clock and

-to_clock parameters. You can use the -nworst and -greater_than parameters with the -from_clock and -to_clock parameters to generate reports with skew to the specified sink pins. You can use the -early and -late parameters to specify the type of skew to be reported.

-rise | -fall

Specifies active transition at sequential devices clock pins. The -rise and -fall parameters are mutually exclusive and cannot be specified together.

Note: You can specify these parameters only with the -type latency parameter.

-launch | -capture

When specified with -type latency, generates a report of either the launch latency values (-launch), or the capture latency values (-capture).

Note: You can specify these parameters only with -type latency.

Default: -launch

-early

Uses hold skew to generate the report. Hold skew is the difference between minimum latency at the start point flip-flop and the maximum latency at the end point flip-flop.

Default: Uses the setup skew.

skew = MaxLatency@StartPointFF - MinLatency@EndPointFF

-late

Uses setup skew to generate the report. Setup skew is the difference between the maximum latency at the start point flip-flop and minimum latency at the end point flip-flop.

skew = MaxLatency@EndPointFF - MinLatency@StartPointFF

report_clock_timing -type skew

-from

coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/controller/clk_en_reg/DFF/CK

-to

coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/des/uk/K_r14_reg_50/DFF/CK

-late

Clock: my_clk

Analysis View: func_slow_max

Skew	Latency	Clock Pin
	1.748	r
		coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/controller/clk_en_reg/DFF/CK
0.145	1.603	r
		coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/des/uk/K_r14_reg_50/DFF/CK

setup_skew = maximum_latency@start_point_FF - minimum_latency@end_point_FF

report_clock_timing -type skew

-from

coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/controller/clk_en_reg/DFF/CK

```
    -to
        coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/des/uk/K_r14_reg_50/DFF/CK
    -early

Clock: my_clk
Analysis View: func_fast_min

          Skew         Latency              Clock Pin
-------------------------------------------------------------------------
                       0.691       r
    coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/controller/clk_en_reg/DFF/CK
         0.027         0.718       r
    coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/des/uk/K_r14_reg_50/DFF/CK
```

hold_skew = maximum_latency@end_point_FF - minimum_latency@start_point_FF

```
innovus #> report_clock_timing -type latency
    -to
        coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/controller/clk_en_reg/DFF/CK
    -early -launch
#####################################################################
#   Command:              report_clock_timing -type latency -to
coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/controller/clk_en_reg/DFF/CK -early -launch
#####################################################################

  Clock: my_clk
  Analysis View: func_fast_min

          ---Latency---
    Source          Network          Total          Clock Pin
-------------------------------------------------------------------------
       0.000          0.691          0.691          r
coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/controller/clk_en_reg/DFF/CK

innovus #> report_clock_timing -type latency
    -to
        coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/des/uk/K_r14_reg_50/DFF/CK
    -early -capture
#####################################################################
#   Command:              report_clock_timing -type latency -to
coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/des/uk/K_r14_reg_50/DFF/CK -early -capture
#####################################################################
```

Clock: my_clk
Analysis View: func_fast_min

---Latency---			
Source	Network	Total	Clock Pin
0.000	0.718	0.718	r

coreinst/ks_core1/periph1_PH/des_top1/des_top_inst/des/uk/K_r14_reg_50/DFF/CK

createBasicPathGroups
analyze_paths_by_basic_path_group
analyze_paths_by_bottleneck
analyze_paths_by_clock_domain
analyze_paths_by_critical_false_path
analyze_paths_by_drv
analyze_paths_by_hier_port
analyze_paths_by_hierarchy
analyze_paths_by_view