Innovus global and localSkew

1. GLOBAL SKEW with CTS built-in delay calculator (DC) and timing analyzer (TA)

report_ccopt_skew_groups -skew_group <SKEW_GROUP> -delay_corner <DC> -late

-late: setup check

-early: hold check

get_ccopt_skew_group_delay -to <DFF/CK> -skew_group <SKEW_GROUP> -check_type setup -delay_corner <DC> -delay_type late

get_ccopt_skew_group_delay -to <DFF/CK> -skew_group <SKEW_GROUP> -check_type setup -delay_corner <DC> -delay_type late

-delay_type late: slow path (i.e. launch path of setup check, capture path of hold check)

-delay_type early: fast path (i.e. capture path of setup check, launch path of hold check)

2. LOCAL SKEW with Common Timing Engine (CTE)

report_clock_timing -type skew -clock my_clk -view <ANALYSIS_VIEW> -late

report_timing -from <DFF_launch/CK> -to <DFF_capture/D> -clock my_clk -view <ANALYSIS_VIEW> -late -path_type full_clock -net

report_clock_timing -type latency -to <DFF_launch/CK> -clock my_clk -view <ANALYSIS_VIEW> -late -launch

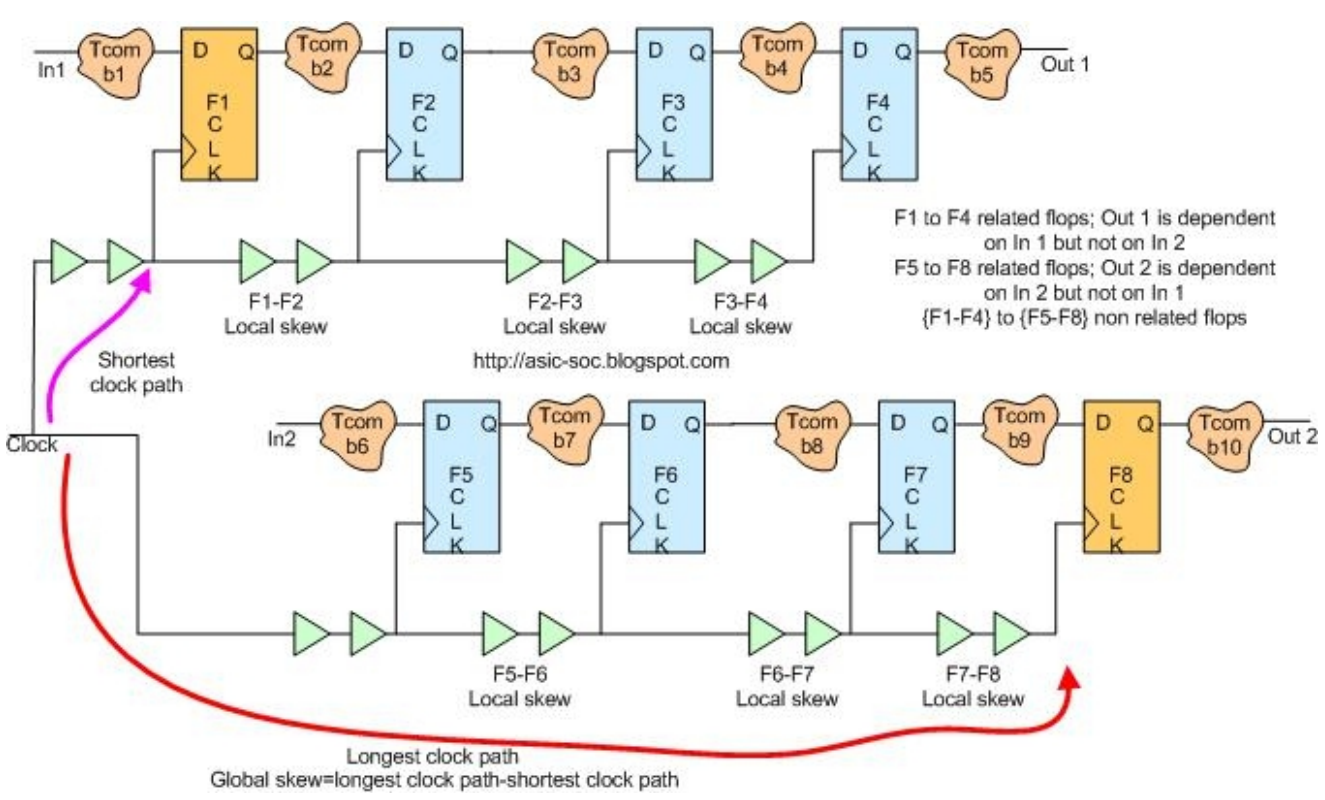
report_clock_timing -type latency -to <DFF_capture/CK> -clock my_clk -view <ANALYSIS_VIEW> -late -capture

-late: setup check

-early: hold check

-capture: latency as capture path

-launch: latency as launch path



Note:

Early & late does impact on caculated latency, skew, which DONT match some Troubleshooting Information(like, "Recommendation for reporting the clock latency and skew corresponding to the different CTS engines")

3 Example

3.1 global skew

$ report_ccopt_skew_groups -skew_group my_clk/functional_func_slow_max -delay_corner slow_max -late -summary

Clock tree timing engine global stage delay update for slow_max:setup.late...

Clock tree timing engine global stage delay update for slow_max:setup.late done. (took cpu=0:00:00.2 real=0:00:00.2)

Because one or several parameters among "-early|-late|-delay_corners" are provided to report_ccopt_skew_groups, the metric data may not be up to date in all delay corners.

Skew Group Structure:

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Skew Group	Sources	Constrained Sinks	Unconstrained Sinks
my_clk/functional_func_slow_max	1	11536	1

Skew Group Summary:

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Timing Corner	Skew Group	ID Target	Min ID	Max ID	Avg ID	Std.Dev. ID	Skew Target Type	Skew Target	Skew Skew window occupancy
slow_max:setup.late	my_clk/functional_func_slow_max	1.007	0.890	1.038	0.997	0.029	auto computed	-	0.148 -

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* - indicates that target was not met.

Skew Group Min/Max path pins:
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Timing Corner	Skew Group	Min ID	PathID	Max ID	PathID
slow_max:setup.late	my_clk/functional_func_slow_max	0.890	-	1.038	-

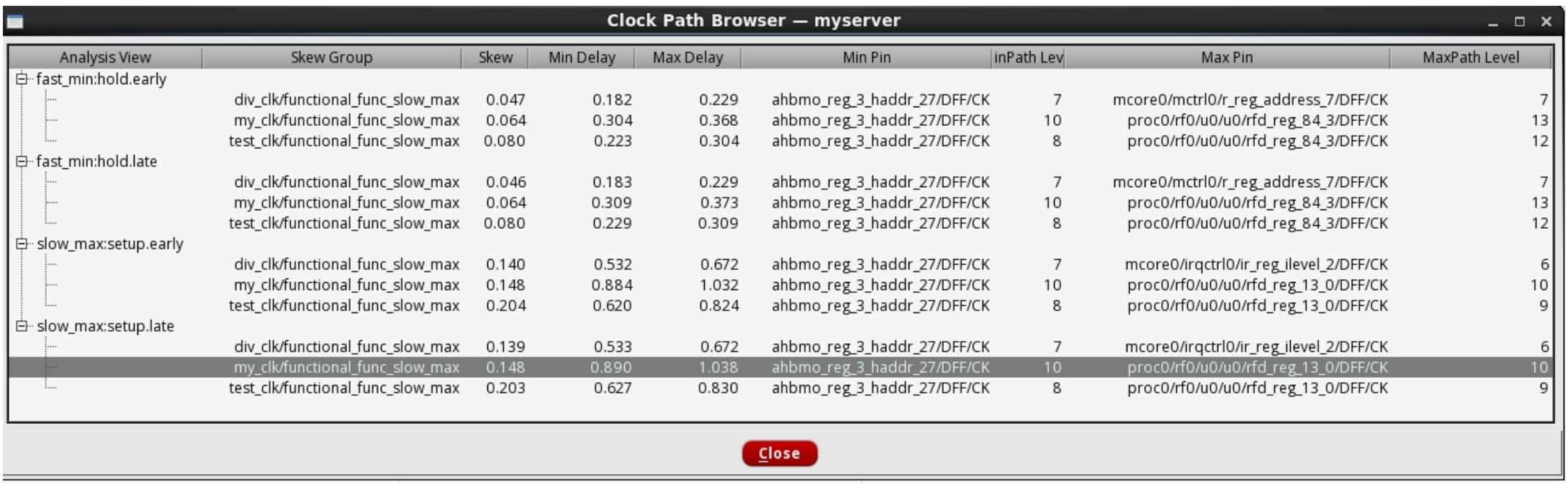
- min ahbmo_reg_3_haddr_27/DFF/CK
- max proc0/rf0/u0/u0/rfd_reg_13_1/DFF/CK

$ get_ccopt_skew_group_delay -to ahbmo_reg_3_haddr_27/DFF/CK -skew_group my_clk/functional_func_slow_max -check_type setup -delay_corner slow_max -delay_type late

0.89

$ get_ccopt_skew_group_delay -to proc0/rf0/u0/u0/rfd_reg_13_1/DFF/CK -skew_group my_clk/functional_func_slow_max -check_type setup -delay_corner slow_max -delay_type late

1.0376



Clock Tree debugger/Clock Path Browser may show different end point, though the skew is same, which is max, show as below:

proc0/rf0/u0/u0/rfd_reg_16_30/DFF/CK my_clk/functional_func_slow_max 1.0374
proc0/rf0/u0/u0/rfd_reg_1_29/DFF/CK my_clk/functional_func_slow_max 1.0375
proc0/rf0/u0/u0/rfd_reg_13_30/DFF/CK my_clk/functional_func_slow_max 1.0375
proc0/rf0/u0/u0/rfd_reg_14_30/DFF/CK my_clk/functional_func_slow_max 1.0375
proc0/rf0/u0/u0/rfd_reg_13_0/DFF/CK my_clk/functional_func_slow_max 1.0376
proc0/rf0/u0/u0/rfd_reg_13_1/DFF/CK my_clk/functional_func_slow_max 1.0376

$ get_ccopt_skew_group_delay -to proc0/rf0/u0/u0/rfd_reg_13_0/DFF/CK -skew_group my_clk/functional_func_slow_max -check_type setup -delay_corner slow_max -delay_type late
1.0376

3.2 local skew

$ report_clock_timing -type skew -clock my_clk -view func_slow_max -late

```
#####################################################################
#    Generated by:          Cadence Innovus 20.14-s095_1
#    OS:                    Linux x86_64(Host ID myserver)
#    Generated on:          Mon May    3 16:18:32 2021
#    Design:                leon
#    Command:                 report_clock_timing -type skew -clock my_clk -view func_slow_max -late
#####################################################################
```

Clock: my_clk
Analysis View: func_slow_max

Skew	Latency	CPPR		Clock Pin
	1.0523		r	proc0/c0/dcache0/r_reg_wb_data1_0/DFF/CK
0.1277	0.8980	-0.0266	r	mcore0/a0/r_reg_cctrl_ics_0/DFF/C

$ report_clock_timing -type latency -to proc0/c0/dcache0/r_reg_wb_data1_0/DFF/CK -clock my_clk -view func_slow_max -late -launch

```
#################################################################
#   Generated by:         Cadence Innovus 20.14-s095_1
#   OS:                   Linux x86_64(Host ID myserver)
#   Generated on:         Mon May   3 16:19:05 2021
#   Design:               leon
#   Command:              report_clock_timing -type latency -to proc0/c0/dcache0/r_reg_wb_data1_0/DFF/CK -clock my_clk -view func_slow_max -late -launch
#################################################################
```

Clock: my_clk
Analysis View: func_slow_max

---Latency---				
Source	Network	Total		Clock Pin
0.0000	1.0523	1.0523	r	proc0/c0/dcache0/r_reg_wb_data1_0/DFF/CK

$ report_clock_timing -type latency -to mcore0/a0/r_reg_cctrl_ics_0/DFF/CK -clock my_clk -view func_slow_max -late -capture

```
#################################################################
#   Generated by:         Cadence Innovus 20.14-s095_1
#   OS:                   Linux x86_64(Host ID myserver)
#   Generated on:         Mon May   3 16:19:31 2021
#   Design:               leon
#   Command:              report_clock_timing -type latency -to mcore0/a0/r_reg_cctrl_ics_0/DFF/CK -clock my_clk -view func_slow_max -late -capture
#################################################################
```

Clock: my_clk
Analysis View: func_slow_max

---Latency---				
Source	Network	Total		Clock Pin
0.0000	0.8980	0.8980	r	mcore0/a0/r_reg_cctrl_ics_0/DFF/CK

$ report_timing -from proc0/c0/dcache0/r_reg_wb_data1_0/DFF/CK -to mcore0/a0/r_reg_cctrl_ics_0/DFF/D -clock my_clk -view

```
#################################################################
#   Generated by:         Cadence Innovus 20.14-s095_1
#   OS:                   Linux x86_64(Host ID myserver)
#   Generated on:         Mon May   3 16:20:50 2021
#   Design:               leon
#   Command:              report_timing -from proc0/c0/dcache0/r_reg_wb_data1_0/DFF/CK -to mcore0/a0/r_reg_cctrl_ics_0/DFF/D -clock my_clk -view func_slow_max
-late -path_type full_clock -net > rpt
#################################################################
Path 1: MET Setup Check with Pin mcore0/a0/r_reg_cctrl_ics_0/DFF/CK
Endpoint:    mcore0/a0/r_reg_cctrl_ics_0/DFF/D          (^) checked with   leading
edge of 'my_clk'
Beginpoint: proc0/c0/dcache0/r_reg_wb_data1_0/DFF/Q (^) triggered by   leading
edge of 'my_clk'
Path Groups: {my_clk}
Analysis View: func_slow_max
Other End Arrival Time          0.8980
- Setup                         0.2120
+ Phase Shift                   4.0000
+ CPPR Adjustment               0.0266
= Required Time                 4.7126
- Arrival Time                  2.6459
```

= Slack Time 2.0667

Clock Rise Edge 0.0000

+ Drive Adjustment 0.0215

= Beginpoint Arrival Time 0.0215

Timing Path:

Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk		0.0215	2.0882	
CGIC_INST/CK	^	clk	TLATNTSCAX6	0.0060	0.0275	2.0942
CGIC_INST/ECK	^	clk_gate	TLATNTSCAX6	0.2109	0.2384	2.3051
clk_out_mux/A	^	clk_gate	MX2X4	0.0000	0.2384	2.3051
clk_out_mux/Y	^	clk2x	MX2X4	0.1862	0.4246	2.4913
clk2x__L1_I0/A	^	clk2x	CLKINVX12	0.0004	0.4250	2.4917
clk2x__L1_I0/Y	v	clk2x__L1_N0	CLKINVX12	0.0589	0.4839	2.5506
clk2x__L2_I3/A	v	clk2x__L1_N0	CLKBUFX12	0.0009	0.4848	2.5515
clk2x__L2_I3/Y	v	clk2x__L2_N3	CLKBUFX12	0.0805	0.5653	2.6320
clk2x__L3_I0/A	v	clk2x__L2_N3	CLKBUFX12	0.0008	0.5661	2.6328
clk2x__L3_I0/Y	v	clk2x__L3_N0	CLKBUFX12	0.0956	0.6617	2.7284
clk2x__L4_I0/A	v	clk2x__L3_N0	CLKINVX12	0.0028	0.6645	2.7312
clk2x__L4_I0/Y	^	clk2x__L4_N0	CLKINVX12	0.0536	0.7181	2.7848
proc0/c0/dcache0/RC_CG_HIER_INST24/RC_CGIC_INST/CK	^	clk2x__L4_N0	TLATNTSCAX6	0.0009	0.7190	2.7857
proc0/c0/dcache0/RC_CG_HIER_INST24/RC_CGIC_INST/EC	^	proc0/c0/dcache0/rc_gclk_978	TLATNTSCAX6	0.2335	0.9525	3.0192
K						
proc0/c0/dcache0/rc_gclk_978__L1_I0/A	^	proc0/c0/dcache0/rc_gclk_978	CLKINVX12	0.0004	0.9529	3.0196
proc0/c0/dcache0/rc_gclk_978__L1_I0/Y	v	proc0/c0/dcache0/rc_gclk_978__L1_N0	CLKINVX12	0.0473	1.0002	3.0669
proc0/c0/dcache0/rc_gclk_978__L2_I1/A	v	proc0/c0/dcache0/rc_gclk_978__L1_N0	CLKINVX12	0.0009	1.0011	3.0678
proc0/c0/dcache0/rc_gclk_978__L2_I1/Y	^	proc0/c0/dcache0/rc_gclk_978__L2_N1	CLKINVX12	0.0496	1.0507	3.1174
proc0/c0/dcache0/r_reg_wb_data1_0/DFF/CK ->	^	proc0/c0/dcache0/rc_gclk_978__L2_N1	SDFFQX1	0.0016	**1.0523**	3.1190
proc0/c0/dcache0/r_reg_wb_data1_0/DFF/Q	^	mcdi_12	SDFFQX1	0.4061	1.4584	3.5251
mcore0/ahb0/g3784/A0	^	mcdi_12	AO22X2	0.0012	1.4596	3.5263
mcore0/ahb0/g3784/Y	^	ahbsi_4_hwdata[0]	AO22X2	0.4259	1.8855	3.9522
mcore0/apb0/g1865/B	^	ahbsi_4_hwdata[0]	AND2X2	0.0017	1.8872	3.9539
mcore0/apb0/g1865/Y	^	mcore0/apbi_0_0	AND2X2	0.4503	2.3375	4.4042
mcore0/a0/g1052/A0	^	mcore0/apbi_0_0	AO22XL	0.0002	2.3377	4.4044
mcore0/a0/g1052/Y	^	mcore0/a0/n_39	AO22XL	0.3082	2.6459	4.7126
mcore0/a0/r_reg_cctrl_ics_0/DFF/D ->	^	mcore0/a0/n_39	SDFFQX1	0.0000	2.6459	4.7126

Clock Rise Edge 0.0000

= Beginpoint Arrival Time 0.0000

Other End Path:

Pin	Edge	Net	Cell	Delay	Arrival Time	Required Time
clk	^	clk		0.0000		-2.0667
CGIC_INST/CK	^	clk	TLATNTSCAX6	0.0051	0.0051	-2.0616
CGIC_INST/ECK	^	clk_gate	TLATNTSCAX6	0.2067	0.2118	-1.8549
clk_out_mux/A	^	clk_gate	MX2X4	0.0000	0.2118	-1.8549
clk_out_mux/Y	^	clk2x	MX2X4	0.1862	0.3980	-1.6687
clk2x__L1_I0/A	^	clk2x	CLKINVX12	0.0002	0.3982	-1.6685
clk2x__L1_I0/Y	v	clk2x__L1_N0	CLKINVX12	0.0586	0.4568	-1.6099
clk2x__L2_I3/A	v	clk2x__L1_N0	CLKBUFX12	0.0009	0.4577	-1.6090
clk2x__L2_I3/Y	v	clk2x__L2_N3	CLKBUFX12	0.0805	0.5382	-1.5285
clk2x__L3_I0/A	v	clk2x__L2_N3	CLKBUFX12	0.0004	0.5386	-1.5281
clk2x__L3_I0/Y	v	clk2x__L3_N0	CLKBUFX12	0.0956	0.6342	-1.4325
clk2x__L4_I2/A	v	clk2x__L3_N0	CLKINVX12	0.0031	0.6373	-1.4294
clk2x__L4_I2/Y	^	clk2x__L4_N2	CLKINVX12	0.0637	0.7010	-1.3657
clk2x__L5_I3/A	^	clk2x__L4_N2	CLKINVX12	0.0019	0.7029	-1.3638
clk2x__L5_I3/Y	v	clk2x__L5_N3	CLKINVX12	0.0737	0.7766	-1.2901
clk2x__L6_I6/A	v	clk2x__L5_N3	CLKINVX12	0.0030	0.7796	-1.2871
clk2x__L6_I6/Y	^	clk2x__L6_N6	CLKINVX12	0.0548	0.8344	-1.2323
clk2x__L7_I13/A	^	clk2x__L6_N6	CLKINVX12	0.0016	0.8360	-1.2307
clk2x__L7_I13/Y	v	clk2x__L7_N13	CLKINVX12	0.0329	0.8689	-1.1978

clk2x__L8_I13/A	v	clk2x__L7_N13	CLKINVX12	0.0001	0.8690	-1.1977
clk2x__L8_I13/Y	^	clk2x__L8_N13	CLKINVX12	0.0285	0.8975	-1.1692
mcore0/a0/r_reg_cctrl_ics_0/DFF/CK	^	clk2x__L8_N13	SDFFQX1	0.0005	**0.8980**	-1.1687

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