University of Victoria

XILINX®

ALTERA®

FPGA Overview

LATTICE SEMICONDUCTOR™

achronix SEMICONDUCTOR CORPORATION

Microsemi (Actel®)

ATMEL

QuickLogic

Objectives

The Objective of this presentation is to:

- Introduce some Coarse-Grained FPGAs, such as Xilinx 7 series, and Altera 10/V Series, and showing comparison between different FPGAs in terms of:
  - Number of Logic Cells/Elements
  - Number of Slices/Adaptive Logic Modules (ALMs)
  - Number of Registers/Flip-flops
  - Number of Memory Blocks
  - Number of dedicated DSPs, including Multipliers/Accumulators
- Show a view of the internal Slice/ALM and DSP block of some FPGAs

Xilinx 7 Series FPGA Families

Maximum Capabilities	**Artix7** (Lowest Power and Cost)	**Kintex7** (Industry's Best Price/Performance)	**Virtex7** (Industry's Highest System Performance)
Logic Cells (k)	16 – 215	65 – 477	326 – 2,000
Slices (4 6-input LUT, 8 Flip-Flop)	2,600 - 33,650 (22,100 L + 11,550 M)	10,250 - 74,650 (47,500 L + 27,150 M)	91,050 - 136,900 (83,750 L + 53,150 M)
Registers FF(x8)	20,800 - 269,200 200 - 1,444 kb Shift-Reg	82,000 - 597,200 419 - 3,394 kb Shift-Reg	728,400 - 1,095,200 3,469 - 6,638 kb Shift-Reg
LUTs (#Slices x4)	10,400 - 134,600	41,000 - 298,600	364,200 - 547,600
Memory Blocks (M18k, 36, Max)	900 - 13,140	4,860 - 34,380	28,620 - 50,760
DSP Slices (One 25 x 18 mul, One 48-bit accumulator, One Pre-adder)	45 – 740	240 – 1,920	700 – 3,600

Altera 10/V FPGA Families

Maximum Capabilities	***Max 10*** **Low-Cost FPGAs**	***Cyclone V*** **Low-Cost FPGAs**	***Arria 10*** **Midrange FPGAs**	***Stratix V*** **High-End FPGAs**
Logic Elements (k)	4 - 100	25 - 301	160 – 660	236 - 952
ALM (4 6-input LUT, 8 Flip-Flop) / LE (m10)	2,000 - 50,000 Each LE: 1 4-input LUT, and 1 Register	9,434 - 113,560	61,510 - 250,540	234,720 - 359,200
Registers FF (k) (x8)	2 - 50	37- 454	246 - 1,002	356 - 1,437
LUTs (x4) (k)	2 - 50	9 - 113	61 - 250	234 - 359
Memory Blocks (M18k, 36, Max)	10 - 182 (M9k)	135 - 1220 (M10k)	440 - 1,713 (M20k)	957 - 2,660 (M20k)
DSP Slices (2 Multipliers Each)	-	25 - 342	156 - 1,678	3,926 (18x18) or 1,963 (27x27) Mul

Xilinx vs Altera

Maximum Capabilities	**Xilinx**	**Altera**
Logic Cells/Elements	16,000 – 2,000,000	2,000 - 952,000
Slices/ ALM	2,600 - 136,900 **Four 6-input LUT, 8 FlipFlop**	2 - 359,200 **8-input LUT, 2 FA, 4 Mux, 4 Reg**
Registers FF	20,800 - 1,095,200	2,000 - 1,437,000 200 - 6,638 kb Shift-Reg
LUTs	10,400 - 547,600	2,000 - 359,200
Memory Blocks	900 - 13,140 **(M18k, 36, Max)**	10 (**M9k**) - 2,660(**M20k**)
DSP Slices	45 – 3,600 **(One 25 x 18 mul, One 48-bit accumulator, One Pre-adder)**	16 - 3,356 **(Two Multipliers)**

Other 5 FPGA Vendors

Maximum Capabilities	Xilinx	Altera	Microsemi IGLOO2	Lattice iCE40 Ultra	Atmel AT40K	Achronix Speedster 22i	QuickLogic PolarPro® II
Logic Cells (k)	16 – 2,000	2 - 952	6 - 146	1.1 - 3.5	5 - 50	660 - 1,725	150
Slices/ ALM/PLM	2,600 - 136,900	2,000 - 359,200	6,000 - 146,000	138 - 440 (8 LUTs + 8 FFs + Carry)	256 - 2,304	-	864
Registers/ FF	20,800 - 1,095,200	2,000 - 1,437,000	6 - 146	1,100 - 3,520	496 - 3,048	-	864
LUTs	10,400 - 547,600	2,000 - 359,200	6 - 146	1,100 - 3,520	512 - 4,608 (2 8-LUT/Cell)	400,000 - 1,100,000	-
Memory Blocks	900 - 50,760	**10** (M9k) - **2,660** (M20k)	**21 - 476** (18kb, 1kb)	16 - 20	-	4,920 - 12,096	8
DSP Slices	45 – 3,600	8 - 1,678	11 - 240	2 - 4 (MULT16, 32-bit Acc)	-	-	-

Xilinx Architecture Alignment

Logic Fabric
LUT-6 CLB

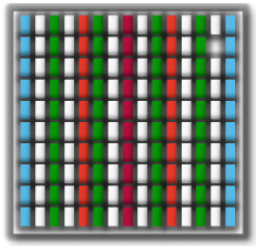
On-Chip Memory
36Kbit/18Kbit Block RAM

DSP Engines
DSP48E1 Slices

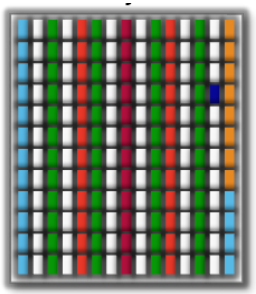
Precise, Low Jitter Clocking
MMCMs

Enhanced Connectivity
PCIe® Interface Blocks

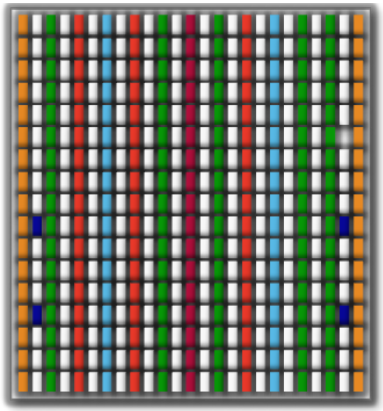
Hi-performance Serial I//O Connectivity
Transceiver Technology



Artix™-7 FPGA



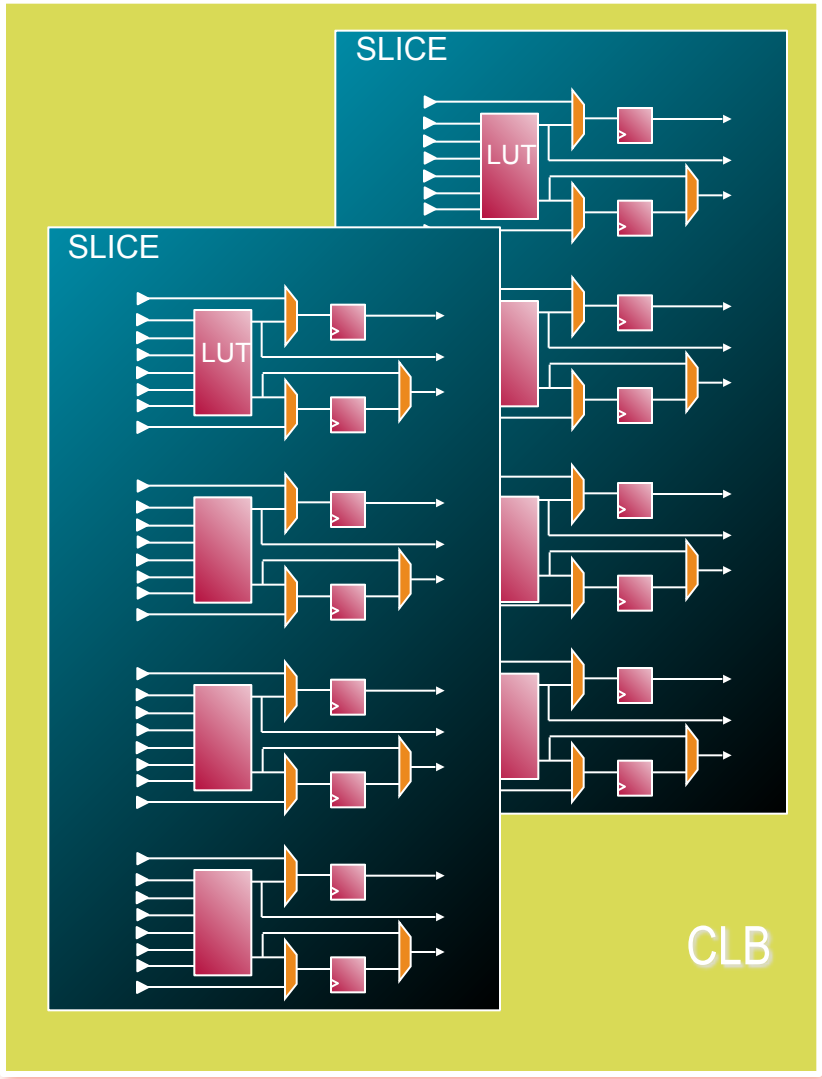
Kintex™-7 FPGA



Virtex®-7 FPGA

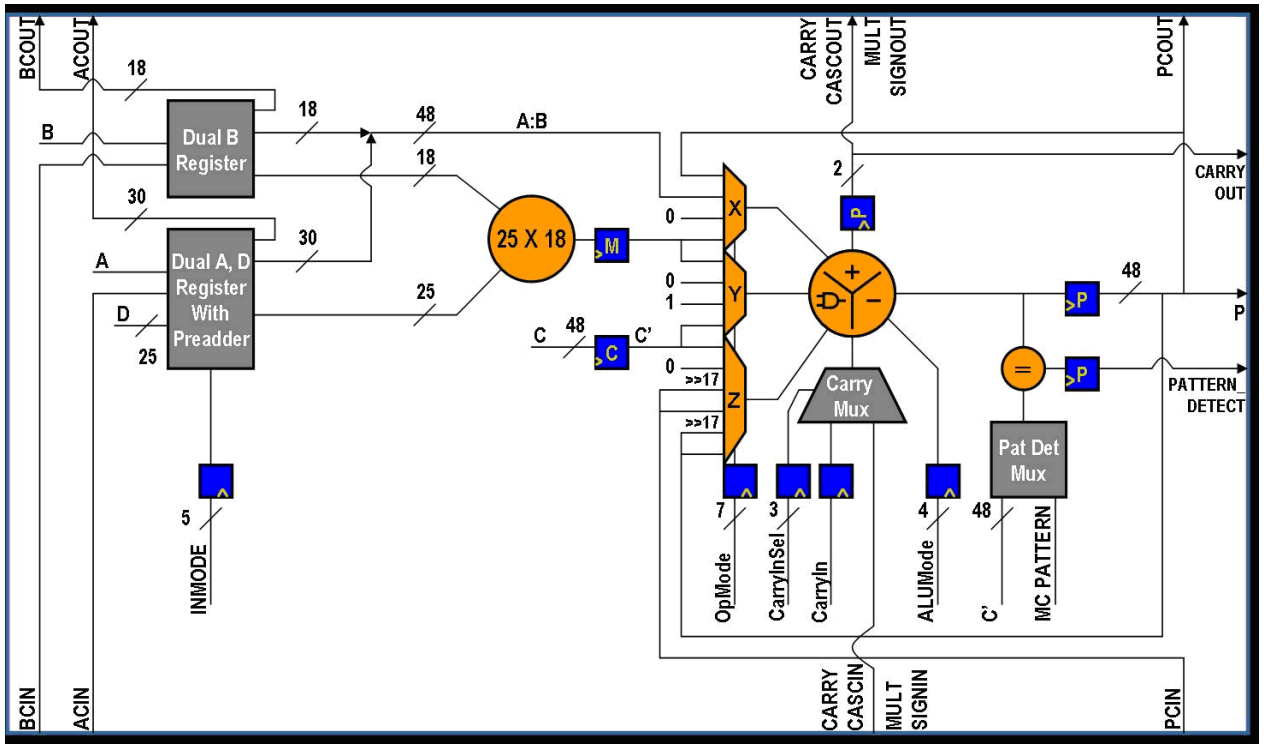
Xilinx CLB Structure

- Two side-by-side slices per CLB
  - Slice_M is memory-capable
  - Slice_L is logic and carry only
- Four 6-input LUTs per slice
  - Single LUT in Slice_M can be a 32-bit shift register or 64 x 1 RAM
- Two flip-flops per LUT
  - Excellent for heavily pipelined designs



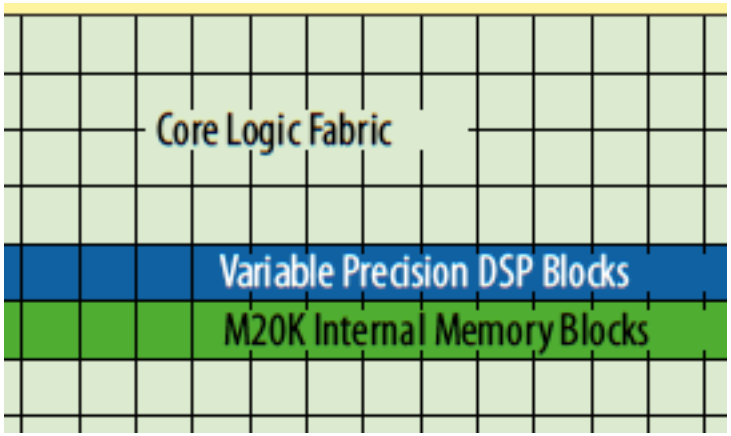
DSP Slice - Xilinx

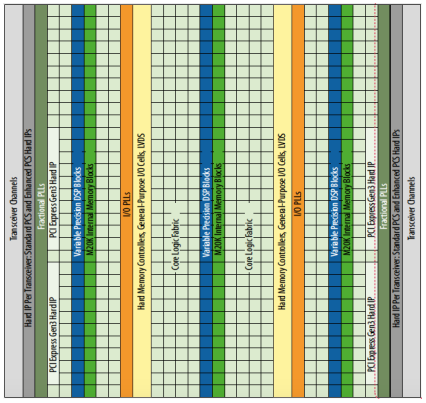
- All 7 series FPGAs share the same DSP slice
  - 25x18 multiplier
  - 25-bit pre-adder
  - Carry in and out
  - 96-bit MACC
  - 48-bit ALU
  - Pattern detect
  - 17-bit shifter



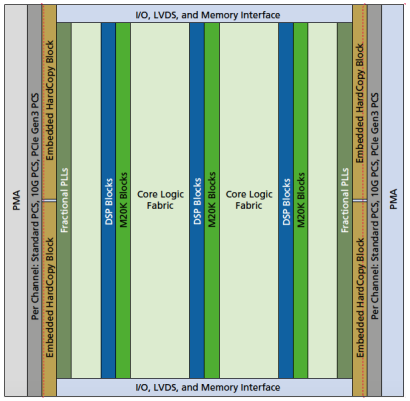
Altera - Architecture Alignment

- Arria 10 and Stratix V:





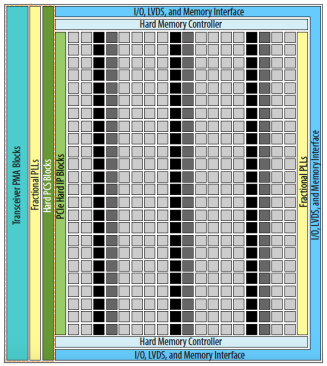
Arria 10 FPGA



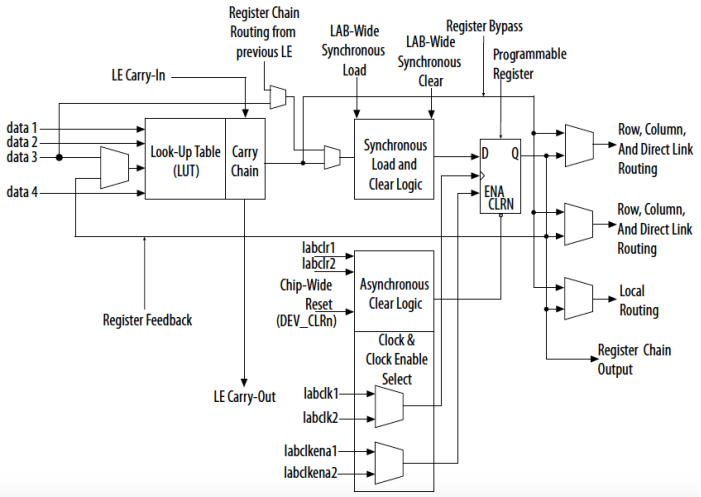
Stratix V FPGA

- Cyclone V:

Core Logic Fabric and MLABs
M10K Internal Memory Blocks
Variable-Precision DSP Blocks



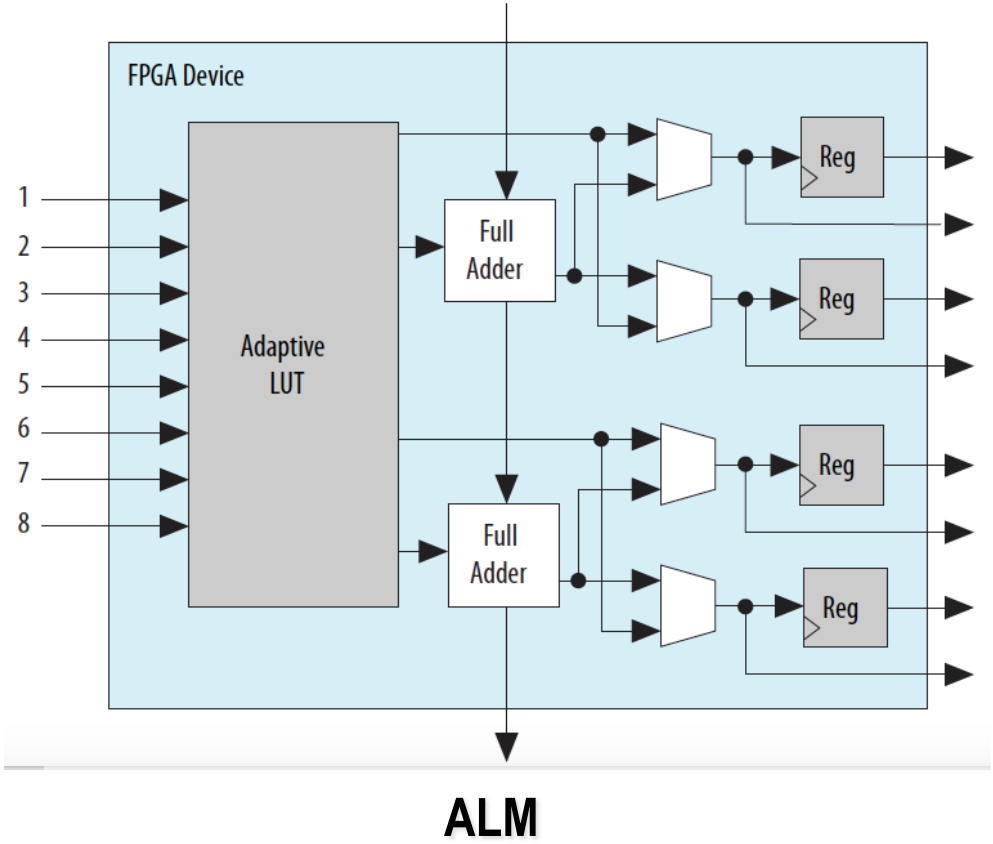
Cyclone V FPGA



Max 10 (FPGA) LE

ALM Structure

- Altera devices use Adaptive Logic Modules (ALM) as the basic building block of the logic fabric.
- The ALM, uses:
  - 8-input look-up table (LUT)
  - 4 dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



ALM

Summary

In this presentation:

- Some Coarse-Grained FPGAs were introduced, such as Xilinx 7 series, and Altera 10/V Series, in addition to the comparison between different FPGAs in terms of:
  - Number of Logic Cells/Elements
  - Number of Slices/Adaptive Logic Modules (ALMs)
  - Number of Registers/Flip-flops
  - Number of Memory Blocks
  - Number of dedicated DSPs, including Multipliers/Accumulators
- The internal Slice/ALM and DSP blocks of the some FPGAs were presented

References

- Arco Xilinx Training: https://arco.esi.uclm.es/public/doc/tutoriales/Xilinx%20Training/
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