EE 4142/ EE5190 LABORATORY - DIGITAL SYSTEMS DESIGN II Spring 2021:
February 7-8 Lab Sessions
Lab #2. – Hexadecimal Full Adder

Objective

The purpose of this lab is to **review** and become familiar with the **design** and **testing** of combinational circuits using modular design (block symbols) in a computer-aided design tool. The circuit is to be designed and simulated in **XilinxVivado environment**.

Prelab (30%) *Due at BEGINNING OF LAB

Using **solely two-input** AND gates and OR gates, implement a **Hexadecimal Adder** in a **modular** manner.

- First, create a **binary Full-adder** module:
  - Write down the binary full adder **truth table**
  - Demonstrate you know how to use **K-Maps** to derive the SOP Boolean equations for Sum and Cout.
  - Implement the obtained equations using **ONLY 2-input** AND and OR gates. Show the resulting **circuit**.
- Now, create the Hexadecimal adder
  - Using a **block diagram** representation of your full adder (corresponding to step 1 above) show how to connect enough instances of it to **create a Hexadecimal adder** (Circuit that is able to add **one hexadecimal digit to another hexadecimal digit**). Show the resulting **circuit**

* Bring a digital copy of your solution to your lab session

In lab session (50%) –

(1) Implement your design in Xilinx
(2) Simulate your design and demonstrate proper behavior of your simulated

waveforms to the TA
(3) Remember to obtain screen images along the way to include in your report

(Schematics, Testbench, Simulation waveform)

Report (20%) *Due Friday Feb 11th by 11:59PM

Create the lab report.