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**EE5190 – Digital Systems Design II**

**Graduate School Spring 2022**

**Lab #1. XOR implementation with NAND gates**

**Objective**

The purpose of this lab is to continue to become familiar with the implementation, testing and verification of simple circuits using a computer-aided design tool. In addition, you will learn how to create a schematic symbol and use instances of it to implement your design.

Using **solely two-input NAND gates**, implement a two-input XOR function in a **modular** manner.

**Procedure**

First, create an inverter using NAND gate this is done by using a two input NAND and using logic operators and while loop that outputs a 1 if all inputs are 0, and outputs a 0 if any given input is a 1 to include a 11 input.

Then, create AND and OR gates using only NAND gates and the inverter module that was previously created.

The AND gate was implemented by setting the ANDs input into the NAND gate by instantiating a NAND and then using a wire to store the output and pass it into the NAND-inverter that will out put the correct waveform for an AND gate.

The OR gate was implemented by instantiating the NAND-inverter and passing the inputs for the OR to the module and using a wire to store the output, the same step is repeated with a second NAND-inverter and the wires are passed to NAND gate and the output will create the OR waveform.

Finally, using the AND, OR and the inverter modules created above, implement the XOR function in the form of sum-of-products. Note: You should not use De Morgan’s theorem by simply converting AND-OR network to NAND-NAND network.

This was create by instantiating an NAND-inverter and using a wire to store the output, and this step is repeated again and then a NAND gate is instantiated and the wires from the NAND-inverters are used as the input and output stored into a wire, this is repeated 2 more times but on the last time the output is the actual output of the circuit. The XOR waveform is created by following these steps.

The following image shows the waveforms that were generated in this lab

Graphical user interface

Description automatically generated

The following image is the schematic that was generated by vivado during the lab

Diagram

Description automatically generated

**Conclusion**

This lab was served as a good refresher in digital logic and gate manipulation and it was a good lab to be exposed to Verilog for the first time as well.