Ihsan Salari

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Education

BASc Electrical Engineering *University of Waterloo* *Grade: 89%* **Waterloo, ON** *present*

Qualifications

- **Programming:** C, C++, Python, Rust, Git, NVIDIA CUDA, ROS 2, LaTeX, MATLAB, SPICE
- **FPGA:** AMD/Xilinx Vivado & Vitis - Verilog & VHDL - Zynq SoC
- **Tools:** STM32, PIC18, AMD/Xilinx, Intel/Altera, Jira, Confluence, Slack
- **Lab:** Oscilloscope, SMD reflow/iron rework, function generator, electronic load, digital multimeter, power supply
- **eCAD:** LTspice, Altium Designer, KiCAD, COMSOL, Fusion 360, OpenSCAD
- **Languages:** French (Native), German (Native), English (Native), Spanish (Beginner)

Experience

Signal Integrity Engineering *Arista Networks, Inc.* **Santa Clara, CA** *09/2025-present*

- Simulated and optimized 200G PAM4 SerDes and PCIe Gen 5 differential pairs using Hyperlynx, HFSS, ADS, and Sigrity.
- Investigated insertion/return losses and TDRs to perform root cause analysis of SI concerns and make PCB layout modifications.
- Tuned vias and ASIC/connector breakouts to meet loss budgets through iterative deduction, 3D modelling and simulation.
- Provided detailed signal integrity reports and collaborated with HW engineers to develop layout of 102.4T switches.
- Performed PCB material characterization and system debug at up to 70GHz using ultra high-end VNAs, TDRs, and oscilloscopes.
- Used Cadence tools to work on and review schematics and layouts and provide hardware design recommendations.
- Prototyped and implemented setups to test viability of future designs, validate current PCBs and perform case-by-case debug.

Power Electronics Designer *aiRadar Inc.* **Vancouver, BC** *01/2025 - 05/2025*

- Spearheaded end-to-end redesign of **3.5MHz GaN**, wide input/output multi-stage dc-to-dc converter for advanced multi-beam sonar, including research, topology selection, simulation, firmware development and testing.
- Implemented robust **STM32** firmware with voltage-fed **PID control**, live telemetry, and extensive **UART** command interface.
- Designed and built breadboard prototypes using GaN FET eval kits and STM32 dev boards for initial testing and PID tuning.
- Proposed and validated converter topologies using **LTspice** simulations that accounted for parasitics at MHz frequencies.
- Authored extensive technical documentation in **LaTeX** detailing power electronics theory, designs tradeoffs, simulation, custom mathematical models, component selection, and embedded firmware architecture.
- Developed and executed board bring-up and test plan; rapidly iterated on testing methodology based on real-time results.
- Collaborated with a fast-paced engineering team and provided regular updates on design, timeline and executive decisions.

Technical Projects

Electrohydrodynamic (Ionic) Propulsion *09/2022 - 10/2023*

- Designed and constructed functioning **50kV 100W** high voltage (HV) flyback power converter with Cockcroft-Walton voltage multiplier simulated in **LTspice**.
- Designed and built working electrohydrodynamic (ionic) thruster that achieved wind speeds of $1.5ms^{-1}$ and thrust of $40mN$.
- Inspired by **MIT research**, authored paper in which the optimal electrode pair spacing in single-stage thrusters consisting of two electrode pairs in parallel operation was derived and confirmed in a custom experiment.

Lorentz Solver *11/2024 - present*

- Computes and subsequently animates particle paths in 3D through complex user-defined electromagnetic spaces which include current carrying coils, uniform E and B fields, charged particles and more for **nuclear fusion reactor simulations**.
- **C++ simulation engine** computes Lorentz force on particles and applies 4th order Runga-Kutta method to compute position.
- **Python** script plots computed particle paths and vector fields using **Manim** mathematical library, enabling dynamic visualizations.
- Developping parallelized **NVIDIA CUDA** implmentation to accelerate computionof magnetic and electric vector fields.