Ihsan Salari

+1 (236)-996-7441 hi@ihsan.cc https://ihsan.cc /in/ihsan-sa Portfolio

Education

BASc Honors Electrical Engineering *University of Waterloo* *Grade: 89%* **Waterloo, ON** *2024 - 2029*

Qualifications

- **High-speed/SI:** 224G PAM4 SerDes, PCIe Gen 5, 102.4T systems, CPO/LPO optics
- **eCAD:** Cadence Allegro/OrCAD, LTspice, HFSS, HyperLynx, ADS, Altium
- **Lab:** 70GHz VNA, TDR, bode plots, logic analyzer, SMD rework
- **Tools:** STM32, AMD/Xilinx Zynq SoC
- **Programming:** C/C++, Python, MATLAB, SPICE, CUDA

Experience

Signal Integrity and Hardware Design *Arista Networks, Inc.* **Santa Clara, CA** *09/2025 - present*

- Fast-tracked selection of compact, highly efficient PMICs for **1.6T LRO OSFP** and **CPO optics**, shaving weeks off schedule.
- Ensured SI on highest priority **102.4T** switch by simulating **224G PAM4 SerDes** and **PCIe Gen 5** differential pairs using **Hyperlynx**/**HFSS**/**ADS** and advised layout to meet loss budgets, reduce crosstalk, reflections, and resonances, and meet DFM.
- Unblocked fabout of two most-advanced 102.4T switches through mission-critical **224G SI debug** using **70GHz VNAs**; ran and analyzed **TDRs** to pinpoint source of discontinuities, quantify skew, and determine impedance variation due to microstrip section.
- Owned end-to-end redesign of **PCIe Gen 5 SSD bridge** card from schematic changes -> layout instructions -> SI -> fabout; ensured separate TX/RX planes to reduce effect of NEXT, confirmed stackup impedance specs, and coordinated with NPI/mech.
- Enabled PCIe Gen 5 by optimizing via impedance (antipads, NFPs, spacing, diameters), meeting -20 dB return loss at Nyquist.
- Caught fatal ethernet magnetics saturation issue on Eth/RS-232 multiplexing project by implementing lab and SPICE sim setups.

Power Electronics Designer *aiRadar, Inc.* **Vancouver, BC** *01/2025 - 05/2025*

- Spearheaded end-to-end redesign of cutting-edge **3.5MHz GaN** wide input/output multi-stage dc-to-dc converter for advanced multi-beam sonar, including research, topology selection, simulation, firmware development, bringup, and testing.
- Designed and built lab prototypes using GaN FET eval kits and STM32 dev boards, enabling initial testing and PID tuning.
- Proposed and validated dc-to-dc converter topologies using **LTspice** simulations, accounting for parasitics at MHz frequencies.
- Authored extensive technical documentation in **LaTeX** detailing power electronics theory, designs tradeoffs, simulation, custom mathematical models, component selection, and embedded firmware architecture.
- Developed and executed board bring-up and test plan; rapidly iterated on testing methodology based on real-time results.
- Implemented **STM32** firmware with voltage-fed **PID control**, live telemetry, and extensive **UART** command interface.

Technical Projects

77GHz mmWave FMCW Radar with Xilinx Zynq Ultrascale+ DSP *09/2025 - present*

- Designed system architecture including RFIC, Kria SoM, I/O and memory selection for automotive and robotics sensing Radar.
- Developing hardware design for Kria K26 SOM, IWR1443 mmWave RFIC, SSD and IO (1G PoE, USB-C PD, JTAG and SD).
- Designing custom stackup optimized for crosstalk reduction and with impedance control for 77GHz RF, CSI2 and 1G Eth.
- Implementing low-cost layout of digital signals and 77GHz RF by reducing stubs, via-shielding, and adding coplanar waveguides.

Electrohydrodynamic (Ionic) Propulsion *09/2022 - 10/2023*

- Designed and constructed **50kV 100W** flyback converter with Cockcroft-Walton voltage multiplier simulated in **LTspice**.
- Designed and built working electrohydrodynamic (ionic) thruster that achieved wind speeds of $1.5ms^{-1}$ and thrust of $40mN$.
- Building on **recent MIT research**, authored a paper deriving optimal electrode spacing for parallel multi-electrode ionic thrusters, validated experimentally.

USB-C Trigger Board *08/2025*

- End-to-end design of **140W USB-C Power Delivery (PD)** trigger board with Extended Power Range (EPR) serial interface.
- Implemented solution based on USB-C PD IC with I2C configuration via onboard STM32 hosting custom negotiation firmware.
- Designed **6-layer PCB** optimizing return paths, power trace dimensions and thermals, and subsequently reflowed prototypes.