N4

Datasheet

4-CH Automotive RX with MIPI-CSI2 Interface

Web : www.nextchip.com

E-mail : sales@nextchip.com
Tel : **+82-2-3460-4700**

[주]넥스트칩 nextchip

REVISION HISTORY

Rev.	Date.	Description	Note
REV 0.0	2017-12-20	Initial Draft	-
REV 0.1	2018-07-31	Update Chapter 6 ELECTRICAL CHARACTERISTICS	P78
REV 0.2	2018-08-06	Add to Constraint for 1080p*4ch parallel output	P03, P79

Nextchip Corporation Ltd
8F, Twosun Venture Forum Bldg., 323, Pangyo-ro, Bundang-gu, Seongnam-si, Gyeonggi-do, Korea 463-400

Nextchip's home page can be found at:
http://www.nextchip.com

Product Overview

N4 includes Automotive 4-Channel RX with MIPI-CSI2/BT.656 Interface. It delivers high quality CVBS, 1M, 2M image. It accepts CVBS, COMET, 1M, 2M analog inputs from Camera and the other video signal sources. It accepts Single-ended/Differential analog SD/HD/FHD video signals, and then Processing Clamp/AGC(Auto Gain Control)/YC Separation and Converting BT.656/BT.1120/MIPI-CSI2 Format. MIPI-CSI2 interface compliant with MIPI D-PHY v1.1.

N4 is able to use same transmission cable with conventional one for CVBS/COMET(SD level), 1M/2M(HD/FHD level) and they provide the superior-image quality by minimizing the interference when separating Y and C.

N4 support Coaxial Communication Protocol communicates between controller(DVR) and camera on the video signal through coaxial cable.

Features

1. Video Decoder

- **Input Formats**
  - 4CH Single-ended & Differential Analog Video Input
    : CVBS / COMET
    : Analog HD 1M/2M

- **Output Formats**

- Support 8bit*4 parallel output port, each port video output format selectable(Up to 720p@25p/30*4ch)
- Support Byte-interleave for each 8bit parallel output port
- Support MIPI-CSI2, 4 Lane for single and virtual channel
- MIPI-CSI2 1/2/4 Data Lane Configuration
  (Up to 1080p@25p/30p*4ch)
  : YUV422 8bit Format
- 2 Data Lanes for up to 720p@50/60, 1080p@25/30 2CH
- 4 Data Lanes for up to 720p@50/60, 1080p@25/30 4CH

- **Image Signal Processor**

- Support Single-ended and Differential Analog video Input up to 2M format for Each CH
- On Chip Analog CLAMP/Anti-aliasing Filter and EQ Filter
- Accepts CVBS, COMET, 720P@25p/30p/50p/60p, 1080P@25p/30p
- Robust Sync detection for weak and unstable signals
- High-performance adaptive comb filter
- Programmable H/V Peaking filter for Luminance
- CTI (Chrominance Transient Improvement)
- Color compensation for PAL
- IF compensation filter
- Robust No-video detection
- Programmable Brightness, Contrast, Saturation and Hue
- Programmable Picture Quality Control

2. MISC

- Built in Clock PLL
- Single 27M Oscillator for all video standards
- Built in 4-Ch Motion Detector(32x24)
- Support 4-Ch Coaxial Communicator
- Support Each Channel MPP Pin and IRQ Pin
- Support I2C serial Interface

3. Operating Voltage

- 3.3V/1.2V Supply Voltage

5. Ordering information

DEVICE	PACKAGE
N4	121-BGA-8x8

6. Applications

- Automotive surround view
- CMS

Functional block diagram

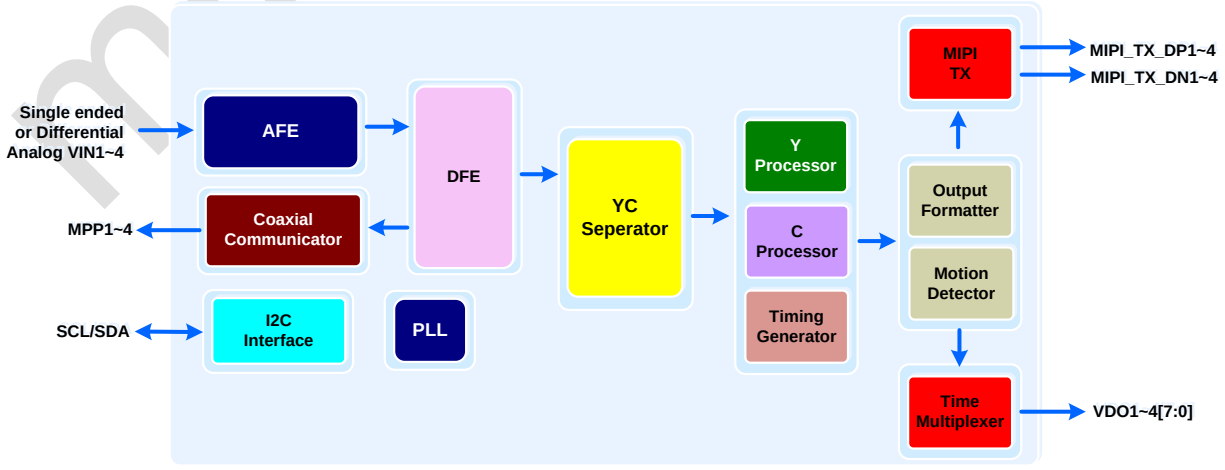


TABLE OF CONTENTS

Contents of Tables

CONTENTS OF FIGURES

Chapter 1
PIN INFORMATION

1.1 PIN ASSIGNMENTS

	1	2	3	4	5	6	7	8	9	10	11	
A	N.C.	VDO1_5	VDO1_4	VDO1_2	VDO1_1	VCLK2	VDO2_7	VDO2_4	VDO2_1	VDO3_6	N.C.	A
B	VCLK1	VDO1_7	VDO1_6	VDO1_3	VDO1_0	GPO4	VDO2_6	VDO2_2	VDO2_0	VDO3_5	VDO3_4	B
C	REFT1	MPP1	MPP2	MPP3	MPP4	GPO3	VDO2_5	VDO2_3	VDO3_7	VDO3_3	VDO3_2	C
D	VINP1	REFB1	AVDD12_CH1	GPO2	DVDD33	DVDD12	DVDD33	DVDD12	VCLK3	VDO3_0	VDO3_1	D
E	REFT2	VINN1	AVDD33	GPO1	VSS	VSS	VSS	DVDD33	GPO5	VCLK4	VDO4_7	E
F	VINP2	REFB2	AVDD12_CH2	VSS	VSS	VSS	VSS	DVDD12	GPO6	VDO4_6	VDO4_5	F
G	REFT3	VINN2	AVDD33	VSS	VSS	DVDD12	DVDD33	GPO7	VDO4_4	VDO4_2	VDO4_3	G
H	VINP3	REFB3	AVDD12_CH3	AVDD12_PLL	DVDD12	DVDD33	SA0	IRQ	GPO8	VDO4_0	VDO4_1	H
J	REFT4	VINN3	AVDD33	TEST0	SA1	MIPI_TX_VREG	AVDD12_MIPI	AVSS_MIPI	SEL18	SCL	SDA	J
K	VINP4	REFB4	AVDD12_CH4	TEST1	MIPI_TX_DN4	MIPI_TX_DN3	MIPI_TX_CN	MIPI_TX_DN2	MIPI_TX_DN1	RSTB	TEST_CLK1	K
L	N.C.	VINN4	AVDD33	SYS_CLK	MIPI_TX_DP4	MIPI_TX_DP3	MIPI_TX_CP	MIPI_TX_DP2	MIPI_TX_DP1	TEST_CLK2	N.C.	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 1.1 Pin Assignments

1.2 PIN DESCRIPTION

Table 1.1 PIN Description

Module Name			
NAME	IO	DESCRIPTION	PIN NO.
System Interface			
RSTB	DI	System Reset(Active Low)	K10
SYS_CLK	DI	Oscillator Input (27MHz)	L4
TEST0	I	Chip Test mode selection1 PIN (Normally Connect to Ground)	J4
TEST1	I	Chip Test mode selection2 PIN (Normally Connect to Ground)	K4
Analog Video Input Interface			
VINP1	AI	Analog Video Positive Input 1	D1
VINN1	AI	Analog Video Negative Input 1	E2
VINP2	AI	Analog Video Positive Input 2	F1
VINN2	AI	Analog Video Negative Input 2	G2
VINP3	AI	Analog Video Positive Input 3	H1
VINN3	AI	Analog Video Negative Input 3	J2
VINP4	AI	Analog Video Positive Input 4	K1
VINN4	AI	Analog Video Negative Input 4	L2
REFT1	AO	ADC Reference Top Output 1	C1
REFB1	AO	ADC Reference Bottom Output 1	D2
REFT2	AO	ADC Reference Top Output 2	E1
REFB2	AO	ADC Reference Bottom Output 2	F2
REFT3	AO	ADC Reference Top Output 3	G1
REFB3	AO	ADC Reference Bottom Output 3	H2
REFT4	AO	ADC Reference Top Output 4	J1
REFB4	AO	ADC Reference Bottom Output 4	K2
Digital Video Parallel Interface			
VCLK1	O	Video Parallel Port1 Output Clock	B1
VDO1_7	O	Video Parallel Port1 Data Output [7]	B2
VDO1_6	O	Video Parallel Port1 Data Output [6]	B3
VDO1_5	O	Video Parallel Port1 Data Output [5]	A2
VDO1_4	O	Video Parallel Port1 Data Output [4]	A3
VDO1_3	O	Video Parallel Port1 Data Output [3]	B4
VDO1_2	O	Video Parallel Port1 Data Output [2]	A4
VDO1_1	O	Video Parallel Port1 Data Output [1]	A5
VDO1_0	O	Video Parallel Port1 Data Output [0]	B5
VCLK2	O	Video Parallel Port2 Output Clock	A6
VDO2_7	O	Video Parallel Port2 Data Output [7]	A7
VDO2_6	O	Video Parallel Port2 Data Output [6]	B7
VDO2_5	O	Video Parallel Port2 Data Output [5]	C7
VDO2_4	O	Video Parallel Port2 Data Output [4]	A8
VDO2_3	O	Video Parallel Port2 Data Output [3]	C8
VDO2_2	O	Video Parallel Port2 Data Output [2]	B8
VDO2_1	O	Video Parallel Port2 Data Output [1]	A9
VDO2_0	O	Video Parallel Port2 Data Output [0]	B9
VCLK3	O	Video Parallel Port3 Output Clock	D9
VDO3_7	O	Video Parallel Port3 Data Output [7]	C9
VDO3_6	O	Video Parallel Port3 Data Output [6]	A10
VDO3_5	O	Video Parallel Port3 Data Output [5]	B10
VDO3_4	O	Video Parallel Port3 Data Output [4]	B11
VDO3_3	O	Video Parallel Port3 Data Output [3]	C10
VDO3_2	O	Video Parallel Port3 Data Output [2]	C11
VDO3_1	O	Video Parallel Port3 Data Output [1]	D11
VDO3_0	O	Video Parallel Port3 Data Output [0]	D10

Digital Video Parallel Interface			
VCLK4	O	Video Parallel Port4 Output Clock	E10
VDO4_7	O	Video Parallel Port4 Data Output [7]	E11
VDO4_6	O	Video Parallel Port4 Data Output [6]	F10
VDO4_5	O	Video Parallel Port4 Data Output [5]	F11
VDO4_4	O	Video Parallel Port4 Data Output [4]	G9
VDO4_3	O	Video Parallel Port4 Data Output [3]	G11
VDO4_2	O	Video Parallel Port4 Data Output [2]	G10
VDO4_1	O	Video Parallel Port4 Data Output [1]	H11
VDO4_0	O	Video Parallel Port4 Data Output [0]	H10
MIPI Interface			
MIPI_TX_DP1	AO	MIPI Data Positive Output Lane 1	L9
MIPI_TX_DN1	AO	MIPI Data Negative Output Lane 1	K9
MIPI_TX_DP2	AO	MIPI Data Positive Output Lane 2	L8
MIPI_TX_DN2	AO	MIPI Data Negative Output Lane 2	K8
MIPI_TX_VREG	AO	0.4V Regulator Output	J6
MIPI_TX_CP	AO	MIPI Clock Positive Output Lane	L7
MIPI_TX_CN	AO	MIPI Clock Negative Output Lane	K7
MIPI_TX_DP3	AO	MIPI Data Positive Output Lane 3	L6
MIPI_TX_DN3	AO	MIPI Data Negative Output Lane 3	K6
MIPI_TX_DP4	AO	MIPI Data Positive Output Lane 4	L5
MIPI_TX_DN4	AO	MIPI Data Negative Output Lane 4	K5
I2C Interface			
SCL	I	I2C Interface Clock (3.3V tolerant)	J10
SDA	B	I2C Interface R/W Data (3.3V tolerant)	J11
SA0	I	Pin1 for Slave Address	H7
SA1	I	Pin2 for Slave Address	J5
ETC Interface			
SEL18	I	Digital I/O Power Control Pin (DVDD ≥ 2.5V, SEL18 = Low)	J9
IRQ	O	Interrupt Request Output	H8
MPP1	O	Coaxial Output1	C2
MPP2	O	Coaxial Output2	C3
MPP3	O	Coaxial Output3	C4
MPP4	O	Coaxial Output4	C5
GPO1	O	Multi-Purpose Pin Output1	E4
GPO2	O	Multi-Purpose Pin Output2	D4
GPO3	O	Multi-Purpose Pin Output3	C6
GPO4	O	Multi-Purpose Pin Output4	B6
GPO5	O	Multi-Purpose Pin Output5	E9
GPO6	O	Multi-Purpose Pin Output6	F9
GPO7	O	Multi-Purpose Pin Output7	G8
GPO8	O	Multi-Purpose Pin Output8	H9

Power / Ground / N.C.			
DVDD12	P	Digital 1.2V Power	H5, D6, G6, D8, F8
DVDD33	P	Digital 3.3V Power	D5, H6, D7, G7, E8
AVDD12_CH1	P	Analog 1.2V Power for CH1 Video AFE	D3
AVDD12_CH2	P	Analog 1.2V Power for CH2 Video AFE	F3
AVDD12_CH3	P	Analog 1.2V Power for CH3 Video AFE	H3
AVDD12_CH4	P	Analog 1.2V Power for CH4 Video AFE	K3
AVDD33	P	Analog 3.3V Power for Video AFE	E3,G3,J3,L3
AVDD12_PLL	P	Analog 1.2V Power for PLL	H4
AVDD12_MIPI	P	Analog 1.2V Power for MIPI TX	J7
VSS	G	Ground	F4, G4, E5, F5, G5, E6, F6, E7, F7
TEST_CLK1	G	Normally Connect to Ground	K11
TEST_CLK2	G	Normally Connect to Ground	L10
AVSS_MIPI	G	Analog Ground for MIPI	J8
N.C	G	N.C	A1,A11,L1,L11

Chapter 2
Automotive RX(1M to 2M)

N4 includes automotive 4-Channel RX with MIPI-CSI2/BT.656 Interface. It delivers high quality CVBS, 1M, 2M image. It accepts CVBS, COMET, 1M, 2M analog inputs from Camera and the other video signal sources. It accepts Single-ended/Differential analog SD/HD/FHD video signals, and then Processing Clamp/AGC(Auto Gain Control)/YC Separation and Converting BT.656/BT.1120/MIPI-CSI2 Format. MIPI-CSI2 interface compliant with MIPI D-PHY v1.1.

N4 includes 4-Channel analog processing circuit that comprises anti-aliasing filter, ADC, CLAMP and Equalizer filter. It shows the best image quality by adaptive high performance comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness, Contrast and several functions such as CTI, Programmable peaking filter and various compensation filters.

2.1 FUNCTIONAL OVERVIEW

N4 1M to 2M RX separates luminance and chrominance signals from Analog Inputs.

The First step to decode RX is to digitize the entire video signal using an A/D converter (ADC). Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic.(AGC)

The video signal also is low-pass filtered in Anti aliasing Filter to remove any high-frequency components that may result in aliasing.
Vertical sync and horizontal sync information are recovered in Genlock block.

When composite video signal is decoded, the luminance and chrominance are separated by YCS(Y/C Separator).

The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, Adaptive Comb Filter is used.

The color demodulator in chroma processing block accepts modulated chrominance data from Adaptive Comb Filter which generate Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sine and cosine subcarrier data.

2.2 ANALOG FRONT END (CLAMP, ANTI-ALIASING FILTER, EQ FILTER)

N4 includes 4 Channel Analog Processing circuits that comprise anti-aliasing filter, EQ Filter, ADC and CLAMP. Because its design is dedicated for video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for **N4**. Anti-aliasing Filter is controlled by Register and include bypass mode that don't have AFE filtering.

2.3 GENLOCK (ROBUST SYNC DETECTION, ROBUST NO-VIDEO DETECTION)

N4 provides a fully digital Genlocking circuitry. The digital Genlocking Circuitry use the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier.

N4 uses the proprietary Genlock mechanism for video application system.

It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

2.4 YCS (Y/C SEPARATOR)

The YCS is used to separate Y and C signal from HD standard video signal. Therefore, the output image is sharper and clearer compared to other device. To achieve this, BSF(Band Split Filter) is used

N4 can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the **N4**, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.5 LUMA PROCESSING

The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

N4 provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The Peaking filter is applied to this purpose and its characteristics can be controlled by register (Y_PEAK_MODE, 0x30[3:0] / 0x31[3:0] / 0x32[3:0] / 0x33[3:0], Bank0) via I2C interface.

2.6 CHROMA PROCESSING

The Chroma Processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The Chroma Demodulator receives modulated chroma from YC separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

2.7 MOTION DETECTOR

N4 supports 4-Channels motion detection function. It supports the output of the detected motion information on the screen. The function allows a screen such as the one shown in Figure 2.1. To be divided in 192 sections each of which can generate information on the motion detection information.

For each section, motion detection can be controlled to be set at on/off. Once a motion is detected, the screen can be rendered dark or reversed in the unit of field to have the spot of the motion generated to be indicated in the screen.

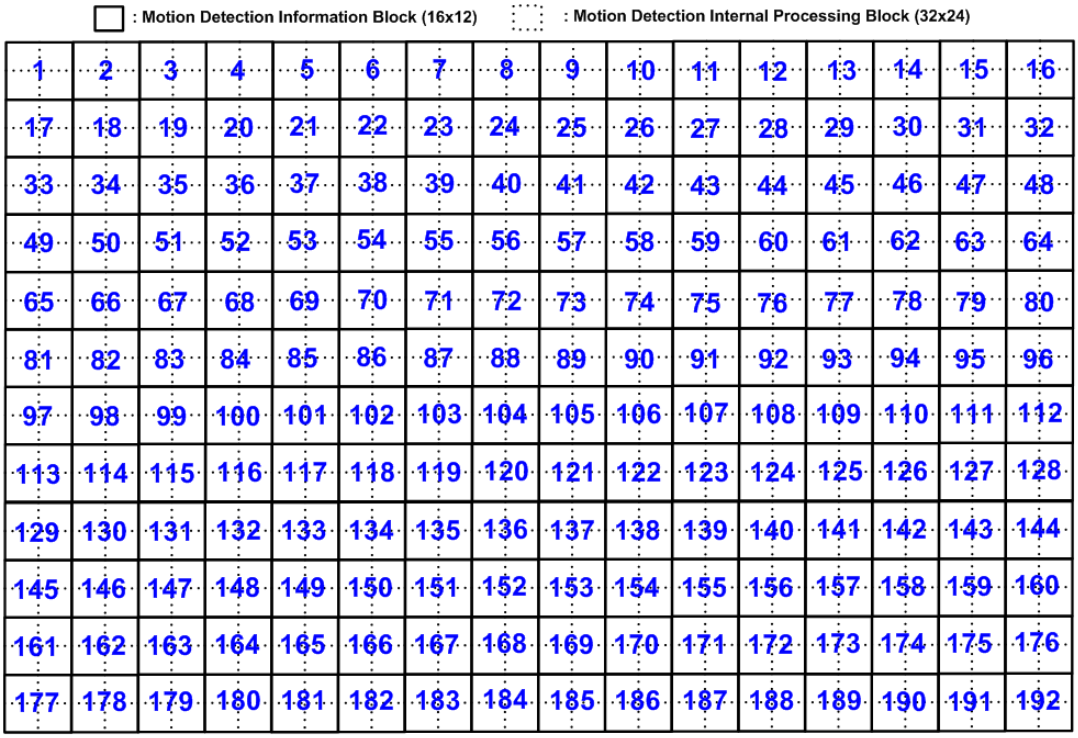


Figure 2.1 Motion Block Mapping

2.8 COAXIAL PROTOCOL

N4 includes Coaxial Protocol generator that sends control signal from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal. **N4** supports Protocol for CVBS/COMET(PELCO) and AHD(A-CP). It depends on Coaxial Cable impedance characteristic. This document presents the concept of Coaxial Protocol. Coaxitron is Pelco's name for a method of sending control signaling from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal (Known as "Up the Coax" or "UTC")

2.8.1 PELCO PROTOCOL

There are two types of Coaxitron command structures. One type, Standard Coaxitron is a series of 15 pulses, or data bits, that are sent within video line 18 of a video field. The other type, Extended Coaxitron, is a series of 32 pulses, where 16 pulses are sent in line 18 and 16 pulses in line 19 of a video field. Refer to Figure 2.2. No pulses are sent when the system is in an idle state

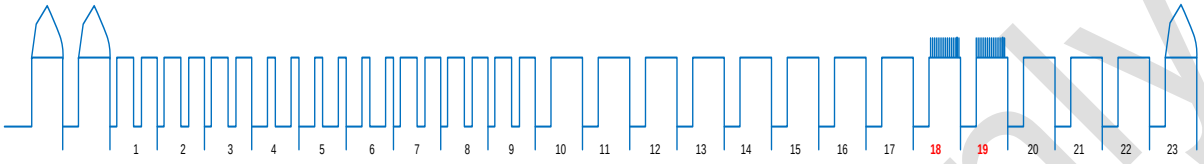


Figure 2.2 Coaxitron Active line

Coaxitron is a pulse width modulated (PWM) that is inserted into video vertical blanking interval. A 2us pulse represents a one(1) and a 1us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 2.3. and Figure 2.4.

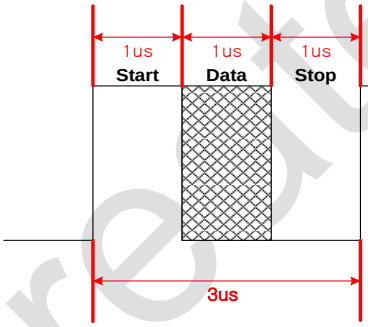


Figure 2.3 Description of One Coaxitron Bit

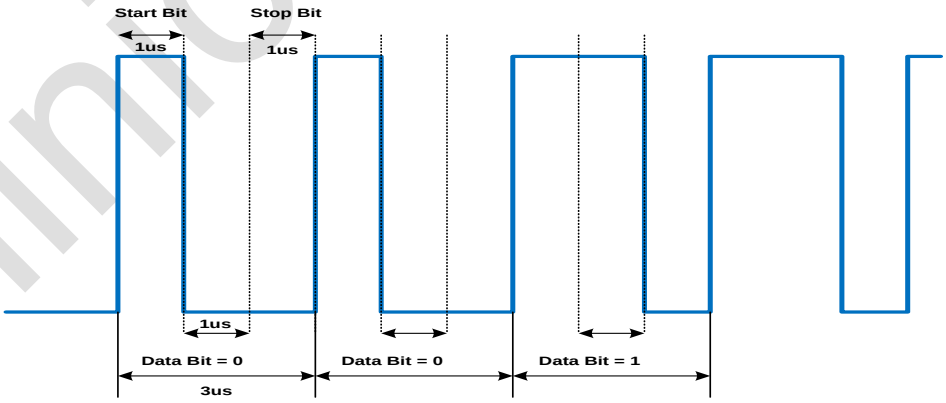


Figure 2.4 Coaxitron Bit Timing

N4 is able to control coaxitron timing format on the video signal.

Start Active line of Coaxitron is 18th line on VBI. Pulse width of Coaxitron is fixed 1us. The size of Coaxial Data is 4 bytes. Refer to Figure 2.5.

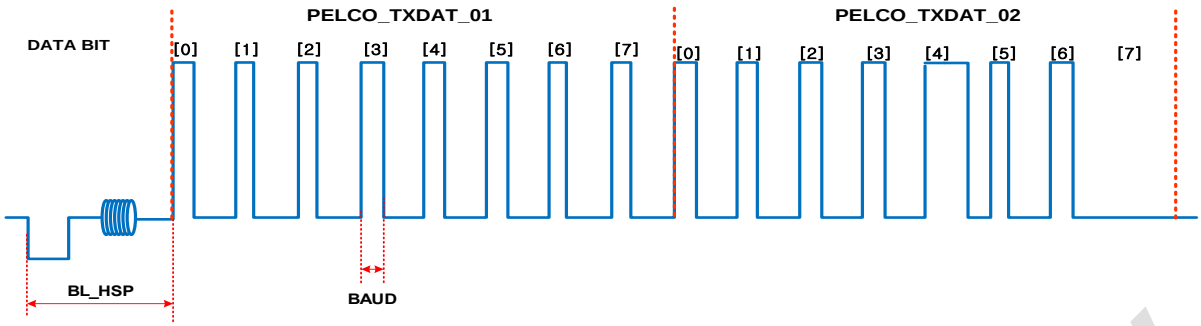


Figure 2.5 Data Structure of Coaxitron Origins (VBI 18th)

2.8.2 A-CP(AHD-Coaxial protocol)

It is an acronym of AHD Coaxial Protocol. This term signifies the interactive communication protocol between Image Signal Processor. As a major feature, A-CP Data located in the 17~20th line. Also Data is 8bit each line.

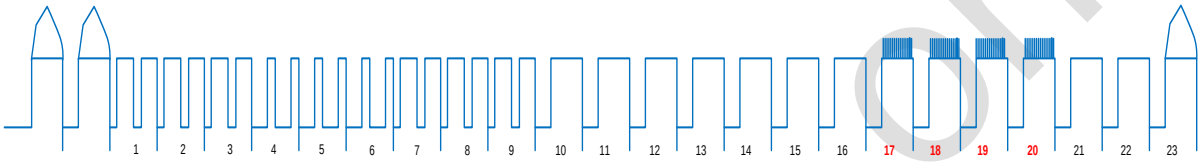


Figure 2.6 A-CP Active line

A-CP is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 1.8us pulse represents a one(1) and a 0.6us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 2.7. and Figure 2.8.

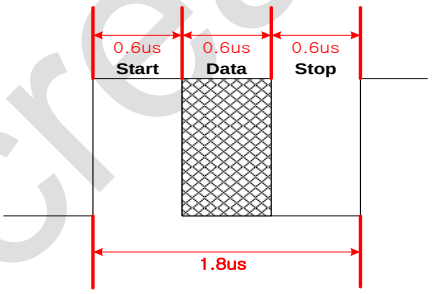


Figure 2.7 Description of A-CP One Data Bit

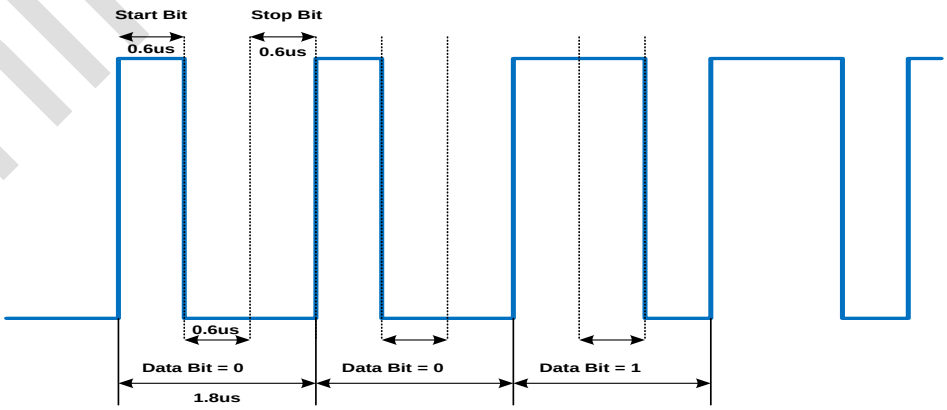


Figure 2.8 Data A-CP Bit Timing

Start Active line of Coaxitron is 17th line on VBI. Pulse width of Coaxitron is fixed 0.6us. The size of Coaxial Data is 4 bytes. Refer to Figure 2.9.

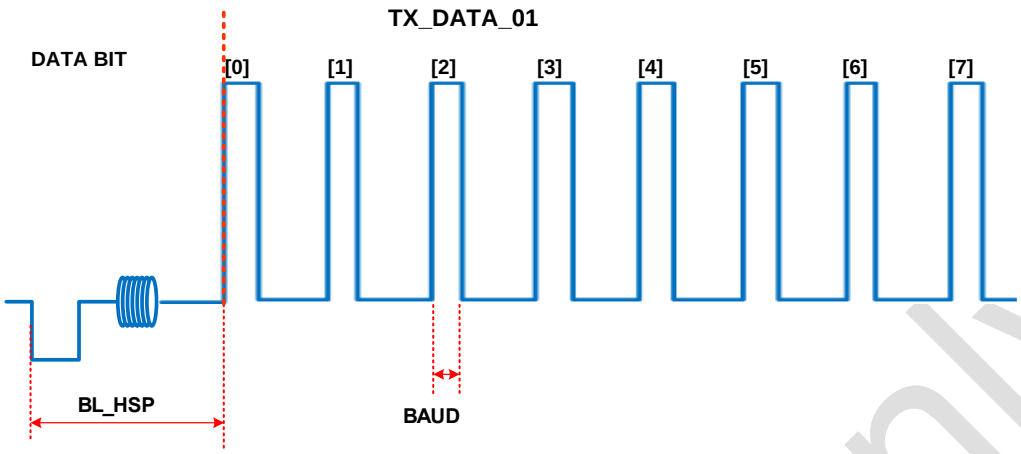


Figure 2.9 Data Structure of Coaxitron Origins (VBI 17th)

Chapter 3
VIDEO OUTPUT INTERFACE

3.1 Digital Output Format

N4 supports a format of standard ITU-R BT.656/1120. Ports of 4 is synchronized by each output clock(VCLK_1~VCLK_4).

3.1.1 ITU-R BT.656/BT.1120 FORMAT

Codes of SAV and EAV are injected into data stream of ITU-R BT.656/1120 to indicate a start and an end of active. Note that a number of pixels for 1H active line are always constant regardless of the actual incoming line length. Therefore, variance of analog input signal is applied to a blank section except codes of EAV and SAV. Figure 3.1 shows data stream of ITU-R BT.656/1120 format. If length of 1H of analog input signals increase or decrease, number of pixel of 'A' increase or decrease.

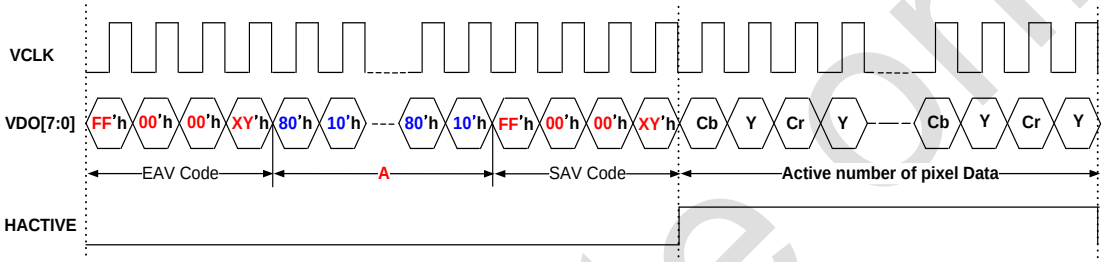


Figure 3.1 Region of active is constant

3.1.2 ITU-R BT.601 FORMAT

N4 support a standard format of ITU-R BT.601.

BT.601 Interface consists of 4 components, 8bit-Video Data, Video Clock, H-SYNC and V-Sync(Figure 3.2). N4 can output H/V-SYNC through GPO1~8 pin and Support up to AHD 1080@25/30P four channels. BT.601 Interface can be set to the following registers:

(BANK1 0xA8=0x10, 0xA9=0x10, 0xAA=0x10, 0xAB=0x10)

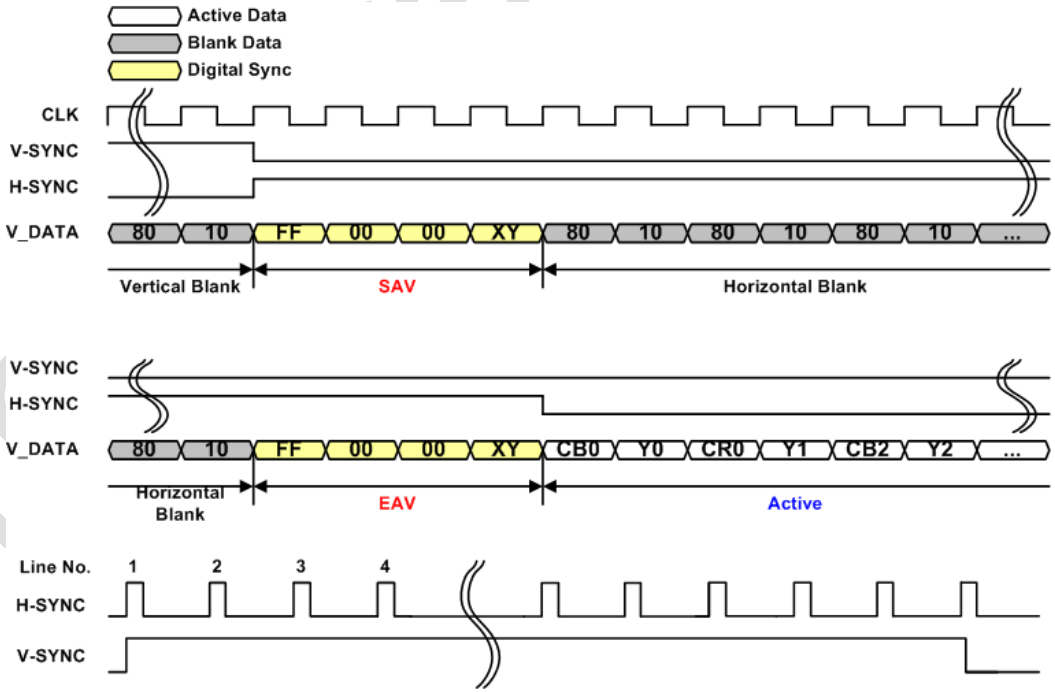


Figure 3.2 BT.601 Interface

3.1.3 VIDEO OUTPUT TIMING INFORMATION

The N4 output timing is like with SD resolution. But some synchronous signals difference with SD resolution as Field information that does not separated EVEN/ODD field. There is next sentence shown timing diagram point of video output.

3.1.3.1 AHD720P @ 30P/25P, 60P/50P H/V Timing

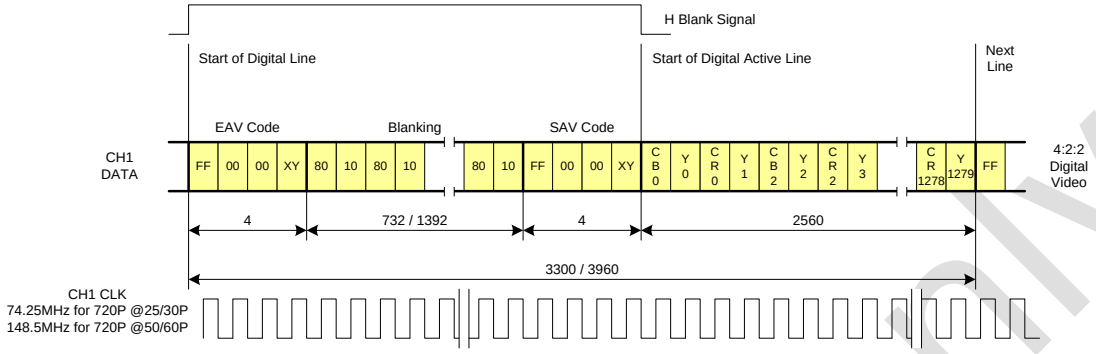
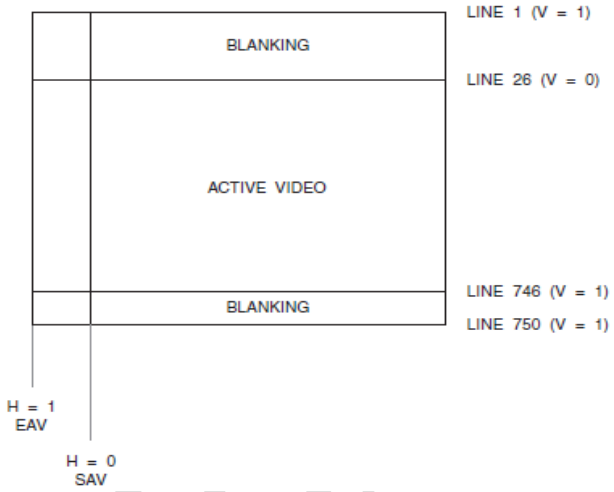


Figure 3.3 AHD720P@30P/25P, 60P/50P Horizontal Timing Diagram



LINE NUMBER	F	V
1–25	0	1
26–745	0	0
746–750	0	1

Figure 3.4 AHD720P@30P/25P, 60P/50P Vertical Timing Diagram

3.1.3.2 AHD1080P @ 30P/25P H/V Timing

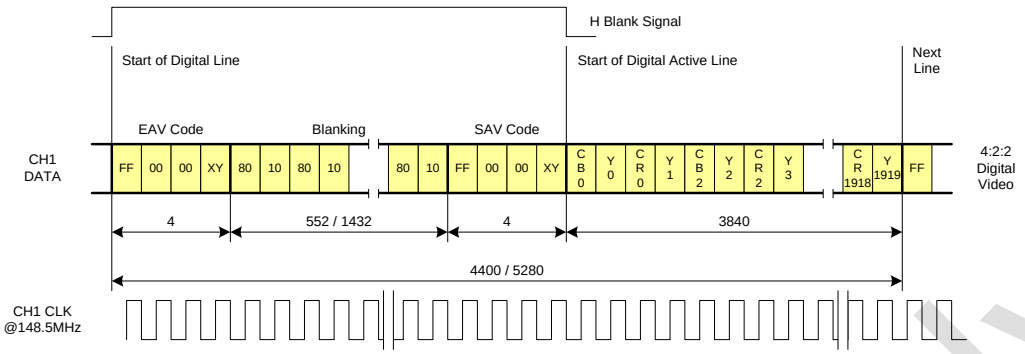
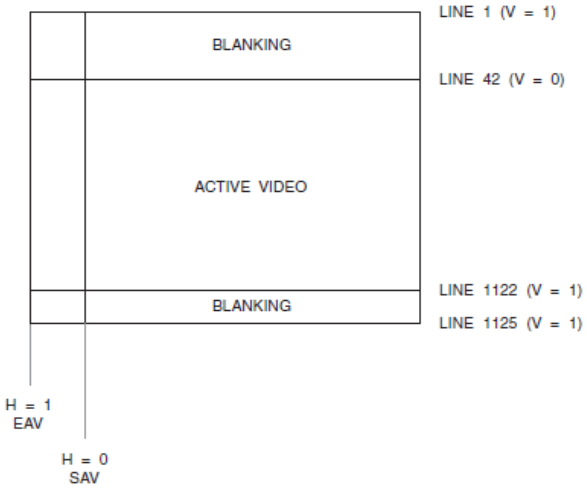


Figure 3.5 AHD1080P@30P/25P Horizontal Timing Diagram



LINE NUMBER	F	V
1–41	0	1
42–1121	0	0
1122–1125	0	1

Figure 3.6 AHD1080P@30P/25P Vertical Timing Diagram

3.1.4 DATA OUTPUT ORDER & DIRECTION CONTROL

N4 can change the order of the output pin in the All Output Mode as shown in Table 3.1. (OUT_DATA_x_INV, 0xD0[3:0] Bank1) Furthermore, as Clock and Data pins control direction so may it does nothing with interconnected back-end device and how control related control register as shown in Table 3.2. (VCLK_x_EN, 0xC8~CB[5] Bank1 / VDO_x_EN, 0xC8~CB[4] Bank1)

Table 3.1 Data Output Pin Order Control

Address (Bank1)	*state*	Data Output of Port X
0xD0[0], OUT_DATA_1_INV	0	VDO_1 [7:0]
	1	VDO_1 [0:7]
0xD0[1], OUT_DATA_2_INV	0	VDO_2 [7:0]
	1	VDO_2 [0:7]
0xD0[2], OUT_DATA_3_INV	0	VDO_3 [7:0]
	1	VDO_3 [0:7]
0xD0[3], OUT_DATA_4_INV	0	VDO_4 [7:0]
	1	VDO_4 [0:7]

Table 3.2 Output Clock and Data Direction Control

Address (Bank1)	*state*	Data Output of Port X
0xC8[5], VCLK_1_EN	0	HI-Z
	1	Output VCLK_1 Enable
0xC9[5], VCLK_2_EN	0	HI-Z
	1	Output VCLK_2 Enable
0xCA[5], VCLK_3_EN	0	HI-Z
	1	Output VCLK_3 Enable
0xCB[5], VCLK_4_EN	0	HI-Z
	1	Output VCLK_4 Enable
0xC8[4], VDO_1_EN	0	HI-Z
	1	Output DATA1 Enable
0xC9[4], VDO_2_EN	0	HI-Z
	1	Output DATA2 Enable
0xCA[4], VDO_3_EN	0	HI-Z
	1	Output DATA3 Enable
0xCB[4], VDO_4_EN	0	HI-Z
	1	Output DATA4 Enable

3.2 MIPI Output Format

N4 supports 4CH Analog Video Input (CVBS/Analgo HD 1M/2M) to a MIPI Interface compliant with MIPI CSI2 V1.1 SPEC. and D-PHY V1.1 SPEC with 1 clock Lane and 4 data Lanes. The max data rate of MIPI data lane is up to 1.5Gbps with YUV422/YUV420/LegacyYUV420-8bit format. The 4 data lane should be used for 4ch 1920x1080@20/30Hz format and 2 data lane can be used for 4ch 1280x720@25/30Hz format. CSI-2 is a lane-scalable specification. The applications that require more bandwidth that what is provide by one data lane or those trying to avoid high clock rates can expand the data path to two, four lanes and obtain approximately linear increases in the peak bus bandwidth. The data stream is distributed between the lanes. This figure shows an example of a 4-lane transmission.

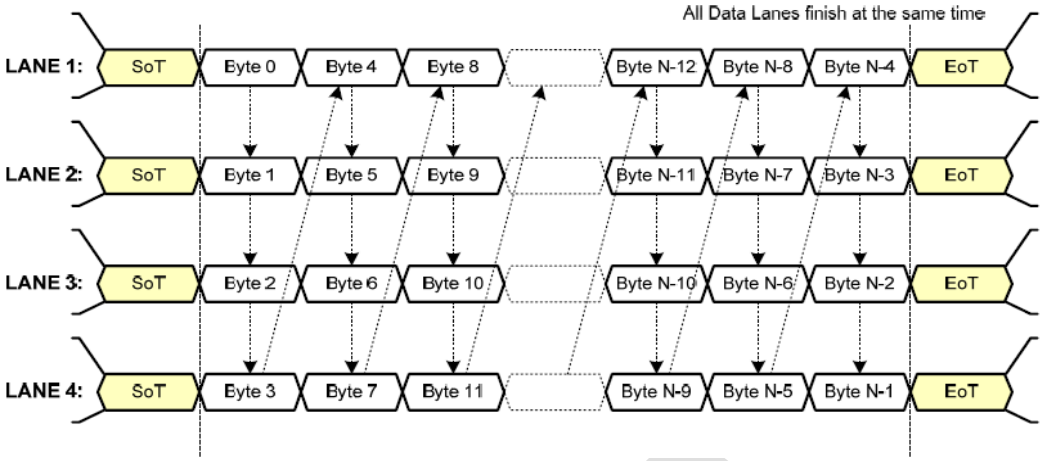


Figure 3.7 Four Lane Multi-Lane Example

3.2.1 Lane States and Line Levels

Transmitter functions determine the Lane state by driving certain Line Levels. During normal operation either a HS-TX or LP-TX is driving a line. A HS-TX always drives the Lane differentially. The two LP-TX's drive the two Lines of a Lane independently and single-ended. This results in two possible High-Speed Lane states and four possible Low-Power Lane states.

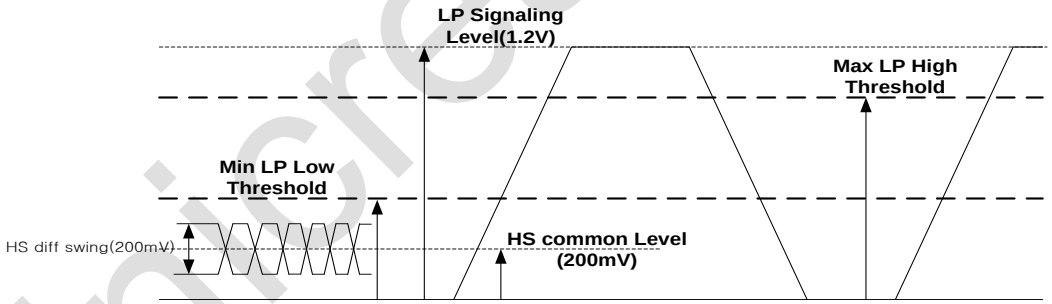


Figure 3.8 Lane Line Levels

Table 3.3 Lane State Decriptions

State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode.
HS-0	HS Low	HS High	Differential-0	N/A, Note 1	N/A, Note 1
HS-1	HS High	HS Low	Differential-1	N/A, Note 1	N/A, Note 1
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A, Note2

Note:

1. During High-Speed transmission the Low-Power Receivers observe LP-00 on the Lines.
2. If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11)

3.2.2 Low-Level Protocol

The Low Level Protocol (LLP) is a byte-oriented, packet-based protocol which supports the transport of arbitrary data using the Short and Long packet format. Two packet structures are defined for the LLP communication: long packets and short packets. For each packet structure, the exit from the low-power state followed by the Start of Transmission(SoT) sequence indicates the start of a packet. The End of Transmission(EoT) sequence followed by the low-power state indicates the end of a packet.

Low LeveL Protocol Features:

- Transport of arbitrary data (payload-independent)
- 8-bit word size
- Support for up to four interleaved virtual channels on the same link
- Special packets for the frame start, frame end information.
- Descriptor for the type, Pixel depth, and format of the application-specific payload data
- 16-bit checksum code for error detection

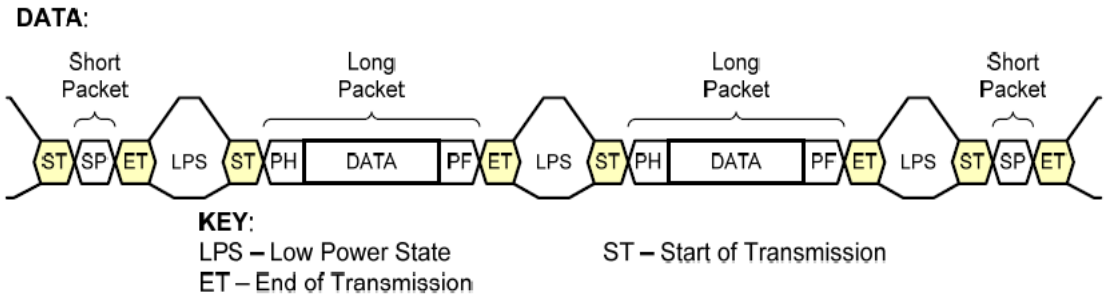


Figure 3.9 LLP Packet format

In the above figure, PH represents the packet header and PF represents the packet footer.

3.2.3 LLP Long Packet Format

A Long Packet shall consist of three elements : a 32-bit Packet Header(PH), an application specific Data Payload with a variable number of 8-bit data words and a 16-bit Packet Footer(PF). The Packet Header is further composed of three elements : an 8-bit Data Identifier, a 16-bit Word Count field and an 8-bit ECC.The Packet footer has one element, a 16-bt checksum.

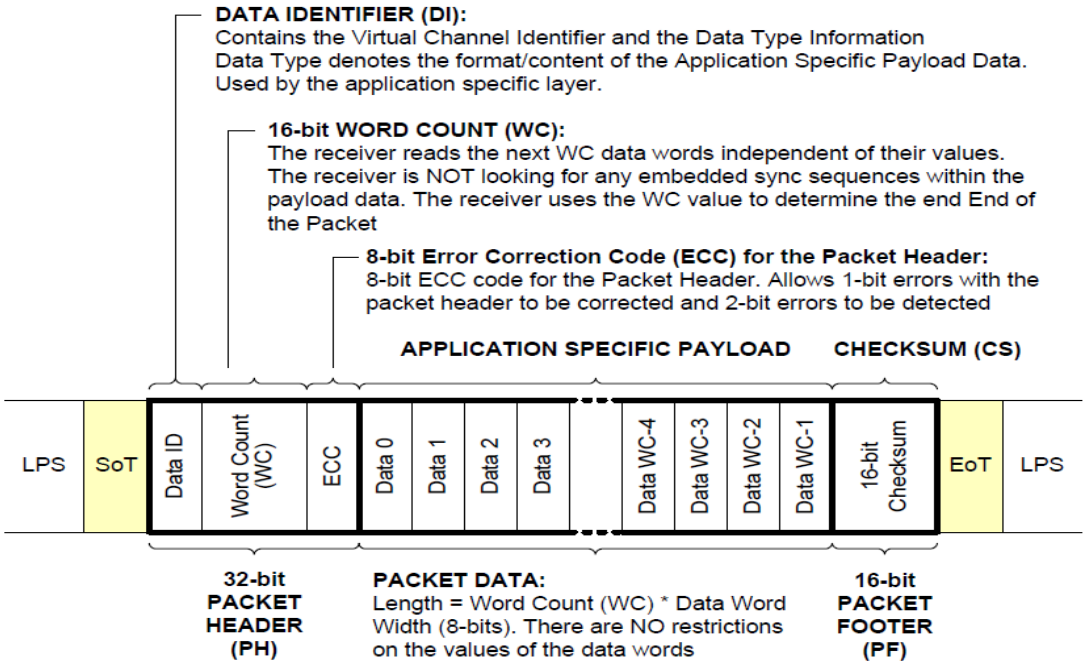


Figure 3.10 Long Packet Structure

3.2.4 LLP Short Packet Format

A Short Packet shall contain only a Packet Header; a Packet Footer shall not be present. The Word Count field in the Packet Header shall be replaced by a Short Packet Data Field.

For Frame Synchronization Data Types the Short Packet Data Field shall be the frame number.

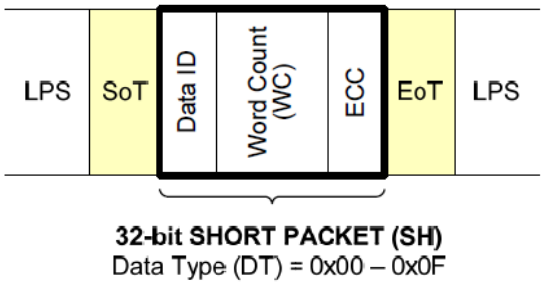


Figure 3.11 Short Packet Structure

3.2.5 Data Identifier

The Data Identifier byte contains the Virtual Channel Identifier(VC) value and the Data Type (DT) value as illustrated in the Figure 3.12. The Virtual Channel Identifier is contained in the two MS bits of the DATA Identifier Byte. The Data Type value is contained in the six LS bits of the Data Identifiers Byte.

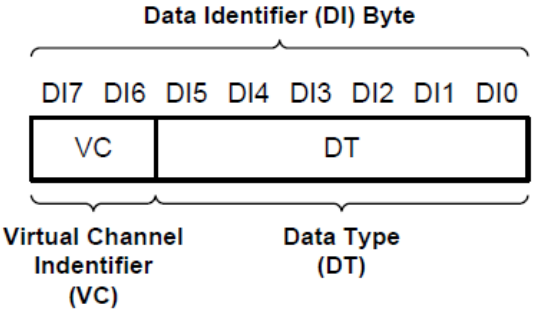


Figure 3.12 Data Identifier Byte

3.2.6 Virtual Channel Identifier Interleaving

The Virtual Channel Identifier allows different data types within a single data stream to be logically separated from each other. Each virtual channel has its own Frame Start and Frame End packet. Therefore, it is possible for different virtual channels to have different frame rates, though the data rate for both channels would remain the same.

Therefore, receivers should be able to de-multiplex different data packets based on the combination of the Virtual Channel Identifier and the Data Type value. For example, data packets containing the same Data Type value but transmitted on different virtual channels are considered to belong to different frames of image data.

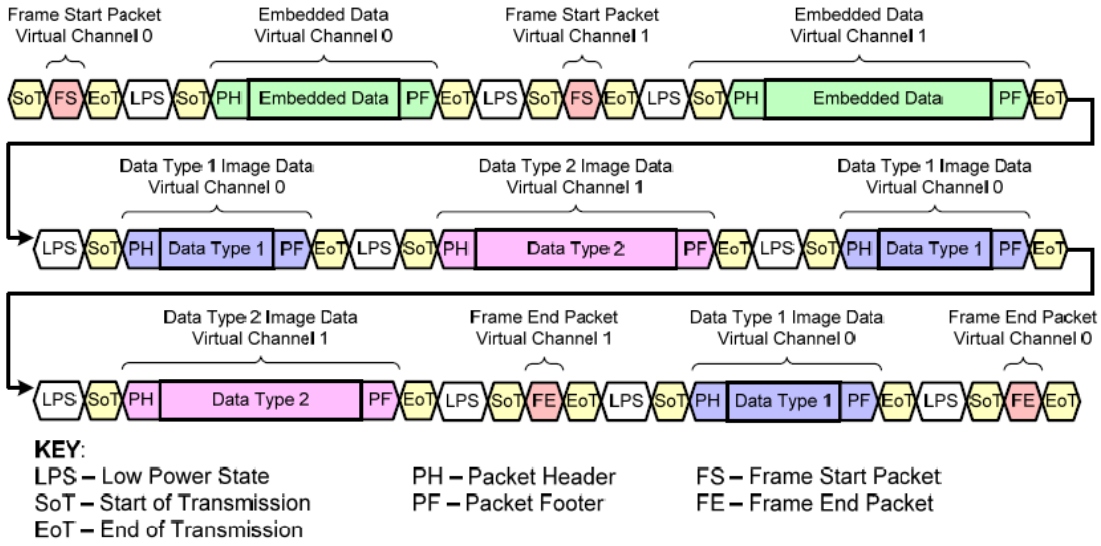


Figure 3.13 Interleaved Data Transmission using Virtual Channels.

3.2.7 YUV Image Data

In the below table defines the data type codes for YUV data format.

YUV420 data formats are divided into legacy and non-legacy data formats. The legacy YUV420 data format is for compatibility with existing systems. The non-legacy YUV420 data formats enable lower cost implementations.

Table 3.4 YUV Image Data Types

Data Type	Description
0x18	**YUV420 8-bit (support)**
0x19	YUV420 10-bit
0x1A	**Legacy YUV420 8-bit(support)**
0x1B	Reserved
0x1C	YUV420 8-bit(CSPS)
0x1D	YUV420 10-bit(CSPS)
0x1E	**YUV422 8-bit(support)**
0x1F	YUV422 10-bit

Legacy YUV420 8-bit data transmission is performed by transmitting UYY…/VYY… sequences in odd/even lines. U component is transferred in odd lines (1,3,5…) and V component is transferred in even lines (2,4,6…).

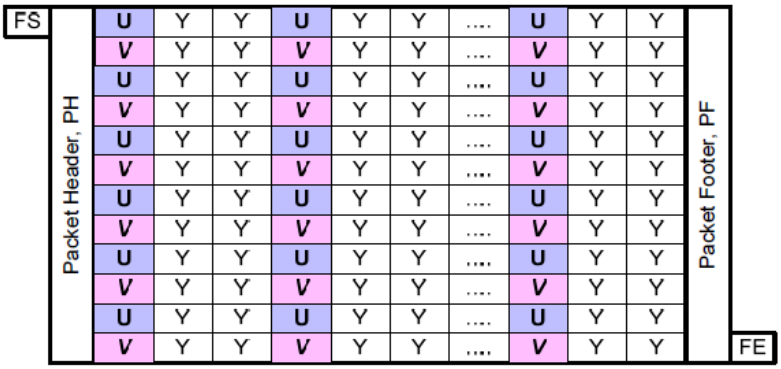


Figure 3.14 Legacy YUV420 8-bit Frame Format

YUV420 8-bit data transmission is performed by transmitting YYYY…/UYVYUYVY… sequences in odd/even lines.

Only the luminance component(Y) is transferred for odd lines (1,3,5 …) and both luminance (Y) and chrominance (U and V) components are transferred for even lines (2,4,6 …). The format for the even lines(UYVY) is identical to the YUV422 8-bit data format.

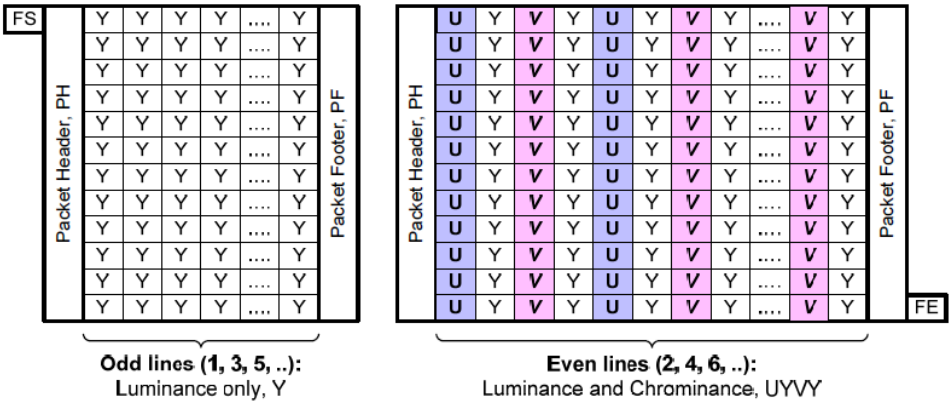


Figure 3.15 YUV420 8-bit Frame Format

Chapter 4
I2C INTERFACE

I2C interface requires 2 wires, SCL (I2C clock) & SDA (I2C R/W data). **N4** provides special device ID as slave addresses (SA0, SA1). So any combination of 7 bit can be defined as slave address of **N4**. The Figure 4.1 shows read/write protocol of I2C interface. The 1st byte transfers the slave address and read/write information. For write mode, the 2nd byte transfers base register index and the 3rd byte transfers date to be written.

For read mode, reading data is transferred during 2nd byte period. The brief I2C interface protocol is shown in Figure 4.2.

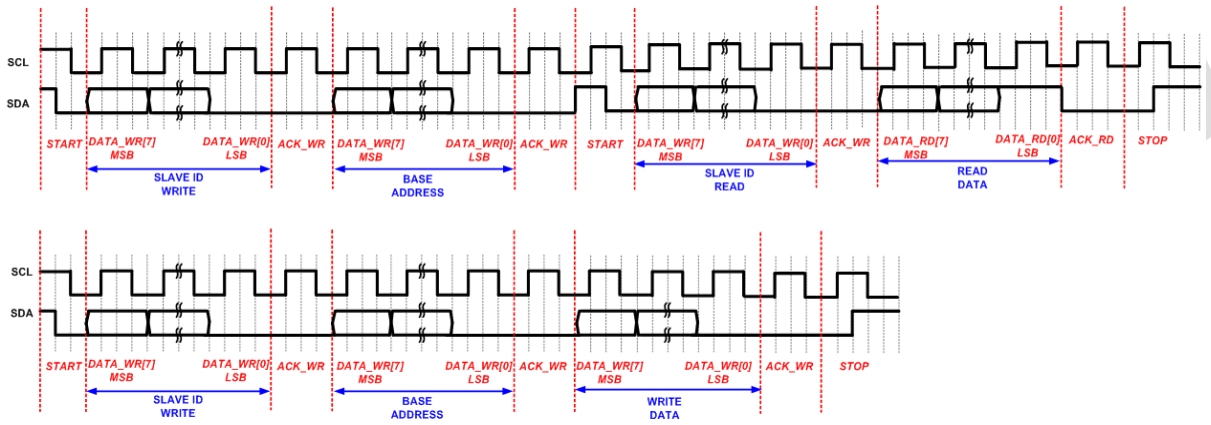


Figure 4.1 I2C Timing Diagram

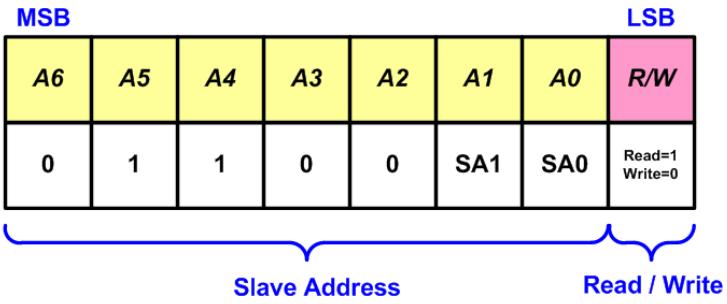


Figure 4.2 I2C Slave Address Configuration

Chapter 5
REGISTER DESCRIPTION

5.1 REGISTER ADDRESS

5.1.1 BANK0 Register(0x00~0x1F) : VIDEO_Format Control

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK0	0x00				- 1 -				PD_VCH_1	0x10
	0x01				- 1 -				PD_VCH_2	0x10
	0x02				- 1 -				PD_VCH_3	0x10
	0x03				- 1 -				PD_VCH_4	0x10
	0x04					SD_MD_1				0x00
	0x05					SD_MD_2				0x00
	0x06					SD_MD_3				0x00
	0x07					SD_MD_4				0x00
	0x08					AHD_MD_1				0x03
	0x09					AHD_MD_2				0x03
	0x0A					AHD_MD_3				0x03
	0x0B					AHD_MD_4				0x03
	0x0C	- 0x00 -								0x00
	0x0D	- 0x00 -								0x00
	0x0E	- 0x00 -								0x00
	0x0F	- 0x00 -								0x00
	0x10		BSF_MODE_1							0x00
	0x11		BSF_MODE_2							0x00
	0x12		BSF_MODE_3							0x00
	0x13		BSF_MODE_4							0x00
	0x14				FLD_INV_1	CHID_VIN1				0x00
	0x15				FLD_INV_2	CHID_VIN2				0x01
	0x16				FLD_INV_3	CHID_VIN3				0x00
	0x17				FLD_INV_4	CHID_VIN4				0x01
	0x18				EX_CBAR_ON_1	NOVID_DET_B_1				0x03
	0x19				EX_CBAR_ON_2	NOVID_DET_B_2				0x03
	0x1A				EX_CBAR_ON_3	NOVID_DET_B_3				0x03
	0x1B				EX_CBAR_ON_4	NOVID_DET_B_4				0x03
	0x1C	DATA_OUT_MODE_1				BGDCOL_1				0x18
	0x1D	DATA_OUT_MODE_2				BGDCOL_2				0x18
	0x1E	DATA_OUT_MODE_3				BGDCOL_3				0x18
	0x1F	DATA_OUT_MODE_4				BGDCOL_4				0x18

5.1.2 BANK0 Register(0x20~0x37) : Y_Control

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK0	0x20	BRIGHTNESS_1								0x00
	0x21	BRIGHTNESS_2								0x00
	0x22	BRIGHTNESS_3								0x00
	0x23	BRIGHTNESS_4								0x00
	0x24	CONTRAST_1								0x8C
	0x25	CONTRAST_2								0x8C
	0x26	CONTRAST_3								0x8C
	0x27	CONTRAST_4								0x8C
	0x28	BLACK_LEVEL_1								0x80
	0x29	BLACK_LEVEL_2								0x80
	0x2A	BLACK_LEVEL_3								0x80
	0x2B	BLACK_LEVEL_4								0x80
	0x2C	H_SHARPNESS_1				V_SHARPNESS_1				0x90
	0x2D	H_SHARPNESS_2				V_SHARPNESS_2				0x90
	0x2E	H_SHARPNESS_3				V_SHARPNESS_3				0x90
	0x2F	H_SHARPNESS_4				V_SHARPNESS_4				0x90
	0x30					Y_PEAK_MODE_1				0x00
	0x31					Y_PEAK_MODE_2				0x00
	0x32					Y_PEAK_MODE_3				0x00
	0x33					Y_PEAK_MODE_4				0x00
	0x34					Y_FIR_MODE_1				0x00
	0x35					Y_FIR_MODE_2				0x00
	0x36					Y_FIR_MODE_3				0x00
	0x37					Y_FIR_MODE_4				0x00

5.1.3 BANK0 Register(0x40~0x5F) : C_Control

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK0	0x40	HUE_1								0xFF
	0x41	HUE_2								0xFF
	0x42	HUE_3								0xFF
	0x43	HUE_4								0xFF
	0x44	U_GAIN_1								0x10
	0x45	U_GAIN_2								0x10
	0x46	U_GAIN_3								0x10
	0x47	U_GAIN_4								0x10
	0x48	V_GAIN_1								0x10
	0x49	V_GAIN_2								0x10
	0x4A	V_GAIN_3								0x10
	0x4B	V_GAIN_4								0x10
	0x4C	U_OFFSET_1								0xF6
	0x4D	U_OFFSET_2								0xF6
	0x4E	U_OFFSET_3								0xF6
	0x4F	U_OFFSET_4								0xF6
	0x50	V_OFFSET_1								0xF4
	0x51	V_OFFSET_2								0xF4
	0x52	V_OFFSET_3								0xF4
	0x53	V_OFFSET_4								0xF4
	0x58	SATURATION_1								0x80
	0x59	SATURATION_2								0x80
	0x5A	SATURATION_3								0x80
	0x5B	SATURATION_4								0x80
	0x5C	PAL_CM_OFF_1			COLOROFF_1	C_KILL_1				0x82
	0x5D	PAL_CM_OFF_2			COLOROFF_2	C_KILL_2				0x82
	0x5E	PAL_CM_OFF_3			COLOROFF_3	C_KILL_3				0x82
	0x5F	PAL_CM_OFF_4			COLOROFF_4	C_KILL_4				0x82

5.1.4 BANK0 Register(0x60~0x7F) : SYNC_Control

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK0	0x60				Y_DELAY_1					0x10
	0x61				Y_DELAY_2					0x10
	0x62				Y_DELAY_3					0x10
	0x63				Y_DELAY_4					0x10
	0x64	DF_CDELAY_1				DF_YDELAY_1				0x06
	0x65	DF_CDELAY_2				DF_YDELAY_2				0x06
	0x66	DF_CDELAY_3				DF_YDELAY_3				0x06
	0x67	DF_CDELAY_4				DF_YDELAY_4				0x06
	0x68	H_DELAY_1								0x80
	0x69	H_DELAY_2								0x80
	0x6A	H_DELAY_3								0x80
	0x6B	H_DELAY_4								0x80
	0x6C				HBLK_MSB_1	H_DLY_MSB_1				0x00
	0x6D				HBLK_MSB_2	H_DLY_MSB_2				0x00
	0x6E				HBLK_MSB_3	H_DLY_MSB_3				0x00
	0x6F				HBLK_MSB_4	H_DLY_MSB_4				0x00
	0x70	V_DELAY_1								0x9E
	0x71	V_DELAY_2								0x9E
	0x72	V_DELAY_3								0x9E
	0x73	V_DELAY_4								0x9E
	0x74	HBLK_END_1								0x00
	0x75	HBLK_END_2								0x00
	0x76	HBLK_END_3								0x00
	0x77	HBLK_END_4								0x00
	0x78	VBLK_END_1								0x22
	0x79	VBLK_END_2								0x22
	0x7A	VBLK_END_3								0x22
	0x7B	VBLK_END_4								0x22
	0x7C	HZOOM_ON_1				ZOOM_DTO_1				0x03
	0x7D	HZOOM_ON_2				ZOOM_DTO_2				0x03
	0x7E	HZOOM_ON_3				ZOOM_DTO_3				0x03
	0x7F	HZOOM_ON_4				ZOOM_DTO_4				0x03

5.1.5 BANK0 Register(0xA4~0xB5) : STATUS

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK0	0xA4				MOTION_1				NOVID_1	Read
	0xA5				MOTION_2				NOVID_2	Read
	0xA6				MOTION_3				NOVID_3	Read
	0xA7				MOTION_4				NOVID_4	Read
	0xA8								COAX_RX_DONE_1	Read
	0xA9								COAX_RX_DONE_2	Read
	0xAA								COAX_RX_DONE_3	Read
	0xAB								COAX_RX_DONE_4	Read
	0xB0					NOVID_4B	NOVID_3B	NOVID_2B	NOVID_1B	Read
	0xB1					MOTION_4B	MOTION_3B	MOTION_2B	MOTION_1B	Read
	0xB2					COAX_RX_DONE_4B	COAX_RX_DONE_3B	COAX_RX_DONE_2B	COAX_RX_DONE_1B	Read
	0xB4	RD_STATE_CLR			STATE_HOLD					0x90
	0xB5				- 0 -	IRQ_INV	IRQ_SEL			0x00

5.1.6 BANK0 Register(0xD0~0xF5) : STATUS

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK0	0xD0								AGC_LOCK_1	Read
	0xD1								AGC_LOCK_2	Read
	0xD2								AGC_LOCK_3	Read
	0xD3								AGC_LOCK_4	Read
	0xD4								CMP_LOCK_1	Read
	0xD5								CMP_LOCK_2	Read
	0xD6								CMP_LOCK_3	Read
	0xD7								CMP_LOCK_4	Read
	0xD8								H_LOCK_1	Read
	0xD9								H_LOCK_2	Read
	0xDA								H_LOCK_3	Read
	0xDB								H_LOCK_4	Read
	0xDC								BW_1	Read
	0xDD								BW_2	Read
	0xDE								BW_3	Read
	0xDF								BW_4	Read
	0xF4	DEV_ID								Read
	0xF5	REV_ID								Read

5.1.7 BANK1 Register(0x97~0xB3) : IP Power Down & MPP

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK1	0x97					CH_RST4	CH_RST3	CH_RST2	CH_RST1	0x0F
	0x98					PD_DEC4	PD_DEC3	PD_DEC2	PD_DEC1	0x00
	0xA8	MPP_TST_SEL1								0x00
	0xA9	MPP_TST_SEL2								0x00
	0xAA	MPP_TST_SEL3								0x00
	0xAB	MPP_TST_SEL4								0x00
	0xB1					MPP4_DIR	MPP3_DIR	MPP2_DIR	MPP1_DIR	0x00
	0xB3					MPP4_INV	MPP3_INV	MPP2_INV	MPP1_INV	0x00

5.1.8 BANK1 Register(0xC0~0xD0) : OUTPUT PORT

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK1	0xC0	VPORT_1_SEQ2				VPORT_1_SEQ1				0x00
	0xC1	VPORT_1_SEQ4				VPORT_1_SEQ3				0x00
	0xC2	VPORT_2_SEQ2				VPORT_2_SEQ1				0x11
	0xC3	VPORT_2_SEQ4				VPORT_2_SEQ3				0x11
	0xC4	VPORT_3_SEQ2				VPORT_3_SEQ1				0x22
	0xC5	VPORT_3_SEQ4				VPORT_3_SEQ3				0x22
	0xC6	VPORT_4_SEQ2				VPORT_4_SEQ1				0x33
	0xC7	VPORT_4_SEQ4				VPORT_4_SEQ3				0x33
	0xC8			VCLK_1_EN	VDO_1_EN	VPORT_1_CH_OUT_SEL				0x30
	0xC9			VCLK_2_EN	VDO_2_EN	VPORT_2_CH_OUT_SEL				0x30
	0xCA			VCLK_3_EN	VDO_3_EN	VPORT_3_CH_OUT_SEL				0x30
	0xCB			VCLK_4_EN	VDO_4_EN	VPORT_4_CH_OUT_SEL				0x30
	0xCC		VPORT_1_OCLK_SEL			VPORT_1_OCLK _DLY_SEL				0x60
	0xCD		VPORT_2_OCLK_SEL			VPORT_2_OCLK _DLY_SEL				0x60
	0xCE		VPORT_3_OCLK_SEL			VPORT_3_OCLK _DLY_SEL				0x60
	0xCF		VPORT_4_OCLK_SEL			VPORT_4_OCLK _DLY_SEL				0x60
	0xD0	- 0x0 -				OUT_DATA_4 _INV	OUT_DATA_3 _INV	OUT_DATA_2 _INV	OUT_DATA_1 _INV	0x00

5.1.9 BANK2~3 Register(0x00~0x1F / 0x80~0x9F) : COAXIAL CH1~4

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK2/3	0x00	CH1_BAUD								0x37
	0x02	CH1_PELCO_BAUD								0x1B
	0x03	CH1_BL_TXST[7:0]								0x05
	0x04	CH1_BL_TXST[15:8]								0x00
	0x05					CH1_ACT_LEN				0x00
	0x07	CH1_PELCO_TXST[7:0]								0x00
	0x08	CH1_PELCO_TXST[15:8]								0x00
	0x09				CH1_COAX_SW_RST	CH1_CNT_MODE			CH1_TX_START	0x00
	0x0A				CH1_TX_BYTE_LENGTH					0x08
	0x0B	CH1_PELCO_8BIT	-RESERVED-		CH1_LINE_8BIT	-RESERVED-	CH1_PACKET_MODE			0x06
	0x0C								CH1_PELCO_CTEN	0x00
	0x0D	CH1_BL_HSP[7:0]								0x46
	0x0E	CH1_BL_HSP[15:8]								0x00
	0x0F								CH1_PELCO_SHOT	0x00
	0x10	CH1_TX_DATA_01								0xAA
	0x11	CH1_TX_DATA_02								0x1C
	0x12	CH1_TX_DATA_03								0x18
	0x13	CH1_TX_DATA_04								0xFF
	0x14	CH1_TX_DATA_05								0xAA
	0x15	CH1_TX_DATA_06								0x3C
	0x16	CH1_TX_DATA_07								0xFF
	0x17	CH1_TX_DATA_08								0xFF
	0x18	CH1_TX_DATA_09								0xAA
	0x19	CH1_TX_DATA_10								0x1B
	0x1A	CH1_TX_DATA_11								0x00
	0x1B	CH1_TX_DATA_12								0x00
	0x1C	CH1_TX_DATA_13								0xAA
	0x1D	CH1_TX_DATA_14								0x3B
	0x1E	CH1_TX_DATA_15								0x00
	0x1F	CH1_TX_DATA_16								0x00

5.1.10 BANK2~3 Register(0x20~0x5D / 0xA0~0xDD) : COAXIAL CH1~4

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK2/3	0x20	CH1_PELCO_TXDAT_01								0x00
	0x21	CH1_PELCO_TXDAT_02								0x00
	0x22	CH1_PELC O_TXDAT_03								0x00
	0x23	CH1_PELCO_TXDAT_04								0x00
	0x2C								CH1_VSO_INV	0x00
	0x2D								CH1_HSO_INV	0x00
	0x2F								CH1_ EVEN_SUM	0x01
	0x3A								CH1_CLEAN	0x00
	0x40	CH1_RX_LINE00								Read
	0x41									
	0x42									
	0x43									
	0x44									
	0x45	CH1_RX_LINE01								Read
	0x46									
	0x47									
	0x48									
	0x49									
	0x4A	CH1_RX_LINE02								Read
	0x4B									
	0x4C									
	0x4D									
	0x4E									
	0x50	CH1_PELCO_8_00								Read
	0x51	CH1_PELCO_8_01								
	0x52	CH1_PELCO_8_02								
	0x53	CH1_PELCO_8_03								
	0x54	CH1_PELCO_8_04								
	0x55	CH1_PELCO_8_05								
	0x56	CH1_PELCO_8_06								
	0x57	CH1_PELCO_8_07								
	0x5C								CH1_ RX_DONE	Read
	0x5D	CH1_RX_COAX_DUTY								Read

5.1.11 BANK2~3 Register(0x60~0x79 / 0xE0~0xF9) : COAXIAL CH1~4

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK2/3	0x60	CH1_DEVICE_ID								0x00
	0x62	CH1_RX_AREA								0x00
	0x63				CH1_DELAY_ON				CH1_COMM_ON	0x00
	0x64	CH1_DELAY_CNT								0x00
	0x65								CH1_MSB	0x00
	0x66	CH1_A_DUTY_ON	-RESERVED-							0x00
	0x67								CH1_INT_MODE	0x00
	0x68	CH1_RX_SZ								0x00
	0x69	CH1_M_DUTY								0x00
	0x6A	CH1_RX_START_POSITION								0x00
	0x6C 0x6D 0x6E 0x6F 0x70	CH1_RX_LINE_03								Read
	0x71 0x72 0x73 0x74 0x75	CH1_RX_LINE_04								Read
	0x76 0x77 0x78 0x79 0x7A	CH1_RX_LINE_05								Read

5.1.12 BANK4 Register(0x00~0x17) : MOTION

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK4	0x00	-RESERVED-				CH1_MOTION_PIC		-RESERVED-	CH1_MOTION_OFF	0x0D
	0x01	CH1_MOD_TSEN								0x60
	0x02	-RESERVED-					CH1_MOD_PSEN			0x23
	0x07	-RESERVED-				CH2_MOTION_PIC		-RESERVED-	CH2_MOTION_OFF	0x0D
	0x08	CH2_MOD_TSEN								0x60
	0x09	-RESERVED-					CH2_MOD_PSEN			0x23
	0x0E	-RESERVED-				CH3_MOTION_PIC		-RESERVED-	CH3_MOTION_OFF	0x0D
	0x0F	CH3_MOD_TSEN								0x60
	0x10	-RESERVED-					CH3_MOD_PSEN			0x23
	0x15	-RESERVED-				CH4_MOTION_PIC		-RESERVED-	CH4_MOTION_OFF	0x0D
	0x16	CH4_MOD_TSEN								0x60
	0x17	-RESERVED-					CH4_MOD_PSEN			0x23

5.1.13 BANK20 Register(0x00~0x1C) : ARBITER

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK20	0x00	CH4_ARB_EN	CH3_ARB_EN	CH2_ARB_EN	CH1_ARB_EN	CH4_MEM_EN	CH3_MEM_EN	CH2_MEM_EN	CH1_MEM_EN	0x00
	0x01	CH4_SCALE_MODE		CH3_SCALE_MODE		CH2_SCALE_MODE		CH1_SCALE_MODE		0x00
	0x02	CH4_TEST_MODE	CH3_TEST_MODE	CH2_TEST_MODE	CH1_TEST_MODE	- 0 -				0x00
	0x0D	- 0 -							ARB_32BIT	0x01
	0x0F	MIPI_CH4_VIDEO_TYPE		MIPI_CH3_VIDEO_TYPE		MIPI_CH2_VIDEO_TYPE		MIPI_CH1_VIDEO_TYPE		0x00
	0x10	CH2_RD_P_MODE				CH1_RD_P_MODE				0x00
	0x11	CH4_RD_P_MODE				CH3_RD_P_MODE				0x00
	0x12	CH1_RD_PACKET[7:0]								0x00
	0x13	CH1_RD_PACKET[15:8]								0x00
	0x14	CH2_RD_PACKET[7:0]								0x00
	0x15	CH2_RD_PACKET[15:8]								0x00
	0x16	CH3_RD_PACKET[7:0]								0x00
	0x17	CH3_RD_PACKET[15:8]								0x00
	0x18	CH4_RD_PACKET[7:0]								0x00
	0x19	CH4_RD_PACKET[15:8]								0x00
	0x1B					CH4_EMB_EN	CH3_EMB_EN	CH2_EMB_EN	CH1_EMB_EN	0x00
	0x1C	CH4_EMB_ARB		CH3_EMB_ARB		CH2_EMB_ARB		CH1_EMB_ARB		0x00

5.1.14 BANK20 Register(0x20~0x3B) : ARBITER

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK20	0x20	CH2_RD_T_MODE				CH1_RD_T_MODE				0x00
	0x21	CH4_RD_T_MODE				CH3_RD_T_MODE				0x00
	0x22	CH1_RD_LINE_TOTAL[7:0]								0x00
	0x23	CH1_RD_LINE_TOTAL[15:8]								0x00
	0x24	CH2_RD_LINE_TOTAL[7:0]								0x00
	0x25	CH2_RD_LINE_TOTAL[15:8]								0x00
	0x26	CH3_RD_LINE_TOTAL[7:0]								0x00
	0x27	CH3_RD_LINE_TOTAL[15:8]								0x00
	0x28	CH4_RD_LINE_TOTAL[7:0]								0x00
	0x29	CH4_RD_LINE_TOTAL[15:8]								0x00
	0x30					MIPI_T_MODE				0x00
	0x32	SOF_PERIOD[15:8]								0x00
	0x33	SOF_PERIOD[7:0]								0x00
	0x34	EOF_PERIOD[15:8]								0x00
	0x35	EOF_PERIOD[7:0]								0x00
	0x36	SOL_PERIOD[15:8]								0x00
	0x37	SOL_PERIOD[7:0]								0x00
	0x38	EOL_PERIOD[15:8]								0x00
	0x39	EOL_PERIOD[7:0]								0x00
	0x3A	CH4_HCNT_ERR	CH3_HCNT_ERR	CH2_HCNT_ERR	CH1_HCNT_ERR	CH4_ARB_NO_OPT	CH3_ARB_NO_OPT	CH2_ARB_NO_OPT	CH1_ARB_NO_OPT	0x00
	0x3B					SWITCH_OPT				0x00

5.1.15 BANK20 Register(0x40~0x5F) : ARBITER

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK20	0x40				ARB_VFC_STABLE_RESET_OPT				SW_RST	0x00
	0x41	CH2_COLI_OPT				CH1_COLI_OPT				0x00
	0x42	CH4_COLI_OPT				CH3_COLI_OPT				0x00
	0x43					CH4_COLI_CLR	CH3_COLI_CLR	CH2_COLI_CLR	CH1_COLI_CLR	0x00
	0x44	CH4_RD_FRM_CLR	CH3_RD_FRM_CLR	CH2_RD_FRM_CLR	CH1_RD_FRM_CLR	CH4_WR_FRM_CLR	CH3_WR_FRM_CLR	CH2_WR_FRM_CLR	CH1_WR_FRM_CLR	0x00
	0x50	CH1_WR_FRAME_CNT[15:8]								0x00
	0x51	CH1_WR_FRAME_CNT[7:0]								0x00
	0x52	CH1_RD_FRAME_CNT[15:8]								0x00
	0x53	CH1_RD_FRAME_CNT[7:0]								0x00
	0x54	CH2_WR_FRAME_CNT[15:8]								0x00
	0x55	CH2_WR_FRAME_CNT[7:0]								0x00
	0x56	CH2_RD_FRAME_CNT[15:8]								0x00
	0x57	CH2_RD_FRAME_CNT[7:0]								0x00
	0x58	CH3_WR_FRAME_CNT[15:8]								0x00
	0x59	CH3_WR_FRAME_CNT[7:0]								0x00
	0x5A	CH3_RD_FRAME_CNT[15:8]								0x00
	0x5B	CH3_RD_FRAME_CNT[7:0]								0x00
	0x5C	CH4_WR_FRAME_CNT[15:8]								0x00
	0x5D	CH4_WR_FRAME_CNT[7:0]								0x00
	0x5E	CH4_RD_FRAME_CNT[15:8]								0x00
	0x5F	CH4_RD_FRAME_CNT[7:0]								0x00

5.1.16 BANK20 Register(0x60~0x70) : ARBITER

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK20	0x60						CH1_H_pack_size[10:8]			0x00
	0x61	CH1_H_pack_size[7:0]								0x00
	0x62						CH2_H_pack_size[10:8]			0x00
	0x63	CH2_H_pack_size[7:0]								0x00
	0x64						CH3_H_pack_size[10:8]			0x00
	0x65	CH3_H_pack_size[7:0]								0x00
	0x66						CH4_H_pack_size[10:8]			0x00
	0x67	CH4_H_pack_size[7:0]								0x00
	0x68	CH1_coli_cnt								0x00
	0x69	CH2_coli_cnt								0x00
	0x6A	CH3_coli_cnt								0x00
	0x6B	CH4_coli_cnt								0x00
	0x70					CH4_coli_out	CH3_coli_out	CH2_coli_out	CH1_coli_out	0x00

5.1.17 BANK21 Register(0x07~0x1C) : MIPI TX

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK21	0x07	MIPI_TX_PHY_PWR_DOWN	MIPI_TX_PHY_REF_SEL			MIPI_TX_LANES_ACTIVE		MIPI_TX_SYS_CORE_RDY	MIPI_TX_SERIAL_IF_EN	0x00
	0x08	MIPI_TX_HRES_IN	MIPI_TX_LP_SLEW_IN			MIPI_TX_CONT_TX_CLK	MIPI_TX_RESTART_EN	MIPI_TX_STANDBY_EOF	MIPI_TX_STANDBY_EN	0x00
	0x0A	- 0 -		MIPI_TX_DATA_TYPE_UD						0x00
	0x0B	- 0x00 -								0x00
	0x0E							MIPI_TX_CHAN_NUM		0x00
	0x0F				- 0 -			MIPI_TX_FRAME_CNT_RST	MIPI_TX_FRAME_CNT_EN	0x00
	0x10			MIPI_TX_T_HS_ZERO						0x12
	0x11					MIPI_TX_T_HS_PREPARE				0x07
	0x12				MIPI_TX_T_HS_TRAIL					0x0A
	0x13			MIPI_TX_T_HS_EXIT						0x10
	0x14		MIPI_TX_T_CLK_ZERO							0x29
	0x15					MIPI_TX_T_CLK_PREPARE				0x06
	0x16				MIPI_TX_T_CLK_TRAIL					0x0A
	0x17			MIPI_TX_T_CLK_PRE						0x02
	0x18			MIPI_TX_T_CLK_POST						0x10
	0x19			MIPI_TX_T_LPX						0x08
	0x1A		MIPI_TX_T_WAKE_UP							0x13
	0x1B		MIPI_TX_T_INIT							0x10
	0x1C			MIPI_TX_T_BGAP						0x0D

5.1.18 BANK21 Register(0x29~0x46) : MIPI TX

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.
BANK21	0x29	ODD_MANUAL_FRAME_CNT[7:0]								0x00
	0x2A	ODD_MANUAL_FRAME_CNT[15:8]								0x00
	0x2B	EVEN_MANUAL_FRAME_CNT[7:0]								0x00
	0x2C	EVEN_MANUAL_FRAME_CNT[15:8]								0x00
	0x2D								- 1 -	0x01
	0x2E								MIPI_CH_ID_TYPE	0x00
	0x2F								MIPI_BYTE_CNT_TYPE	0x00
	0x30	MIPI_TX_LINE_BYTE_CNT_CH1[7:0]								0x00
	0x31	MIPI_TX_LINE_BYTE_CNT_CH1[15:8]								0x0F
	0x32	MIPI_TX_LINE_BYTE_CNT_CH2[7:0]								0x00
	0x33	MIPI_TX_LINE_BYTE_CNT_CH2[15:8]								0x0F
	0x34	MIPI_TX_LINE_BYTE_CNT_CH3[7:0]								0x00
	0x35	MIPI_TX_LINE_BYTE_CNT_CH3[15:8]								0x0F
	0x36	MIPI_TX_LINE_BYTE_CNT_CH4[7:0]								0x00
	0x37	MIPI_TX_LINE_BYTE_CNT_CH4[15:8]								0x0F
	0x38			MIPI_TX_DATA_TYPE_CH1						0x1E
	0x39			MIPI_TX_DATA_TYPE_CH2						0x1E
	0x3A			MIPI_TX_DATA_TYPE_CH3						0x1E
	0x3B			MIPI_TX_DATA_TYPE_CH4						0x1E
	0x3C	CH4_DATA_TYPE_OPT		CH3_DATA_TYPE_OPT		CH2_DATA_TYPE_OPT		CH1_DATA_TYPE_OPT		0x00
	0x3E		MIPI_CH2_FRAME_OPT				MIPI_CH1_FRAME_OPT			0x00
	0x3F		MIPI_CH4_FRAME_OPT				MIPI_CH3_FRAME_OPT			0x00
	0x44				MIPI_SRC_CLK_INV			- 0 -	- 0 -	0x00
	0x45	MIPI_BYTE_CLK_INV				MIPI_DATA_CLK_INV		MIPI_DATA_CLK_SEL		0x02
	0x46	- 0 -			- 0 -				PD_MIPI_CLK	0x00

5.2 Register Description

5.2.1 VIDEO Registers

- **Registers to Power Down Mode**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x00	PD_VCH1	[0]	0x0	**Power Down for Channel x** **:** Power Down for Channel x AFE. (Active High, Video AFE Power Down is high) **0 :** Normal Operation **1 :** Power Down
	0x01	PD_VCH2			
	0x02	PD_VCH3			
	0x03	PD_VCH4			

- **Registers to Select SD Mode**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x04	SD_MD_1	[3:0]	0x00	**SD_MD** **:** SD Mode Selection. **0:** Default **E:** SD_NTSC MODE **F:** SD_PAL MODE **Etc.:** Don't use
	0x05	SD_MD_2			
	0x06	SD_MD_3			
	0x07	SD_MD_4			

- **Registers to Select AHD Mode**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x08	AHD_MD_1	[3:0]	0x03	**AHD_MD_x** **:** AHD Mode Selection. **0:** SD Mode **2:** 1080 30P MODE **3:** 1080 25P MODE **4:** 720 60P MODE **5:** 720 50P MODE **C:** 720 30P MODE **D:** 720 25P MODE **Etc.:** Don't use
	0x09	AHD_MD_2			
	0x0A	AHD_MD_3			
	0x0B	AHD_MD_4			

- **Registers to Control Comb Filter**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x10	BSF_MODE_1	[6:0]	0x00	**BSF_MODE_x :** Selects the filter to make primary separation of the brightness and color signals. (x = channel 1~4) **00 :** AHD MODE **A0 :** SD MODE **DD :** PAL MODE **60 :** Manual MODE
	0x11	BSF_MODE_2			
	0x12	BSF_MODE_3			
	0x13	BSF_MODE_4			

Registers to Control Field Polarity

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x14	FLD_INV_4	[7]	0	**FLD_INV_x** : Field Polarity Control (x = channel 1~4) 0 : not Inversion 1 : Inversion
	0x15	FLD_INV_3	[6]		
	0x16	FLD_INV_2	[5]		
	0x17	FLD_INV_1	[4]		

Registers to Control Channel ID

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x14	CHID_VIN1	[3:0]	0x00	**CHID_VIN_x** : Register to put CHANNEL ID to distinguish channel. (0x0~0xF) (x = channel 1~4)
	0x15	CHID_VIN2		0x01	
	0x16	CHID_VIN3		0x00	
	0x17	CHID_VIN4		0x01	

Registers to Control TEST

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x18	EX_CBAR_ON_1	[4]	0x0	**EX_CBAR_ON** : When No Video , External Color Bar On/Off Control **0 :** External Color Bar Off **1 :** External Color Bar On
	0x19	EX_CBAR_ON_2			
	0x1A	EX_CBAR_ON_3			
	0x1B	EX_CBAR_ON_4			

Registers to Control Sync Detection

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x18	NOVID_DET_B_1	[3:0]	0x3	**NOVID_DET_B_x** (x = channel 1~4) : Select Condition for No video detection, High Active. **0 :** If the input video is not detected sync, decision to NO Video **1 :** If width of detected sync is narrower than video standard, decision to NO Video **2 :** If Vertical sync don't exist, decision to NO Video **3 :** If the CLAMP is not stable, decision to NO Video
	0x19	NOVID_DET_B_2			
	0x1A	NOVID_DET_B_3			
	0x1B	NOVID_DET_B_4			

Registers to Control Data Out Mode

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x1C	DATA_OUT_MODE_1	[7:4]	0x1	**DATA_OUT_MODE_x** **:** It limits a level of output data, can change signals of Cb and Cr each. (x = channel 1~4) **0000** : Y(016~235), Cb(016~240), Cr(016~240) **0001** : Y(001~254), Cb(001~254), Cr(001~254) **0010** : Y(000~255), Cb(000~255), Cr(000~255) **0011** : Cb / Cr Change, 016~235 **0100** : Cb / Cr Change, 001~254 **0101** : Cb / Cr Kill, 016~235 **0110** : Cb / Cr Kill, 001~254 **Others** : Background color output
	0x1D	DATA_OUT_MODE_2			
	0x1E	DATA_OUT_MODE_3			
	0x1F	DATA_OUT_MODE_4			

Registers to Control Back Ground Color

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x1C	BGDCOL_1	[3:0]	0x8	**BGDCOL_x** **:** When No-Video, Background Color is used. (x = channel 1~4) **0000** : Blue **0001** : White (75%) **0010** : Yellow **0011** : Cyan **0100** : Green **0101** : Magenta **0110** : Red **0111** : Blue **1000** : Black **1001** : Gray **1010** : Red (NEXTCHIP*) **1011** : Yellow (NEXTCHIP*) **1100** : Magenta (NEXTCHIP*) **1101** : Green (NEXTCHIP*) **1110** : Blue (NEXTCHIP*) **1111** : Cyan (NEXTCHIP*) *** These color information is exactly same as controllers provided by NEXTCHIP**
	0x1D	BGDCOL_2			
	0x1E	BGDCOL_3			
	0x1F	BGDCOL_4			

Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x20	BRIGHTNESS_1	[7:0]	0x00	**BRIGHTNESS_x :** Brightness control; DC level of the Luma signal is adjustable up to -128 ~ +127. BRIGHTNESS consists of 2's Complements. (x = channel 1~4) **00000001** : + 1 **01111111** : + 127 **10000000** : - 128 **11111111** : - 1
	0x21	BRIGHTNESS_2			
	0x22	BRIGHTNESS_3			
	0x23	BRIGHTNESS_4			

Registers to Control Contrast

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x24	CONTRAST_1	[7:0]	0x8C	**CONTRAST_x :** Contrast control, Gain level of the Luma signal is adjustable up to x2. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4) **00000000** : ≒ x 0 **01000000** : ≒ x 0.5 **10000000** : ≒ x 1 **11111111** : ≒ x 2
	0x25	CONTRAST_2			
	0x26	CONTRAST_3			
	0x27	CONTRAST_4			

Registers to Control Black Level

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x28	BLACK_LEVEL_1	[7:0]	0x80	**BLACK_LEVEL** **:** This represents the value, which is to be subtracted from Y that has passed the Comb Filter in order to remove Sync.
	0x29	BLACK_LEVEL_2			
	0x2A	BLACK_LEVEL_3			
	0x2B	BLACK_LEVEL_4			

Registers to Control Sharpness

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x2C	H_SHARPNESS_1	[7:4]	0x90	**H_SHARPNESS_x :** Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4) **0000** : x 0 **0100** : x 0.5 **1000** : x 1 **1111** : x 2
	0x2D	H_SHARPNESS_2			
	0x2E	H_SHARPNESS_3			
	0x2F	H_SHARPNESS_4			
	0x2C	V_SHARPNESS_1	[3:0]		**V_SHARPNESS_x :** Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4) **0000** : x 1 **0100** : x 2 **1000** : x 3 **1111** : x 4
	0x2D	V_SHARPNESS_2			
	0x2E	V_SHARPNESS_3			
	0x2F	V_SHARPNESS_4			

Registers to Control Peaking Filter

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x30	Y_PEAK_MODE_1	[3:0]	0x00	**Y_PEAK_MODE_x :** Y Peaking Filter control (x = channel 1~4) **0000** : 0dB **0001** : 2dB **0010** : 3.5dB **0011** : 6dB **0100 ~ 1111 :** Don't use
	0x31	Y_PEAK_MODE_2			
	0x32	Y_PEAK_MODE_3			
	0x33	Y_PEAK_MODE_4			

Registers to Control Low Pass Filter

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x34	Y_FIR_MODE_1	[3:0]	0x00	**Y_FIR_MODE_x :** Y Low Pass Filter control (x = channel 1~4) **0000** : bypass **0101** : 8MHz **0001** : 6MHz **0110** : 8.5MHz **0010** : 6.5MHz **1000** : 9.5MHz **0011** : 7MHz **0111** : 9MHz **0100** : 7.5MHz
	0x35	Y_FIR_MODE_2	[3:0]		
	0x36	Y_FIR_MODE_3	[3:0]		
	0x37	Y_FIR_MODE_4	[3:0]		

Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x40	HUE_1	[7:0]	0xFF	**HUE_x** : Color HUE Control Value (360°/256 per HUE Value 1 unit) (x = channel 1~4) **00000000** : 0° **01000000** : 90° **10000000** : 180° **11111111** : 360°
	0x41	HUE_2			
	0x42	HUE_3			
	0x43	HUE_4			
	0x44	U_GAIN_1	[7:0]	0x10	**U_GAIN_x** : U Gain Value (Adjustable up to x2) (x = channel 1~4) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x45	U_GAIN_2			
	0x46	U_GAIN_3			
	0x47	U_GAIN_4			
	0x48	V_GAIN_1	[7:0]	0x10	**V_GAIN_x** : V Gain Value (Adjustable up to x2) (x = channel 1~4) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x49	V_GAIN_2			
	0x4A	V_GAIN_3			
	0x4B	V_GAIN_4			
	0x4C	U_OFFSET_1	[7:0]	0xF6	**U_OFFSET_x** : U offset value is adjustable up to ± 7. U offset consists of 2's complements. (x = channel 1~4) **0001** : + 1 **0111** : + 7 **1000** : - 8 **1111** : - 1
	0x4D	U_OFFSET_2			
	0x4E	U_OFFSET_3			
	0x4F	U_OFFSET_4			
	0x50	V_OFFSET_1	[7:0]	0xF4	**V_OFFSET_x** : V offset value is adjustable up to ± 7. V offset consists of 2's complements. (x = channel 1~4) **0001** : + 1 **0111** : + 7 **1000** : - 8 **1111** : - 1
	0x51	V_OFFSET_2			
	0x52	V_OFFSET_3			
	0x53	V_OFFSET_4			
	0x58	SATURATION_1	[7:0]	0x80	**SATURATION_x** : Color Gain Value (Adjustable up to x2) (x = channel 1~4) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x59	SATURATION_2			
	0x5A	SATURATION_3			
	0x5B	SATURATION_4			

Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x5C	PAL_CM_OFF_1	[7]	0x1	**PAL_CM_OFF_x** (x = channel 1~4) : PAL Compensation On/Off. **0** : PAL Compensation applied when SD PAL Mode, **1** : PAL Compensation not applied when SD NTSC or AHD Mode.
	0x5D	PAL_CM_OFF_2			
	0x5E	PAL_CM_OFF_3			
	0x5F	PAL_CM_OFF_4			
	0x5C	COLOROFF_1	[4]	0x0	**COLOROFF_x** (x = channel 1~4) : COLOR OFF **0 :** Color ON **1 :** Color OFF
	0x5D	COLOROFF_2			
	0x5E	COLOROFF_3			
	0x5F	COLOROFF_4			
	0x5C	C_KILL_1	[3:0]	0x02	**C_KILL_x[3]** (x = channel 1~4) : Select to Color kill mode **0 :** Not Y/C separation **1 :** Color kill after Y/C separation **C_KILL_x[2:0]** (x = channel 1~4) : color kill control. **000 :** Burst Amplitude 10% Under & FSC Unlock **001 :** Burst Amplitude 5% Under & FSC Unlock **010 :** Burst Amplitude 10 % Under **011 :** Burst Amplitude 5% Under **100 :** Always color on **101 :** Always color on. **110 :** Always color off **111 :** Always color off
	0x5D	C_KILL_2			
	0x5E	C_KILL_3			
	0x5F	C_KILL_4			

Registers to Control Y_DELAY

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x60	Y_DELAY_1	[4:0]	0x10	**Y_DELAY_ ON_x** (x = channel 1~4) : Y DELAY Control, controllable between 0x00 ~ 0x1F.
	0x61	Y_DELAY_2			
	0x62	Y_DELAY_3			
	0x63	Y_DELAY_4			

Registers to Control Y/C DELAY

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x64	DF_YDELAY_1	[3:0]	0x06	**DF_YDELAY_x** (x = channel 1~4) : Y(Luminance) delay can be controlled between 0x0 ~ 0xF.
	0x65	DF_YDELAY_2			
	0x66	DF_YDELAY_3			
	0x67	DF_YDELAY_4			
	0x64	DF_CDELAY_4	[7:4]		**DF_CDELAY_x** (x = channel 1~4) : C(Chrominance) delay can be controlled between 0x0 ~ 0xF.
	0x65	DF_CDELAY_3			
	0x66	DF_CDELAY_2			
	0x67	DF_CDELAY_1			

Registers to Control Video Output Horizontal Timing

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x68	H_DELAY_1	[7:0]	0x80	**H_DELAY_x** : Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal. (x = channel 1~4)
	0x69	H_DELAY_2			
	0x6A	H_DELAY_3			
	0x6B	H_DELAY_4			
	0x6C	H_DLY_MSB_1	[3:0]	0x0	**HDLY_MSBS_0x** : H_DELAY MSB Register
	0x6D	H_DLY_MSB_2			
	0x6E	H_DLY_MSB_3			
	0x6F	H_DLY_MSB_4			
	0x6C	HBLK_MSB_1	[4]	0	**HBLK_MSB_x** (x = channel number) : Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed. HBLK_MSB_x is MSB Bit of Bank0 0x60~63.
	0x6D	HBLK_MSB_2			
	0x6E	HBLK_MSB_3			
	0x6F	HBLK_MSB_4			
	0x74	HBLK_END_1	[7:0]	0x00	**HBLK_END_x** (x = channel number) : Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed.
	0x75	HBLK_END_2			
	0x76	HBLK_END_3			
	0x77	HBLK_END_4			

Registers to Control Video Output Vertical Timing

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x70	V_DELAY_1	[7:0]	0x9E	**V_DELAY_x[7:6]** **:** Select to vblk_str_fld (x = channel 1~4) **00 : evenfld 01 : !evenfld 10 : 0 11 : 1** **V_DELAY_x[5]** **:** V_DELAY_x[4:0] Control Enable (x = channel 1~4) **V_DELAY_x[4:0] (When V_DELAY_x[5] = 1)** **:** Register to determine the Vertical start position of output image to Vsync extracted in analog input signal. (x = channel 1~4)
	0x71	V_DELAY_2			
	0x72	V_DELAY_3			
	0x73	V_DELAY_4			
	0x78	VBLK_END_1	[7:0]	0x22	**VBLK_END_x[7:6]** **:** Select to vblk_end_fld (x = channel 1~4) **00 : evenfld 01 : !evenfld 10 : 0 11 : 1** **VBLK_END_x[5]** **:** VBLK_END_x[4:0] Control Enable (x = channel 1~4) **VBLK_END_x[4:0] (When VBLK_END_x[5] = 1)** **:** Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then the Active region is changed. (x = channel 1~4)
	0x79	VBLK_END_2			
	0x7A	VBLK_END_3			
	0x7B	VBLK_END_4			

Registers to Control Horizontal ZOOM

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0x7C	HZOOM_ON_1	[7]	0	**HZOOM_ON_x** (x = channel number) **:** This Register can be turned on or off Horizontal ZOOM. **0:** ZOOM OFF **1:** ZOOM ON
	0x7D	HZOOM_ON_2			
	0x7E	HZOOM_ON_3			
	0x7F	HZOOM_ON_4			
	0x7C	ZOOM_DTO_1	[3:0]	0x03	**ZOOM_DTO _x** (x = channel 1~4) **:** H_ZOOM Area setting
	0x7D	ZOOM_DTO_2			
	0x7E	ZOOM_DTO_3			
	0x7F	ZOOM_DTO_4			

Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0xA4	NOVID_1	[4]	Read	**NOVID_0x** : Each Channel Video Decoder No Video detection Status. (x = Channel number) **0** : On Video **1** : No Video
	0xA5	NOVID_2			
	0xA6	NOVID_3			
	0xA7	NOVID_4			
	0xA4	MOTION_1	[0]	Read	**MOTION_0x** : Each Channel Motion detection Status (x = Channel number) **0** : No MOTION **1** : On MOTION
	0xA5	MOTION_2			
	0xA6	MOTION_3			
	0xA7	MOTION_4			

Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0xA8	COAX_RX_DONE_1	[0]	Read	**COAX_RX_DONE_x** : COAXIAL_RX_Detecting Status (x = channel number) **0** : No Detecting **1** : COAXIAL_RX_Detecting
	0xA9	COAX_RX_DONE_2			
	0xAA	COAX_RX_DONE_3			
	0xAB	COAX_RX_DONE_4			

Registers to Status Registers (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0xB0	NOVID_1B	[0]	Read	**NOVID_0xB** : Each Channel Video Decoder No Video detection Status with HOLD option (x = Channel number) **0** : On Video **1** : No Video
		NOVID_2B	[1]		
		NOVID_3B	[2]		
		NOVID_4B	[3]		
	0xB1	MOTION_1B	[0]		**MOTION_0xB** : Each Channel Motion detection Status with HOLD option (x = Channel number) **0** : No MOTION **1** : On MOTION
		MOTION_2B	[1]		
		MOTION_3B	[2]		
		MOTION_4B	[3]		
	0xB2	COAX_RX_DONE_1B	[0]		**COAX_RX_DONE_B** : COAXIAL_RX_Detecting Status with HOLD option (x = channel number) **0** : No Detecting **1** : COAXIAL_RX_Detecting
		COAX_RX_DONE_2B	[1]		
		COAX_RX_DONE_3B	[2]		
		COAX_RX_DONE_4B	[3]		

Registers to Interrupt clear for Status Registers

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0xB4	RD_STATE_CLR	[7]	0x90	**RD_STATE_CLR** **:** Interrupt clear condition selection **0** : Interrupt clear when BANK0, 0xB2 Addr Register Read **1** : Interrupt clear when BANK0, 0xA8~0xAB / B2 Addr Register Read
		STATE_HOLD	[4]		**STATE_HOLD** **:** Interrupt Hold condition selection **0** : No Hold Option, State is Real Time update. **1** : Hold Option operation. State is Hold until cleared

Registers to Control IRQ

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0xB5	IRQ_INV	[3]	0x00	**IRQ_INV** **:** IRQ pin output signal inversion **0** : Not Inversion **1** : Inversion
		IRQ_SEL	[2:0]		**IRQ_SEL** **:** Select IRQ pin output signals selection **0** : **0 (Zero)** **1** : interrupt request by the No video detection **3** : interrupt request by the Motion detection **Others** : BNCO

Registers to Show Locking Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0xD0	AGC_LOCK_1	[0]	Read	**AGC_LOCK_x** : Video AGC Locking Status (x = channel number) **0** : No Locking **1** : Locking
	0xD1	AGC_LOCK_2			
	0xD2	AGC_LOCK_3			
	0xD3	AGC_LOCK_4			
	0xD4	CMP_LOCK_1	[0]	Read	**CMP_LOCK_x** : Video CLAMP Locking status (x = channel number) **0** : No Locking **1** : Locking
	0xD5	CMP_LOCK_2			
	0xD6	CMP_LOCK_3			
	0xD7	CMP_LOCK_4			
	0xD8	H_LOCK_1	[0]	Read	**H_LOCK_x** : Video Horizontal Locking status (x = channel number) **0** : No Locking **1** : Locking
	0xD9	H_LOCK_2			
	0xDA	H_LOCK_3			
	0xDB	H_LOCK_4			
	0xDC	BW_1	[0]	Read	**BW_x** : Black and White Detection status (x = channel number) **0** : Color Mode **1** : B/W Mode
	0xDD	BW_2			
	0xDE	BW_3			
	0xDF	BW_4			

Registers to Show Chip Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
0	0xF4	DEV_ID	[7:0]	Read	**DEV_ID** : It shows Device ID (N4 = 0xB0)
	0xF5	REV_ID	[7:0]	Read	**REV_ID** : It shows Revision ID (0x00)

5.2.2 PD and MPP Registers

- **Registers to Control Each Channel Reset**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0x97	CH_RST_4	[3]	0x0F	**CH_RST_x** : Each Video Channel Reset (x = channel number) **0** : Channel_x Reset **1** : Channel_x On
		CH_RST_3	[2]		
		CH_RST_2	[1]		
		CH_RST_1	[0]		

- **Registers to Control CLK Power Down**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0x98	PD_DEC_4	[3]	0x00	**PD_DEC_x** : Each Decoder Clock Power Down (x = channel number) **0** : Decoder Clock Power On **1** : Decoder Clock Power Off
		PD_DEC_3	[2]		
		PD_DEC_2	[1]		
		PD_DEC_1	[0]		

- **Registers to Control MPP**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0xA8	MPP_TST_SEL1	[7:0]	0x00	**MPP_TST_SEL1[3:0]** : Coaxial Output select though MPP1 pin **0** : Coaxial_Ch1 Out **1** : Coaxial_Ch2 Out **2** : Coaxial_Ch3 Out **3** : Coaxial_Ch4 Out **MPP_TST_SEL1[7:4]** : BT.601 CH1 HV Output select though GPIO1~2 pin **1** : CH1 BT601_H and V Signal Out
	0xA9	MPP_TST_SEL2	[7:0]	0x00	**MPP_TST_SEL2[3:0]** : Coaxial Output select though MPP2 pin **0** : Coaxial_Ch2 Out **1** : Coaxial_Ch3 Out **2** : Coaxial_Ch4 Out **3** : Coaxial_Ch1 Out **MPP_TST_SEL2[7:4]** : BT.601 CH2 HV Output select though GPIO3~4 pin **1** : CH2 BT601_H and V Signal Out
	0xAA	MPP_TST_SEL3	[7:0]	0x00	**MPP_TST_SEL3[3:0]** : Coaxial Output select though MPP3 pin **0** : Coaxial_Ch3 Out **1** : Coaxial_Ch4 Out **2** : Coaxial_Ch1 Out **3** : Coaxial_Ch2 Out **MPP_TST_SEL3[7:4]** : BT.601 CH3 HV Output select though GPIO5~6 pin **1** : CH3 BT601_H and V Signal Out
	0xAB	MPP_TST_SEL4	[7:0]	0x00	**MPP_TST_SEL4[3:0]** : Coaxial Output select though MPP4 pin **0** : Coaxial_Ch4 Out **1** : Coaxial_Ch1 Out **2** : Coaxial_Ch2 Out **3** : Coaxial_Ch3 Out **MPP_TST_SEL4[7:4]** : BT.601 CH4 HV Output select though GPIO7~8 pin **1** : CH4 BT601_H and V Signal Out

- **Registers to Control MPP**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0xB1	MPP1_DIR	[0]	0x00	**MPPx_DIR** : MPPx pin direction control (x = MPP pin number) **0** : Output Direction **1** : Input Direction
		MPP2_DIR	[1]		
		MPP3_DIR	[2]		
		MPP4_DIR	[3]		
	0xB3	MPP1_INV	[0]	0x00	**MPPx_INV** : MPPx pin output signal inversion (x = MPP pin number)
		MPP2_INV	[1]		
		MPP3_INV	[2]		
		MPP4_INV	[3]		

5.2.3 Video Output Control Registers

- **Registers to Select Video Output**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0xC0	VPORT1_SEQ1	[3:0]	0x00	**VPORTx_SEQy** **:** Select the type of output video signal through each video output port (x = VDO output port number, y= channel count for 1 port) **0** : Normal Display of Channel 1 **1** : Normal Display of Channel 2 **2** : Nomal Display of Channel 3 **3** : Normal Display of Channel 4 **4** : Only Y Display of Channel 1 **5** : Only Y Display of Channel 2 **6** : Only Y Display of Channel 3 **7** : Only Y Display of Channel 4 **8** : H_Half Display of Channel 1 **9** : H_Half Display of Channel 2 **A** : H_Half Display of Channel 3 **B** : H_Half Display of Channel 4 **C** : Only C Display of Channel 1 **D** : Only C Display of Channel 2 **E** : Only C Display of Channel 3 **F** : Only C Display of Channel 4
		VPORT1_SEQ2	[7:4]		
	0xC1	VPORT1_SEQ3	[3:0]		
		VPORT1_SEQ4	[7:4]		
	0xC2	VPORT2_SEQ1	[3:0]	0x11	
		VPORT2_SEQ2	[7:4]		
	0xC3	VPORT2_SEQ3	[3:0]		
		VPORT2_SEQ4	[7:4]		
	0xC4	VPORT3_SEQ1	[3:0]	0x22	
		VPORT3_SEQ2	[7:4]		
	0xC5	VPORT3_SEQ3	[3:0]		
		VPORT3_SEQ4	[7:4]		
	0xC6	VPORT4_SEQ1	[3:0]	0x33	
		VPORT4_SEQ2	[7:4]		
	0xC7	VPORT4_SEQ3	[3:0]		
		VPORT4_SEQ4	[7:4]		

- **Registers to Select Video Output**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0xC8	VPORT_1_CH_OUT_SEL	[3:0]	0x0	**VPORT_x_CH_OUT_SEL** **:** Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) **0** : 1-Port 1CH data **2** : 1-Port 2CH time-mixed data **8** : 1-Port 4CH time-mixed data **Etc.:** Don't use
	0xC9	VPORT_2_CH_OUT_SEL			
	0xCA	VPORT_3_CH_OUT_SEL			
	0xCB	VPORT_4_CH_OUT_SEL			

● Registers to Control Video Output Port Enable

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0xC8	VCLK_1_EN	[5]	0x3	**VCLK_x_EN** **:** Video Output Port_x CLK Enable (x = VDO output port number) **0** : Disable **1** : Enable
	0xC9	VCLK_2_EN			
	0xCA	VCLK_3_EN			
	0xCB	VCLK_4_EN			
	0xC8	VDO_1_EN	[4]		**VDO_x_EN** **:** Video Output Port_x VDO Enable (x = VDO output port number) **0** : Disable **1** : Enable
	0xC9	VDO_2_EN			
	0xCA	VDO_3_EN			
	0xCB	VDO_4_EN			

● Registers to Control Data

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0xD0	OUT_DATA_4_INV	[3]	0x00	**VDO_INV_x** **:** It sorts output video data inversely. (**0 :** [7:0], **1 :** [0:7]) **OUT_DATA_1_INV :** VDO_1 Port output order control **OUT_DATA_2_INV :** VDO_2 Port output order control **OUT_DATA_3_INV :** VDO_3 Port output order control **OUT_DATA_4_INV :** VDO_4 Port output order control
		OUT_DATA_3_INV	[2]		
		OUT_DATA_2_INV	[1]		
		OUT_DATA_1_INV	[0]		

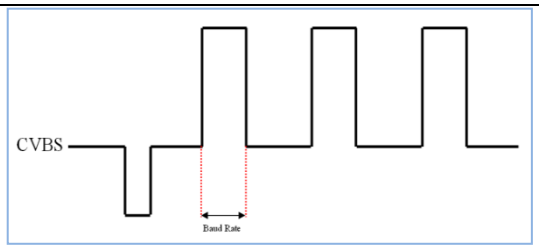
● Registers to Select Video Output Clock

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
1	0xCC	VPORT_1_OCLK_SEL	[6:4]	0x60	**VPORT_x_OCLK_SEL** **:** Select clock frequency and phase of each port. (x = Port number) **0~3** : PLL divided by 4 with phase#1~4 (37.125Mhz) **4~5** : PLL divided by 2 with phase#1~2 (74.25Mhz) **6~7** : PLL clk with phase#1~2(148Mhz)
	0xCD	VPORT_2_OCLK_SEL			
	0xCE	VPORT_3_OCLK_SEL			
	0xCF	VPORT_4_OCLK_SEL			
	0xCC	VPORT_1_OCLK_DLY_SEL	[3:0]		**VPORT_x_OCLK_DLY_SEL** **:** Delay the output clock in the unit of ≒ (VCLK / 16) ns. Can be delayed up (x = Port number) . **0** : ≒ (VCLK / 16) * **0** ns. **4** : ≒ (VCLK / 16) * **4** ns # Delay value = (VCLK / 16) * DLY_SEL Value ns
	0xCD	VPORT_2_OCLK_DLY_SEL			
	0xCE	VPORT_3_OCLK_DLY_SEL			
	0xCF	VPORT_4_OCLK_DLY_SEL			

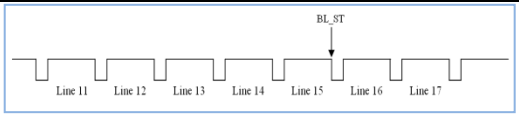
5.2.4 COAXIAL Registers

- CH1 Coaxial Register : Bank2 0x00~0x7F
- CH2 Coaxial Register : Bank2 0x80~0xFF
- CH3 Coaxial Register : Bank3 0x00~0x7F
- CH4 Coaxial Register : Bank3 0x80~0xFF

● **Registers to Control Baud Rate**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x00 / 0x80	CHx_BAUD	[7:0]	0x37	**CHx_BAUD** (x = Channel Number) : A-CP TX Baud Rate
	0x02 / 0x82	CHx_PELCO_BAUD		0x1B	**CHx_PELCO_BAUD** (x = Channel Number) : PELCO TX Baud Rate
Coaxial protocol 1H Line					

● **Registers to Control Start Point of VBI(Vertical Blank Interval)**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x04 / 0x84	CHx_BL_TXST[15:8]	[7:0]	0x00	**CHx_BL_TXST** (x = Channel Number) : A-CP Protocol TX start Line in VBI
	0x03 / 0x83	CHx_BL_TXST[7:0]		0x05	
	0x05 / 0x85	CHx_ACT_LEN	[3:0]	0x00	**CHx_ACT_LEN** (x = Channel Number) : A-CP Line number
	0x08 / 0x88	CHx_PELCO_TXST [15:8]	[7:0]	0x00	**CHx_PELCO_TXST** (x = Channel Number) : PELCO Protocol TX Start Line in VBI
	0x07 / 0x87	CHx_PELCO_TXST [7:0]			
Coaxial protocol Active Start Point of VBI(Vertical Blank Interval)					

- **Registers to Control Coaxial Protocol**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x09 / 0x89	CHx_COAX_SW_RST	[4]	0x00	**CHx_COAX_SW_RST** (x = Channel Number) : Coaxial Software Reset
		CHx_CNT_MODE	[3]		**CHx_CNT_MODE** (x = Channel Number) : A-CP Protocol Enable Signal
		CHx_TX_START	[0]		**CHx_TX_START** (x = Channel Number) : A-CP Protocol Enable Signal
	0x0A / 0x8A	CHx_TX_BYTE_LENGTH	[4:0]	0x08	**CHx_TX_BYTE_LENGTH** (x = Channel Number) : Transmission amount In A-CP Protocol
	0x0B / 0x8B	CHx_PELCO_8BIT	[7]	0x06	**CHx_PELCO_8BIT** (x = Channel Number) : Pelco Protocol 8Bit mode Selection **0** : Pelco Protocol Exp mode **1** : Pelco Protocol 8bit mode
		CHx_LINE_8BIT	[4]		**CHx_LINE_8BIT** (x = Channel Number) : A-CP Protocol Origin Mode Selection **0** : Pelco Protocol Mode **1** : A-CP Protocol Origin Mode
		CHx_PACKET_MODE	[2:0]		**CHx_PACKET_MODE** (x = Channel Number) : Coaxial Protocol Type **2** : Pelco Protocol Origin Mode **4** : Pelco Protocol Exp mode(Pelco_32bit Mode) **Others** : Manual
	0x0C / 0x8C	CHx_PELCO_CTEN	[0]	0x00	**CHx_PELCO_CTEN** (x = Channel Number) : PELCO Protocol Enable Bit (Active High)
	0x0E / 0x8E	CHx_BL_HSP [15:7]	[7:0]	0x00	**CHx_BL_HSP** (x = Channel Number) : Start Point in Coaxial Protocol Active Line
	0x0D / 0x8D	CHx_BL_HSP [7:0]		0x46	
	0x0F / 0x8F	CHx_PELCO_SHOT	[0]	0x00	**CHx_PELCO_SHOT** (x = Channel Number) : PELCO Protocol One Operation Enable signal

● Registers to Control Coaxial Data

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x10 / 0x90	CHx_TX_DATA_01	[7:0]	0xAA	**CHx_TX_DATA_01 ~ CHx_TX_DATA_04** (x = Channel Number) : 1st field Data in A-CP Protocol
	0x11 / 0x91	CHX_TX_DATA_02		0x1C	
	0x12 / 0x92	CHX_TX_DATA_03		0x18	
	0x13 / 0x93	CHX_TX_DATA_04		0xFF	
	0x14 / 0x94	CHX_TX_DATA_05	[7:0]	0xAA	**CHx_TX_DATA_05 ~ CHx_TX_DATA_08** (x = Channel Number) : 2nd field Data in A-CP Protocol
	0x15 / 0x95	CHX_TX_DATA_06		0x3C	
	0x16 / 0x96	CHX_TX_DATA_07		0xFF	
	0x17 / 0x97	CHX_TX_DATA_08		0xFF	
	0x18 / 0x98	CHX_TX_DATA_09	[7:0]	0xAA	**CHx_TX_DATA_09 ~ CHx_TX_DATA_12** (x = Channel Number) : 3rd field Data in A-CP Protocol
	0x19 / 0x99	CHX_TX_DATA_10		0x1B	
	0x1A / 0x9A	CHX_TX_DATA_11		0x00	
	0x1B / 0x9B	CHX_TX_DATA_12		0x00	
	0x1C / 0x9C	CHX_TX_DATA_13	[7:0]	0xAA	**CHx_TX_DATA_13 ~ CHx_TX_DATA_16** (x = Channel Number) : 4th field Data in A-CP Protocol
	0x1D / 0x9D	CHX_TX_DATA_14		0x3B	
	0x1E / 0x9E	CHX_TX_DATA_15		0x00	
	0x1F / 0x9F	CHX_TX_DATA_16		0x00	

● Registers to Control Coaxial Data

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x20 / 0xA0	CHx_PELCO_TXDAT_01	[7:0]	0x00	**CHx_PELCO_TXDAT_01 ~ CHx_PELCO_TXDAT_02** : 18th Line in PELCO Protocol (x = Channel Number)
	0x21 / 0xA1	CHx_PELCO_TXDAT_02		0x00	
	0x22 / 0xA2	CHx_PELCO_TXDAT_03		0x00	**CHx_PELCO_TXDAT_03 ~ CHx_PELCO_TXDAT_04** : 19th Line in PELCO Protocol (x = Channel Number)
	0x23 / 0xA3	CHx_PELCO_TXDAT_04		0x00	

- **Registers to Control Coaxial Protocol**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x2C / 0xAC	CHx_VSO_INV	[0]	0	**CHx_VSO_INV** (x = Channel Number) : Vertical Sync Inverter (Active High)
	0x2D / 0xAD	CHx_HSO_INV	[0]	0	**CHx_HSO_INV** (x = Channel Number) : Horizontal Sync Inverter (Active High)
	0x2F / 0xAF	CHx_EVEN_SUM	[0]	1	CHx_EVEN_SUM (x = Channel Number) : Control Protocol Active line on each field

- **Registers to Control Coaxial Protocol**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x3A / 0xBA	CHx_CLEAN	[0]	0	**CHx_CLEAN** (x = Channel Number) : RX Register is Read Only. So it need clean Condition First, this register set ON. Second, Read I2C Protocol 0x90. And then Clean RX Registers.

- **Registers to Read Coaxial Status**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x50 / 0xD0	CHx_PELCO_8_00	[7:0]	Read	**CHx_PELCO_8_00 ~ CHx_PELCO_8_07** (x = Channel Number) : Coaxial Output 8bit Data Read Register
	0x51 / 0xD1	CHx_PELCO_8_01			
	0x52 / 0xD2	CHx_PELCO_8_02			
	0x53 / 0xD3	CHx_PELCO_8_03			
	0x54 / 0xD4	CHx_PELCO_8_04			
	0x55 / 0xD5	CHx_PELCO_8_05			
	0x56 / 0xD6	CHx_PELCO_8_06			
	0x57 / 0xD7	CHx_PELCO_8_07			

- **Registers to Read Coaxial Status**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x5C / 0xDC	CHx_RX_DONE	[0]	Read	**CHx_RX_DONE** (x = Channel Number) : Coaxial RX Request Done

- **Registers to Read Coaxial Status**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x5D / 0xDD	CHx_RX_COAX_DUTY	[7:0]	Read	**CHx_RX_COAX_DUTY** (x = Channel Number) : Coaxial RX 8bit DUTY Read

Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x60 / 0xE0	CHx_ DEVICE_ID	[7:0]	0x00	**CHx_ DEVICE_ID** (x = Channel Number) : Define Device_ID in Protocol's Header
	0x62 / 0xE2	CHx_RX_AREA	[7:0]	0x00	**CHx_RX_AREA** (x = Channel Number) **:** Coaxial RX Area 8-bit
	0x63 / 0xE3	CHx_DELAY_ON	[4]	0x00	**CHx_DELAY_ON** (x = Channel Number) : Enable to use DELAY CNT Register
		CHx_COMM_ON	[0]		**CHx_COMM_ON** (x = Channel Number) **:** Coaxial RX Software Reset
	0x64 / 0xE4	CHx_DELAY_CNT	[7:0]	0x00	**CHx_DELAY_CNT** (x = Channel Number) : How many delay input signal based clock

Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x65 / 0xE5	CHx_ MSB	[0]	0	**CHx_ MSB** (x = Channel Number) **:** Coaxial RX MSB Change Mode
	0x66 / 0xE6	CHx_A_DUTY_ON	[7]	0	**CHx_A_DUTY_ON** (x = Channel Number) **:** Coaxial RX DUTY Mode
	0x67 / 0xE7	CHx_INT_MODE	[0]	0	**CHx_INT_MODE** (x = Channel Number) **:** Coaxial RX Interrupt Mode
	0x68 / 0xE8	CHx_RX_SZ	[7:4]	0x00	**CHx_RX_SZ** (x = Channel Number) **:** Coaxial RX Line MAX Set
	0x69 / 0xE9	CH1_M_DUTY	[7:0]	0x00	**CH1_M_DUTY** (x = Channel Number) **:** Coaxial RX DUTY Set
	0x6A / 0xEA	CH1_RX_START_POSITION	[7:0]	0x00	**CH1_RX_START_POSITION** (x = Channel Number) **:** Coaxial RX Start Point in Line

- **Registers to Read Coaxial Status**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
2~3	0x40 / 0xC0	RX_LINE00	[7:0]	Read	RX_LINE00 : Coaxial Output 40bit line0 Read Register
	0x41 / 0xC1				
	0x42 / 0xC2				
	0x43 / 0xC3				
	0x44 / 0xC4				
	0x45 / 0xC5	RX_LINE01	[7:0]	Read	RX_LINE01 : Coaxial Output 40bit line1 Read Register
	0x46 / 0xC6				
	0x47 / 0xC7				
	0x48 / 0xC8				
	0x49 / 0xC9				
	0x4A / 0xCA	RX_LINE02	[7:0]	Read	RX_LINE02 : Coaxial Output 40bit line2 Read Register
	0x4B / 0xCB				
	0x4C / 0xCC				
	0x4D / 0xCD				
	0x4E / 0xCE				
	0x6C / 0xEC	RX_LINE03	[7:0]	Read	RX_LINE03 : Coaxial Output 40bit line3 Read Register
	0x6D / 0xED				
	0x6E / 0xEE				
	0x6F / 0xEF				
	0x70 / 0xF0				
	0x71 / 0xF1	RX_LINE04	[7:0]	Read	RX_LINE04 : Coaxial Output 40bit line4 Read Register
	0x72 / 0xF2				
	0x73 / 0xF3				
	0x74 / 0xF4				
	0x75 / 0xF5				
	0x76 / 0xF6	RX_LINE05	[7:0]	Read	RX_LINE05 : Coaxial Output 40bit line5 Read Register
	0x77 / 0xF7				
	0x78 / 0xF8				
	0x79 / 0xF9				
	0x7A / 0xFA				

5.2.5 MOTION Registers

- **Registers to Detect Motion**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
4	0x00	CH1_MOTION_OFF	[0]	ON = 0x0D OFF = 0x0C	**CHx_MOTION_OFF** **:** Motion Detection On/Off Selection (x = channel number) **0** : Motion detection on **1** : Motion detection off
	0x07	CH2_MOTION_OFF			
	0x0E	CH3_MOTION_OFF			
	0x15	CH4_MOTION_OFF			
	0x00	CH1_MOTION_PIC	[3:2]		**CHx_MOTION_PIC** **:** Indicates the type of processing made on the area where motion is generated. (x = channel number) **0** : No processing made on the area where motion is generated. **1** : EVEN_FLD (Luma – 32) **2** : EVEN_FLD (Luma – 48) **3** : ALL FLD (Luma – 48)
	0x07	CH2_MOTION_PIC			
	0x0E	CH3_MOTION_PIC			
	0x15	CH4_MOTION_PIC			

- **Registers to Detect Motion**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
4	0x01	CH1_MOD_TSEN	[7:0]	0x60	**CHx_MOD_TSEN** **:** Motion Temporal Sensitivity. (x = channel number) The value (the sum of the motion block) bases on which it is determined whether motion is generated or not (0 -> 255 The greater the number, the less sensitive it gets)
	0x08	CH2_MOD_TSEN			
	0x0F	CH3_MOD_TSEN			
	0x16	CH4_MOD_TSEN			

- **Registers to Detect Motion**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
4	0x02	CH1_MOD_PSEN	[2:0]	0x23	**CHx_MOD_PSEN** : Motion Pixel Sensitivity Control Register. (x = channel number) It is determine Motion Brightness level. **0** : bypass **4** : 1/16 **1** : 1/2 **5** : 1/32 **2** : 1/4 **others** : 1/64 **3** : 1/8
	0x09	CH2_MOD_PSEN			
	0x10	CH3_MOD_PSEN			
	0x17	CH4_MOD_PSEN			

5.2.6 MIPI INTERFACE

- **Each Channels Enable Registers for Arbiter**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x00	CH4_ARB_EN	[7]	0x0	**ARB_EN** : Enable each ch# Arbiter Module **0** : CH1 **2** : CH2 **4** : CH3 **8** : CH4
		CH3_ARB_EN	[6]		
		CH2_ARB_EN	[5]		
		CH1_ARB_EN	[4]		
		CH4_MEM_EN	[3]	0x0	**MEM_EN** : MIPI MEM Enable MODE **0** : CH1 **2** : CH2 **4** : CH3 **8** : CH4
		CH3_MEM_EN	[2]		
		CH2_MEM_EN	[1]		
		CH1_MEM_EN	[0]		
	0x01	CH4_SCALE_MODE	[7:6]	0x00	**SCALE_MODE** : Data Downsizing Mode **0** : original **1** : 1/2 Down **2** : 1/4 Down
		CH3_SCALE_MODE	[5:4]		
		CH2_SCALE_MODE	[3:2]		
		CH1_SCALE_MODE	[1:0]		

- **Registers for Arbiter Special Function**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x0D	ARB_32BIT	[0]	0x01	**ARB_32BIT** : Internal Interface MODE **0** : 16bit mode for 2 Lanes **1** : 32bit mode for 4 lanes
	0x0F	MIPI_CH1_VIDEO_TYPE	[1:0]	0x00	**VIDEO_TYPE** : Video YCbCr Format type selection **0** : 4:2:2 Format **1** : 4:2:0 Format (Legacy) **2** : 4:2:0 Format **3** : Reserved
		MIPI_CH2_VIDEO_TYPE	[3:2]		
		MIPI_CH3_VIDEO_TYPE	[5:4]		
		MIPI_CH4_VIDEO_TYPE	[7:6]		
	0x1B	CH4_EMB_EN	[3]	0x00	**CHx_EMB_EN** : Enable Embedded Data Insertion. **0** : Off **1**: On
		CH3_EMB_EN	[2]		
		CH2_EMB_EN	[1]		
		CH1_EMB_EN	[0]		
	0x1C	CH4_EMB_ARB	[7:6]	0x00	**EMB_ARB[1:0]** : Embedded Data Insertion Line Selection **EMB_ARB[0]** : First Line Insertion On / Off **EMB_ARB[1]** : Last Line Insertion On / Off
		CH3_EMB_ARB	[5:4]		
		CH2_EMB_ARB	[3:2]		
		CH1_EMB_ARB	[1:0]		

Registers for Data Transmission

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x10	CH1_RD_P_MODE	[3:0]	0x00	**RD_P_MODE** : Data Transmission Packet size Option **0** : Auto **15** : Manual Mode
		CH2_RD_P_MODE	[7:4]		
	0x11	CH3_RD_P_MODE	[3:0]		
		CH4_RD_P_MODE	[7:4]		
	0x12	CH1_RD_PACKET[7:0]	[7:0]	0x00	**RD_PACKET** : Manual Read Packet Size
	0x13	CH1_RD_PACKET[15:8]			
	0x14	CH2_RD_PACKET[7:0]			
	0x15	CH2_RD_PACKET[15:8]			
	0x16	CH3_RD_PACKET[7:0]			
	0x17	CH3_RD_PACKET[15:8]			
	0x18	CH4_RD_PACKET[7:0]			
	0x19	CH4_RD_PACKET[15:8]			

Registers to control Arbiter Memory

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x20	CH1_RD_T_MODE	[3:0]	0x00	**RD_T_MODE** : Read Memory Total Line Option **0** : Auto **1** : 1080 lines **2** : 720 lines **3** : 240 lines **4** : 288 lines **15** : Manual Mode
		CH2_RD_T_MODE	[7:4]		
	0x21	CH3_RD_T_MODE	[3:0]		
		CH4_RD_T_MODE	[7:4]		
	0x22	CH1_RD_LINE_TOTAL[7:0]	[7:0]	0x00	**CHx_RD_LINE_TOTAL** : Manual Total Line
	0x23	CH1_RD_LINE_TOTAL[15:8]			
	0x24	CH2_RD_LINE_TOTAL[7:0]			
	0x25	CH2_RD_LINE_TOTAL[15:8]			
	0x26	CH3_RD_LINE_TOTAL[7:0]			
	0x27	CH3_RD_LINE_TOTAL[15:8]			
	0x28	CH4_RD_LINE_TOTAL[7:0]			
	0x29	CH4_RD_LINE_TOTAL[15:8]			

Registers for Data Timing

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x30	MIPI_T_MODE	[3:0]	0x00	**MIPI_T_MODE** : MIPI Transmission Latency Timing Option **0 :** Predefined Value. **others :** Manual Value.
	0x32	SOF_PERIOD[15:8]	[7:0]	0x00	**SOF_PERIOD** **:** Manual SOF Timing Parameter
	0x33	SOF_PERIOD[7:0]			
	0x34	EOF_PERIOD[15:8]			**EOF_PERIOD** **:** Manual EOF Timing Parameter
	0x35	EOF_PERIOD[7:0]			
	0x36	SOL_PERIOD[15:8]			**SOL_PERIOD** **:** Manual SOL Timing Parameter
	0x37	SOL_PERIOD[7:0]			
	0x38	EOL_PERIOD[15:8]			**EOL_PERIOD** **:** Manual EOL Timing Parameter
	0x39	EOL_PERIOD[7:0]			

Registers to control Arbiter

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x3A	CH4_HCNT_ERR	[7]	0x00	**HCNT_ERR** **:** Enable H SIZE Error Option in transmission. **ARB_NO_OPT** **:** When Video Status is No_Video, None Transmission **0 :** Disable **1 :** Enable
		CH3_HCNT_ERR	[6]		
		CH2_HCNT_ERR	[5]		
		CH1_HCNT_ERR	[4]		
		CH4_ARB_NO_OPT	[3]		
		CH3_ARB_NO_OPT	[2]		
		CH2_ARB_NO_OPT	[1]		
		CH1_ARB_NO_OPT	[0]		
	0x3B	SWITCH_OPT	[3:0]	0x00	**SWITCH_OPT** **:** Arbitration Priority Option. **0 :** Switching every 1 line Priority Channel, **1 :** Switching every 4 line Priority Channel, **2 :** Switching every 8 line Priority Channel, **3 :** Switching every 16 line Priority Channel,

Registers to reset Arbiter

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x40	ARB_VFC_STABLE_RESET_OPT	[4]	0x00	**ARB_VFC_STABLE_RESET_OPT** : if Video Status is unstable, reset Internal IPs **0** : Disable **1** : Enable
		SW_RST	[0]		**SW_RST** : Arbiter SW_RST **0** : Disable **1** : Enable

Registers to avoid Arbiter Collision

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x41	CH1_COLI_OPT	[3:0]	0x00	**COLI_OPT** : Collision Option **0:** 5 Line **2:** 3 line **1:** 4 line **3:** 2 line
		CH2_COLI_OPT	[7:4]		
	0x42	CH3_COLI_OPT	[3:0]		
		CH4_COLI_OPT	[7:4]		
	0x43	CH4_COLI_CLR	[3]	0x0	**COLI_CLR** : reset Collision count **0** : Disable **1** : Enable
		CH3_COLI_CLR	[2]		
		CH2_COLI_CLR	[1]		
		CH1_COLI_CLR	[0]		

- **Registers to reset Arbiter**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x44	CH4_RD_FRM_CLR	[7]	0x0	RD_FRM_CLR : reset internal Read Frame count Status WR_FRM_CLR : reset Internal Write Frame count Status 0 : Disable 1 : Enable
		CH3_RD_FRM_CLR	[6]		
		CH2_RD_FRM_CLR	[5]		
		CH1_RD_FRM_CLR	[4]		
		CH4_WR_FRM_CLR	[3]		
		CH3_WR_FRM_CLR	[2]		
		CH2_WR_FRM_CLR	[1]		
		CH1_WR_FRM_CLR	[0]		
20	0x50	CH1_WR_FRAME_CNT[15:8]	[7:0]	0x00	WR_FRAME_CNT : Internal Write Frame Count Status
	0x51	CH1_WR_FRAME_CNT[7:0]			
	0x54	CH2_WR_FRAME_CNT[15:8]			
	0x55	CH2_WR_FRAME_CNT[7:0]			
	0x58	CH3_WR_FRAME_CNT[15:8]			
	0x59	CH3_WR_FRAME_CNT[7:0]			
	0x5C	CH4_WR_FRAME_CNT[15:8]			
	0x5D	CH4_WR_FRAME_CNT[7:0]			
	0x52	CH1_RD_FRAME_CNT[15:8]			RD_FRAME_CNT : Internal Read Frame Count Status
	0x53	CH1_RD_FRAME_CNT[7:0]			
	0x56	CH2_RD_FRAME_CNT[15:8]			
	0x57	CH2_RD_FRAME_CNT[7:0]			
	0x5A	CH3_RD_FRAME_CNT[15:8]			
	0x5B	CH3_RD_FRAME_CNT[7:0]			
	0x5E	CH4_RD_FRAME_CNT[15:8]			
	0x5F	CH4_RD_FRAME_CNT[7:0]			

Registers to control H Package Size

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x60	CH1_H_pack_size[10:8]	[2:0]	0x00	H_pack_size : Manual one H Package Size
	0x61	CH1_H_pack_size[7:0]	[7:0]		
	0x62	CH2_H_pack_size[10:8]	[2:0]		
	0x63	CH2_H_pack_size[7:0]	[7:0]		
	0x64	CH3_H_pack_size[10:8]	[2:0]		
	0x65	CH3_H_pack_size[7:0]	[7:0]		
	0x66	CH4_H_pack_size[10:8]	[2:0]		
	0x67	CH4_H_pack_size[7:0]	[7:0]		

Registers to control Arbiter

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
20	0x68	CH1_coli_cnt	[7:0]	0x00	coli_cnt : Collision Count status
	0x69	CH2_coli_cnt			
	0x6A	CH3_coli_cnt			
	0x6B	CH4_coli_cnt			
	0x70	CH1_coli_out	[0]		coli_out :Transmission Collision error Status
		CH2_coli_out	[1]		
		CH3_coli_out	[2]		
		CH4_coli_out	[3]		

5.2.7 MIPI TX

- **Register to Control MIPI TX PHY**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
21	0x07	MIPI_TX_PHY_PWR_DOWN	[7]	0x00	**MIPI_TX_PHY_PWR_DOWN** **:** Enable the Power Down Mode for MIPI TX PHY. **0 :** Normal Operation **1 :** Power Down
		MIPI_TX_PHY_REF_SEL	[6:4]		**MIPI_TX_PHY_REF_SEL** **:** Control the Reference level trim.
		MIPI_TX_LANES_ACTIVE	[3:2]		**MIPI_TX_LANES_ACTIVE** **:** Enable the Serial data lane **0 :** 1Lane Mode **1 :** 2Lane Mode **Others :** 4Lane Mode
		MIPI_TX_SYS_CORE_RDY	[1]		**MIPI_TX_SYS_CORE_RDY** **:** Enable for the serialized function provided by the system control once the system core has completed initialization. **0 :** Disable **1 :** Enable
		MIPI_TX_SERIAL_IF_EN	[0]		**MIPI_TX_SERIAL_IF_EN** **:** Enable for this instance of the serial interface. If the serial interface is not being used (MIPI_TX_SERIAL_IF_EN = 0) then the protocol layer will drive the internals of the PHY to its lowest power state (ultra-low power state) while tri-stating the output pads. **0 :** Disable **1 :** Enable
	0x08	MIPI_TX_HRES_IN	[7]	0x00	**MIPI_TX_HRES_IN** **:** Control the High-speed resistor trim.
		MIPI_TX_LP_SLEW_IN	[6:4]		**MIPI_TX_LP_SLEW_IN** **:** Control the MIPI low-power driver slew rate trim.
		MIPI_TX_CONT_TX_CLK	[3]		**MIPI_TX_CONT_TX_CLK** **:** Enable the MIPI TX Continuous Clock Transmission. If asserted the transmitted MIPI clock is kept active between packets. **0 :** Non-continuous Clock Transmission **1 :** Continuous Clock Transmission
		MIPI_TX_RESTART_EN	[2]		**MIPI_TX_RESTART_EN** **:** When asserted the interface completes the transmission of the current packet and sends an end of frame packet **0 :** Disable **1 :** Enable
		MIPI_TX_STANDBY_EOF	[1]		**MIPI_TX_STANDBY_EOF** **0 :** respond to MIPI_TX_STANBY_EN at end of current line/packet **1 :** respond to MIPI_TX_STANBY_EN at end of current frame
		MIPI_TX_STANDBY_EN	[0]		**MIPI_TX_STANDBY_EN** **:** Asserted when the chip is to go into standby. The interface completes the transmission of the current packet and sends an end of frame packet and then optionally goes into ultra low power mode. **0 :** Disable **1 :** Enable

- **Register to Control MIPI TX**

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
21	0x0A	MIPI_TX_DATA_TYPE_UD	[5:0]	0x00	**MIPI_TX_DATA_TYPE_UD** **:** Select the Data Type for User Definition.
	0x0E	MIPI_TX_CHAN_NUM	[1:0]	0x00	**MIPI_TX_CHAN_NUM** **:** Select the Virtual Channel ID. Channel number to be inserted in the MIPI packet header.
	0x0F	MIPI_TX_FRAME_CNT_RST	[1]	0x00	**MIPI_TX_FRAME_CNT_RST** **:** Asserted to reset the frame counter.
		MIPI_TX_FRAME_CNT_EN	[0]		**MIPI_TX_FRAME_CNT_EN** **:** Asserted if the frame counter value is to be inserted in the WC field of a start/end of frame short packet. **0 :** Disable **1 :** Enable

Register to Control MIPI TX Timing Parameter

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
21	0x10	MIPI_TX_T_HS_ZERO	[5:0]	0x12	**MIPI_TX_T_HS_ZERO** : Control the Timing Parameter of HS Zero State at Start for Data Lane.
	0x11	MIPI_TX_T_HS_PREPARE	[3:0]	0x07	**MIPI_TX_T_HS_PREPARE** : Control the Timing Parameter of LP-00 State for Data Lane.
	0x12	MIPI_TX_T_HS_TRAIL	[4:0]	0x0A	**MIPI_TX_T_HS_TRAIL** : Control the Timing Parameter of HS Zero State at End for Data Lane.
	0x13	MIPI_TX_T_HS_EXIT	[5:0]	0x10	**MIPI_TX_T_HS_EXIT** : Control the Timing Parameter of LP-11 to HS Burst State for Clock Lane.
	0x14	MIPI_TX_T_CLK_ZERO	[6:0]	0x29	**MIPI_TX_T_CLK_ZERO** : Control the Timing Parameter of HS Zero State at Start for Clock Lane.
	0x15	MIPI_TX_T_CLK_PREPARE	[3:0]	0x06	**MIPI_TX_T_CLK_PREPARE** : Control the Timing Parameter of LP-00 State for Clock Lane.
	0x16	MIPI_TX_T_CLK_TRAIL	[4:0]	0x0A	**MIPI_TX_T_CLK_TRAIL** : Control the Timing Parameter of HS Zero State at End for Clock Lane.
	0x17	MIPI_TX_T_CLK_PRE	[5:0]	0x02	**MIPI_TX_T_CLK_PRE** : Control the Timing Parameter of Data Transfer Start from Clock Lane.
	0x18	MIPI_TX_T_CLK_POST	[5:0]	0x10	**MIPI_TX_T_CLK_POST** : Control the Timing Parameter of Clock Transfer End from Data Transfer End.
	0x19	MIPI_TX_T_LPX	[5:0]	0x08	**MIPI_TX_T_LPX** : Control the Timing Parameter of Transition Time for LP Data Transfer.
	0x1A	MIPI_TX_T_WAKE_UP	[6:0]	0x13	**MIPI_TX_T_WAKE_UP** : Control the Timing Parameter of Exit Time from ULP State.
	0x1B	MIPI_TX_T_INIT	[6:0]	0x10	**MIPI_TX_T_INIT** : Control the Timing Parameter of Initialisation Time when First Transitioning to the LP-11 State after Power Up/Reset.
	0x1C	MIPI_TX_T_BGAP	[5:0]	0x0D	**MIPI_TX_T_BGAP** : Time to Enable the Band Gap.

Registers to Control MIPI TX

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
21	0x29	ODD_MANUAL_FRAME_CNT[7:0]	[7:0]	0x00	**ODD_MANUAL_FRAME_CNT** : Select the Odd Frame Count Value for Odd Field.
	0x2A	ODD_MANUAL_FRAME_CNT[15:8]	[7:0]	0x00	
	0x2B	EVEN_MANUAL_FRAME_CNT[7:0]	[7:0]	0x00	**EVEN_MANUAL_FRAME_CNT** : Select the Even Frame Count Value for Even Field.
	0x2C	EVEN_MANUAL_FRAME_CNT[15:8]	[7:0]	0x00	
	0x2E	MIPI_CH_ID_TYPE	[0]	0x0	**MIPI_CH_ID_TYPE** : Select the MIPI Virtual Channel ID Insertion Mode. 0 : Auto Insertion Mode 1 : Manual Insertion Mode
	0x2F	MIPI_BYTE_CNT_TYPE	[0]	0x0	**MIPI_BYTE_CNT_TYPE** : Select the Line Byte Count Insertion Mode. 0 : Auto Insertion Mode 1 : Manual Insertion Mode
	0x30	MIPI_TX_LINE_BYTE_CNT_CH1[7:0]	[7:0]	0x00	**MIPI_TX_LINE_BYTE_CNT_CHx** : Select the Line Byte Count Value for Virtual Channel-x (x = channel number)
	0x31	MIPI_TX_LINE_BYTE_CNT_CH1[15:8]	[7:0]	0x0F	
	0x32	MIPI_TX_LINE_BYTE_CNT_CH2[7:0]	[7:0]	0x00	
	0x33	MIPI_TX_LINE_BYTE_CNT_CH2[15:8]	[7:0]	0x0F	
	0x34	MIPI_TX_LINE_BYTE_CNT_CH3[7:0]	[7:0]	0x00	
	0x35	MIPI_TX_LINE_BYTE_CNT_CH3[15:8]	[7:0]	0x0F	
	0x36	MIPI_TX_LINE_BYTE_CNT_CH4[7:0]	[7:0]	0x00	
	0x37	MIPI_TX_LINE_BYTE_CNT_CH4[15:8]	[7:0]	0x0F	
	0x38	MIPI_TX_DATA_TYPE_CH1	[5:0]	0x1E	**MIPI_TX_DATA_TYPE_CHx** Select the Data Type for Virtual Channel-x. (x = channel number)
	0x39	MIPI_TX_DATA_TYPE_CH2	[5:0]	0x1E	
	0x3A	MIPI_TX_DATA_TYPE_CH3	[5:0]	0x1E	
	0x3B	MIPI_TX_DATA_TYPE_CH4	[5:0]	0x1E	
	0x3C	CH4_DATA_TYPE_OPT	[7:6]	0x00	**CHx_DATA_TYPE_OPT** : Select the Data Type Option for Virtual Channel-x. (x = channel number) **0 :** Non-Embedded Data **1 :** Supported Embedded Data(0x12) **2 :** Supported Embedded Data(User Definition)
		CH3_DATA_TYPE_OPT	[5:4]		
		CH2_DATA_TYPE_OPT	[3:2]		
		CH1_DATA_TYPE_OPT	[1:0]		
	0x3E	MIPI_CH2_FRAME_OPT	[6:4]	0x00	**MIPI_CHx_FRAME_OPT** : Select the Frame Count Option for Virtual Channel-x. (x = channel number) **0 :** Free-running for Progressive. **1 :** Fix to “1” for Odd Field, “2” for Even Field. **2 :** Fix to “2” for Odd Field, “1” for Even Field. **3:** Manual Mode. Fix to “Manual Odd” for Odd Field, “Manual Even” for Even Field. **4:** Free-running for Interlaced Type NTSC MAX 60. **5:** Free-running for Interlaced Type PAL MAX 50. **6:** Free-running for Interlaced Type MAX 16’hFFFF.
		MIPI_CH1_FRAME_OPT	[2:0]		
	0x3F	MIPI_CH4_FRAME_OPT	[6:4]	0x00	
		MIPI_CH3_FRAME_OPT	[2:0]		

Registers to Control MIPI TX Clock

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr			Default	
21	0x44	MIPI_SRC_CLK_INV	[4]	0x00	**MIPI_SRC_CLK_INV** : Select the MIPI PLL Output Clock Phase. **0** : Positive Phase **1** : Negative Phase
	0x45	MIPI_BYTE_CLK_INV	[7]	0x02	**MIPI_BYTE_CLK_INV** : Select the MIPI Byte Clock Phase. **0** : Positive Phase **1** : Negative Phase
		MIPI_DATA_CLK_INV	[3]		**MIPI_DATA_CLK_INV** : Select the MIPI Data Clock Phase. **0** : Positive Phase **1** : Negative Phase
		MIPI_DATA_CLK_SEL	[1:0]		**MIPI_DATA_CLK_SEL** : Select the MIPI Data Clock Divide. **0** : Divide by 8 **1** : Divide by 4 **2** : Divide by 2 **3** : Divide by 1
	0x46	PD_MIPI_CLK	[0]	0x00	**PD_MIPI_CLK** : Enable the Power Down Mode for MIPI TX Controller. **0** : Normal Operation **1** : Power Down

Chapter 6
ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

Table 6.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
1.2V Power Supply Voltage	VDD1A/ VDD1D	-0.5	-	1.32	V	
3.3V Power Supply Voltage	VDD3A/ VDD3D	-0.5	-	3.63	V	
Voltage for Digital Input pins	V_{DI}	-0.5	-	VDD3D+ 0.5	V	
Voltage for Analog Input pins	V_{AI}	-0.5	-	1.92	V	
Storage Temperature	T_S	-50	-	150	℃	
Junction Temperature	T_J	-40	-	125	℃	
Vapor phase soldering (15 Sec)	T_{VSOL}	-	-	220	℃	

* **Note** : This Device should be operated under recommended operating condition. Since, absolute maximum rating condition can either cause device reliability problem or damage the device sufficiently to cause immediate failure.

6.2 RECOMMENDED OPERATING CONDITION

Table 6.2 Recommended Operating Condition

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
1.2V Analog Power Supply Voltage	VDD1A	1.1	1.2	1.3	V	
1.2V Digital Power Supply Voltage	VDD1D	1.08	1.2	1.32	V	
3.3V Analog Power Supply Voltage	VDD3A	3.1	3.3	3.5	V	
3.3V Digital Power Supply Voltage	VDD3D	2.97	3.3	3.63	V	
Ambient operating temperature	T_A	-40	-	85	℃	

6.3 DC CHARACTERISTICS

Table 6.3 DC Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
Input Low Voltage	V_{IL}	-0.3	-	VDD3D*0.3	V	
Input High Voltage	V_{IH}	VDD3D*0.7	-	VDD3D+0.3	V	
Input Leakage Current	I_L	-	-	±10	uA	
Input Capacitance	C_{IN}	-	5	-	pF	
Output Low Voltage	V_{OL}	-	-	0.4	V	
Output High Voltage	V_{OH}	2.4	-	-	V	
Tri-State Output Leakage Current	I_{OZ}	-	-	±10	uA	
Output Capacitance	C_{OUT}	-	5	-	pF	

6.4 AC CHARACTERISTICS

Table 6.4 AC Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
(Power Supply Current)			① / ②			
1.2V Digital Power Supply Current	I_{VDD1D}	-	134 / 190	-	mA	
3.3V Digital Power Supply Current	I_{VDD3D}	-	60 / 10	-	mA	
1.2V Analog Power Supply Current	I_{VDD1A}		163 / 225		mA	
3.3V Analog Power Supply Current	I_{VDD3A}	-	104 / 104	-	mA	
① only Parallel 720p 4ch output ② only MIPI 1080p 4ch output # When using 1080p 4ch output, only MIPI out is supported						
(Clock Pin)						
SYS_CLK frequency	f_{SYS_CLK}	-	27.0	-	MHz	
SYS_CLK duty cycle	f_{DUTY}	45	-	55	%	
(Reset Pin)						
RSTB setup time	t_{SU}	1			uSec	
RSTB pulse width low	t_{PWL_rstb}	1			uSec	
RSTB release time (low to high)	t_{REL_rstb}	10			uSec	
(Host Interface Pins)						
SCL clock frequency	f_{SCL}	-	100	400	kHz	
Hold time(repeated) START condition.	$t_{HD:STA}$	0.6	-	-	uSec	
LOW period of the SCL clock	t_{LOW}	1.3	-	-	uSec	
HIGH period of the SCL clock	t_{HIGH}	0.6	-	-	uSec	
Set-up time for a repeated START condition	$t_{SU:STA}$	0.6	-	-	uSec	
Data hold time	t_{HD_DAT}	0	-	0.9	uSec	
Data set-up time	t_{SU_DAT}	100	-	-	ns	
Rise time of both SDA and SCL signals	t_r	20	-	300	ns	
Fall time of both SDA and SCL signals	t_f	20	-	300	ns	
Set-up time for STOP condition	$t_{SU:STO}$	0.6	-	-	uSec	
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	-	uSec	
Capacitive load for each bus line	C_b	-	-	400	pF	

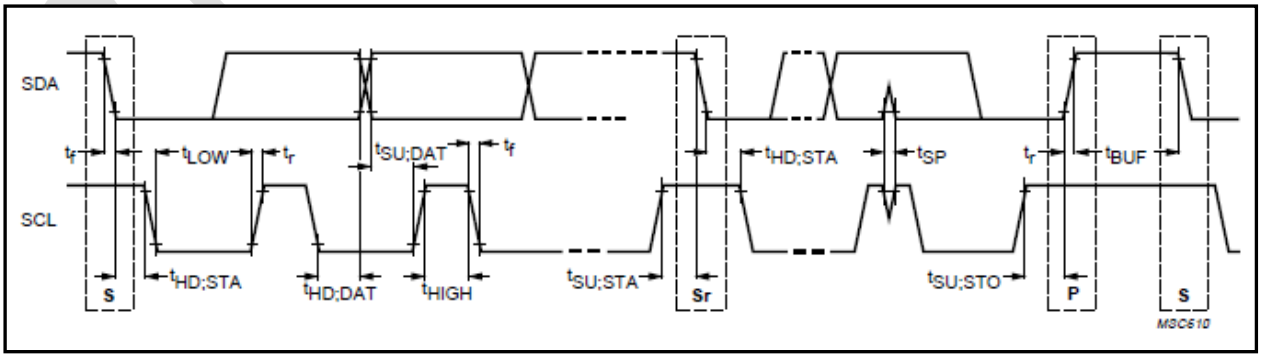


Figure 6.1 SCL and SDA Timing Diagram

6.5 MIPI HS/LP Transmitter Timing

Table 6.5 MIPI HS/LP Transmitter Timing

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
(HS Transmitter DC Specifications)						
HS transmit static common mode voltage	V_{CMTX}	150	200	250	mV	1
V_{CMTX} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{CMTX(1,0)}\|$			5	mV	2
Single ended output impedance	Z_{OS}	40	50	62.5	Ω	
Single ended output impedance mismatch	ΔZ_{OS}			10	%	
HS transmit differential volage	$\|V_{OD}\|$	140	200	270	mV	1
V_{OD} mismatch when output is Differential-1 or Differential-0	$\|\Delta V_{OD}\|$			14	mV	2
HS output high voltage	V_{OHHS}			360	mV	1
1. Value when driving into load impedance anywhere in the Z_{ID} range 2. A transmitter should minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation, and optimize signal integrity.						
(HS Transmitter AC Specifications)						
HS Data TX Common Level Variations Above 450MHz	$\Delta V_{CMTX(HF)}$			15	mV_{RMS}	
HS Data TX Common Level Variations Between 50-450MHz	$\Delta V_{CMTX(LF)}$			25	mV_{PEAK}	
HS Data TX 20%-80% Rise Time and Fall Time	t_R and t_F			0.3	UI	1,2
				0.35	UI	1,3
		150			ps	4
The frequency 'fh' is the highest fundamental frequency for data transmission 1. UI is equal to 1/(2*fh). 2. Applicable when supporting maximum HS bit rates ≤ 1Gbps(UI ≥ 1ns). 3. Applicable when supporting maximum HS bit rates > 1Gbps(UI ≤ 1ns) but less than 1.5Gbps(UI ≥ 0.667ns) 4. Applicable when supporting maximum HS bit rates ≤ 1.5Gbps. However, to avoid excessive radiation, bit rates < 1Gbps(UI ≥ 1ns), should not use value below 150ps.						
(LP Transmitter DC Specifications)						
LP TX Thevenin Output High Voltage Level	V_{OH}	1.1	1.2	1.3	V	
LP TX Thevenin Output Low Voltage Level	V_{OL}	-50		50	mV	
LP TX Output Impedance	Z_{OLP}	110			Ω	
(LP Transmitter AC Specifications)						
LP TX 15%-85% Rise Time Level	T_{RLP}			25	ns	1
LP TX 15%-85% Fall Time Level	T_{FLP}			25	ns	1
LP TX 30%-85% Rise Time and Fall Time	T_{REOT}			35	ns	2,3
LP TX Slew Rate @ C_{LOAD} =70pF	$\partial V/\partial t_{SR}$			150	mV/ns	1,4,5
LP TX Load Capacitance	C_{LOAD}	0		70	pF	1
1. C_{LOAD} include the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay. 2. The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive. 3. With an additional load capacitance C_{CM} between 0 and 60pF on the terminvation center tap at RX side of the Lane. 4. This value represents a corner point in a piecewise linear curve. 5. When the output voltage is in the range specified by $V_{PIN(absmax)}$.						

Chapter 7
PACKAGE INFORMATION

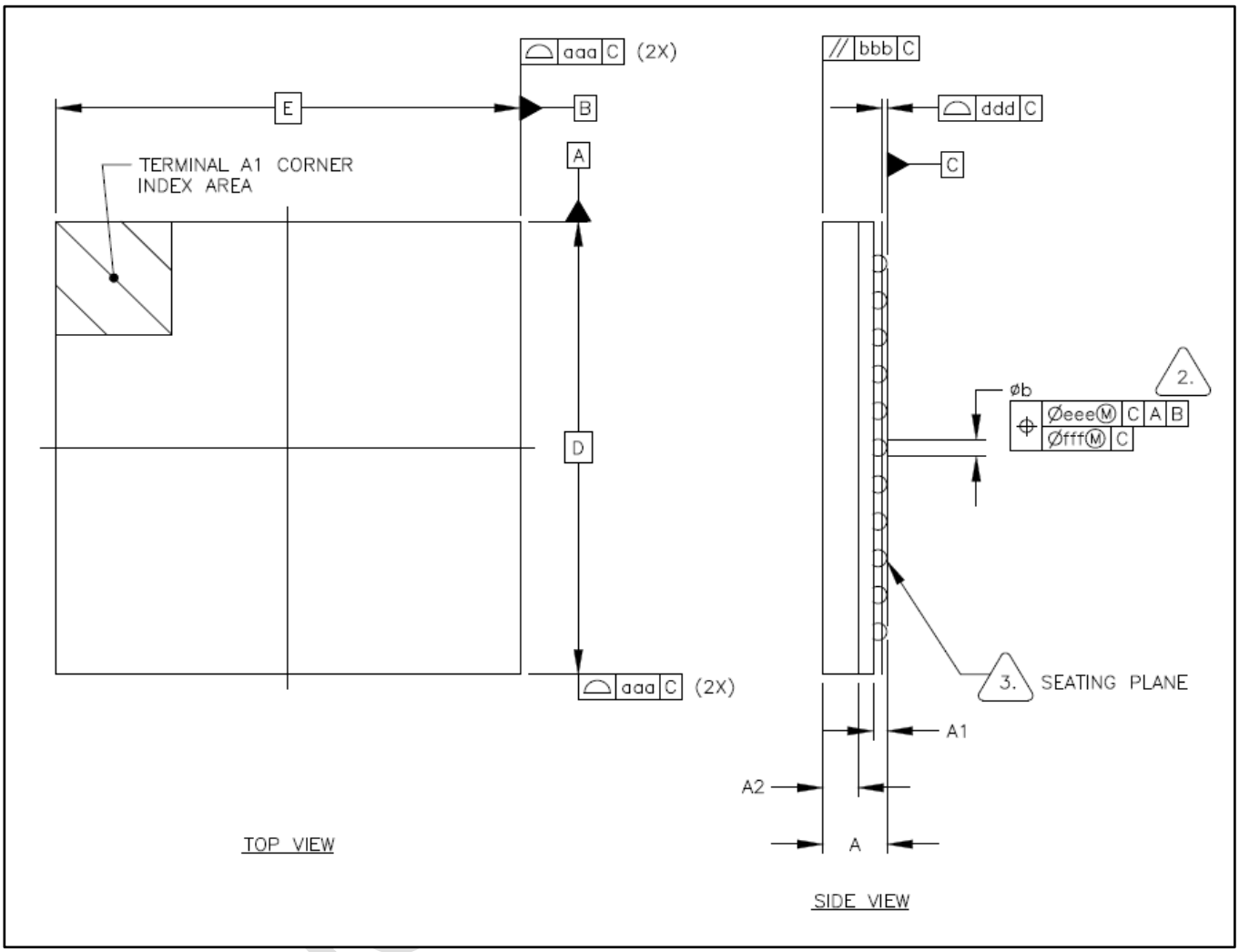


Figure 7.1 N4 121-BGA-8x8 Package Information(Top and Side view)

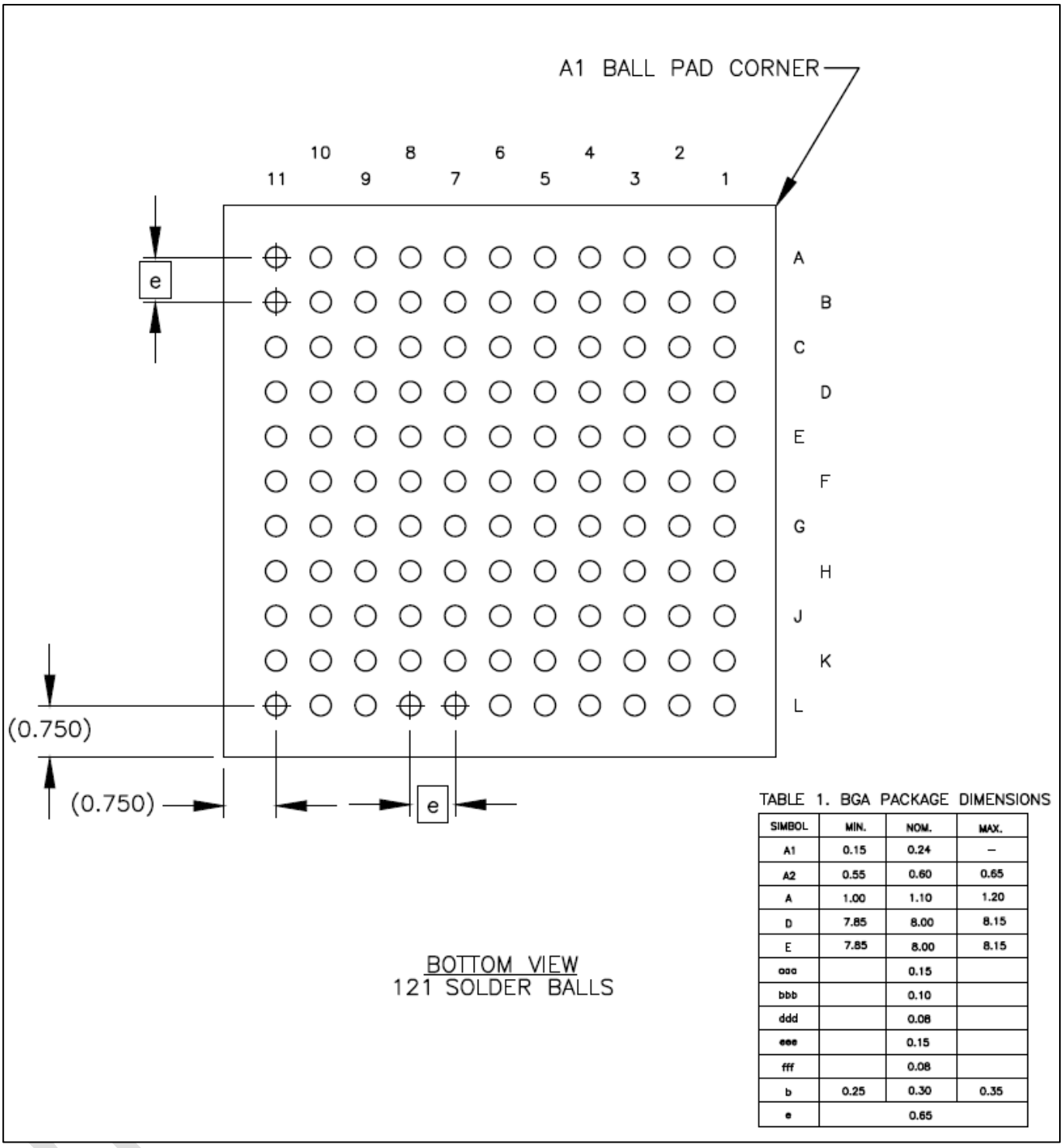


TABLE 1. BGA PACKAGE DIMENSIONS

SIMBOL	MIN.	NOM.	MAX.
A1	0.15	0.24	–
A2	0.55	0.60	0.65
A	1.00	1.10	1.20
D	7.85	8.00	8.15
E	7.85	8.00	8.15
aaa		0.15	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.08	
b	0.25	0.30	0.35
e		0.65	

Figure 7.2 N4 121-BGA-8x8 Package Information(Bottom view)