Techpoint

TP2815

Quad HD-TVI / CVBS / HD Analog Video Decoder with Single MIPI-CSI2 Output, Bi-directional Data Channel

Preliminary Data Sheet

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1 Introduction

1.1 Description

TP2815 is the universal HD/SD video decoder supporting High Definition Transport Video Interface (HD-TVI) video, NTSC/PAL CVBS video as well as common HD analog video format decoding. It integrates 4 multi-standard decoders for simultaneous 4 channels decoding of existing HD analog format. It also can work with any legacy CVBS camera for backward compatibility.

The primary application is for Automotive HD AVM or any other applications require transport of HD video for extended reach. TP2815 has internal clamping, automatic gain control amplifier on each channel for optimal signal conditioning. It also incorporates Anti-aliasing filter to reduce crosstalk. Its programmable equalization amplifier and automatic control loop maintain the best performance when using low quality and long cable.

TP2815 does majority of the signal processing digitally for its consistency and performance. All control loops are programmable for maximum flexibility. All pixel data are line-locked sampled. It has programmable picture control functions for flexible video quality adjustment. Working with compatible encoders and host controller, it supports 2-way data communication over the same video cable. For the legacy SD CVBS signal, it can also provide programmable upstream data support. The video outputs are flexible and compatible with MIPI-CSI2 v1.1 protocol. Multiple channels outputs are supported through standard MIPI virtual channel format configuration.

1.2 Features

- Supports 4-CH HD-TVI and other HD analog video decoding up to FHD 1080P30/25 resolution
- Supports 4-CH NTSC/PAL CVBS video decoding

Input

- High speed 10-bit Analog-to-Digital converters (ADC) for 2X over-sampling
- Programmable DC restoration or clamp control
- Programmable gain amplifier (PGA) and Automatic Gain Control (AGC) for best S/N performance
- Programmable Anti-aliasing low pass filter
- Embedded Equalizer (EQ) amplifier for best extended reach performance
- Adaptive EQ algorithm for different cable characteristics.

Signal Processing

- Brightness, Contrast, Saturation, Hue and Sharpness control through host interface
- Supports SMPTE-296M and SMPTE-274M standard sampling for HD and FHD signals
- Advanced Sync processor for best low signal performance
- Internal digital Horizontal PLL for Line-Locked sampling
- Internal digital Color PLL for accurate color demodulation
- Color gain control and programmable color killer for best small signal performance
- Internal digital filters for HD Y/C separation
- Integrated high quality adaptive 4H comb filter YC separation for NTSC/PAL CVBS decoding to minimize false color and cross luminance artifacts.
- Free run mode with optional blue screen

Output

- MIPI CSI-2 1.1 compliant transmitter up to 4 lanes
- Supports flexible Virtual Channel forwarding engine for multiple lanes operation
- Supports non-standard pseudo frame mode

Audio

- 5 mono analog audio channels with 10-bit ADC and digital processing
- Supports down stream coaxial audio over video processing for all channels independently
- Built-in programmable gain control and anti-aliasing filter for each channel
- Single channel audio DAC with reconstruction filter and gain control.
- Support 8 or 16KHz sampling rate
- I2S interface support single/multiple output with mixing capability
- Cascade-able up to 4 devices with mixed coaxial and base-band audio selection.

General

- Up-stream data insertion through host interface
- Programmable down-stream data decoding
- Fast 2-wire serial host interface
- Power down mode
- Internal PLL for clock generation
- 1.2/3.3/1.8V operation
- 88pin QFN
- Single 27MHz clock operation

2 Order Information

Package Description

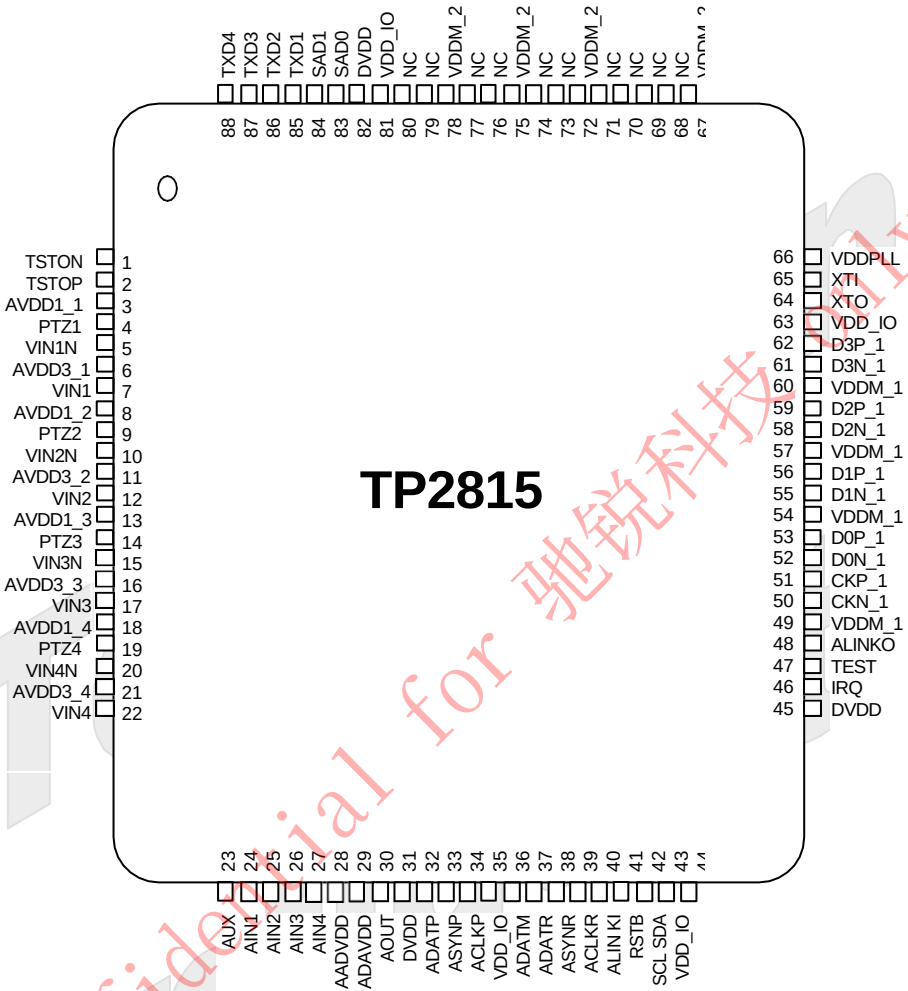
Part #	Name	Description	Pin Count	Body Size
TP2815-NA1*	EPQFN 88L	Quad Flat No Lead Package with Exposed Pad	88	10 x 10 mm^2

Note:

* Industrial Grade

3 Pin Diagram

88L QFN (Top View)



3.1 Pin Description(88L)

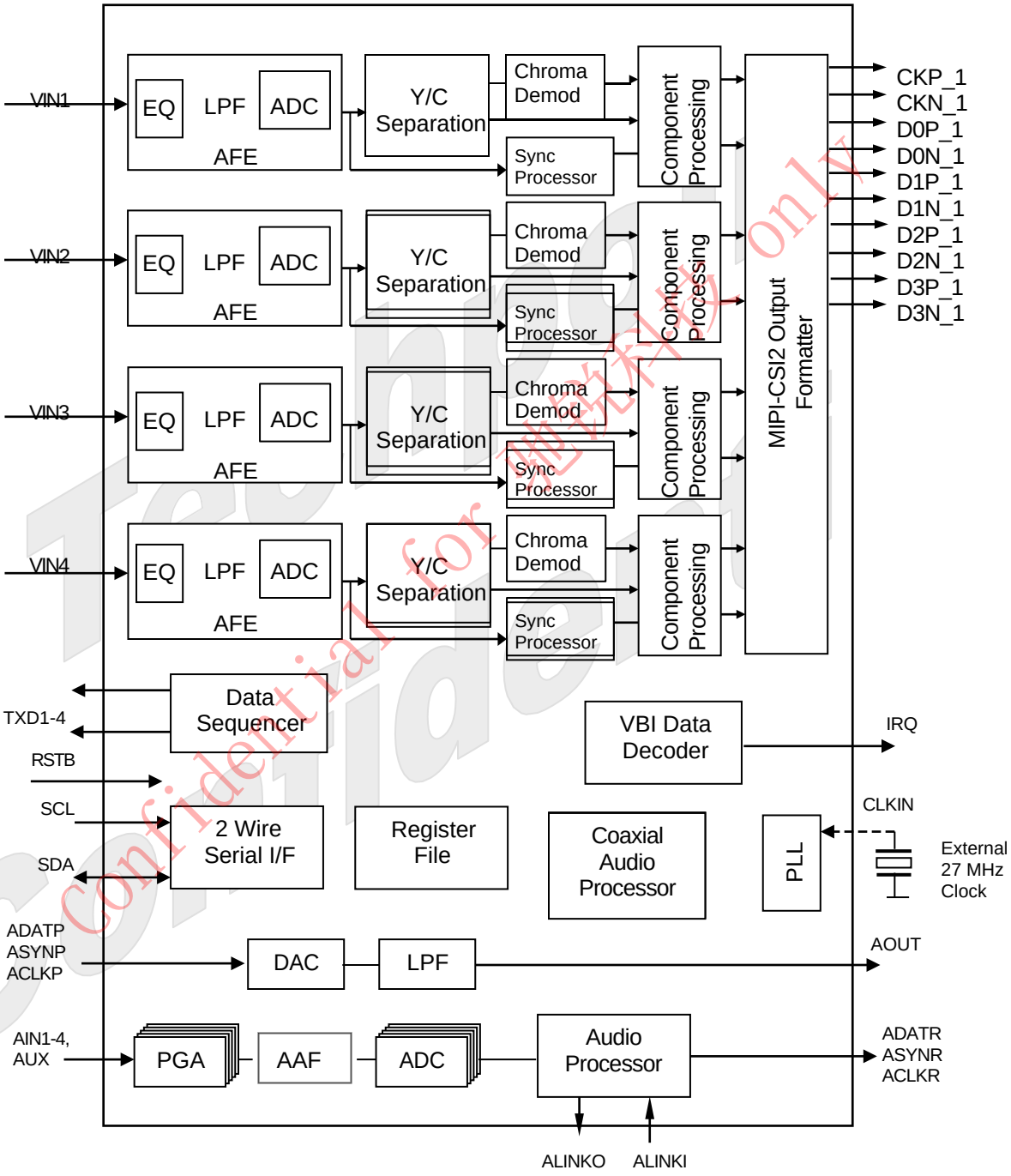
Pin#	I/O	Pin Name	Description
Analog Section			
7, 12, 17, 22	I	VIN1-4	Analog Video input. The signal should be AC coupled in by 0.1uF
5, 10, 15, 20	I	VIN1-4N	Multi-function pins. These signals should be AC coupled by 0.1uF to the negative video input or ground.
4, 9, 14, 19	O	PTZ1-4	Multi-function pins. Left unconnected.
3, 8, 13, 18	P	AVDD1_1-4	Analog 1.2V power supply
6, 11, 16, 21	P	AVDD3_1-4	Analog 3.3V power supply
66	P	VDDPLL	Analog 1.2V PLL power supply
1, 2	O	TSTON,TSTOP	Analog Test Pins. Unconnected during normal operation
24,25,26,27	I	AIN1-4	Analog audio input
23	I	AUX	Analog audio AUX input
30	O	AOUT	Analog audio output
28, 29	P	AADVDD, ADAVDD	Analog 3.3V power supply
MIPI Section			
50	O	CKN_1	MIPI port 1 Clock output (negative)
51	O	CKP_1	MIPI port 1 Clock output (positive)
52	O	D0N_1	MIPI port 1 Lane 0 data output (negative)
53	O	D0P_1	MIPI port 1 Lane 0 data output (positive)
55	O	D1N_1	MIPI port 1 Lane 1 data output (negative)
56	O	D1P_1	MIPI port 1 Lane 1 data output (positive)
58	O	D2N_1	MIPI port 1 Lane 2 data output (negative)
59	O	D2P_1	MIPI port 1 Lane 2 data output (positive)
61	O	D3N_1	MIPI port 1 Lane 3 data output (negative)
62	O	D3P_1	MIPI port 1 Lane 3 data output (positive)
49, 54, 57, 60	P	VDDM_1	MIPI port 1.2V Supply

Pin#	I/O	Pin Name	Description
67, 72, 75, 78	P	VDDM_2	MIPI port 1.2V Supply
Digital Section			
65	I	XTI	Clock input
64	O	XTO	Clock Output
83	I	SAD0	The MPU Serial interface Chip Address Select bit0
84	I	SAD1	The MPU Serial interface Chip Address Select bit1
42	I	SCL	The MPU Serial interface Clock Line
43	B	SDA	The MPU Serial interface Data Line
41	I	RSTB	Reset input. Low active
46	O	IRQ	Interrupt signal output
85	O	TXD1	CH1 Up stream data signal output
86	O	TXD2	CH2 Up stream data signal output
87	O	TXD3	CH3 Up stream data signal output
88	O	TXD4	CH4 Up stream data signal output
47	I	TEST	Test pin
32	B	ADATP	Audio Digital Data for Playback
33	B	ASYNP	Audio Sync for Playback
34	B	ACLKP	Audio Clock for Playback
36	O	ADATM	Audio Digital Data M for Record
37	O	ADATR	Audio Digital Data R for Record
38	B	ASYNR	Audio Sync for Record
39	B	ACLKR	Audio Clock for Record
40	I	ALINKI	Audio Digital Data for Cascade Input
48	O	ALINKO	Audio Digital Data for Cascade Output
35, 44, 63, 81	P	VDD_IO	Digital 3.3V/1.8V power supply
31, 45, 82	P	DVDD	Digital 1.2V power supply
Exposed Pad	P	GND	Connect to system ground

I = Input, O=Output, B=Bidirectional, P=Power

4 Functional Description

4.1 Block Diagram



4.2 Analog Front End(AFE)

The analog front-end conditions and digitizes the AC coupled HD-TVI signal or conventional CVBS signal for further processing. It consists of EQ (equalizer), LPF (anti-alias filter), PGA (Programmable Gain Amplifier), clamp circuits and 10-bit over-sampling high speed ADC (Analog-to-Digital Converter). The clamping circuit restores the DC component of the input signal to establish the proper black level. The PGA together with its control loop compensates for the signal amplitude irregularity due to channel condition and mismatches. It can support a signal variation of +-6dB. The EQ and its associated feedback loop compensates for the high frequency signal loss due to long cable transmission. The LPF removes signal images due to sampling process and prepares it for digitization. The filter order and corner frequency can be controlled through register. Both EQ and PGA can both operate in automatic and manual modes through register control. The high speed ADC has 10-bit resolution.

4.3 Sync Processor

The sync processor of TP2815 extracts the horizontal synchronization and the vertical synchronization signals in the video signal. The processor contains digital phase-locked-loops and decision logic to achieve reliable sync detection in various signal conditions. Minor irregularity in the sync period due to noise can be filtered out. It can also generate free run signal during video loss and allows the sampling of the video signal in line-locked fashion.

4.4 Y/C separation

The Y/C separation module separates the luminance and chrominance components of the HD-TVI signal for further processing. This is achieved by simple low-pass and band-pass filter combination due to the spectrum allocation of the luma and chroma signals. For the CVBS signal, a 4H/5-line adaptive comb filter is employed to achieve the high quality 2D Y/C separation. It minimizes the artifacts typically associated with CVBS signalseparation.

4.5 Chroma demodulation

The chroma demodulation of the HD-TVI or CVBS signal is done by quadrature down mixing and low-pass filtering. The local carrier signal for use in the quadrature demodulation is generated by direct digital synthesis PLL that locks onto the input sub-carrier reference signal on every scan line. This arrangement allows the demodulation to be done easily with single crystal frequency.

4.6 Automatic Chroma Gain Control

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by high-frequency loss in video signal. The range of ACC controls are –6db to +26db.

4.7 Color Killer

For low color amplitude signals, black and white video, or noisy signals, the color will be “killed” for easy viewing. The color killer uses the burst amplitude measurement as well as sub-carrier PLL status to switch off the color in theoutput.

4.8 Component Processing

The TP2815 supports the typical brightness, contrast, color saturation and hue adjustment for changing the output videocharacteristic.

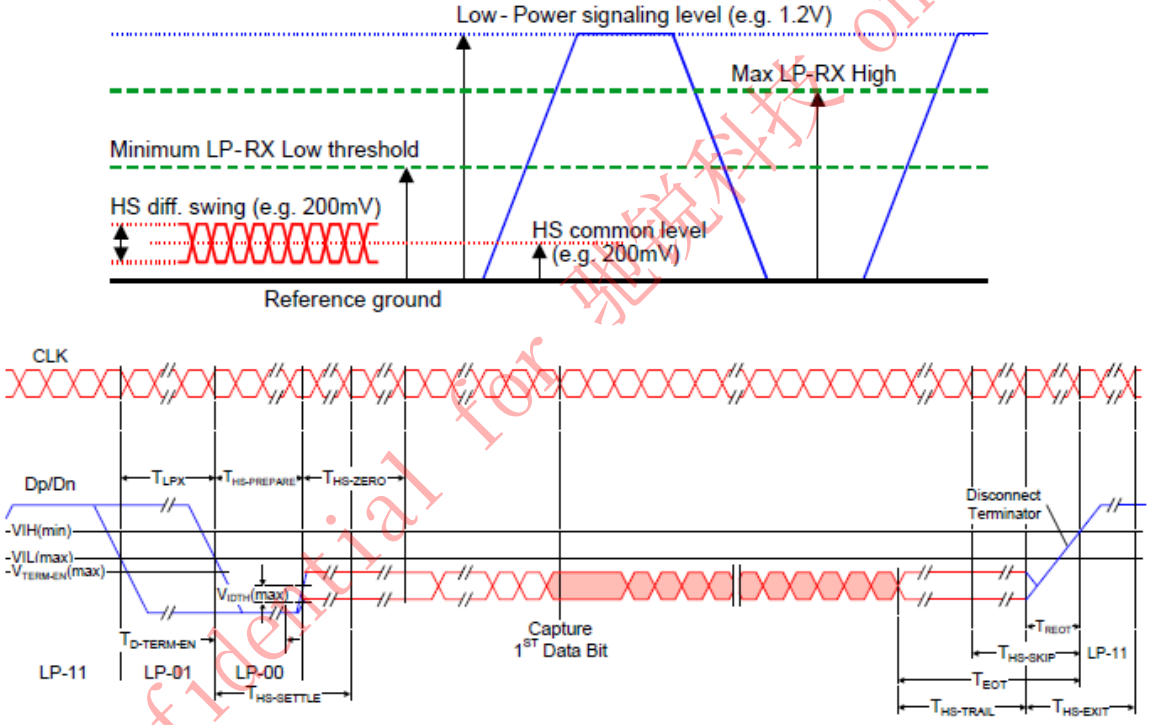
4.9 Sharpness

The TP2815 also provides a sharpness control function through control registers. The center peaking frequency depends on the operating modes.

4.10 MIPI Output

The TP2815 contains a single independent MIPI transmitter port compatible with MIPI CSI-2 v1.1 interface and D-PHY v1.1 standards.

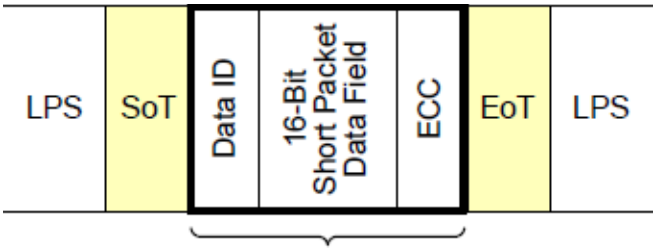
The MIPI transmitter consists of a low level protocol module that handles all necessary header insertion and mode control and the MIPI physical layer module that handles data conversion and MIPI compatible signal level generation. The D-PHY uses a combination of High Speed Differential Signaling (HS) and Low Power Signaling (LP) to communicate with the MIPI receiver on the other side of the link. The LP signals use their relative voltage levels to communicate state information.



• Figure 1 D-PHY LP & HS Line Levels & Data Burst Transmission

A D-PHY burst transmission consists of the LP state changes signalling a Start of Transmission (SoT), followed by the payload data, then a transition to the Stop state (also called the Low Power State) signalling the End of Transmission (EoT).

CSI-2 transmissions consist of either short packets or long packets. Short packets are used to transmit Frame Start (FS) and Frame End (FE) signals at the beginning (before the first active horizontal line) and end (after the last active line) of a full video frame. Long packets are used to transmit a single horizontal line of video at a time. The packet structure for short and long packets are shown in the figures below.



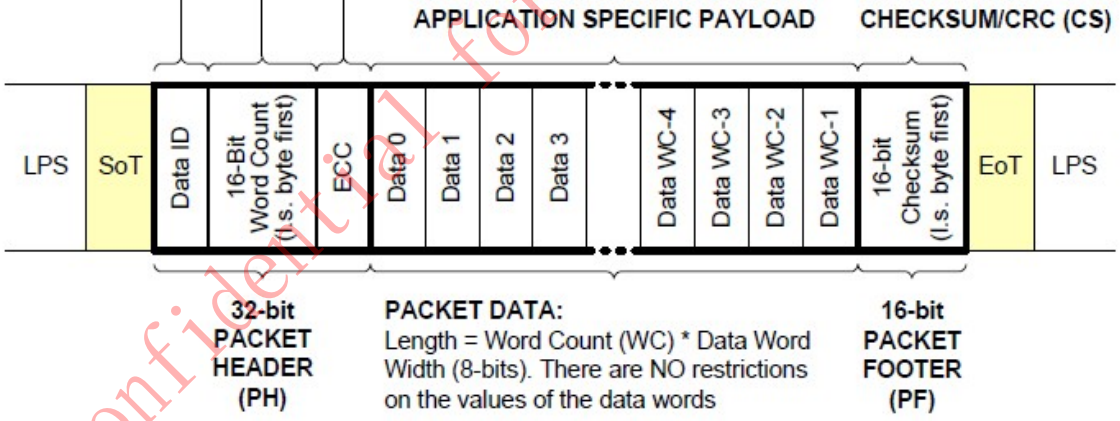
32-bit SHORT PACKET (SH)
Data Type (DT) = 0x00 – 0x0F

Figure 2 Short Packet Structure

DATA IDENTIFIER (DI):
Contains the Virtual Channel Identifier and the Data Type Information
Data Type denotes the format/content of the Application Specific Payload Data.
Used by the application specific layer.

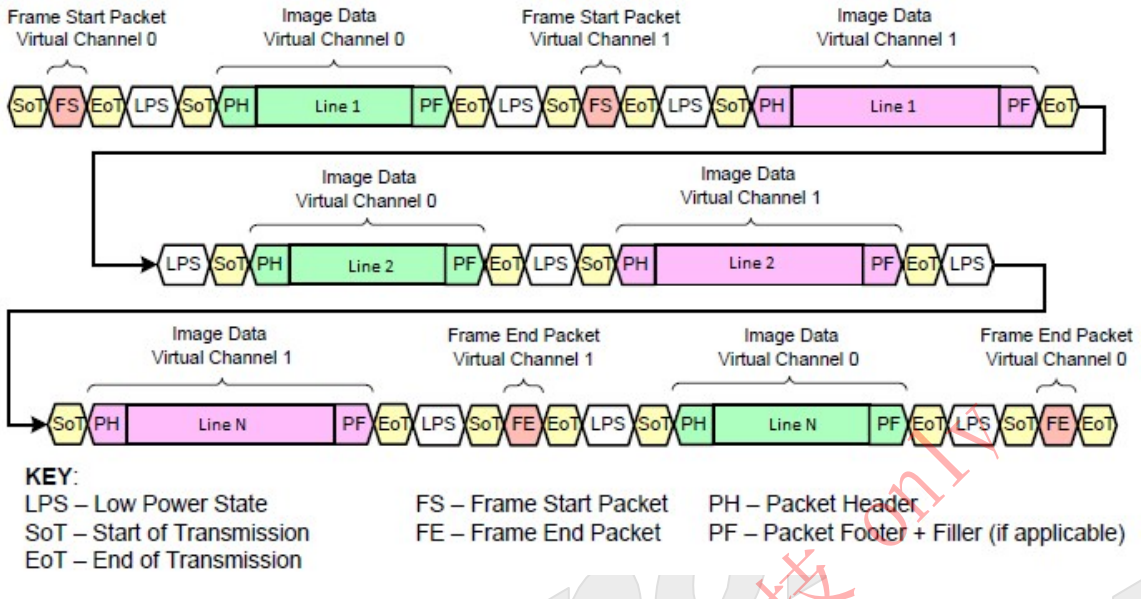
16-bit WORD COUNT (WC):
The receiver reads the next WC data words independent of their values. The receiver is NOT looking for any embedded sync sequences within the payload data. The receiver uses the WC value to determine the end End of the Packet

8-bit Error Correction Code (ECC) for the Packet Header:
8-bit ECC code for the Packet Header. Allows 1-bit errors with the packet header to be corrected and 2-bit errors to be detected



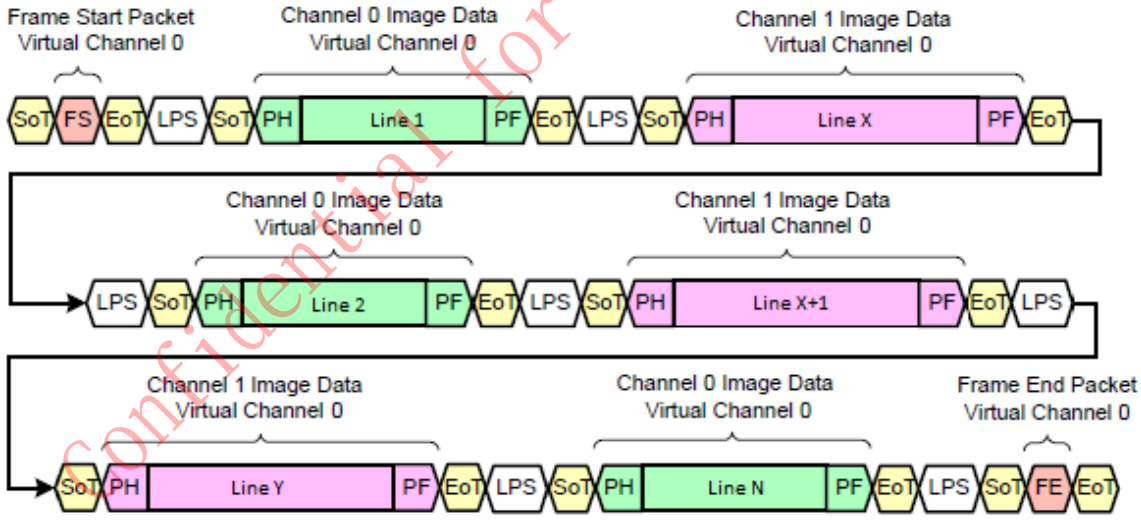
• Figure 3 Long Packet Structure

The protocol module can take up to 4 independent video channels data stream of the same format that have been multiplexed into a single data stream on a per line basis. These channels can be transmitted over the MIPI interface in one of two ways. The first way uses the MIPI Virtual Channel (VC) Identifier in the upper two bits of the Data ID byte of the packet to distinguish between the channels. All channels have their own independent FS and FE packets to identify the first and last lines of the frame.



• Figure 4 Interleaved Data Transmission Using Virtual Channels

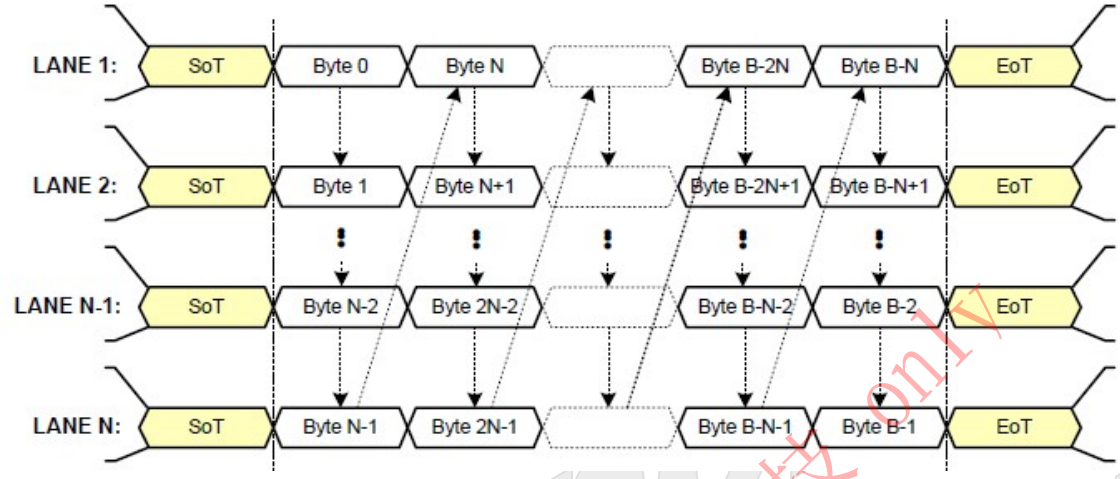
The second way of multiplexing multiple channels over the MIPI interface uses a Pseudo Single Frame Mode (PSFM) of operation over a single Virtual Channel. Only the first channel has accurate FS and FE signals which may be asynchronous to the others. A 4-byte header is added to the start of the packet data containing information necessary to sync to the frame. An individual packet still contains a single line from one of the channels.



• Figure 5 Interleaved Data Transmission Using PSFM

After the protocol handling, it is then de-multiplexed into 1 or 2 or 4 data lanes following the MIPI CSI-2 specification before forwarding to the analog D-PHY module for data seralization and level conversion. In addition, the MIPI interface may be split into two independent channels of two data lanes each, sharing a common clock lane. This “dual-mode” uses 2 CSI protocol blocks, each capable of taking any of the four video channels. In this mode, CSI-0 always outputs to data lanes 0 & 1, and CSI-2 outputs to lanes 2 &3.

The first byte of data is always sent on data lane 1. If 2 or more lanes are used, the second byte will be sent on data lane 2 and so on. If the number of bytes sent is not divisible by the number of lanes, any lanes without a byte to send at the final byte time will enter the EoT sequence.



• Figure 6 N-Lane D-PHY Byte Ordering

The MIPI transmitter supports various combination of input channel and output lanes provided the maximum output data rate is less than 1.54Gb/s. The minumum data rate should be at least 148Mb/s. An on-chip PLL generates all necessary clocks from a 27MHz crystal or clock input.

4.11 Audio

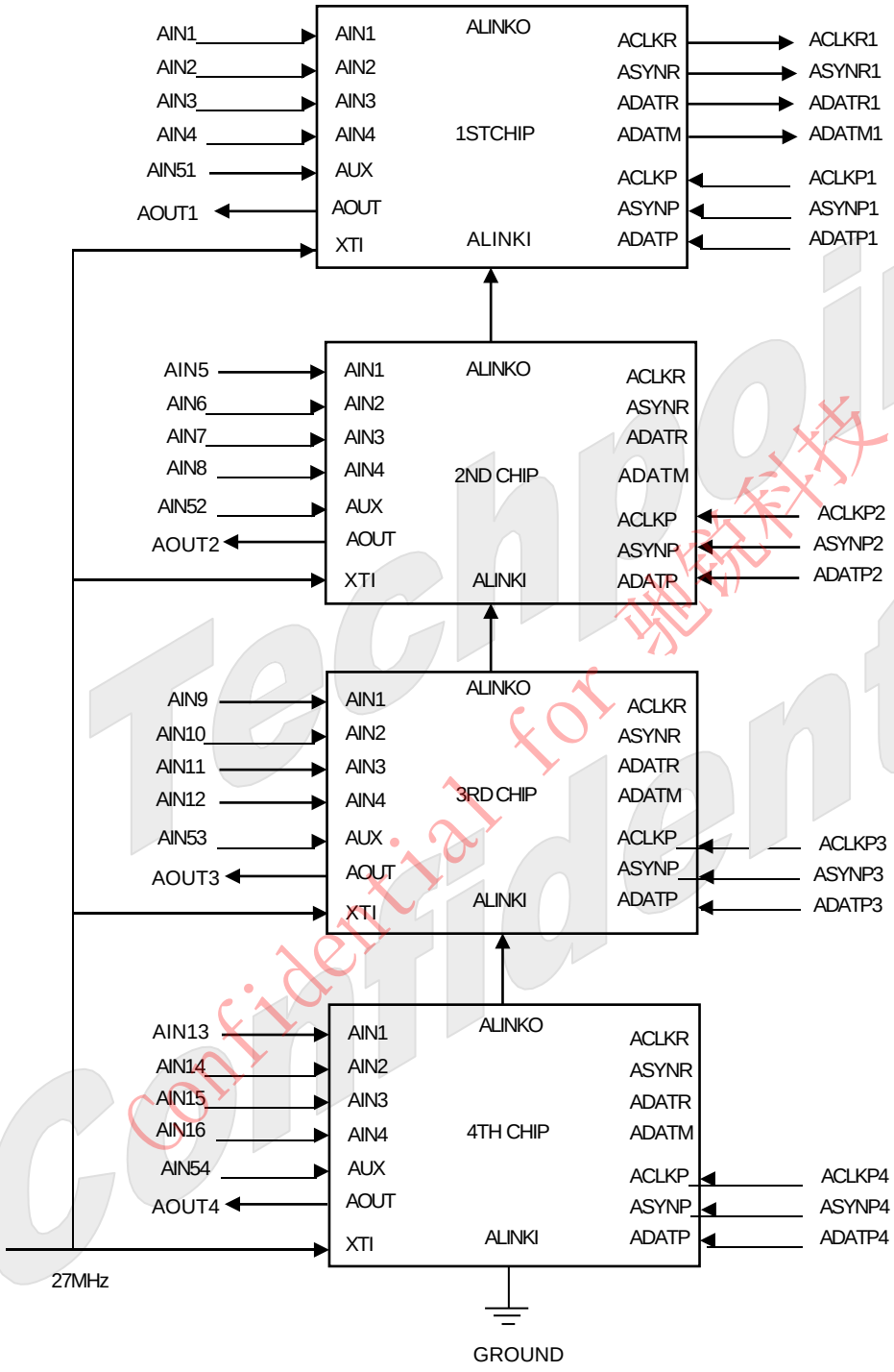
The audio input module integrates a 5-Ch audio front-end, analog-to-digital converter, digital processing circuits and I2S encoder. It supports 5-Ch mono analog audio inputs with single/multiple I2S output with the capability of cascading up to 4 devices and 16-Ch audio inputs. Each analog channel has programmable gain control block and built-in anti-aliasing filter. The digitization supports the standard 8 and 16 KHz sampling rate.

In addition to the base band audio channels, it also supports over-the-video-cable coaxial audio processing for every video channel. All of these audio channels can be mixed or selected for recording or playback.

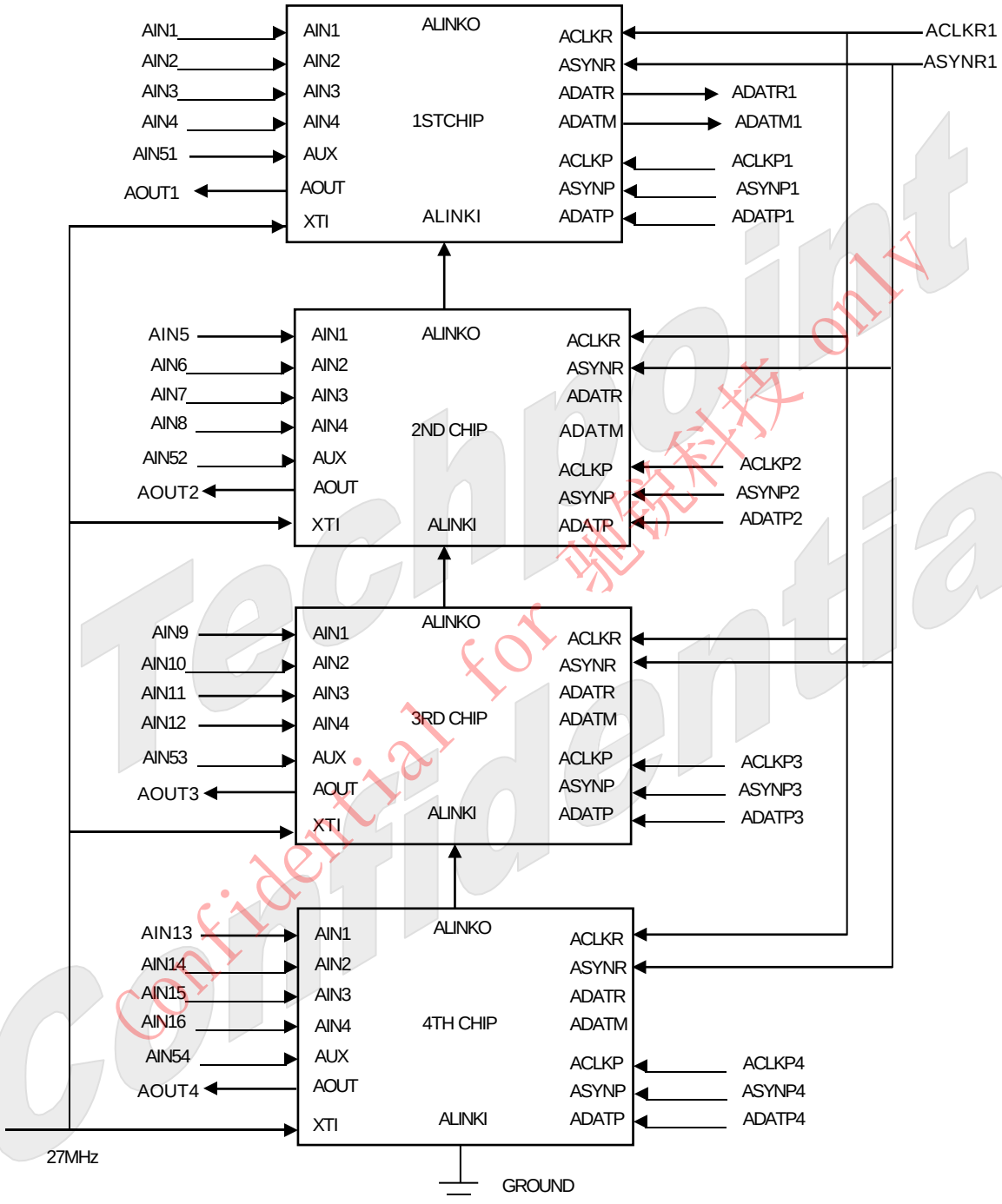
The audio output module integrates I2S input module, an audio digital-to-analog converter (DAC) and reconstruction filter with output level control capability.

All cascaded chips need to share one clock source for their XTI pin input in order for the audio cascade mode to function properly.

Following pages show typical audio cascade system. TP2815 support up to 4 digital audio playback ACLKP/ASYNP/ADATP input. System may also select only necessary ACLKP/ASYNP/ADATP in 4 digital audio playback input. Unused ACLKP/ASYNP/ADATP can be no connection.



Master mode audio cascade



Slave mode audio cascade

4.12 Power Management

The TP2815 can be put into power-down mode through software control.

4.13 Host Interface

The TP2815 registers are accessed via 2-WIRE serial interface that is compatible to standard I2C protocol. It operates as a slave device. Serial clock and data lines, SCL and SDA, transfer data from the bus master at a rate up to 400 Kbits/s. The TP2815 has two serial interface address select pins (SAD1/SAD0) to program up to four unique serial addresses. This allows TP2815 to share the same serial bus with other system components without address conflict.

Its device ID can be programmed through pin configuration based on following table.

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	SAD1	SAD0	1=Read 0=Write

5 Parametric Information

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVDD3, AVDDPLL to Ground	-	**-0.5**	-	4.0	V
AVDD1 to Ground		**-0.5**	-	1.6	V
DVDD to Ground	-	**-0.5**	-	1.6	V
VDD_IO to Ground	-	**-0.5**	-	4.0	V
Digital Signal Input Pin to Ground	-	-0.5	-	VDD_IO+ 0.5	V
Analog Input Voltage	-	Ground – 0.5	-	1.92	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C

NOTE: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect devicereliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the ranges list in above table can induce destructive latch-up.

5.2 Recommended Operation Condition

5.2.1 Power Supply

Parameter	Symbol	Min	Typ	Max	Units
Power Supply — IO(3.3/1.8V)	VDD_IO	3.15/1.7	3.3/1.8	3.45/2.0	V
Power Supply — Analog 3.3V	AVDD3	3.15	3.3	3.45	V
Power Supply — Analog 1.2V	AVDD1	1.1	1.2	1.3	V
Power Supply — Digital	DVDD	1.1	1.2	1.3	V
Maximum $\|V_{DD\_IO} – AVDD\|$		-	-	0.3	V
Ambient Operating Temperature (Industrial)	T_A	-40		+85	°C

5.2.2 Reference Clock Input

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (XTI)(3.3/1.8V)	V_{IH}	2.0/1.5	-	VDD_IO + 0.5/0.2	V
Input Low Voltage (XTI)(3.3/1.8V)	V_{IL}	-	-	0.8/0.6	V
Input Clock Frequency	Fclk		27		MHz
Crystal Spec (when supported)					
Nominal frequency (fundamental)		-	27	-	MHz
Deviation base on normal operation condition		-50	-	+50	ppm
Load capacitance	CL	-	20	-	pF
Series resistor	RS	-	80	-	Ohm

Oscillator Input					
Nominal frequency		-	27	74.25	MHz
Deviation		-50	-	+50	ppm
Duty cycle		-	-	55	%

5.3 AC/DC Characteristic

5.3.1 Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
Digital Core +MIPI Supply current	DVDD		168/177/268/287 *	320	mA
Analog AFE+ADC Supply current	AVDD	-	127/127/131/131 *	139	mA
PLL Supply current	AVDDPLL	-	7	8	mA
Analog Supply current	AVDD3		50	79	
Audio Supply current	ADA AADVDD		28	30	
Digital Core Supply current	VDDIO		5	6	

* CVBS / 720P30/25 / 1080P30/25 /1080P60/50

5.3.2 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)(3.3/1.8V)	V_{IH}	2.0/1.5	-	-	V
Input Low Voltage (TTL)(3.3/1.8V)	V_{IL}	-	-	0.8/0.6	V
Input High Voltage (XTI)(3.3/1.8V)	V_{IH}	2.0/1.5	-	VDD_IO + 0.5/0.2	V
Input Low Voltage (XTI)(3.3/1.8V)	V_{IL}	-	-	0.8/0.6	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF
Digital Outputs					
Output High Voltage (I_{OH} = –12 mA)(3.3/1.8V)	V_{OH}	2.4/1.5	-	VDD_IO	V
Output Low Voltage (I_{OL} = 12 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF

5.3.3 Analog Electrical Characteristic

Parameter	Symbol	Min	Typ	Max	Units
Analog Input					
Analog Pin Input voltage	Vi	0.5	1	1.5	Vpp
Analog Pin Input Capacitance	C_A	-	7	-	pF

ADCs					
ADC resolution	ADCR	-	10	-	bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	-	160	MHz
Video bandwidth (-3db)	BW	-	70	-	MHz

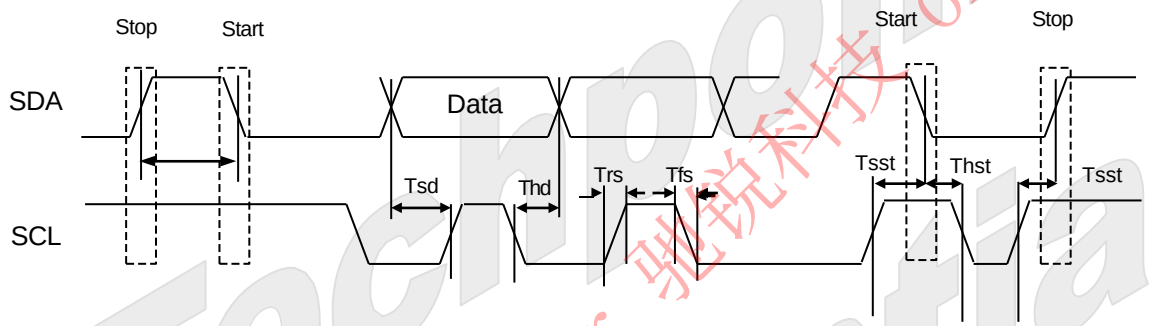
5.3.4 Decoder Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Horizontal PLL					
Line frequency	f_{LN}	15.625		45	KHz
Static deviation	Δf_H	-	-	6.2	%
Vertical PLL					
Frame/Field frequency	f_{LN}	15		60	KHz
Static deviation	Δf_H	-	-	5.5	%
Subcarrier PLL					
Lock in range (SPR=0) – HD 1080p, 720p60/50	$\Delta f_{S\text{-}HD}$	-		±4500	Hz
Lock in range (SPR=0) – HD 720p30/25	$\Delta f_{S\text{-}HD}$	-		±2200	Hz
Lock in range (SPR=2) - SD	$\Delta f_{S\text{-}SD}$	-		±800	Hz

5.3.5 Serial Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup time for start/stop condition	Tsst	200			ns
Hold time for start / stop condition	Thst	200			ns
Data setup time (write)	Tsd	250			ns
Data hold time (write)	Thd(w)	250	-		ns
SCL, SDA rise time	Trs			1000 / 300*	ns
SCL, SDA fall time	Tfs			300*	ns
SCL (Falling edge) to SDA delay time (read)	Thd(r)	250			ns
SCL clock frequency	fscl	-	100	400	KHz

Note: * Fast mode (400KHz)



5.3.6 HS Transmitter DC characteristics

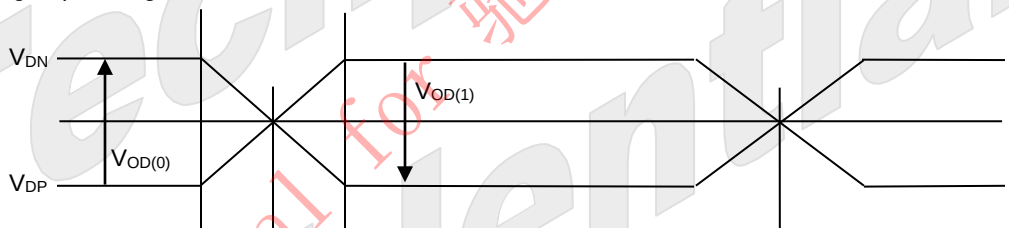
Parameter	Symbol	Min	Typ	Max	Units
HS transmit static common mode voltage 1*	VCMTX	150	200	250	mV
VCMTX mismatch when output is Differential-1 or Differnetial-0 2*	|ΔVcmtx(1,0)|			5	mV
HS transmit differential voltage 1*	|Vod|	140	200	270	mV
Vod mismatch when output is Differential-1 or Differential-0 1*	|ΔVod|			10	mV
HS output high voltage 1*	Vohhs			360	mV
Single-ended output impedance	Zos	40	50	62.5	Ω
Single-ended output impedance mismatch	ΔZos			10	%

Note:

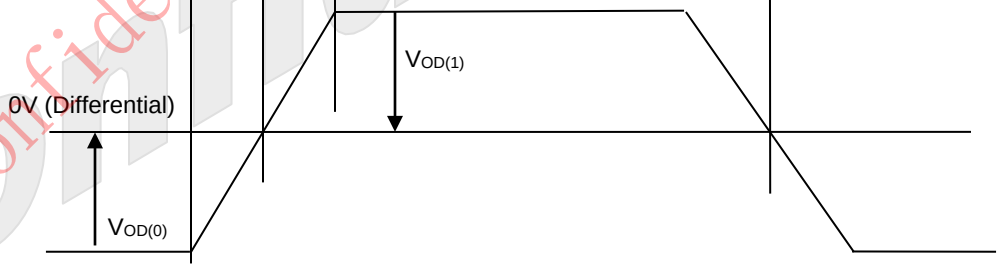
1*. The voltage level when driving into load impedance anywhere in the ZID range.

2*. A transmitter should minimize ΔVod and ΔVcmtx(1,0) in order to minimize radiation, and Optimize signal integrity.

Ideal Single-Ended High Speed Signals



Ideal Differential High speed signal



5.3.7 HS Transmitter AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Common-level variations above 450MHz	ΔVcmtx (HF)			15	mVrms
Common-level variations between 50-450MHz	ΔVcmtx (LF)			25	mVrms
Unit Interval Instantaneous	UIinst		6.7340 3.3670 1.6835 0.8417		ns
UI Variation (UI≥1ns)	ΔUI	-10		10	%
Clock Lane DDR Clock Frequency (= 1/(2*UIinst min)	fhmax		74.25 148.5 297 594		MHz
Data to Clock Skew (UI≥1ns)	Tskew	-0.15		0.15	UIinst
20%-80% rise time and fall time	tr and tf			0.3	UI 1*, 2*
				0.35	UI 1*, 3*
		150			Ps 4*

Note: The frequency 'fh' is the highest fundamental frequency for data transmission

1*. UI is equal to 1/(2*fh).

2*. Applicable when supporting maximum HS bit rates ≤ 1Gbps(UI ≥ 1 ns).

3*. Applicable when supporting maximum HS bit rates > 1Gbps(UI<= 1 ns) but less than 1.5Gbps(UI=>0.667ns)

4*. Applicable when supporting maximum HS bit rates <= 1.5Gbps. However, to avoid excessive radiation, bit rates < 1Gbps (UI ≥ 1ns), should not use values below 150ps.

5.3.8 HS Transmitter AC Characteristics – Global

Parameter	Symbol	Min	Typ	Max	Units
Time for the Data Lane receiver to enable the HS line termination	Td-term-en	Time for Dn to reach V-term-en		35 + 4 x Ulinst	ns
Transmitted time interval from the start of Ths-trail to the start of the LP-11 state to following a HS burst	Teot			105 + 12xUlinst	ns
Time that the transmitter drives LP=11 following a HS burst	Ths-exit	100			ns
Data Lane HS Entry	Ths-prepare	40 + 4xUlinst		85 + 6xUlinst	
Ths-prepare + time that the transmitter drives the HS-0 stat prior to transmitting the Sync sequence	Ths-prepare + Ths-zero	145 + 10xUlinst			ns
Time interval during which the HS receiver shall ignore any data Lane HS transitions, starting from the beginning of Ths-settle	Ths-settle	85 + 6xUlinst		145 + 10xUlinst	ns
Time interval during which the HS-RX should ignore any transitions on the data Lane, following a HS burst. He end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	Ths-skip	40		55 + 4xUlinst	ns
Data Lane HS Exit	Ths-trail	60 + 4xUlinst			ns
Transmitted length of LP state	Tlpx	50			ns
Recovery Time from Ultra Low Power State (ULPS)	Twakeup	1			ms

5.3.9 LP Transmitter DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Thevenin output high level 1*	Voh	1.1	1.2	1.3	V
Thevenin output low level	Vol	-50		50	mV
Output impedance of LP transmitter	Zolp	110			Ω

Note:

1 Applicable when the supported data rate <= 1.5 Gbps.

5.3.10 LP Transmitter AC Characteristics

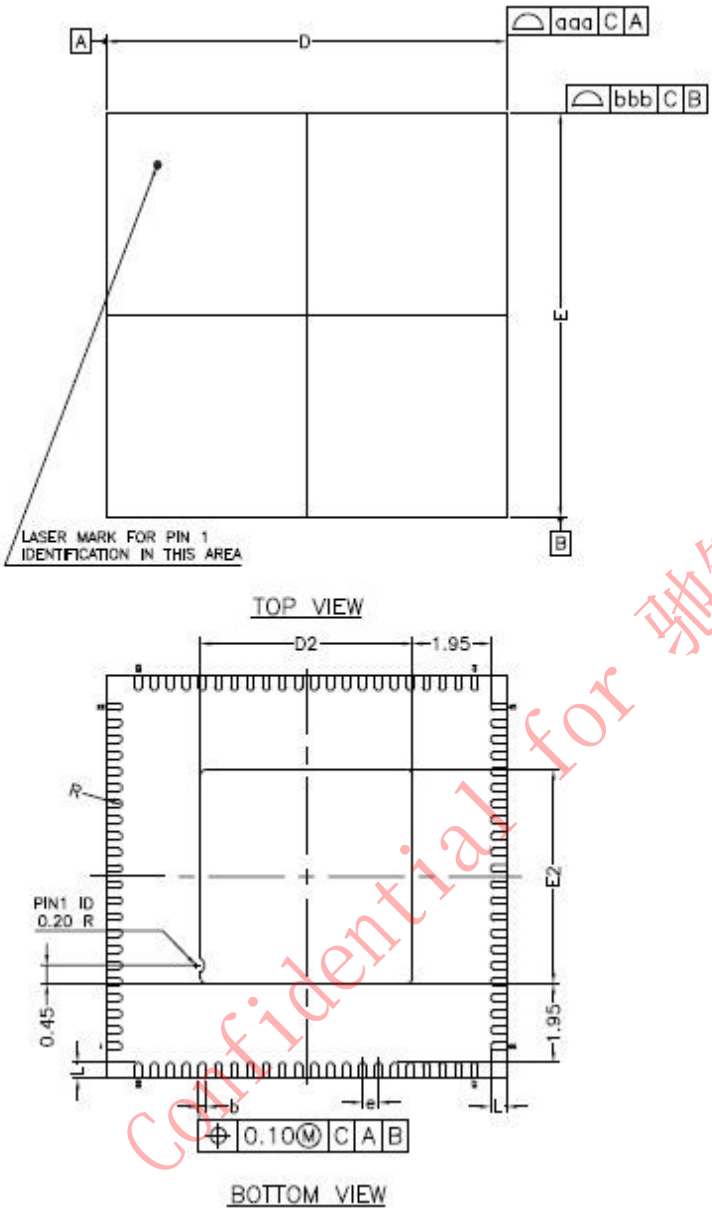
Parameter		Symbol	Min	Typ	Max	Units
15%-85% rise time and fall time 1*		Trlp/Tflp			25	ns
30% - 85% rise time and fall time Cload≤70pF		Treot			35	ns
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	Tlp-pulse-tx	40			ns
	All other pulses		20			ns
Period of the LP exclusive-OR clock		Tlp-per-tx	90			ns
Slew rate @Cload = 0pF 1*		ΔV/Δtsr			500	mV/ns
Slew rate @Cload = 5pF 1*					300	
Slew rate @Cload = 20pF 1*					250	
Slew rate @Cload = 70pF 1*					150	
Slew rate @Cload = 0 to 70pF (Falling Edge Only)			30			
			25			
Slew rate @Cload = 0 to 70pF (Rising Edge Only)			30			
			25			
Load Capacitance 1*		Cload	0		70	pF

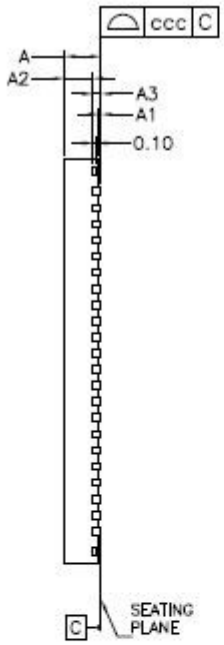
Note:

1*. Cload includes the low-frequenc equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distrited line capacitance can be up to 50pF for a transmission line with 2ns delay.

6 Mechanical Data

88 Pin EP-QFN





SIDE VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.025	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.13	0.18	0.23	0.005	0.007	0.009
D	10.00 bsc			0.394 bsc		
D2	5.20	5.30	5.40	0.205	0.209	0.213
E	10.00 bsc			0.394 bsc		
E2	5.20	5.30	5.40	0.205	0.209	0.213
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.065	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

7 Control Registers

7.1 TP2815 Register SUMMARY

*Index 00–3F, 79-88 are common for all channels and the PAGE register select the channel(s) affected by read/write to this register space when APAGE=0 and MPAGE=0.

Video Decoder

Index	7	6	5	4	3	2	1	0	Reset
00									11h
01	VDLOSS	VLOCK	HLOCK	SLOCK	VDET	EQDET	NINTL	CDET	-
02	MD1120	GMEN	OPLMT	F444	MD656	SD	P720	ITLC	C2h
03	EGAIN				SYWD	CVSTD			-
04	STATUS								-
05	NCY4								00h
06	SRESET	-	BGW	CKPLVD	ACSY	AGC_EN	AGCGAIN [8]	EQRST	32h
07	BPASS2	EQ_EN	EQGAIN						40h
08	AGCGAIN [7-0]								00h
09	MAXEN	DETEN	EQREF						24h
0A	MAXTH				EQHY				48h
0B	BPASS1	TL_EN	TFREQ	TLGAIN					40h
0C			EQSY	FSEL	TLHY				43h
0D	FLT	PBW	FS4	COMB	YCMB	SDSTD			50h
0E	-	-	-	CMCP					00h
0F	UOFF				VOFF				00h
10	-	BRIGHTNESS							00h
11	-	CONTRAST							40h
12	-	UVGAIN							40h
13	HUE								00h
14	HGM	NMD	SHARPNESS						00h
15		HDELAY [10-8]			AO	YDLY			13h
16	HDELAY [7-0]								15h
17	HACTIVE [7-0]								00h
18	VDELAY [7-0]								19h
19	VACTIVE [7-0]								D0h
1A	VACTIVE [11-8]				HACTIVE [11-8]				25h
1B		RDSEL			-				00h
1C	YCM	-	-	NPXL [12-8]					06h
1D	NPXL [7-0]								72h
1E	HPXL								80h
1F	VLNN								80h

Index	7	6	5	4	3	2	1	0	Reset
20	PCLAMP								30h
21	WPGN				CLPGN				86h
22	SYHT								38h
23	CLMP								3Ch
24	-	FR	FMT		NMGN				04h
25	PKWT								FFh
26	CLEN	CKLY	GTST	SFLT	CBW		PSP	CLMD	05h
27	MP	UE	UG						2Dh
28	VLCKOUT		VLCKIN		VMODE	DETV	AFLD	VINT	00h
29	LOSSCNT				HSWIN				48h
2A	CKLM	CFQ			FCS	LCS	HPM		30h
2B	CKILLHY		CGAINMAX						4Ah
2C	FQEN	CHLOK	SPR		ACCT		SPM		0Ah
2D	PGATE								30h
2E	CGAINTH								70h
2F	TEST								00h
30	BFSTD [27-20]								48h
31	BFSTD [19-12]								BAh
32	BFSTD [11-4]								2Eh
33	BFSTD [3-0]				HS	HPRNG	FGAP		90h
34				CIDEN	CHID				00h
35	A135	DS2	FSL	-	-				05h
36	-								DCh
37	-								00h
38	CL_ISET	AFE_ISET			DIF_EN	DIFCM		IB_ISET	40h
39	LPF_VM	LPF_S2	EQ_SEL		LPF_SEL		VCOM_SEL		0Eh
3A	EQ1BP	EQ1FQ			EQ2BP	EQ2FQ			32h
3B	ADC_CTL								25h
3C									00h
3D	ADC_PD	T_PD_B	PD_CLP		PD_BUF	PD_LPF	PD_EQ	PDA	60h
3E	AFE_CTL				T_AFE			TO_EN	00h
3F	-								00h

Coaxial Audio Decoder

80		ADDI					AUDSS	AUDMD	50h
81	CADET			AGAP					10h
82	AUDSTRT								18h
83	AUDPOS								3Eh
84	AUDLEN								15h
85	ADDS [23-16]								07h
86	ADDS [15-8]								0Fh
87	ADDS [7-0]								A5h
88	AUDTH								58h

Special UP Data Channel

D8	AUGEN	ATONE	AUGORD	AUGDMD	AUGSB	AUGFMT	AUGMD	**00h**
D9	AUGWD							**68h**
DA	AUGHDLY [7-0]							**C0h**
DB	AUGDR		AUGSPLN					**18h**
DC	AUGHDLY [8]	AUGVST						**10h**
DD	AUGVLEN							**10h**
DE	AUGSTUS							**-**
DF	AUGDAT							**-**

General Control

* Following Index can be read/write accessible when APAGE=0 and MPAGE=0

Index	7	6	5	4	3	2	1	0	Reset
40		APAGE			MPAGE	ALLWE	PAGE		**00h**
41	PTZ TEST	TADC_SEL				TAFE34	TAFE12	PDTAFE	**01h**
42	CLKSELVD2		CLKSELVD1		CLKSELPHY		CLKSELCSI		**00h**
43	CLKSELSYS2				CLKSELSYS1				**00h**
44	CLKSELSYS4				CLKSELSYS3				**00h**
45		CLKSEL AUG	CLKSELIRQ	PDPORTCLK		VDCKEXT SYNCSEL	PD_PTZ		**00h**
B3	IRQLEN								**FAh**
B4				AUXIRQ	AIN4IRQ	AIN3IRQ	AIN2IRQ	AIN1IRQ	**00h**
B5	V4HIRQ	V3HIRQ	V2HIRQ	V1HIRQ	V4IRQ	V3IRQ	V2IRQ	V1IRQ	**00h**
B6	V4RXIRQ	V3RXIRQ	V2RXIRQ	V1RXIRQ	V4TXIRQ	V3TXIRQ	V2TXIRQ	V1TXIRQ	**00h**
B8	V4IRQMD		V3IRQMD		V2IRQMD		V1IRQMD		**00h**
B9					HL4IRQEN	HL3IRQEN	HL2IRQEN	HL1IRQEN	**00h**
BA			AUXIRQMD						**00h**
BB	AIN4IRQMD		AIN3IRQMD		AIN2IRQMD		AIN1IRQMD		**00h**
BE	IRQCLRMD		IRQ EDGE	IRQPOL	TESTIRQ	MBIST	TESTMODE		**00h**

Digital Ports and MISC Control

F0					OCK148		PLL297		**00h**
F1						VD1LMD	SYSLD		**00h**
F4	VCKRST				SYSCLK4PD	SYSCLK3PD	SYSCLK2PD	SYSCLK1PD	**00h**
F5	VADCK4POL	VADCK3POL	VADCK2POL	VADCK1POL	SYSCLK4MD	SYSCLK3MD	SYSCLK2MD	SYSCLK1MD	**F0h**
FC	TESTOSWP	TESTOUT	TESTOUTSEL						**00h**
FD	SACNTN	EXTCK	BOHM	BO7	REVISION				**00h**
FE	DEVICE_ID [15-8]								**28h**
FF	DEVICE_ID [7-0]								***55h***

Data Channel

* Following Index 55-A8, C0-D7 are common for all channels and PAGE register select the channel(s) affected by read/write to this register space when APAGE=0 and MPAGE=0.

Index	7	6	5	4	3	2	1	0	Reset
55	TXDATA1 [47-40]								00h
56	TXDATA1 [39-32]								00h
57	TXDATA1 [31-24]								00h
58	TXDATA1 [23-16]								00h
59	TXDATA1 [15-8]								00h
5A	TXDATA1 [7-0]								00h
5B	TXDATA2 [47-40]								00h
5C	TXDATA2 [39-32]								00h
5D	TXDATA2 [31-24]								00h
5E	TXDATA2 [23-16]								00h
5F	TXDATA2 [15-8]								00h
60	TXDATA2 [7-0]								00h
61									00h
62	TXDATA3 [39-32]								00h
63	TXDATA3 [31-24]								00h
64	TXDATA3 [23-16]								00h
65	TXDATA3 [15-8]								00h
66	TXDATA3 [7-0]								00h
67									00h
68	TXDATA4 [39-32]								00h
69	TXDATA4 [31-24]								00h
6A	TXDATA4 [23-16]								00h
6B	TXDATA4 [15-8]								00h
6C	TXDATA4 [7-0]								00h
6D	CAP_TX								00h
6E	DAT_TX								00h
6F	TXMODE	TXDOE	TX PELCO2	TX PELCO1	TXDAH	TXACP	TXIRQ EN	TXEN	00h
70	TXDPOL	TXIRQ MD	TX 2BYTE	TXMFR	TXLMD	TXLNUM			00h
71	ST1P5	FIFO IRQEN	DRVEN	DCKEX	TXFLD		TXHST [11-10]		00h
72				TXADRPI PE	FFCYC	TXDAHBIT			00h
73			PTZACM ODE	PTZSRC SEL	PTZSTN1				06h
8A	RXDATA1 [47-40]								00h
8B	RXDATA1 [39-32]								00h
8C	RXDATA1 [31-24]								00h
8D	RXDATA1 [23-16]								00h
8E	RXDATA1 [15-8]								00h
8F	RXDATA1 [7-0]								00h
90	RXDATA2 [47-40]								00h
91	RXDATA2 [39-32]								00h
92	RXDATA2 [31-24]								00h
93	RXDATA2 [23-16]								00h

Index	7	6	5	4	3	2	1	0	Reset
94	RXDATA2 [15-8]								00h
95	RXDATA2 [7-0]								00h
96	RXDATA3 [47-40]								00h
97	RXDATA3 [39-32]								00h
98	RXDATA3 [31-24]								00h
99	RXDATA3 [23-16]								00h
9A	RXDATA3 [15-8]								00h
9B	RXDATA3 [7-0]								00h
9C	RXDATA4 [47-40]								00h
9D	RXDATA4 [39-32]								00h
9E	RXDATA4 [31-24]								00h
9F	RXDATA4 [23-16]								00h
A0	RXDATA4 [15-8]								00h
A1	RXDATA4 [7-0]								00h
A2	CAP_RX								00h
A3	DAT_RX								00h
A4	RXL8 DET	RXL7 DET	RXL6 DET	RXL5 DET	RXL4 DET	RXL3 DET	RXL2 DET	RXL1 DET	00h
A7	RX IRQMD2	RX STFALL	RXPWM	RX PELCO	RXDAH	RXACP	RXIRQ EN	RXEN	00h
A8	RXDAHBNUM		RX 2BYTE	RXMFR	RXLMD	RXLNUM			00h
AE		RXL2 CRC3	RXL2 CRC2	RXL2 CRC1		RXL1 CRC3	RXL1 CRC2	RXL1 CRC1	00h
AF		RXL4 CRC3	RXL4 CRC2	RXL4 CRC1		RXL3 CRC3	RXL3 CRC2	RXL3 CRC1	00h
B0		RXL6 CRC3	RXL6 CRC2	RXL6 CRC1		RXL5 CRC3	RXL5 CRC2	RXL5 CRC1	00h
C0	TXLINE2 [11-8]				TXLINE1 [11-8]				00h
C1	TXLINE4 [11-8]				TXLINE3 [11-8]				00h
C2	TXLINE1 [7-0]								0Bh
C3	TXLINE2 [7-0]								0Ch
C4	TXLINE3 [7-0]								00h
C5	TXLINE4 [7-0]								00h
C6		TXBITCKNUM							1Fh
C7	TXHST [7-0]								78h
C8	TXHST [9-8]		TXBITNUM						27h
C9	RXLINE2 [11-8]				RXLINE1 [11-8]				00h
CA	RXLINE4 [11-8]				RXLINE3 [11-8]				00h
CB	RXLINE1 [7-0]								07h
CC	RXLINE2 [7-0]								08h
CD	RXLINE3 [7-0]								00h
CE	RXLINE4 [7-0]								00h
CF		RXFREQ [22-16]							04h
D0	RXFREQ [15-8]								00h
D1	RXFREQ [7-0]								00h
D2	RXTHLEVEL								60h
D3		RXDEMD	RXHINUM						10h

D4		RXADRPIPE	RXHST [9-8]	RXHEND [11-8]	**06h**
D5	RXHST [7-0]				**BE**
D6	RXHEND [7-0]				**39h**
D7			RXBITNUM		**27h**

Audio

* Following Index can be read/write accessible when APAGE=1 and MPAGE=0.

Index	7	6	5	4	3	2	1	0	Reset
00				RPOS0					00h
01				RPOS1					00h
02				RPOS2					00h
03				RPOS3					00h
04				RPOS4					00h
05				RPOS5					00h
06				RPOS6					00h
07				RPOS7					00h
08				RPOS8					00h
09				RPOS9					00h
0A				RPOS10					00h
0B				RPOS11					00h
0C				RPOS12					00h
0D				RPOS13					00h
0E				RPOS14					00h
0F				RPOS15					00h
10				RPOS50					00h
11				RPOS51					00h
12				RPOS52					00h
13				RPOS53					00h
14		ACKI [22-16]							09h
15		ACKI [15-8]							B5h
16		ACKI [7-0]							83h
17	ACAS MAS	ACLK27 POL	ACASO MD	RECSB	R0DLY	REC8BIT	RRISE	RECDSP	00h
18	ADACK POL	AADCK POL	MACK MD	AMD	MFMANU	MFMODE			21h
19	MUTEM	MUTER	RACKSL	ACASEN	RDTMOE	RDTROE	RSYNOE	RACKOE	00h
1A				ADAOUTSEL					00h
1B		PB8BIT	PBSB	PB0DLY	PBRISE	PBDSP	PBLR	PBMAS	00h
1C				ADETTH					08h
1D		AFPOL	AATEST	AFTEST	AFDIS	TADACO	ATHRU	ADCCTL	00h
1E					VBG_SL	ISEL_AD			00h
1F		PWD12_ BACK	PWD12_ DAC	DCK_INV	AOUT_GAIN				08h

Index	7	6	5	4	3	2	1	0	Reset
20	MPOS0								00h
21	MPOS1								00h
22	MPOS2								00h
23	MPOS3								00h
24	MPOS4								00h
25	MPOS5								00h
26	MPOS6								00h
27	MPOS7								00h
28	MPOS8								00h
29	MPOS9								00h
2A	MPOS10								00h
2B	MPOS11								00h
2C	MPOS12								00h
2D	MPOS13								00h
2E	MPOS14								00h
2F	MPOS15								00h
30	MPOS50								00h
31	MPOS51								00h
32	MPOS52								00h
33	MPOS53								00h
34	AIN2MIXRATE				AIN1MIXRATE				55h
35	AIN4MIXRATE				AIN3MIXRATE				55h
36	PBMIXRATE				AUXMIXRATE				55h
37			PBM MUTE	AUXM MUTE	AIN4M MUTE	AIN3M MUTE	AIN2M MUTE	AIN1M MUTE	3Fh
38		ACAS MIXEN	AMIXMD		DAOGAIN				38h
39	GAIN_AIN2				GAIN_AIN1				88h
3A	GAIN_AIN4				GAIN_AIN3				88h
3B					GAIN_AUX				08h
3C			PWD12_ ADC	PWD12_ AUX	PWD12_ AIN4	PWD12_ AIN3	PWD12_ AIN2	PWD12_ AIN1	00h
3D								ARST	00h
3E	AUDIO_TEST								00h
41							AIN1ADJ [9-8]		00h
42	AIN1ADJ [7-0]								00h
43							AIN2ADJ [9-8]		00h
44	AIN2ADJ [7-0]								00h
45							AIN3ADJ [9-8]		00h
46	AIN3ADJ [7-0]								00h
47							AIN4ADJ [9-8]		00h
48	AIN4ADJ [7-0]								00h
49							AUXADJ [9-8]		00h
4A	AUXADJ [7-0]								00h

Index	7	6	5	4	3	2	1	0	Reset
4B							AIN1DC [9-8]		-
4C	AIN1DC [7-0]								-
4D							AIN2DC [9-8]		-
4E	AIN2DC [7-0]								-
4F							AIN3DC [9-8]		-
50	AIN3DC [7-0]								-
51							AIN4DC [9-8]		-
52	AIN4DC [7-0]								-
53							AUXDC [9-8]		-
54	AUXDC [7-0]								-
55							AIN1IN [9-8]		-
56	AIN1IN [7-0]								-
57							AIN2IN [9-8]		-
58	AIN2IN [7-0]								-
59							AIN3IN [9-8]		-
5A	AIN3IN [7-0]								-
5B							AIN4IN [9-8]		-
5C	AIN4IN [7-0]								-
5D							AUXIN [9-8]		-
5E	AUXIN [7-0]								-
5F				AIN1DET					-
60				AIN2DET					-
61				AIN3DET					-
62				AIN4DET					-
63							AIN1AV [9-8]		-
64	AIN1AV [7-0]								-
65							AIN2AV [9-8]		-
66	AIN2AV [7-0]								-
67							AIN3AV [9-8]		-
68	AIN3AV [7-0]								-
69							AIN4AV [9-8]		-
6A	AIN4AV [7-0]								-
6B							AUXAV [9-8]		-
6C	AUXAV [7-0]								-
6D							AIN1ADJDC [9-8]		-
6E	AIN1ADJDC [7-0]								-
6F							AIN2ADJDC [9-8]		-
70	AIN2ADJDC [7-0]								-
71							AIN3ADJDC [9-8]		-
72	AIN3ADJDC [7-0]								-
73							AIN4ADJDC [9-8]		-
74	AIN4ADJDC [7-0]								-
75							AUXADJDC [9-8]		-
76	AUXADJDC [7-0]								-
77			TNUM3		TNUM2		TNUM1		39h
78			RNUM4		RNUM3		RNUM2		-
79		PD12BG	LDO_BG	LDO_PD	ACKDLY	ATEST_SEL			00h
7A	ADC_CTRL								00h
7B					CXSEL [3-0]				00h

MIPI & PLL

* Following Index can be read/write accessible when APAGE=0 and MPAGE=1.

Index	7	6	5	4	3	2	1	0	Reset
00	PWD12 BG	ISEL			VBG SELB	IPSEL			44h
01	CKHS BUF1	CKHS BUF0	CKLPBUF		CKINV SEL	CKPH			F0h
02					CKHINV SER	CKINV SER	PWD12 CK	MIPI CKEN	00h
03		D-PH1				D_PH0			00h
04		D-PH3			SKIP_ FRAME3	D-PH2			00h
06	HSTX3 BUF1	HSTX2 BUF1	HSTX1 BUF1	HSTX0 BUF1	HSTX3 BUF0	HSTX2 BUF0	HSTX1 BUF0	HSTX0 BUF0	FFh
07	LPTXBUF3		LPTXBUF2		LPTXBUF1		LPTXBUF0		FFh
08	PWD_3	PWD_2	PWD_1	PWD_0	MIPIEN3	MIPIEN2	MIPIEN1	MIPIEN0	00h
09	MIPITEST1								00h
0A	MIPITEST2								00h
10	RST_PLL _REG	PWDPLL	VCO_SEL		LOCK_ ENB	LOCK_VREF			20h
11	DEGLITCH_SEL		TEST_SEL			ICP_SEL			03h
12	DIV_PRE_FB		DIV_POST_FB						54h
13	DIV_FIN			BYPASS _27M	DIV_OUT_PRE		DIV_OUT_POST		E7h
14	RST_CL K_GEN	DIV_CSI_CLK			BIT_CLK 2_SEL	DIV_PHY_CLK			33h
15				DIV_CLK_DEC			DIV_BIT_CLK		0ch
18	VC_ID								E4h
19			FORMAT						1Eh
20		NUM_CHANNELS				NUM_LANES			24h
21	TP_ENA	DUAL_ MODE	SKIP_ FRAME2	SKIP_ FRAME1	PSFM	SKIP_ FRAME0	SEND_ LN_END	FRAME_ NUM_EN	03h
22	CSI2_CH_EN				CSI1_CH_EN				0Fh
23							STOP _CLK	ULPM _CLK	00h
24	ULPM				CLKESC				00h
25	T_LPX								04h
26	T_PREP								06h
27	T_TRAIL								03h
28	T_WAKE								18h
29	T_EXIT								02h
2B	CH0_HACTIVE_LN [7-0]								R
2C	CH0_HACTIVE_LN [15-8]								R
2D	CH1_HACTIVE_LN [7-0]								R
2E	CH1_HACTIVE_LN [15-8]								R
2F	CH2_HACTIVE_LN [7-0]								R
30	CH2_HACTIVE_LN [15-8]								R
31	CH3_HACTIVE_LN [7-0]								R
32	CH3_HACTIVE_LN [15-8]								R

33					RST _PHY	RST _CSI	RST _MUX	RST _BTG	**00h**
34	CH4_VCI		CH3_VCI		CH2_VCI		CH1_VCI		**E4h**
35	FE_ADJ		FE_WAIT						**55h**
36	OVERFLOW				UNDERFLOW				**00h**

7.2 Decoder Registers

7.2.1 Reserved Register

Index	7	6	5	4	3	2	1	0	Reset
00									11h

7.2.2 Video Input Status

Index	7	6	5	4	3	2	1	0	Reset
01	VDLOSS	VLOCK	HLOCK	SLOCK	VDET	EQDET	NINTL	CDET	R

7 Video Loss

Sensitivity can be controlled by MISSCNT

0 = Video present

1 = Video loss

6 Vertical PLL Lock

0 = Not lock

1 = Lock

5 Horizontal PLL Lock

0 = Not lock

1 = Lock

4 Carrier PLL Lock

0 = Not lock

1 = Lock

3 Video Detect

0 = No video

1 = Video detected

2 EQ or 50Hz (SD mode) Detect

0 = None

1 = Detected or 50Hz (SD mode)

1 Interlaced Video

0 = Interlaced video

1 = Progressive video

0 CDET

0 = carrier detected

1 = No carrier detected

7.2.3 Decoding Control

Index	7	6	5	4	3	2	1	0	Reset
02	MD1120	GMEN	OPLMT	F444	MD656	SD	P720	ITLC	**C2h**

7 Output mode

0 = 16-bit

1 = 8-bit

6 Y/C order control for 8-bit mode. Not valid for 16-bit mode.

0 = Y first

1 = C first

5 Output limit

0 = 1-254

1 = Limit output range based on standard, i.e. Y=16-235, Cb/Cr=16-240.

4 F444

0 = Even pixel count (Default)

1 = Odd/Even count

3 MD656

0 = BT.1120 format, double-byte header

1 = BT.656 format output, single-byte header

2 SD mode

0 = HD mode

1 = SD mode only

1 P720

0 = 1080p decoding

1 = 720p decoding

0 ITLC

0 = Progressive mode decoding

1 = Interlace mode decoding

7.2.4 Detection Status

Index	7	6	5	4	3	2	1	0	Reset
03	EQGAIN				SYWD	CVSTD			-

This is read only register

7-4 EQGAIN

The current adaptive equalizer gain value

3 SYWD

0 = TVIv1.0

1 = TVIv2.0

2-0 CVSTD

The detected standard of current input video assuming the FSL setting matches the SYSCLK selection.

0 = 720p/60

1 = 720p/50

2 = 1080p/30

3 = 1080p/25

4 = 720p/30

5 = 720p/25

6 = SD

7 = other formats

Note: The standard detection is for reference only. The accuracy may be affected by the current invoked decoding standard. It is recommended to confirm by setting the decoder accordingly.

7.2.5 Internal Status

Index	7	6	5	4	3	2	1	0	Reset
04	Device Internal status								-

7-0 Device Internal Status

The device internal status can be accessed through this register with the control of status control register 0x2F. Read-only register. Reserved for debugging. Set as recommended.

7.2.6 Reserved

Index	7	6	5	4	3	2	1	0	Reset
05	NCY4								00h

7-0 NCY4, Reserved

7.2.7 Reset Control

Index	7	6	5	4	3	2	1	0	Reset
06	SRESET	-	BGW	CKPLVD	ACSY	AGC_EN	AGCGAIN [8]	EQRST	**32h**

7 SRESET

Writing '1' to this bit performs soft reset of the logics but not affecting the register value. The bit is self-resetting after written.

6 Reserved

5 BGW, Burst gate control

4 CKPLVD

0 = Non-inverted

1 = Inverted clock phase

3 ACSY, Reserved

2 AGC_EN

0 = Automatic Gain Control (AGC) function is enabled (Default)

1 = AGC is disabled

1 AGCGAIN [8]

Bit 8 of the 9-bit Programmable Gain Amplifier (PGA) control

0 EQRST

Writing "1" to this bit resets the adaptive EQ to its original state. This bit is self-resetting after written.

7.2.8 EQ2 Control

Index	7	6	5	4	3	2	1	0	Reset
07	BPASS2	EQ_EN	EQGAIN						**40h**

7 BPASS2

1 = Analog EQ2 is used

0 = Factory function

6 EQ_EN

0 = Adaptive EQ2 is disabled

1 = Adaptive EQ2 is enabled (Default)

5-0 EQGAIN

This bits set the EQ2 gain value when the adaptive gain control loop is disabled.

7.2.9 PGA Gain Control

Index	7	6	5	4	3	2	1	0	Reset
06		-	-		-	AGC_EN	AGCGAIN [8]		32h
08	AGCGAIN [7-0]								00h

7-0 AGCGAIN [8-0]

A 9-bit PGA gain control value. It allows manual gain control when AGC function is disabled. The default value is 100h.

7.2.10 EQ2 Reference

Index	7	6	5	4	3	2	1	0	Reset
09	MAXEN	DETEN	EQREF						24h

7 MAXEN

0 Enable EQ limiter function

1 Disable

6 DETEN

0 Enable EQ detection function

1 Disable

5-0 These bits set the Equalizer gain control loop reference threshold. The default is 24h. The control loop refers this value for operation.

7.2.11 EQ2 Hysteresis

Index	7	6	5	4	3	2	1	0	Reset
0A	MAXTH				EQHY				48h

7-4 These bits set the threshold to control the EQ limiter function

3-0 These bits control the EQ adaptive loop decision hysteresis value.

7.2.12 EQ1 Control

Index	7	6	5	4	3	2	1	0	Reset
0B	BPASS1	TL_EN	TFREQ	TLGAIN					40h

7 BPASS1

1 = Analog EQ is used

0 = Internal Test function

6 TL_EN

0 = Adaptive EQ1 is disabled

1 = Adaptive EQ1 is enabled (Default)

5 TFREQ Frequency control

0 = High (Default)

1 = Low

4-0 TLGAIN

This bits set the EQ1 gain value when the adaptive gain control loop is disabled.

7.2.13 EQ1 Hysteresis

Index	7	6	5	4	3	2	1	0	Reset
0C			EQSY	FSEL	TLHY				43h

5 Sync EQ control

0 = Off (Default) 1 = On

4 EQ clock frequency control

0 = 148M 1 = 74M

3-0 These bits control the EQ adaptive loop decision hysteresis value.

7.2.14 Comb Filter and SD Format control

Index	7	6	5	4	3	2	1	0	Reset
0D	FLT	PBW	FS4	COMB	YCMB	SDSTD			50h

7 FLT, Use as recommended.

6 PBW, Comb filter control. Use as recommended in special mode.

5 FS4. It is used with SD=1 and SDSTD to control the comb filter operation.

0 = SD mode only 1 = special HD mode

4 Comb filter control

0 = Off 1 = On (Default)

3 Y control in B/W mode

0 = High 1 = Low

2-0 These bits control the SD/HD decoding format

0 = NTSC-M (720p30)

1 = PAL-B (720p25)

2 = PAL-M (1080p30)

3 = PAL-N (1080p25)

4 = PAL-60

5 = NTSC 4.43

6, 7 = Not supported

7.2.15 Brightness Control

Index	7	6	5	4	3	2	1	0	Reset
10		BRIGHTNESS							00h

7 Reserved

6-0 Brightness

This register controls the Brightness of the video by controlling the black level. It is in 2's complement format with a range of –64 to +63.

7.2.16 Contrast Control

Index	7	6	5	4	3	2	1	0	Reset
11		CONTRAST							40h

7 Reserved

6-0 CONTRAST. It provides up to 6dB of luminance gain control. The default 0 dB gain value is 40h

7.2.17 Saturation Control

Index	7	6	5	4	3	2	1	0	Reset
12		UVGAIN							40h

7 Reserved

6-0 Saturation

It provides up to 6dB of color gain control. The default 0 dB gain value is 40h

7.2.18 Hue Control

Index	7	6	5	4	3	2	1	0	Reset
13	HUE								00h

7-0 Hue

This value is represented in 2's complement value for both positive (reddish) and negative (greenish) color tone control. It provides +- 90 degree of color shift at roughly 2.9 degree per step.

7.2.19 Sharpness Control

Index	7	6	5	4	3	2	1	0	Reset
14	HGM	NMD		SHARPNESS					00h

7 HGM. EQ control. For debugging purpose.

6-5 NMD. Special filter mode control. Use as recommended.

4-0 Sharpness

It provides 31 levels of sharpness control from 0 up to 9 dB gain. The sharpness has a center frequency of about 15MHz.

7.2.20 Y/C delay Control

Index	7	6	5	4	3	2	1	0	Reset
15		HDELAY [10-8]			AO	YDLY			13h

7 Reserved

6-4 H delay [10-8]

3 AO, Reserved

2-0 YDLY

These bits adjust the luminance data delay relative to the chrominance data for Y/C alignment. Larger value represents larger delay.

7.2.21 Output H-delay Control

Index	7	6	5	4	3	2	1	0	Reset
15		HDELAY [10-8]							13h
16	HDELAY [7-0]								15h

H Delay [10-0]

It sets the distance from the internal sync reference point to the start of the active video output. This 11-bit value is in 2's complement format to have a control –1024 to +1023 pixels.

7.2.22 Output H Active Control

Index	7	6	5	4	3	2	1	0	Reset
1A					HACTIVE [11-8]				25h
17	HACTIVE [7-0]								00h

H Active [11-0]

It sets the horizontal output length in number of output pixels. The active length for different standards is as follow.

720p = 1280d or 500h

1080p = 1920d or 780h

7.2.23 Output Vertical Delay

Index	7	6	5	4	3	2	1	0	Reset
18	VDELAY [7-0]								19h

7-0 The Vertical Delay register controls the starting line of the display output from the vertical sync.

7.2.24 Output Vertical Active Control

Index	7	6	5	4	3	2	1	0	Reset
1A		VACTIVE [11-8]							25h
19	VACTIVE [7-0]								D0h

V Active [11-0]

This is the 12-bit register that defines the number of active output lines per frame. The standard values are

720p – 720d or 2D0h

1080p – 1080d or 438h

7.2.25 Read Selection Control

Index	7	6	5	4	3	2	1	0	Reset
1B			RDSEL		-				00h

Reserved

7.2.26 NPXL

Index	7	6	5	4	3	2	1	0	Reset
1C	YCM			NPXL [12-8]					06h
1D	NPXL [7-0]								72h

NPXL, Number of Pixels per line[12-0]

This register needs to be set correctly for each decoding standard as following table.

Npxl	720p60/50	720p30/25	1080p30/25	QHD30/25	5M20	8M15	480i	576i
Decimal	1650 / 1980	3300* / 1650** 3960* / 1980**	2200 / 2640	3300 / 3960	3750	4400	4720* / 2360**	4752* / 2376**
Hex	672 / 7BC	CE4* / 672** F78* / 7BC**	898 / A50	CE4 / F78	EA6	1130	1270* / 938**	1290* / 948**

* V1 148.5MHz **74.25MHz

7 YCM, reserved for special mode. Used with FS4.

7.2.27 Readout H Position Control

Index	7	6	5	4	3	2	1	0	Reset
1E	HPXL								80h

Reserved

7.2.28 Readout V Position Control

Index	7	6	5	4	3	2	1	0	Reset
1F	VLNN								80h

Reserved

7.2.29 Clamp Position Control

Index	7	6	5	4	3	2	1	0	Reset
20	PCLAMP								30h

7-0 It controls the clamping position in number pixels relative to the internal sync reference. Factory recommended value should be used.

7.2.30 Clamping Gain Control

Index	7	6	5	4	3	2	1	0	Reset
21	WPGN				CLPGN				86h

7-4 White Peak Gain

It controls the white peak function loop speed. Use factory recommended value.

3-0 Clamp Gain

It controls the clamping loop gain and speed. Use factory recommended value.

7.2.31 Sync Amplitude AGC Control

Index	7	6	5	4	3	2	1	0	Reset
22	SYHT								38h

7-0 Sync Amplitude

It is used as the target sync amplitude value for AGC control. Default 38h should be used.

7.2.32 Clamping Level Control

Index	7	6	5	4	3	2	1	0	Reset
23	CLMP								3Ch

7-0 Clamping Level

It is used as the target clamping level for clamping control loop. Default of 3Ch should be used.

7.2.33 AGC Loop Gain Control

Index	7	6	5	4	3	2	1	0	Reset
24	-	FR	FMT		NMGN				04h

7 Reserved

6 FR (Reserved)

5-4 FMT (Reserved)

3-0 AGC loop gain

It controls the AGC loop gain and speed. Use default unless noted otherwise.

7.2.34 Peak White Control

Index	7	6	5	4	3	2	1	0	Reset
25	PKWT								FFh

7-0 Peak White Level

It sets the peak white detection level. The function can be disabled by setting value of FFh.

7.2.35 Clamping Control

Index	7	6	5	4	3	2	1	0	Reset
26	CLEN	CKLY	GTST	SFLT	CBW		PSP	CLMD	**05h**

7 Clamp Enable

0 = Enable (Default)

1 = Disable

6 Clamp Current Control

0 = 1X

1 = 2X

5 GTST

Reserved for debugging use. Default should be used.

4 SFLT, Sync filter bandwidth selection

0 = High (Default)

1 = Low.

3-2 CBW

Color bandwidth control for SD decoding. Use as recommended.

1 PSP (Reserved)

0 Clamping control

1 = Normal mode 0 = Detection mode.

7.2.36 Reserved

Index	7	6	5	4	3	2	1	0	Reset
27	MP	UE	UG						**2Dh**

7-0 Reserved

7.2.37 Vertical Synchronization Control

Index	7	6	5	4	3	2	1	0	Reset
28	VLCKOUT		VLCKIN		VMODE	DETV	AFLD	VINT	00h

7-6 Vertical lock out count

Number of losing lock frames before the vertical PLL is locked out.

5-4 Vertical lock in count

Number of in-sync frames before the vertical PLL is locked in.

3 Vertical Synchronization mode

0 = Count down mode (Default)

1 = Continue search mode

2 DETV

0 = PLL is used to vertical synchronization (Default)

1 = Special synchronization mode not for normal use.

1 Reserved

0 Vertical Sync detection pulse width

0 = normal (Default)

1 = long (for SD input use)

7.2.38 Video Detection Control

Index	7	6	5	4	3	2	1	0	Reset
29	LOSSCNT				HSWIN				48h

7-4 Video Loss Count

These bits control the video loss detection sensitivity. Larger value has longer detection time.

3-0 HSWIN

Reserved

7.2.39 Color, H PLL and Free Run Control

Index	7	6	5	4	3	2	1	0	Reset
2A	CKLM	CFQ			FCS	LCS	HPM		30h

7 Color Killer Control

0 = Color killer enabled (Default)

1 = Color killer disabled

6-4 Color PLL lock detection threshold. Reserved for debugging. Use as recommended.

3 Force free run mode

0 = Disabled

1 = Forced free-run

2 Free run mode color control

0 = Normal input video data

1 = Blue screen

1-0 Horizontal PLL Control

0,1 = Normal operating mode (Default)

2,3h = special operating mode

7.2.40 Color Killer Threshold Control

Index	7	6	5	4	3	2	1	0	Reset
2B	CKILLHY		CGAINMAX						4Ah

7-6 Color Killer Hysteresis

Larger value represents larger hysteresis

5-0 Color Killer Threshold

It is implemented as color loop gain control. Larger value represents smaller color killer level. The default setting is for HD mode with EQ. It is recommended to set 70h for SD modes.

7.2.41 Color PLL Control

Index	7	6	5	4	3	2	1	0	Reset
2C	FQEN	CHLOK	SPR		ACCT		SPM		0Ah

7 Color Carrier Frequency Detection

0 = Disabled

1 = Enabled

*Should be 0 for best result.

6 Color PLL reset while H is not locked

0 = Disabled

1 = Enabled

5-4 Color PLL Pull-in Range Control (Follow factory recommendation)

0 = small (Default)

1 = Normal

2 = medium

3 = Wide

3-2 Color Gain Loop Speed Control

0 = Fixed gain

1 = slow

2 = medium (Default)

3 = fast

1-0 Color PLL Bandwidth

0 = Small

1 = Medium

2 = Normal

3 = Fast

7.2.42 Color Burst Gate Control

Index	7	6	5	4	3	2	1	0	Reset
2D	PGATE								30h

7-0 Color Burst Gate Position

These bits control the color burst gate position relative to the internal horizontal sync position. Use as recommended.

7.2.43 Color Gain Reference

Index	7	6	5	4	3	2	1	0	Reset
2E	CGAINTH								70h

7-0 Color Gain Loop Reference

These bits define the color gain control loop reference value. Use as recommended.

7.2.44 Test

Index	7	6	5	4	3	2	1	0	Reset
2F	TEST								00h

7-0 Reserved for debug use

7.2.45 Color Carrier DDS Control

Index	7	6	5	4	3	2	1	0	Reset
30	BFSTD [27-20]								48h
31	BFSTD [19-12]								BAh
32	BFSTD [11-4]								2Eh
33	BFSTD [3-0]				HS	HPRNG	FGAP		90h

27-0 BFSTD. Set as recommended.

3 HS Horizontal PLL control for special operation. Set as recommended.

2-1 HPRNG Horizontal PLL control. Use as recommended.

0 FGAP These bits control the output for non-orthogonal sampling mode. Use as recommended. 0 is for normal mode.

7.2.46 CHID Control

Index	7	6	5	4	3	2	1	0	Reset
34				CIDEN	CHID				00h

7-5 Reserved Function.

4 CIDEN

1 = Enable 0 = Disable

3-0 CHID

Select one of 16 possible CHID

7.2.47 MISC Control

Index	7	6	5	4	3	2	1	0	Reset
35	A135	DS2	FSL						**05h**

7 A135 – Averaging. Reserved

6 DS2, special output mode

1 = Enable 0 = Disable

5 FSL

1 = status readouts reflect 74.25MHz system clock 0 = status reflects 148.5MHz system clock

4-0 Set as recommended.

7.2.48 AFE Control

Index	7	6	5	4	3	2	1	0	Reset
38	CL_ISET	AFE_ISET			DIF_EN	DIFCM		IB_ISET	**40h**

7 CL_ISET, reserved.

6-4 AFE ISET, AFE current control

000 = 20uA (low power default)

001 = 22.5uA

010 = 25.0uA

011 = 27.5uA

100 = 30uA (default)

101 = 32.5uA

110 = 35.0uA

111 = 37.5uA

3 DIF_EN

0 = Single-end mode (Default)

1 = Differential mode

2-1 DIFCM, Common mode control for differential mode.

00, 01 = Disabled

10 = Enabled

11 = Enabled with double clamping strength

0 IB_ISET

0 = BG bias mode

1 = VDD bias mode

7.2.49 AFE LPF Control

Index	7	6	5	4	3	2	1	0	Reset
39	LPF_VM	LPF_S2	EQ_SEL		LPF_SEL		VCOM_SEL		0Eh

7 LPF_VM. It controls the LPF common mode. Use as recommended.

6 LPF_S2. It is the bit 2 of LPF_SEL [2-0].

5-4 EQ_SEL. These are for special EQ mode control.

0 = normal EQ gain

1, 2, 3 = boosted EQ gain

3-2 LPF_SEL

000 = Bypass 001 = 10MHz 010 = 25MHz 011 = 50MHz

100 = 60MHz 101 = 62MHz 110 = 65MHz 111 = 70MHz

1-0 VCOM_SEL. LPF output common mode selection

00 = 10% lower

01 = 5% lower

10 = normal operation

11 = 5% higher

7.2.50 AFE EQ Control

Index	7	6	5	4	3	2	1	0	Reset
3A	EQ1BP	EQ1FQ			EQ2BP	EQ2FQ			32h

7 EQ1 Bypass Control

1 = Bypass 0 = Enabled

6-4 EQ1 Response Control

000 = lowest corner frequency

…

111 = highest corner frequency

3 EQ2 Bypass Control

1 = Bypass 0 = Enabled

2-0 EQ2 Response Control

000 = lowest corner frequency

…

111 = highest corner frequency with 6dB additional mid gain.

7.2.51 AFE ADC Control

Index	7	6	5	4	3	2	1	0	Reset
3B	ADC_CTL								25h

7-0 ADC control (Reserved)

7 Bandgap referenced biasing

0 = bandgap referenced 1= Vdd referenced biasing

6-4 ADC bias current selection

000 = 30uA 001 = 35uA 010 = 40uA 011 = 45uA

100 = 50uA 101 = 55uA 110 = 60uA 111 = 65uA

3 ADC bias selection

0 = Normal operation 1= Reserved

2-0 ADC full-scale reference voltage selection. Use 101 as the default

000 = 0.75V 001 = 0.80V 010 = 0.85V 011 = 0.90V

100 = 0.95V 101 = 1.00V 110 =1.05V 111 = 1.10V

7.2.52 AFE Power Down Control

Index	7	6	5	4	3	2	1	0	Reset
3D	ADC_PD	T_PD_B	PD_CLP		PD_BUF	PD_LPF	PD_EQ	PDA	60h

7 ADC Power Down

0 = Normal operation (Default)

1 = Power down

6 Test buffer PD

Reserved

5-4 Clamp Power Down

0 = Normal operation

1 = PD

2 = N/A

3 Buffer Power Down

Reserved

2 TEST mux polarity selection

Reserved

1 EQ Power Down

Reserved

0 Video AFE Power Down

0 = Normal operation (Default)

1 = PD

7.2.53 AFE Test Control

Index	7	6	5	4	3	2	1	0	Reset
3E	AFE_CTL				T_AFE			TO_EN	00h

7-4 AFE_CTL

3-1 Test AFE

0 = Normal operation (Default)

Other = Test

0 Test Output Enable

0 = Enable (Default)

1 = Disable

7.2.54 Coaxial Audio ControlI

Index	7	6	5	4	3	2	1	0	Reset
80	ASMD	ADDI					AUDSS	AUDMD	50h

6-4 ADDI, Audio loop control. Use as recommended.

1 AUDSS, Use as recommended

0 AUDMD, 0 = Default mode. 1 = Special mode

7.2.55 Coaxial Audio ControlII

Index	7	6	5	4	3	2	1	0	Reset
81	CADET			AGAP					10h

7 CADET, Reserved, Read only.

4-0 AGAP, Use recommended setting

7.2.56 Coaxial Audio Starting Line

Index	7	6	5	4	3	2	1	0	Reset
82	AUDSTRT								18h

7-0 AUDSTRT, Audio decoding starting line control

7.2.57 Coaxial Audio Position

Index	7	6	5	4	3	2	1	0	Reset
83	AUDPOS								18h

7-0 AUDPOS, Audio position relative to the sync

7.2.58 Coaxial Audio Length

Index	7	6	5	4	3	2	1	0	Reset
84	AUDLEN								15h

7-0 AUDLEN, Audio sample width control

7.2.59 Coaxial Audio ADDS

Index	7	6	5	4	3	2	1	0	Reset
85	ADDS [23-16]								07h
86	ADDS [15-8]								0Fh
87	ADDS [7-0]								A5h

23-0 ADDS [23-0], Reserved for debugging purpose.

7.2.60 Coaxial Audio Detection Threshold

Index	7	6	5	4	3	2	1	0	Reset
88	AUDTH								58h

7-0 AUDTH, audio detection threshold control

7.3 General Control Registers

7.3.1 Page Register

Index	7	6	5	4	3	2	1	0	Reset
40		APAGE			MPAGE	ALLWE	PAGE		00h

7 Reserved

6 APAGE

0 = disable audio register access

1 = enable audio register access

5,4 Reserved

3 MPAGE

0 = disable MIPI register access

1 = enable MIPI register access

2 ALLWE

1-0 PAGE

ALLWE and PAGE make Register address 0x00 to 0x3F access control as bellow table when APAGE=0. If ALLWE=1, register write to index 0x00~0x3F affects all channels.

ALLWE	PAGE	Write Register	Read Register
0	0	VIN1 Video	VIN1 Video
0	1	VIN2 Video	VIN2 Video
0	2	VIN3 Video	VIN3 Video
0	3	VIN4 Video	VIN4 Video
1	0	All VIN1-4 Video	VIN1 Video
1	1	All VIN1-4 Video	VIN2 Video
1	2	All VIN1-4 Video	VIN3 Video
1	3	All VIN1-4 Video	VIN4 Video

When APAGE=0 and ALLWE=0,PAGE select data register 0x55-0xA8,0xC0-0xD7.

PAGE=0 VIN1 data register select

PAGE=1 VIN2 data register select

PAGE=2 VIN3 data register select

PAGE=3 VIN4 data register select

7.3.2 AFE Test Register

Index	7	6	5	4	3	2	1	0	Reset
41	PTZ_TEST	TADC_SEL			RSV41-3	TAFE34	TAFE12	PDTAFE	**01h**

7 PTZ_TEST

0 = normal operation

1 = TXD1/2/3/4 input is used to Video AFE P_PTZ_OUTA/B/C/D input. Test purpose only.

6-5 TADC_SEL

000 = default 1xx = reserved

3 Reserved

2-1 TAFE34, TAFE12

0 = Ch1 selected

1 = Ch2 selected

2 = Ch3 selected

3 = Ch4 selected

0 PDTAFE, test ports power down control

0 = Test mode 1 = Normal operation

7.3.3 PLL Selection Control 1 Register

Index	7	6	5	4	3	2	1	0	Reset
42	CLKSELVD2		CLKSELVD1		CLKSELPHY		CLKSELCSI		00h

7-6 CLKSELVD2

00 = VD Port 2 VD MUX clock uses PLL1 CLK_DEC2X

01 = VD Port 2 VD MUX clock uses PLL2 CLK_DEC2X

10 = VD Port 2 VD MUX clock uses PLL1 CLK_DEC

11 = VD Port 2 VD MUX clock uses PLL2 CLK_DEC

5-4 CLKSELVD1

00 = VD Port 1 VD MUX clock uses PLL1 CLK_DEC2X

01 = VD Port 1 VD MUX clock uses PLL2 CLK_DEC2X

10 = VD Port 1 VD MUX clock uses PLL1 CLK_DEC

11 = VD Port 1 VD MUX clock uses PLL2 CLK_DEC

3-2 CLKSELPHY

00 = MIPI Port 1 PHY clock uses PLL1, MIPI Port 2 PHY clock uses PLL1

01 = MIPI Port 1 PHY clock uses PLL2, MIPI Port 2 PHY clock uses PLL1

10 = MIPI Port 1 PHY clock uses PLL1, MIPI Port 2 PHY clock uses PLL2

11 = MIPI Port 1 PHY clock uses PLL2, MIPI Port 2 PHY clock uses PLL2

1-0 CLKSELCSI

00 = MIPI Port 1 CSI clock uses PLL1, MIPI Port 2 CSI clock uses PLL1

01 = MIPI Port 1 CSI clock uses PLL2, MIPI Port 2 CSI clock uses PLL1

10 = MIPI Port 1 CSI clock uses PLL1, MIPI Port 2 CSI clock uses PLL2

11 = MIPI Port 1 CSI clock uses PLL2, MIPI Port 2 CSI clock uses PLL2

7.3.4 PLL Selection Control 2 Register

Index	7	6	5	4	3	2	1	0	Reset
43	CLKSELSYS2				CLKSELSYS1				00h

7-4 CLKSELSYS2

HD decoder channel 2 clock selection

[3] : 0 = regular mode 1: 4-phase mode

[2:1] 00 = phase 0 01: phase 1 10: phase 2 11: phase 3

[0] 0 = PLL1 1 = PLL2

3-0 CLKSELSYS1

HD decoder channel 1 clock selection

[3] : 0 = regular mode 1: 4-phase mode

[2:1] 00 = phase 0 01: phase 1 10: phase 2 11: phase 3

[0] 0 = PLL1 1 = PLL2POST_DIV2

7.3.5 PLL Selection Control 3 Register

Index	7	6	5	4	3	2	1	0	Reset
44	CLKSELSYS4				CLKSELSYS3				00h

7-4 CLKSELSYS4

HD decoder channel 4 clock selection

[3] : 0 = regular mode 1: 4-phase mode

[2:1] 00 = phase 0 01: phase 1 10: phase 2 11: phase 3

[0] 0 = PLL1 1 = PLL2

3-0 CLKSELSYS3

HD decoder channel 3 clock selection

[3] : 0 = regular mode 1: 4-phase mode

[2:1] 00 = phase 0 01: phase 1 10: phase 2 11: phase 3

[0] 0 = PLL1 1 = PLL2POST_DIV2

7.3.6 PLL Digital Control 4 Register

Index	7	6	5	4	3	2	1	0	Reset
45			CLKSELAUG	CLKSELIRQ	PDPORTCLK		VDCKEXTSYNCSEL	PD_PTZ	09h

5 CLKSELAUG, Select AUGFF module operating clock

0: PLL1 1: PLL2

4 CLKSELIRQ, Select IRQ module operating clock

0: PLL1 1: PLL2

3-2 PDPORTCLK

[0] 1: Power down MIPI/DVI port 1 clock 0: Power on MIPI/DVI port 1 clock

[1] 1: Power down MIPI/DVI port 2 clock 0: Power on MIPI/DVI port 2 clock

The PLL output clock frequency can be obtained with following equation.

1 VDCKEXTSYNCSEL, Select external SYNC signal pipeline clock

0: PLL1 VDCK 1: PLL2 VDCK

0 PD_PTZ, Power down PTZ logic

7.3.7 IRQ Length Register

Index	7	6	5	4	3	2	1	0	Reset
B3	IRQLEN								FAh

7-0 IRQLEN

When IRQEDGE=1, self-reset edge interrupt mode is used. This register determines the length of IRQ pin active period. IRQ pin output (IRQLEN+1) 74.25MHz/4 clock period active signal. If IRQLEN=00h, self-reset edge interrupt mode is disabled.

7.3.8 Audio IRQ Status Register

Index	7	6	5	4	3	2	1	0	Reset
B4				AUXIRQ	AIN4IRQ	AIN3IRQ	AIN2IRQ	AIN1IRQ	00h

All bits are reset to 0 after this index B4 register data are read when IRQCLRMD=1.These bits are read only when IRQCLRMD=1.

Each bit is reset to 0 after bit value 1 is written into each bit when IRQCLRMD=0.

When more than one bit of Index B4-B6 register are 1,IRQ pin output active state.

7-5 Reserved

4 AUXIRQ

0 = AUX status changed interrupt is not activated.

1 = AUX status changed interrupt is activated.

3 AIN4IRQ

0 = AIN4 status changed interrupt is not activated

1 = AIN4 status changed interrupt is activated

2 AIN3IRQ

0 = AIN3 status changed interrupt is not activated

1 = AIN3 status changed interrupt is activated

1 AIN2IRQ

0 = AIN2 status changed interrupt is not activated

1 = AIN2 status changed interrupt is activated

0 AIN1IRQ

0 = AIN1 status changed interrupt is not activated

1 = AIN1 status changed interrupt is activated

7.3.9 Video IRQ Status Register

Index	7	6	5	4	3	2	1	0	Reset
B5	V4HIRQ	V3HIRQ	V2HIRQ	V1HIRQ	V4IRQ	V3IRQ	V2IRQ	V1IRQ	**00h**

All bits are reset to 0 after this index B5 register data are read when IRQCLRMD=1.These bits are read only when IRQCLRMD=1.

Each bit is reset to 0 after bit value 1 is written into each bit when IRQCLRMD=0.

When more than one bit of Index B4-B6 register are 1,IRQ pin output active state.

7 V4HIRQ

0 = VIN4 HLOCK changed interrupt is not activated.

1 = VIN4 HLOCK changed interrupt is activated.

6 V3HIRQ

0 = VIN3 HLOCK changed interrupt is not activated.

1 = VIN3 HLOCK changed interrupt is activated.

5 V2HIRQ

0 = VIN4 HLOCK changed interrupt is not activated.

1 = VIN2 HLOCK changed interrupt is activated.

4 V1HIRQ

0 = VIN1 HLOCK changed interrupt is not activated.

1 = VIN1 HLOCK changed interrupt is activated.

3 V4IRQ

0 = VIN4 video lost/detect interrupt is not activated

1 = VIN4 video lost/detect interrupt is activated

2 V3IRQ

0 = VIN3 video lost/detect interrupt is not activated

1 = VIN3 video lost/detect interrupt is activated

1 V2IRQ

0 = VIN2 video lost/detect interrupt is not activated

1 = VIN2 video lost/detect interrupt is activated

0 V1IRQ

0 = VIN1 video lost/detect interrupt is not activated

1 = VIN1 video lost/detect interrupt is activated

7.3.10 Data IRQ Status Register

Index	7	6	5	4	3	2	1	0	Reset
B6	V4RXIRQ	V3RXIRQ	V2RXIRQ	V1RXIRQ	V4TXIRQ	V3TXIRQ	V2TXIRQ	V1TXIRQ	**00h**

All bits are reset to 0 after this index B6 register data are read when IRQCLRMD=1.These bits are read only when IRQCLRMD=1.

Each bit is reset to 0 after bit value 1 is written into each bit when IRQCLRMD=0.

When more than one bit of Index B4-B6 register are 1,IRQ pin output active state.

7 V4RXIRQ

0 = VIN4 RX receive data interrupt is not activated

1 = VIN4 RX receive data interrupt is activated

6 V3RXIRQ

0 = VIN3 RX receive data interrupt is not activated

1 = VIN3 RX receive data interrupt is activated

5 V2RXIRQ

0 = VIN2 RX receive data interrupt is not activated

1 = VIN2 RX receive data interrupt is activated

4 V1RXIRQ

0 = VIN1 RX receive data interrupt is not activated

1 = VIN1 RX receive data interrupt is activated

3 V4TXIRQ

0 = VIN4 TX transmit data interrupt is not activated

1 = VIN4 TX transmit data interrupt is activated

2 V3TXIRQ

0 = VIN3 TX transmit data interrupt is not activated

1 = VIN3 TX transmit data interrupt is activated

1 V2TXIRQ

0 = VIN2 TX transmit data interrupt is not activated

1 = VIN2 TX transmit data interrupt is activated

0 V1TXIRQ

0 = VIN1 TX transmit data interrupt is not activated

1 = VIN1 TX transmit data interrupt is activated

7.3.11 Video Lost-Detect IRQ ControlRegister

Index	7	6	5	4	3	2	1	0	Reset
B8	V4IRQMD		V3IRQMD		V2IRQMD		V1IRQMD		00h

7-6 V4IRQMD

0h = VIN4 Video Lost-Detect interrupt disabled

1h = the interrupt is generated when VIN4 input video status changes from detected to lost.

2h = the interrupt is generated when VIN4 input video status changes from lost to detected.

3h = the interrupt is generated when VIN4 input video status is changed.

5-4 V3IRQMD

0h = VIN3 Video Lost-Detect interrupt disabled

1h = the interrupt is generated when VIN3 input video status changes from detected to lost.

2h = the interrupt is generated when VIN3 input video status changes from lost to detected.

3h = the interrupt is generated when VIN3 input video status is changed.

3-2 V2IRQMD

0h = VIN2 Video Lost-Detect interrupt disabled

1h = the interrupt is generated when VIN2 input video status changes from detected to lost.

2h = the interrupt is generated when VIN2 input video status changes from lost to detected.

3h = the interrupt is generated when VIN2 input video status is changed.

1-0 V1IRQMD

0h = VIN1 Video Lost-Detect interrupt disabled

1h = the interrupt is generated when VIN1 input video status changes from detected to lost.

2h = the interrupt is generated when VIN1 input video status changes from lost to detected.

3h = the interrupt is generated when VIN1 input video status is changed.

7.3.12 HLOCK IRQ Enable ControlRegister

Index	7	6	5	4	3	2	1	0	Reset
B9					HL4IRQ EN	HL3IRQ EN	HL2IRQ EN	HL1IRQ EN	00h

7-4 Reserved

3 HL4IRQEN

0 = Disable VIN4 HLOCK status changed interrupt

1 = Enable VIN4 HLOCK status changed interrupt

2 HL3IRQEN

0 = Disable VIN3 HLOCK status changed interrupt

1 = Enable VIN3 HLOCK status changed interrupt

1 HL2IRQEN

0 = Disable VIN2 HLOCK status changed interrupt

1 = Enable VIN2 HLOCK status changed interrupt

0 HL1IRQEN

0 = Disable VIN1 HLOCK status changed interrupt

1 = Enable VIN1 HLOCK status changed interrupt

7.3.13 AUX IRQ Mode Register

Index	7	6	5	4	3	2	1	0	Reset
BA			AUXIRQMD						00h

7-6 Reserved

5-4 AUXIRQMD

0h = AUX Lost-Detect interrupt disabled

1h = the interrupt is generated when AUX input status changes from detected to lost.

2h = the interrupt is generated when AUX input status changes from lost to detected.

3h = the interrupt is generated when AUX input status is changed.

3-0 Reserved

7.3.14 Audio IRQ Mode Register

Index	7	6	5	4	3	2	1	0	Reset
BB	AIN4IRQMD		AIN3IRQMD		AIN2IRQMD		AIN1IRQMD		00h

7-6 AIN4IRQMD

0h = AIN4 Lost-Detect interrupt disabled

1h = the interrupt is generated when AIN4 input status changes from detected to lost.

2h = the interrupt is generated when AIN4 input status changes from lost to detected.

3h = the interrupt is generated when AIN4 input status is changed.

5-4 AIN3IRQMD

0h = AIN3 Lost-Detect interrupt disabled

1h = the interrupt is generated when AIN3 input status changes from detected to lost.

2h = the interrupt is generated when AIN3 input status changes from lost to detected.

3h = the interrupt is generated when AIN3 input status is changed.

3-2 AIN2IRQMD

0h = AIN2 Lost-Detect interrupt disabled

1h = the interrupt is generated when AIN2 input status changes from detected to lost.

2h = the interrupt is generated when AIN2 input status changes from lost to detected.

3h = the interrupt is generated when AIN2 input status is changed.

1-0 AIN1IRQMD

0h = AIN1 Lost-Detect interrupt disabled

1h = the interrupt is generated when AIN1 input status changes from detected to lost.

2h = the interrupt is generated when AIN1 input status changes from lost to detected.

3h = the interrupt is generated when AIN1 input status is changed.

7.3.15 IRQ Control Register

Index	7	6	5	4	3	2	1	0	Reset
BE	IRQCLR MD		IRQ EDGE	IRQPOL	TESTIRQ	MBIST	TESTMODE		**00h**

7 IRQCLRMD

0 = Index B4/B5/B6 each IRQ bit is reset to 0 when bit value 1 is written in each bit.

1 = Index B4/B5/B6 data are reset to 00h when Index B4/B5/B6 data are read.

6 Reserved

5 IRQEDGE

0 = active state output and software IRQ clear mode.

When any IRQ status bit in index B4, B5 and B6 status register is set to 1, the IRQ pin continues output active status until all bits in B4, B5 and B6 registers are read (cleared).

1 = self reset edge interrupt mode.

When more than one bit in Index B4 Audio IRQ Status Register bit4-0 and Index B5 Video IRQ Status Register bit7-0 and Index B6 Data IRQ Status Register are set to 1, IRQ pin output active status for a period of time determined by the Index B3 IRQ Length register.

4 IRQPOL

0 = Low active interrupt output on IRQ pin (Default)

1 = High active interrupt output on IRQ pin

3 TESTIRQ

0 = IRQ pin is normal operation

1 = IRQ pin output test signal TESTOUTSEL select when TESTIRQ=1. Test purpose only

TESTOUTSEL	IRQ pin
00h	VIN1 VDLOSS
01h	VIN2 VDLOSS
02h	VIN3 VDLOSS
03h	VIN4 VDLOSS
04h	VIN1 HLOCK
05h	VIN2 HLOCK
06h	VIN3 HLOCK
07h	VIN4 HLOCK
08h	VIN1 EQDET
09h	VIN2 EQDET
0Ah	VIN3 EQDET

0Bh	VIN4 EQDET
0Ch	VIN1 VLOCK
0Dh	VIN2 VLOCK
0Eh	VIN3 VLOCK
0Fh	VIN4 VLOCK
1Fh	Audio FSDVLD

2 MBIST

0 = normal operation

1 = Memory BIST test mode. Test purpose only

1-0 TESTMODE

0 = normal operation mode. This value must be selected in normal operation. (Default)

1 =clamp test mode.

Clamp control ports in AFE module have following pin input connection.

DN_CLAMPH_* = VD1_3

DN_CLAMPL_* = VD1_2

UP_CLAMPH_* = VD1_1

UP_CLAMPL_* = VD1_0

2 = digital test mode 1

Following is the 10bit digital test input data assignment.

[VD1_7-0, TXD4, TXD3] pins

3 = digital test mode 2

TP2815: Reserved

7.4 Special Up Channel Control Registers

These registers 0xD8 to 0xDE are effective for one channel at a time depending on the 0x40 [1-0] PAGE setting

7.4.1 Up Channel General Control

Index	7	6	5	4	3	2	1	0	Reset
D8	AUGEN	ATONE		AUGORD	AUGDMD	AUGSB	AUGFMT	AUGMD	00h

7 AUGEN, Up channel control, 1 = Enable

6-5 ATONE, Reserved

4 AUGORD, Bit order control, 0 = Normal 1 = swapped

3 AUGDMD, Transmission mode control, 0 = demand based 1 = full based

2 AUGSB, Start bit control 1 = 1/0 0 = 1

1 AUGFMT, Format control 0 = TVI 1 = Pelco

0 AUGMD, Function control 1 = Normal 0 = Reserved

7.4.2 Up Channel Bit Width

Index	7	6	5	4	3	2	1	0	Reset
D9	AUGWD								68h

7-0 AUGWD, Bit cell width control

7.4.3 Up Channel H Delay

Index	7	6	5	4	3	2	1	0	Reset
DC	AUGHDLY [8]								10h
DA	AUGHDLY [7-0]								C0h

8-0 AUGHDLY, H start delay control

7.4.4 Up Channel H Length

Index	7	6	5	4	3	2	1	0	Reset
DB	AUGSPLN								18h

3-0 AUGSPLN, Bit length control

7.4.5 Dynamic Range

Index	7	6	5	4	3	2	1	0	Reset
DB	AUGDR								18h

7-6 AUGDR, dynamic range selection 00=14b 01=13b 10=12b 11=11b

7.4.6 Up Channel V Delay

Index	7	6	5	4	3	2	1	0	Reset
DC	AUGHDLY [8]	AUGVST							10h

7 AUGHDLY8

6-0 AUGVST [6-0], V start control

7.4.7 Up Channel V Length

Index	7	6	5	4	3	2	1	0	Reset
DD	AUGVLEN								10h

7-0 AUGVLEN, V length control

7.4.8 Up Channel FIFO Status

Index	7	6	5	4	3	2	1	0	Reset
DE	AUGSTUS								-

7-0 AUGSTUS, FIFO entry status

7.4.9 Up Channel FIFO Data

Index	7	6	5	4	3	2	1	0	Reset
DF	AUGDAT								-

7-0 AUGDAT, FIFO Data (Write only)

7.5 Digital Port and Misc Control Registers

7.5.1 Digital Video Port Clock Control

Index	7	6	5	4	3	2	1	0	Reset
F0					OCK148		PLL297		00h

7-4 Reserved

3-2 OCK148

[0] VD port 1 output clock CLK_DEC phase shift selection 1: shift 0: no shift

[1] VD port 2 output clock CLK_DEC phase shift selection 1: shift 0: no shift

1-0 PLL297

[0] VD port 1 MUX clock selection

1: CLK_DEC/CLK_DEC2X divided by 2

0: CLK_DEC/CLK_DEC2X

[1] VD port 2 MUX clock selection

1: CLK_DEC/CLK_DEC2X divided by 2

0: CLK_DEC/CLK_DEC2X

7.5.2 MISC Output Control

Index	7	6	5	4	3	2	1	0	Reset
F1						VD1LMD	SYSLD		00h

7-3 Reserved

2 VD1LMD, Test purpose only.

0 = Normal VD2L output

1 = Test purpose. VD1L -> VD2L.

1 SYSLD, Internal data loading phase for debugging purpose. Use as directed.

0 Reserved

7.5.3 VideoClock Power Down Control

Index	7	6	5	4	3	2	1	0	Reset
F4	VCKRST				SYSCLK 4PD	SYSCLK 3PD	SYSCLK 2PD	SYSCLK 1PD	00h

7 VCKRST

Writing '1' to this bit performs soft reset of video clock timing logics. The bit is self-resetting after written.

6-4 Reserved

3 SYSCLK4PD

0 = VIN4 HDTV Decoder is in normal clock operation.

1 = VIN4 HDTV Decoder is in clock power down mode.

2 SYSCLK3PD

0 = VIN3 HDTV Decoder is in normal clock operation.

1 = VIN3 HDTV Decoder is in clock power down mode.

1 SYSCLK2PD

0 = VIN2 HDTV Decoder is in normal clock operation.

1 = VIN2 HDTV Decoder is in clock power down mode.

0 SYSCLK1PD

0 = VIN1 HDTV Decoder is in normal clock operation.

1 = VIN1 HDTV Decoder is in clock power down mode.

7.5.4 System Clock Control

Index	7	6	5	4	3	2	1	0	Reset
F5	VADCK4 POL	VADCK3 POL	VADCK2 POL	VADCK1 POL	SYSCLK 4MD	SYSCLK 3MD	SYSCLK 2MD	SYSCLK 1MD	**F0h**

7 VADCK4POL

0 = Not inverse VIN4 ADC clock polarity

1 = Inverse VIN4 ADC clock polarity

6 VADCK3POL

0 = Not inverse VIN3 ADC clock polarity

1 = Inverse VIN3 ADC clock polarity

5 VADCK2POL

0 = Not inverse VIN2 ADC clock polarity

1 = Inverse VIN2 ADC clock polarity

4 VADCK1POL

0 = Not inverse VIN1 ADC clock polarity

1 = Inverse VIN1 ADC clock polarity

3 SYSCLK4MD

0 = VIN4 HDTV Decoder system clock is 148.5MHz.

1 = VIN4 HDTV Decoder system clock is 74.25MHz.

2 SYSCLK3MD

0 = VIN3 HDTV Decoder system clock is 148.5MHz.

1 = VIN3 HDTV Decoder system clock is 74.25MHz

1 SYSCLK2MD

0 = VIN2 HDTV Decoder system clock is 148.5MHz.

1 = VIN2 HDTV Decoder system clock is 74.25MHz.

0 SYSCLK1MD

0 = VIN1 HDTV Decoder system clock is 148.5MHz.

1 = VIN1 HDTV Decoder system clock is 74.25MHz.

7.5.5 Test Data Output Selection

Index	7	6	5	4	3	2	1	0	Reset
FC	TESTO SWP	TEST OUT	TESTOUTSEL						**00h**

7 TESTOSWP, Used for test purpose only.

0 = Output test signal {bit[15:8], bit[7:0]} to debug port.

1 = Output test signal {bit[7:0], bit[15:8]} to debug port.

6 TESTOUT

0 = normal operation (Default)

1 = Reserved for test purpose only

5-0 TESTOUTSEL

TEST OUTSEL	Bit15 (MSB) – Bit0 (LSB)
00h	VIN1: ADC9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC
01h	VIN2: ADC9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC
02h	VIN3: ADC9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC
03h	VIN4: ADC9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC
04h	VIN1: VLOCK, HLOCK, SLOCK, VDET, EQDET, NINTL, MONO, GVAL8-0
05h	VIN2: VLOCK, HLOCK, SLOCK, VDET, EQDET, NINTL, MONO, GVAL8-0
06h	VIN3: VLOCK, HLOCK, SLOCK, VDET, EQDET, NINTL, MONO, GVAL8-0
07h	VIN4: VLOCK, HLOCK, SLOCK, VDET, EQDET, NINTL, MONO, GVAL8-0
08h	VIN4RXIRQ, VIN3RXIRQ, VIN2RXIRQ, VIN1RXIRQ, VIN4TXIRQ, VIN3TXIRQ, VIN2TXIRQ, VIN1TXIRQ, VIN4VIRQ, VIN3VIRQ, VIN2VIRQ, VIN1VIRQ, CKOUT_D, CKOUT_C, CKOUT_B, CKOUT_A
09h	VIN4PLLSYNC, VIN4CVSTD2-0, VIN3PLLSYNC, VIN3CVSTD2-0, VIN2PLLSYNC, VIN2CVSTD2-0, VIN1PLLSYNC, VIN1CVSTD2-0
0Ah	VIN1: VDCRO9-2, VD1120HS, VD1120VS, VDLOSS, PLLSYNC, VLOCK, HLOCK, SLOCK, VDET
0Bh	VIN2: VDCRO9-2, VD1120HS, VD1120VS, VDLOSS, PLLSYNC, VLOCK, HLOCK, SLOCK, VDET
0Ch	VIN3: VDCRO9-2, VD1120HS, VD1120VS, VDLOSS, PLLSYNC, VLOCK, HLOCK, SLOCK, VDET
0Dh	VIN4: VDCRO9-2, VD1120HS, VD1120VS, VDLOSS, PLLSYNC, VLOCK, HLOCK, SLOCK, VDET

0Eh	3'b000, RXLD, TXLD, ID_PHASE, VLDCYC, START_STOP, BIT_ACK, SDATO, SDATI, SCLK, RCOUNT
0Fh	ADAC9-0, ADACLK, AMCLKO, FS64, FSDVLD, 2'b00
10h	AIN1_ADC9-0, CALSW, CKK_AUX, CKK_AIN4, CKK_AIN3, CKK_AIN2, CKK_AIN1
11h	AIN2_ ADC9-0, CALSW, CKK_AUX, CKK_AIN4, CKK_AIN3, CKK_AIN2, CKK_AIN1
12h	AIN3_ ADC9-0, CALSW, CKK_AUX, CKK_AIN4, CKK_AIN3, CKK_AIN2, CKK_AIN1
13h	AIN4 _ADC9-0, CALSW, CKK_AUX, CKK_AIN4, CKK_AIN3, CKK_AIN2, CKK_AIN1
14h	AUX_ADC9-0, CALSW, CKK_AUX, CKK_AIN4, CKK_AIN3, CKK_AIN2, CKK_AIN1
15h	AADC1DC9-0, CALSW, AMCLKO, AADCLK, FS64, 2'b00
16h	AADC2DC9-0, CALSW, AMCLKO, AADCLK, FS64, 2'b00
17h	AADC3DC9-0, CALSW, AMCLKO, AADCLK, FS64, 2'b00
18h	AADC4DC9-0, CALSW, AMCLKO, AADCLK, FS64, 2'b00
19h	AUXDC9-0, CALSW, AMCLKO, AADCLK, FS64, 2'b00
1Ah	AADC1DC9-0, AMCLKO, ADET4-0
1Bh	AADC2DC9-0, AMCLKO, ADET4-0
1Ch	AADC3DC9-0, AMCLKO, ADET4-0
1Dh	AADC4DC9-0, AMCLKO, ADET4-0
1Eh	AUXDC9-0, AMCLKO, ADET4-0
1Fh	TESTPCMDATA15-0
20h	VIN1: HEQOUT9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC
21h	VIN2: HEQOUT9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC
22h	VIN3: HEQOUT9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC
23h	VIN4: HEQOUT9-0, CLMPDNX, CLMPUPX, CLMPDN, CLMPUP, VDLOSS, PLLSYNC

7.5.6 Revision

Index	7	6	5	4	3	2	1	0	Reset
FD	SACNTN	EXTCK	BOHM	BO7	REVISION				00h

7 SACNTN

0 = normal SCL/SDA bus mode.(Default)

1 = test SCL/SDA bus mode. Test purpose only.

6 EXTCK

0 = normal 148.5MHz system clock mode with PLL module.(Default)

1 = XTI pin input becomes 148.5MHz system clock source.

5 BOHM

Reserved for future use.

4 BO7

Reserved for future use.

3-0 REVISION.

These bits show the revision number of this chip. These bits are read only.

7.5.7 DEVICE_ID

Index	7	6	5	4	3	2	1	0	Reset
FE	DEVICE_ID [15-8]								28h
FF	DEVICE_ID [7-0] – TP2815								55h

These bits are read only.

7.6 DATA Channel Control Registers

***Following Index 55-A8, C0-D7 Data registers can be read/write accessible when APAGE=0 and ALLWE=0. Every PAGE=0/1/2/3 has these exactly the same registers corresponding to each video channel.**

7.6.1 Video Line 1 Transmit Data

Index	7	6	5	4	3	2	1	0	Reset
55	TXDATA1 [47-40]								00h
56	TXDATA1 [39-32]								00h
57	TXDATA1 [31-24]								00h
58	TXDATA1 [23-16]								00h
59	TXDATA1 [15-8]								00h
5A	TXDATA1 [7-0]								00h

47-0 TXDATA1

These register are effective when TXMFR=0.Sets first TX data line value to be transmitted. The MSB of any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmit mode, TXDATA1 [39]=1 need to be set up if TXDATA1 is transmitted. If all TXDATA1 bits are 0, TXDATA1 transmit is disabled.

7.6.2 Video Line 2 Transmit Data

Index	7	6	5	4	3	2	1	0	Reset
5B	TXDATA2 [47-40]								00h
5C	TXDATA2 [39-32]								00h
5D	TXDATA2 [31-24]								00h
5E	TXDATA2 [23-16]								00h
5F	TXDATA2 [15-8]								00h
60	TXDATA2 [7-0]								00h

47-0 TXDATA2

These register are effective when TXMFR=0.Sets second TX data line value to be transmitted. The MSB of any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmit mode, TXDATA2 [39]=1 need to be set up if TXDATA2 is transmitted. If all TXDATA2 bits are 0, TXDATA2 transmit is disabled.

7.6.3 Video Line 3 Transmit Data

Index	7	6	5	4	3	2	1	0	Reset
62	TXDATA3 [39-32]								00h
63	TXDATA3 [31-24]								00h
64	TXDATA3 [23-16]								00h
65	TXDATA3 [15-8]								00h
66	TXDATA3 [7-0]								00h

39-0 TXDATA3

These registers are effective when TXMFR=0.Sets third TX data line value to be transmitted. The MSB of any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmit mode, TXDATA3 [39]=1 need to be set up if TXDATA3 is transmitted. If all TXDATA3 bits are 0, TXDATA3 transmit is disabled.

7.6.4 Video Line 4 Transmit Data

Index	7	6	5	4	3	2	1	0	Reset
68	TXDATA4 [39-32]								00h
69	TXDATA4 [31-24]								00h
6A	TXDATA4 [23-16]								00h
6B	TXDATA4 [15-8]								00h
6C	TXDATA4 [7-0]								00h

39-0 TXDATA4

These registers are effective when TXMFR=0.Sets fourth TX data line value to be transmitted. The MSB of any TX data value defined by TXBITNUM register must be 1. For example, in default 40bits transmit mode, TXDATA4 [39]=1 need to be set up if TXDATA4 is transmitted. If all TXDATA4 bits are 0, TXDATA4 transmit is disabled.

7.6.5 Transmit Data FIFO Status

Index	7	6	5	4	3	2	1	0	Reset
6D	CAP_TX								00h

7-0 CAP_TX

This register is effective when TXMFR=1.This register shows the number of TX data bytes stored in Transmit Data FIFO. Transmit Data FIFO can have up to 16 data bytes per one time. When software write one data byte in DAT_TX register, the value of CAP_TX is incremented. When TX transmit logic is read first-in first-out data byte in Transmit Data FIFO, the value of CAP_TX is decremented.

7.6.6 Transmit Data FIFO Write

Index	7	6	5	4	3	2	1	0	Reset
6E	DAT_TX								00h

7-0 DAT_TX

This register is effective when TXMFR=1.When software write one data byte in this index register, that one data byte is stored in Transmit Data FIFO by first-in first-out byte order. When software read DAT_TX, the value of this register shows the value of next first-out data byte to be read by TX transmit logic.

7.6.7 TX Format Control

Index	7	6	5	4	3	2	1	0	Reset
6F	TXMODE	TXDOE	TX PELCO2	TX PELCO1	TXDAH	TXACP	TXIRQ EN	TXEN	00h

7 TXMODE

0 = VINn TX data is transferred only once after TXEN=0 at first and TXEN=1 at next

1 = The value of Transmit Data Register is transferred per each frame when TXEN=

6 TXDOE

0 = TXDn pin output tri-state (Default)

1 = TXDn pin output enable

5-2

(1) TXDAH=0 mode with TXMFR=0,TXLMD=0

REGISTERS	TP MODE TECHPOINT TVI GENERAL	PELCO1 MODE PELCO FIRST EXPANSION EXTENDED 15 BIT COAXITRON	PELCO2 MODE PELCO SECOND EXPANSION 32 BIT COAXITRON	ACP MODE HD ACP COAXITRON
TXPELCO2	0	0	1	0
TXPELCO1	0	1	0	0
TXDAH	0	0	0	0
TXACP	0	0	0	1
TXLINE1	Bh	Fh	Fh	11h
TXLINE2	Ch	0h	10h	12h
TXLINE3	Dh for 4 line mode 0h for 2 line mode	0h	0h	13h for 4 line mode 0h for 2 line mode
TXLINE4	Eh for 4 line mode 0h for 2 line mode	0h	0h	14h for 4 line mode 0h for 2 line mode
TXBITCKNUM	1Fh	49h	49h	24h
TXBITNUM	27h	2Ch	2Fh	17h
TXHST	78h for TVI 1.0 DFh for TVI 2.0	214h	214h	215h

TP MODE transmission bit order is MSB at first and bit0 last.

TXDATAn [MSB], TXDATAn [MSB-1]…TXDATAn [1], TXDATAn [0]

In PELCO1, PELCO2 and ACP MODE, one unit data is START, DATA, STOP 3 bit encoding.

START	DATA	STOP
1	TXDATAn[x]	0

TXDATAn [x] is transmitted with START DATA STOP format from TXDATAn LSB bit0 at first.

PELCO1 MODE transmission bit setup and transmission bit order.

Set up TXDATA1 [14:0]

TXDATA1 [0], TXDATA1 [1]…TXDATA1 [13], TXDATA1 [14]

PELCO2 MODE transmission bit setup and transmission bit order.

Set up TXDATA1 [15:0] and TXDATA2 [15:0]

TXDATAn [0], TXDATAn [1]…TXDATAn [14], TXDATAn [1

ACP MODE transmission bit setup and transmission bit order.

Set up TXDATA1 [7:0], TXDATA2 [7:0], TXDATA3 [7:0] and TXDATA4 [7:0]

TXDATAn [0], TXDATAn [1]…TXDATAn [6], TXDATAn [7]

(2) TXDAH=1 mode

REGISTERS	HDCVI MODE
TXPELCO2	0
TXPELCO1	0
TXDAH	1
TXACP	0
TXLMD	1
TXLNUM	5
TXLINE1	10h
TXBITCKNUM	15h
TXBITNUM	17h
TXHST	25Bh

1 TXIRQEN

0 = Disable VINn TX transmit data interrupt

1 = Enable VINn TX transmit data interrupt

0 TXEN

0 = Disable VINn TX data transfer.

1 = Enable VINn TX data transfer.

7.6.8 TX Multi Frame Control

Index	7	6	5	4	3	2	1	0	Reset
70	TXDPOL	TXIRQ MD	TX 2BYTE	TXMFR	TXLMD	TXLNUM			**00h**

7 TXDPOL TXDn signal polarity control

0 = not inverse TXDn signal polarity

1 = inverse TXDn signal polarity

6 TXIRQMD

0 = VINn TX data interrupt is not generated.

1 = VINn TX data interrupt is generated under TXMODE control.

5 TX2BYTE

0 = 1 data byte transfer when TXDAH=1 or TXACP=1

1 = 2 data bytes transfer when TXDAH=1 or TXPELCO1=1 or TXPELCO2=1

4 TXMFR

0 = TX data transfer is non multi frame transfer (Default)

1 = TX data transfer is multi frame transfer with Transmit Data FIFO control by CAP_TX and DAT_TX.

3 TXLMD=0 mode. Independent TX 4 line control

Register TXLINE1, TXLINE2, TXLINE3 and TXLINE4 decide any TX data transfer line.

TXLMD=1 mode. Continuous start line to end line control

2-0 TX start line number is TXLINE1.TX end line number is TXLINE1 + TXLNUM.In this mode,all lines from start line number to end line number are all TX data transfer active line.

7.6.9 TX Field Control

Index	7	6	5	4	3	2	1	0	Reset
71	ST1P5	FIFO IRQEN	DRVEN	DCKEX	TXFLD		TXHST [11-10]		00h

7 ST1P5

0 = start bit is normal 1bit 1

1 = start bit is 1 bit 1 and 0.5bit 0

6 FIFOIRQEN

0 = disable DAT_TX FIFO IRQ

1 = enable DAT_TX FIFO IRQ

5 This bit controls the optional data driver for video AFE channel (Reserved)

0 = disable

1 = enable

4 DCKEX

0 = Data clock enable is controlled by only SYSCLKnMD. This is original mode.

1 = Data clock enable is expanded in SYSCLKnMD=1.This is optional mode.

3-2 VINn TX field control in SD video mode

0,3 = transmit TX data in both field1 (odd) and field2 (even)

1 = transmit TX data in only field1 (odd)

2 = transmit TX data in only field2 (even)

1-0 TXHST [11-10]

TX H start register bit11-10

7.6.10 TXDAHBIT

Index	7	6	5	4	3	2	1	0	Reset
72				TXADRPIPE	FFCYC	TXDAHBIT			00h

4 TXADRPIPE. 1=Add 27MHz pipeline for I2C access to DAHFIFO. 0=Normal Mode

3 FFCYC. 1=FIFO cycling mode.

2-0 TXDAHBIT

Number of bits per line when TXDAH=1 (CVI) mode is enable.

0 = 32bits 1 = 24bits 2 = 21bits 3 = 18bits 4 = 16bits

7.6.11 RX Line 1 Data

Index	7	6	5	4	3	2	1	0	Reset
8A	RXDATA1 [47-40]								00h
8B	RXDATA1 [39-32]								00h
8C	RXDATA1 [31-24]								00h
8D	RXDATA1 [23-16]								00h
8E	RXDATA1 [15-8]								00h
8F	RXDATA1 [7-0]								00h

47-0 RXDATA1

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE1 can be read out from these registers.

7.6.12 RX Line 2 Data

Index	7	6	5	4	3	2	1	0	Reset
90	RXDATA2 [47-40]								00h
91	RXDATA2 [39-32]								00h
92	RXDATA2 [31-24]								00h
93	RXDATA2 [23-16]								00h
94	RXDATA2 [15-8]								00h
95	RXDATA2 [7-0]								00h

47-0 RXDATA2

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE2 can be read out from these registers.

7.6.13 RX Line 3 Data

Index	7	6	5	4	3	2	1	0	Reset
96	RXDATA3 [47-40]								00h
97	RXDATA3 [39-32]								00h
98	RXDATA3 [31-24]								00h
99	RXDATA3 [23-16]								00h
9A	RXDATA3 [15-8]								00h
9B	RXDATA3 [7-0]								00h

47-0 RXDATA3

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE3 can be read out from these registers.

7.6.14 RX Line 4 Data

Index	7	6	5	4	3	2	1	0	Reset
9C	RXDATA4 [47-40]								00h
9D	RXDATA4 [39-32]								00h
9E	RXDATA4 [31-24]								00h
9F	RXDATA4 [23-16]								00h
A0	RXDATA4 [15-8]								00h
A1	RXDATA4 [7-0]								00h

47-0 RXDATA4

These registers are effective when RXMFR=0.RX data received on the vertical line RXLINE4 can be read out from these registers.

7.6.15 RX Data FIFO Status

Index	7	6	5	4	3	2	1	0	Reset
A2	CAP_RX								00h

7-0 CAP_RX

This register is effective when RXMFR=1.This register shows the number of data bytes stored in RX Data FIFO. When RX logic store new received one data byte, this register value is incremented. When software read DAT_RX RX Data FIFO register, this register value is decremented.

7.6.16 RX Data FIFO

Index	7	6	5	4	3	2	1	0	Reset
A3	DAT_RX								00h

7-0 DAT_RX

This register is effective when RXMFR=1.This register shows the value of new RX data byte stored in RX Data FIFO by first-in first-out order after RX logic received new RX data byte.

7.6.17 RXLINE Status

Index	7	6	5	4	3	2	1	0	Reset
A4	RXL8 DET	RXL7 DET	RXL6 DET	RXL5 DET	RXL4 DET	RXL3 DET	RXL2 DET	RXL1 DET	**00h**

These registers are read only. Bit4-7 are effective when RXMFR=1,RXLMD=1 and RXLNUM=7.

7 RXL8DET

0 = Data is not received in 8th RXLINE.

1 = Data is received in 8th RXLINE.

6 RXL7DET

0 = Data is not received in 7th RXLINE.

1 = Data is received in 7th RXLINE.

5 RXL6DET

0 = Data is not received in 6th RXLINE.

1 = Data is received in 6th RXLINE.

4 RXL5DET

0 = Data is not received in 5th RXLINE.

1 = Data is received in 5th RXLINE.

3 RXL4DET

0 = Data is not received in 4th RXLINE.

1 = Data is received in 4th RXLINE.

2 RXL3DET

0 = Data is not received in 3rd RXLINE.

1 = Data is received in 3rd RXLINE.

1 RXL2DET

0 = Data is not received in 2nd RXLINE.

1 = Data is received in 2nd RXLINE.

0 RXL1DET

0 = Data is not received in 1st RXLINE.

1 = Data is received in 1st RXLINE.

7.6.18 RX Format Control

Index	7	6	5	4	3	2	1	0	Reset
A7	RX IRQMD2	RX STFALL	RXPWM	RX PELCO	RXDAH	RXACP	RXIRQ EN	RXEN	**00h**

7 RXIRQMD2

0 = Disable RXIRQMD2

1 = RXIRQ is generated when RX detection counter has more than 1 value.

6 RXSTFALL

0 = RX data bits are received first rising edge

1 = RX data bits are received first falling edge

5 RXPWM

0 = ACKI bit clock received mode

1 = Pulse width modulated data received mode. This bit is effective when RXPELCO=1 or RXACP=1 is selected

4-2

REGISTERS	TP MODE TECHPOINT TVI RX	HDCVI RX MODE	PELCO RX MODE	ACP RX MODE
RXPELCO	0	0	1	0
RXDAH	0	1	0	0
RXACP	0	0	0	1

1 RXIRQEN

0 = Disable VINn RX receive data interrupt

1 = Enable VINn RX receive data interrupt

0 RXEN

0 = Disable VINn RX data receive

1 = Enable VINn RX data receive

7.6.19 RX Multi Frame Control

Index	7	6	5	4	3	2	1	0	Reset
A8	RXDAHBNUM		RX 2BYTE	RXMFR	RXLMD	RXLNUM			00h

7-6 RXDAHBNUM

Number of byte per line when RXDAH=1 (CVI) mode is enable

0 = 1 byte 1 = 2 byte 2 = 3 byte

5 RX2BYTE

0 = 1 data byte receive per line when RXDAH=1 or RXACP=1

1 = 2 data bytes receive per line when RXDAH=1 or RXPELCO=1

4 RXMFR

0 = RX data receive is non multi frame receive(Default)

1 = RX data receive is multi frame receive with Receive Data FIFO control by CAP_RX and DAT_RX.

3 RXLMD=0 mode. Independent RX 4 line control

Register RXLINE1, RXLINE2, RXLINE3 and RXLINE4 decide any RX data receive line.

RXLMD=1 mode. Continuous start line to end line control

2-0 RX start line number is RXLINE1.RX end line number is RXLINE1 + RXLNUM. In this mode, all lines from start line number to end line number are all RX data receive active line.

7.6.20 RX Line1-2 CRC Status

Index	7	6	5	4	3	2	1	0	Reset
AE		RXL2 CRC3	RXL2 CRC2	RXL2 CRC1		RXL1 CRC3	RXL1 CRC2	RXL1 CRC1	00h

These registers are read only. These registers are effective when RXDAH=1.

7 Reserved

6 RXL2CRC3

This bit shows third byte CRC value in 2ND RXLINE

5 RXL2CRC2

This bit shows second byte CRC value in 2ND RXLINE

4 RXL2CRC1

This bit shows first byte CRC value in 2ND RXLINE

3 Reserved

2 RXL1CRC3

This bit shows third byte CRC value in 1ST RXLINE

1 RXL1CRC2

This bit shows second byte CRC value in 1ST RXLINE

0 RXL1CRC1

This bit shows first byte CRC value in 1ST RXLINE

7.6.21 RX Line3-4 CRC Status

Index	7	6	5	4	3	2	1	0	Reset
AF		RXL4 CRC3	RXL4 CRC2	RXL4 CRC1		RXL3 CRC3	RXL3 CRC2	RXL3 CRC1	00h

These registers are read only. These registers are effective when RXDAH=1.

7 Reserved

6 RXL4CRC3

This bit shows third byte CRC value in 4TH RXLINE

5 RXL4CRC2

This bit shows second byte CRC value in 4TH RXLINE

4 RXL4CRC1

This bit shows first byte CRC value in 4TH RXLINE

3 Reserved

2 RXL3CRC3

This bit shows third byte CRC value in 3RD RXLINE

1 RXL3CRC2

This bit shows second byte CRC value in 3RD RXLINE

0 RXL3CRC1

This bit shows first byte CRC value in 3RD RXLINE

7.6.22 RX Line5-6 CRC Status

Index	7	6	5	4	3	2	1	0	Reset
B0		RXL6 CRC3	RXL6 CRC2	RXL6 CRC1		RXL5 CRC3	RXL5 CRC2	RXL5 CRC1	**00h**

These registers are read only. These registers are effective when RXDAH=1.

7 Reserved

6 RXL6CRC3

This bit shows third byte CRC value in 6TH RXLINE

5 RXL6CRC2

This bit shows second byte CRC value in 6TH RXLINE

4 RXL6CRC1

This bit shows first byte CRC value in 6TH RXLINE

3 Reserved

2 RXL5CRC3

This bit shows third byte CRC value in 5TH RXLINE

1 RXL5CRC2

This bit shows second byte CRC value in 5TH RXLINE

0 RXL5CRC1

This bit shows first byte CRC value in 5TH RXLINE

7.6.23 TX Data Line 1 Control

Index	7	6	5	4	3	2	1	0	Reset
C0					TXLINE1 [11-8]				00h
C2	TXLINE1 [7-0]								0Bh

11-0 TXLINE1

Set up first TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.6.24 TX Data Line 2 Control

Index	7	6	5	4	3	2	1	0	Reset
C0	TXLINE2 [11-8]								00h
C3	TXLINE2 [7-0]								0Ch

11-0 TXLINE2

This register is effective when TXLMD=0.Set up second TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.6.25 TX Data Line 3 Control

Index	7	6	5	4	3	2	1	0	Reset
C1					TXLINE3 [11-8]				00h
C4	TXLINE3 [7-0]								00h

11-0 TXLINE3

This register is effective when TXLMD=0.Set up third TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.6.26 TX Data Line 4 Control

Index	7	6	5	4	3	2	1	0	Reset
C1	TXLINE4 [11-8]								00h
C5	TXLINE4 [7-0]								00h

11-0 TXLINE4

This register is effective when TXLMD=0.Set up 4th TX transmitting data line number.

If 000h is set up, this line doesn't execute TX function.

7.6.27 TX Data Bit Clock Number

Index	7	6	5	4	3	2	1	0	Reset
C6		TXBITCKNUM							1Fh

7 Reserved

6-0 TXBITCKNUM

(TXBITCKNUM+1) shows the number of 74.25MHz clocks per one data bit for VINn.

7.6.28 TX Data H Start Control

Index	7	6	5	4	3	2	1	0	Reset
71							TXHST [11-10]		00h
C7	TXHST [7-0]								78h
C8	TXHST [9-8]								27h

11-0 TXHST [11-0]

It controls the VINn TX transmit data horizontal start position.

7.6.29 TX Data Bit Number

Index	7	6	5	4	3	2	1	0	Reset
C8			TXBITNUM						27h

5-0 TXBITNUM

(TXBITNUM+1) shows the number of data bit including first start bit 1 per line for VINn.

7.6.30 RX Data Line 1 Control

Index	7	6	5	4	3	2	1	0	Reset
C9					RXLINE1 [11-8]				00h
CB	RXLINE1 [7-0]								07h

11-0 RXLINE1

Set up vertical line number to receive first line RX data for VINn.

If 000h is set up, this line doesn't execute RX function.

7.6.31 RX Data Line 2 Control

Index	7	6	5	4	3	2	1	0	Reset
C9	RXLINE2 [11-8]								00h
CC	RXLINE2 [7-0]								08h

11-0 RXLINE2

This register is effective when RXLMD=0.Set up vertical line number to receive second line RX data for VINn. If 000h is set up, this line doesn't execute RX function.

7.6.32 RX Data Line 3 Control

Index	7	6	5	4	3	2	1	0	Reset
CA					RXLINE3 [11-8]				00h
CD	RXLINE3 [7-0]								00h

11-0 RXLINE3

This register is effective when RXLMD=0.Set up vertical line number to receive third line RX data for VINn. If 000h is set up, this line doesn't execute RX function.

7.6.33 RX Data Line 4 Control

Index	7	6	5	4	3	2	1	0	Reset
CA	RXLINE4 [11-8]								00h
CE	RXLINE4 [7-0]								00h

11-0 RXLINE4

This register is effective when RXLMD=0.Set up vertical line number to receive 4th line RX data for VINn. If 000h is set up, this line doesn't execute RX function.

7.6.34 RX Bit Frequency

Index	7	6	5	4	3	2	1	0	Reset
CF		RXFREQ [22-16]							04h
D0	RXFREQ [15-8]								00h
D1	RXFREQ [7-0]								00h

22-0 RXFREQ

VINn RX data bit frequency control.

2 ^23 / 32 =23'h040000 (Default)

Default bit frequency for RX receiving data is 74.25MHz/32=2.3203125M

7.6.35 RX Data Threshold

Index	7	6	5	4	3	2	1	0	Reset
D2	RXTHLEVEL								60h

7-0 RXTHLEVEL

Define RX receiving data threshold level for VINn.

7.6.36 RX High Detection Control

Index	7	6	5	4	3	2	1	0	Reset
D3		RXDEMD	RXHINUM						10h

7 Reserved

6 RXDEMD

0 = Once RX data received in RXLINEn line, keep RXLnDET=1 until RXLINEn=000h is written.

1 = Update RX data received status RXLnDET in RXLINEn line in every frame if RXLINEn is not 000h.

5-0 RXHINUM

Sets the data detection threshold for VINn. If the high-level detection per RX received bit is more than RXHINUM, that bit is treated as 1, otherwise, it is treated as 0. Unit 1 number corresponds to one 74.25MHz clock.

7.6.37 RX Horizontal Start

Index	7	6	5	4	3	2	1	0	Reset
D4		RXADRPIPE	RXHST [9-8]						06h
D5	RXHST [7-0]								BEh

6 RXADRPIPE. 1=Add 27MHz pipeline for I2C access to DAHFIFO. 0=Normal Mode

9-0 RXHST

Define the horizontal detection start position of RX receiving data for VINn

7.6.38 RX Horizontal End

Index	7	6	5	4	3	2	1	0	Reset
D4					RXHEND [11-8]				06h
D6	RXHEND [7-0]								39h

11-0 RXHEND

Define the horizontal detection end position of RX receiving data for VINn.

7.6.39 RX Bit Number

Index	7	6	5	4	3	2	1	0	Reset
D7			RXBITNUM						27h

7-6 Reserved

5-0 RXBITNUM

(RXBITNUM+1) sets the total data bit number including first start bit 1 per line for VINn.

7.7 Audio Control Registers

***Following Index can be read/write accessible when APAGE=1.**

7.7.1 ADATR Output Data Select

Index	7	6	5	4	3	2	1	0	Reset
00				RPOS0					00h
01				RPOS1					00h
02				RPOS2					00h
03				RPOS3					00h
04				RPOS4					00h
05				RPOS5					00h
06				RPOS6					00h
07				RPOS7					00h
08				RPOS8					00h
09				RPOS9					00h
0A				RPOS10					00h
0B				RPOS11					00h
0C				RPOS12					00h
0D				RPOS13					00h
0E				RPOS14					00h
0F				RPOS15					00h
10				RPOS50					00h
11				RPOS51					00h
12				RPOS52					00h
13				RPOS53					00h

ADATR pin output serial digital audio data per one audio Fs sampling period by following timing order.

AMD=0 mode: Total 16 output timing position. Total 16 digital audio data are serialized.

ASYNR=0 RPOS0 RPOS1 RPOS2 RPOS3 RPOS4 RPOS5 RPOS6 RPOS7

ASYNR=1 RPOS8 RPOS9 RPOS10 RPOS11 RPOS12 RPOS13 RPOS14 RPOS15

AMD=1 mode: Total 20 output timing position as bellow. Total 20 digital audio data are serialized.

ASYNR=0 RPOS0 RPOS1 RPOS2 RPOS3 RPOS4 RPOS5 RPOS6 RPOS7 RPOS50 RPOS51

ASYNR=1 RPOS8 RPOS9 RPOS10 RPOS11 RPOS12 RPOS13 RPOS14 RPOS15 RPOS52 RPOS53

Output data at each timing position can be selected with following order by these registers.

01h = AIN1 (First chip AIN1) data

02h = AIN2 (First chip AIN2) data

03h = AIN3 (First chip AIN3) data

04h = AIN4 (First chip AIN4) data

05h = AIN5 (Second chip AIN1) data

06h = AIN6 (Second chip AIN2) data

07h = AIN7 (Second chip AIN3) data

08h = AIN8 (Second chip AIN4) data

09h = AIN9 (Third chip AIN1) data

0Ah = AIN10 (Third chip AIN2) data

0Bh = AIN11 (Third chip AIN3) data

0Ch = AIN12 (Third chip AIN4) data

0Dh = AIN13 (Forth chip AIN1) data

0Eh = AIN14 (Forth chip AIN2) data

0Fh = AIN15 (Forth chip AIN3) data

10h = AIN16 (Forth chip AIN4) data

11h = AUX1 (First chip AUX) data

12h = AUX2 (Second chip AUX) data

13h = AUX3 (Third chip AUX) data

14h = AUX4 (Forth chip AUX) data

15h = PB1 (First chip digital audio input) data

16h = PB2 (Second chip digital audio input) data

17h = PB3 (Third chip digital audio input) data

18h = PB4 (Forth chip digital audio input) data

19h = Mixing data

Others = 0 data output (no data output)

7.7.2 Audio Master Frequency Control

Index	7	6	5	4	3	2	1	0	Reset
14		ACKI [22-16]							**09h**
15	ACKI [15-8]								**B5h**
16	ACKI [7-0]								**83h**

ACKI [22-0] register is effective when MFMANU=1 and RACKSL=0.ACKI register defines audio system clock frequency by following equation.

AMD=0 mode

ACKI = 2 ^ 23 x 4 x 64 x Fs / XTI freq

AMD=1 mode

ACKI = 2 ^ 23 x 5 x 64 x Fs / XTI freq

For example, AMD=0 mode, Fs=8kHz audio sampling

ACKI = 2 ^ 23 x 4 x 64 x 8kHz / 27MHz = 636291.4512 = 09B583h

7.7.3 Record Audio Data Output Control

Index	7	6	5	4	3	2	1	0	Reset
17	ACASMAS	ACLK27POL	ACASOMD	RECSB	R0DLY	REC8BIT	RRISE	RECDSP	00h

7 ACASMAS

0 = audio cascade slave mode

1 = audio cascade master mode

6 ACLK27POL

0 = audio system clock is made from XTI

1 = audio system clock is made from inversed XTI

5 ACASOMD

0 = ALINKO output is made by negative edge of audio system clock

1 = ALINKO output is made by positive edge of audio system clock

4 RECSB

0 = ADATR/ADATM output data is signed format

1 = ADATR/ADATM output data is non-signed format

3 R0DLY

0 = ADATR/ADATM is 1T ACLKR delay output

1 = ADATR/ADATM is 0T ACLKR delay output

2 REC8BIT

0 = ADATR/ADATM is 16bit output mode

1 = ADATR/ADATM is 8bit output mode

1 RRISE

0 = ASYNR/ADATR/ADATM is ACLKR falling edge sync mode

1 = ASYNR/ADATR/ADATM is ACLKR rising edge sync mode

0 RECDSP

0 = ASYNR is I2S mode

1 = ASYNR is one ACLKR period high (1) sync mode. DSP mode

7.7.4 Master Audio Clock Control

Index	7	6	5	4	3	2	1	0	Reset
18	ADACK POL	AADCK POL	MACK MD	AMD	MFMANU	MFMODE			21h

7 ADACKPOL

0 = audio DAC clock polarity is not inversed

1 = audio DAC clock polarity is inversed

6 AADCKPOL

0 = audio ADC clock polarity is not inversed

1 = audio ADC clock polarity is inversed

5 MACKMD

0 = high period of audio clock in master mode is one XTI clock leng

1 = audio clock in master mode is near duty 50-50 when audio sampling rate Fs is less than 16 z

4 AMD

0 = AIN1/AIN2/AIN3/AIN4 only mode

1 = AIN1/AIN2/AIN3/AIN4/AUX mode

3 MFMANU

0 = audio system clock frequency in master mode is selected by MFMODE

1 = audio system clock frequency in master mode is controlled by ACKI register

2-0 MFMODE

This register select audio sampling rate Fs by following order automatically when MFMANU=0.

0h = 8kHz

1h = 16kHz

7.7.5 Record Audio Control

Index	7	6	5	4	3	2	1	0	Reset
19	MUTEM	MUTER	RACKSL	ACASEN	RDTMOE	RDTROE	RSYNOE	RACKOE	**00h**

7 MUTEM

0 = ADATM output is normal operation

1 = ADATM output is always 0

6 MUTER

0 = ADATR output is normal operation

1 = ADATR output is always 0

5 RACKSL

0 = Master audio clock mode. Audio clock is made in internal module.

1 = Slave audio clock mode. Audio clock is made by ACLKR input.

4 ACASEN

0 = Disable audio cascade

1 = Enable audio cascade

3 RDTMOE

0 = ADATM pin is tri-state output

1 = ADATM pin is normal output

2 RDTROE

0 = ADATR pin is tri-state output

1 = ADATR pin is normal output

1 RSYNOE

0 = ASYNR pin is input

1 = ASYNR pin is output

0 RACKOE

0 = ACLKR pin is input

1 = ACLKR pin is output

7.7.6 Audio DAC Data Select

Index	7	6	5	4	3	2	1	0	Reset
1A				ADAOUTSEL					00h

ADAOUTSEL select audio DAC output data by following order.

01h = AIN1 (First chip AIN1) data

02h = AIN2 (First chip AIN2) data

03h = AIN3 (First chip AIN3) data

04h = AIN4 (First chip AIN4) data

05h = AIN5 (Second chip AIN1) data

06h = AIN6 (Second chip AIN2) data

07h = AIN7 (Second chip AIN3) data

08h = AIN8 (Second chip AIN4) data

09h = AIN9 (Third chip AIN1) data

0Ah = AIN10 (Third chip AIN2) data

0Bh = AIN11 (Third chip AIN3) data

0Ch = AIN12 (Third chip AIN4) data

0Dh = AIN13 (Forth chip AIN1) data

0Eh = AIN14 (Forth chip AIN2) data

0Fh = AIN15 (Forth chip AIN3) data

10h = AIN16 (Forth chip AIN4) data

11h = AUX1 (First chip AUX) data

12h = AUX2 (Second chip AUX) data

13h = AUX3 (Third chip AUX) data

14h = AUX4 (Forth chip AUX) data

15h = PB1 (First chip digital audio input) data

16h = PB2 (Second chip digital audio input) data

17h = PB3 (Third chip digital audio input) data

18h = PB4 (Forth chip digital audio input) data

19h = Mixing data

Others = 0 data output (no data output)

7.7.7 Playback Audio Control

Index	7	6	5	4	3	2	1	0	Reset
1B		PB8BIT	PBSB	PB0DLY	PBRISE	PBDSP	PBLR	PBMAS	00h

7 Reserved

6 PB8BIT

0 = ADATP is 16bit input

1 = ADATP is 8bit input

5 PBSB

0 = ADATP input data is signed format

1 = ADATP input data is non-signed format

4 PB0DLY

0 = ADATP is 1T ACLKP delay input

1 = ADATP is 0T ACLKP delay input

3 PBRISE

0 = ASYNP/ADATP is ACLKP falling edge sync mode

1 = ASYNP/ADATP is ACLKP rising edge sync mode

2 PBDSP

0 = ASYNP is I2S mode

1 = ASYNP is one ACLKP period high (1) sync mode. DSP mode

1 PBLR

0 = Receive ADATP data from L(0) side in I2S mode

1 = Receive ADATP data from R(1) side in I2S mode

0 PBMAS

0 = ACLKP/ASYNP is input

1 = ACLKP/ASYNP is output

7.7.8 Audio Detection Control

Index	7	6	5	4	3	2	1	0	Reset
1C	ADETTH								08h

7-0 This register determine amplitude level to detect audio data

7.7.9 Audio ADC/DAC Test

Index	7	6	5	4	3	2	1	0	Reset
1D		AFPOL	AATEST	AFTEST	AFDIS	TADACO	ATHRU	ADCCTL	00h

7 Reserved

6 AFPOL

0 = Polarity of CALSW signal to audio ADC is not inversed

1 = Polarity of CALSW signal to audio ADC is inversed

5 AATEST

0 = Audio ADC and Audio DAC are in normal operation

1 = Test purpose only

XTI input is connected to audio ADC clock input and audio DAC clock input.

{VD2_7-0, TXD4, TXD3} input is connected to audio DAC data input.

4 AFTEST

0 = CALSW signal to audio ADC is in normal operation

1 = Test purpose only

CALSW signal audio ADC is always cut-off control status.

3 AFDIS

0 = Enable automatic DC level adjustment for audio ADC data

1 = Disable automatic DC level adjustment for audio ADC data

2 TADACO

0 = Audio DAC input data is normal data

1 = Test purpose only

{VD2_7-0, TXD4, TXD3} input is connected to audio DAC data input.

1 ATHRU

0 = Audio DAC input data is normal data

1 = Test purpose only

One of audio ADC output data is connected to audio DAC data input.

ADAOUTSEL register defines the audio ADC data by following order.

01h = AIN1 audio ADC output data

02h = AIN2 audio ADC output data

03h = AIN3 audio ADC output data

04h = AIN4 audio ADC output data

Others = AUX audio ADC output data

0 ADCCTL

The control of writing 0 and then 1 restart automatic DC level adjustment for audio ADC data.

7.7.10 Audio ADC Control

Index	7	6	5	4	3	2	1	0	Reset
1E					VBG_SL	ISEL_AD			00h

3 VGB_SL

0 = BG reference

1 = VDD reference

2-0 ISEL_AD, current control

0 = Default

7.7.11 Audio DAC Control

Index	7	6	5	4	3	2	1	0	Reset
1F		PWD12_BACK	PWD12_DAC	DCK_INV	AOUT_GAIN				08h

7 Reserved

6 PWD12_BACK

0 = Normal operation for audio DAC backend

1 = Power down for audio DAC backend

5 PWD12_DAC

0 = Normal operation for audio DAC

1 = Power down for audio DAC

4 DCK_INV

0 = Audio DAC clock is normal in audio DAC

1 = Audio DAC clock is inverted in audio DAC

3-0 AOUT_GAIN

AOUT gain control in audio DAC backend

Gain range from -6dB to 6dB with 0dB at AOUT_GAIN=0xA

7.7.12 ADATM Output Select

Index	7	6	5	4	3	2	1	0	Reset
20				MPOS0					00h
21				MPOS1					00h
22				MPOS2					00h
23				MPOS3					00h
24				MPOS4					00h
25				MPOS5					00h
26				MPOS6					00h
27				MPOS7					00h
28				MPOS8					00h
29				MPOS9					00h
2A				MPOS10					00h
2B				MPOS11					00h
2C				MPOS12					00h
2D				MPOS13					00h
2E				MPOS14					00h
2F				MPOS15					00h
30				MPOS50					00h
31				MPOS51					00h
32				MPOS52					00h
33				MPOS53					00h

ADATM pin output serial digital audio data per one audio Fs sampling period by following timing order.

AMD=0 mode: Total 16 output timing position. Total 16 digital audio data are serialized.

ASYNR=0 MPOS0 MPOS1 MPOS2 MPOS3 MPOS4 MPOS5 MPOS6 MPOS7

ASYNR=1 MPOS8 MPOS9 MPOS10 MPOS11 MPOS12 MPOS13 MPOS14 MPOS15

AMD=1 mode: Total 20 output timing position as bellow. Total 20 digital audio data are serialized.

ASYNR=0 MPOS0 MPOS1 MPOS2 MPOS3 MPOS4 MPOS5 MPOS6 MPOS7 MPOS50 MPOS51

ASYNR=1 MPOS8 MPOS9 MPOS10 MPOS11 MPOS12 MPOS13 MPOS14 MPOS15 MPOS52 MPOS53

Output data at each timing position can be selected with following order by these registers.

01h = AIN1 (First chip AIN1) data

02h = AIN2 (First chip AIN2) data

03h = AIN3 (First chip AIN3) data

04h = AIN4 (First chip AIN4) data

05h = AIN5 (Second chip AIN1) data

06h = AIN6 (Second chip AIN2) data

07h = AIN7 (Second chip AIN3) data

08h = AIN8 (Second chip AIN4) data

09h = AIN9 (Third chip AIN1) data

0Ah = AIN10 (Third chip AIN2) data

0Bh = AIN11 (Third chip AIN3) data

0Ch = AIN12 (Third chip AIN4) data

0Dh = AIN13 (Forth chip AIN1) data

0Eh = AIN14 (Forth chip AIN2) data

0Fh = AIN15 (Forth chip AIN3) data

10h = AIN16 (Forth chip AIN4) data

11h = AUX1 (First chip AUX) data

12h = AUX2 (Second chip AUX) data

13h = AUX3 (Third chip AUX) data

14h = AUX4 (Forth chip AUX) data

15h = PB1 (First chip digital audio input) data

16h = PB2 (Second chip digital audio input) data

17h = PB3 (Third chip digital audio input) data

18h = PB4 (Forth chip digital audio input) data

19h = Mixing data

Others = 0 data output (no data output)

7.7.13 Mixing Rate Control

Index	7	6	5	4	3	2	1	0	Reset
34	AIN2MIXRATE				AIN1MIXRATE				**55h**
35	AIN4MIXRATE				AIN3MIXRATE				**55h**
36	PBMIXRATE				AUXMIXRATE				**55h**

Mixed audio data is controlled by the mixing ratio of different audio data sources as follow.

AIN1MIXRATE is mixing rate for AIN1 digital data.

AIN2MIXRATE is mixing rate for AIN2 digital data.

AIN3MIXRATE is mixing rate for AIN3 digital data.

AIN4MIXRATE is mixing rate for AIN4 digital data.

AUXMIXRATE is mixing rate for AUX digital data.

PBMIXRATE is mixing rate for ACLKP/ASYNP/ADATP digital audio input data.

The mixing percentage can be expressed as %= MIXRATE / (2^ (4+AMIXMD))

7.7.14 Mixing Mute Control

Index	7	6	5	4	3	2	1	0	Reset
37			PBM MUTE	AUXM MUTE	AIN4M MUTE	AIN3M MUTE	AIN2M MUTE	AIN1M MUTE	3Fh

These register control mixing mute on/off (do mixing/don't mixing) per each digital audio data.

0 = Mute off. Do mixing of this digital audio data.

1 = Mute on. NO mixing of this digital audio data.

PBMMUTE is for ACLKP/ASYNP/ADATP digital audio input data.

AUXMMUTE is for AUX digital audio data.

AIN4MMUTE is for AIN4 digital audio data.

AIN3MMUTE is for AIN3 digital audio data.

AIN2MMUTE is for AIN2 digital audio data.

AIN1MMUTE is for AIN1 digital audio data.

7.7.15 Digital Audio Gain Control

Index	7	6	5	4	3	2	1	0	Reset
38		ACAS MIXEN	AMIXMD		DAOGAIN				38h

7 Reserved

6 ACASMIXEN

0 = Not add digital mixing audio data received in digital audio cascade input signal

1 = Add digital mixing audio data received in digital audio cascade input signal

5-4 AMIXMD

This register selects digital audio mixing mode.

0h = MIXRATE /16

1h = MIXRATE /32

2h = MIXRATE /64

3h = MIXRATE / 128

MIXRATE is the value of Mix Rate Control register

3-0 DAOGAIN

DAOGAIN do digital gain control for audio DAC input data.

Gain control equation

Output = Input x (1 x DAOGAIN[3] + 1/2 x DAOGAIN[2] + 1/4 x DAOGAIN[1] + 1/8 x DAOGAIN[0])

Default 8h is gain 1. Digital audio data is not changed by DAOGAIN in this default value.

7.7.16 Analog Audio Input Gain Control

Index	7	6	5	4	3	2	1	0	Reset
39	GAIN_AIN2				GAIN_AIN1				88h
3A	GAIN_AIN4				GAIN_AIN3				88h
3B					GAIN_AUX				08h

These registers control the gain of analog audio input signal. range -6dB to +6dB.

Default 8h = 0dB.

GAIN_AIN1 is for AIN1 input signal

GAIN_AIN2 is for AIN2 input signal

GAIN_AIN3 is for AIN3 input signal

GAIN_AIn4 is for AIN4 input signal

GAIN_AUX is for AUX input signal

7.7.17 Audio ADC Power Down Control

Index	7	6	5	4	3	2	1	0	Reset
3C			PWD12_ ADC	PWD12_ AUX	PWD12_ AIN4	PWD12_ AIN3	PWD12_ AIN2	PWD12_ AIN1	00h

5 PWD12_ADC

0 = Audio ADC is in normal operation

1 = Audio ADC is in power down mode

4 PWD12_AUX

0 = AUX input portion (Buffer + PGA + AAF) is in normal operation

1 = AUX input portion (Buffer + PGA + AAF) is in power down mode

3 PWD12_AIN4

0 = AIN4 input portion (Buffer + PGA + AAF) is in normal operation

1 = AIN4 input portion (Buffer + PGA + AAF) is in power down mode

2 PWD12_AIN3

0 = AIN3 input portion (Buffer + PGA + AAF) is in normal operation

1 = AIN3 input portion (Buffer + PGA + AAF) is in power down mode

1 PWD12_AIN2

0 = AIN2 input portion (Buffer + PGA + AAF) is in normal operation

1 = AIN2 input portion (Buffer + PGA + AAF) is in power down mode

0 PWD12_AIN1

0 = AIN1 input portion (Buffer + PGA + AAF) is in normal operation

1 = AIN1 input portion (Buffer + PGA + AAF) is in power down mode

7.7.18 Audio Reset

Index	7	6	5	4	3	2	1	0	Reset
3D								ARST	00h

7-1 Reserved

0 ARST

Writing '1' to this bit performs soft reset of digital audio logics but not affecting the register value. The bit is self-resetting after written.

7.7.19 Analog Audio Test

Index	7	6	5	4	3	2	1	0	Reset
3E	AUDIO_TEST								00h

7-6 Audio AFE Test (Set to Bit2-Bit0=111, Reg1F=6Xh)

00; Ground level

01; 3.3V Power level

10; Input Buffer output

11; Low Pass Filter output

5-3 Audio AFE Interface Test (Set to Bit2-Bit0=000, Reg1F=6Xh)

000; Open/Off

001; ADC positive reference

010; ADC reference common

011; ADC negative reference

100; Audio Mux outputP

101; Audio Mux outputN

110; S2D outputP

111; S2D outputN

2-0 Audio BACK END Test

000; Normal Operation Mode

001; Audio Front End Test mode

010; VREFH test (Set to Reg1F=4Xh)

100; DAC VCOM Test (Set to Reg1F=4Xh)

110; Resister test (Set to Reg1F=6Xh)

Recommend Reg3E=00h (Normal Operation)

7.7.20 Digital Audio Input DC level Control

Index	7	6	5	4	3	2	1	0	Reset
41							AIN1ADJ [9-8]		00h
42	AIN1ADJ [7-0]								00h
43							AIN2ADJ [9-8]		00h
44	AIN2ADJ [7-0]								00h
45							AIN3ADJ [9-8]		00h
46	AIN3ADJ [7-0]								00h
47							AIN4ADJ [9-8]		00h
48	AIN4ADJ [7-0]								00h
49							AUXADJ [9-8]		00h
4A	AUXADJ [7-0]								00h

These register control DC level of digital audio data received from audio ADC. These register value are signed format value. MSB bit9 is signed bit.

Calculated output data is signed format.

Output data = original signed digital audio data + AINnADJ

For example,

+1 level up

Output data = original signed digital audio data + 001h

-1 level down

Output data = original signed digital audio data + 3FFh

7.7.21 DC Adjusted Digital Audio Data Readout

Index	7	6	5	4	3	2	1	0	Reset
4B							AIN1DC [9-8]		-
4C	AIN1DC [7-0]								-
4D							AIN2DC [9-8]		-
4E	AIN2DC [7-0]								-
4F							AIN3DC [9-8]		-
50	AIN3DC [7-0]								-
51							AIN4DC [9-8]		-
52	AIN4DC [7-0]								-
53							AUXDC [9-8]		-
54	AUXDC [7-0]								-

These registers show digital audio input data adjusted DC level by automatic adjustment and AINnADJ register adjustment. These registers are read only. These registers are test purpose only.

7.7.22 Digital Audio Input Data Readout

Index	7	6	5	4	3	2	1	0	Reset
55							AIN1IN [9-8]		-
56	AIN1IN [7-0]								-
57							AIN2IN [9-8]		-
58	AIN2IN [7-0]								-
59							AIN3IN [9-8]		-
5A	AIN3IN [7-0]								-
5B							AIN4IN [9-8]		-
5C	AIN4IN [7-0]								-
5D							AUXIN [9-8]		-
5E	AUXIN [7-0]								-

These registers show digital audio input data received from audio ADC. These registers are read only. These registers are test purpose only.

7.7.23 Audio Input Status

Index	7	6	5	4	3	2	1	0	Reset
5F				AIN1DET					-
60				AIN2DET					-
61				AIN3DET					-
62				AIN4DET					-

These registers are read only.

7-4 Reserved

4-0 AIN1DET, It reflects the detection status of 5 audio inputs channel AUX, AIN4, AIN3, AIN2 and AIN1 of the current chip.

In the audio cascade mode, AIN2DET, AIN3DET and AIN4DET correspond to the input status of chip #2, #3 and #4, respectively.

7.7.24 Average Audio ADC Data

Index	7	6	5	4	3	2	1	0	Reset
63							AIN1AV [9-8]		02h
64	AIN1AV [7-0]								00h
65							AIN2AV [9-8]		02h
66	AIN2AV [7-0]								00h
67							AIN3AV [9-8]		02h
68	AIN3AV [7-0]								00h
69							AIN4AV [9-8]		02h
6A	AIN4AV [7-0]								00h
6B							AUXAV [9-8]		02h
6C	AUXAV [7-0]								00h

These registers show average value of continuous 128 audio ADC data when audio ADC CALSW=0,audio input is cut off condition. These registers are read only. These registers are test purpose only.

7.7.25 Adjusted Audio DC Level

Index	7	6	5	4	3	2	1	0	Reset
6D							AIN1ADJDC [9-8]		02h
6E	AIN1ADJDC [7-0]								00h
6F							AIN2ADJDC [9-8]		02h
70	AIN2ADJDC [7-0]								00h
71							AIN3ADJDC [9-8]		02h
72	AIN3ADJDC [7-0]								00h
73							AIN4ADJDC [9-8]		02h
74	AIN4ADJDC [7-0]								00h
75							AUXADJDC [9-8]		02h
76	AUXADJDC [7-0]								00h

These registers show adjusted DC level by holding average value of continuous 128 audio ADC data when audio ADC CALSW=0,audio input is cut off condition. These registers are read only. These registers are test purpose only.

7.7.26 CASCADE TX Test Data

Index	7	6	5	4	3	2	1	0	Reset
77			TNUM3		TNUM2		TNUM1		39h

This register set up test data in cascade cell location 2, 9 and 16 for Tnum1, Tnum2 and Tnum3, respectively.

Reserved for debugging purpose.

7.7.27 CASCADE RX Test Data

Index	7	6	5	4	3	2	1	0	Reset
78			RNUM4		RNUM3		RNUM2		-

This register stores the received test data in cascade mode. Reserved for debugging purpose.

7.7.28 CASCADE TX Data

Index	7	6	5	4	3	2	1	0	Reset
79		PD12BG	LDO_BG	LDO_PD	ACKDLY	ATEST_SEL			00h

This register is reserved for debugging purpose.

6 PD12BG, 1.2V BG power down control

5 LDO_BG, BG selection for LDO

4 LDO_PD, LDO power down control

3 ACKDLY, Clock delay control

2-0 ATEST_SEL, Analog test modes control.

7.7.29 CASCADE TX Data

Index	7	6	5	4	3	2	1	0	Reset
7A	ADC_CTRL								00h

This register is reserved for internal debugging.

7.7.30 Coaxial Audio Selection

Index	7	6	5	4	3	2	1	0	Reset
7B					CXSEL				00h

3-0 CXSEL. These bits control the audio data selection for each corresponding channel. CXSEL [0] controls channel 1 and etc.

1 = Coaxial audio 0 = AIN base-band audio

7.7.31 Bias Gen & VTG Control

Index	7	6	5	4	3	2	1	0	Reset
00	PWD12 BG	ISEL			VBG SELB	IPSEL			44h

7 PWD12BG

0 = BANDGAP is normal operation

1 = BANDGAP is power down

6-4 ISEL

Bias Current Adjust

3 VBGSELB

Bandgap select

2-0 IPSEL

Driver Reference DC Adjust

~~7.7.31~~7.7.32 Clock Lane Control Register

Index	7	6	5	4	3	2	1	0	Reset
01	CKHS BUF1	CKHS BUF0	CKLPBUF		CKINV SEL	CKPH			F0h

7 CKHSBUF1

Driving Capability control 1

6 CKHSBUF0

Driving Capability control 0

5-4 CKLPBUF

Clock Lane Slew rate control for Low power Clock driver

00 : 0pF 01 : 5pF 10 : 20pF 11 : 70pF

3 CKINVSEL

Clock output invert select

2-0 CKPH

Clock output delay control

7.8 MIPI and PLL Control Registers

7.8.1 MIPICKEN

Index	7	6	5	4	3	2	1	0	Reset
02					CKHINVSER	CKINVSER	PWD12CK	MIPICKEN	00h

7-4 Reserved

3 CKHINVSER

Half Full Speed Clock invert for Serializer

0 = not inversed

1 = inversed

2 CKINVSER

Full Speed Clock invert for Serializer

0 = not inversed

1 = inversed

1 PWD12CK

0 = CK Lane is normal operation

1 = CK Lane is power down

0 MIPICKEN

0 = disable MIPI Clock output

1 = enable MIPI Clock output

7.8.2 Lane0-1 Data Latch Clock Phase Select

Index	7	6	5	4	3	2	1	0	Reset
03		D_PH1				D_PH0			00h

7 Reserved

6-4 D_PH1

Lane1 data Latch clock phase select for Serializer

3 Reserved

2-0 D_PH0

Lane0 data Latch clock phase select for Serializer

7.8.3 Lane2-3 Data Latch Clock Phase Select

Index	7	6	5	4	3	2	1	0	Reset
04		D_PH3			SKIP_ FRAME3	D_PH2			00h

7 Reserved

6-4 D_PH3

Lane3 data Latch clock phase select for Serializer

3 SKIP_FRAME3

0 = Frame Start/End sent at each field VBLANK for channel 3

1 = Frame Start/End sent only at even field VBLANK for channel 3

2-0 D_PH2

Lane2 data Latch clock phase select for Serializer

7.8.4 HS Driver Capability Select

Index	7	6	5	4	3	2	1	0	Reset
06	HSTX3 BUF1	HSTX2 BUF1	HSTX1 BUF1	HSTX0 BUF1	HSTX3 BUF0	HSTX2 BUF0	HSTX1 BUF0	HSTX0 BUF0	FFh

7 HSTX3BUF1

Lane3 HS Driver capability select1

6 HSTX2BUF1

Lane2 HS Driver capability select1

5 HSTX1BUF1

Lane1 HS Driver capability select1

4 HSTX0BUF1

Lane0 HS Driver capability select1

3 HSTX3BUF0

Lane3 HS Driver capability select0

2 HSTX2BUF0

Lane2 HS Driver capability select0

1 HSTX1BUF0

Lane1 HS Driver capability select0

0 HSTX0BUF0

Lane0 HS Driver capability select0

7.8.5 Low Power mode Slew Rate Control

Index	7	6	5	4	3	2	1	0	Reset
07	LPTXBUF3		LPTXBUF2		LPTXBUF1		LPTXBUF0		FFh

7-6 LPTXBUF3

Lane3 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

5-4 LPTXBUF2

Lane2 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

3-2 LPTXBUF1

Lane1 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

1-0 LPTXBUF0

Lane0 PHY Driver Low Power mode slew rate control

00: 0pF 01: 5pF 10: 20pF 11: 70pF

7.8.6 MIPI Output Enable Control

Index	7	6	5	4	3	2	1	0	Reset
08	PWD_3	PWD_2	PWD_1	PWD_0	MIPIEN3	MIPIEN2	MIPIEN1	MIPIEN0	00h

7 PWD_3

0 = Lane3 is disable (power down) for Serializer

1 = Lane3 is enable for Serializer

6 PWD_2

0 = Lane2 is disable (power down) for Serializer

1 = Lane2 is enable for Serializer

5 PWD_1

0 = Lane1 is disable (power down) for Serializer

1 = Lane1 is enable for Serializer

4 PWD_0

0 = Lane0 is disable (power down) for Serializer

1 = Lane0 is enable for Serializer

3 MIPIEN3

0 = Lane3 MIPI Output disable

1 = Lane3 MIPI Output enable

2 MIPIEN2

0 = Lane2 MIPI Output disable

1 = Lane2 MIPI Output enable

1 MIPIEN1

0 = Lane1 MIPI Output disable

1 = Lane1 MIPI Output enable

0 MIPIEN0

0 = Lane0 MIPI Output disable

1 = Lane0 MIPI Output enable

7.8.7 MIPITEST1

Index	7	6	5	4	3	2	1	0	Reset
09	MIPITEST1								00h

Reserved

7.8.8 MIPITEST2

Index	7	6	5	4	3	2	1	0	Reset
0A	MIPITEST2								00h

Reserved

7.8.9 PLL Control 1 (General)

Index	7	6	5	4	3	2	1	0	Reset
10	RST_PLL_REG	PWDPLL	VCO_SEL		LOCK_ENB	LOCK_VREF			20h

7 RST_PLL_REG

0 = normal

1 = register controlled reset

6 PWDPLL

0 = normal

1 = register controlled PLL power down

5-4 VCO_SEL

00 = 600MHz

01 = 800MHz

10 = 1.3GHz

11 = 1.7GHz

3 LOCK_ENB. When disabled, the PLL lock output stays high.

0 = lock detector enabled

1 = disabled

2-0 LOCK_VREF. PLL lock detector duty cycle threshold selection (2.27% per step)

000 = 81.8%

001 = 84.07%

…

111 = 97.7%

7.8.10 PLL Control 2 (Loop)

Index	7	6	5	4	3	2	1	0	Reset
11	DEGLITCH_SEL		TEST_SEL			ICP_SEL			03h

7:6 DEGLITCH_SEL

00 = no deglitching function

01 = reject 1ns clock glitch

10 = reject 2ns clock glitch

11 = reject 3ns clock glitch

5-3 TEST_SEL TEST mux selection

000=

100=test mux enabled, input reference clock is muxed to the output

101= test mux enabled, PLL input divider output is muxed to the output

110= test mux enabled, feedback clock at the PFD input node is muxed out

111= test mux enabled, lock detector output is muxed out

2-0 ICP_SEL charge pump current selection

000 = 2.5uA

001=5.0uA

010=7.5uA

011=10.0uA (default)

100=12.5uA

101=15.0uA

110=17.5uA

111=20.0uA

7.8.11 PLL Control 3 (FB Divider)

Index	7	6	5	4	3	2	1	0	Reset
12	DIV_PRE_FB		DIV_POST_FB						54h

7-6 DIV_PRE_FB PLL feedback pre-divider selection

00 = div-by-1

01 = div-by-2

10 = div-by-4

11 = no division. Divider output clock stays at low

5 DIV_POST_FB<5:0> Feedback divider control

000000= div-by-2,

… …

010100= div-by-22 (default)

… …

111110= div-by-64,

111111= div-by-65

Division number = 2 + DIV_POST_FB

Please note, the divider speed limit is 1.1G.

7.8.12 PLL Control 4 (Pre & Post Divider)

Index	7	6	5	4	3	2	1	0	Reset
13	DIV_FIN			BYPASS_27M	DIV_OUT_PRE	DIV_OUT_POST			E7h

This PLL generates PLL output clock (F_PLL) with an output divider. The output divider includes a pre-divider, a post-divider, and a mux with option to bypass 27MHz reference clock.

7-6 DIV_FIN<2:0>

000 = div-by-2

001 = div-by-3

010 = div-by-4

011 = div-by-5

100 = div-by-6

101 = div-by-7

110 = div-by-8

111 = div-by-1

4 BYPASS_27M

0 = normal

1 = bypass output divider. The output divider has a mux to bypass 27MHz clock to the output

3 DIV_OUT_PRE

0 = div by 1

1 = div-by-2

2-0 DIV_OUT_POST<2:0>

000 = div by2

001 = div-by-3

010 = div-by-4

011 = div-by-5

100 = div by6

101 = div-by-7

110 = div-by-8

111 = div-by-1

Please note, the divider speed limit is 1.1GHz if DIV_OUT_POST<2:0>= 000 to 110. If the clock speed is higher than the limit, the output will get a wrong frequency, or no clock output at all. However, for DIV_OUT_POST<2:0>=111, the output clock has no speed limitation.

7.8.13 PLL Control 5 (Dividers)

Index	7	6	5	4	3	2	1	0	Reset
14	RST_CLK_GEN	DIV_CSI_CLK			BIT_CLK2_SEL	DIV_PHY_CLK			33h

The PLL is followed by a Clock Generator (CLK_GEN) to create multiple clocks. Register 14, and 15 control the CLK_GEN operation.

7 RST_CLK_GEN Divider Reset

0 = normal operation

1 = reset all the dividers inside the CLK_GEN

6-4 DIV_CSI_CLK CSI_CLK frequency selection

000, CSI_CLK = F_PLL/1

001, CSI_CLK = F_PLL/2

010, CSI_CLK = F_PLL/4

011, CSI_CLK = F_PLL/8 (default)

100, CSI_CLK = F_PLL/16

101, CSI_CLK = F_PLL/32

110, CSI_CLK = F_PLL/64

111, CSI_CLK = F_PLL/128

3 BIT_CLK2_SEL BIT_CLK output mux selection

0 = use own PLL to generate the BIT_CLK

1 = use BIT_CLK2_IN from the other PLL to generate BIT_CLK clock

2-0 DIV_PHY_CLK PHY_CLK frequency selection

000, PHY_CLK = F_PLL/1

001, PHY_CLK = F_PLL/2

010, PHY_CLK = F_PLL/4

011, PHY_CLK = F_PLL/8 (default)

100, PHY_CLK = F_PLL/16

101, PHY_CLK = F_PLL/32

110, PHY_CLK = F_PLL/64

111, PHY_CLK = F_PLL/128

7.8.14 PLL Control 6 (Dividers)

Index	7	6	5	4	3	2		0	Reset
15	N/A			DIV_CLK_DEC			DIV_BIT_CLK		**0Ch**

7-5 Reserved

4-2 DIV_CLK_DEC CLK_DEC frequency selection

000, CLK_DEC = F_PLL/1

001, CLK_DEC = F_PLL/2

010, CLK_DEC = F_PLL/4

011, CLK_DEC = F_PLL/8 (default)

100, CLK_DEC = F_PLL/16

101, CLK_DEC = F_PLL/32

110, CLK_DEC = F_PLL/64

111, CLK_DEC = F_PLL/128

The register DIV_CLK_DEC also controls CLK_DEC2X and CLK_DECDIV2 frequency simultaneously. The relationship is CLK_DEC2X = CLK_DEC*2, and CLK_DECDIV2 = CLK_DEC/2. However, when DIV_CLK_DEC=000, CLK_DEC2X=low (stay at low, with no active output clock). Similarly, when DIV_CLK_DEC=111, CLK_DECDIV2=low (stay at low, with no active output clock).

1-0 DIV_BIT_CLK BIT_CLK frequency selection

00, BIT_CLK = F_PLL/1

01, BIT_CLK = F_PLL/2

10, BIT_CLK = F_PLL/4

11, BIT_CLK = F_PLL/8

7.8.15 MIPI DATA FORMAT

Index	7	6	5	4	3	2	1	0	Reset
19			FORMAT						1Eh

7-6 Reserved

5-3 FORMAT

MIPI output format as defined in the MIPI CSI specification. Only the following formats are valid for this device.

18h = YUV 4:2:0 8-bit

1Ah = YUV 4:2:0 LEGACY 8-bit

1Eh = YUV 4:2:2 8-bit (default)

24h = RGB 24-Bbit

2Bh = RAW 10-bit

30h = YUV 4:4:4 8-bit (user defined MIPI format)

7.8.16 MIPI NUM_LANES

Index	7	6	5	4	3	2	1	0	Reset
20		NUM_CHANNELS				NUMLANES			24h

7 Reserved

6-4 NUM_CHANNELS

Number of video channels to be processed

3 Reserved

2-0 NUM_LANES

Number of MIPI data lanes to use for Tx

7.8.17 MIPI MODE Control

Index	7	6	5	4	3	2	1	0	Reset
21	TP_ENA	DUAL_ MODE	SKIP_ FRAME2	SKIP_ FRAME1	PSFM	SKIP_ FRAME0	SEND_ LN_END	FRAME_ NUM_EN	03h

7 TP_ENA

0 = Normal output

1 = Test pattern output

6 DUAL_MODE

0 = Single CSI to NUM_LANES DPHY data lanes

1 = Dual CSI split between available DPHY data lanes (NUM_LANES ea

5 SKIP_FRAME2

0 = Frame Start/End sent at each field VBLANK for channel 2

1 = Frame Start/End sent only at even field VBLANK for channel 2

4 SKIP_FRAME1

0 = Frame Start/End sent at each field VBLANK for channel 1

1 = Frame Start/End sent only at even field VBLANK for channel 1

3 PSFM

0 = Normal framing independent on each channel

1 = Pseudo-Single Frame Mode (explained in MIPI descriptic

2 SKIP_FRAME0

0 = Frame Start/End sent at each field VBLANK for channel 0

1 = Frame Start/End sent only at even field VBLANK for channel 0

1 SEND_LN_END

0 = Video lines sent at start of HACTIVE

1 = Video lines sent at end of HACTIVE

0 FRAME_NUM_EN

0 = Frame numbering is disabled (frame number is always 0)

1 = Frame numbering is enabled (counts from 1 to 15)

7.8.18 MIPI CH_ENA

Index	7	6	5	4	3	2	1	0	Reset
22	CSI2_CH_ENA				CSI1_CH_ENA				0Fh

7-4 Enable video channels 4 through 1 on CSI-2 (DUAL_MODE only)

3-0 Enable video channels 4 through 1 on CSI-1

7.8.19 MIPI STOPCLK Control

Index	7	6	5	4	3	2	1	0	Reset
23							STOP CLK	ULPM CLK	00h

7-2 Reserved

1 STOPCLK

0 = normal operation

1 = Force DPHY clock lane into STOP state

0 UPMCLK

0 = normal operation

1 = Put clock lane into Ultra Low Power Mode

7.8.20 MIPI CLKESC

Index	7	6	5	4	3	2	1	0	Reset
24	ULPM				CLKESC				00h

7-4 ULPM [3-0]

0 = normal operation

1 = Put data lanes into ULPM (1-bit per lane)

3-0 CLKESC [3-0]

0 = normal operation

1 = Data lane Clock Escape request (1-bit per lane)

7.8.21 MIPI LP Transition TimeControl

Index	7	6	5	4	3	2	1	0	Reset
25	T_LPX								04h

7-0 T_LPX All lanes Low Power state transition time (phy_clk cycles)

7.8.22 T_PREP Control

Index	7	6	5	4	3	2	1	0	Reset
26	T_PREP								06h

7-0 T_PREP All lanes preparation time (phy_clk cycles)

7.8.23 T_TRAIL Control

Index	7	6	5	4	3	2	1	0	Reset
27	T_TRAIL								03h

7-0 T_TRAIL All lanes ~final Tx bit trail time (phy_clk cycles)

7.8.24 T_WAKE Control

Index	7	6	5	4	3	2	1	0	Reset
28	T_WAKE								18h

7-0 T_WAKE All lanes ULPM wake up time (phy_clk cycles)

7.8.25 T_EXIT Control

Index	7	6	5	4	3	2	1	0	Reset
29	T_EXIT								02h

7-0 T_EXIT All lanes STOP state wait time between lines (phy_clk cycles)

7.8.26 HACTIVE_LN Status

Index	7	6	5	4	3	2	1	0	Reset
2B	CH0_HACTIVE_LN [7-0]								R
2C	CH0_HACTIVE_LN [15-8]								R
2D	CH1_HACTIVE_LN [7-0]								R
2E	CH1_HACTIVE_LN [15-8]								R
2F	CH2_HACTIVE_LN [7-0]								R
30	CH2_HACTIVE_LN [15-8]								R
31	CH3_HACTIVE_LN [7-0]								R
32	CH3_HACTIVE_LN [15-8]								R

CHx_HACTIVE_LN [15-0]

Detected horizontal active line length in pixels (read only)

7.8.27 Digital MIPI Reset

Index	7	6	5	4	3	2	1	0	Reset
33					RST_PHY	RST_CSI	RST_MUX	RST_IN	00h

7-4 Reserved

3 RST_PHY

0 = DPHY modules are in normal operation

1 = DPHY modules are in reset

2 RST_CSI

0 = CSI modules are in normal operation

1 = CSI modules are in reset

1 RST_MUX

0 = VC mux/FIFO modules are in normal operation

1 = VC mux/FIFO modules are in reset

0 RST_IN

0 = MIPI Input modules are in normal operation

1 = MIPI input modules are in reset

7.8.28 Virtual Channel ID

Index	7	6	5	4	3	2	1	0	Reset
34	CH4_VCI		CH3_VCI		CH2_VCI		CH1_VCI		E4h

7-6 CH4_VCI

Virtual Channel ID for video channel4

5-4 CH3_VCI

Virtual Channel ID for video channel3

3-2 CH2_VCI

Virtual Channel ID for video channel2

1-0 CH1_VCI

Virtual Channel ID for video channel 1

7.8.29 FE_WAIT Control

Index	7	6	5	4	3	2	1	0	Reset
35	FE_ADJ		FE_WAIT						15h

7-6 FE_ADJ

Frame End wait adjustment for odd field (-2 to 1 in two's compliment)

5-0 FE_WAIT

Frame End wait in lines after VACTIVE fall (PSFM mode)

7.8.30 OVERFLOW/UNDERFLOW FIFO Status

Index	7	6	5	4	3	2	1	0	Reset
36	OVERFLOW				UNDERFLOW				00h

7-4 OVERFLOW

Channel 0-3 - FIFO overflow indicator (read only)

3-0 UNDERFLOW

Channel 0-3 - FIFO underflow indicator (read only)

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10 Revision history

Date	Note
9/18/2019	Initial Draft
9/24/2019	Update Pin diagram and VDDPLL
12/17/2019	Multiple updates for preliminary release
04/17/2020	Updates to include 1.8V I/O support