An Open-Source Adaptive Event-Based ADC for Bio-Signal Acquisition in 130nm CMOS

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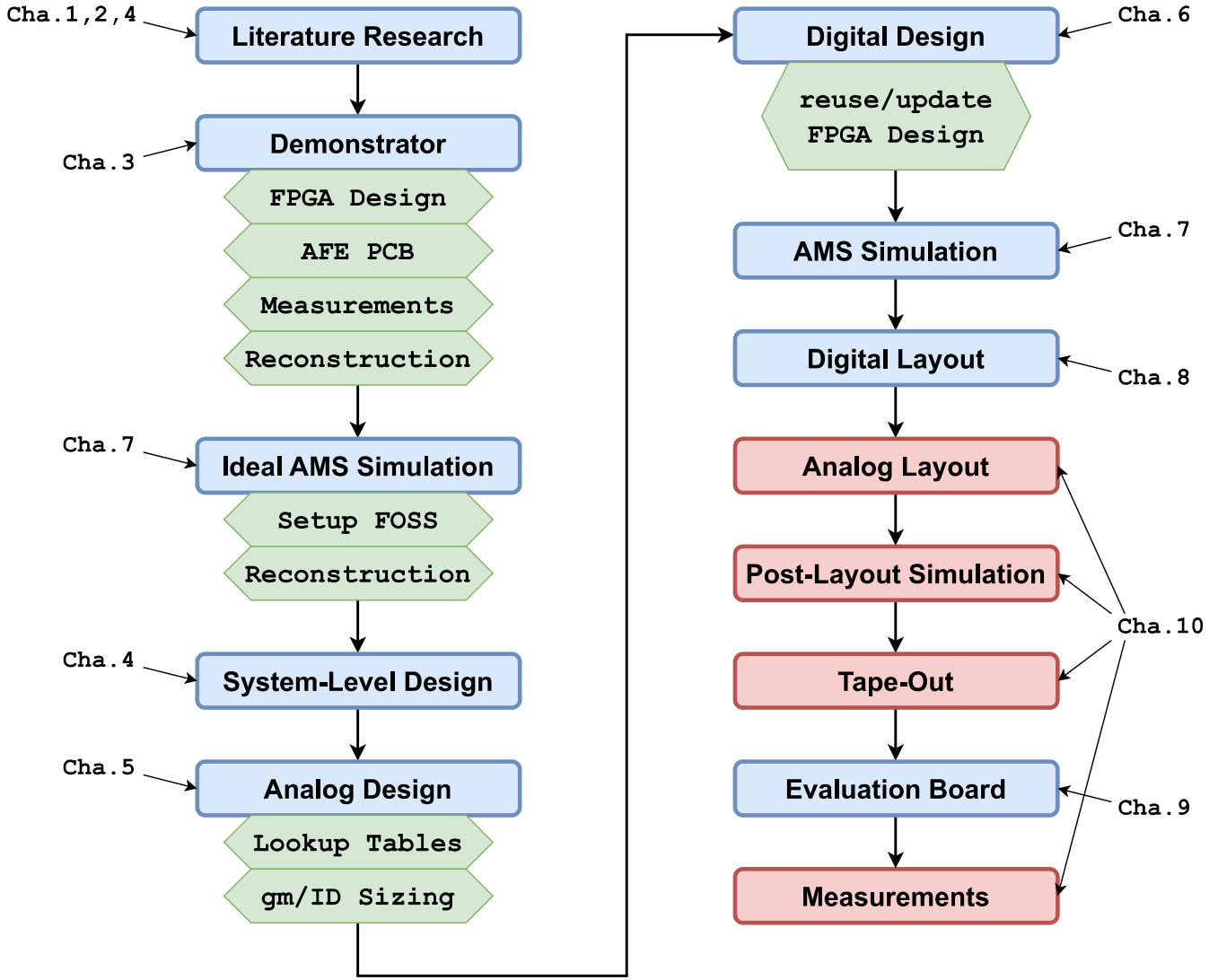
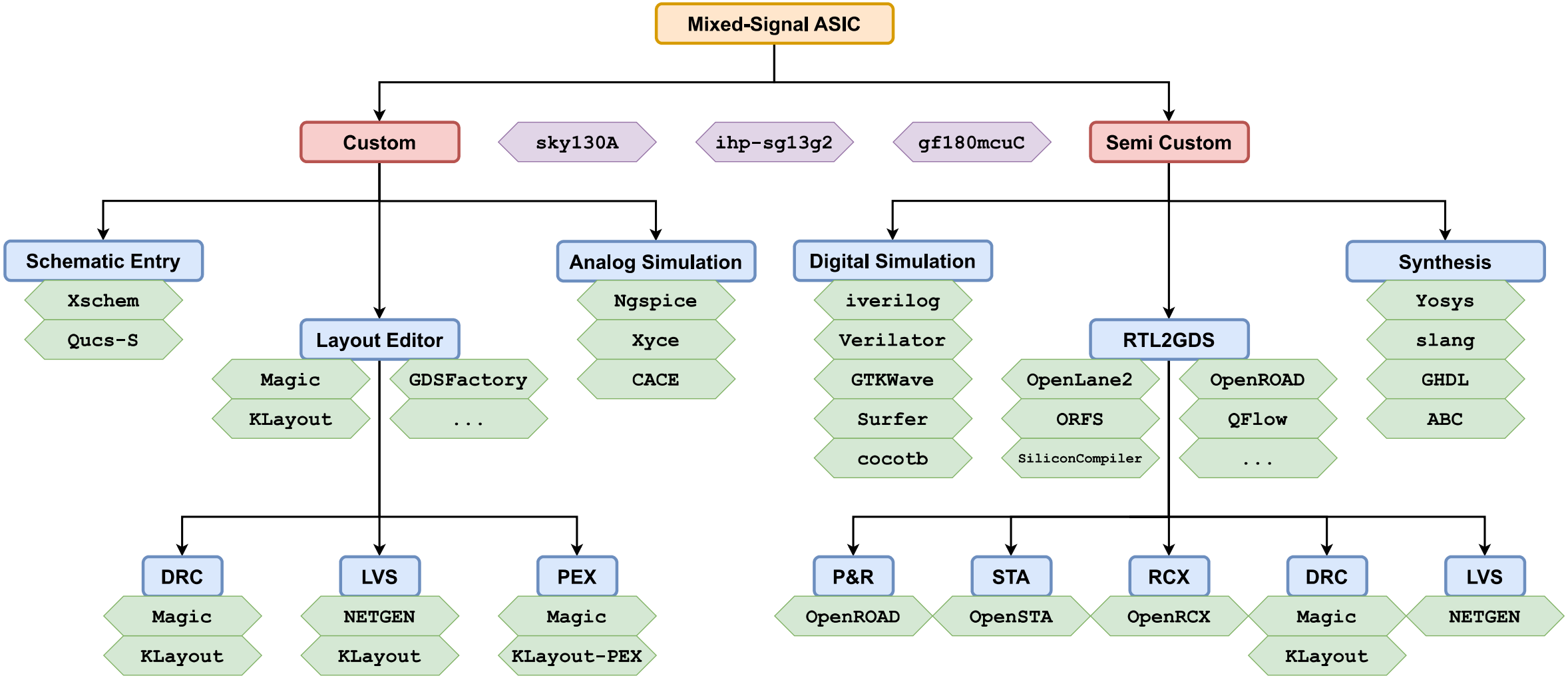
Thesis Organization



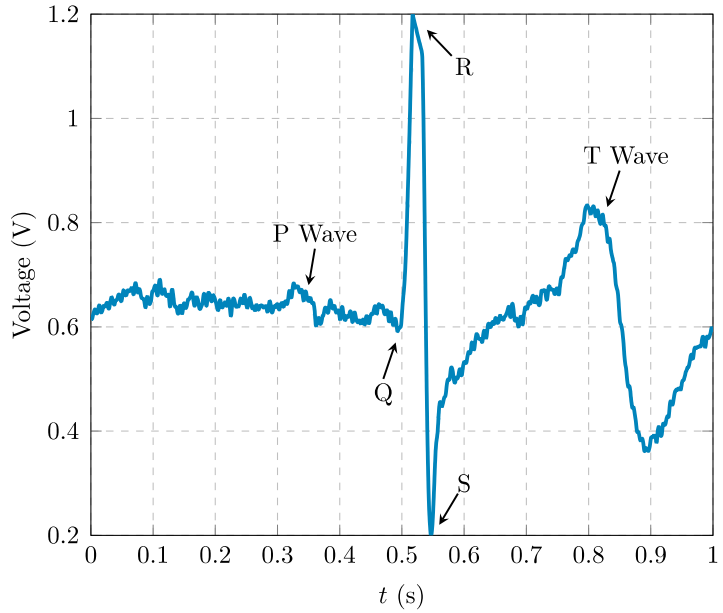
IIC-OSIC-TOOLS



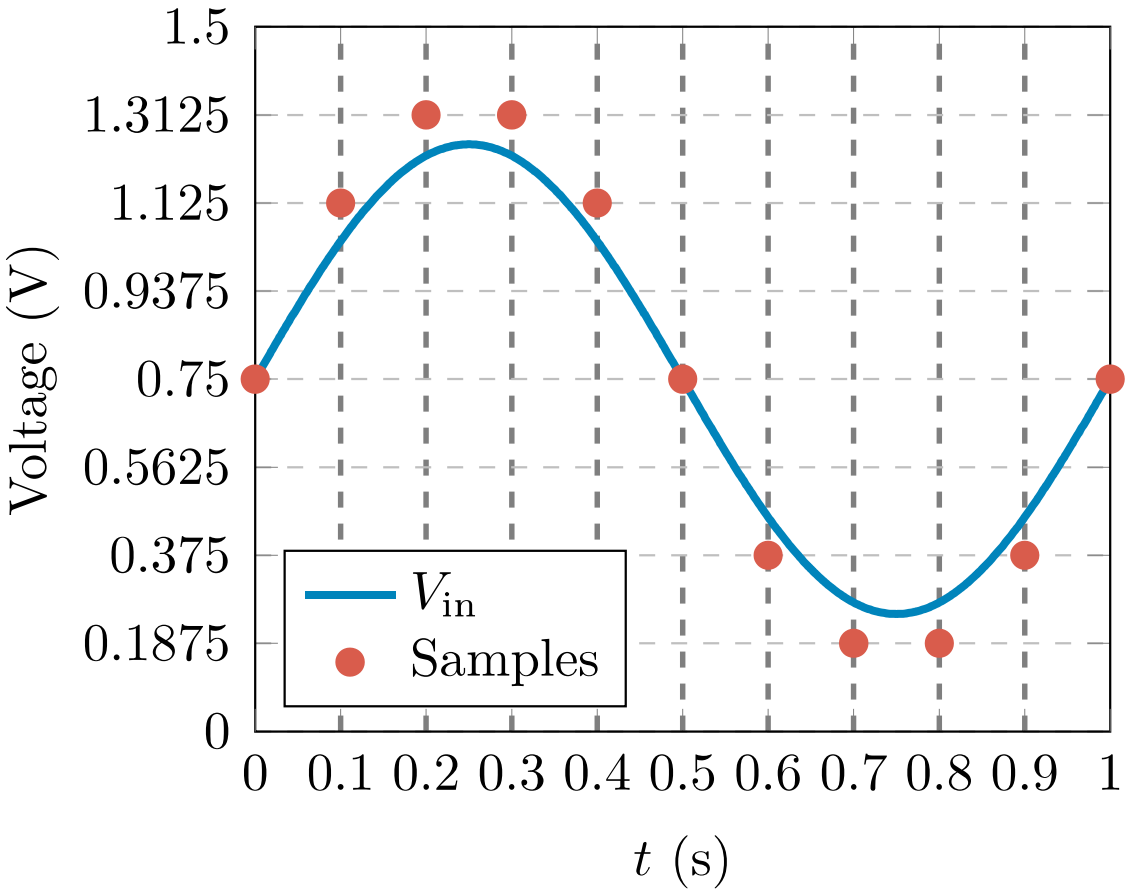
Theoretical Background

Nyquist vs. Event-Based ADC

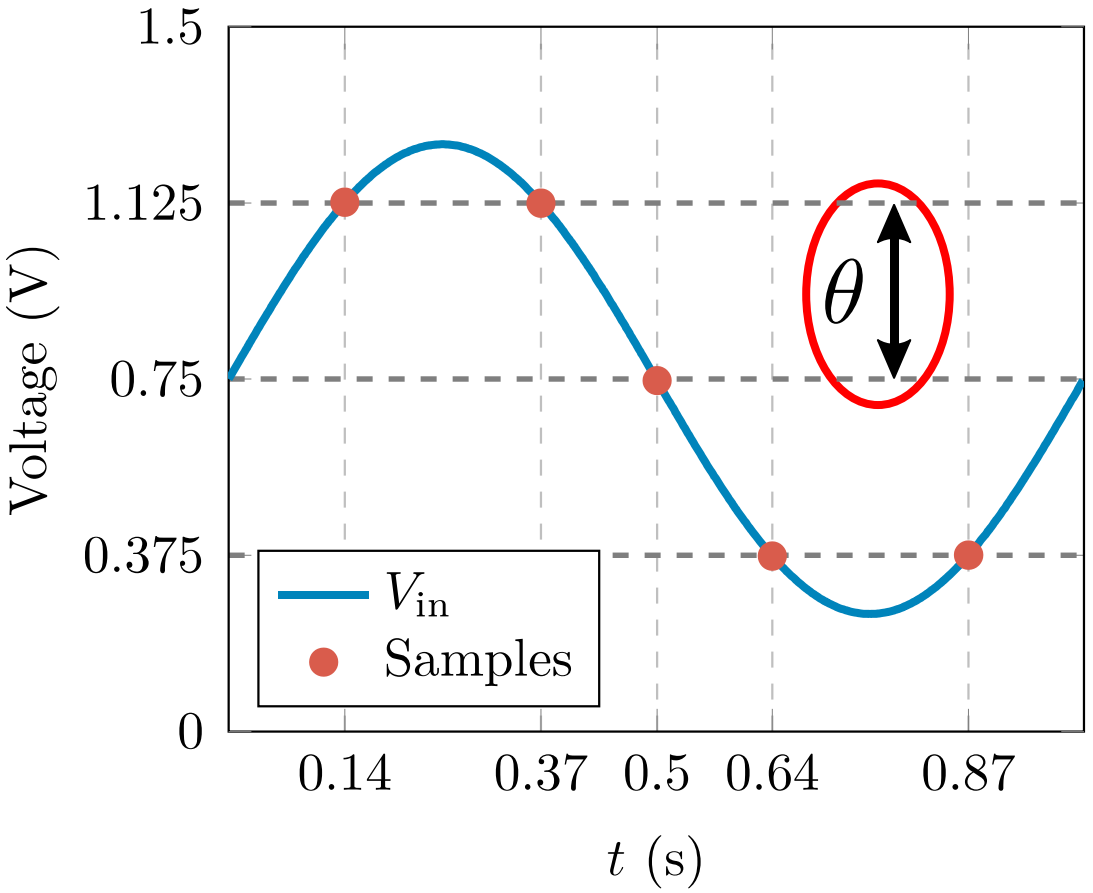
- Nyquist ADCs sample input at a fixed sample rate → uniform samples
- Voltage values are quantized and encoded → amplitude quantization
- Event-based ADCs only produce samples when input exceeds a predefined threshold θ → non-uniform event pulses (spikes)
- Time between spikes is measured and encoded → time quantization
- For sparse signals, event-based ADCs significantly decrease:
  - number of samples
  - storage resources
  - computational effort
  - power consumption



Nyquist vs. Event-Based ADC – Time Domain



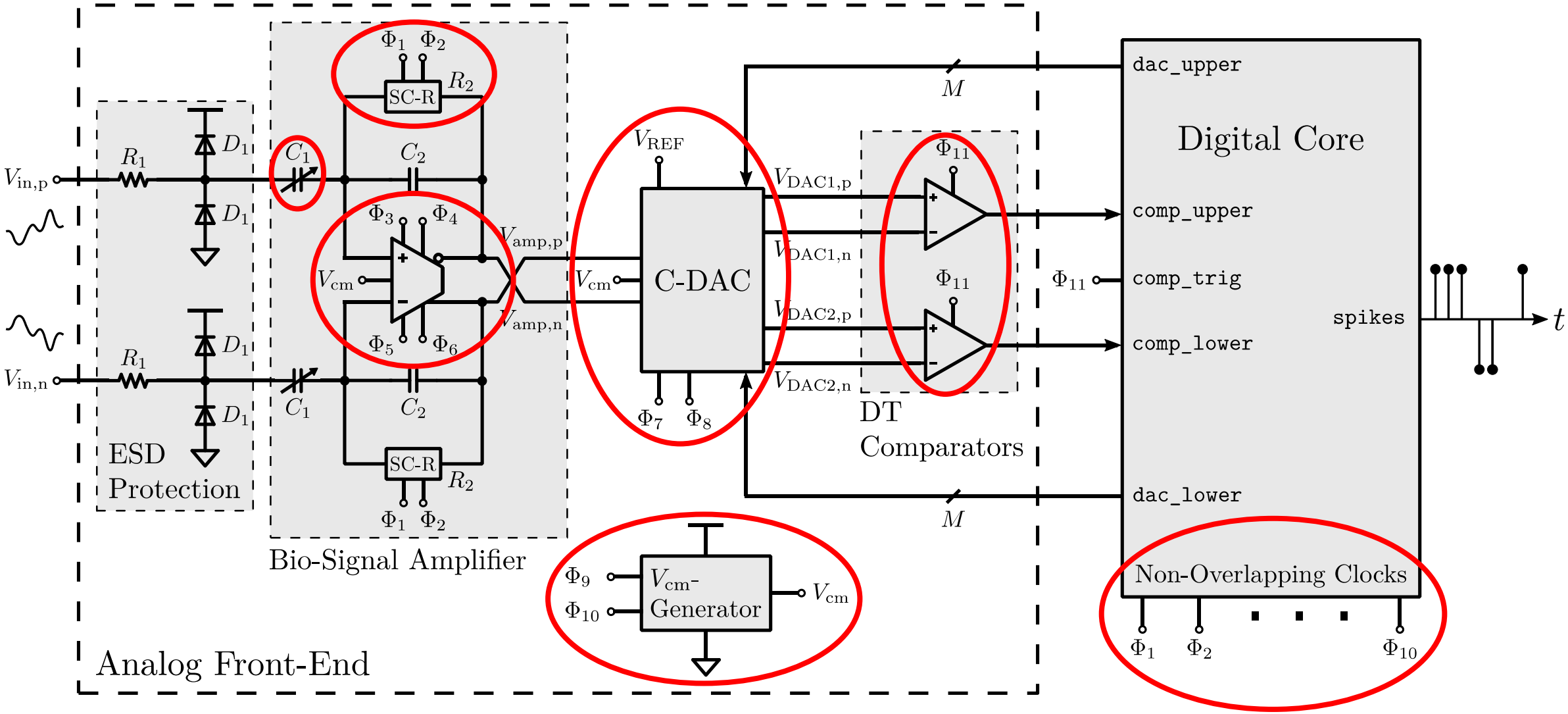
(a) Nyquist ADC



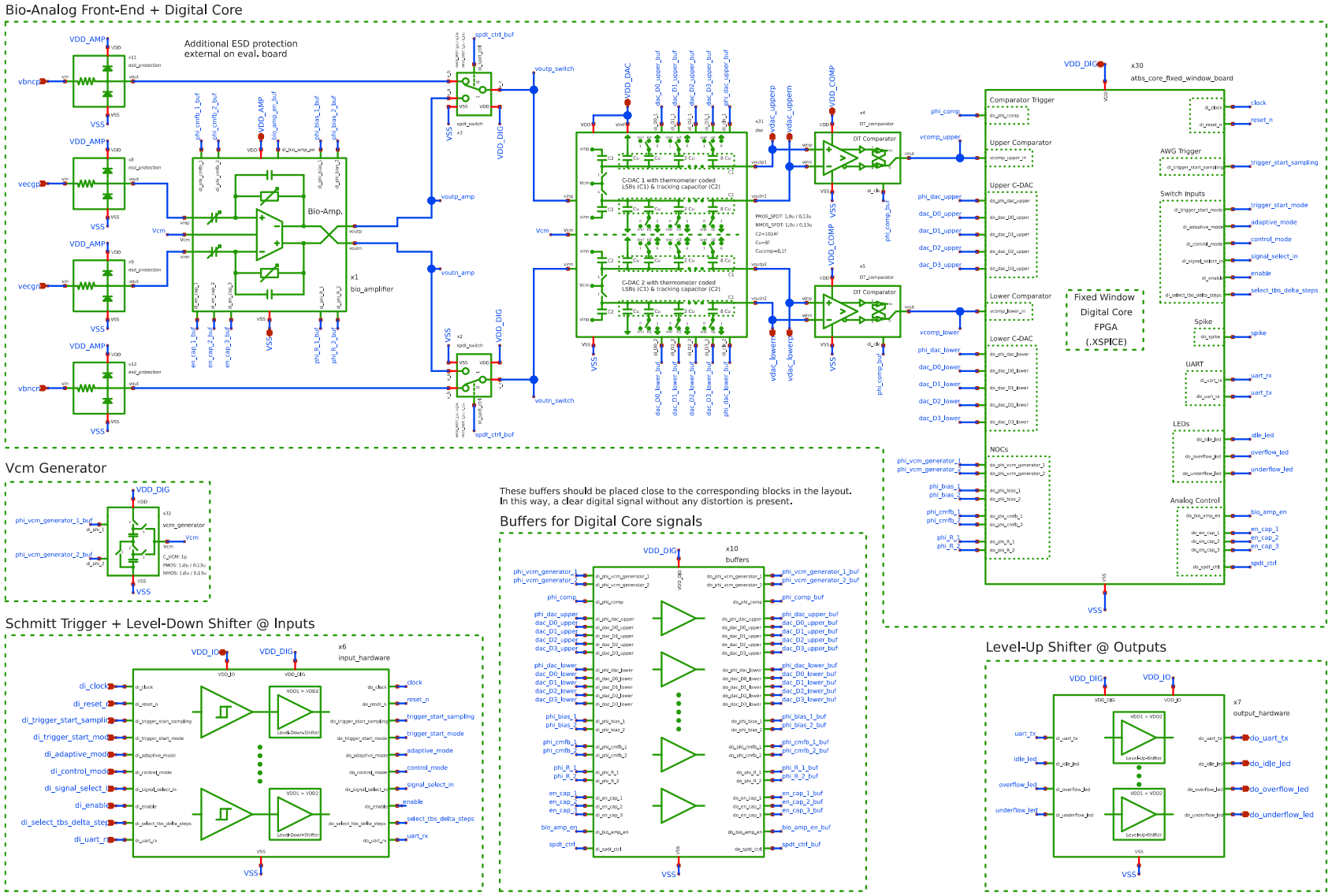
(b) Event-Based ADC

ASIC Design

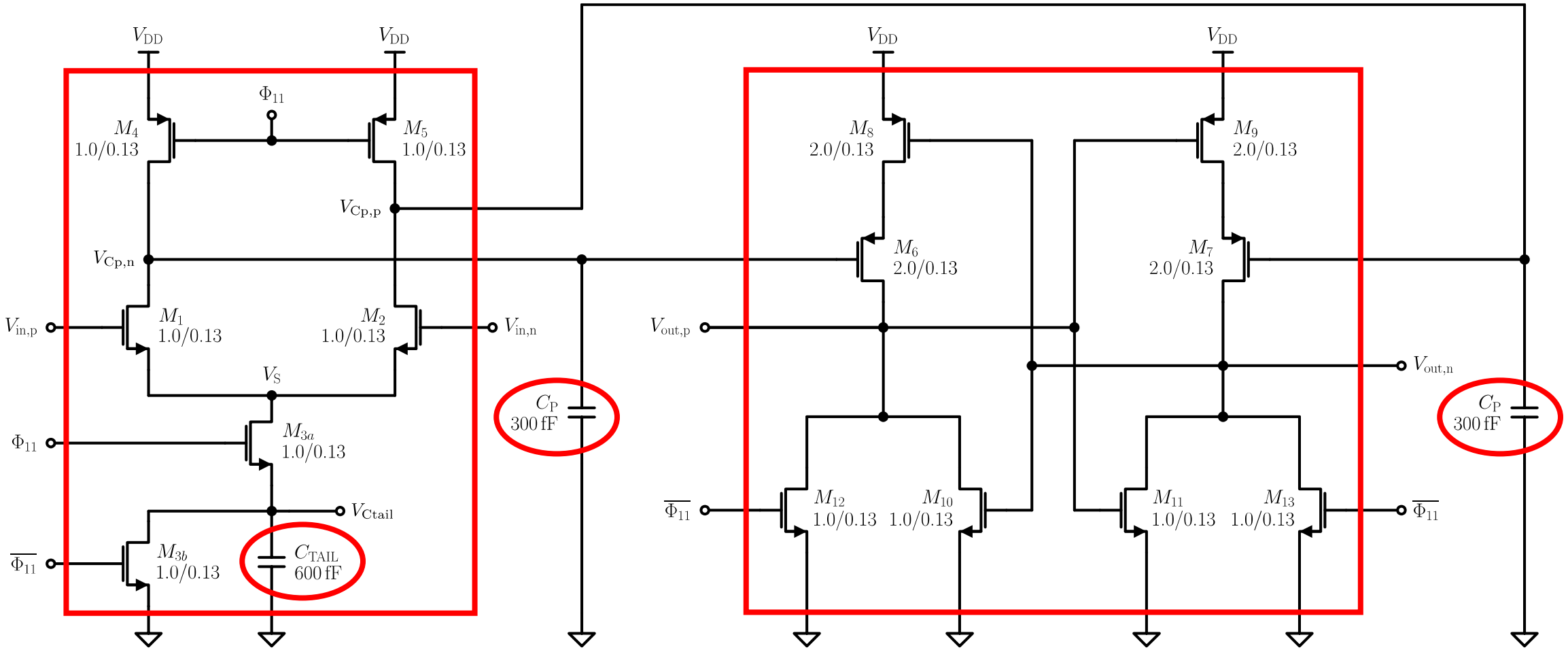
Block Diagram



Top-Level in Xschem

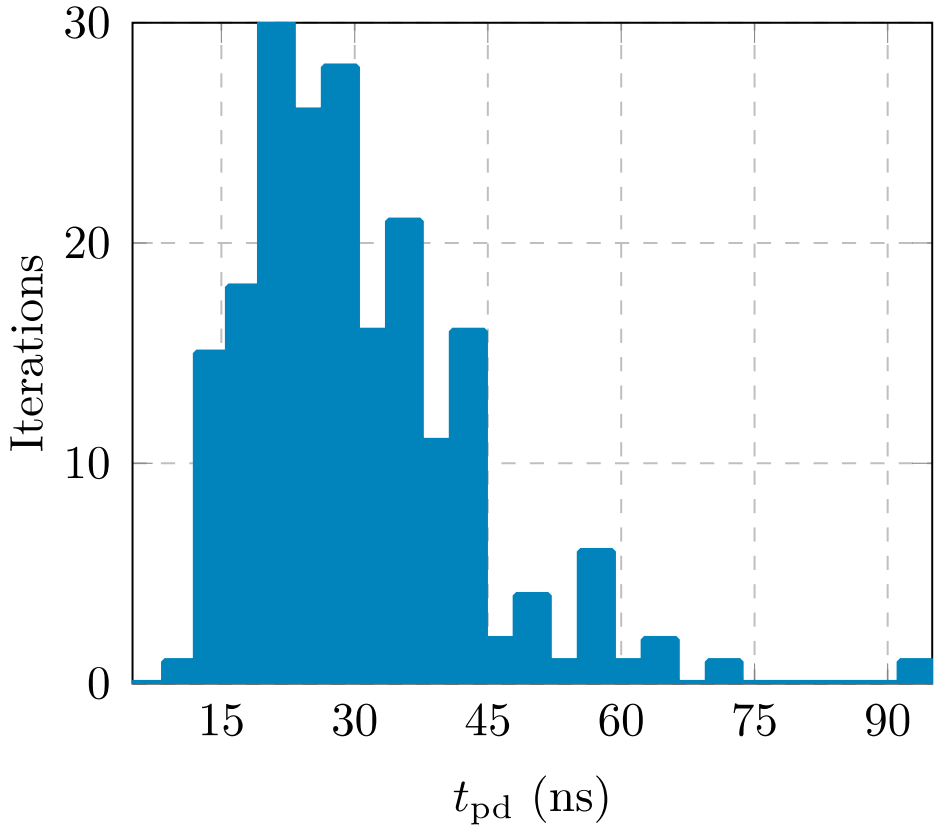


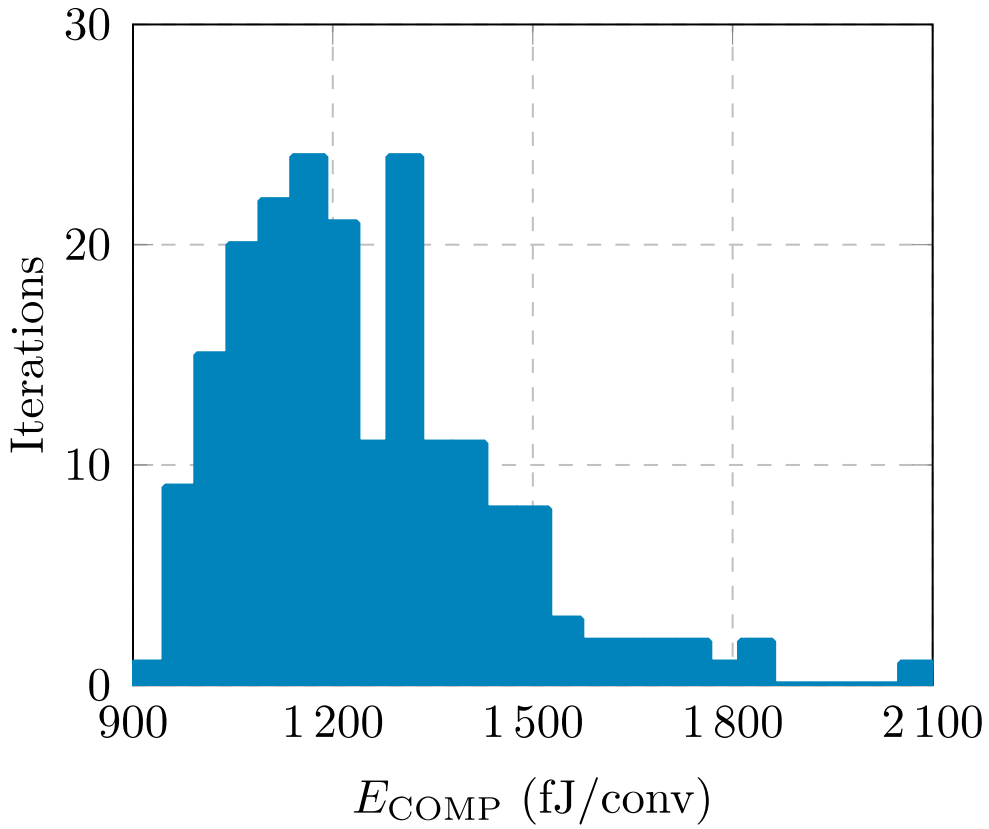
DT Comparator – Circuit



DT Comparator – MC Simulation

- Monte Carlo process variation simulation with CACE
- 200 iterations



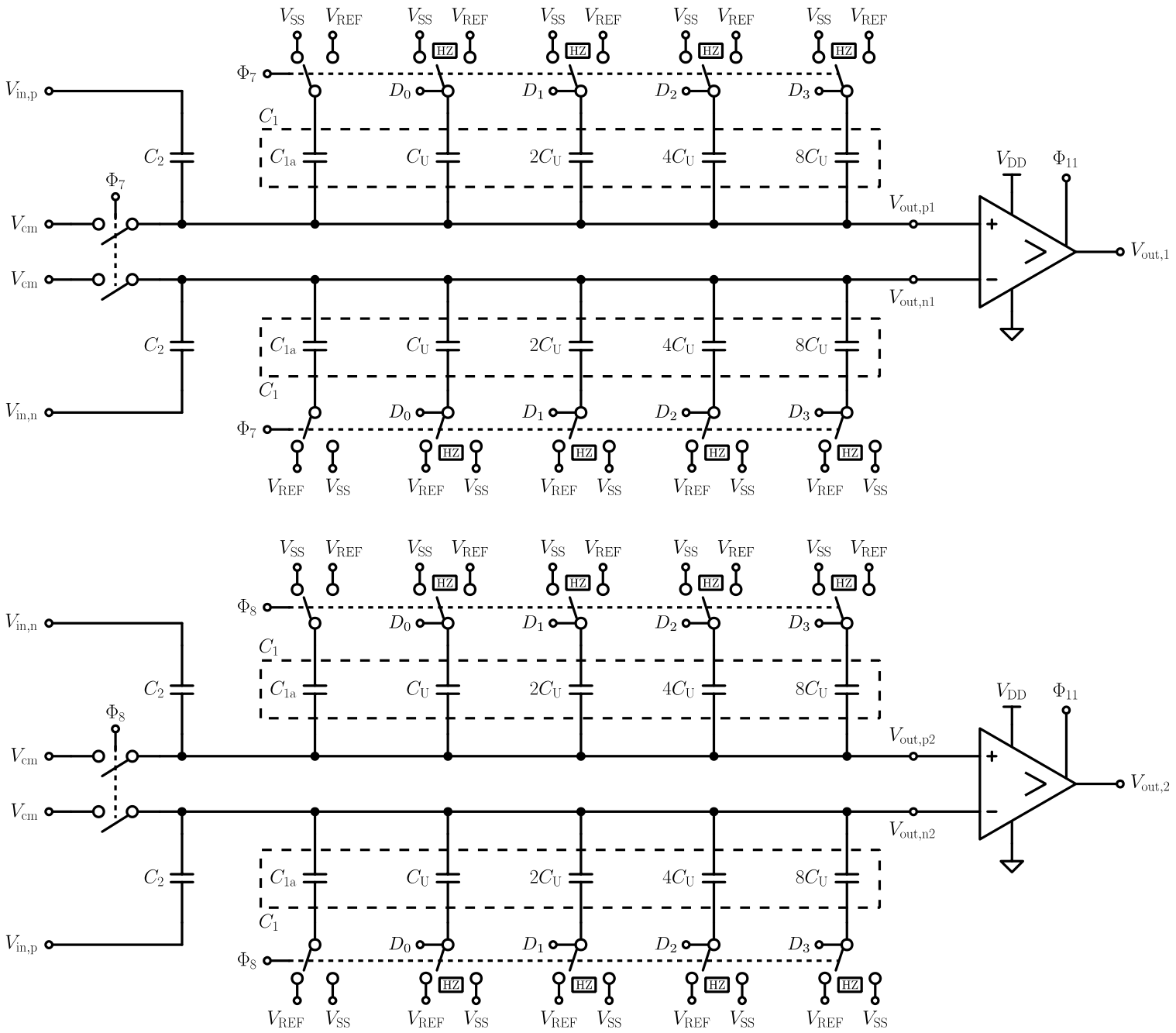


Capacitive DAC

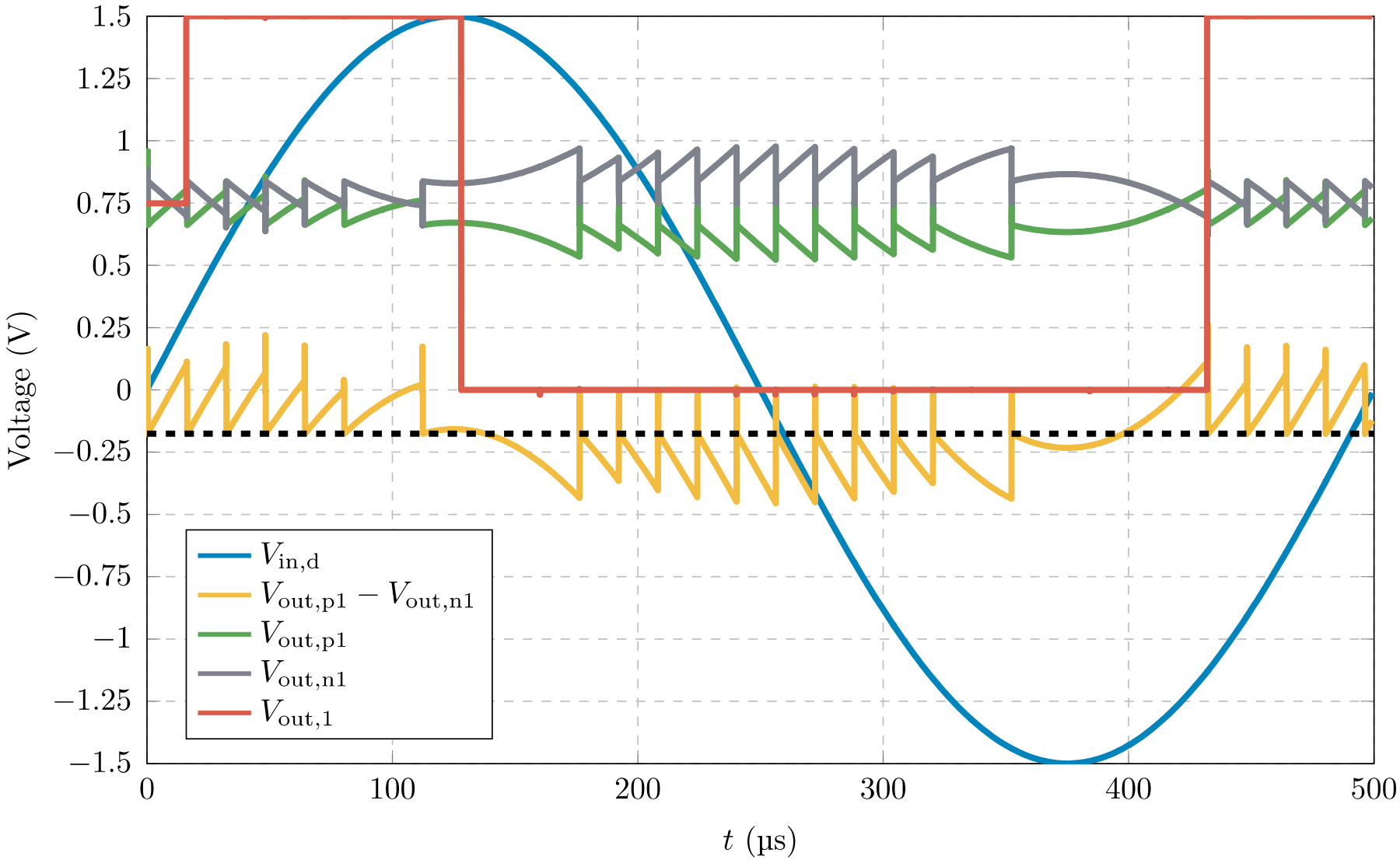
- Reset: $\Phi_7 = \Phi_8 = 1$
- Tracking: $\Phi_7 = \Phi_8 = 0$

$$C_1 = C_\mathrm{U} 2^{M-1}$$

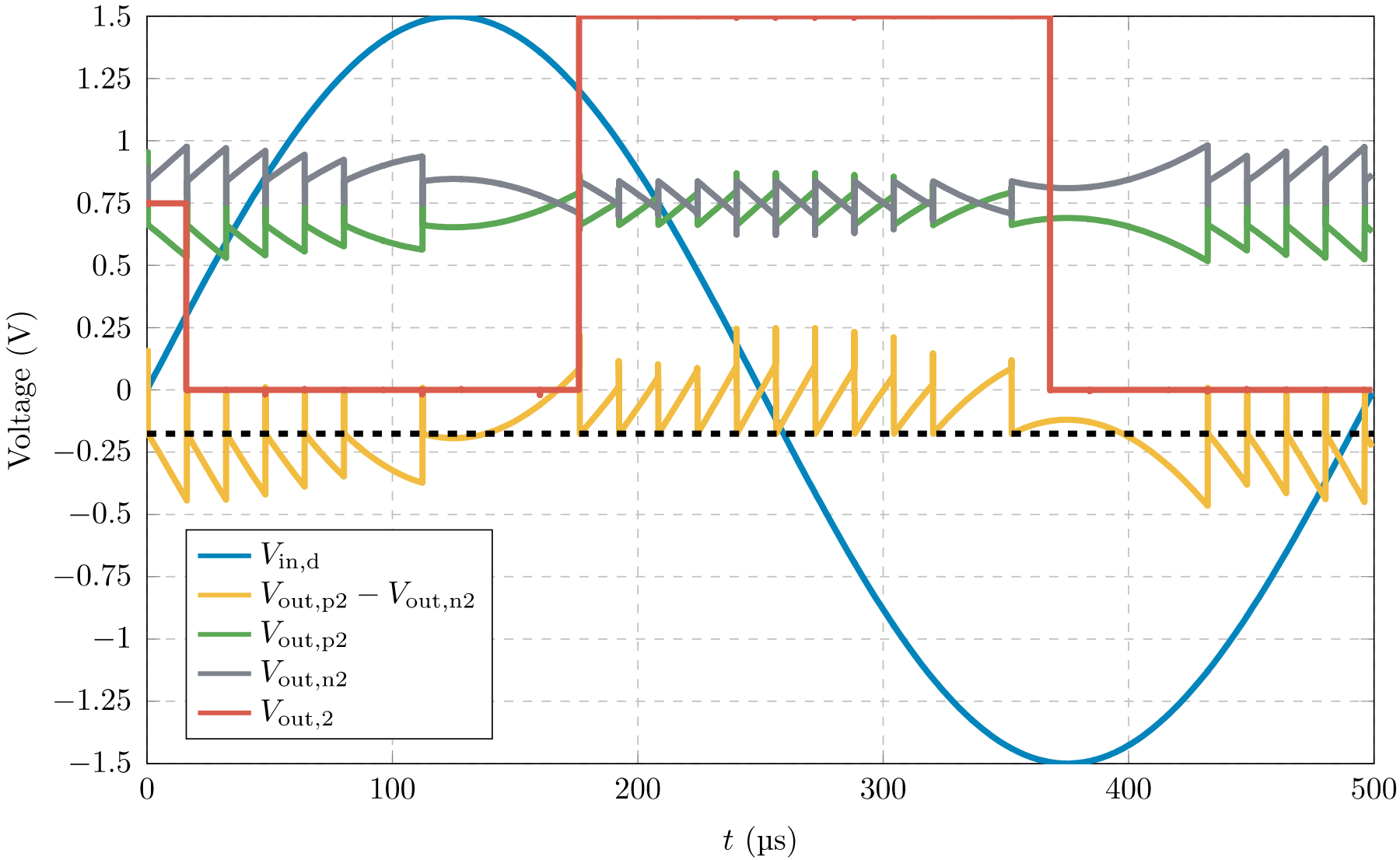
$$V_\mathrm{LSB} = 2\frac{C_1}{C_2} = 2\frac{C_\mathrm{U} 2^{M-1}}{C_2} = \frac{2V_\mathrm{DD}}{2^F}$$



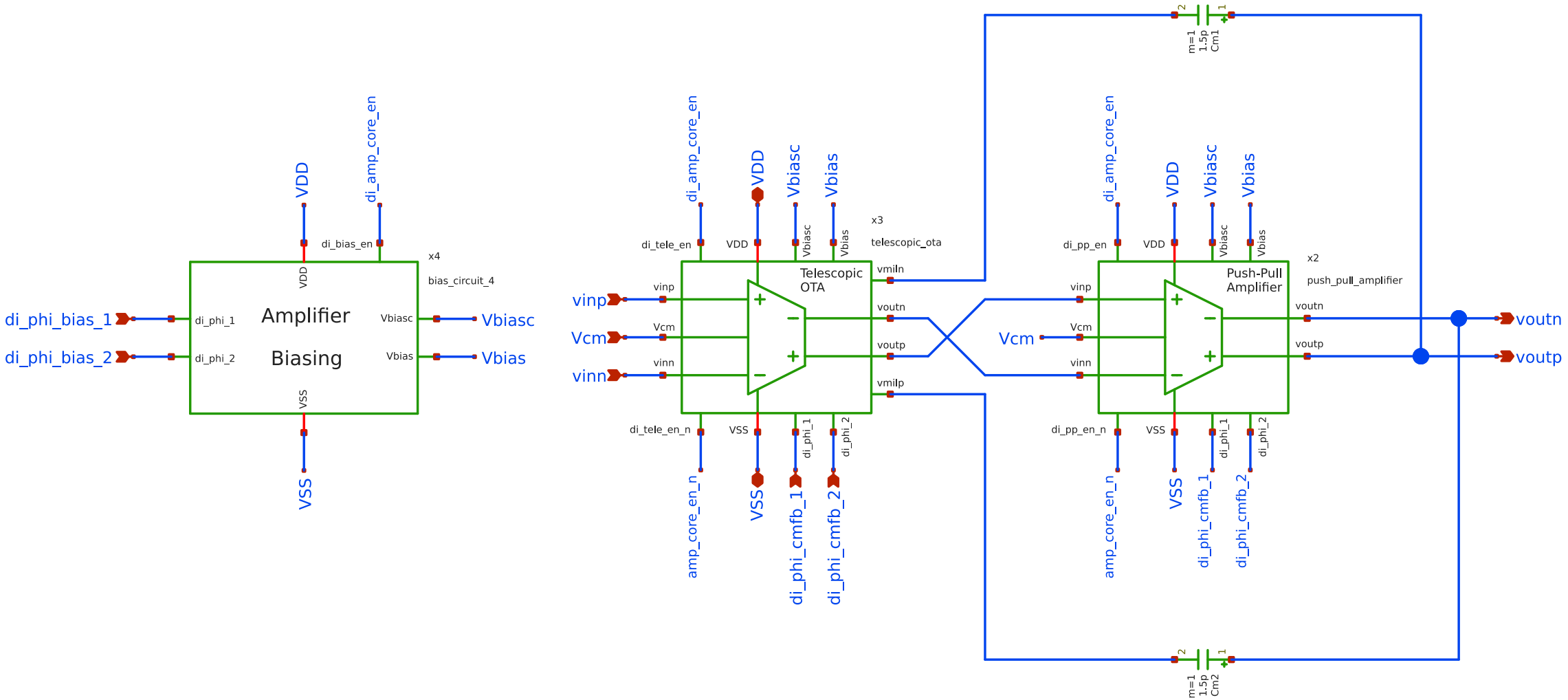
Upper DAC + Comparator – Transient Simulation



Lower DAC + Comparator – Transient Simulation



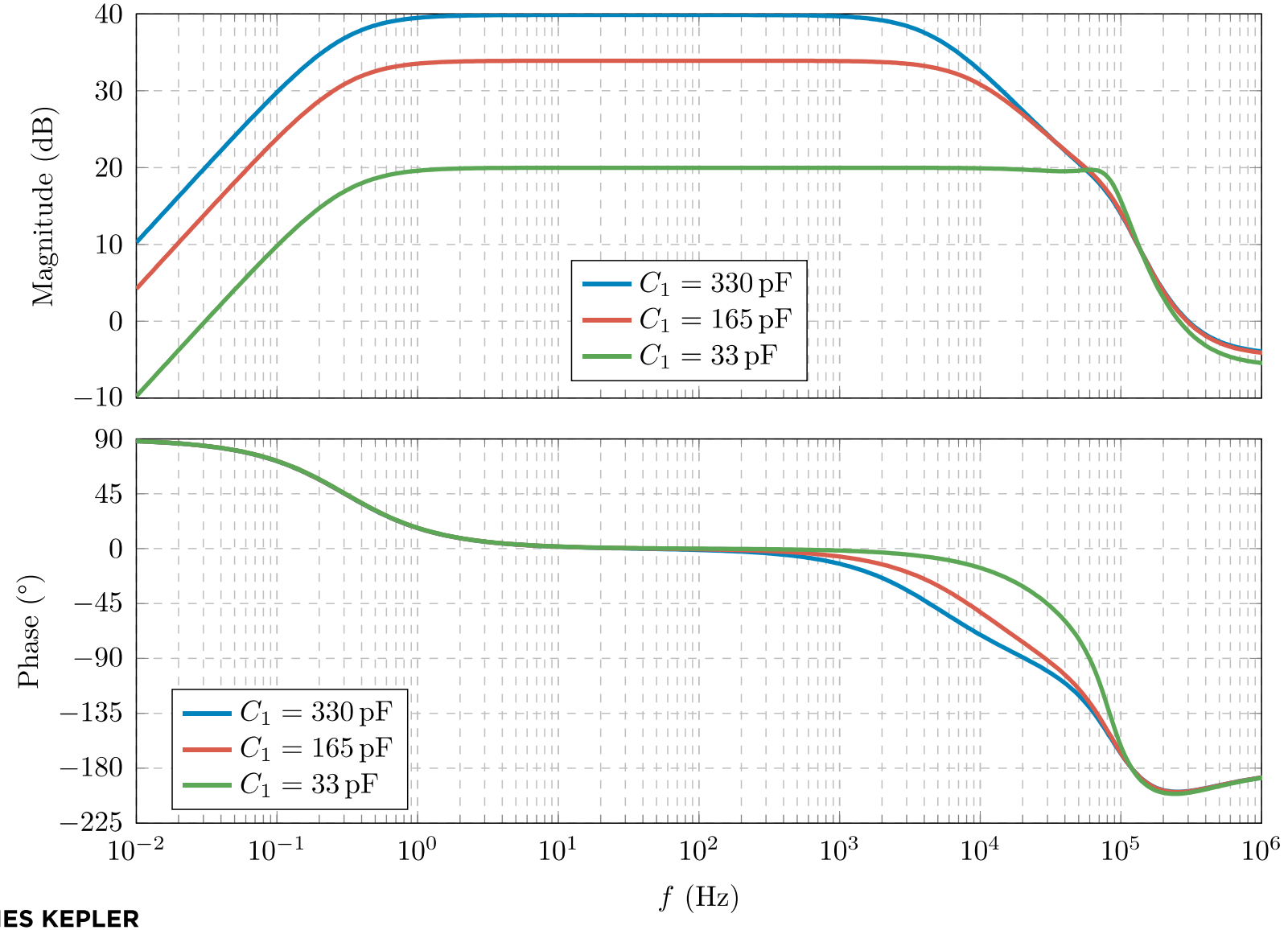
Amplifier Core in Xschem



Testbenches in Xschem

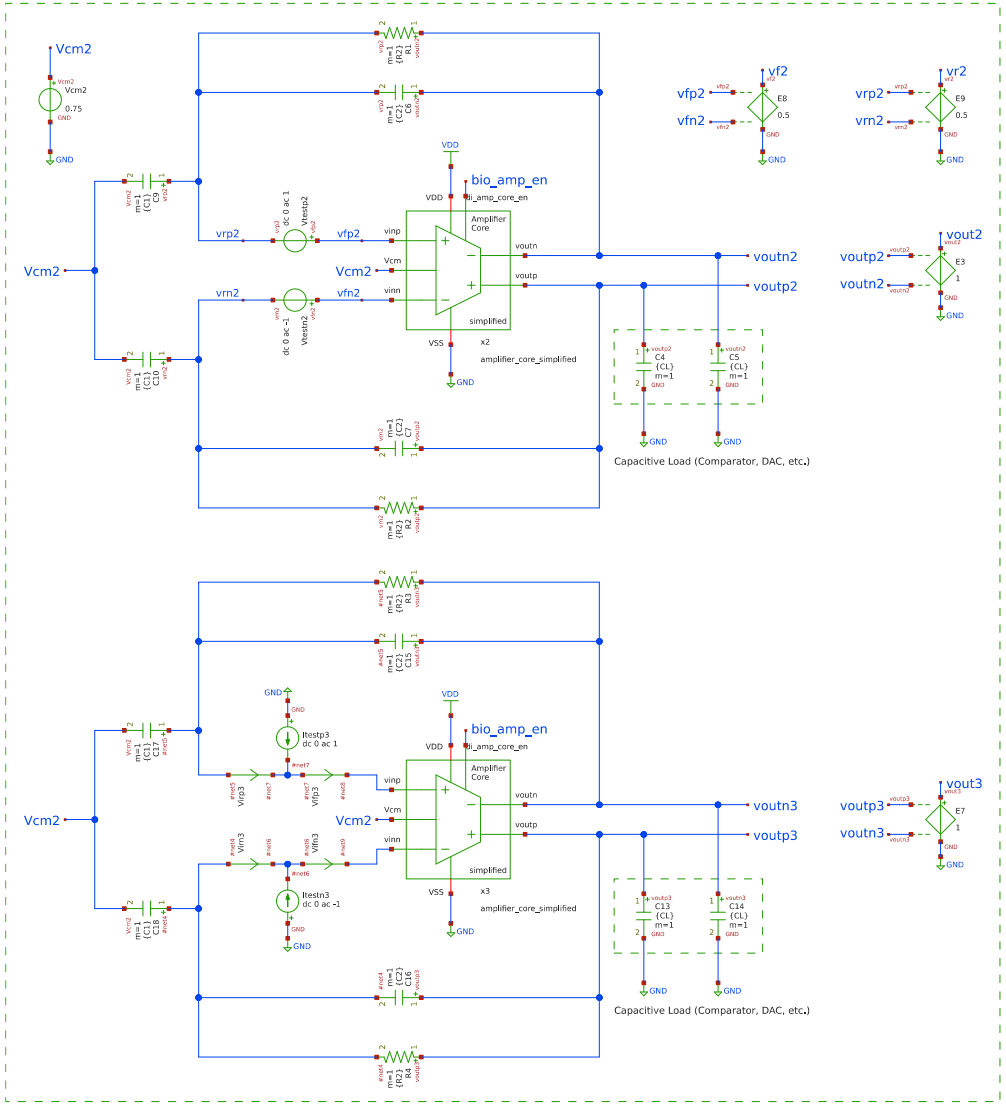
- Different testbenches are available for:
  - Open-loop gain
  - Closed-loop gain
  - Loop gain
  - Common-Mode Rejection Ratio (CMRR)
  - Power-Supply Rejection Ratio (PSRR)
  - Input impedance
- Problem with switched-capacitor circuits:
  - No periodic AC analysis → long looped transient analysis
  - Temporarily swapped with idealized resistors

Simulation Results – Closed-Loop Gain

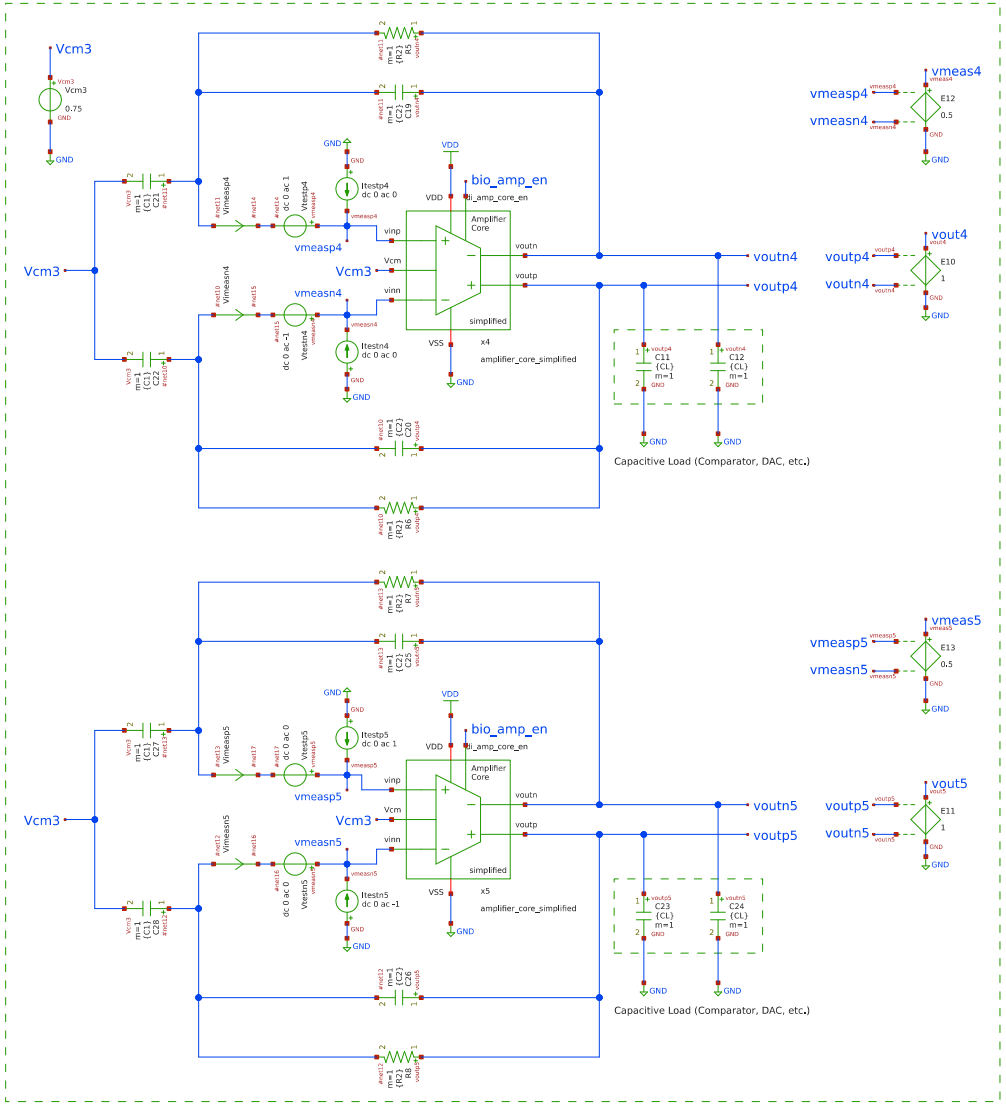


Fully-Differential OTA – Loop Gain Simulation

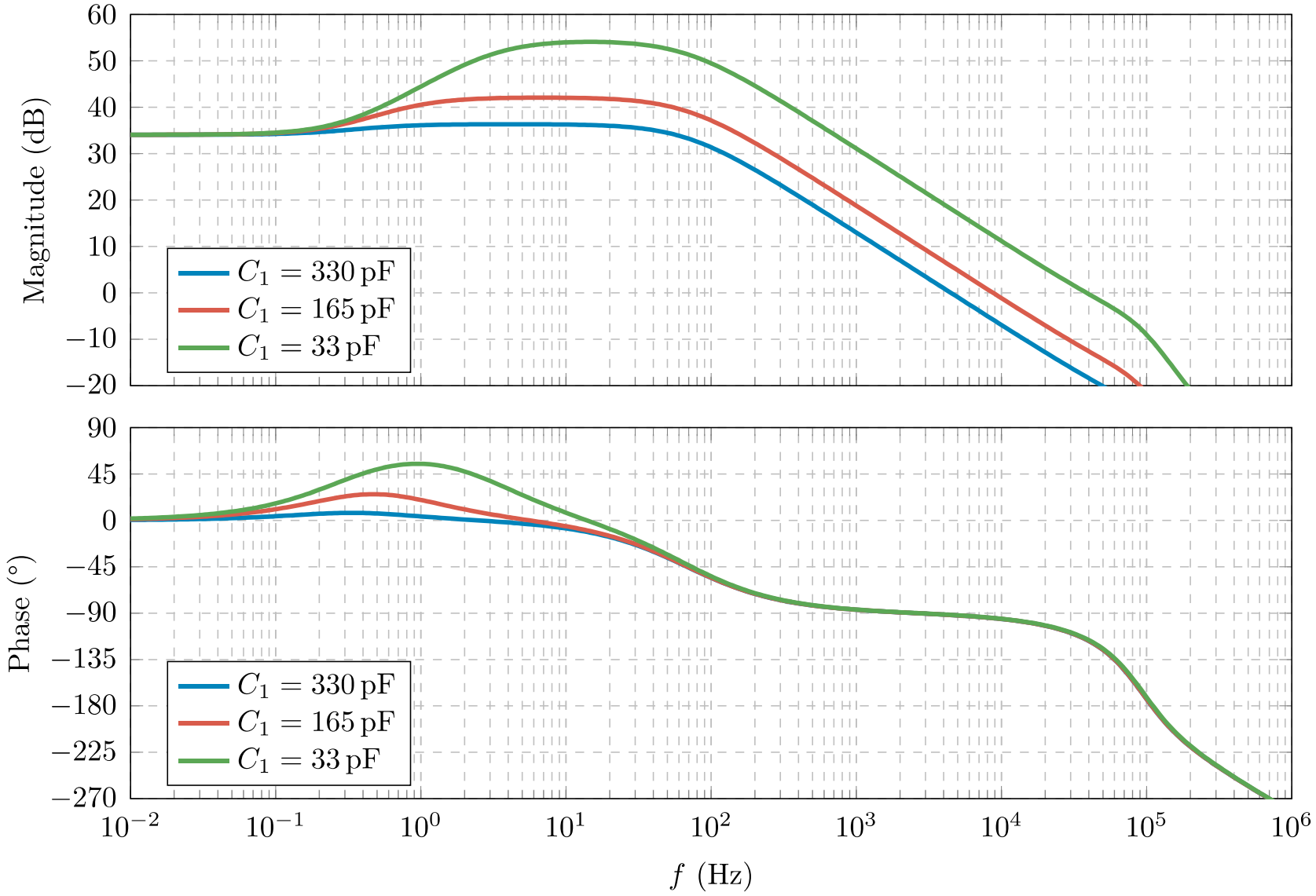
Middlebrook's Method



Tian's Method



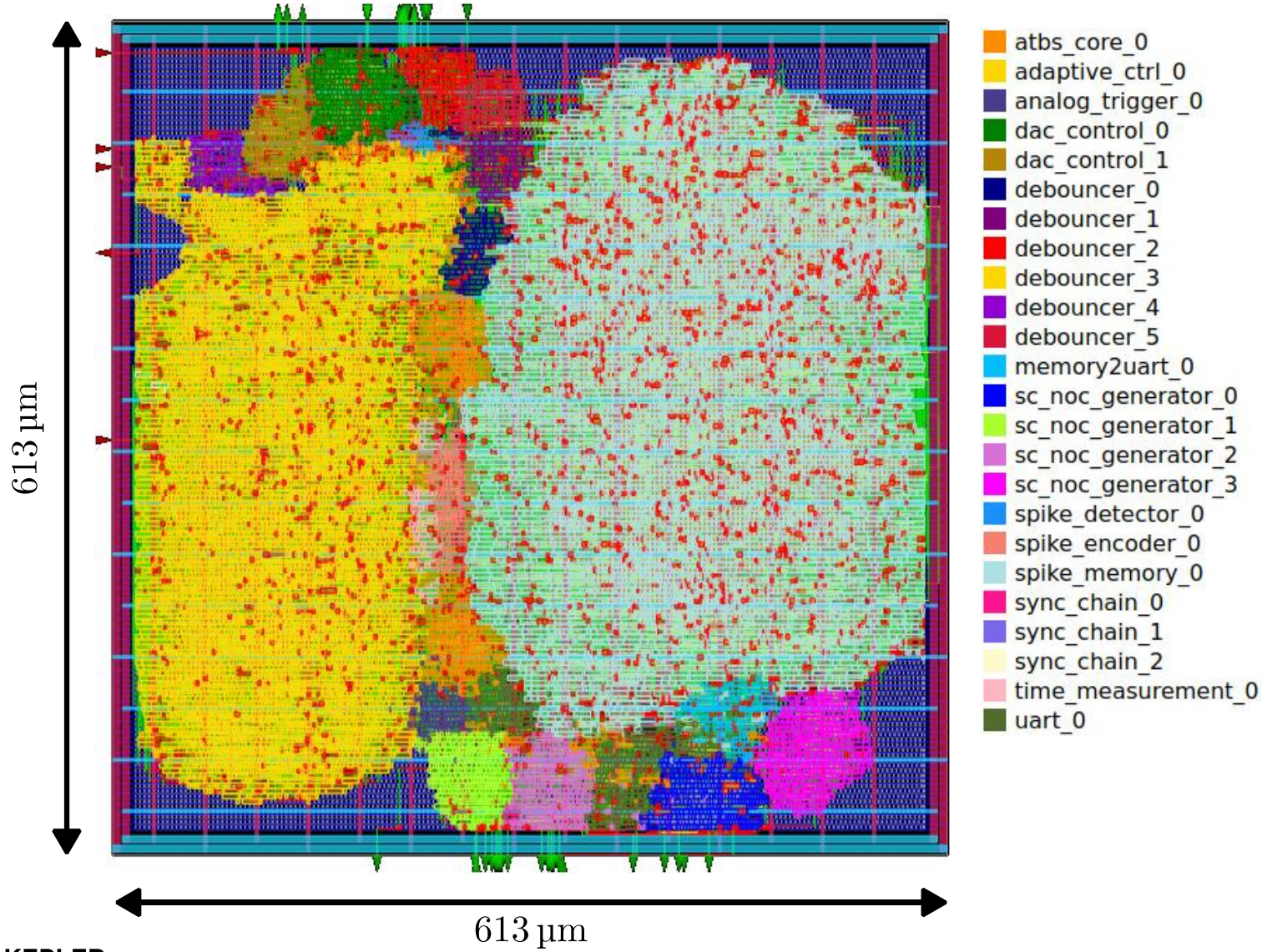
Simulation Results – Loop Gain



Gate-level Analog Mixed-Signal Simulation

- Gate-level synthesized digital design included in Xschem
- VHDL to Verilog with GHDL / Yosys
- Verilog to Xspice
  - QFlow scripts: vlog2Verilog, vlog2Spice and spi2xspice.py
  - Timing information
  - Decision levels
- Template & step-by-step instruction for SG13G2 and IIC-OSIC-TOOLS: https://github.com/simi1505/SG13G2_ASIC-Design-Template
- Also supports layout generation with OpenROAD Flow Scripts (ORFS)

Digital Core – OpenROAD GUI



Conclusion

Conclusion

- Achievements:
  - Important theoretical findings
  - Development of new architecture
  - Transistor-level design
  - Set up of gate-level analog mixed-signal simulation
- Outlook:
  - Analog layout
  - Post-layout simulation
  - Tape-out
  - Chip verification with measurements

Resources

- Analog Circuit Design Course @ JKU:

  https://github.com/iic-jku/analog-circuit-design

- GitHub Repository (Event-Based ADC):

  https://github.com/iic-jku/SG13G2_ATBS-ADC

- GitHub Repository (SG13G2 ASIC Design Template):

  https://github.com/simi1505/SG13G2_ASIC-Design-Template

- Master Thesis:

  https://epub.jku.at/obvulihs/content/titleinfo/12118473?query=dorrer

- YouTube Video: coming soon!

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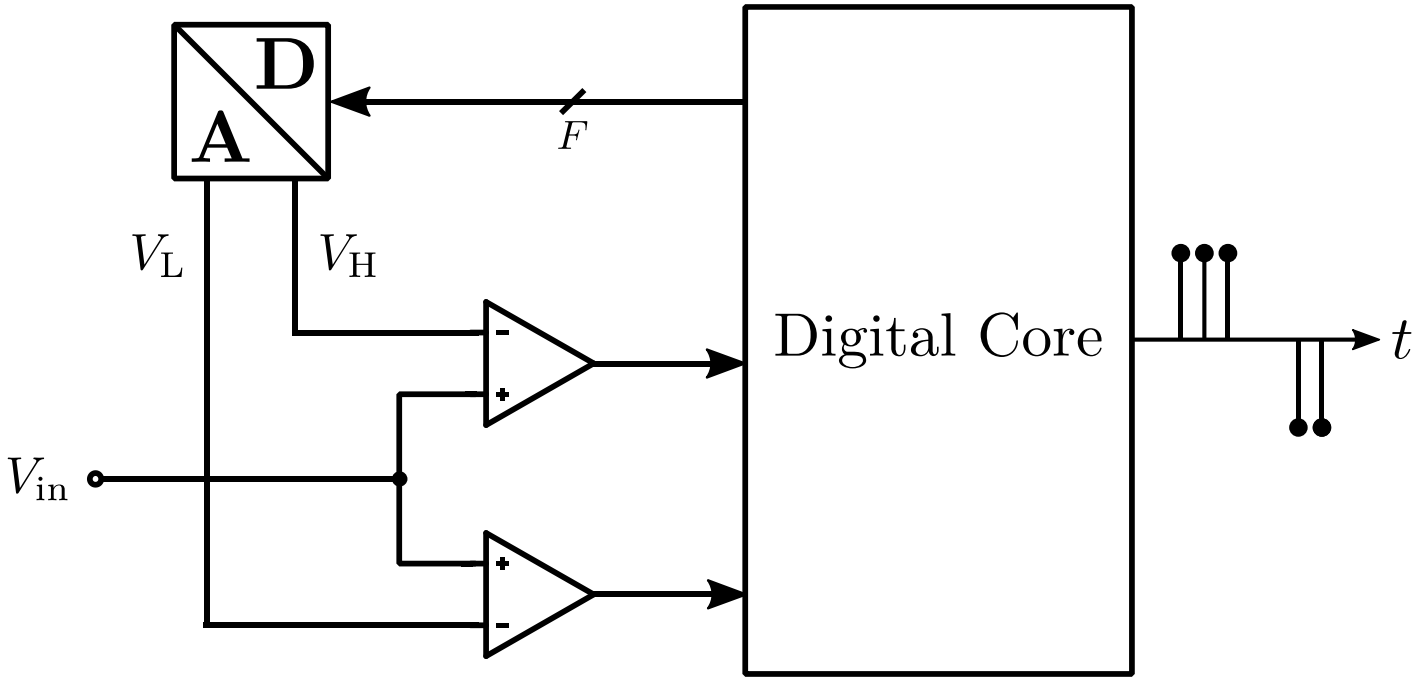
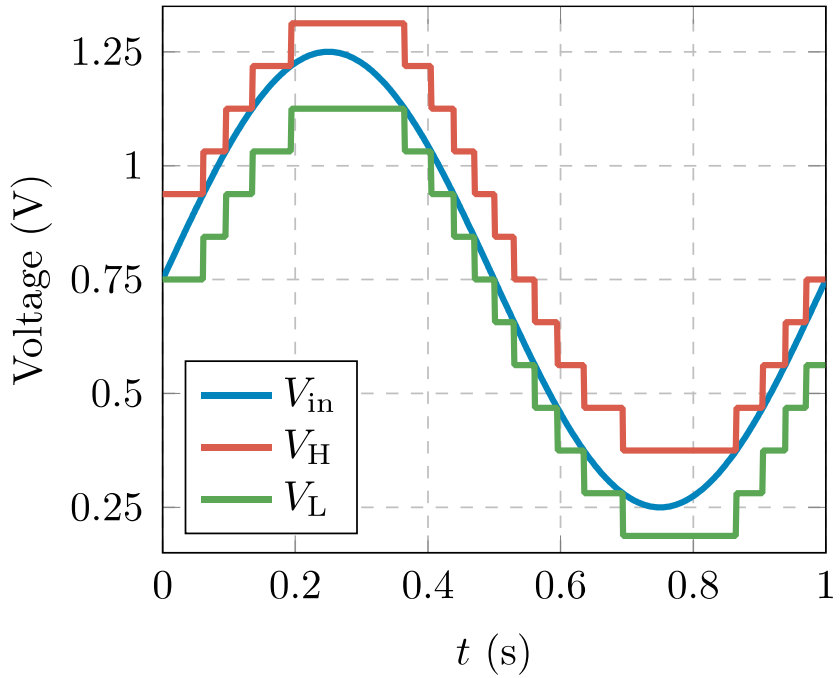
Applications for Event-Based ADCs

- Bio-signal acquisition with battery-powered, wireless, and wearable devices such as:
  - Fitness trackers
  - Emergency medical sensors
  - Internet of Things (IoT) devices

Floating-Window Architecture

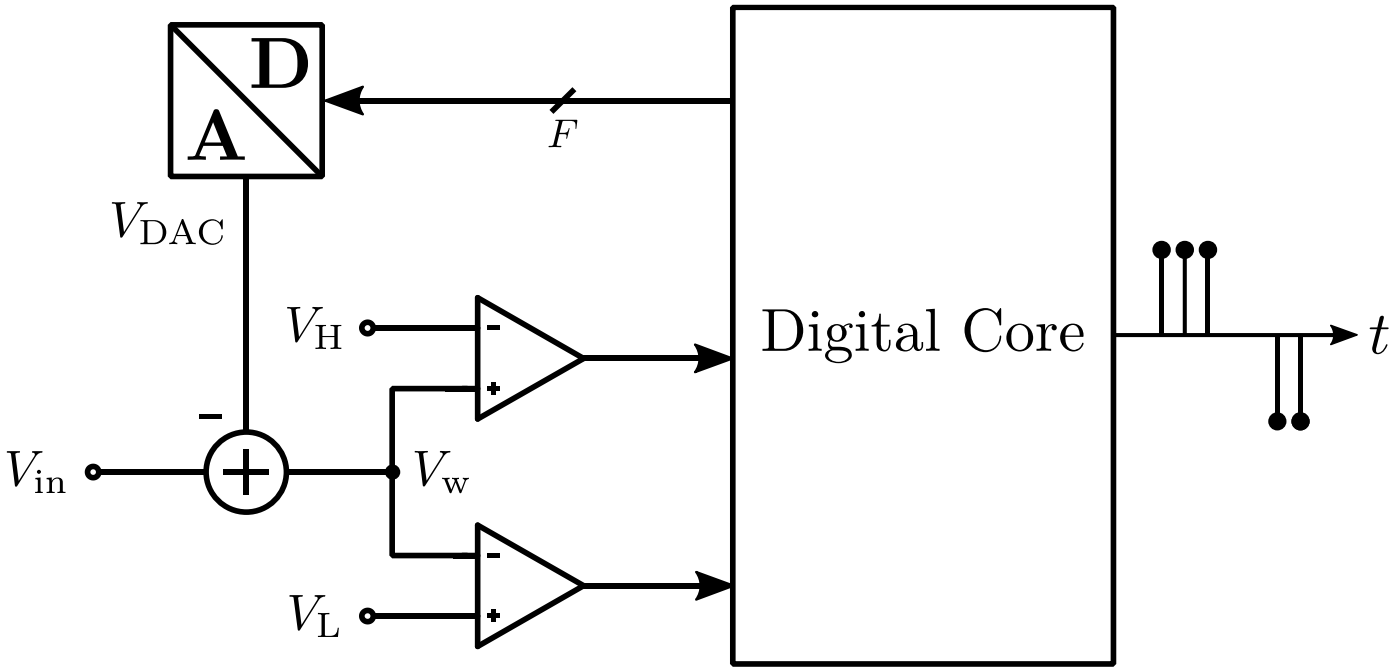
- If $V_{\text{in}} > V_{\text{H}}$, the upper comparator outputs a logic one, and both DAC voltages shift up by θ and vice versa for $V_{\text{in}} < V_{\text{L}}$.

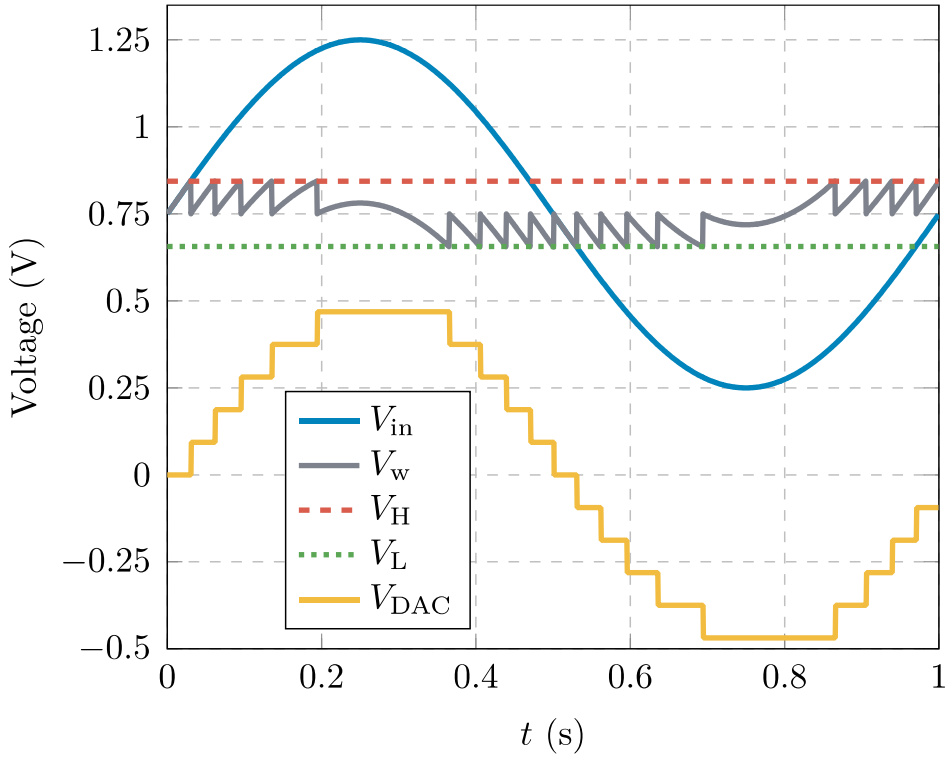




Fixed-Window Architecture

- V_{in} is wrapped within V_{H} and V_{L} whenever a threshold crossing occurs, by subtracting the current DAC voltage from V_{in}.





Nyquist vs. Event-Based ADC – Aliasing

- Nyquist ADC: The sampling limit induced by aliasing is defined by the Shannon-Nyquist theorem:

$$f_s > 2f_{\max}$$

- Event-based ADC: The aliasing effect is caused by their slew rate:

$$\mathrm{SR} = \max \left| \frac{\mathrm{d}V_{\mathrm{in}}(t)}{\mathrm{d}t} \right| < \frac{\theta}{t_{\mathrm{loop}}} = \frac{V_{\mathrm{REF}}/2^F}{t_{\mathrm{loop}}}$$

$$t_{\mathrm{loop}} = t_{\mathrm{pd}} + t_{\mathrm{core}} + t_{\mathrm{settle}}$$

- The maximum frequency for sine waves ($\mathrm{SR} = 2\pi A f_{\max}$) for event-based ADCs with fixed thresholds can be expressed as:

$$f_{\max} = \frac{V_{\mathrm{REF}}}{2\pi t_{\mathrm{loop}} A_{\max} 2^F}$$

Nyquist vs. Event-Based ADC – SQNR

- Nyquist ADC: The time- and frequency-domain SQNR for a full-scale amplitude sine wave, resulting from uniformly distributed amplitude quantization, depends on the ADC resolution (N):

$$\mathrm{SQNR} = 6.02N + 1.76$$

- Event-based ADCs: The SQNR, resulting from time quantization, depends on the clock resolution (T_{clk}) and the input signal's frequency (f_{sig}):

$$\mathrm{SQNR} = 20\log_{10}(R) - 14.2$$

where R is the resolution or oversampling ratio:

$$R = \frac{1}{f_{\mathrm{sig}} T_{\mathrm{clk}}} = \frac{f_{\mathrm{clk}}}{f_{\mathrm{sig}}}$$

- Event-based ADCs can achieve an SQNR equivalent to that of an N-bit Nyquist ADC while requiring only a DAC with fewer than N bits ($F < N$).

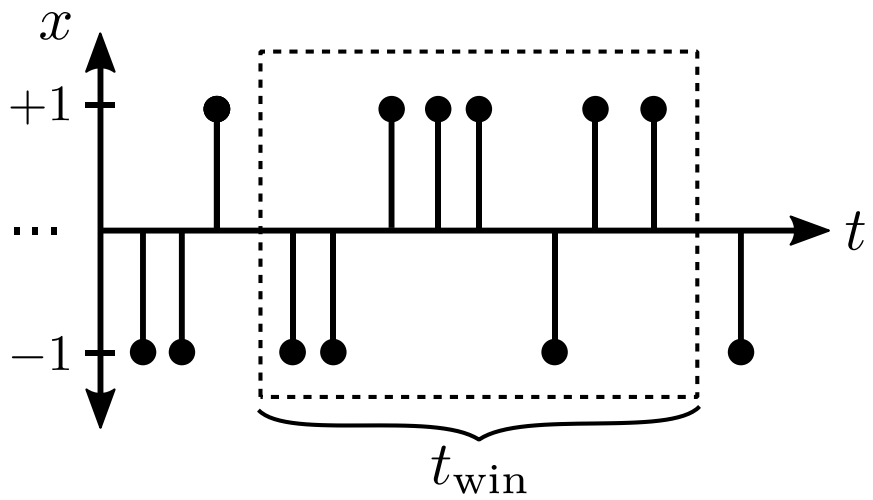
Continuous-Time vs. Discrete-Time

- Continuous-time (CT) system:
  - CT comparator, CT DAC, and asynchronous or clockless digital core
  - Minimize clock uncertainty and loop delay
  - Ideally, no amplitude and no time quantization and no aliasing!
  - Limited by high power consumption and nonidealities of AFE
- Discrete-time (DT) system:
  - Trigger AFE periodically or adaptively
  - Reduction of power consumption
  - Introduction of clock uncertainty and limiting the slew rate to:

$$T_{\mathrm{trig}} \geq (t_{\mathrm{pd}} + t_{\mathrm{core}} + t_{\mathrm{settle}}) = t_{\mathrm{loop}}$$

Adaptive Threshold-Based Sampling

- Input signal dependent adaption of threshold θ
- Reduce number of samples
- Increase maximum slew rate
- Calculation of Weyl's discrepancy within a defined time window



- If the discrepancy is larger / lower than a certain value, θ is doubled / halved.

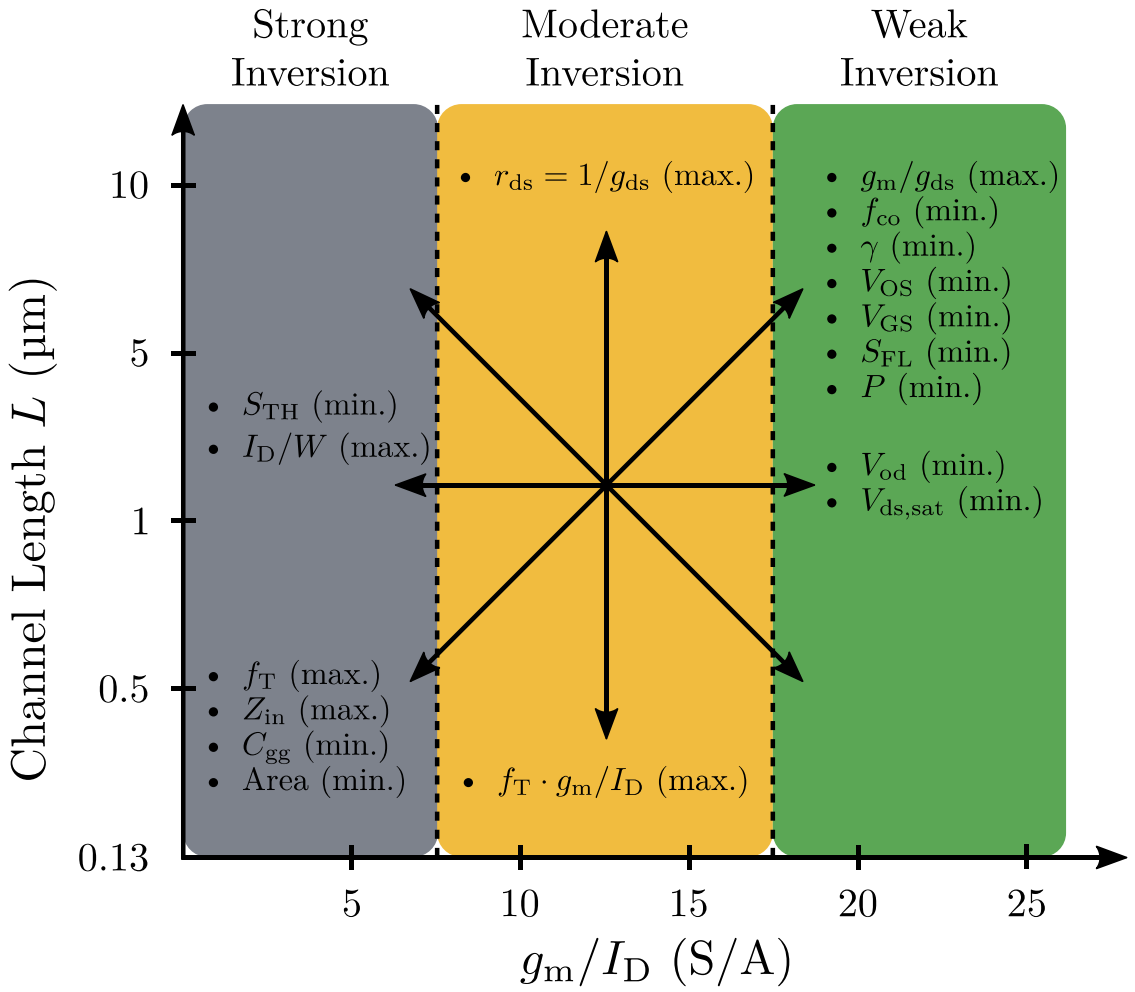
State of the Art

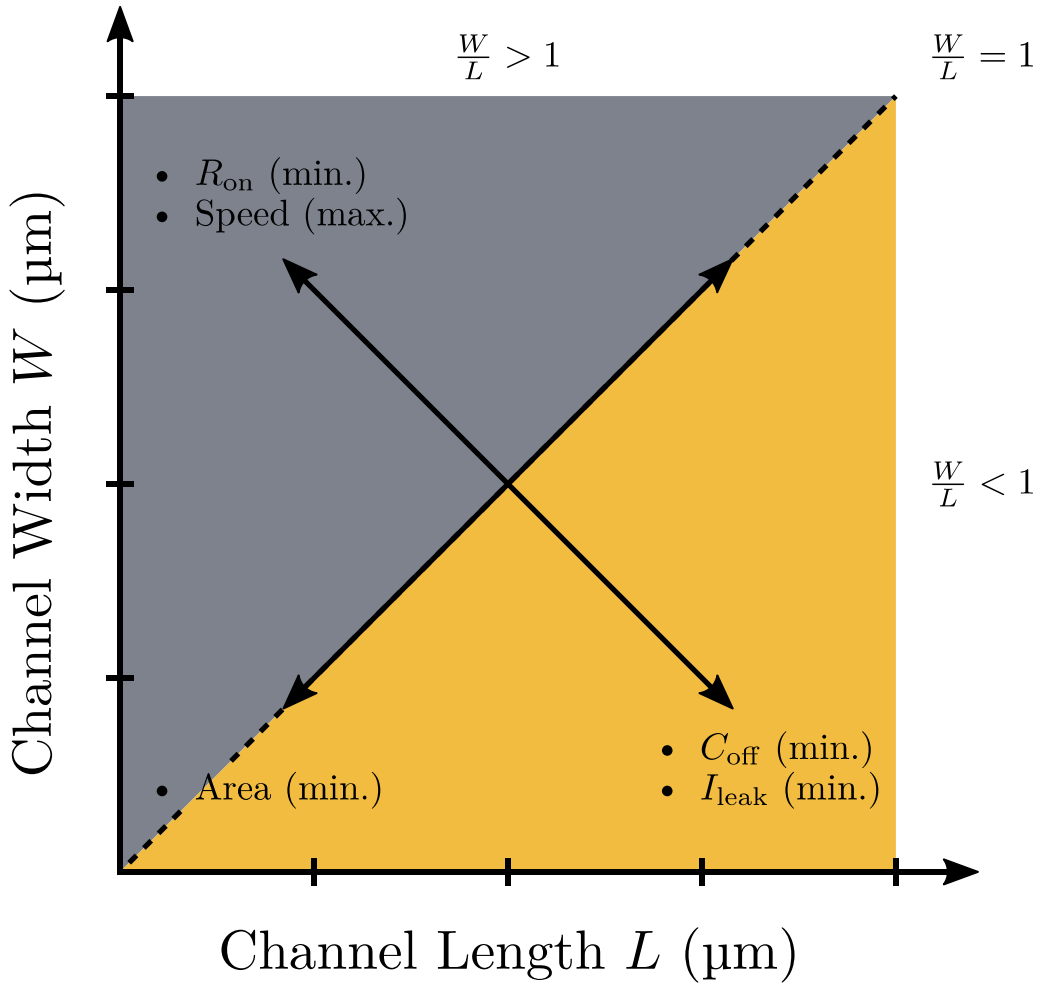
References	floating-window / fixed-window	single-ended / fully-differential	adaptive thresholds / adaptive trigger	continuous-time / discrete-time
Werzi, 2025	floating-window	single-ended	adaptive thresholds	continuous-time AFE / synchronous digital core
Van Assche, 2024	floating-window	single-ended	adaptive trigger	discrete-time
Timmermans, 2023	fixed-window	fully-differential	fixed thresholds	continuous-time
Jing, 2023	floating-window	single-ended	adaptive thresholds	continuous-time
Yazdani, 2022	fixed-window	fully-differential	fixed thresholds	continuous-time
Maslik, 2018	floating-window	single-ended	fixed thresholds	continuous-time
Zhang, 2014	floating-window	single-ended	fixed thresholds	continuous-time
Weltin-Wu, 2013	floating-window	single-ended	adaptive thresholds	continuous-time
Trakimas, 2011	floating-window	fully-differential	adaptive thresholds	continuous-time
Li, 2011	fixed-window	single-ended	fixed thresholds	continuous-time
This work - demonstrator	floating-window	single-ended	fixed & adaptive thresholds	continuous-time AFE / synchronous digital core
This work - ASIC	fixed-window	fully-differential	fixed & adaptive thresholds	discrete-time

$g_\mathrm{m}/I_\mathrm{D}$-Methodology

- Sizing transistors depends on numerous design specifications and tradeoffs
- Analytical models:
  - Square-law equations deviate from actual transistor behavior
  - Even worse in deep submicron processes
  - Especially problematic for moderate and weak inversion
- $g_\mathrm{m}/I_\mathrm{D}$-Methodology:
  - Compute lookup tables over a wide range of operating points
  - Sizing scripts with Jupyter notebooks
  - Easier migration to different circuit specifications and PDKs
  - https://github.com/iic-jku/analog-circuit-design

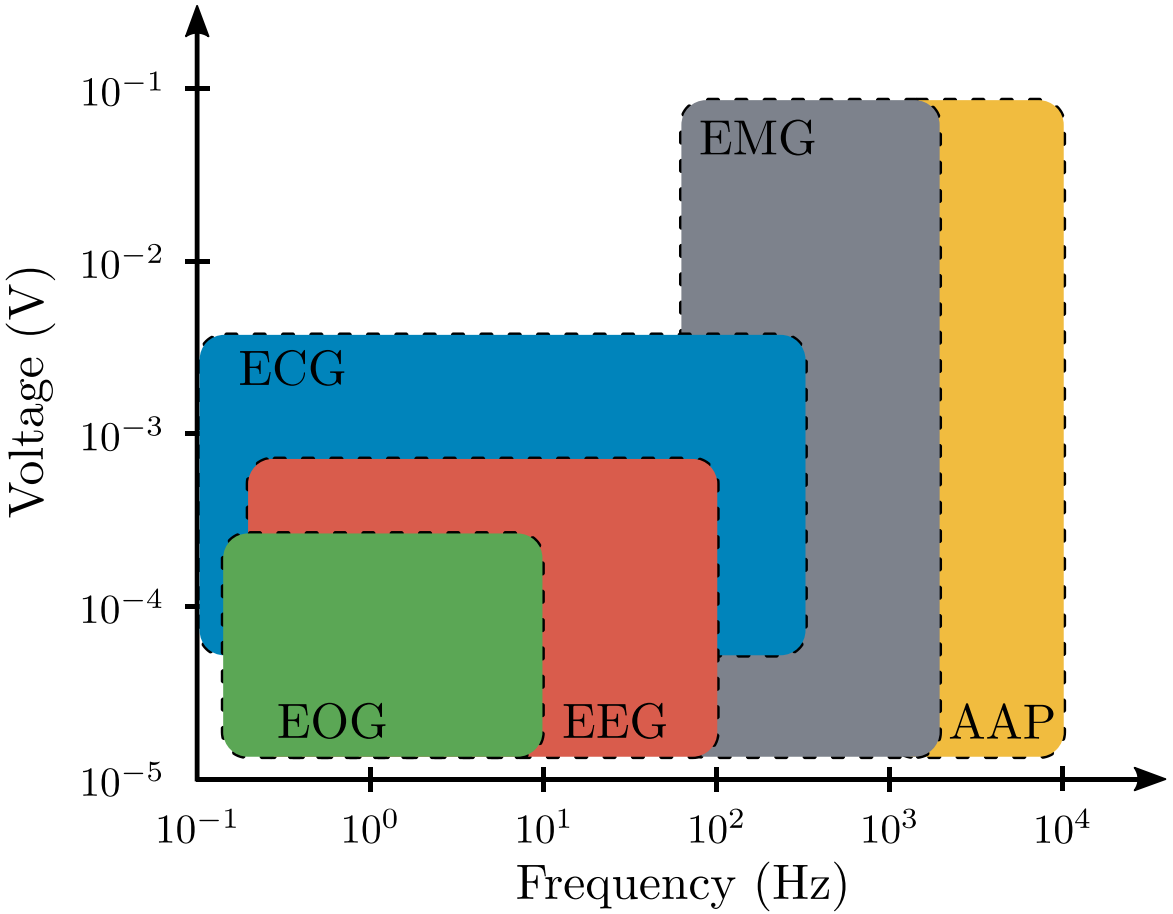
Tradeoffs in Analog Circuit Design

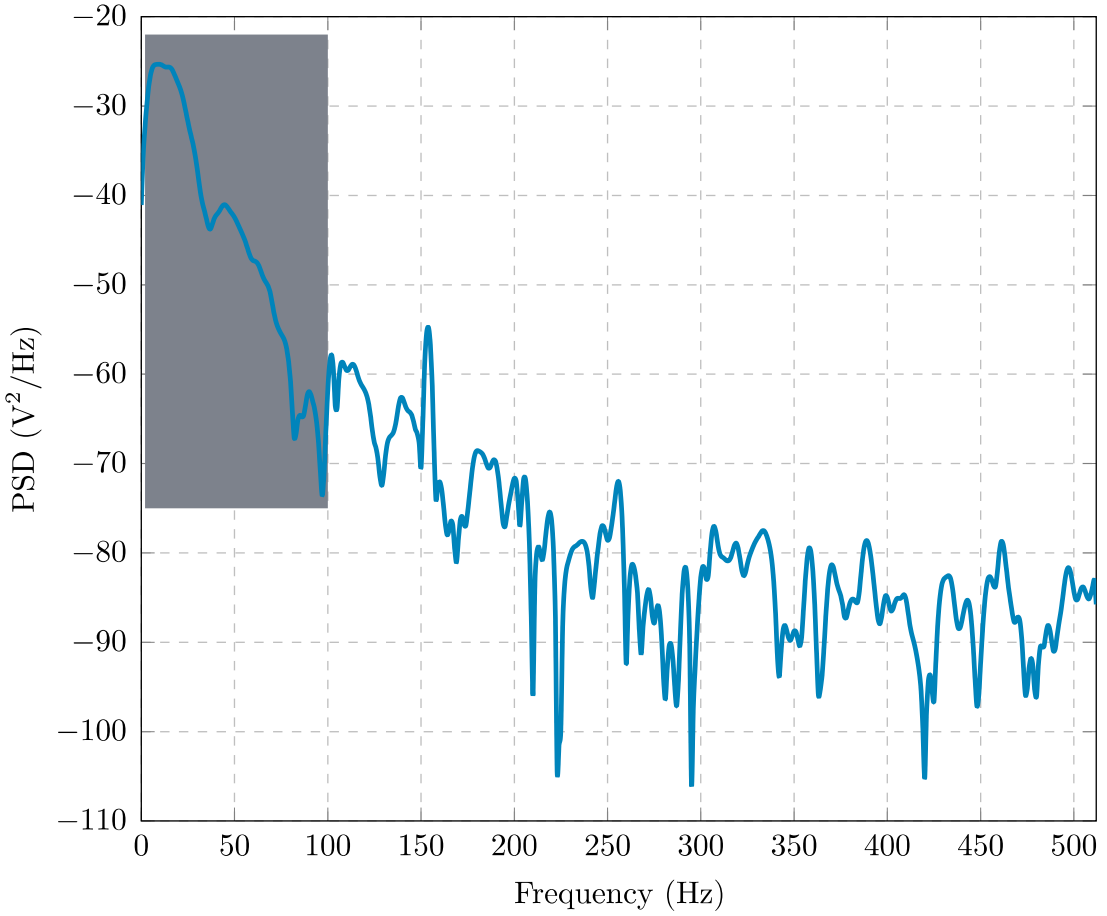




Bandwidth & Gain

- EEG: $B \approx 100\,\text{Hz}$, $20\,\mu\text{V}$ to $800\,\mu\text{V}$
- ECG: $B \approx 500\,\text{Hz}$, $70\,\mu\text{V}$ to $5\,\text{mV}$





Input / Electrode Impedance

- High input impedance of bio-signal AFEs
- High impedance of non-invasive electrodes

Material	Impedance (MΩ) @ 10 Hz	Impedance (MΩ) @ 125 Hz
Ag/AgCl	0.23	0.05
Metal Plate	0.66	0.10
Thin Film	64	6
Cotton	185	33
MEMS	0.65	0.65
Silver Coated	-	0.25
Gold Alloy	-	0.21

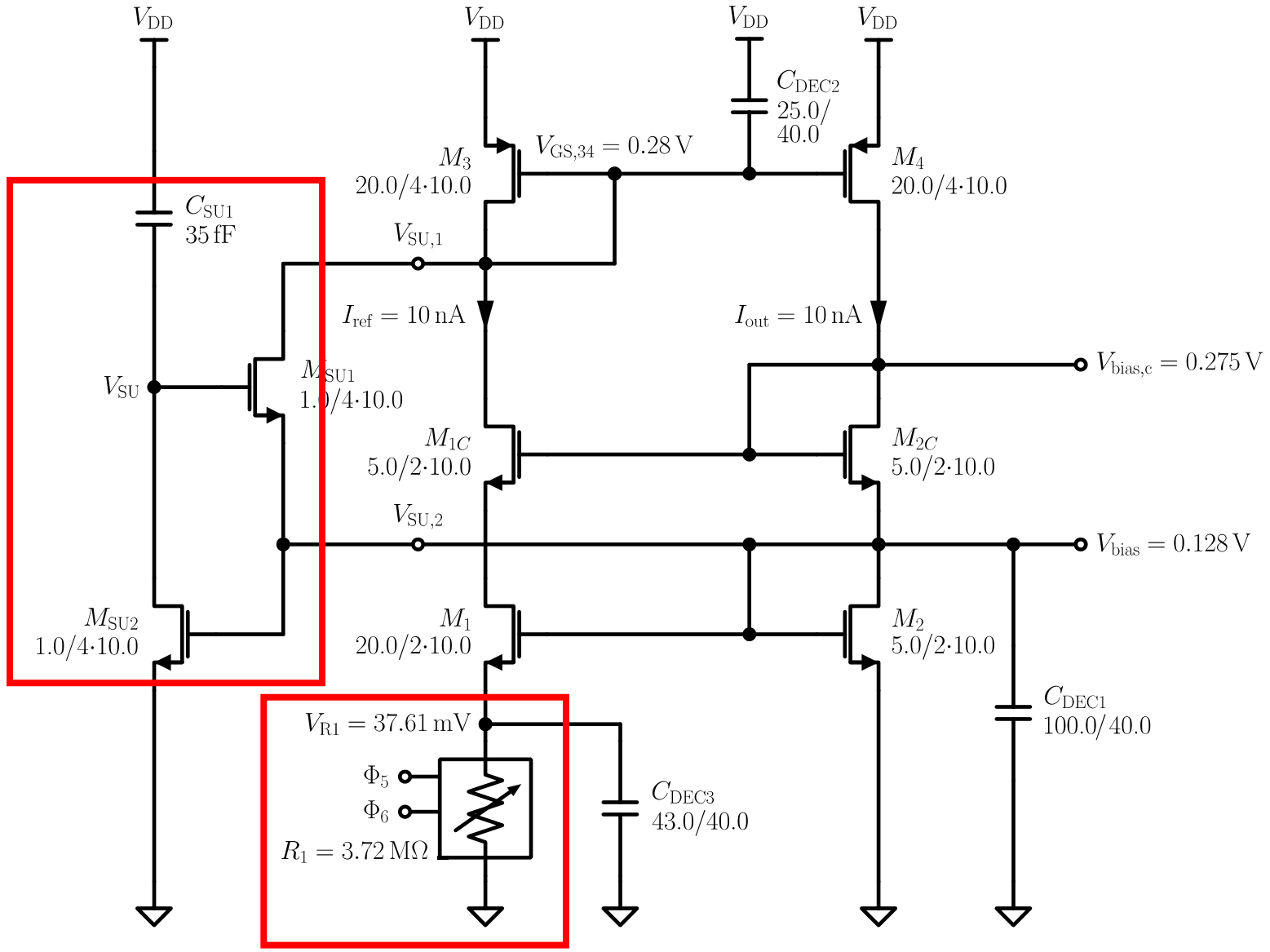
β-Multiplier Reference

$$g_{m,M2} = \frac{2}{R_1}\left(1 - \sqrt{\frac{W_2}{W_1}}\right)$$

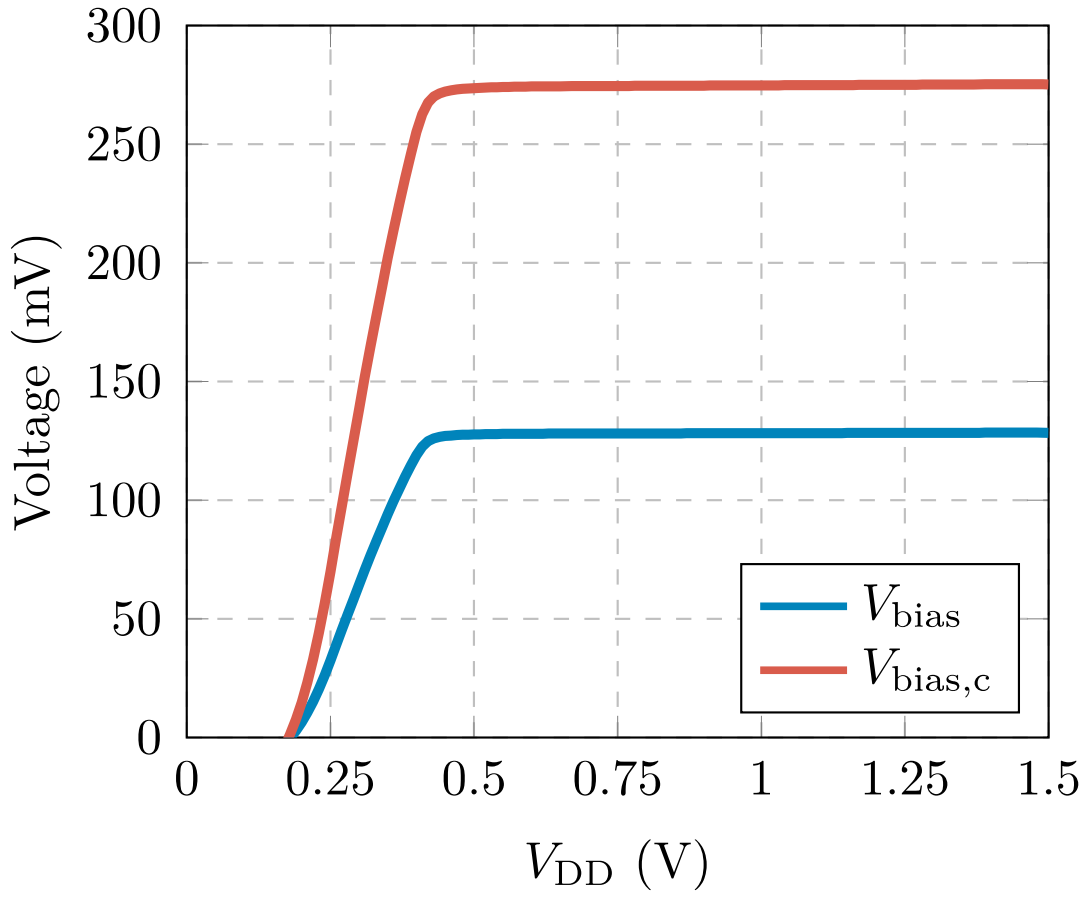
$$W_1 = 4W_2$$

$$g_{m,M2} = \frac{1}{R_1}$$

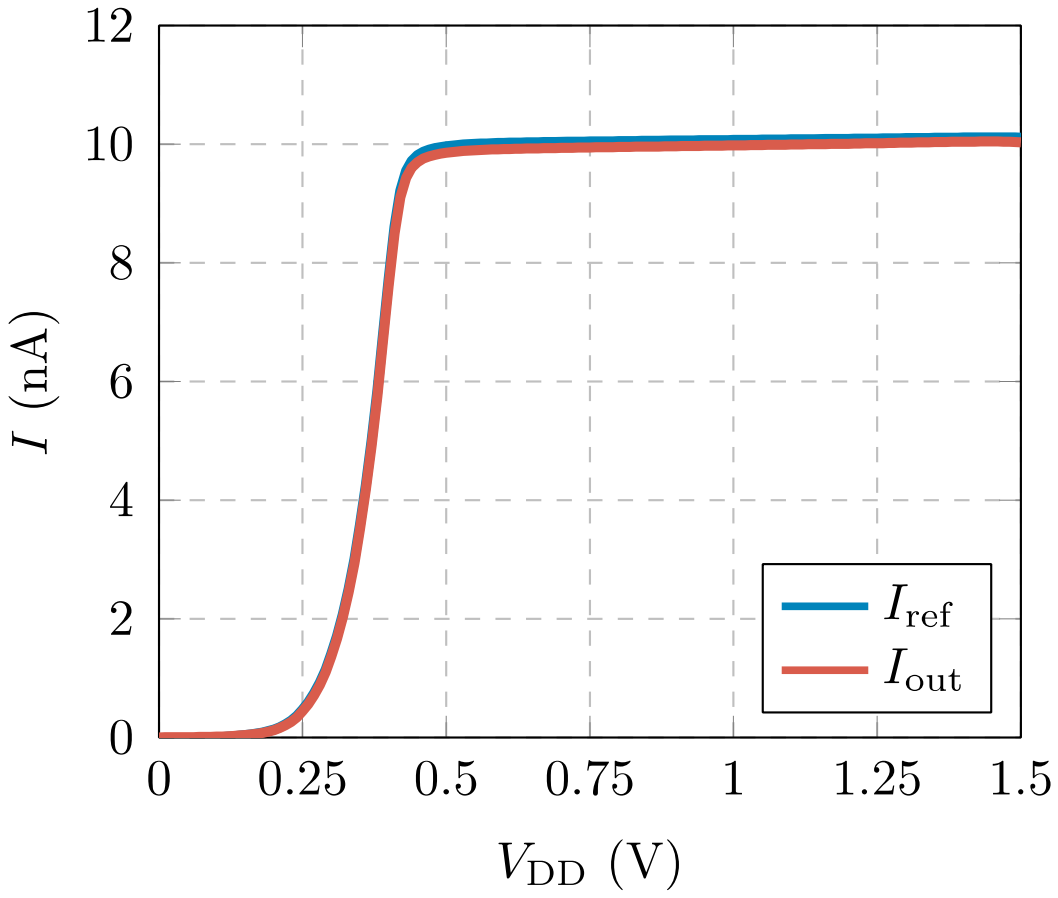
$$I_{ref} = \frac{V_{GS2} - V_{GS1}}{R_1}$$



β-Multiplier Reference

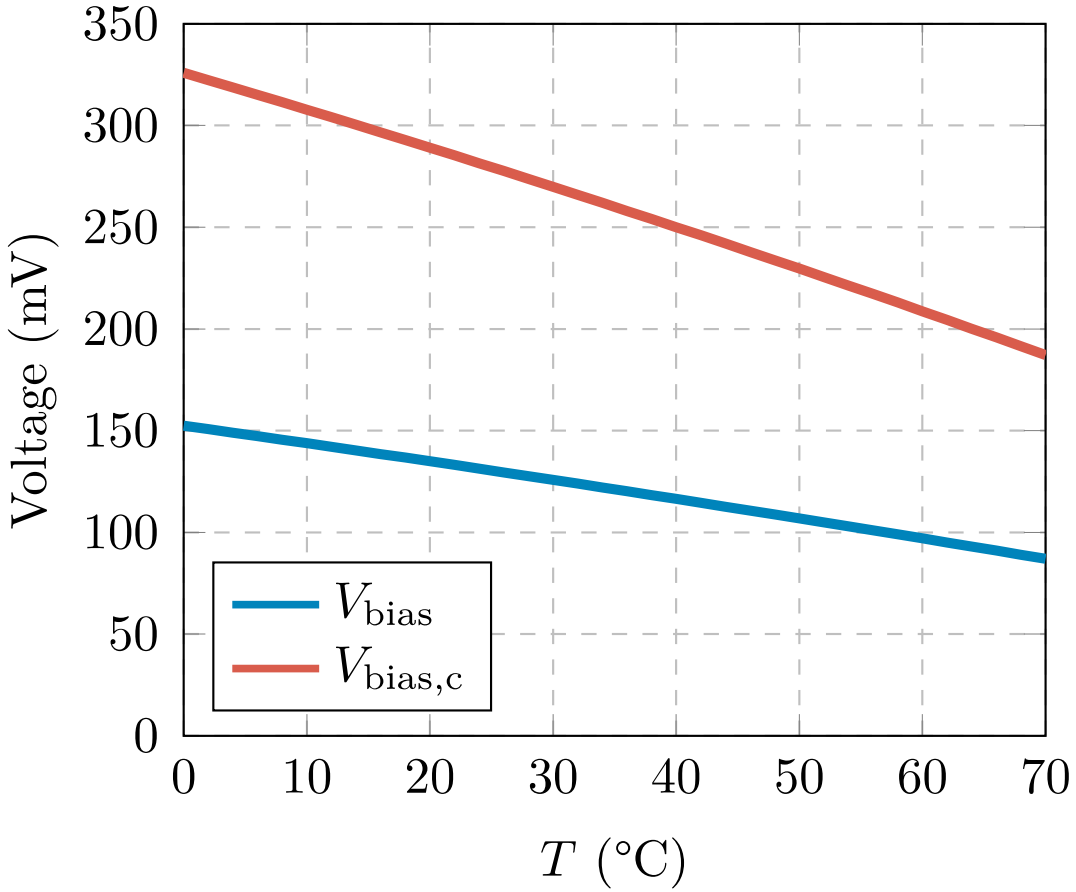


(a) idealized R_1

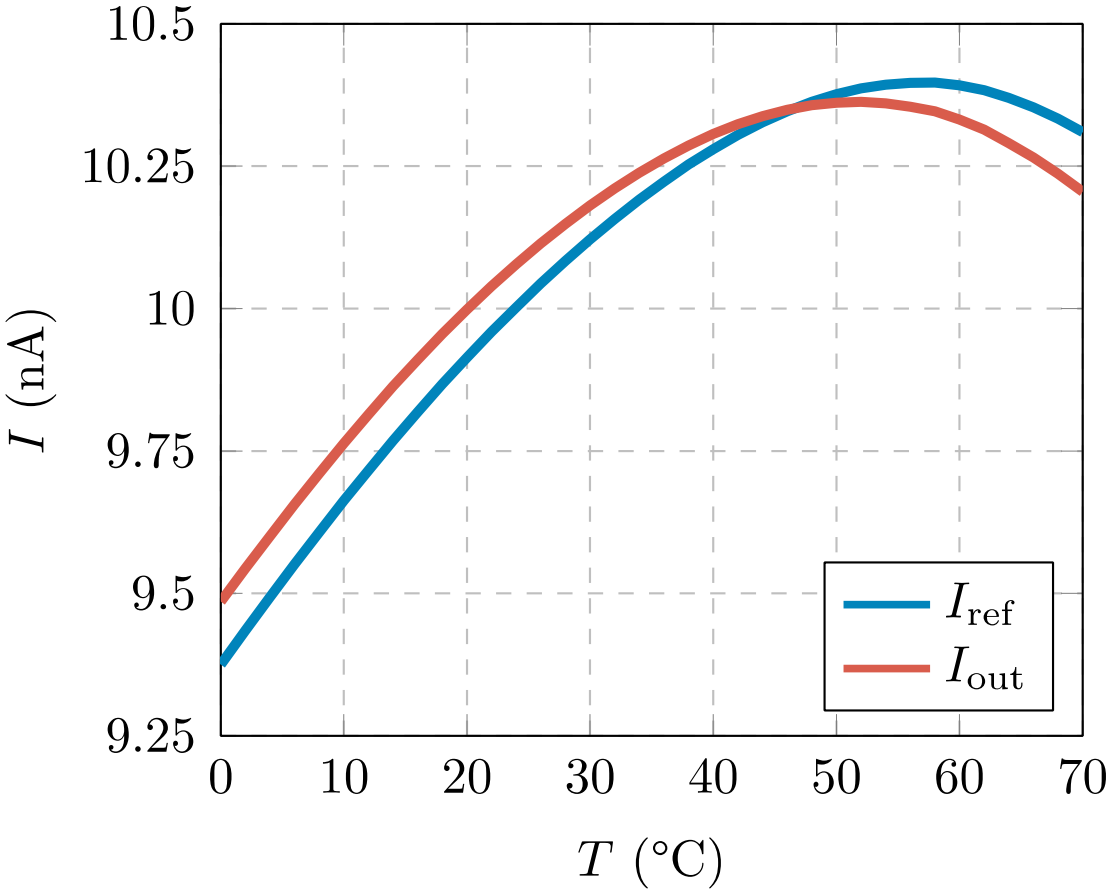


(b) idealized R_1

β-Multiplier Reference



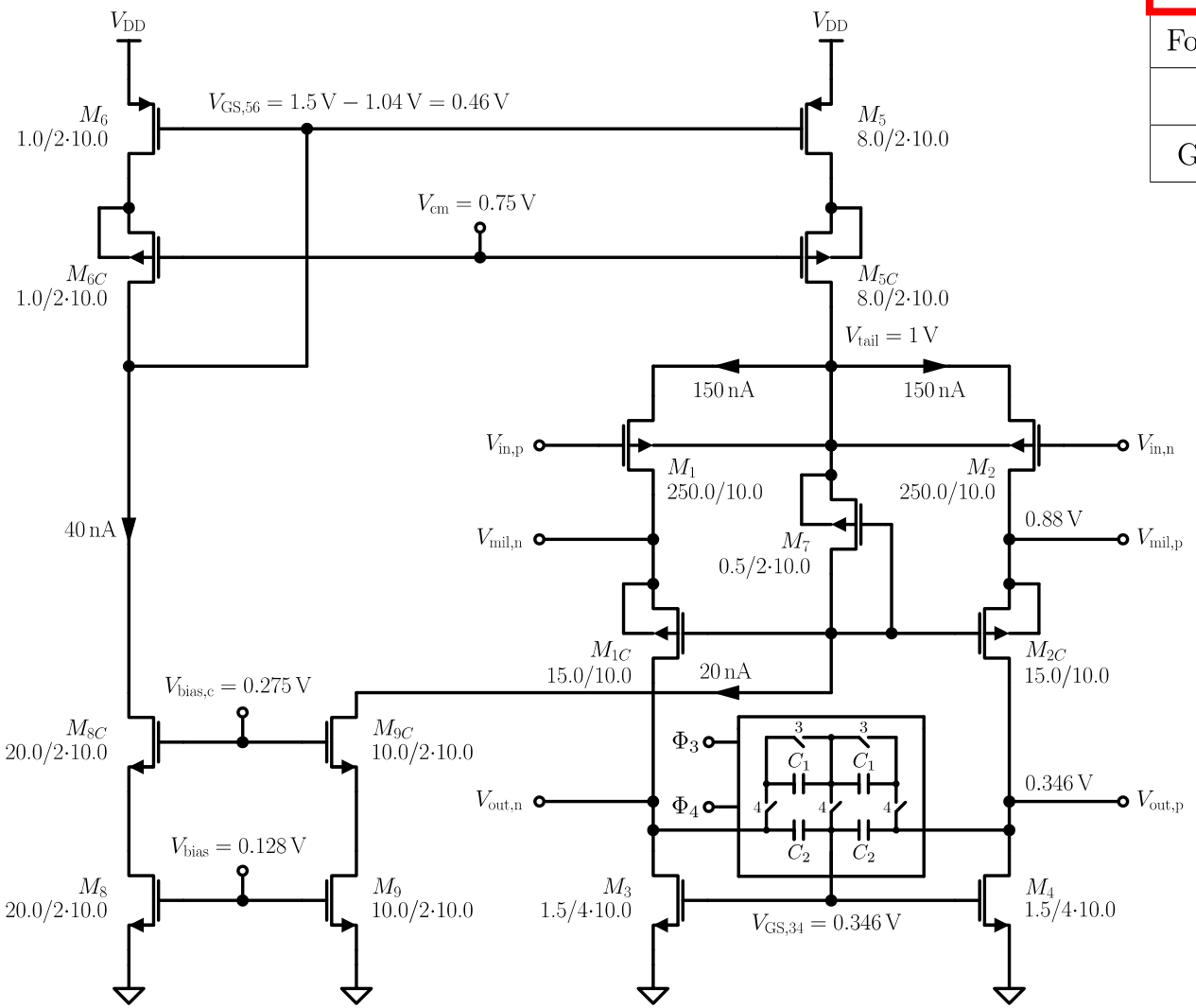
(c) SC R_1



(d) SC R_1

Telescopic Input Stage

OTA Topology	Gain	Output Swing	Speed	Power Dissipation	Noise
Telescopic	medium	medium	highest	low	low
Folded-cascode	medium	medium	high	medium	medium
Two-stage	high	highest	low	medium	low
Gain-boosted	high	medium	medium	high	medium



g_m/I_D (simulation)

$$H_{dm,0} = \frac{g_{m12}}{g_{ds12}\frac{g_{ds12C}}{g_{m12C}} + g_{ds34}} = 44.78\,\text{dB}\ (44.94\,\text{dB})$$

$$f_c = \frac{g_{ds12}\frac{g_{ds12C}}{g_{m12C}} + g_{ds34}}{2\pi C_L} = 4.32\,\text{kHz}\ (4.48\,\text{kHz})$$

$$f_T = H_{dm,0} f_c = \frac{g_{m12}}{2\pi C_L} = 749.34\,\text{kHz}\ (791.18\,\text{kHz})$$

Push-Pull Output Stage

- Increases output voltage swing
- Increases open-loop gain