

The schematic diagram illustrates the external supply voltage circuit for the LD1117 voltage regulator. It features two input supplies: X1 (Supply) and X3 (3.3V\_IN). X1 is connected to X2, which provides the +5V input to the LD1117 (U2). X3 is connected to X4, which provides the +3.3V input to the LD1117. The LD1117 output (VO) is connected to JP6 (SEL\_VCC), which provides the +3.3V output. The circuit includes decoupling capacitors C6 (22uF), C3 (100nF), C4 (100nF), C7 (22uF), and C8 (100nF). Resistor R31 is 0R and R32 is 0R. The output voltage is +3.3V.

### Filtering Analog / Digital Supply

The diagram illustrates a power supply filtering circuit. It starts with a +3.3V source connected to a node before inductor L1 (100R@100MHz). After L1, there is a node connected to AVDD and a 100nF capacitor C11 to GND. This is followed by a node connected to PWFBOUT and a 22uF capacitor C14 to GND. Then, there is a node connected to PWFBIN and a 100nF capacitor C12 to GND. Finally, there is a node connected to PWFBIN and a 100nF capacitor C13 to GND. An inductor L2 (100R@100MHz) is connected between the node before C13 and the node after C13.

[illegible]

**RESET Circuit**

The circuit diagram shows the following components and connections:

- +3.3V** supply connected to resistor **R30** (10k).
- Resistor **R30** is connected to a node that branches to a push-button switch **S2** (B3U-1000) and a capacitor **C15** (470nF).
- The push-button switch **S2** is connected to **GND**.
- The capacitor **C15** is connected to **GND**.
- A test point **TP6** is located at the node between R30, S2, and C15.
- The output of this node is connected to the **PHY\_RST** pin of the PHY78C01 chip.

### Quartz Circuit

The diagram illustrates a Quartz Circuit. It features two input pins, X1 and X2, connected to a central quartz crystal component labeled XT1. The crystal is specified as 25MHz. Each input pin (X1 and X2) is connected to the crystal through a 22pF capacitor, labeled C1 and C2 respectively. Both capacitors are connected to ground (GND). Additionally, there is a separate component labeled X5, which is an external clock source (EXT. CLK). It has three pins labeled 1, 2, and 3, with pin 1 being the output.

# 100 Mbps MII & Interface

Length-Matching of TX & RX Data with CLK!

The diagram shows a 3x20 pin connector with three columns of pins labeled X9, X10, and X11. The pins are numbered 1 to 20 in each column. The connections are as follows:

- Column X9:**
  - Pin 1: COL
  - Pin 2: TXEN
  - Pin 3: TXD3
  - Pin 4: TXD2
  - Pin 5: TXD1
  - Pin 6: FPGA +5V
  - Pin 7: TXD0
  - Pin 8: TXC
  - Pin 9: RXC
  - Pin 10: RXD3
  - Pin 11: RXD2
  - Pin 12: RXD1
  - Pin 13: FPGA +3.3V
  - Pin 14: RXD0
  - Pin 15: CRS
  - Pin 16: (empty)
  - Pin 17: (empty)
  - Pin 18: (empty)
  - Pin 19: (empty)
  - Pin 20: (empty)
- Column X10:**
  - Pin 1: 1
  - Pin 2: 3
  - Pin 3: 5
  - Pin 4: 7
  - Pin 5: 9
  - Pin 6: 11
  - Pin 7: 13
  - Pin 8: 15
  - Pin 9: 17
  - Pin 10: 19
  - Pin 11: 21
  - Pin 12: 23
  - Pin 13: 25
  - Pin 14: 27
  - Pin 15: 29
  - Pin 16: 31
  - Pin 17: 33
  - Pin 18: 35
  - Pin 19: 37
  - Pin 20: 39
- Column X11:**
  - Pin 1: 2
  - Pin 2: 4
  - Pin 3: 6
  - Pin 4: 8
  - Pin 5: 10
  - Pin 6: 12
  - Pin 7: 14
  - Pin 8: 16
  - Pin 9: 18
  - Pin 10: 20
  - Pin 11: 22
  - Pin 12: 24
  - Pin 13: 26
  - Pin 14: 28
  - Pin 15: 30
  - Pin 16: 32
  - Pin 17: 34
  - Pin 18: 36
  - Pin 19: 38
  - Pin 20: 40

On the right side, the following signals are connected to the pins:

- Pin 10: RXDV
- Pin 11: RXER
- Pin 12: MDIO\_0R
- Pin 13: MDIO\_0R
- Pin 14: PHY\_RST
- Pin 15: GND

Legend:

- FPGA +5V
- FPGA +3.3V
- MDIO\_0R
- PHY\_RST
- GND

DNP R47-R48: Also used for Zero Crossing Switches on TBS PCB

The schematic shows two resistors, R47 and R48, connected between the MDC and MDIO signals and their respective 0R pins. The connections are as follows:

- R47: MDC --- R47 --- MDC\_0R
- R48: MDIO --- R48 --- MDIO\_0R

The schematic diagram illustrates the 100 Mbps Serial Network Interface. It features a network interface chip (U3, 749013011A) connected to a network connector (X7, 74980100001). The interface includes various passive components such as resistors (R40-R46, R41-R42, R36), capacitors (C16-C22), and a transformer (U3). The diagram is labeled "100 Mbps Serial Network Interface".

1. This configuration shows

-> Enable: Auto negotiation, FD 100Mbps, Link Down Power Saving, MII interface

-> Disable: Isolate, Repeater mode

2. These seven configuration pins could be connected to VDD or GND directly.

Device Configuration Interface

Figure 1 shows the pin configuration for the Device Configuration Interface. The interface is a 14-pin connector (S1) with pins 1-7 connected to +3.3V and pins 8-14 connected to GND. The pins are labeled with their functions: RPTR/RTT2, ISOLATE, ANE, DUPLEX, SPEED, LDPS, and MIU/SNIB/TXDS. The default state is OFF.

**Management Pins**

CRS  
+3.3V  
R35 5.1k  
GND

COL  
+3.3V  
R33 5.1k  
GND

MDIO  
+3.3V  
R5 1.5k  
GND

RXER  
+3.3V  
R34 5.1k  
GND

R33 is reserved for 8201CL/CP LED Mode (internal Pull-Down R)  
0: CP LED Mode (DNP)  
1: BL LED Mode

R34 is reserved for ensuring 8201BL/CL/CP latch to UTP Mode.