### 17.2 Options

Use `option option=val option=val` to set various options; important ones are:

- `abstol` sets the absolute current error tolerance (default is 1pA)
- `gmin` is the conductance applied at every node for convergence improvement (default is 1e-12); this can be critical for very high impedance circuits
- `klu` sets the KLU matrix solver
- `list` print the summary listing of the input data
- `maxord` sets the numerical order of the integration method (default is 2 for Gear)
- `method` set the numerical integration method to `gear` or `trap` (default is `trap`)
- `node` prints the node table
- `opts` prints the option values
- `temp` sets the simulation temperature
- `reltol` set the relative error tolerance (default is 0.001 = 0.1%)
- `savecurrents` saves the terminal currents of all devices
- `sparse` sets the sparse matrix solver, which can run noise analysis, but is slower than `klu`
- `vntol` sets the absolute voltage error tolerance (default is 1µV)
- `warn` enables the printing of the SOA warning messages

### 17.3 Convergence Helper

- `option gmin` can be used to increase the conductance applied at every node
- `option method=gear` can lead to improved convergence
- `.nodeset` can be used to specify initial node voltage guesses
- `.ic` can be used to set initial conditions

## 18 Appendix: Xschem Cheatsheet

When opening Xschem, using `Help -> Keys` a pop-up windows comes up with many useful shortcuts. The most useful are:

#### 18.0.0.1 Moving around in a schematic:

- `Cursor keys` to move around
- `Ctrl-e` to go back to parent schematic
- `e` to descend into selected symbol
- `f` full zoom on schematic
- `Shift-z` to zoom in
- `Ctrl-z` to zoom out

#### 18.0.0.2 Editing schematics:

- `Del` to delete elements
- `Ins` to insert elements from library
- `Escape` to abort an operation
- `Ctrl-#` to rename components with duplicate names
- `c` to copy elements
- `Alt-Shift-l` to add wire label
- `Alt-l` to add label pin
- `m` move selected objects
- `q` to edit properties
- `Ctrl-s` to save schematic
- `t` to place a text
- `Shift-T` to toggle the `ignore` flag on an instance
- `u` to undo an operation
- `w` to draw a wire
- `Shift-W` draw wire and snap to close pin or net point
- `&` to join, break, and collapse wires

#### 18.0.0.3 Viewing/Simulating Schematics

- `5` to only view probes
- `k` to highlight selected net
- `Shift-K` to unhighlight all nets
- `Shift-o` to toggle light/dark color scheme
- `s` to run a simulation

# 19 Circuit Designer's Etiquette

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## 19.1 Prolog

A consistent naming and schematic drawing style, as well as VHDL/Verilog coding scheme, is a huge help in avoiding errors and increasing productivity. Even if just one person works on a design, the error rate is lowered. If multiple persons work together in a team, a consistent working style is a big help for smooth cooperation without misunderstanding each other's intentions. Consistency also helps to reuse existing blocks. In a well-done design, the documentation is included in the schematic/source code, so there is no searching for a piece of documentation somewhere else (which is often not found anyway).