An Open-Source Adaptive Event-Based ADC for Bio-Signal Acquisition in 130nm CMOS

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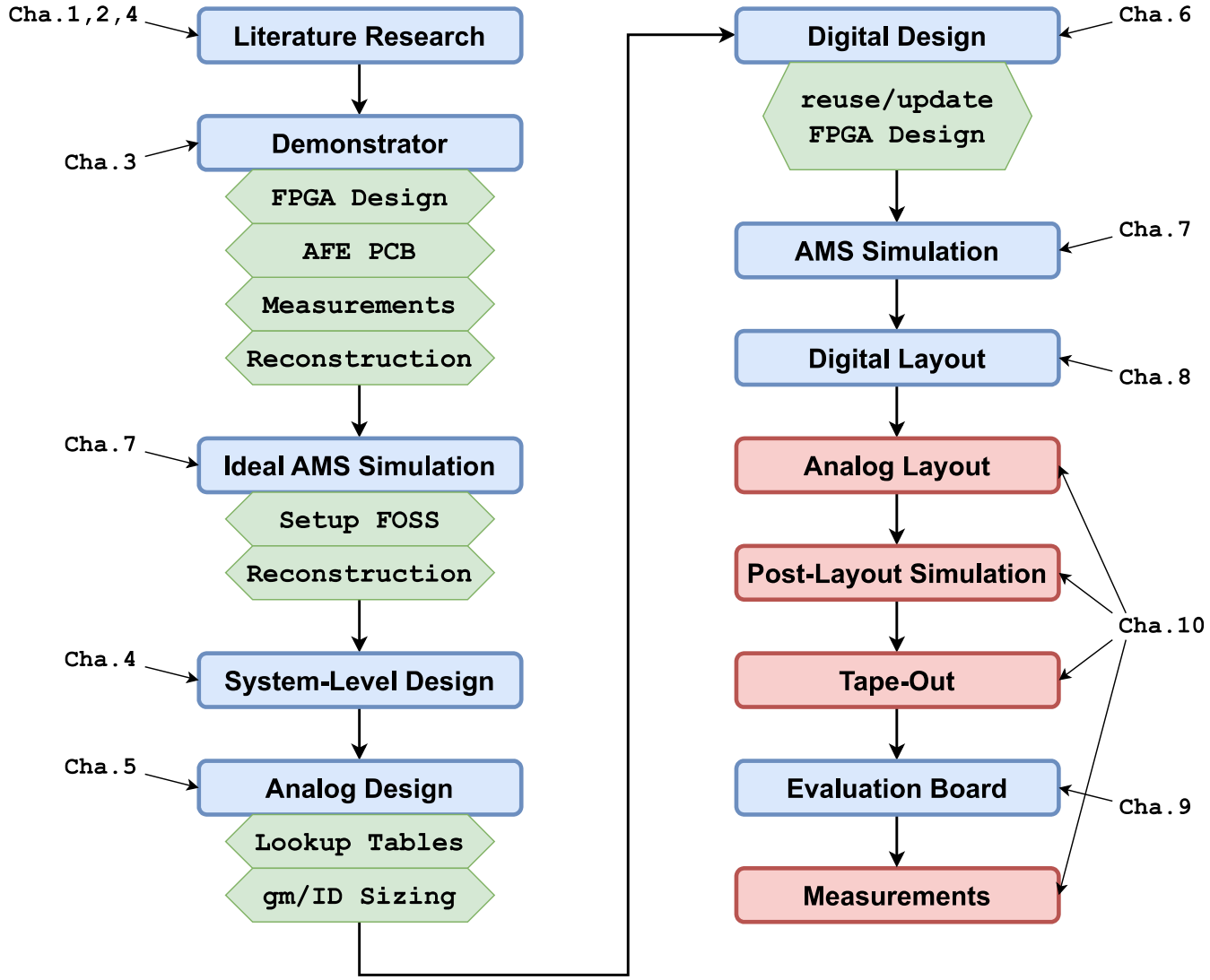
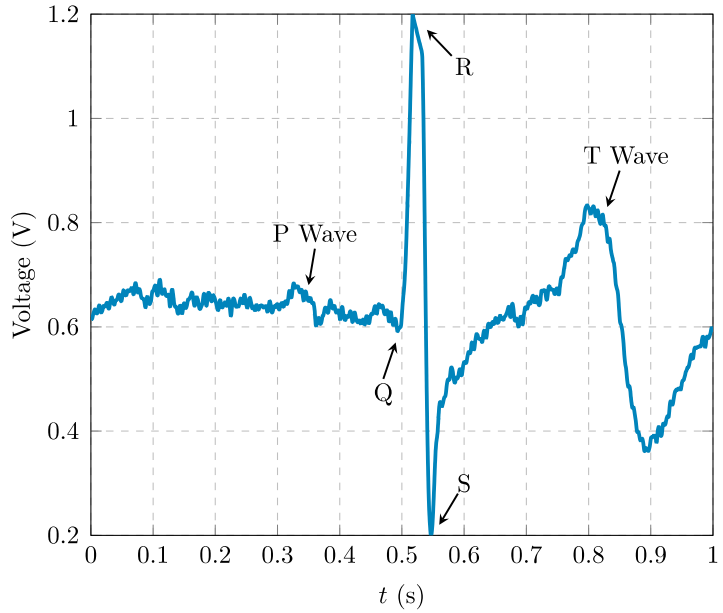
Thesis Organization



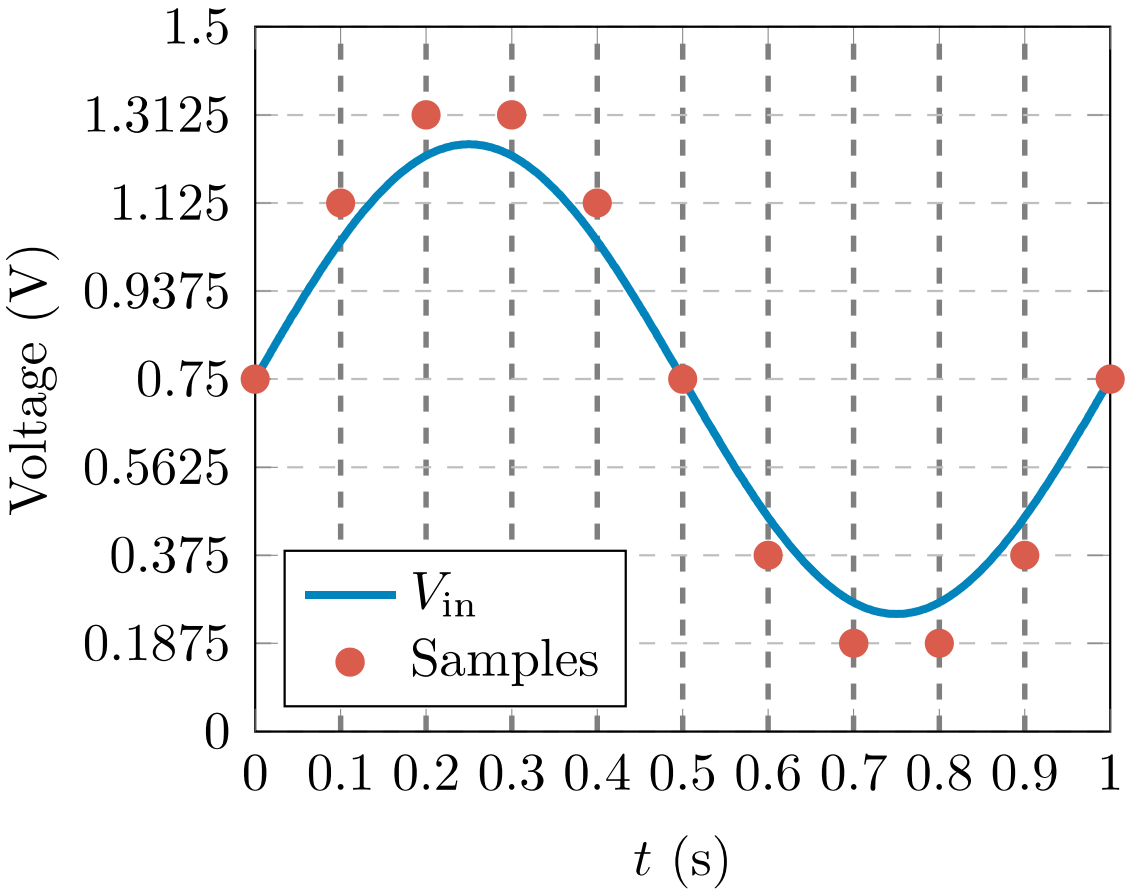
Theoretical Background

Nyquist vs. Event-Based ADC

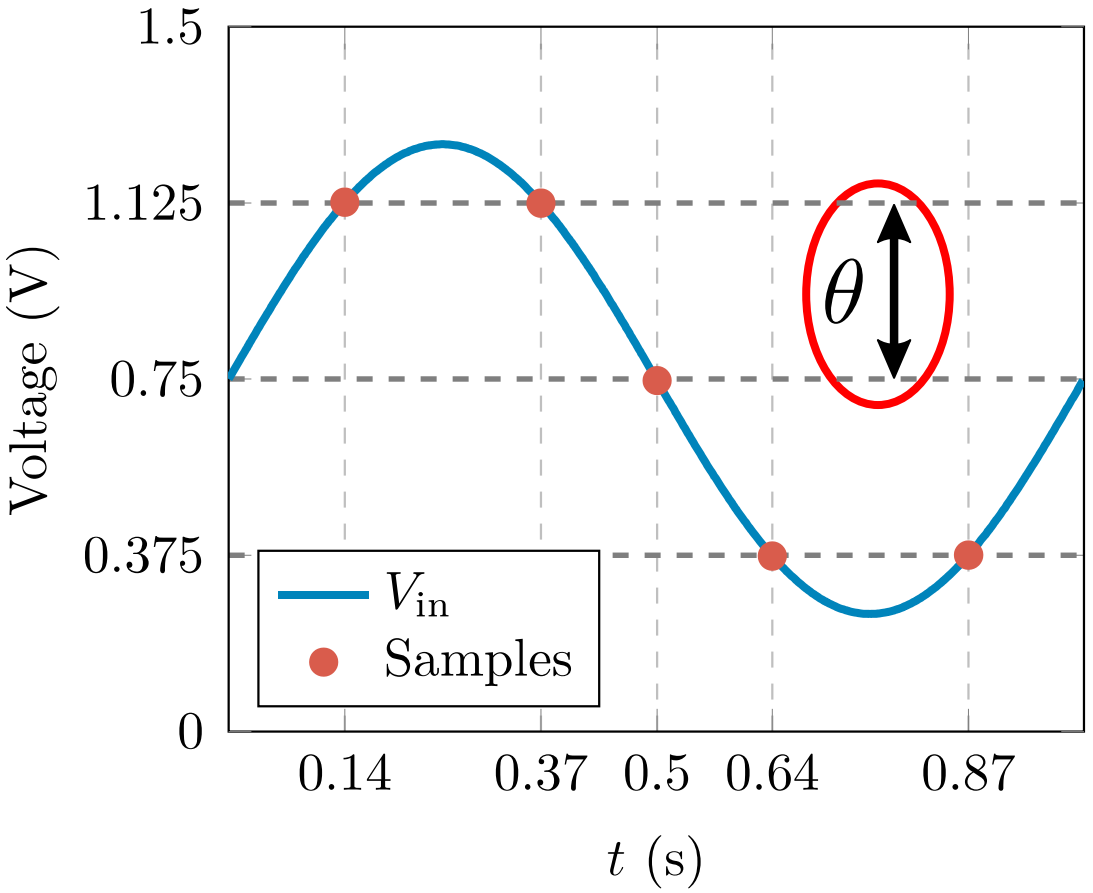
- Nyquist ADCs sample input at a fixed sample rate → uniform samples
- Voltage values are quantized and encoded → amplitude quantization
- Event-based ADCs only produce samples when input exceeds a predefined threshold θ → non-uniform event pulses (spikes)
- Time between spikes is measured and encoded → time quantization
- For sparse signals, event-based ADCs significantly decrease:
  - number of samples
  - storage resources
  - computational effort
  - power consumption



Nyquist vs. Event-Based ADC – Time Domain



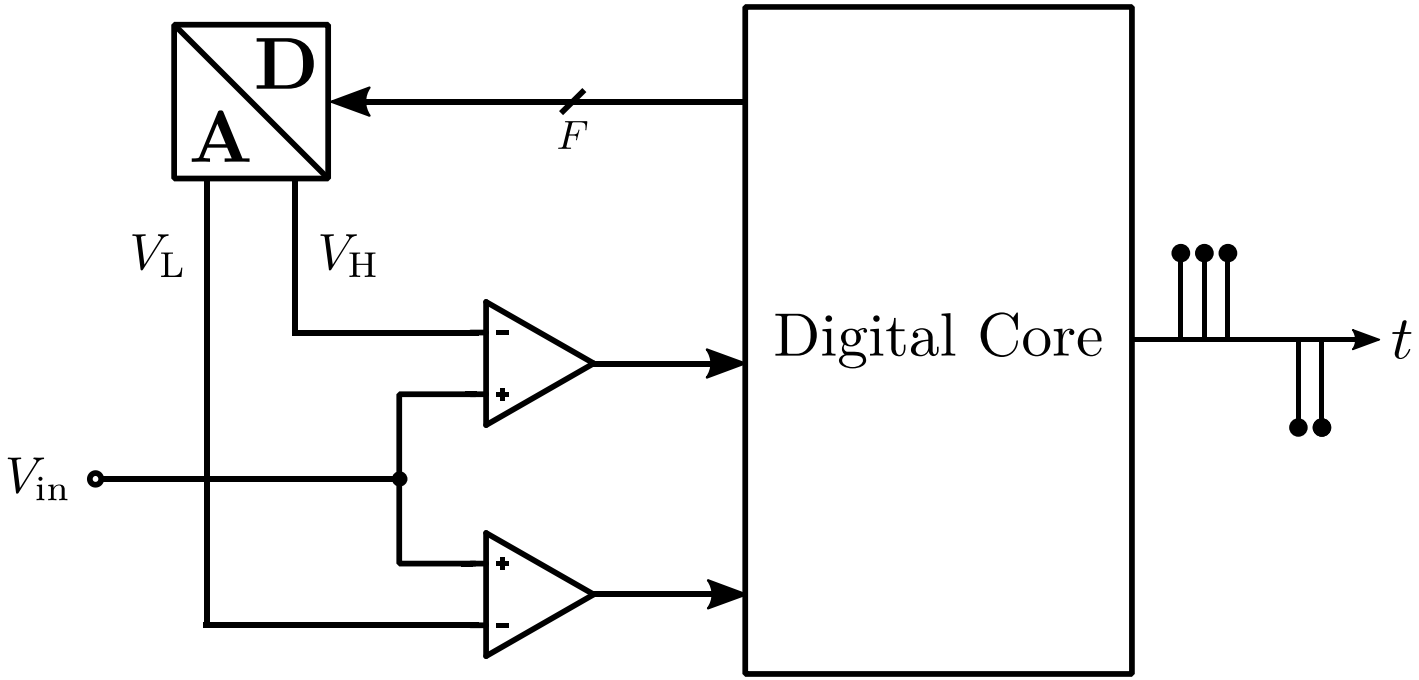
(a) Nyquist ADC

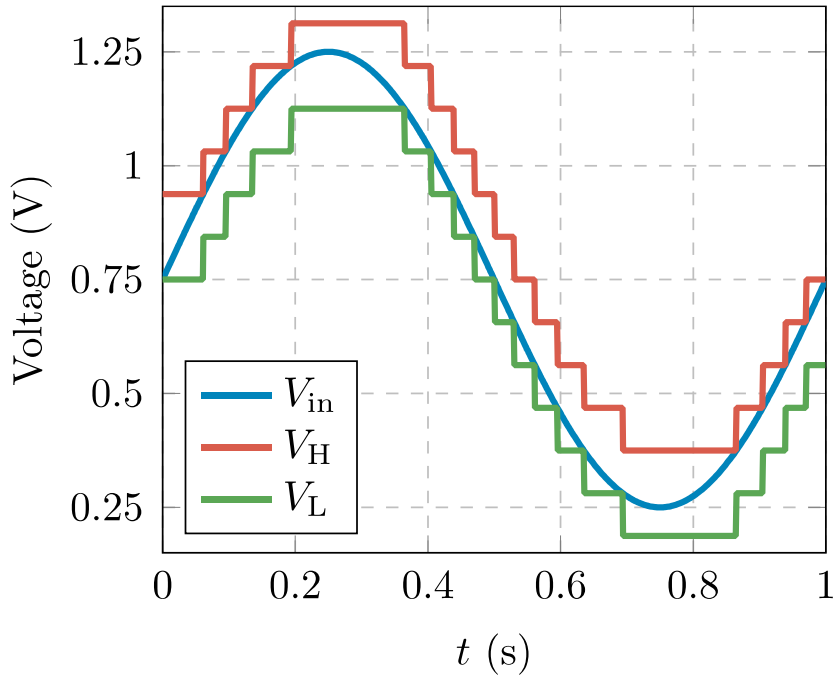


(b) Event-Based ADC

Floating-Window Architecture

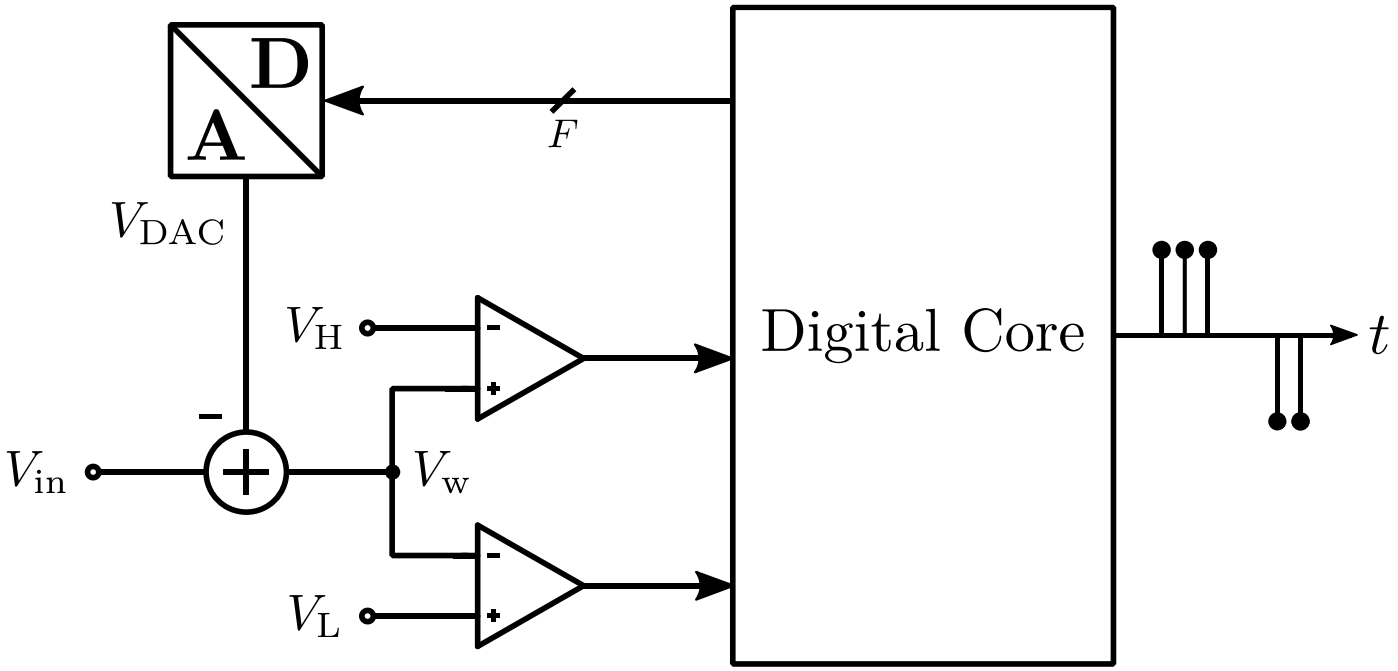
- If $V_{\text{in}} > V_{\text{H}}$, the upper comparator outputs a logic one, and both DAC voltages shift up by θ and vice versa for $V_{\text{in}} < V_{\text{L}}$.

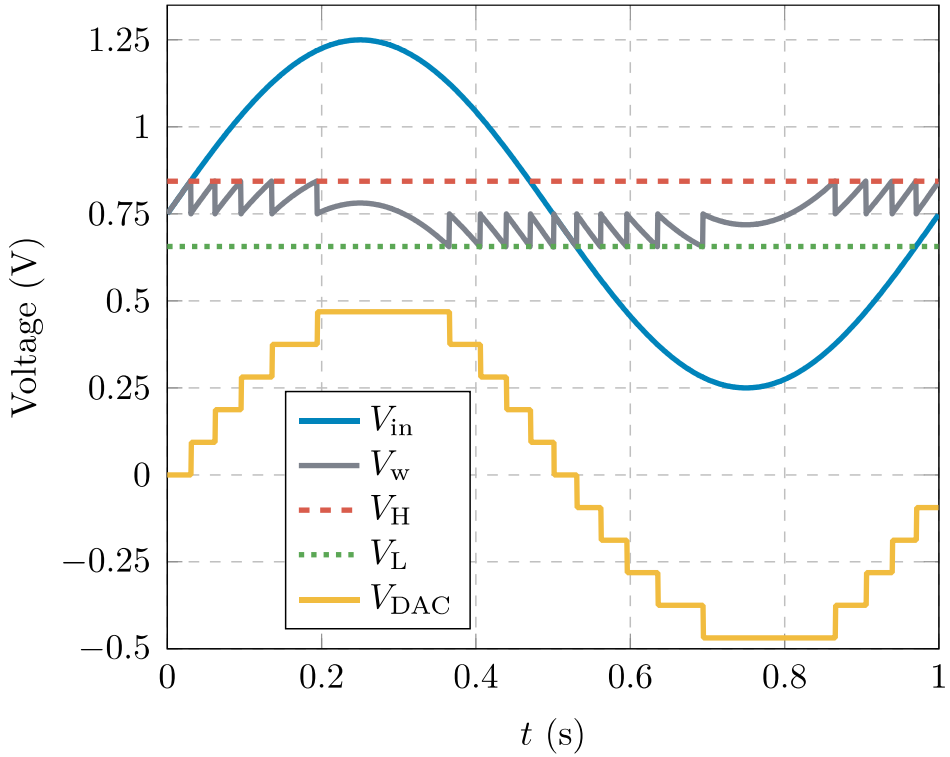




Fixed-Window Architecture

- V_{in} is wrapped within V_{H} and V_{L} whenever a threshold crossing occurs, by subtracting the current DAC voltage from V_{in}.





Nyquist vs. Event-Based ADC – Aliasing

- Nyquist ADC: The sampling limit induced by aliasing is defined by the Shannon-Nyquist theorem:

$$f_s > 2f_{\max}$$

- Event-based ADC: The aliasing effect is caused by their slew rate:

$$\mathrm{SR} = \max \left| \frac{\mathrm{d}V_{\mathrm{in}}(t)}{\mathrm{d}t} \right| < \frac{\theta}{t_{\mathrm{loop}}} = \frac{V_{\mathrm{REF}}/2^F}{t_{\mathrm{loop}}}$$

$$t_{\mathrm{loop}} = t_{\mathrm{pd}} + t_{\mathrm{core}} + t_{\mathrm{settle}}$$

- The maximum frequency for sine waves ($\mathrm{SR} = 2\pi A f_{\max}$) for event-based ADCs with fixed thresholds can be expressed as:

$$f_{\max} = \frac{V_{\mathrm{REF}}}{2\pi t_{\mathrm{loop}} A_{\max} 2^F}$$

Nyquist vs. Event-Based ADC – SQNR

- Nyquist ADC: The time- and frequency-domain SQNR for a full-scale amplitude sine wave, resulting from uniformly distributed amplitude quantization, depends on the ADC resolution (N):

$$\mathrm{SQNR} = 6.02N + 1.76$$

- Event-based ADCs: The SQNR, resulting from time quantization, depends on the clock resolution (T_{clk}) and the input signal's frequency (f_{sig}):

$$\mathrm{SQNR} = 20\log_{10}(R) - 14.2$$

where R is the resolution or oversampling ratio:

$$R = \frac{1}{f_{\mathrm{sig}} T_{\mathrm{clk}}} = \frac{f_{\mathrm{clk}}}{f_{\mathrm{sig}}}$$

- Event-based ADCs can achieve an SQNR equivalent to that of an N-bit Nyquist ADC while requiring only a DAC with fewer than N bits ($F < N$).

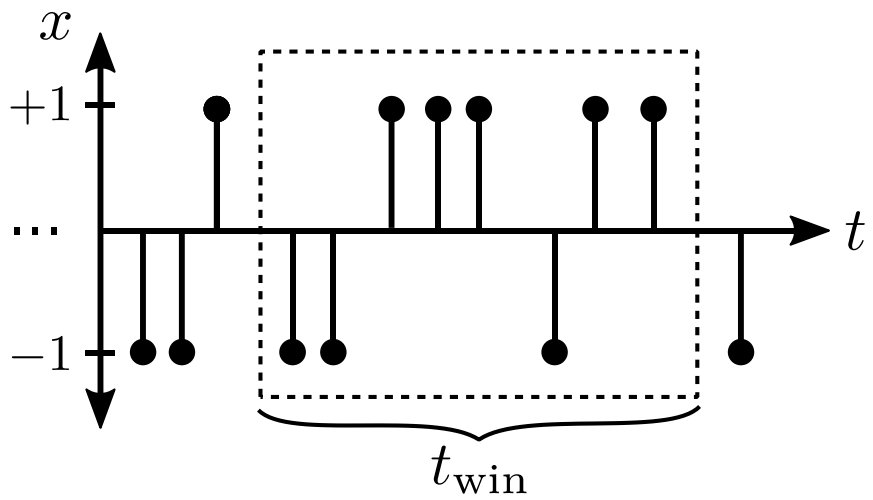
Continuous-Time vs. Discrete-Time

- Continuous-time (CT) system:
  - CT comparator, CT DAC, and asynchronous or clockless digital core
  - Minimize clock uncertainty and loop delay
  - Ideally, no amplitude and no time quantization and no aliasing!
  - Limited by high power consumption and nonidealities of AFE
- Discrete-time (DT) system:
  - Trigger AFE periodically or adaptively
  - Reduction of power consumption
  - Introduction of clock uncertainty and limiting the slew rate to:

$$T_{\mathrm{trig}} \geq (t_{\mathrm{pd}} + t_{\mathrm{core}} + t_{\mathrm{settle}}) = t_{\mathrm{loop}}$$

Adaptive Threshold-Based Sampling

- Input signal dependent adaption of threshold θ
- Reduce number of samples
- Increase maximum slew rate
- Calculation of Weyl's discrepancy within a defined time window



- If the discrepancy is larger / lower than a certain value, θ is doubled / halved.

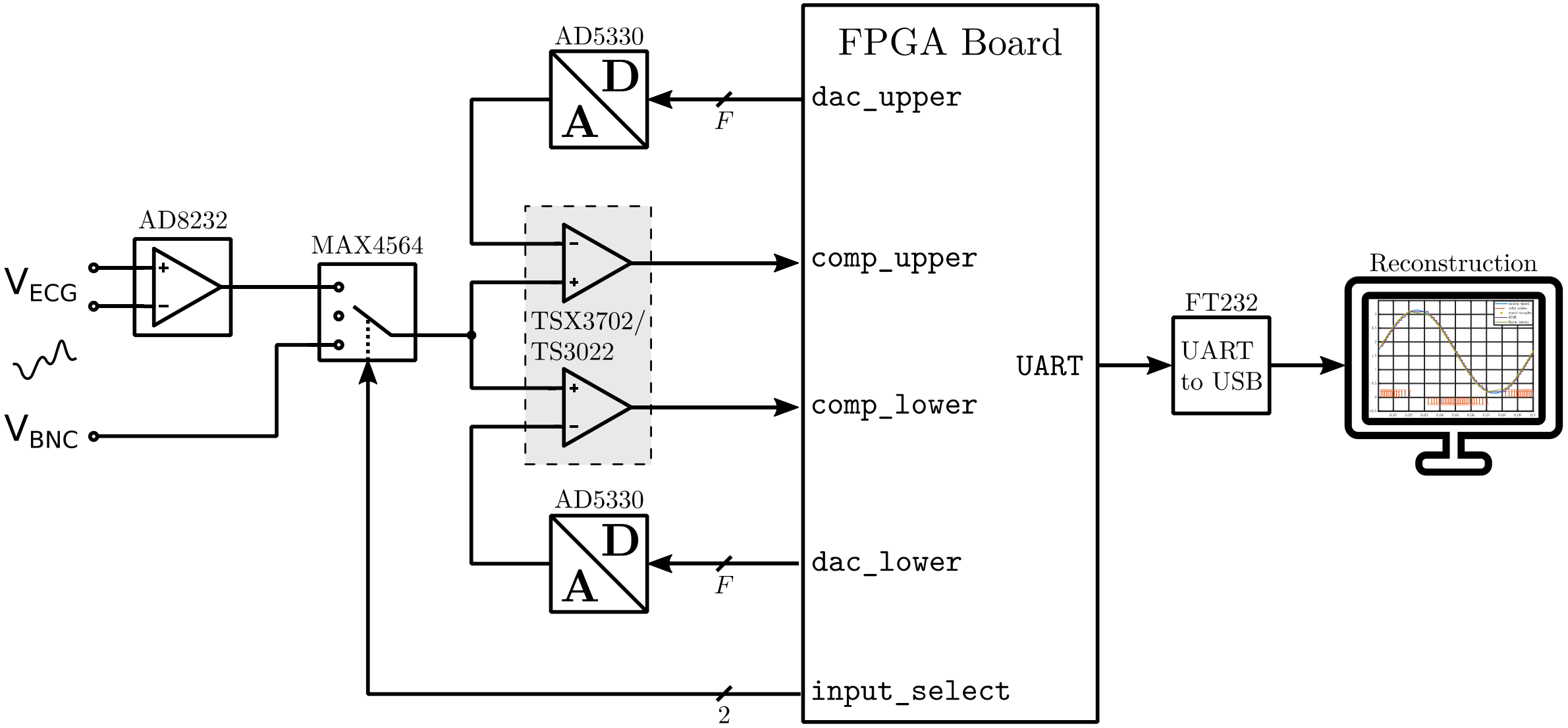
State of the Art

References	floating-window / fixed-window	single-ended / fully-differential	adaptive thresholds / adaptive trigger	continuous-time / discrete-time
Werzi, 2025	floating-window	single-ended	adaptive thresholds	continuous-time AFE / synchronous digital core
Van Assche, 2024	floating-window	single-ended	adaptive trigger	discrete-time
Timmermans, 2023	fixed-window	fully-differential	fixed thresholds	continuous-time
Jing, 2023	floating-window	single-ended	adaptive thresholds	continuous-time
Yazdani, 2022	fixed-window	fully-differential	fixed thresholds	continuous-time
Maslik, 2018	floating-window	single-ended	fixed thresholds	continuous-time
Zhang, 2014	floating-window	single-ended	fixed thresholds	continuous-time
Weltin-Wu, 2013	floating-window	single-ended	adaptive thresholds	continuous-time
Trakimas, 2011	floating-window	fully-differential	adaptive thresholds	continuous-time
Li, 2011	fixed-window	single-ended	fixed thresholds	continuous-time
This work - demonstrator	floating-window	single-ended	fixed & adaptive thresholds	continuous-time AFE / synchronous digital core
This work - ASIC	fixed-window	fully-differential	fixed & adaptive thresholds	discrete-time

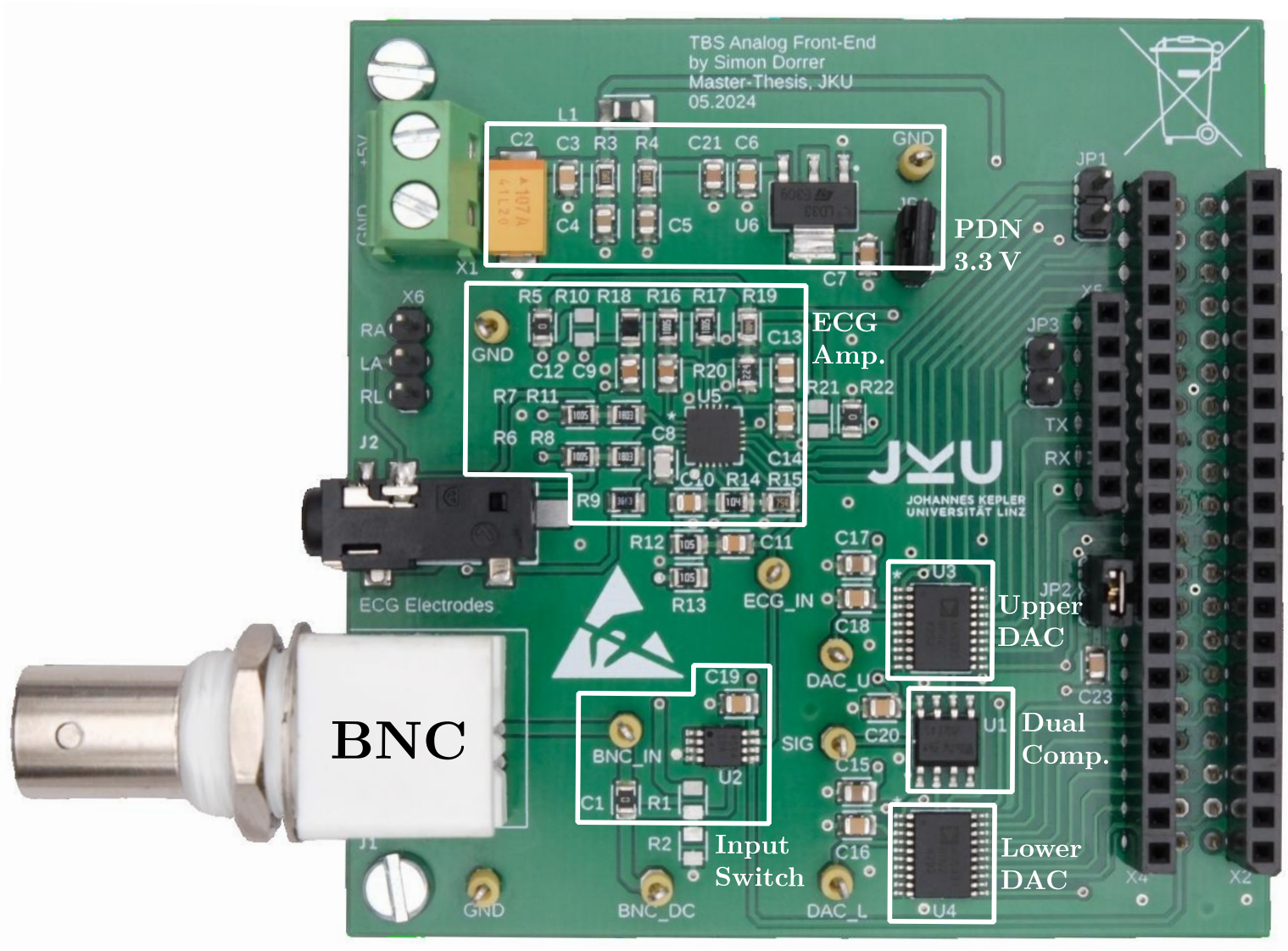
Table: Summary of implemented event-based ADCs and their architectures

PCB-Level Demonstrator

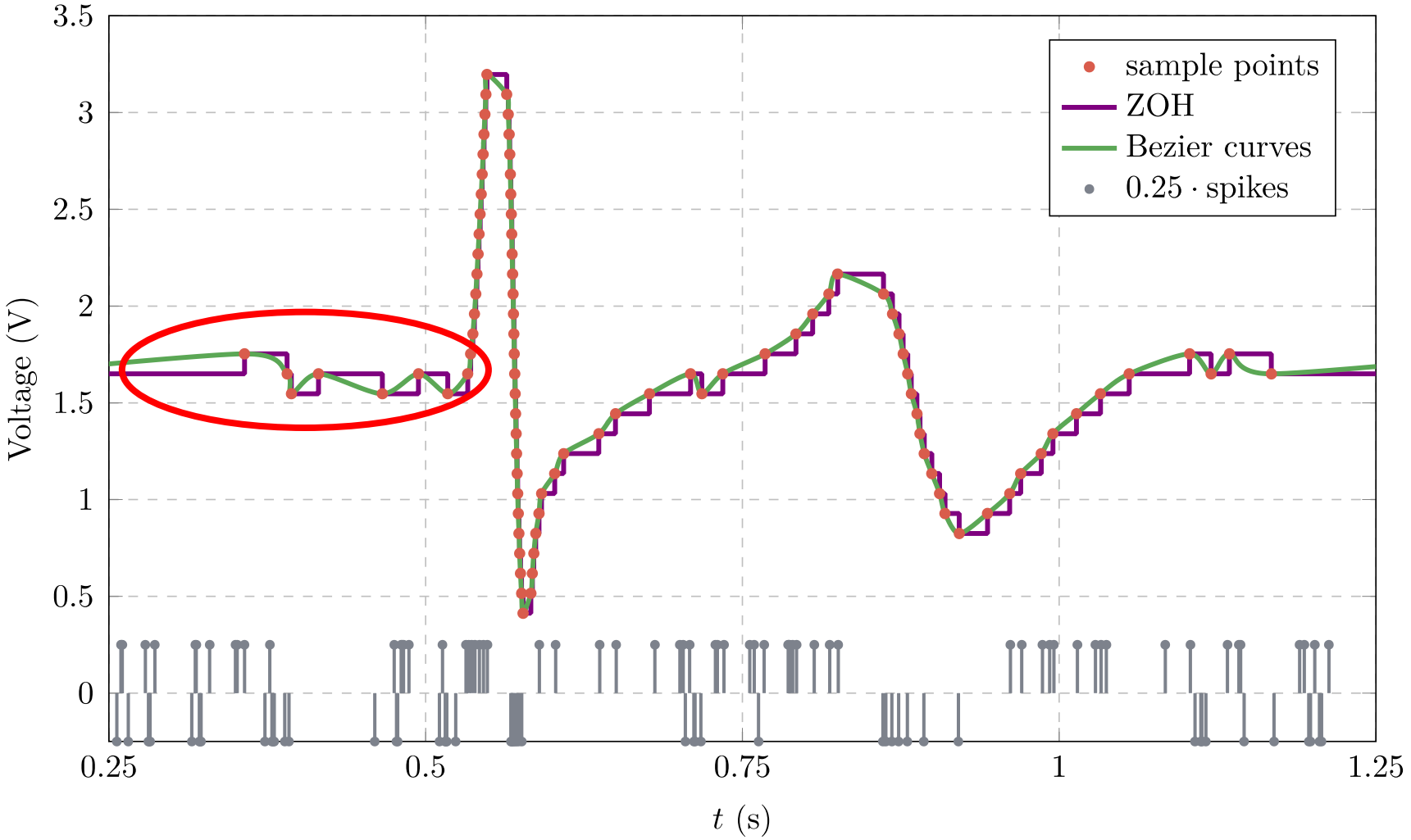
Block Diagram



Analog Front-End PCB

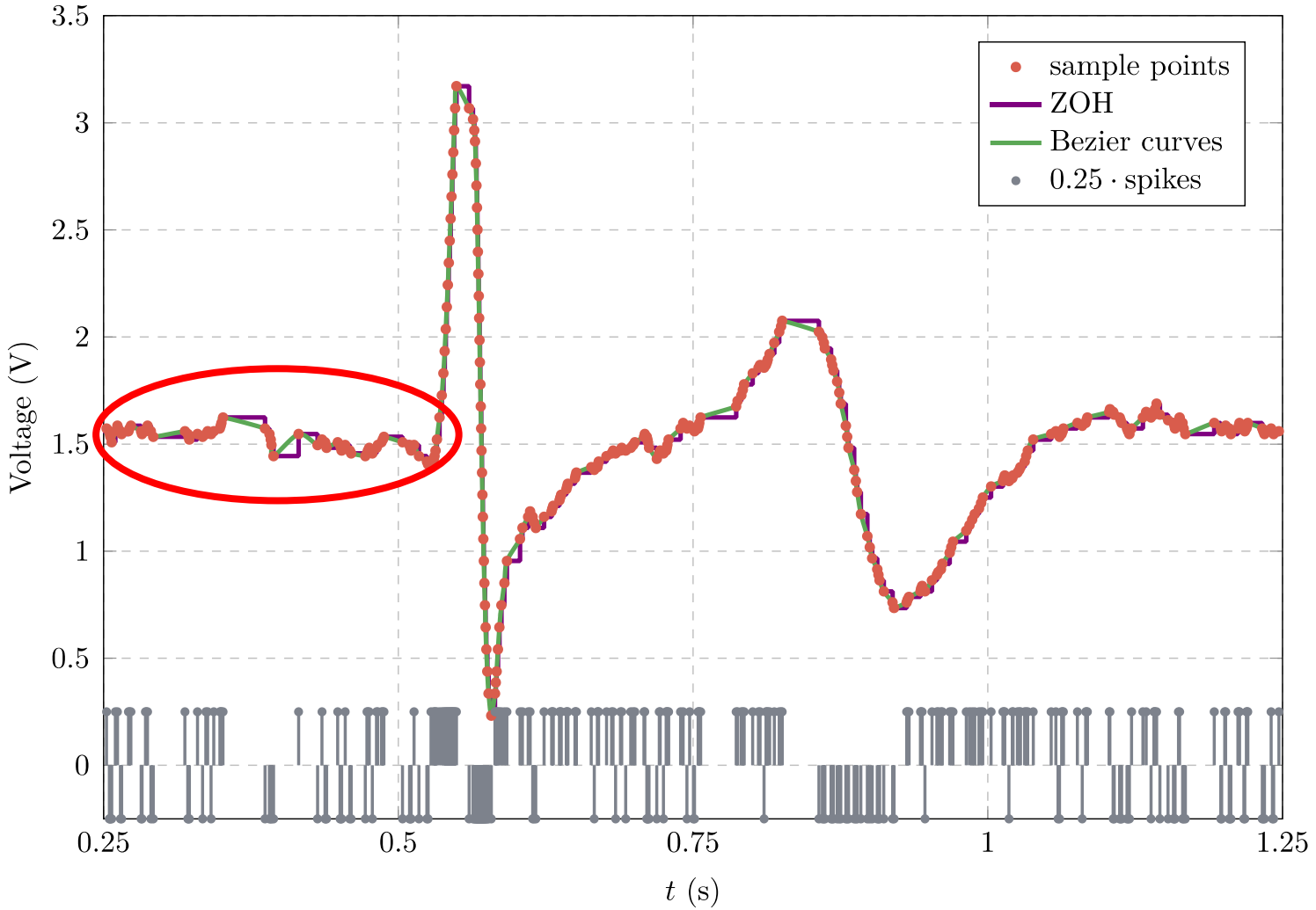


Reconstruction Results – ECG – TBS



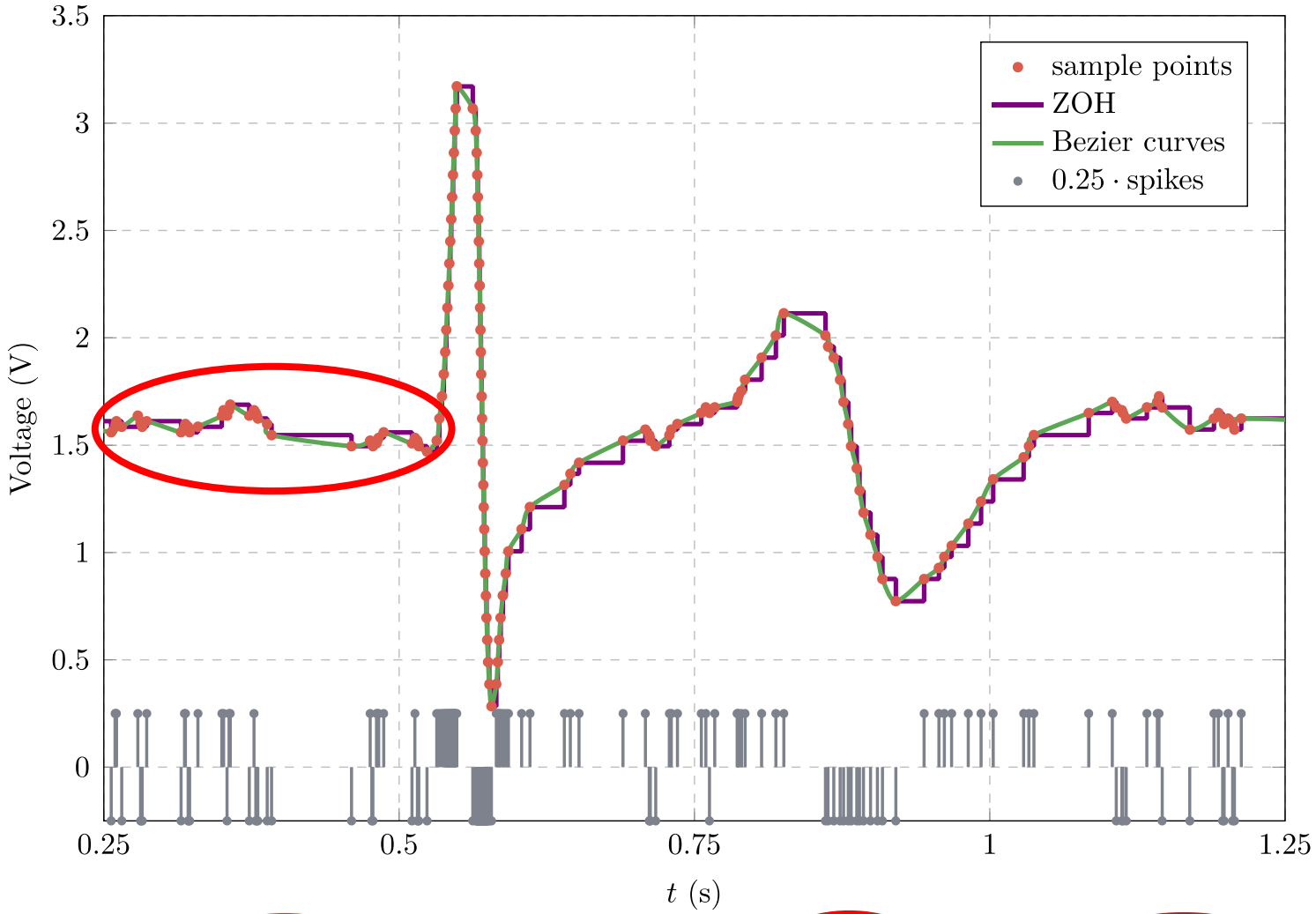
(a) TBS, $F = 5$ bits, 96 samples

Reconstruction Results – ECG – ATBS



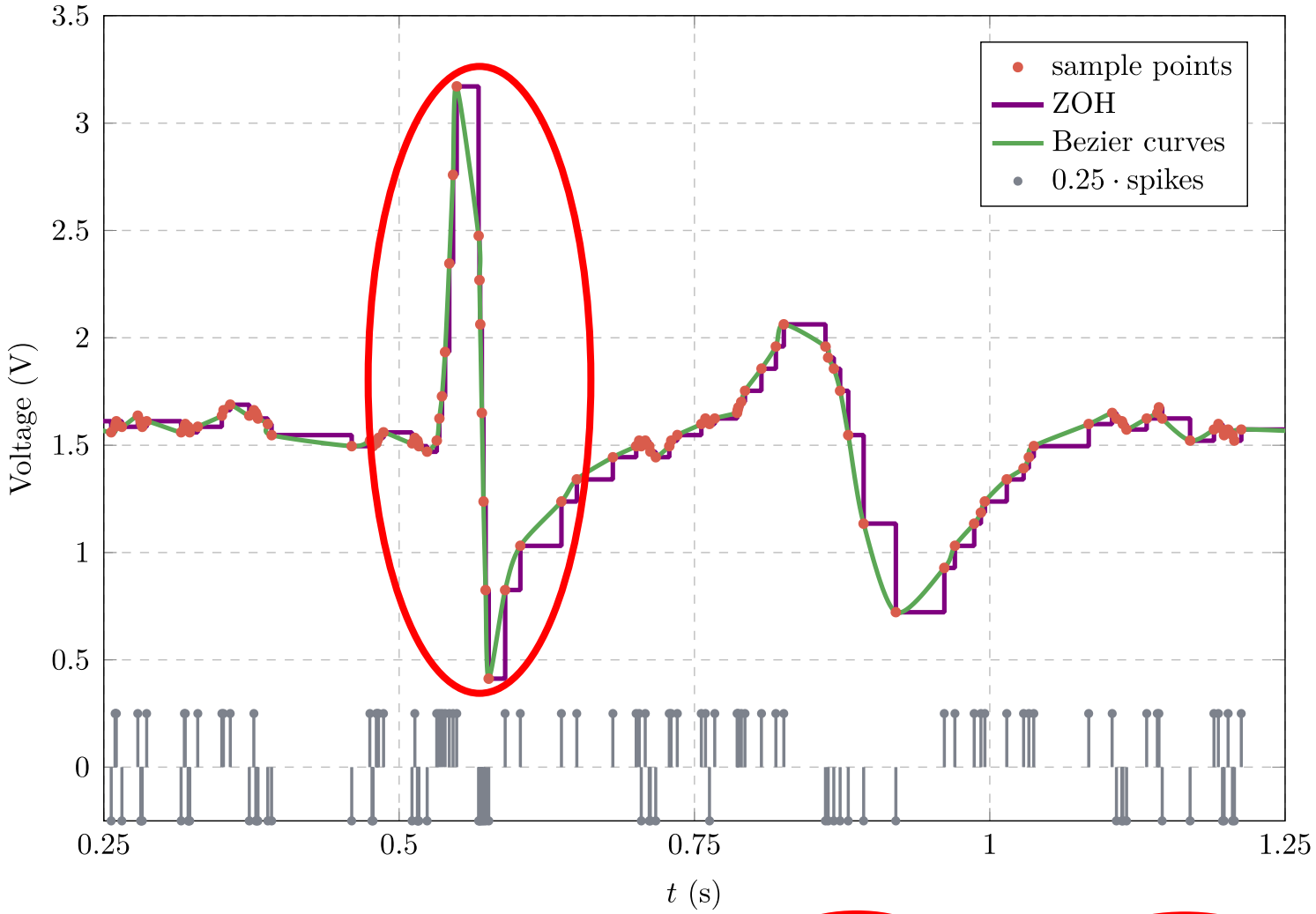
(b) ATBS, $t_{\text{win}} = 4\,\text{ms}$, $F = 5 \ldots 8\,\text{bits}$, $F_{\text{min}} = 5\,\text{bits}$, $\theta_{\text{max}} = 8\theta = 103.13\,\text{mV}$, 330 samples

Reconstruction Results – ECG – ATBS



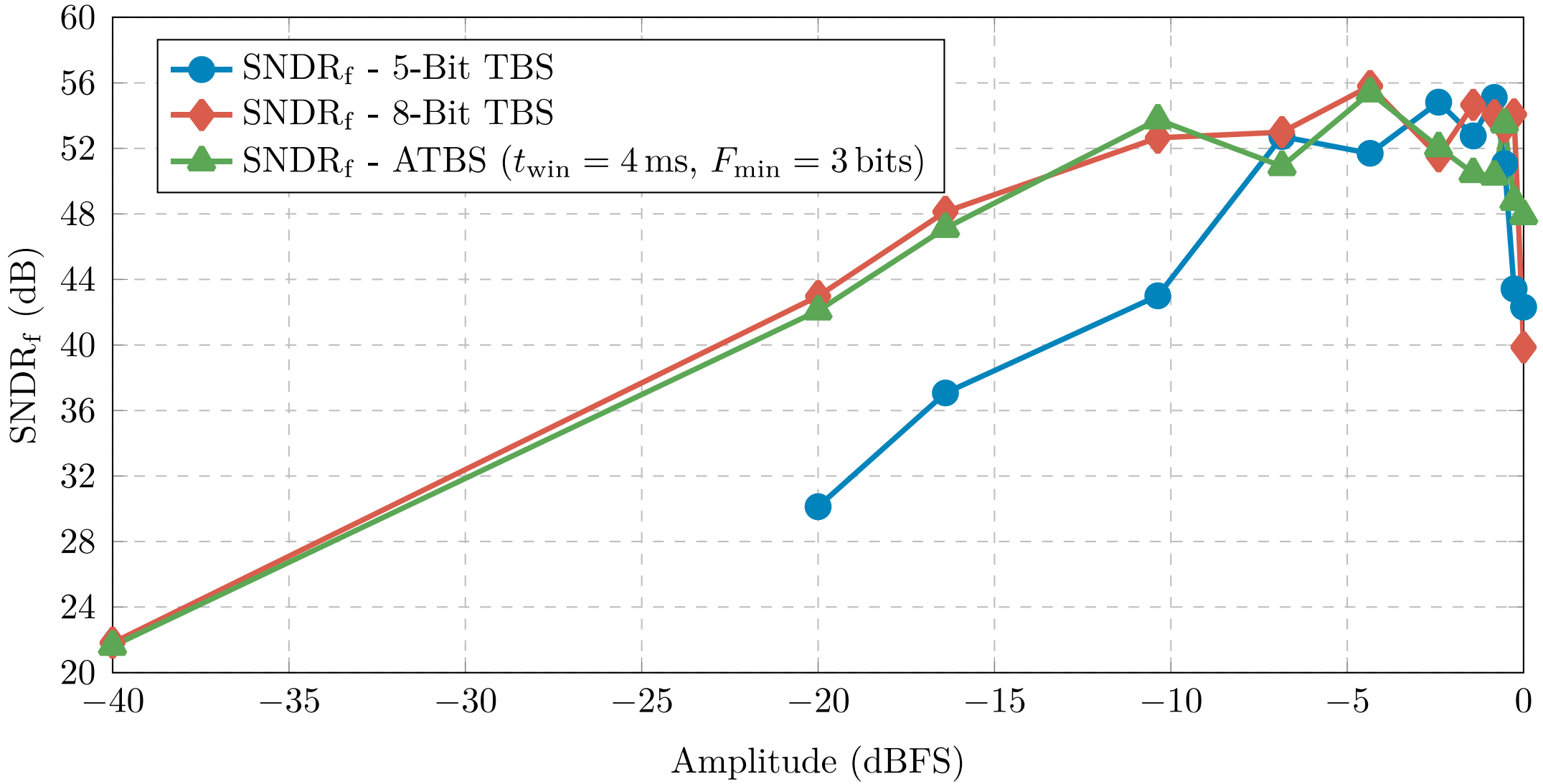
(c) ATBS, $t_{\text{win}} = 16\,\text{ms}$, $F = 5 \ldots 8\,\text{bits}$, $F_{\text{min}} = 5\,\text{bits}$, $\theta_{\text{max}} = 8\theta = 103.13\,\text{mV}$, 165 samples

Reconstruction Results – ECG – ATBS



(d) ATBS, $t_{\text{win}} = 16\,\text{ms}$, $F = 3 \ldots 8\,\text{bits}$, $F_{\text{min}} = 3\,\text{bits}$, $\theta_{\text{max}} = 32\theta = 412.5\,\text{mV}$, 118 samples

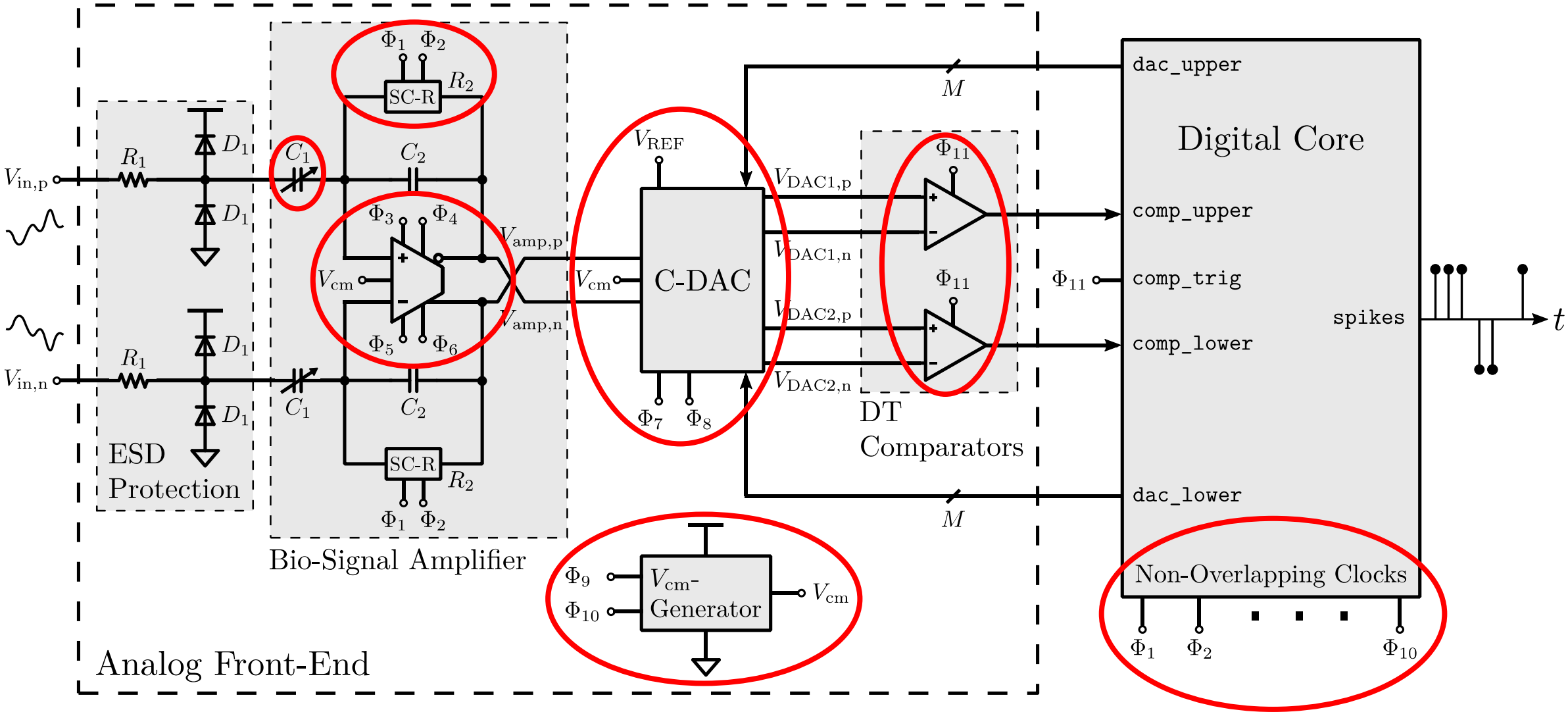
Reconstruction Results – Sine



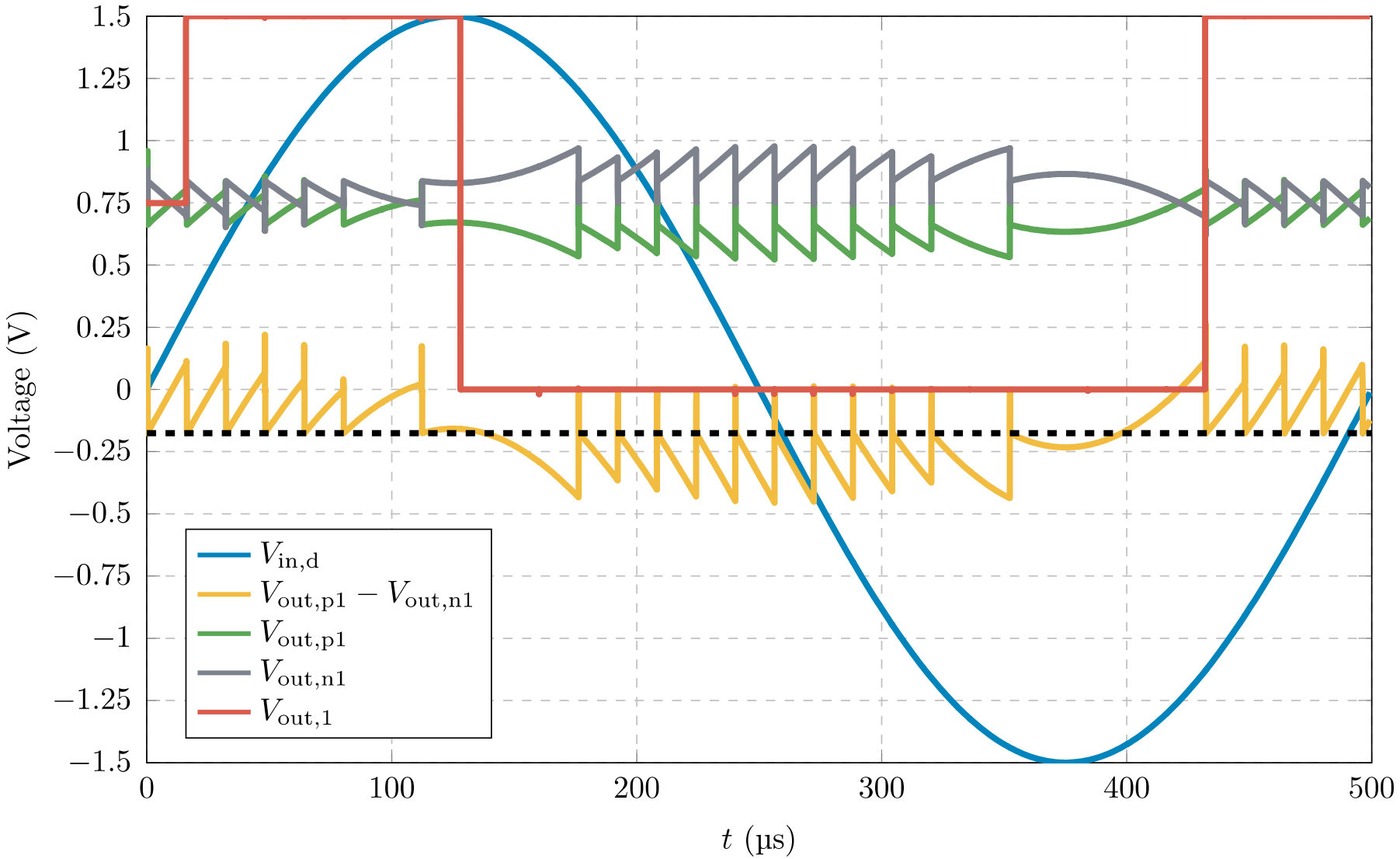
ASIC Design

Block Diagram

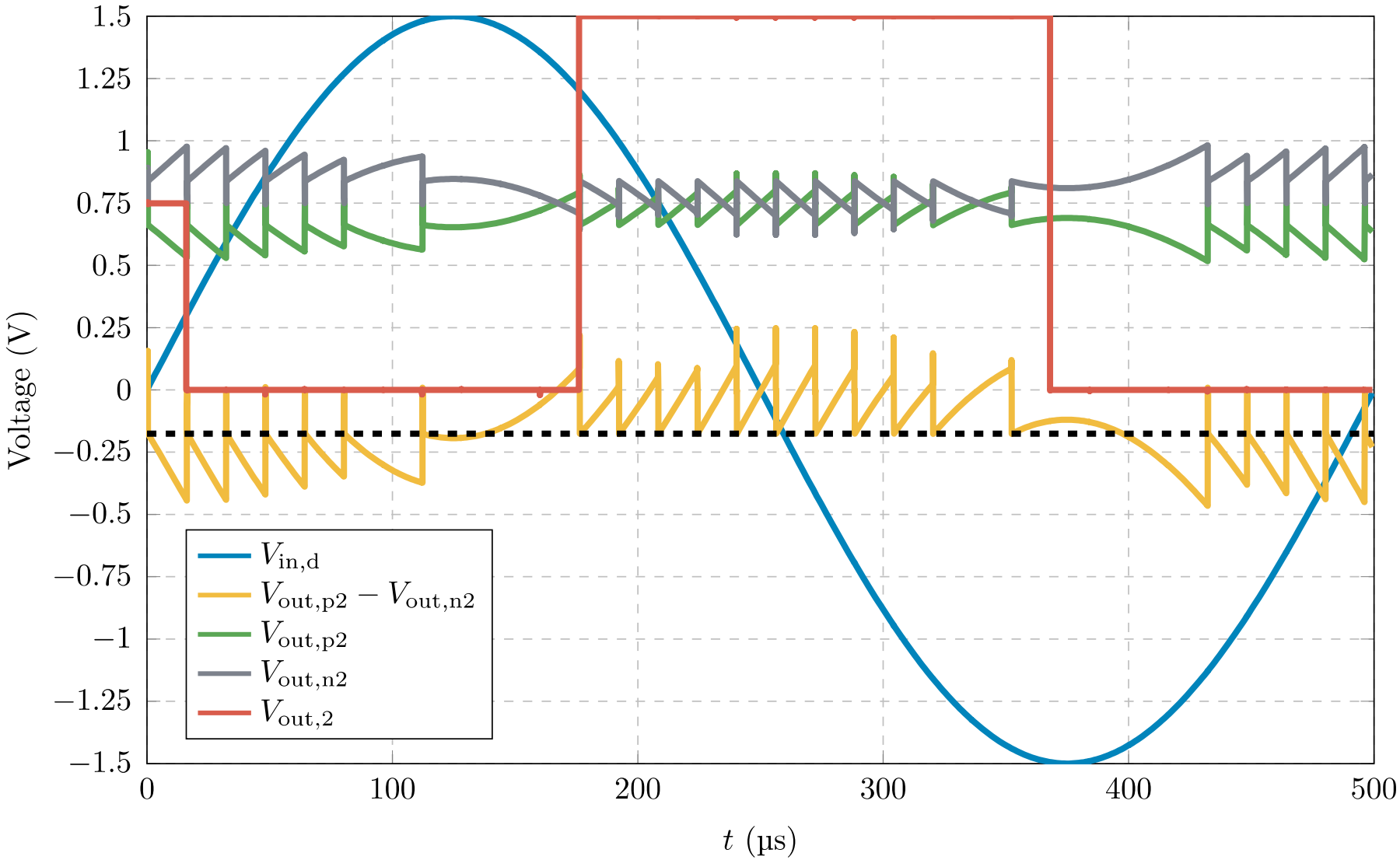
$$H_{cl}(j\omega) = -\frac{R_2}{R_1}\frac{1}{1+j\omega C_2 R_2}\frac{j\omega C_1 R_1}{1+j\omega C_1 R_1} \xrightarrow{R_2 \gg R_1} H_{cl}(j\omega) = -\frac{C_1}{C_2}\frac{j\omega C_2 R_2}{1+j\omega C_2 R_2}$$



Upper DAC + Comparator – Transient Simulation



Lower DAC + Comparator – Transient Simulation



Conclusion

Conclusion

- Achievements:
  - Important theoretical findings
  - Proof of concept with PCB-level demonstrator
  - Development of new architecture
  - Transistor-level design
- Outlook:
  - Analog Layout
  - Post-layout simulation
  - Tape-out
  - Chip verification with measurements

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