Analog Circuit Design

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Introduction

This is the material for an intermediate-level MOSFET circuit design course, held at JKU under course number 336.009 ("KV Analoge Schaltungstechnik").

The course makes heavy use of circuit simulation, using **Xschem** for schematic entry and **ngspice** for simulation. The 130nm CMOS technology **SG13G2** from IHP Microelectronics is used.

Tools and PDK are integrated in the **IIC-OSIC-TOOLS** Docker image, which will be used during the coursework.

> **Note**
>
> All course material is made publicly available on GitHub and shared under the Apache-2.0 license.

IHP's SG13G2 130nm CMOS Technology

SG13G2 is the name of a 130nm CMOS technology (strictly speaking BiCMOS) from IHP Microelectronics. It features low-voltage (thin-oxide) core MOSFET, high-voltage (thick-oxide) I/O MOSFET, various types of linear resistors, and 7 layers of Aluminium metallization (5 thin plus 2 thick metal layers). This PDK is open-source, and the complete process specification can be found at SG13G2 process specification. While we will not do layouts in this course, the layout rules can be found at SG13G2 layout rules.

For our circuit design, the most important parameters of the available devices are summarized in the following:

- **Low-voltage NMOS**: Device `sg13_lv_nmos`; operating voltage nominal $V_{DD} = 1.5\,\text{V}$, $L_{min} = 0.13\,\mu\text{m}$, $V_{th} \approx 0.5\,\text{V}$; a triple-well option for the NMOS is available.
- **Low-voltage PMOS**: Device `sg13_lv_pmos`; operating voltage nominal $V_{DD} = 1.5\,\text{V}$, $L_{min} = 0.13\,\mu\text{m}$, $V_{th} \approx -0.47\,\text{V}$.
- **High-voltage NMOS**: Device `sg13_hv_nmos`; operating voltage nominal $V_{DD} = 3.3\,\text{V}$, $L_{min} = 0.45\,\mu\text{m}$, $V_{th} \approx 0.7\,\text{V}$; a triple-well option for the NMOS is available.
- **High-voltage PMOS**: Device `sg13_hv_pmos`; operating voltage nominal $V_{DD} = 3.3\,\text{V}$, $L_{min} = 0.45\,\mu\text{m}$, $V_{th} \approx -0.65\,\text{V}$.
- **Silicided poly resistor**: Device `rsil`; $R_\square = 7\,\Omega \pm 10\%$, $\text{TC}_1 = 3100\,\text{ppm/K}$
- **Poly resistor**: Device `rppd`; $R_\square = 260\,\Omega \pm 10\%$, $\text{TC}_1 = 170\,\text{ppm/K}$
- **Poly resistor high**: Device `rhigh`; $R_\square = 1360\,\Omega \pm 15\%$, $\text{TC}_1 = -2300\,\text{ppm/K}$
- **MIM capacitor**: Device `cap_cmim`; $C' = 1.5\,\text{fF}/\mu\text{m}^2 \pm 10\%$, $\text{VC}_1 = -26\text{ppm/V}$, $\text{TC}_1 = 3.6\text{ppm/K}$, breakdown voltage $> 15\,\text{V}$

- **MOM capacitor**: The metal stack is well-suited for MOM capacitors due to 5 thin metal layers, but no primitive capacitor device is available at this point.

Schematic Entry Using Xschem

Xschem is an open-source schematic entry tool with emphasis on integrated circuits. For up-to-date information of the many features of Xschem and the basic operation of it please look at the available online documentation. Usage of Xschem will be learned with the first few basic examples, essentially using a single MOSFET. The usage model of Xschem is that the schematic is hierarchically drawn, and the simulation and evaluation statements are contained in the schematics. Further, Xschem offers embedded graphing, which we will mostly use.

Circuit Simulation Using ngspice

ngspice is an open-source circuit simulator with SPICE dependency (Nagel 1975). Besides the usual simulated types like `op` (operating point), `dc` (dc sweeps), `tran` (time-domain), or `ac` (small-signal frquency sweeps), ngspice offers a script-like control interface, where many different simulation controls and result evaluations can be done. For detailed information please refer to the latest online manual.

Integrated IC Design Environment (IIC-OSIC-TOOLS)

In order to make use of the various required components (tools like Xschem and ngspice, PDKs like SG13G2) easier, we will use the **IIC-OSIC-TOOLS**. This is a pre-compiled Docker image which allows to do circuit design on a virtual machine on virtually any type of computing equipment (personal PC, Raspberry Pi, cloud server) on various operating systems (Windows, macOS, Linux). For further information like installed tools, how to setup a VM, etc. please look at IIC-OSIC-TOOLS GitHub page.

> **Tip**
>
> Please make sure to receive information about your personal VM access ahead of the course start.

Experienced users can install this image on their personal computer, for JKU students the IIC will host a VM on our compute cluster and provide personal login credentials.

> **Note**
>
> In this course, we assume that students have a basic knowledge of Linux and how to operate it using the terminal. If you are not yet familiar with Linux (which is basically a must when doing integrated circuit design as many tools are only available on Linux), then please check out a Linux introductory course or tutorial online, there are many

ressources available.

First Steps

In this first chapter we will learn to use Xschem for schematic entry, and how to operate the ngspice SPICE simulator for circuit simulations. Further, we will make ourself familiar with the transistor and other passive components available in the IHP Microelectronics SG13G2 technology. While this is strictly speaking a BiCMOS technology offering MOSFETs as well as SiGe HBTs, we will use it as a pure CMOS technology.

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET)

In this course, we will not dive into semiconductor physics and derive the device operation bottom-up starting from a fundamental level governed by quantum mechanics. Instead, we will treat the MOSFET as a macroscopic by assuming we have a 4-terminal device, and the performance of this device regarding its terminal voltages and currents we will largely derive from the simulation model.

The circuit symbol that we will use for the n-channel MOSFET is shown in Figure 1, and for the p-channel MOSFET it is shown in Figure 2. A control voltage between gate ("G") and source ("S") causes a current to flow between drain ("D") and source. The MOSFET is a 4-terminal device, so the bulk ("B") can also control the drain-source current flow. Often, the bulk is connected to source, and then the bulk terminal is not shown to declutter the schematics.

Note

Strictly speaking is the drain-source current of a MOSFET controlled by the voltage between gate and bulk and the voltage between drain and source. Since bulk is often connected to source anyway, and many circuit designers historically were already familiar with the operation of the bipolar junction transistor, it is common to consider the gate-source voltage (besides the drain-source voltage) as the controlling voltage. This focus on gate-source implies that the source is special compared to the drain. In a typical physical MOSFET, however, the drain and source are constructed exactly the same, and which terminal is drain, and which terminal is source, is only determined by the applied voltage potentials, and can change dynamically during operation (think of a MOSFET operating as a switch... which side is the drain, which side is the source?). Unfortunately, this focus on a "special" source has made its way into some MOSFET compact models. The model that is used in SG13G2 luckily uses the PSP model, which is formulated symmetrically with regards to drain and source, and is thus very well suited for analog and RF circuit design. For a detailed understanding of the PSP model please refer to the model documentation.

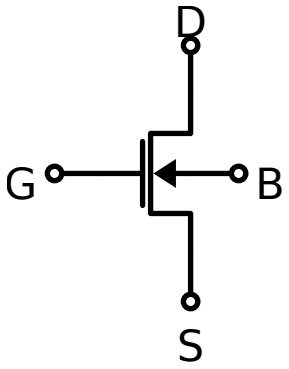

Figure 1: Circuit symbol of n-channel MOSFET.

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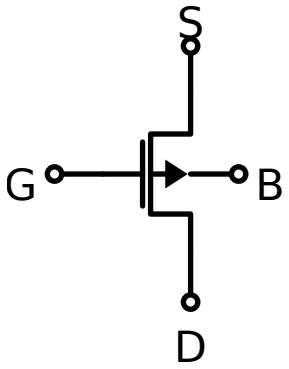

Figure 2: Circuit symbol of p-channel MOSFET.

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For hand calculations and theoretical discussions we will use the following simplified large-signal model, shown in Figure 3. A current source I_{DS} models the current flow between drain and source, and it is controlled by the three control voltages V_{GS}, V_{DS}, and V_{SB}. Note that in this way (since $I_{\mathrm{DS}} = f(V_{\mathrm{DS}})$) also a resistive behavior between D and S can be modelled. In case that B and S are shorted then simply $V_{\mathrm{SB}} = 0$.

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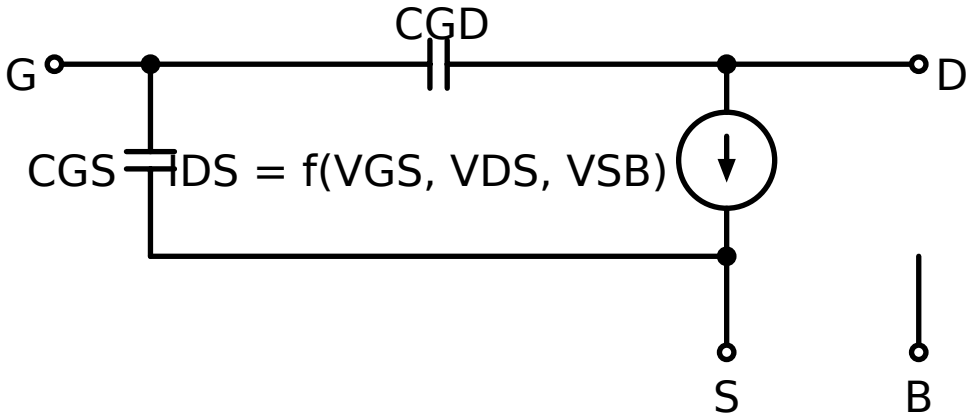

Figure 3: The MOSFET large-signal model.

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In an ideal MOSFET no dc current is flowing into the gate, the behavior is purely capacitive. We model this by two capacitors: $C_{GG} = C_{GS} + C_{GD}$ is the total capacitance when looking into the gate of the MOSFET. C_{GS} is usually the dominant capacitance, and C_{GD} models the capacitive feedback between D and G, usually induced by a topological overlap capacitance in the physical construction of the MOSFET. This capacitance is often small compared to C_{GS}, but in situations where we have a large voltage swing at the drain this capacitance will be affected by the Miller effect. In hand calculations we will often set $C_{GD} = 0$.

> **Note**
>
> The bulk connection in Figure 3 seems floating as we only consider it a control terminal, where the potential difference between source and bulk influences the behaviour of the MOSFET. However, we do not consider resistive or capacitive effects associated with this node, which is of course a gross simplification, but nevertheless one we will make in this course.

Now, as we are skipping the bottom-up approach of deriving the MOSFET large-signal behaviour from basic principles, we need to understand the behaviour of the elements of the large-signal model in Figure 3 by using a circuit simulator and observing what happens. And generally, a first step in any new IC technology should be to investigate basic MOSFET performance, by doing simple dc sweeps of V_{GS} and V_{DS} and looking at I_{DS} and other large- and small-signal parameters.

As a side note, the students who want to understand MOSFET behaviour from a physical angle should consult the MOSFET chapter from the JKU course "Design of Complex Integrated Circuits" (VL 336.048). A great introduction into MOSFET operation and fabrication is given in (Hu 2010), which is available freely online and is a recommended read. A very detailed description of the MOSFET (leaving usually no question unanswered) is provided in (Tsividis and McAndrew 2011).

Now, in order to get started, basic Xschem testbenches are prepared, and first simple dc sweeps of various voltages and currents will be done. But before that, please look at the import note below!

> **!** Important
>
> Throughout this material, we will stick to the following notations:
>
> - A **dc quantity** is shown with an upper-case letter with upper-case subscripts, like V_{GS}.
> - Double-subscripts denote **dc sources**, like V_{DD} and V_{SS}.
> - An **ac (small-signal) quantity** is a lower-case letter with a lower-case subscript, like g_{m}.
> - A **total quantity** (dc plus ac) is shown as a lowercase letter with upper-case subscript, like i_{DS}.
> - A upper-case letter with a lower-case subscript is used to denote **RMS quantities**, like I_{ds}.

Large-Signal MOSFET Model

We start with an investigation into the large-signal MOSFET model shown in Figure 3 by using the simple testbench for the LV NMOS shown in Figure 4.

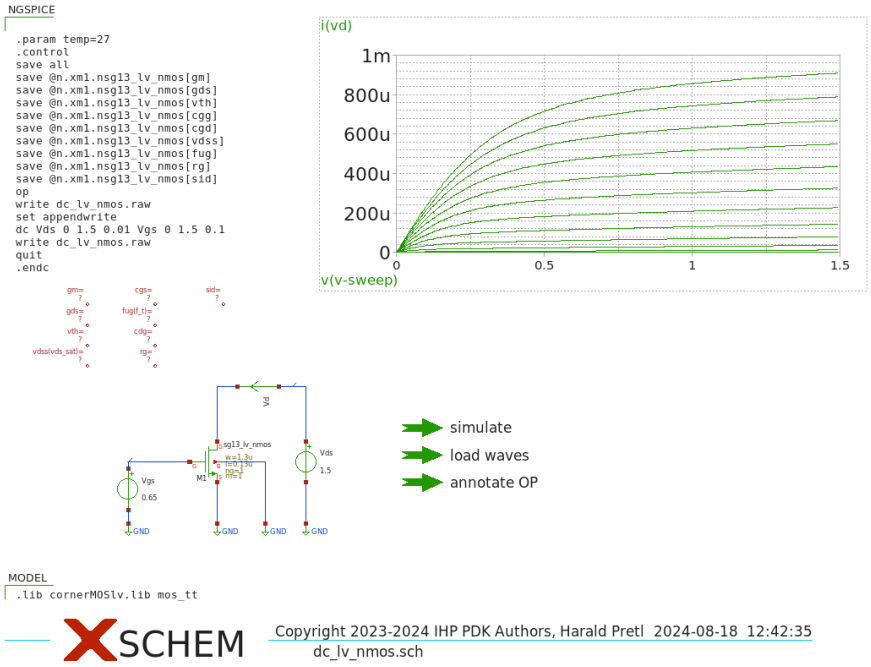

Figure 4: Testbench for NMOS dc sweeps.

Exercise

Please try to execute the following steps and answer these questions:

1. Get the LV NMOS testbench (available at https://github.com/iic-jku/analog-circuit-design/blob/main/xschem/dc_lv_nmos.sch) working in your IIC-OSIC-TOOLS environment.
2. Make yourself familiar with Xschem (change the schematic in various ways, run a simulation, graph the result).
3. Make youself familiar with ngspice (run various simulations, save nets and parameters, use the embedded Xschem graphing, explore the interactive ngspice shell to look at MOSFET model parameters).
4. Explore the LV NMOS `sg13_lv_nmos`:
    1. How is I_{DS} affected by V_{GS} and V_{DS}?
    2. Change W and L of the MOSFET. What is the impact on the above parameters? Can you explain the variations?
    3. When looking at the model parameters in ngspice, you see that there is a C_{GD} and a C_{DG}. Why is this, what could be the difference? Sometimes these capacitors show a negative value, why?
5. Build testbenches in Xschem for the LV PMOS, the HV NMOS, and the HV PMOS. Explore the different results.
    1. For a given W and L, which device provides more drain current? How are the capacitances related?
    2. If you would have to size an inverter, what would be the ideal ratio of W_p/W_n? Will you exactly design this ratio, or are the reasons to deviate?
    3. There are LV and HV MOSFETs, and you investigated the difference in performance. What is the rationale when designing circuits for selection either an LV type, and when to choose an HV type?
6. Build a test bench to explore the body effect, start with LV NMOS.
    1. What happens when $V_{BS} \neq 0$?

Small-Signal MOSFET Model

As you have seen in the previous investigations, the large-signal model of Figure 3 describes the behaviour of the MOSFET across a wide range of voltages applied at the MOSFET terminals. Unfortunately, for hand analysis dealing with a nonlinear model is close to impossible, at the very least it is quite tedious.

However, for many practical situations, we bias a MOSFET with a set of dc voltages applied to its terminal, and only apply small signal excursions during operation. If we do this, we can linearize the large-signal model in this dc operating point, and resort to a small-signal model which can be very useful for hand calculations. Many experienced designers analyze their circuits by doing these kind of hand calculations and describing the circuit analytically, which

is a great way to understand fundamental performance limits and relationships between parameters.

We will use the small-signal MOSFET model shown in Figure 5 for this course. The current-source $i_{ds} = g_m v_{gs}$ models the drain current as a function of v_{gs}, and the resistor g_{ds} models the dependency of the drain current by v_{ds}. The drain current dependency on the source-bulk voltage (the so-called "body effect") is introduced by the current source $i_{ds} = g_{mb} v_{sb}$.

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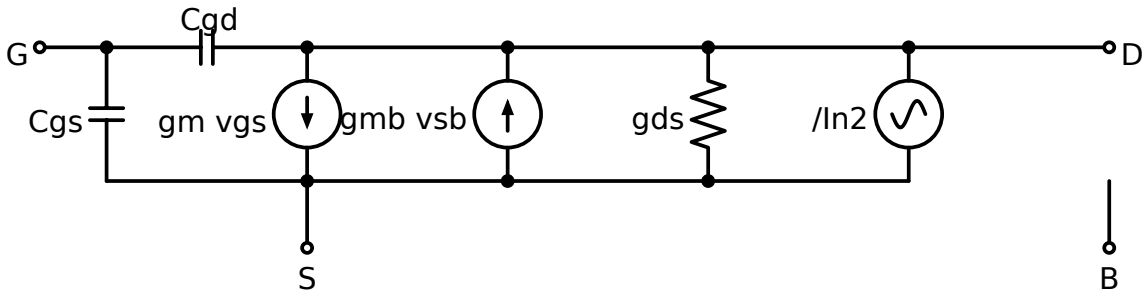


Figure 5: The MOSFET small-signal model.

Source: Article Notebook

As any electronic device the MOSFET introduces noise into the circuit. In this course we will only consider the drain-source current noise of the MOSFET, given by $\overline{I_n^2} = 4kT\gamma g_{d0}$ ($\overline{I_n^2}$ is the power-spectral density of the noise in A^2/Hz; k is the Boltzmann constant; T is the absolute temperature; γ is a parameter in simplified theory changing between $\gamma = 2/3$ in saturation and $\gamma = 1$ for triode operation; g_{d0} is equal to g_m in saturation and g_{ds} in triode).

> **Note**
>
> Sometimes we will refer to different operating modes of the MOSFET like "saturation" or "triode". Generally speaking, when the drain-source voltage is small, then the MOSFET acts as a resistor, and this mode of operation we call "triode" mode. When the drain-source voltage is increased, at some point the drain-source current saturates and is no longer a strong function of the drain-source voltage. This mode is called "saturation" mode. As you can see in the large-signal investigations, these transitions happen gradually, and it is difficult to define a precise point where one operating mode switches to the other one. In this sense we use terms like "triode" and "saturation" only in an approximative sense.

Now we need to see how the small-signal parameters seen in Figure 5 can be investigated and estimated using circuit simulation.

Exercise

Please try to execute the following steps and answer the following questions:

1. Reuse the LV NMOS testbench (available at https://github.com/iic-jku/analog-circuit-design/blob/main/xschem/dc_lv_nmos.sch).
2. Explore the LV NMOS `sg13_lv_nmos`:
    1. How are g_m and g_ds changing when you change the dc node voltages?
    2. What is the ratio of g_m to g_mb? What is the physical reason behind this ratio (you might want to revisit MOSFET device physics at this point)?
    3. Take a look at the device capacitances C_gs and C_gd. Why are they important? What is the relation to f_T? *Note: f_T is the transit frequency where the current gain of the MOSFET drops to 1, and can be approximated by $2\pi f_\mathrm{T} = g_\mathrm{m}/C_\mathrm{gg}$.*
    4. Look at the drain noise current according to the MOSFET model and compare with a hand calculation of the noise. In the noise equation there is the factor γ, which in triode is $\gamma = 1$ and in saturation is $\gamma = 2/3$ according to basic text books. Which value of γ are you calculating? Why might it be different?
3. Go back to your testbench for the LVS PMOS `sg13_lv_pmos`:
    1. What is the difference in g_m, g_ds, and other parameters between the NMOS and the PMOS? Why could they be different?

Conclusion

Congratulations for making it thus far! By now you should have a solid grasp of the tool handling of Xschem and ngspice, and you should be familiar with the large- and small-signal operation of both NMOS and PMOS, and the parameters describing these behaviours. If you feel you are not sufficiently fluent in these things, please go back to the beginning of Section and revisit the relevant sections, or dive into further reading about the MOSFET operation, like in (Hu 2010).

Transistor Sizing Using gm/ID Methodology

When designing integrated circuits it is an important question how to select various parameters of a MOSFET, like W, L, or the bias current I_D. In comparison to using discrete components in PCB design, or also compared to a bipolar junction transistor (BJT), we have these degrees of freedom, which make integrated circuit design so interesting.

Often, transistor sizing in entry-level courses is based on the square-law model, where a simple analytical equation for the drain current can be derived. However, in nanometer CMOS, the MOSFET behaviour is much more complex than these simple models. Also, this

highly simplified derivations introduce concepts like the threshold voltage or the overdrive voltage, which are interesting from a theoretical viewpoint, but bear little practical use.

> **Note**
>
> One of the many simplifactions of the square-law model is that the mobility of the charge carriers is assumed constant (it is not). Further, the existance of a threshold voltage is assumed, but in fact this voltage is just existing given a certain definition, and depending on definition, its value changed. In addition, in nm CMOS, the threshold voltage is a function on many thing, like W and L.

An additional shortcoming of the square-law model is that it is only valid in strong inversion, i.e. for large V_{GS} where the drain current is dominated by the drift current. As soon as the gate-source voltage gets smaller, the square-law model breaks, as the drain current component based on diffusion currents gets dominant. Modern compact MOSFET models (like the PSP model used in SG13G2) use hundreds of parameters and fairly complex equations to somewhat properly describe MOSFET behaviour over a wide range of parameters like W, L, and temperature. A modern approach to MOSFET sizing is thus based on the thought to use exactly these MOSFET models, characterize them, put the resulting data into tables and charts, and thus learn about the complext MOSFET behaviour and use it for MOSFET sizing.

Being a well-established approach we select the $g_{\mathrm{m}}/I_{\mathrm{D}}$ methodology introduced by P. Jespers and B. Murmann in (Jespers and Murmann 2017). A brief introduction is available here as well.

The $g_{\mathrm{m}}/I_{\mathrm{D}}$ methodology has the huge advantage that is catches MOSFET behavior quite accurately over a wide range of operating conditions, and the curves look very similar for pretty much all CMOS technologies, form micrometer bulk CMOS down to nanometer FinFET devices. Of course the absolute values change, but the method applies universally.

MOSFET Characterization Testbench

In order to get the required tabulated data we use a testbench in Xschem which sweeps the terminal voltages, and records various large- and small-signal parameters, which are then stored in large tables. The testbench for the LV NMOS is shown in Figure 6, and the TB for the LV PMOS is shown in Figure 7.

We will use Jupyter notebooks to inspect the resulting data, and interpret some important graphs. This will greatly help to understand the MOSFET behaviour.

NMOS Characterization

First, we will start looking at the LV NMOS. In Section we have the corresponding graphs for the LV PMOS. In this lecture, we will only use the LV MOSFETs. While there are also the HV types available, they are mainly used for high-voltage circuits, like circuits

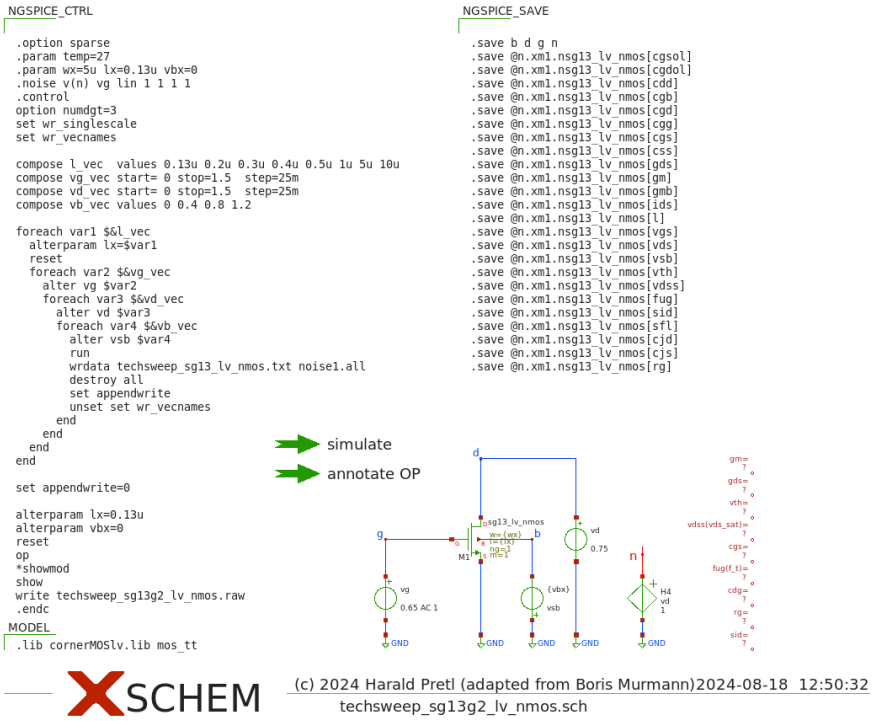


Figure 6: Testbench for LV NMOS $g_\mathrm{m}/I_\mathrm{D}$ characterization.

connecting to the outside world. Here, we only will design low-voltage circuits running at a nominal supply voltage of 1.5 V, so only the LV types are of interest to us.

The first import graph is the plot of $g_\mathrm{m}/I_\mathrm{D}$ and f_T versus the gate-source voltage V_GS. First let us answer the question why $g_\mathrm{m}/I_\mathrm{D}$ is a good parameter to look at, and actually this is also the central parameter in the $g_\mathrm{m}/I_\mathrm{D}$ methodology. In many circuits that are biased in class-A (i.e., with a constant quiescent current that is larger than the largest signal excursion, see biasing) we want to get a large amplification from a MOSFET, which corresponds to a large g_m. We want this by spending the minimum biasing current possible (ideally zero), as we always design for minimum power consumption. Thus, a high $g_\mathrm{m}/I_\mathrm{D}$ ratio is good.

> **Note**
>
> Designing for minimum power consumption is pretty much always mandated. For battery-operated equipment it is a paramount requirement, but also in other equipment electrical energy consumption is a concern, and often severly limited by the cooling capabilities of the electrical system.

However, as can be seen in the below plot, there exists a strong and unfortunate trade-off with device speed, characterized here by the transit frequency f_T. It would be ideal if there exists a design point where we get high transconductance per bias current concurrently to having the fastest operation, but unfortunately, this is clearly not the case. The $g_\mathrm{m}/I_\mathrm{D}$ peaks for $V_\mathrm{GS} < 0.3\,\mathrm{V}$, and the highest speed we get at $V_\mathrm{GS} \approx 1.2\,\mathrm{V}$. The dashed vertical line plots

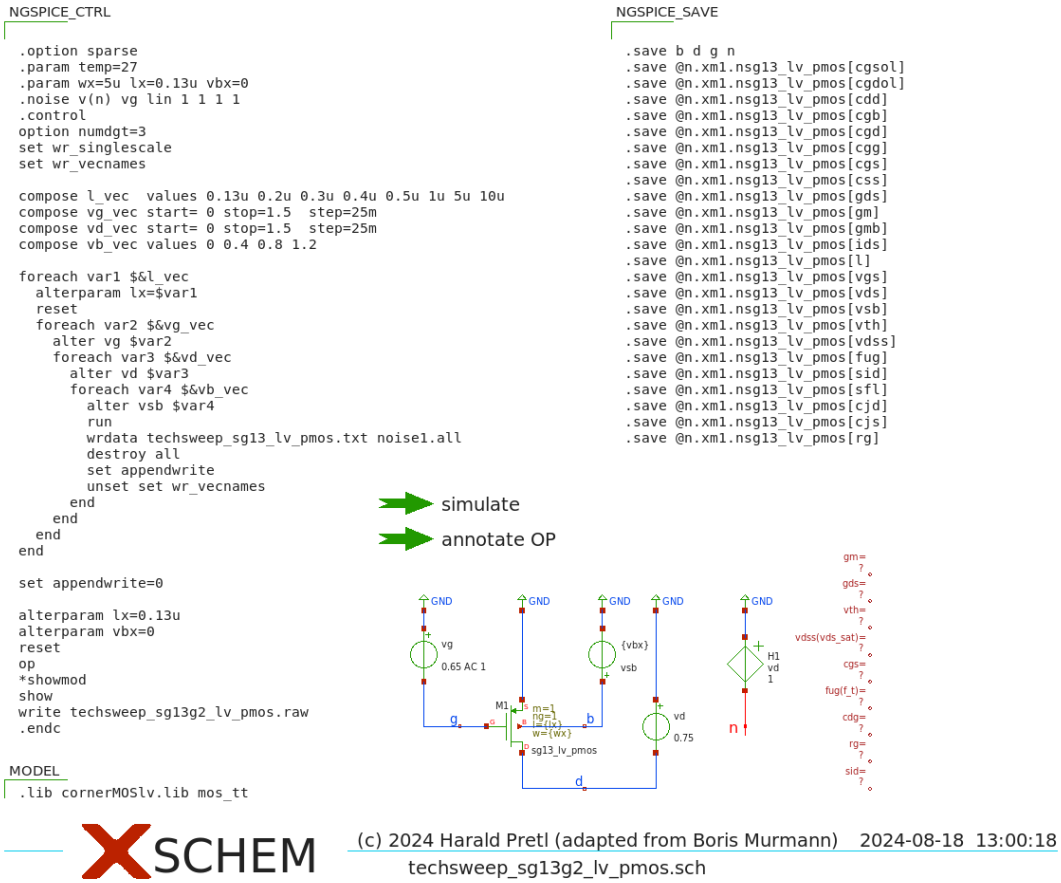


Figure 7: Testbench for LV PMOS $g_\mathrm{m}/I_\mathrm{D}$ characterization.

the nominal threshold voltage, as you can see in this continuum of parameter space, it marks not a particularly special point.

Note that

$$\frac{g_\mathrm{m}}{I_\mathrm{D}} = \frac{1}{nV_\mathrm{T}} \tag{1}$$

for a MOSFET in weak inversion (i.e., small gate-source voltage). n is the subthreshold slope, and $V_\mathrm{T} = kT/q$ which is 25.8 mV at 300 K. We thus have $n \approx 1.38$ for this LV NMOS, which falls nicely into the usual range for n of 1.3 to 1.5 for bulk CMOS (FinFET have n very close to 1).

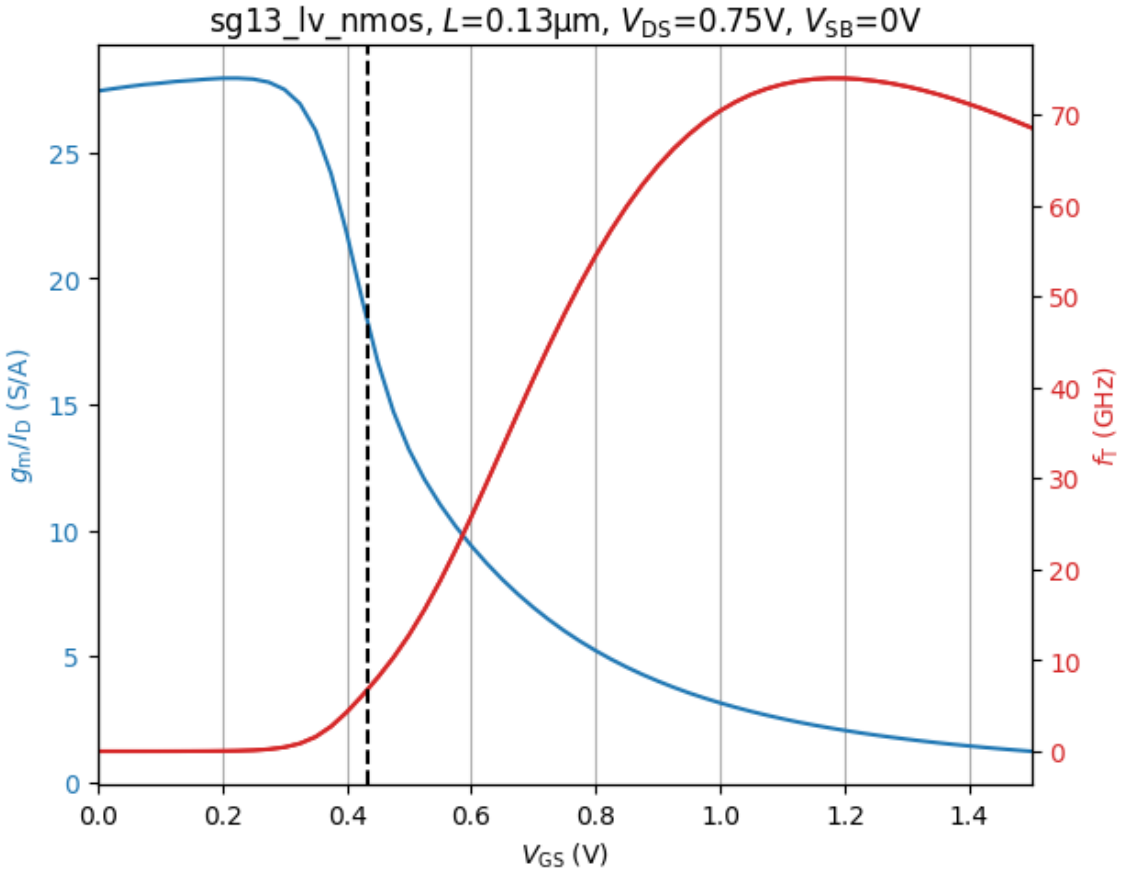
For the classical square-law model of the MOSFET in strong inversion, $g_\mathrm{m}/I_\mathrm{D}$ is given as

$$\frac{g_\mathrm{m}}{I_\mathrm{D}} = \frac{2}{V_\mathrm{GS} - V_\mathrm{th}} = \frac{2}{V_\mathrm{od}} \tag{2}$$

with V_th the threshold voltage and V_od the so-called "overdrive voltage."

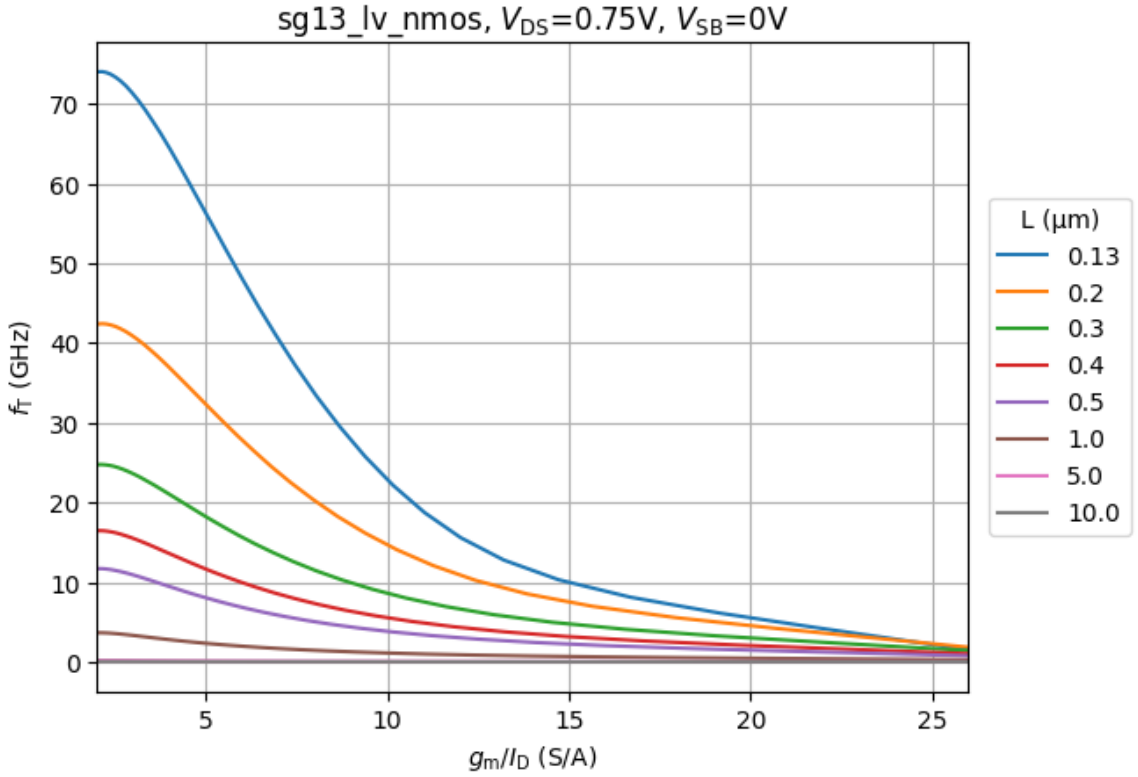
> **Note**
>
> Why are we so often using 300 K for a typical condition? As this corresponds to roughly 27°C, this accounts for some self heating compared to otherwise usual room temperatures. Further, engineers like round numbers which are easy to remember, so 300 K is used as a proxy for room temperature.

As we can also see from belows plot, the peak transit frequency of the LV NMOS is about 75 GHz, which allows building radio-frequency circuits up to ca. $f_\mathrm{T}/10 = 7.5$ GHz, which is a respectible number. It is no coincidence, that the transition for RF design in the GHz-range switched from BJT-based technologies to CMOS roughly in the timeframe when 130nm CMOS became available (ca. 2000).



Source: Article Notebook

The following figure plots f_T against $g_\mathrm{m}/I_\mathrm{D}$ for several different L. As you can see, device speeds maximizes for a low $g_\mathrm{m}/I_\mathrm{D}$ and a short L. As you can see the drain-source voltage is kept at $V_\mathrm{DS} = 0.75\,\mathrm{V} = V_\mathrm{DD}/2$, which is a typical value keeping the MOSFET in saturation across the characterization sweeps. Further, the source-bulk voltage is kept at $V_\mathrm{SB} = 0\,\mathrm{V}$, which means bulk and source terminals are connected.



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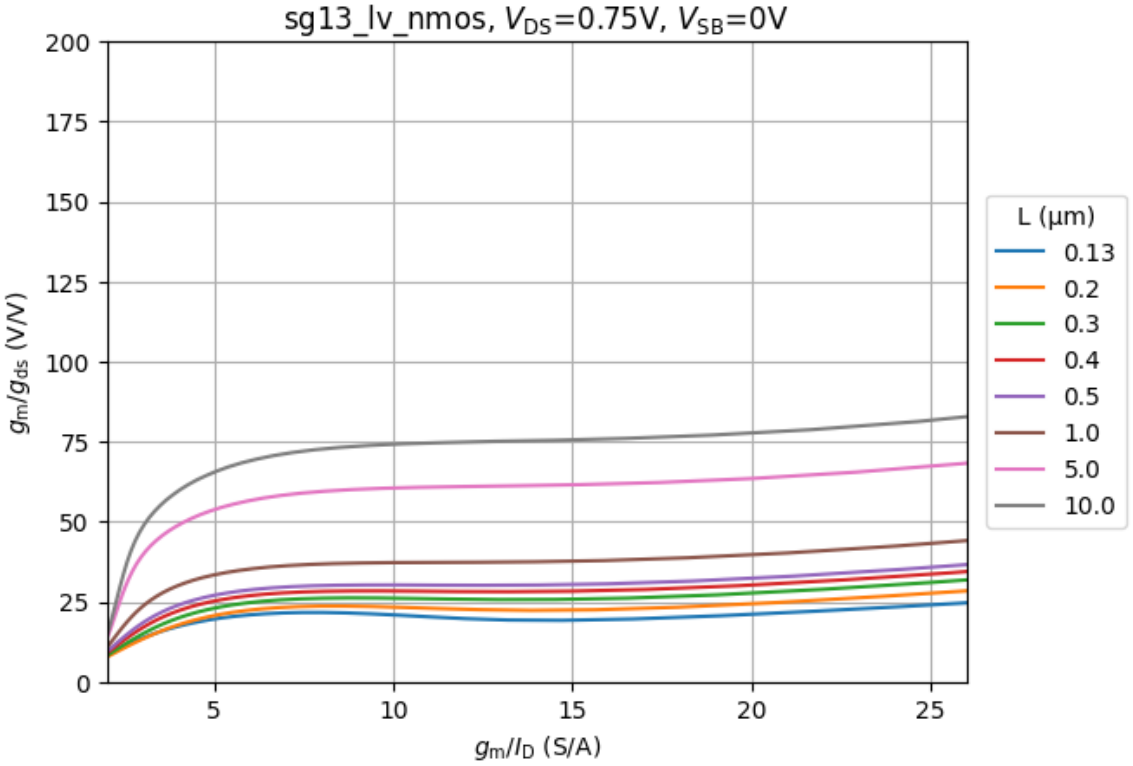
The next plot shows the ratio of g_m/g_{ds} versus g_m/I_D. The ratio g_m/g_{ds} is the so-called **"self-gain"** of the MOSFET, and shows the maximum voltage gain we can achieve in a single transistor configuration. As one can see the self gain increases for increasing L, but this also gives a slower transistor, so again there is a trade-off. This plot allows us to select the proper L of a MOSFET if we know which amount of self gain we need.



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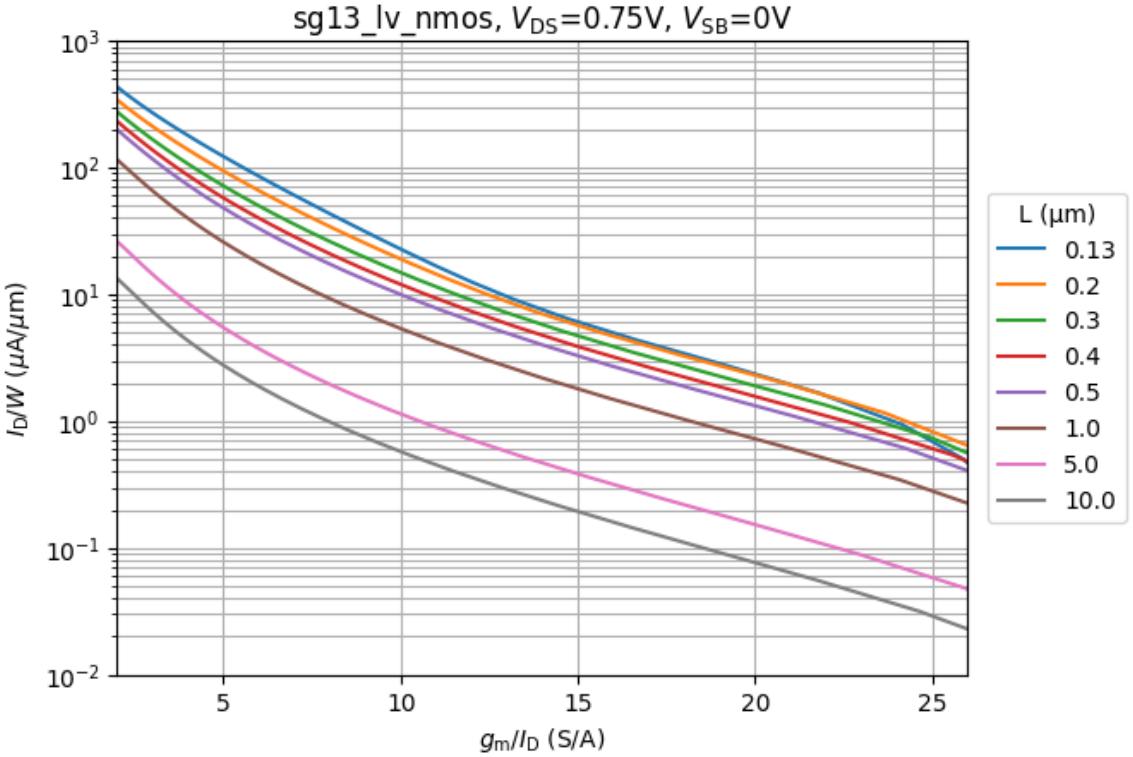
The following figure plots the drain current density I_D/W as a function of g_m/I_D and L. With this plot we can find out how to set the W of a MOSFET once we know the biasing current I_D, the L (selected according to self gain, f_T, and other considerations) and the g_m/I_D design point we selected. The drain current density I_D/W is a very useful nomalized metric to use, because the physical action in the MOSFET establishes a charge density in the channel below the gate, and the changing of the W of the device merely transforms this charge density into an absolute parameter (together with L).



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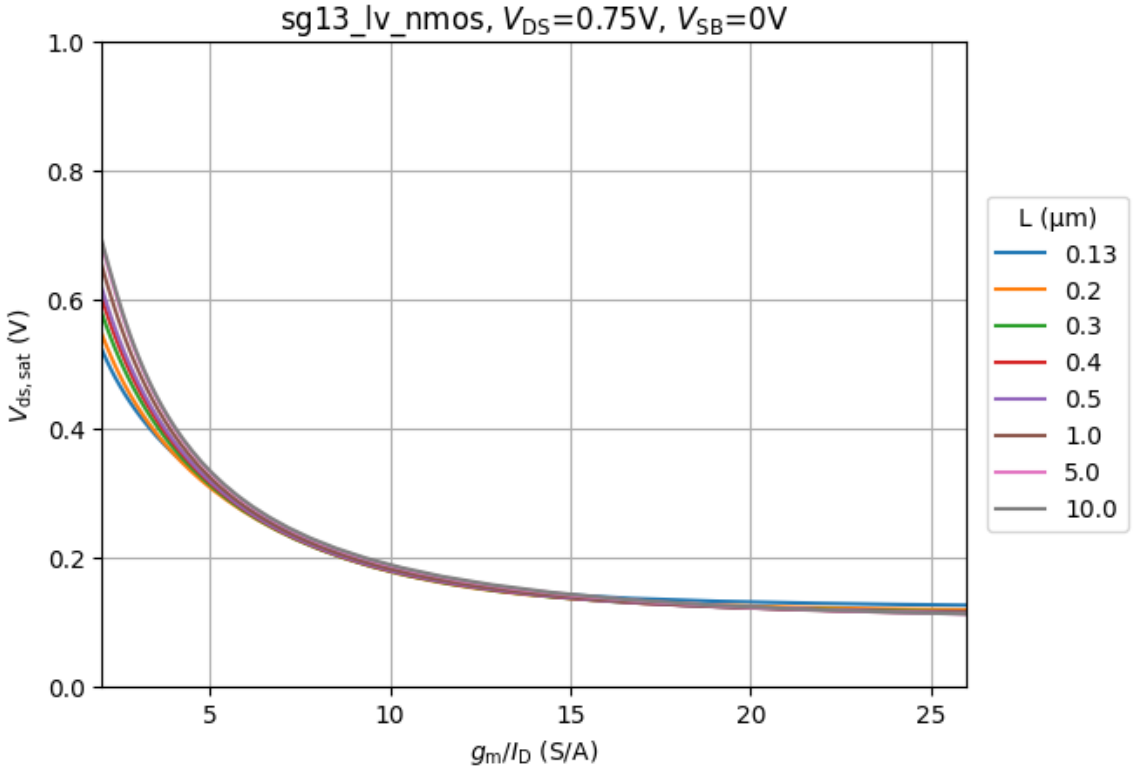
The following plot shows the minimum drain-source voltage $V_{\mathrm{ds,sat}}$ that we need to establish in order to keep the MOSFET in saturation. As you can see, this value is almost independent of L, and increases for small $g_\mathrm{m}/I_\mathrm{D}$. So for low-voltage circuits, where headroom is precious, we tend to bias at $g_\mathrm{m}/I_\mathrm{D} \geq 10$, wheres for fast circuits we need to go to small $g_\mathrm{m}/I_\mathrm{D} \leq 5$ requiring substantial voltage headroom per MOSFET stage that we stack on top of each other.



Source: Article Notebook

For analog circuits the noise performance is usually quite important. Thermal noise of a resistor (the Johnson-Nyquist noise) has a flat power-spectral density (PSD) given by $\overline{V_\mathrm{n}^2}/\Delta f = 4kTR$, where k is Boltzmann's constant, T absolute temperature, and R the value of the resistor (the unit of $\overline{V_\mathrm{n}^2}/df$ is V^2/Hz). This PSD is essentially flat until very high frequencies where quantum effects start to kick in.

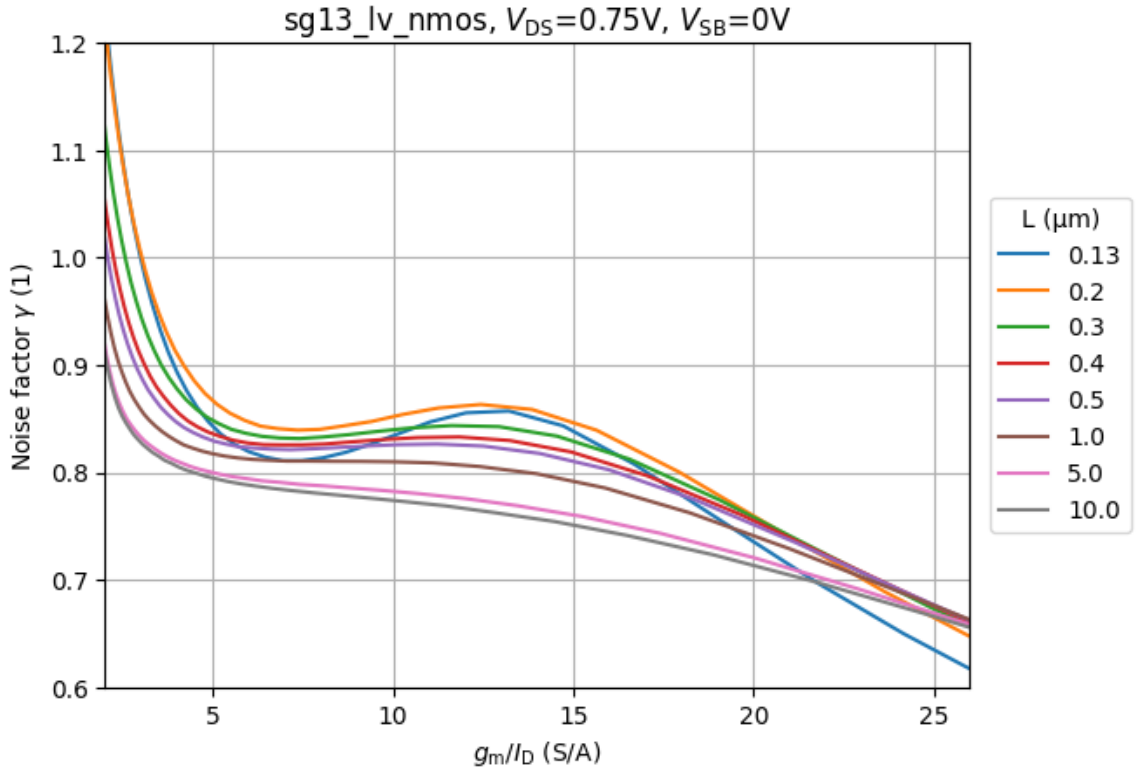
> **Note**
>
> We usually leave the Δf away for a shorter notation, so we write $\overline{V_\mathrm{n}^2}$ when we actually mean $\overline{V_\mathrm{n}^2}/\Delta f$.
> Please also note that the pair of kT pretty much always shows up together, so when you do a calculation and you miss the one or the other, that is often a sign for miscalculation.
> Fuerther, when working with PSD there is the usage of a one-sided (f runs from 0 to ∞) or two-sided PSD (f runs from $-\infty$ to ∞). The default in this lecture is the usage of a **one-sided PSD**.

In this lecture the only MOSFET noise we consider is the drain noise, showing up as a current noise between drain and source, and given by

$$\overline{I_{\mathrm{d,n}}^2} = 4kT\gamma g_{\mathrm{d0}} \tag{3}$$

In saturation (the MOSFET operating as a current source), $g_{\mathrm{d0}} = g_\mathrm{m}$, whereas in triode (the MOSFET operating as a switch), $g_{\mathrm{d0}} = g_{\mathrm{ds}}$.

The factor γ is a function of many things (in classical theory, $\gamma = 2/3$ in saturation and $\gamma = 1$ in triode), and it is characterized in the following plot as a function of $g_\mathrm{m}/I_\mathrm{D}$ and L. So when calculating MOSFET noise we can lookup γ in the below plot, and use Equation 3 to calculate the effective drain current noise.



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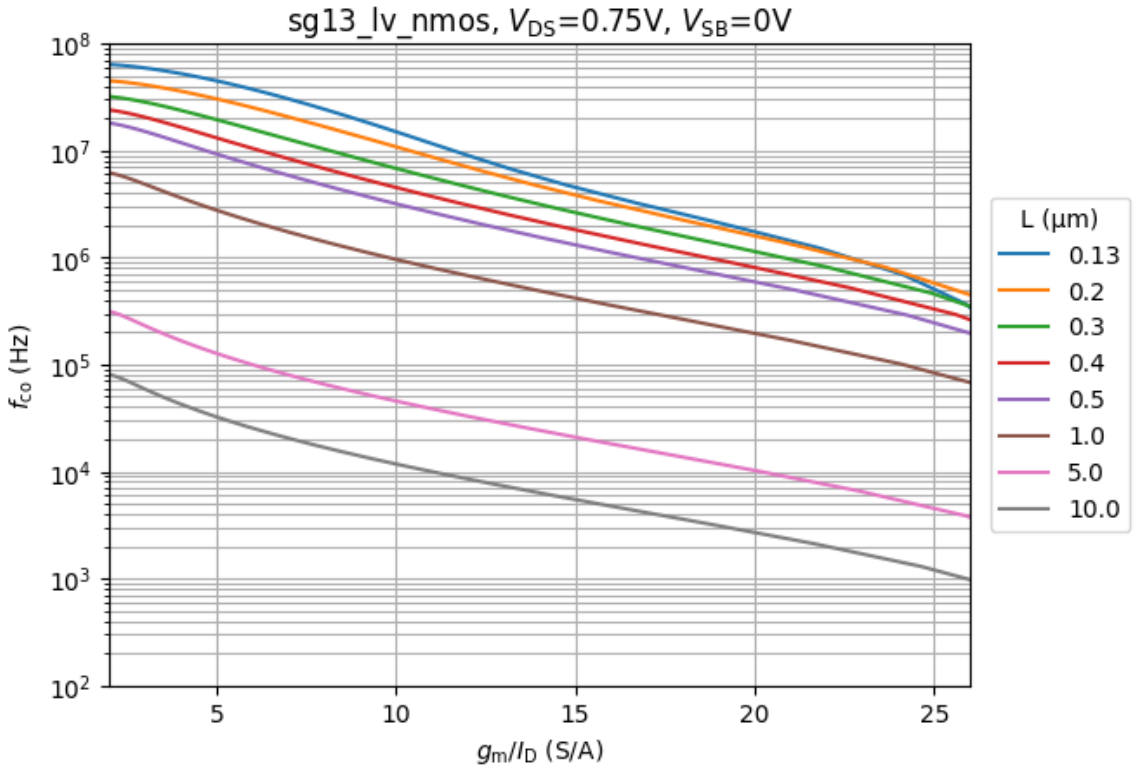
In a MOSFET, unfortunately, besides the thermal noise according to Equation 3, there is also a substantial low-frequency excess noise, called "flicker noise" due to its characteristic $\overline{I^2_{\mathrm{d,nf}}} = K_\mathrm{f}/f$ behaviour (this means that this noise PSD decreases versus frequency). In order to characterize this flicker noise the following plot shows the cross-over frequency f_co, where the flicker noise is as large as the thermal noise. As can be seen in the below plot, this frequency is a strong function of L and $g_\mathrm{m}/I_\mathrm{D}$. Generally, the flicker noise is proportional to $(WL)^{-1}$, so the larger the device is, the lower the flicker noise. The parameter $g_\mathrm{m}/I_\mathrm{D}$ largely stays constant when we keep W/L constant, so for a given $g_\mathrm{m}/I_\mathrm{D}$ flicker noise is proportinal to $1/L^2$. However, increasing L lowers device speed dramatically, so here we have a trade-off between flicker-noise performance and MOSFET speed, and this can have dramatic consequences for high-speed circuits.

> **Note**
>
> The physical origin of flicker noise is the crystal interface between silicon (Si) and the silicondioxide (SiO_2). Since these are different materials, there are dangling bonds,

which can capture charge charriers travelling in the channel. After a random time, these carriers are released, and flicker noise is the result. The amount of flicker noise is a function of the manufacturing process, and will generally be different between device types and wafer foundries.

As you can see in the following plot, f_{co} can reach well into the 10's of MHz for short MOSFETs, significantly degrading the noise performance of a circuit.



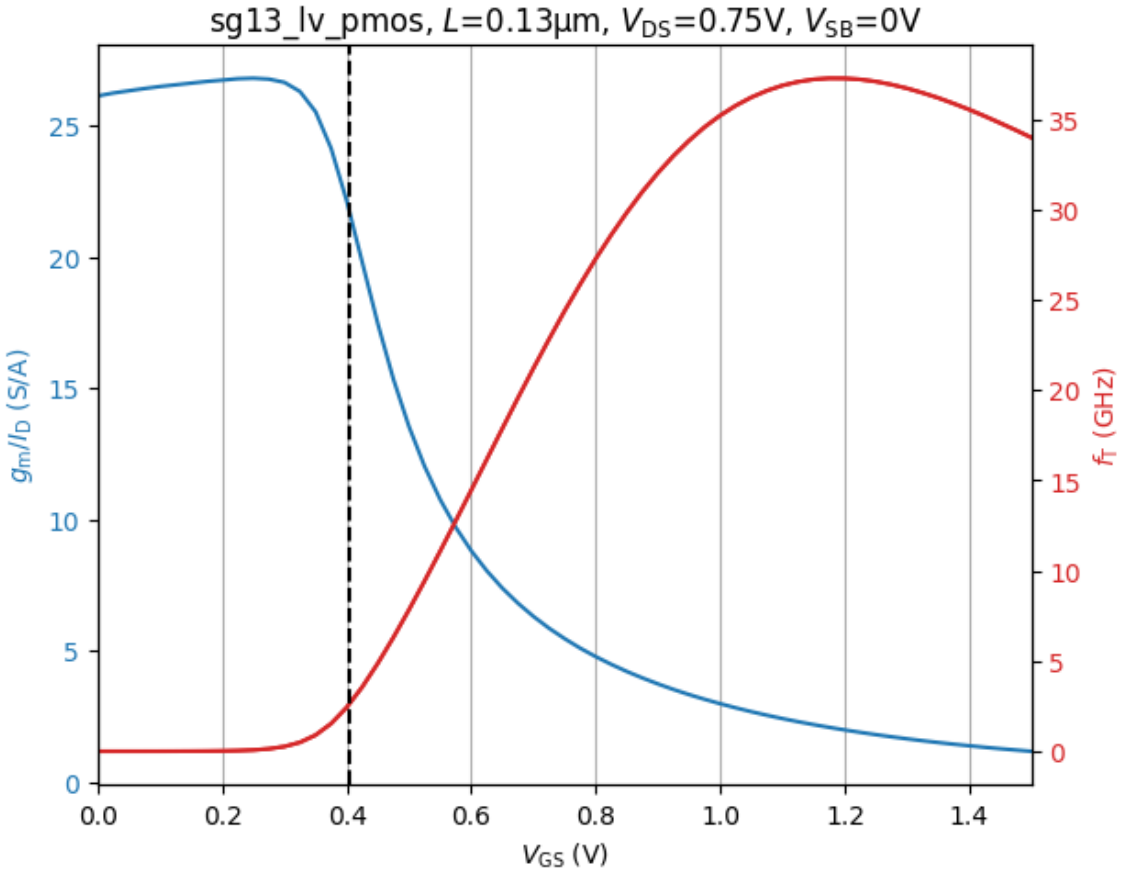
Source: Article Notebook

PMOS Characterization

In the following, we have the same plots as discussed in Section , but now for the PMOS.

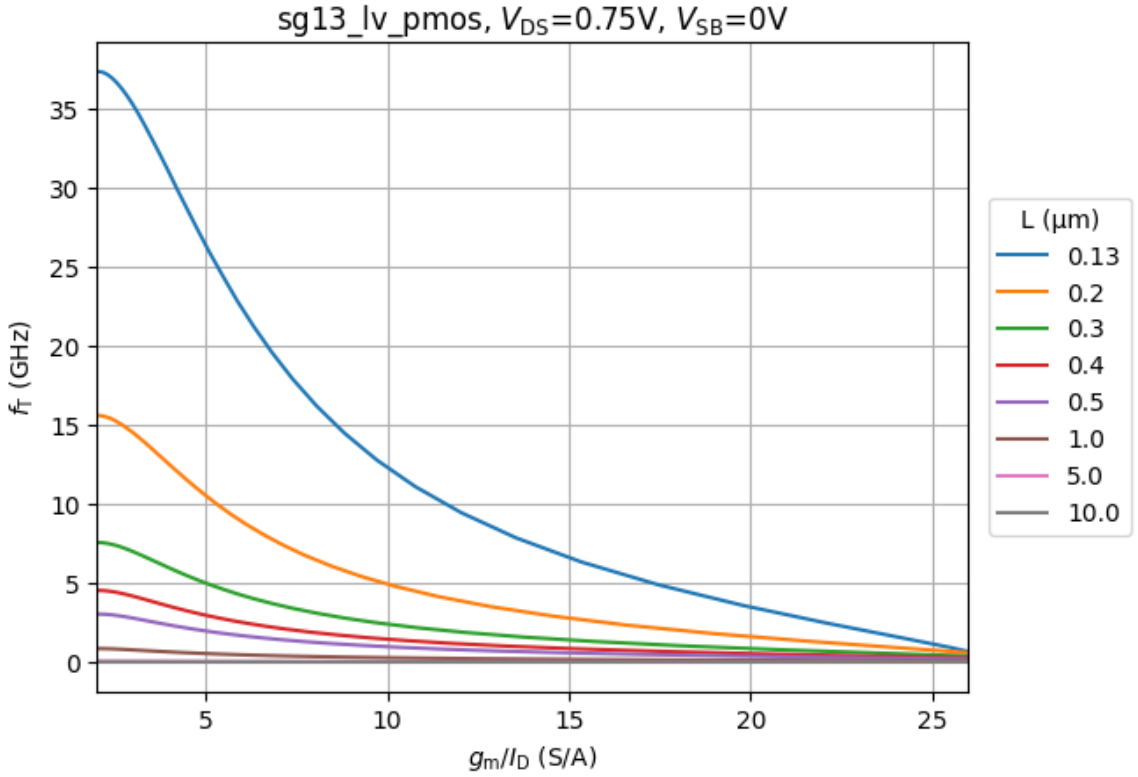
> **Note**
>
> In all PMOS plots we plot positive values for voltages and currents, to have compatible plots to the NMOS. Of course, in a PMOS, voltages and currents have different polarity compared to the PMOS.

g_m/I_D and f_T versus the gate-source voltage V_{GS}:



Source: Article Notebook

f_T against g_m/I_D for several different L. One can see significantly lower top speed for the PMOS compared to the NMOS, which means for high-speed circuits the NMOS should be used.

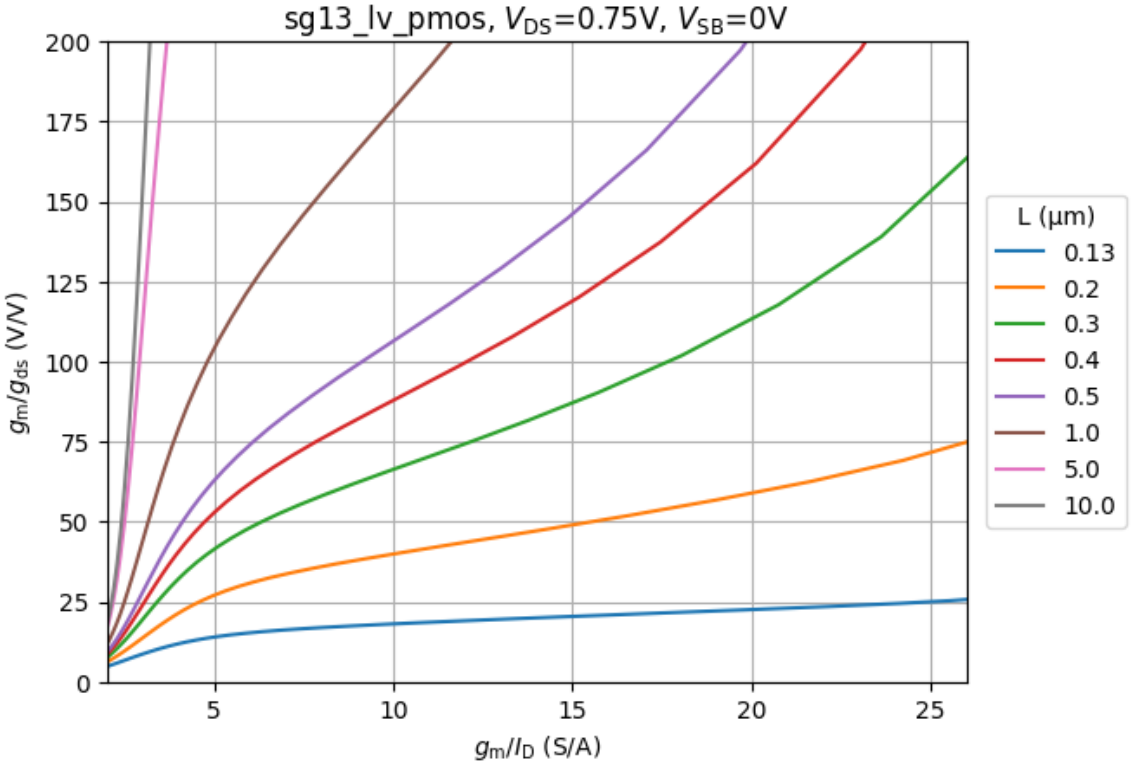


Source: Article Notebook

g_m/g_{ds} versus g_m/I_D. Unfortunately, one can see a modelling error for the PMOS in this plot. The self gain g_m/g_{ds} reaches non-physical values, which indicates an issue with the g_{ds} modelling for the PMOS. We can not use these values for our circuit sizing, so we will use the respective NMOS plots also for the PMOS.

! Important

This example shows how important it is to benchmark the device models when starting to use a new technology. Modelling artifacts like the one shown are quite often happening, as setting up the device compact models and parametrizing them according to measurement data is a very complex task. In any case, just be aware that modelling issues could exist in whatever PDK you are using!



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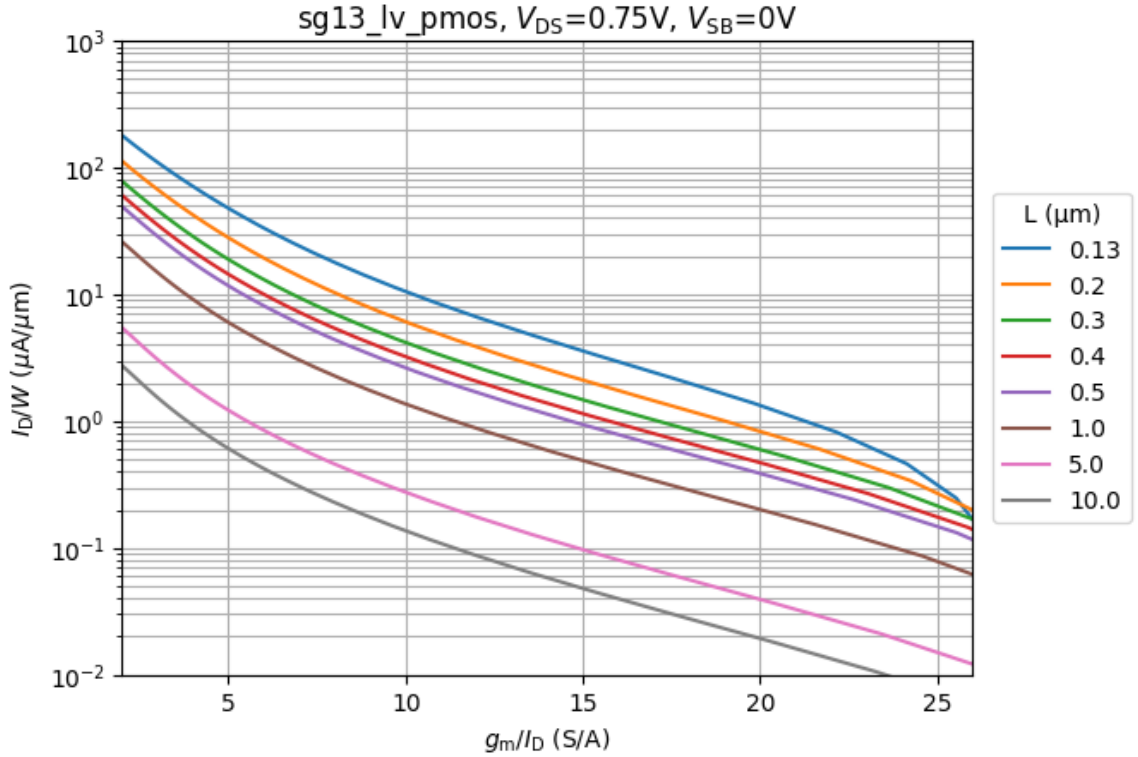
Drain current density I_D/W as a function of g_m/I_D and L:



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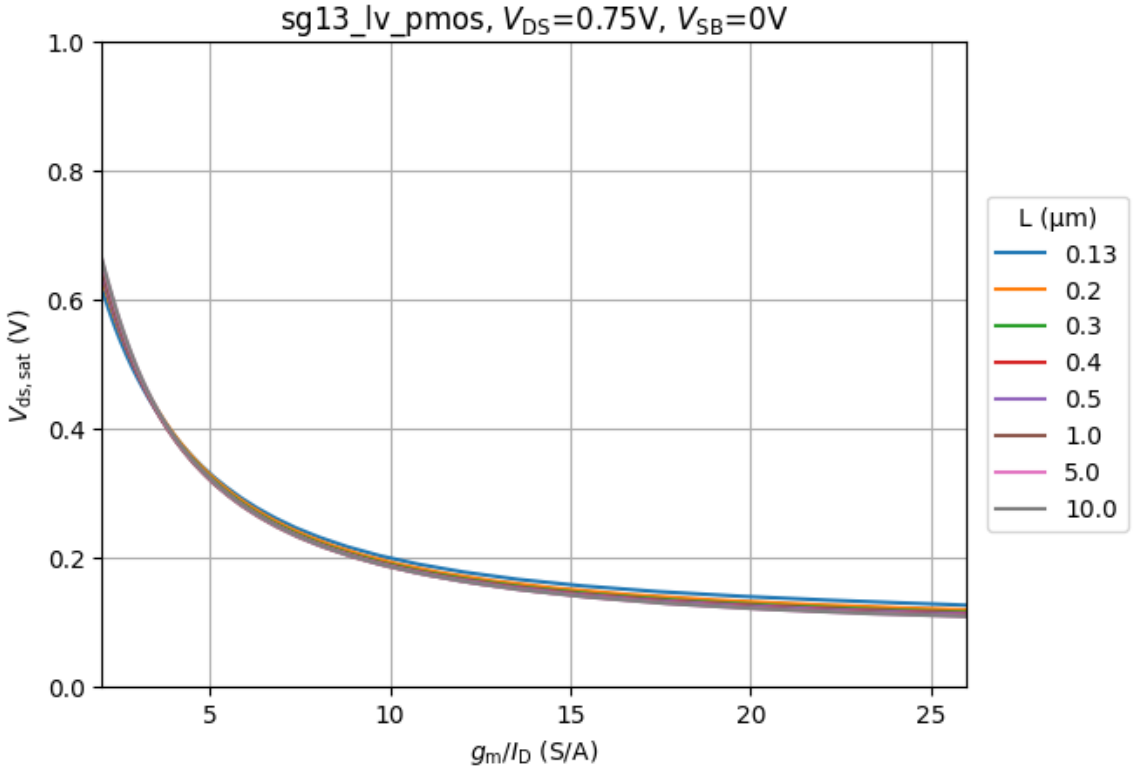
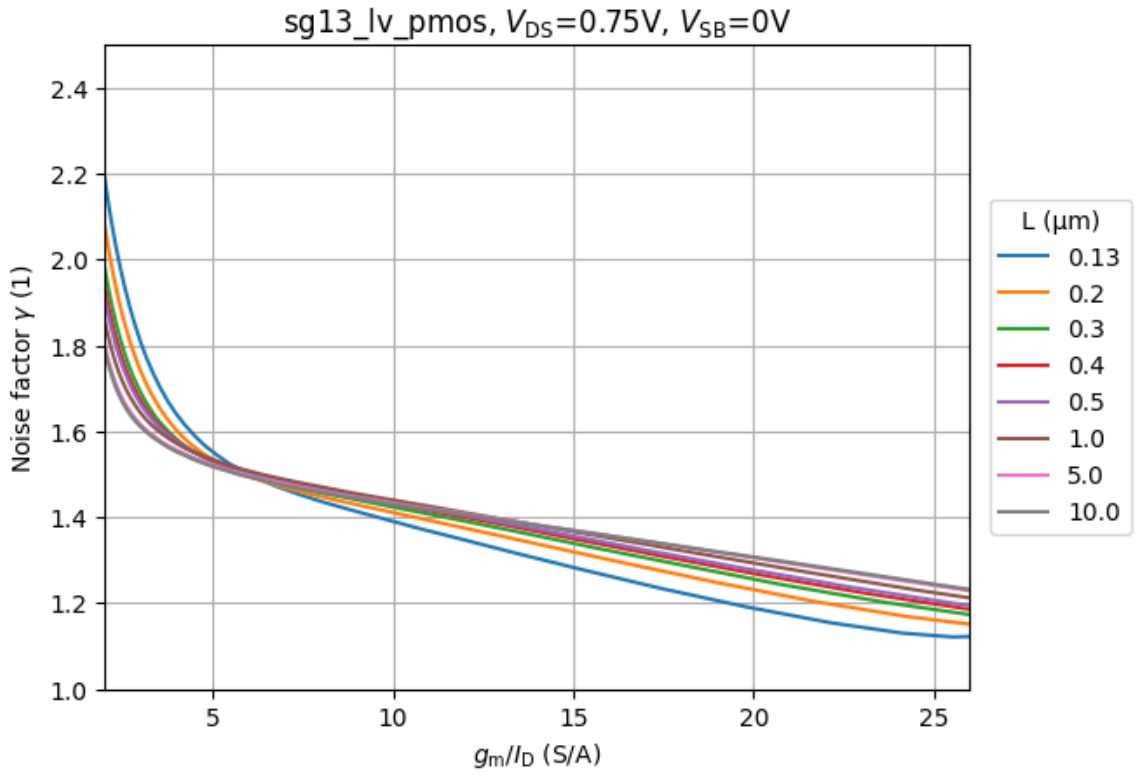
Minimum drain-source voltage $V_{\mathrm{ds,sat}}$ versus $g_{\mathrm{m}}/I_{\mathrm{D}}$ and L:



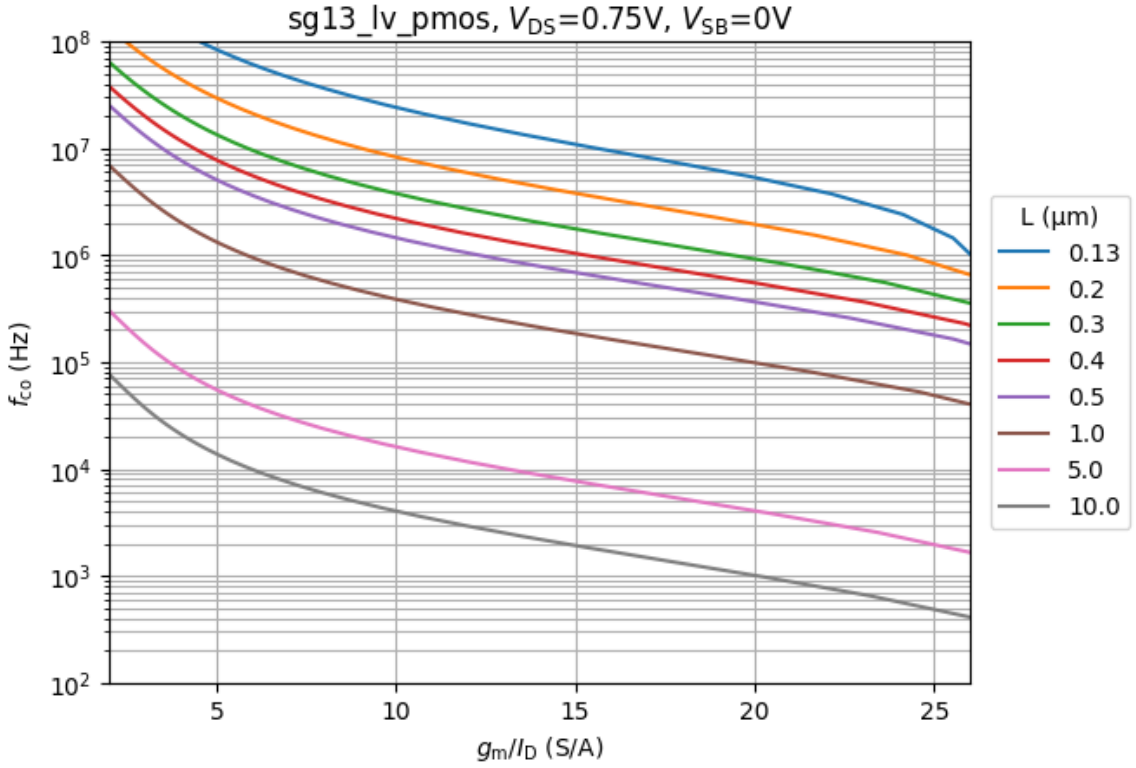
Source: Article Notebook

Noise factor γ versus $g_{\mathrm{m}}/I_{\mathrm{D}}$ and L:



Source: Article Notebook

Flicker noise corner frequency f_{co} versus g_m/I_D and L. If you compare this figure carefully with the NMOS figure you can see that for some operating points the flicker noise for the PMOS is lower than for the NMOS. This is often true for CMOS technologies, so it can be an advantage to use a PMOS transistor in places where flicker noise is critical, like an OTA input stage. Using PMOS has the further advantage that the bulk node can be tied to source (which for NMOS is only possible in a triple-well technology, which is often not available), which gets rid of the body effect.



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First Circuit: MOSFET Diode

The first (simple) circuit we will investigate is a MOSFET, where the gate is shorted with a drain, a so-called MOSFET "diode", which is shown in Figure 8. This diode is one half of a current mirror, which we will investigate in a future section.

Source: Article Notebook

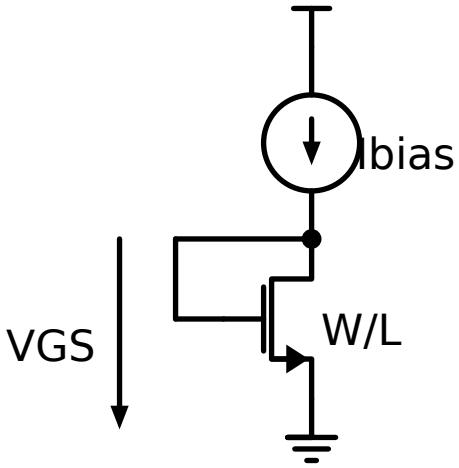

Figure 8: A MOSFET connected as a diode.

Source: Article Notebook

Why looking at a single-transistor circuit at all? By starting with the simplest possible circuit we can develop important skills in circuit analysis (setting up and calculating a small-signal model, calculating open-loop gain, calculate noise) and Xschem/ngspice simulation testbench creation. We safely assume that also the Mona Lisa was not Leonardo da Vinci's first painting, so let's start slow.

This diode is usually biased by a current source, shown as I_{bias} in the figure. Depending on MOSFET sizing with W and L, a certain gate-source voltage V_{GS} will develop. This voltage can be used as a biasing voltage for other circuit parts, for example.

> **Note**
>
> It is important to realize that this configuration essentially employs a feedback loop for operation. The voltage at the drain of the MOSFET is sensed by the gate, and the gate voltage changes until the I_{D} is exactly equal to I_{bias}. In this sense this is probably the smallest feedback circuit one can build.

MOSFET Diode Sizing

We will now build this circuit in Xschem. For sizing the MOSFET we will use the $g_{\text{m}}/I_{\text{D}}$ methodology introduced in Section .

> **Exercise**
>
> Please build a MOSFET diode circuit in Xschem where you use an LV NMOS, set $I_{\text{bias}} = 20\,\mu\text{A}$, $L = 0.13\,\mu\text{m}$, and we want to use $g_{\text{m}}/I_{\text{D}} = 10$ (often a suitable compromise between transistor speed and g_{m} efficiency).

1. Use the figures in Section to find out the proper value for W.
2. What is f_T for this MOSFET? What is the value for g_m and g_{ds}?
3. Draw the circuit in Xschem, and simulate the operating point. Do the values match to the values found out before during circuit sizing?

Before continuing, please finish the previous exercise. Once you are done, compare with the below provided solution.

Solution

1. Using the fact that $I_{bias} = I_D = 20\,\mu A$ and $g_m/I_D = 10$ directly provides $g_m = 0.2\,mS$.
2. Using the self-gain plot, we see that $g_m/g_{ds} \approx 21$, so $g_{ds} \approx 9.5\,\mu S$. The f_T can easily be found in the respective plot to be $f_T = 23\,GHz$.
3. The W of the MOSFET we find using the drain current density plot and the given bias current. Rounding to half-microns results in $W = 1\,\mu m$.
4. Since we are looking at the graphs, we further find $\gamma = 0.84$, $V_{ds,sat} = 0.18\,V$, and $f_{co} \approx 15\,MHz$.
5. In addition, we expect $V_{GS} \approx 0.6\,V$.

An example Jupyter notebook to extract these values accurately you can find here. An Xschem schematic for this exercise is provide as well.

MOSFET Diode Large-Signal Behaviour

As discussed above, the MOSFET diode configuration is essentially a feedback loop. Before we will analyse this loop in small-signal, we want to investgate how this loop settles in the time domain, and by doing this we can observe the large-signal settling behaviour. To simulate this, we change the dc bias source from the previous example to a transient current source, which we will turn on after some ns. The resulting Xschem testbench is shown in Figure 9.

In Figure 9 another interesting effect can be observed: While the turn-on happens quite rapidly (essentially the bias current source charges the gate capacitance, until the gate-source voltage is large enough that the drain current counteracts the bias current), the turn-off shows a very long settling tail. This is due to the fact that as the gate capacitance is discharged by the drain current the V_{GS} drops, which in turn reduces the drain current, which will make the discharge even slower. We have an effect similar to the capacitor discharge by a diode (Hellen 2003).

It is thus generally a good idea to add power-down switches to the circuits to disable the circuit quickly by pulling floating nodes to a defined potential (usually V_{DD} or V_{SS}) and to avoid long intermediate states during power down. This will also allow a turn-on from a well-defined off-state.

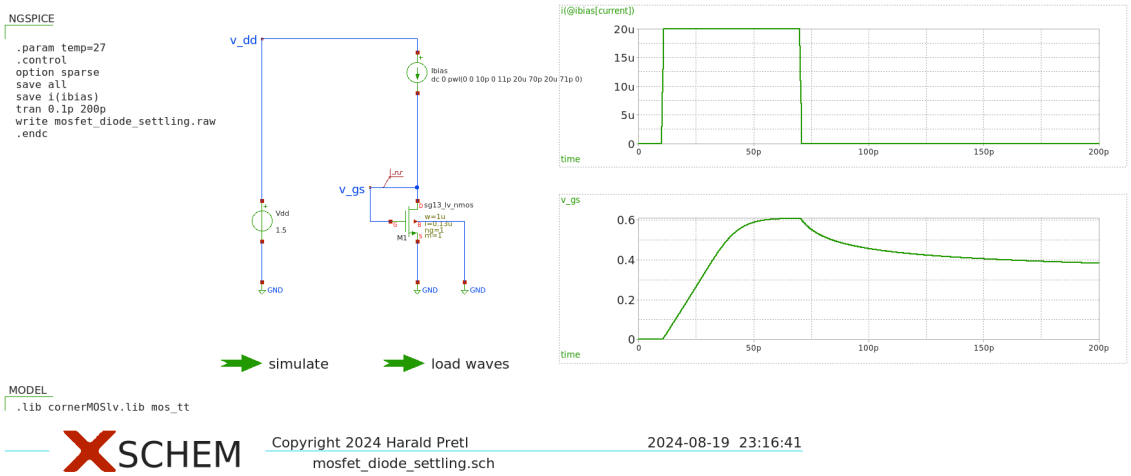

Figure 9: Testbench for MOSFET diode transient settling.

MOSFET Diode Small-Signal Analysis

We now want to investigate the small-signal behaviour of the MOSFET diode. Based on the small-signal model of the MOSFET in Figure 5 we realize that gate and drain are shorted, and we also connect bulk to source. We can thus simplify the circit to the one shown in Figure 10.

Source: Article Notebook

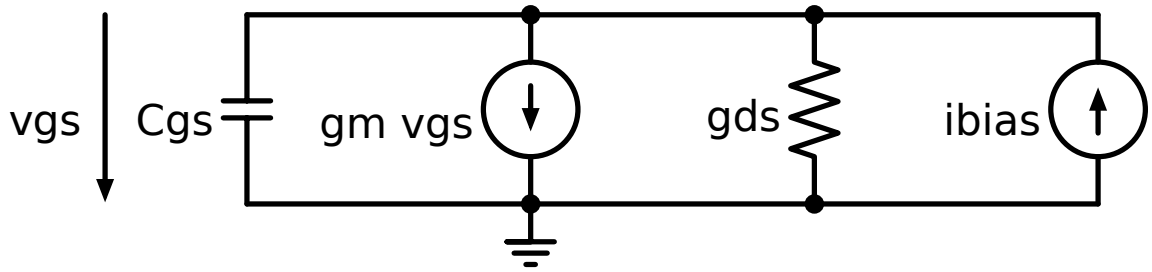

Figure 10: The MOSFET diode small-signal model.

Source: Article Notebook

> **Note**
>
> For small-signal analysis we would not need to declare one node as the ground potential. However, when doing so, and selecting the ground node strategically, we can simplify the analysis, as we usually do not formulate KCL for the ground node (as we have only $N-1$ independent KCL equations, N being the number of nodes of a circuit), and the potential difference equations are simpler if one node is at $0\,V$.

For calculating the small-signal impedance of the MOSFET diode we formulate KCL at the top node to get

$$i_{\text{bias}} - sC_{\text{gs}}v_{\text{gs}} - g_{\text{m}}v_{\text{gs}} - g_{\text{ds}}v_{\text{gs}} = 0.$$

It follows that

$$Z_{\text{diode}}(s) = \frac{v_{\text{gs}}}{i_{\text{bias}}} = \frac{1}{g_{\text{m}} + g_{\text{ds}} + sC_{\text{gs}}}. \tag{4}$$

When neglecting g_{ds} and at dc we get $Z_{\text{diode}} = 1/g_{\text{m}}$, which is an important result and should be memorized.

> **Important**
>
> In circuit analysis it is often algebraically easier to work with conductances instead of impedances, so please remember that Ohm's law for a conductance is $I = GU$, and for a capacitance is $I = sCU$. When writing equations, it is also practical to keep sC together, so we will strive to sort terms accordingly.

Looking at Equation 4 we see that for low frequencies, the diode impedance is resistive, and for high frequencies it becomes capactive as the gate-source capacitance starts to dominate. The corner frequeny of this low-pass can be calculated as

$$\omega_{\text{c}} = \frac{g_{\text{m}} + g_{\text{ds}}}{C_{\text{gs}}} \approx \omega_{\text{T}}$$

which is pretty much the transit frequency of the MOSFET!

MOSFET Diode Stability Analysis

The diode-connected MOSFET forms a feedback loop. What is the open-loop gain? For calculating it, we are breaking the loop, and apply a dummy C^*_{gs} at the right side to keep the impedances correct. A circuit diagram is shown in Figure 11, we break the loop at the dotted connection. As we can see in this example, it is critically important when breaking up a loop for analysis (also for simulation!) to keep the terminal impedances the same. Only in special cases where the load impedance is very high or the driving impedance is very low is it acceptable to disregard loading effects!

Source: Article Notebook

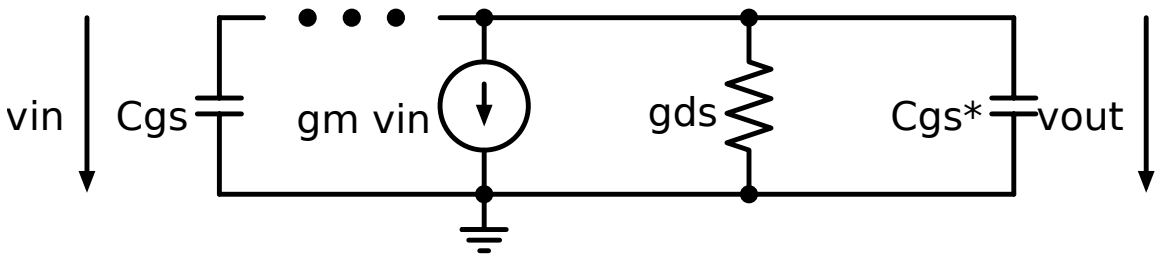

Figure 11: The MOSFET diode small-signal circuit for open-loop analysis.

Source: Article Notebook

By inspecting Figure 11 we see that

$$v_{\text{out}} = -g_{\text{m}} v_{\text{in}} \frac{1}{g_{\text{ds}} + sC_{\text{gs}}}.$$

The open-loop gain $H_{\text{ol}}(s)$ is thus

$$H_{\text{ol}}(s) = \frac{v_{\text{out}}}{v_{\text{in}}} = -\frac{g_{\text{m}}}{g_{\text{ds}} + sC_{\text{gs}}}. \tag{5}$$

Inspecting Equation 5 we realize that

1. the dc gain $g_{\text{m}}/g_{\text{ds}}$ is the self-gain of the MOSFET, so $20\log(0.2 \cdot 10^{-3}/9.6 \cdot 10^{-6}) = 26.4\,\text{dB}$, and
2. there is a pole at $\omega_{\text{p}} = -g_{\text{ds}}/C_{\text{gs}}$, which is at $9.6 \cdot 10^{-6}/(2\pi \cdot 1.4 \cdot 10^{-15}) = 1.1\,\text{GHz}$.

With this single pole location in $H_{\text{ol}}(s)$ this loop is perfectly stable at under all conditions.

The question is now how to simulate this open-loop gain, and how to break the loop open in simulation? In general there are various methods, as we can use artificially large (ideal) inductors and capacitors to break loops open and still establish the correct dc operating points for the ac loop analysis. However, mimicking the correct loading can be an issue, and requires a lot of careful consideration. There is an alternative method which breaks the loop open only by adding an ac voltage source in series (thus keeps the dc operating point intact), or injects current using a current source. Based on both measurements the open-loop gain can be calculated. This is called **Middlebrook's method** (Middlebrook 1975) which is based on double injection, and we will use it for our loop simulations.

> **Middlebrook's Method**
>
> When we want to do an open-loop gain analysis, we break the loop at one point by inserting (1) an ac voltage source, and (2) attach an ac current source, as shown in Figure 12 and Figure 13.

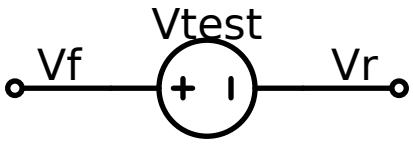

Figure 12: Middlebrook voltage loop gain simulation.

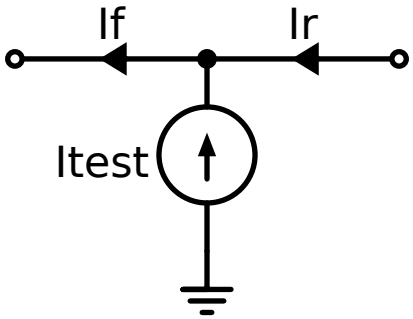

Figure 13: Middlebrook current loop gain simulation.

For both cases we do an ac analysis, and find the corresponding transfer functions T_v and T_i:

$$T_\mathrm{v} = -\frac{V_\mathrm{r}}{V_\mathrm{f}}$$

and

$$T_\mathrm{i} = -\frac{I_\mathrm{r}}{I_\mathrm{f}}$$

Then, we can calculate the closed-loop transfer function $T(s) = H_{\mathrm{ol(s)}}$ as

$$T(s) = \frac{T_\mathrm{v}T_\mathrm{i} - 1}{T_\mathrm{v} + T_\mathrm{i} + 2}$$

We now want to simulate the open-loop transfer function $H_\mathrm{ol}(s)$ by using Middlebrook's method and confirm our analysis above.

Exercise

Please build a simulation testbench in Xschem to simulate the open-loop transfer function of the MOSFET diode. Confirm the dc gain and pole location as given by Equation 5.
If you are getting stuck you can look at this Xschem testbench, shown in Figure 14.

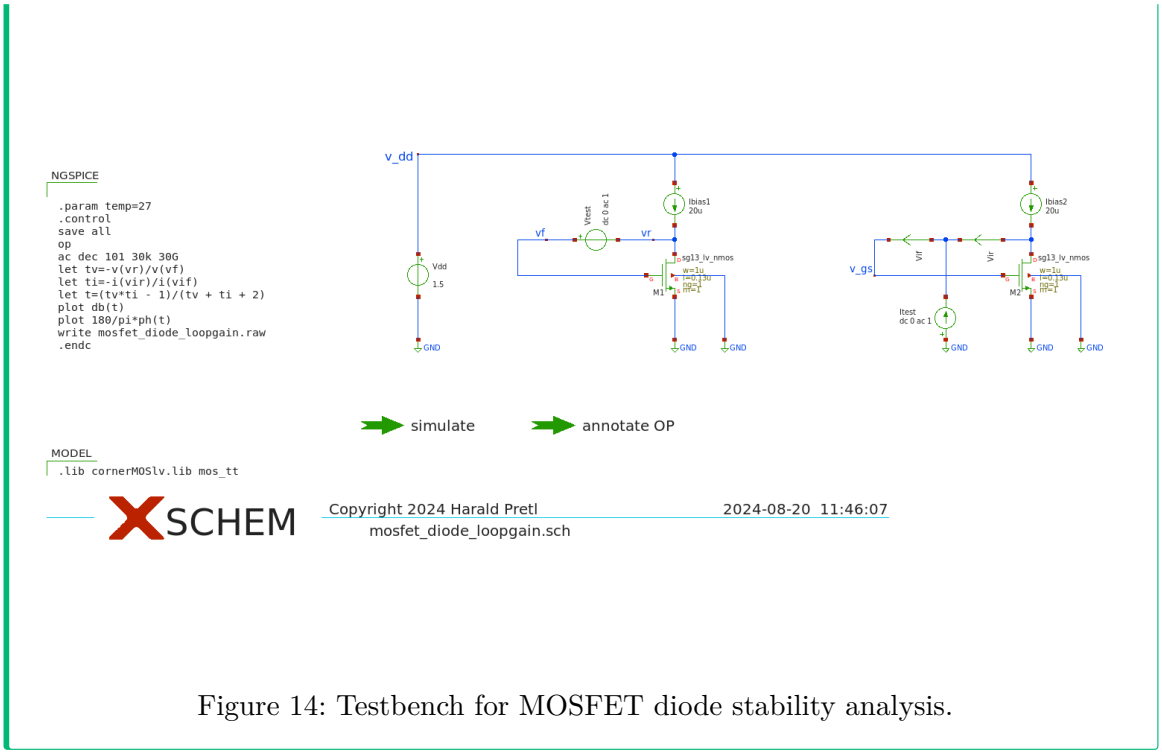

Figure 14: Testbench for MOSFET diode stability analysis.

From simulation we see that the open-loop gain is 24.9 dB at low frequencies, which matches quite well our prediction of 26.4 dB. In the Bode plot we see a low-pass with a -3 dB corner frequency of 1.4 GHz, which again is fairly close to our prediction of 1.1 GHz.

MOSFET Diode Noise Calculation

As a final exercise on the MOSFET diode circuit we want to calculate the output noise when we consider V_{GS} the output reference voltage which is created when passing a bias current through the MOSFET diode. The bias current we will assume noiseless.

We will use the small-signal circuit shown in Figure 15.

Source: Article Notebook

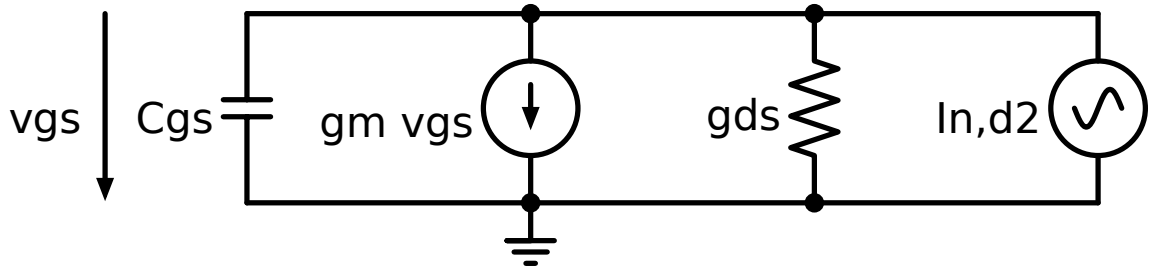

Figure 15: The MOSFET diode small-signal model with drain noise source.

Source: Article Notebook

As we have already calculated the small-signal diode impedance in Equation 4 we will use this result, and just note that the drain current noise of the MOSFET flows through this impedance. The noise voltage at v_{gs} is this given as

$$\overline{V_{\mathrm{n}}^2} = Z_{\mathrm{diode}}^2 \overline{I_{\mathrm{n,d}}^2}.$$

The drain current noise of the MOSFET is given as (introduced in @#sec-mosfet-smallsignal-model)

$$\overline{I_{\mathrm{n,d}}^2} = 4kT\gamma g_{\mathrm{m}}.$$

For low frequencies (ignoring g_{ds} and C_{gs}) we get

$$\overline{V_{\mathrm{n}}^2} = Z_{\mathrm{diode}}^2 \overline{I_{\mathrm{n,d}}^2} = \frac{1}{g_{\mathrm{m}}^2} 4kT\gamma g_{\mathrm{m}} = \frac{4kT\gamma}{g_{\mathrm{m}}}$$

which is the thermal noise of a resistor of value $1/g_{\mathrm{m}}$ enhanced by the factor γ.

We now calculate the full equation, and after a bit of algebra arrive at

$$\overline{V_{\mathrm{n}}^2}(f) = \frac{4kT\gamma g_{\mathrm{m}}}{(g_{\mathrm{m}} + g_{\mathrm{ds}})^2 + (2\pi f C_{\mathrm{gs}})^2}. \tag{6}$$

If we are interested in the PSD of the noise then Equation 6 gives us the result. If we are interested in the rms value (the total noise) we need to integrate this equation.

$$\int_0^\infty \frac{a}{b^2 + (cf)^2} df = \frac{\pi a}{2bc}$$

Using the integral help from the previous info box, we can easily get at

$$V_{\mathrm{n,rms}}^2 = \int_0^\infty \overline{V_{\mathrm{n}}^2}(f) df = \frac{kT\gamma g_{\mathrm{m}}}{(g_{\mathrm{m}} + g_{\mathrm{ds}}) C_{\mathrm{gs}}}. \tag{7}$$

The form of Equation 7 is the exact solution, but we gain additional insight if we assume that $g_{\mathrm{m}} + g_{\mathrm{ds}} \approx g_{\mathrm{m}}$ and then

$$V_{\mathrm{n,rms}}^2 = \frac{kT\gamma}{C_{\mathrm{gs}}}. \tag{8}$$

Inspecting Equation 8 we see our familiar kT/C noise enhanced by the factor γ! Calculating this value for our MOSFET diode we get $\sqrt{V_{\mathrm{n,rms}}^2} = \sqrt{1.38 \cdot 10^{-23} \cdot 300 \cdot 0.84 / 1.4 \cdot 10^{-15}} = 1.58\,\mathrm{mV}$, which is a sizeable value! We run circuits in this technology at $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, which leaves us with a signal swing of ca. $1.1\,\mathrm{V_{pp}}$, resulting in a dynamic range in this case of $20\log(1.58 \cdot 10^{-3}/0.39) \approx -48\,\mathrm{dB}$.

Important

Large BW circuits can integrate noise over a wide bandwidth resulting in considerable rms noise.

Exercise

Please build a simulation testbench in Xschem to simulate the noise performance of the MOSFET diode, and confirm the rms noise value that we just calculated. Look at the rms value and the PSD of the noise, and play around with the integration limits. What is the effect? Can you see the flicker noise in the PSD? How much is its contribution to the rms noise?
If you are getting stuck you can look at this Xschem testbench, shown in Figure 16.

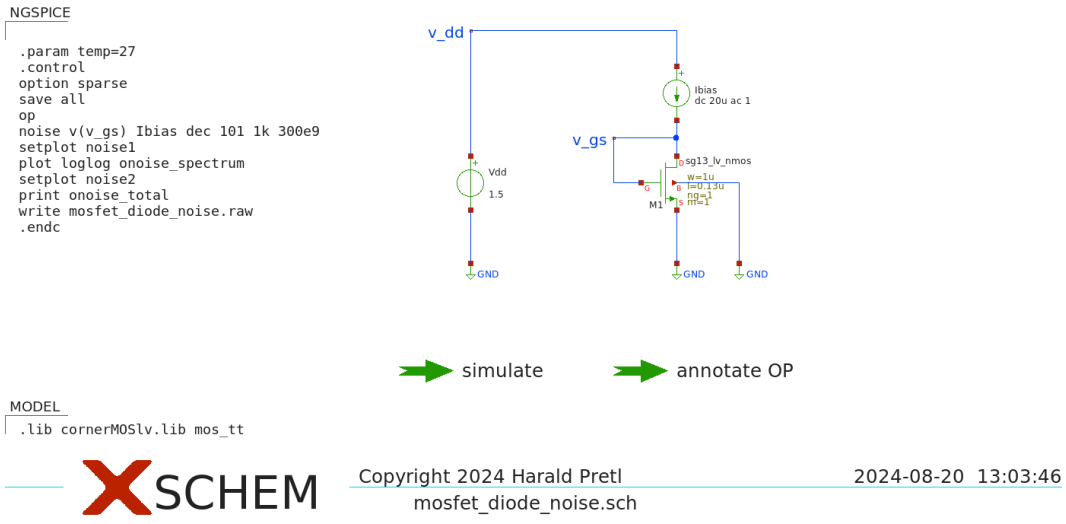

Figure 16: Testbench for MOSFET diode noise analysis.

Conclusion

In this section we investigated the simple MOSFET-diode circuit. We learned important skills like how to derive a small-signal model, how to calculate important features like noise and open-loop gain for stability analysis. We introduced Middlebrook's method to have a mechanism to open up loops in simulation (and calculation) without disturbing operating points for change loading conditions.

If you feel that you have not yet mastered these topics or are uncertain in the operation of ngspice, please go back to the beginning of the section and read through the theory and redo the exercises.

Current Mirror

In this section we will look into a fundamental building block which is often used in integrated circuit design, the **current mirror**. A diagram is shown in Figure 17 with one MOSFET diode converting the incoming bias current into a voltage, and two output MOSFETs working as current sources, which are biased from the diode. By properly selecting all W and L the input current can be scaled, and multiple copies can be created atn once. Shown in the figure are two output currents, but any number of parallel branches can be realized.

Source: Article Notebook

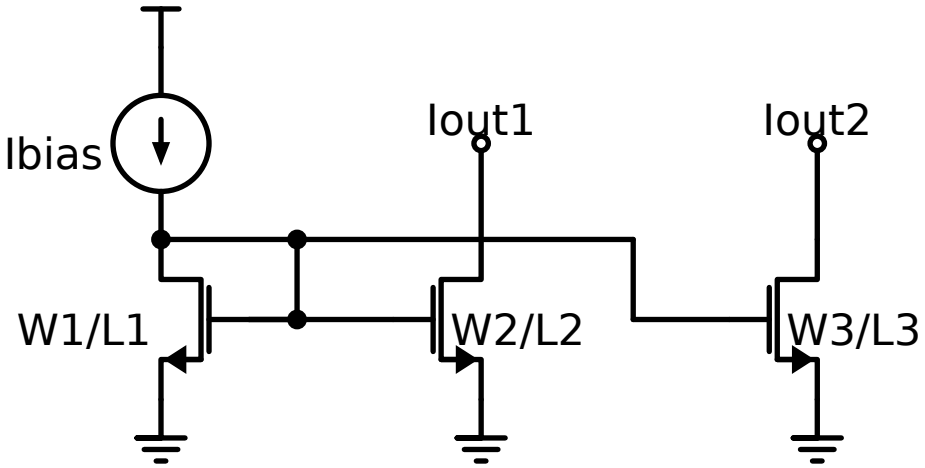

Figure 17: A current mirror with two output branches.

Source: Article Notebook

The output current I_{out1} is then given by

$$I_{\text{out1}} = I_{\text{bias}} \frac{W_2}{L_2} \frac{L_1}{W_1}$$

and the output current I_{out2} is given by

$$I_{\text{out2}} = I_{\text{bias}} \frac{W_3}{L_3} \frac{L_1}{W_1}.$$

For good matching in layout care has to be taken that the MOSFET widths and lengths are constructed out of **unit elements** of identical size, where an appropiate amount of these single units are then arranged in series or parallel configuration to arrive at the target W and L.

As we know from earlier investigations of the MOSFET performance in Section the drain current of a MOSFET is a function of V_{GS} and V_{DS}. As long as the MOSFET stays in saturation (i.e., $V_{DS} > V_{ds,dsat}$) the drain current is just a mild function of V_{DS} (essentially the effect of g_{ds}, which is the output conductance of the MOSFET). A fundamental flaw of the basic current mirror shown in Figure 17 is the mismatch of the V_{DS} of the MOSFET. The input-side diode has $V_{GS} = V_{DS}$, whereas the output current sources have a V_{DS} depending on the connected circuitry. Improved current mirrors exist (basically fixing this flaw), still, when just a simple current mirror is required this structure is used for its simplicity.

Exercise

Please construct a current mirror based on the MOSFET-diode which we sized in Section . The input current $I_{bias} = 20\,\mu A$, and we want three output currents of size $10\,\mu A$, $20\,\mu A$, and $40\,\mu A$.
Sweep the output voltage of all three current branches and see over which voltage range an acceptable current is created. For which output voltage range is the current departing from its ideal value, and why?
You see that the slope of the output current is quite bad, as g_{ds} is too large. We can improve this by changing the length to $L = 5\,\mu m$ (for motivation, please look at the graphs in Section). In addition, for a current mirror we are not interested in a high g_m/I_D value, so we can use $g_m/I_D = 5$ in this case. Please size the current mirror MOSFETs accordingly (please round the W to half micron, to keep sizes a bit more practical). Compare this result to the previous one, what changed?
In case you get stuck, here are Xschem schematics for the original and the improved current mirrors.

Differential Pair

Like the current mirror in Section the **differential pair** is an ubiquitous building block often used in integrated circuit design. The fundamental structure is given in Figure 18.

Source: Article Notebook

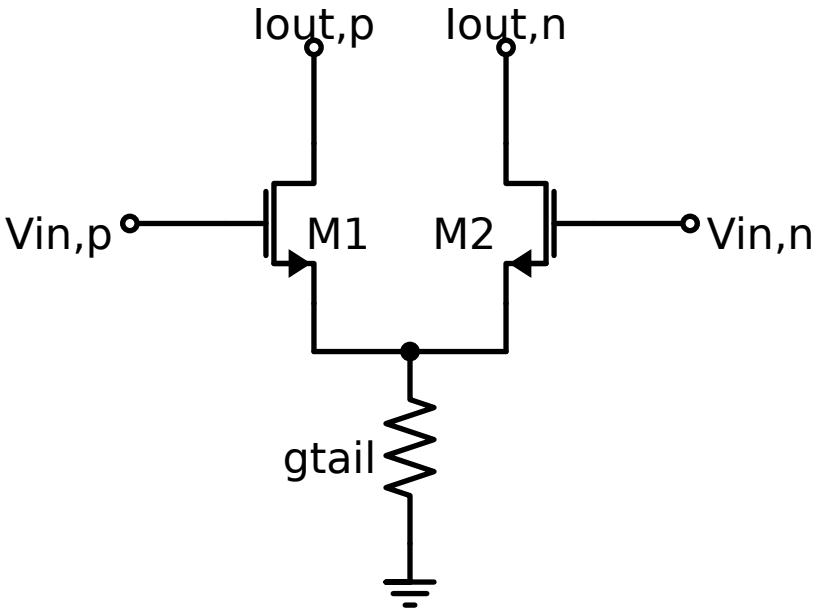

Figure 18: A differential pair.

Source: Article Notebook

In order to understand its operation it is instructive to separate the input condition into (1) a purely differential voltage, and (2) into a common-mode voltage, and see what the impact on the output currents is.

Differential Operation of the Diffpair

For a differential mode of operation we assume that the input common mode voltage is constant, i.e. $V_{\text{in,p}} + V_{\text{in,n}} = V_{\text{CM}}$. A differential input voltage v_{in} then results in

$$V_{\text{in,p}} = V_{\text{CM}} + \frac{v_{\text{in}}}{2}$$

and

$$V_{\text{in,n}} = V_{\text{CM}} - \frac{v_{\text{in}}}{2}.$$

For a small-signal differential drive the potential at the tail point stays constant and we can treat it as a virtual ground. The output current on each side is then given by (neglecting g_{ds} and g_{mb} of M_1 and M_2)

$$i_{\text{out,p}} = g_{\text{m1}} \left(\frac{v_{\text{in}}}{2} \right)$$

and

$$i_{\text{out,n}} = g_{\text{m2}} \left(-\frac{v_{\text{in}}}{2} \right).$$

Usually we assume symmetry in the differential pair, so $g_{m1} = g_{m2} = g_m$. The differential output current i_{out} is then given by

$$i_{out} = i_{out,p} - i_{out,n} = g_m v_{in} \tag{9}$$

We see in Equation 9 that the differential output current is simply the differential input voltage multiplied by the g_m of the individual transistor. We also note that the bottom conductance g_{tail} plays no role for the small-signal differential operation.

Common-Mode Operation of the Diffpair

Usually, the source conductance g_{tail} is realized by a current source and ideally should be $g_{tail} = 0$. If this is the case, then the output currents are not a function of the common-mode input voltage (at least as long as bias points keep the MOSFET in triode), and (I_{tail} is set by the tail current source)

$$I_{out,p} = I_{out,n} = \frac{I_{tail}}{2}.$$

However, if we assume a realistic tail current source then $g_{tail} > 0$. For analysis we can simply look at a half circuit since everything is symmetric. In order to simplify the analysis a bit we remove all capacitors from the MOSFET small-signal model and set $g_{ds} = g_{mb} = 0$. We arrive then at the small-signal equivalent circuit shown in Figure 19 (note that we set $v_{in,p} = v_{in,n} = v_{in}$ and $i_{out,p} = i_{out,n} = i_{out}$ under symmetry considerations).

Source: Article Notebook

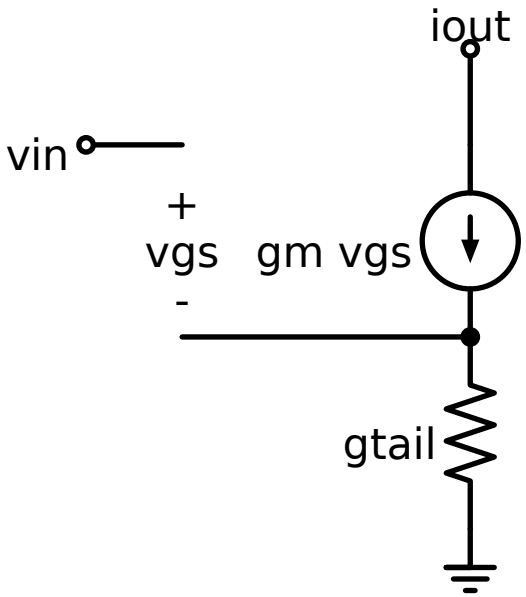

Figure 19: Small-signal model of the differential pair half-circuit in common-mode operation.

Source: Article Notebook

Formulating KVL for the input-side loop we get

$$v_{\text{in}} = v_{\text{gs}} + \frac{i_{\text{ds}}}{g_{\text{tail}}}.$$

With $i_{\text{out}} = i_{\text{ds}} = g_{\text{m}} v_{\text{gs}}$ we arrive at

$$i_{\text{out}} = \frac{g_{\text{m}} g_{\text{tail}}}{g_{\text{m}} + g_{\text{tail}}} v_{\text{in}} \tag{10}$$

Interpreting Equation 10 we can distinguish the following extreme cases:

1. If $g_{\text{tail}} = 0$ (ideal tail current source) then $i_{\text{out}} = 0$, the common-mode voltage variation from the input is suppressed and does not show up at the common-mode output current (which is constant due to the ideal tail current source). This is usually the case that we want to achieve.
2. If $g_{\text{tail}} = \infty$ then $i_{\text{out}} = g_{\text{m}} v_{\text{in}}$, which means the output current is a function of the MOSFET g_{m}. If everything is perfectly matched, then the differential output current is zero, but the common-mode output current changes according to the common-mode input voltage. In special cases this can be a wanted behaviour, this configuration is called a "pseudo-differential pair."

A Basic 5-Transistor OTA

Suited with the knowledge of basic transitor operation (Section and Section) and the working knowledge of the current mirror (Section and Section) as well as the differential pair (Section) we can now start to design our first real circuit. A fundamental (simple) circuit that is often used for basic tasks is the 5-transistor operational transconductance amplifier (OTA). A circuit diagram of this 5T-OTA is shown in Figure 20.

Source: Article Notebook

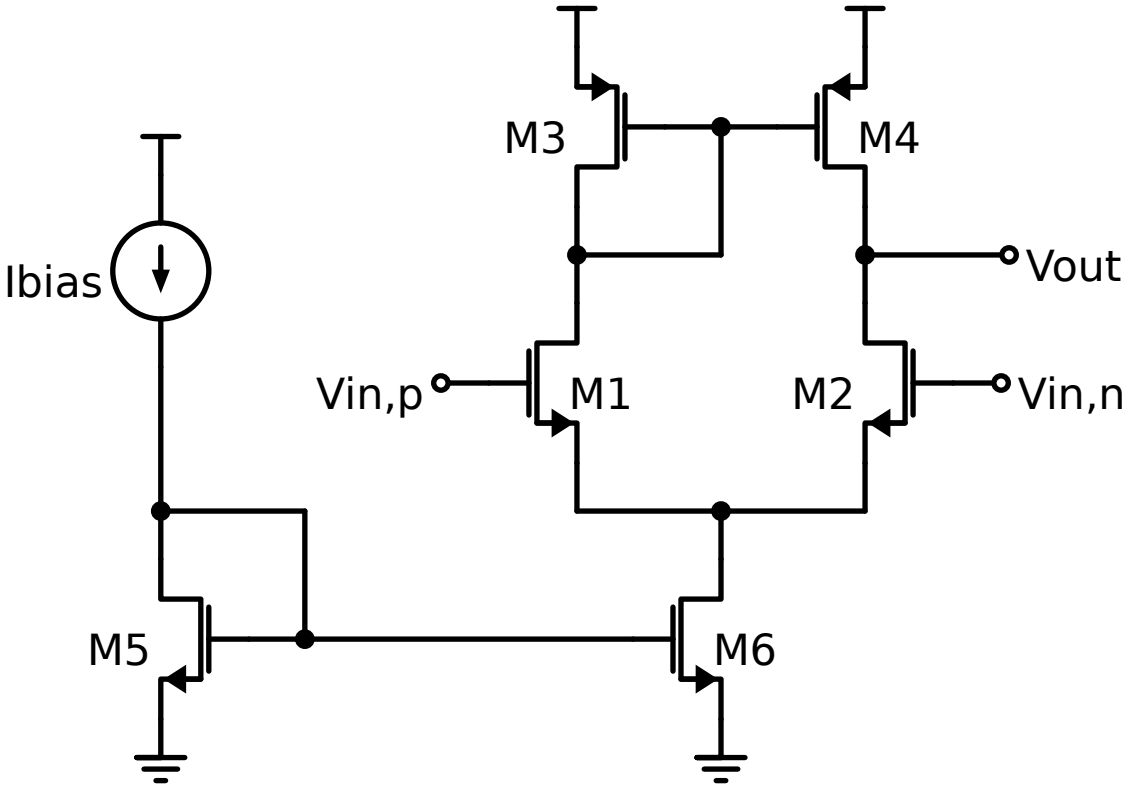

Figure 20: The 5-transistor OTA.

Source: Article Notebook

The operation is as follows: $M_{1,2}$ form a differential pair which is biased by the current source M_6. $M_{5,6}$ form a current mirror, thus the input bias current I_{bias} sets the bias current in the OTA. The differential pair $M_{1,2}$ is loaded by the current mirror $M_{3,4}$ which mirrors the output current of M_1 to the right side. Here, the currents from M_4 and M_2 are summed, and together with the conductance effective at the output node a voltage builds up.

As this is an OTA the output is a current; if the load impedance is high (i.e., purely capacitive) then the voltage gain of the OTA can be high (of course, in this simple OTA it is limited). With a high-impedance loading this OTA can provide a voltage output, and this is actually how OTAs are mostly operated.

Voltage Buffer with OTA

In order to design an OTA we need an application, and from this we need to derive the circuit specifications. We want to use this OTA to realize a voltage buffer which lighly loads a voltage source and can drive a large capacitive load. Such a configuration is often used to, e.g., buffer a reference voltage that is needed (and thus loaded) by another circuit. The block diagram of this configuration is shown in Figure 21.

Source: Article Notebook

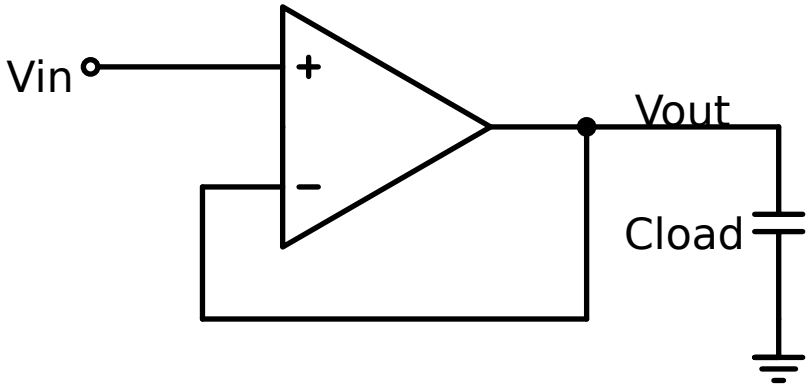

Figure 21: A voltage buffer (based on OTA) driving a capacitive load.

Source: Article Notebook

If the voltage gain of the OTA is Figure 21 is high, then $V_{\text{out}} \approx V_{\text{in}}$. We now want to design an OTA for this application for the following spefication values (see Table 1).

Table 1: Voltage buffer specification

Specification	Value	Unit
Load capacitance C_{load}	50	fF
Input voltage range (for buffering bandgap voltage)	1.1—1.3	V
Signal bandwidth (3dB)	>1	MHz
Voltage gain error	<1	%
Total output noise (rms)	<1	mV_{rms}
Supply voltage	1.45—1.5—1.55	V
Supply current (as low as possible)	<100	µA
Stability	stable for rated C_{load}	
Turn-on time (settled to with 1%)	<10	µs
Externally provided bias current (nominal)	20	µA

Large-Signal Analysis of the OTA

The first step when receiving a design task is to look at the specifications, and see whether they make sense. Detailed performance of the design will be the result of the circuit simulation, but before we step into sizing we need to do a few simple calculations to (a) allows to do back-of-the-envelope gauging if the specification makes sense, and (b) the derived analytical equations will serve as guide for the sizing procedure.

- In terms of large-signal operation, we will now check whether the input and output voltage range, as well as the settling time can be roughly met.
- When the input is at its maximum of 1.3 V, we see that we need to keep M_1 in saturation. We can calculate that $V_{\mathrm{DS1}} = V_{\mathrm{DD}} - V_{\mathrm{GS3}} + V_{\mathrm{GS1}} - V_{\mathrm{in}} = 1.45 - 0.6 + 0.6 - 1.3 = 0.15\,\mathrm{V}$, which barely leaves enough margin, so we must keep the gate-source voltages of M_1 and M_3 resonably small.
- When the input is at its minimum of 1.1 V, we see that the V_{DS} of M_6 is calculated as $V_{\mathrm{DS6}} = V_{\mathrm{in}} - V_{\mathrm{GS1}} = 1.1 - 0.6 = 0.5\,\mathrm{V}$, so this leaves plenty of margin.
- For the output voltage, when the output voltage is on the high side, it leaves $V_{\mathrm{DS4}} = V_{\mathrm{DD}} - V_{\mathrm{out}} = 1.45 - 1.3 = 0.15\,\mathrm{V}$, whis is on the edge.
- When the output voltage is on the low side, it leaves $V_{\mathrm{DS2}} = V_{\mathrm{out}} - V_{\mathrm{in}} + V_{\mathrm{GS2}} = 1.3 - 1.55 + 0.6 = 0.35\,\mathrm{V}$, so this should work.

In summary, we think that we can make an NMOS-input OTA like the one in Figure 20 work for the required supply and input- and output voltages. If this would not work out, we need to look for further options, like a PMOS-input OTA, or a NMOS/PMOS-input OTA.

Another large-signal specification item that we can quickly check is the settling time. Under slewing conditions, we complete bias current in the OTA is steered towards the output (try to understand why this is the case), so when the output capacitor is fully discharged, and we assume just a linear ramp due to constant-current charging of the output capacitor, the settling time is

$$T_{\mathrm{slew}} \approx \frac{C_{\mathrm{load}} V_{\mathrm{out}}}{I_{\mathrm{tail}}} = \frac{50 \cdot 10^{-15} \cdot 1.3}{100 \cdot 10^{-6}} = 0.65\,\mathrm{ns}$$

so this leaves plenty of margin for additional slow-signal settling due to the limited bandwidth, as well as reducing the supply current.

The small-signal settling (assuming one pole at the bandwidth corner frequency) leads to an approximate settling time (1% error corresponds to $\approx 5\tau$) of

$$T_{\mathrm{slew}} \approx \frac{5}{2\pi f_{\mathrm{c}}} = \frac{5}{2\pi \cdot 1 \cdot 10^{-6}} = 0.8\,\mu\mathrm{s}.$$

which also checks out.

Small-Signal Analysis of the OTA

Cascode Stage

A Fully-Differential OTA

Biasing the OTA

An RC-OPAMP Filter

Summary & Conclusion

Appendix: ngspice Cheat Sheet

Appendix: Xschem Cheat Sheet

Source: Article Notebook

Hellen, Edward H. 2003. "Verifying the diode–capacitor circuit voltage decay." *American Journal of Physics* 71 (8): 797–800. https://doi.org/10.1119/1.1578070.

Hu, Chenming. 2010. *Modern Semiconductor Devices for Integrated Circuits*. Pearson.

Jespers, Paul G. A., and Boris Murmann. 2017. *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge University Press.

Middlebrook, R. D. 1975. "Measurement of loop gain in feedback systems." *International Journal of Electronics* 38 (4): 485–512. https://doi.org/10.1080/00207217508920421.

Nagel, Laurence W. 1975. "SPICE2: A Computer Program to Simulate Semiconductor Circuits." PhD thesis, EECS Department, University of California, Berkeley. http://www2.eecs.berkeley.edu/Pubs/TechRpts/1975/9602.html.

Tsividis, Yannis, and Colin McAndrew. 2011. *Operation and Modeling of the MOS Transistor*. Oxford University Press.