

```
.option sparse
.temp 27
.param wx=5u lx=0.13u vbx=0
.noise v(n) vg lin 1 1 1 1
.control
option numdgt=3
set wr_singlescale
set wr_vecnames

compose l_vec values 0.13u 0.2u 0.3u 0.4u 0.5u 1u 5u 10u
compose vg_vec start= 0 stop=1.5 step=25m
compose vd_vec start= 0 stop=1.5 step=25m
compose vb_vec values 0 0.4 0.8 1.2

foreach var1 $&l_vec
    alterparam lx=$var1
    reset
    foreach var2 $&vg_vec
        alter vg $var2
        foreach var3 $&vd_vec
            alter vd $var3
            foreach var4 $&vb_vec
                alter vsb $var4
                run
                wrdata techsweep_sg13_lv_pmos.txt noise1.all
                destroy all
                set appendwrite
                unset set wr_vecnames
            end
        end
    end
end
end
end

set appendwrite=0

alterparam lx=0.13u
alterparam vbx=0
reset
op
*showmod
show
write techsweep_sg13g2_lv_pmos.raw
.endc
```

→ simulate
→ annotate

The circuit diagram shows a PMOS transistor model. The gate is connected to GND, the source is connected to VG (0.65 AC 1), and the drain is connected to VB (0).

```
.lib cornerMOSlv.lib mos_tt
```

```
.save b d g n
.save @n.xm1.nsg13_lv_pmos[cgso]
.save @n.xm1.nsg13_lv_pmos[cgdo]
.save @n.xm1.nsg13_lv_pmos[cd]
.save @n.xm1.nsg13_lv_pmos[cb]
.save @n.xm1.nsg13_lv_pmos[cd]
.save @n.xm1.nsg13_lv_pmos[cg]
.save @n.xm1.nsg13_lv_pmos[cs]
.save @n.xm1.nsg13_lv_pmos[cs]
.save @n.xm1.nsg13_lv_pmos[gs]
.save @n.xm1.nsg13_lv_pmos[gm]
.save @n.xm1.nsg13_lv_pmos[gm]
.save @n.xm1.nsg13_lv_pmos[ids]
.save @n.xm1.nsg13_lv_pmos[l]
.save @n.xm1.nsg13_lv_pmos[vgs]
.save @n.xm1.nsg13_lv_pmos[vds]
.save @n.xm1.nsg13_lv_pmos[vsb]
.save @n.xm1.nsg13_lv_pmos[vth]
.save @n.xm1.nsg13_lv_pmos[vdss]
.save @n.xm1.nsg13_lv_pmos[fug]
.save @n.xm1.nsg13_lv_pmos[sid]
.save @n.xm1.nsg13_lv_pmos[sf]
.save @n.xm1.nsg13_lv_pmos[cjd]
.save @n.xm1.nsg13_lv_pmos[cjs]
.save @n.xm1.nsg13_lv_pmos[rq]
```

[illegible]

```
gm=?
gds=?
vth=?
vdss(vds_sat)=?
cgs=?
fug(f_t)=?
cdg=?
rg=?
sid=?
```