Analog Circuit Design

Harald Pretl

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Table of contents

Introduction

This is the material for an intermediate-level MOSFET circuit design course, held at JKU under course number 336.009 ("KV Analoge Schaltungstechnik").

The course makes heavy use of circuit simulation, using **Xschem** for schematic entry and **ngspice** for simulation. The 130nm CMOS technology **SG13G2** from IHP Microelectronics is used.

Tools and PDK are integrated in the **IIC-OSIC-TOOLS** Docker image, which will be used during the coursework.

The MOSFET

In this first chapter we will learn to use Xschem for schematic entry, and how to operate the ngspice SPICE simulator for circuit simulations. Further, we will make ourself familiar with the transistor and other passive components available in the IHP Microelectronics SG13G2 technology. While this is strictly speaking a BiCMOS technology offering MOSFETs as well as SiGe HBTs, we will use it as a pure CMOS technology.

IHP's SG13G2 130nm CMOS Technology

SG13G2 is the name of a 130nm CMOS technology (strictly speaking BiCMOS) from IHP Microelectronics. It features low-voltage (thin-oxide) core MOSET, high-voltage (thick-oxide) I/O MOSFET, various types of linear resistors, and 7 layers of Aluminium metallization (5 thin, 2 thick metal layers). This PDK is open-source, and the complete process specification can be found at SG13G2 process specification. While we will not do layouts in this course, the layout rules can be found at SG13G2 layout rules.

For our circuit design, the most important parameters of the available devices are summarized in the following:

- **Low-voltage NMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx 0.5\,\mathrm{V}$; a triple-well option for the NMOS is available.
- **Low-voltage PMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx -0.47\,\mathrm{V}$.
- **High-voltage NMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 3.3\,\mathrm{V}$, $L_{\mathrm{min}} = 0.45\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx 0.7\,\mathrm{V}$; a triple-well option for the NMOS is available.
- **High-voltage PMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx -0.65\,\mathrm{V}$.
- **Silicided poly resistor**: $R_{\square} = 7\,\Omega \pm 10\%$, $\mathrm{TC}_1 = 3100\,\mathrm{ppm/K}$
- **Poly resistor**: $R_{\square} = 260\,\Omega \pm 10\%$, $\mathrm{TC}_1 = 170\,\mathrm{ppm/K}$
- **Poly resistor high**: $R_{\square} = 1360\,\Omega \pm 15\%$, $\mathrm{TC}_1 = -2300\,\mathrm{ppm/K}$
- **MIM capacitor**: $C = 1.5\,\mathrm{fF}/\mu\mathrm{m}^2 \pm 10\%$, $\mathrm{VC}_1 = -26\mathrm{ppm/V}$, $\mathrm{TC}_1 = 3.6\mathrm{ppm/K}$, breakdown voltage $> 15\,\mathrm{V}$
- **MOM capacitor**: Well-suited metal stack due to 5 thin metal layers, but no primitive capacitor available.