Analog Circuit Design

Harald Pretl

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Introduction

This is the material for an intermediate-level MOSFET circuit design course, held at JKU under course number 336.009 ("KV Analoge Schaltungstechnik").

The course makes heavy use of circuit simulation, using **Xschem** for schematic entry and **ngspice** for simulation. The 130nm CMOS technology **SG13G2** from IHP Microelectronics is used.

Tools and PDK are integrated in the **IIC-OSIC-TOOLS** Docker image, which will be used during the coursework.

All course material is made publicly available and shared under the Apache-2.0 license.

IHP's SG13G2 130nm CMOS Technology

SG13G2 is the name of a 130nm CMOS technology (strictly speaking BiCMOS) from IHP Microelectronics. It features low-voltage (thin-oxide) core MOSET, high-voltage (thick-oxide) I/O MOSFET, various types of linear resistors, and 7 layers of Aluminium metallization (5 thin, 2 thick metal layers). This PDK is open-source, and the complete process specification can be found at SG13G2 process specification. While we will not do layouts in this course, the layout rules can be found at SG13G2 layout rules.

For our circuit design, the most important parameters of the available devices are summarized in the following:

- **Low-voltage NMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx 0.5\,\mathrm{V}$; a triple-well option for the NMOS is available.
- **Low-voltage PMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx -0.47\,\mathrm{V}$.
- **High-voltage NMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 3.3\,\mathrm{V}$, $L_{\mathrm{min}} = 0.45\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx 0.7\,\mathrm{V}$; a triple-well option for the NMOS is available.
- **High-voltage PMOS**: Operating voltage nom. $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx -0.65\,\mathrm{V}$.
- **Silicided poly resistor**: $R_{\square} = 7\,\Omega \pm 10\%$, $\mathrm{TC}_1 = 3100\,\mathrm{ppm/K}$
- **Poly resistor**: $R_{\square} = 260\,\Omega \pm 10\%$, $\mathrm{TC}_1 = 170\,\mathrm{ppm/K}$
- **Poly resistor high**: $R_{\square} = 1360\,\Omega \pm 15\%$, $\mathrm{TC}_1 = -2300\,\mathrm{ppm/K}$
- **MIM capacitor**: $C = 1.5\,\mathrm{fF}/\mu\mathrm{m}^2 \pm 10\%$, $\mathrm{VC}_1 = -26\mathrm{ppm/V}$, $\mathrm{TC}_1 = 3.6\mathrm{ppm/K}$, breakdown voltage $> 15\,\mathrm{V}$
- **MOM capacitor**: Well-suited metal stack due to 5 thin metal layers, but no primitive capacitor available.

Schematic Entry Using Xschem

Xschem is an open-source schematic entry tool with emphasis on integrated circuits. For up-to-date information of the many features of Xschem please look at the online documentation. Usage of Xschem will be learned with the first few basic examples, essentially a single MOSFET. The usage model of Xschem is that the schematic is hierarchically drawn, and the simulation and evaluation statements are contained in the schematics. Further, Xschem offers embedded graphing, which we will mostly use.

Circuit Simulation Using ngspice

ngspice is an open-source circuit simulator with SPICE dependency. Besides the usual simulated types like `op` (operating point), `dc` (dc sweeps), `tran` (time-domain), or `ac` (for small-signal frquency sweeps), ngspice offers a script-like control interface, where many

different simulation controls and result evaluations can be done. For detailed information please refer to the latest manual.

Integrated IC Design Environment (IIC-OSIC-TOOLS)

In order to make usage of the various required components (tools like Xschem, PDK like SG13G2) easier, we will use the IIC-OSIC-TOOLS. This is a pre-setup Docker image which allows to design on a virtual machine on virtually any type of computing equipment. For further information like installed tools, how to setup a VM, etc. please look at IIC-OSIC-TOOLS GitHub page.

Experienced users can install this image on their personal computer, for JKU students the IIC will host a VM on our compute cluster and provide personal login credentials.

First Steps

In this first chapter we will learn to use Xschem for schematic entry, and how to operate the ngspice SPICE simulator for circuit simulations. Further, we will make ourself familiar with the transistor and other passive components available in the IHP Microelectronics SG13G2 technology. While this is strictly speaking a BiCMOS technology offering MOSFETs as well as SiGe HBTs, we will use it as a pure CMOS technology.

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET)

A first step in any new IC technology should be to investigate basic MOSFET performance, by doing simple dc sweeps of V_{GS} and V_{DS} and looking at I_{DS} and other large- and small-signal parameters.

As this is an intermediate-level course, some basic knowledge about MOSFET operation, basic device equations, and small-signal equivalent circuits is assumed. This knowledge will be practiced, though, throughout the course, by doing exercises to compare hand calculation with actual simulation results. JKU students should be familiar with the MOSFET chapter from "Design of Complex Integrated Circuits" (VL 336.048).

In order to get started, basic Xschem testbenches are prepared.

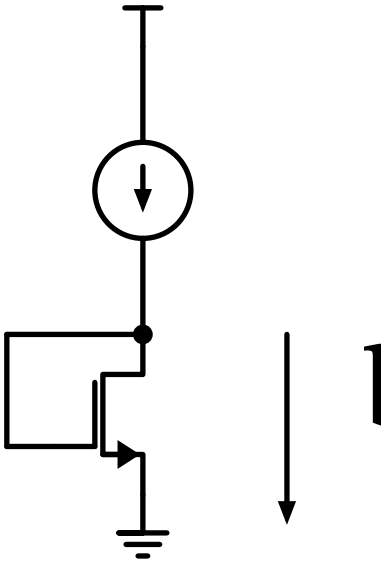
Student Exercise

We start with a simple testbench for the LV NMOS, see here.

1. Try to get the LV NMOS testbench at https://github.com/iic-jku/analog-circuit-design/blob/main/xschem/dc_lv_nmos.sch working in your IIC-OSIC-TOOLS environment.
2. Make yourself familiar with Xschem (change the schematic, run a simulation, graph the result).

3. Make youself familiar with ngspice (run various simulations, save nets and parameters, use the embedded Xschem graphing, explore the interactive ngspice shell to look and MOSFET model parameters).
4. Explore the LV NMOS
    1. How are g_m, g_ds, and V_th changing when you change the dc node voltages?
    2. Can you hand-calculate g_m? Does it fit? See what happens when $V_\mathrm{GS} > V_\mathrm{th}$ or $V_\mathrm{GS} < V_\mathrm{th}$, and concurrently vary V_DS.
    3. Change W and L of the MOSFET. What is the impact on the above parameters? Can you explain the variations?
    4. How is V_th changing with W and L? Can you explain what you are seeing.
    5. Take a look at the device capacitances C_GG and C_GD. Why are they important? What is the relation to f_T?
    6. When looking at the model parameters in ngspice, you see that there is a C_GD and a C_DG. Why, what is the difference? Sometimes these capacitors show a negative value, why?
    7. In this course we will only consider the drain-source current noise of the MOSFET. Look at the simulated value and compare with a hand calculation of the noise. In the noise equation there is the factor γ, which in triode is $\gamma = 1$ and in saturation is $\gamma = 2/3$ according to basic text books. Which value of γ are you calculating? Why might it be different?
5. Build test benches in Xschem for the LV PMOS, the HV NMOS, and the HV PMOS. Explore the different results.
    1. Which is the fastest device? Why?
    2. What is the difference in g_m and other parameters between these four different MOSFETs? Why?
    3. If you would have to size an inverter, what would be the ideal ratio of W_p/W_n? Will you exactly design this ratio, or are the reasons to deviate?
    4. There are LV and HV MOSFETs, and you investigated the difference in performance. What is the rationale when designing circuits for selection either an LV type, and when to choose an HV type?
6. Build a test bench to explore the body effect, start with LV NMOS.
    1. What happens when $V_\mathrm{BS} \neq 0$?
    2. What is the ratio of g_m to g_mB? What is the physical reason behind this ratio (you might want to revisit MOSFET device physics at this point)?

First Circuit: MOSFET Diode



Source: Article Notebook

Transistor Sizing Using Inversion Coefficient

Current Mirror

Differential Pair

Cascode Stage

A Basic 5-Transistor OTA

A Fully-Differential OTA

Biasing the OTA

An RC-OPAMP Filter

Summary & Conclusion

Appendix: ngspice Cheat Sheet

Appendix: Xschem Cheat Sheet

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