Analog Circuit Design

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Introduction

This is the material for an intermediate-level MOSFET circuit design course, held at JKU under course number 336.009 ("KV Analoge Schaltungstechnik").

The course makes heavy use of circuit simulation, using **Xschem** for schematic entry and **ngspice** for simulation. The 130nm CMOS technology **SG13G2** from IHP Microelectronics is used.

Tools and PDK are integrated in the **IIC-OSIC-TOOLS** Docker image, which will be used during the coursework.

> **Note**
>
> All course material is made publicly available on GitHub and shared under the Apache-2.0 license.

IHP's SG13G2 130nm CMOS Technology

SG13G2 is the name of a 130nm CMOS technology (strictly speaking BiCMOS) from IHP Microelectronics. It features low-voltage (thin-oxide) core MOSFET, high-voltage (thick-oxide) I/O MOSFET, various types of linear resistors, and 7 layers of Aluminium metallization (5 thin plus 2 thick metal layers). This PDK is open-source, and the complete process specification can be found at SG13G2 process specification. While we will not do layouts in this course, the layout rules can be found at SG13G2 layout rules.

For our circuit design, the most important parameters of the available devices are summarized in the following:

- **Low-voltage NMOS**: Device `sg13_lv_nmos`; operating voltage nominal $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx 0.5\,\mathrm{V}$; a triple-well option for the NMOS is available.
- **Low-voltage PMOS**: Device `sg13_lv_pmos`; operating voltage nominal $V_{\mathrm{DD}} = 1.5\,\mathrm{V}$, $L_{\mathrm{min}} = 0.13\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx -0.47\,\mathrm{V}$.
- **High-voltage NMOS**: Device `sg13_hv_nmos`; operating voltage nominal $V_{\mathrm{DD}} = 3.3\,\mathrm{V}$, $L_{\mathrm{min}} = 0.45\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx 0.7\,\mathrm{V}$; a triple-well option for the NMOS is available.
- **High-voltage PMOS**: Device `sg13_hv_pmos`; operating voltage nominal $V_{\mathrm{DD}} = 3.3\,\mathrm{V}$, $L_{\mathrm{min}} = 0.45\,\mu\mathrm{m}$, $V_{\mathrm{th}} \approx -0.65\,\mathrm{V}$.
- **Silicided poly resistor**: Device `rsil`; $R_{\square} = 7\,\Omega \pm 10\%$, $\mathrm{TC}_1 = 3100\,\mathrm{ppm/K}$
- **Poly resistor**: Device `rppd`; $R_{\square} = 260\,\Omega \pm 10\%$, $\mathrm{TC}_1 = 170\,\mathrm{ppm/K}$
- **Poly resistor high**: Device `rhigh`; $R_{\square} = 1360\,\Omega \pm 15\%$, $\mathrm{TC}_1 = -2300\,\mathrm{ppm/K}$
- **MIM capacitor**: Device `cap_cmim`; $C' = 1.5\,\mathrm{fF}/\mu\mathrm{m}^2 \pm 10\%$, $\mathrm{VC}_1 = -26\mathrm{ppm/V}$, $\mathrm{TC}_1 = 3.6\mathrm{ppm/K}$, breakdown voltage $> 15\,\mathrm{V}$
- **MOM capacitor**: The metal stack is well-suited for MOM capacitors due to 5 thin metal layers, but no primitive capacitor device is available at this point.

Schematic Entry Using Xschem

Xschem is an open-source schematic entry tool with emphasis on integrated circuits. For up-to-date information of the many features of Xschem and the basic operation of it please look at the available online documentation. Usage of Xschem will be learned with the first few basic examples, essentially using a single MOSFET. The usage model of Xschem is that the schematic is hierarchically drawn, and the simulation and evaluation statements are contained in the schematics. Further, Xschem offers embedded graphing, which we will mostly use.

Circuit Simulation Using ngspice

ngspice is an open-source circuit simulator with SPICE dependency (Nagel 1975). Besides the usual simulated types like `op` (operating point), `dc` (dc sweeps), `tran` (time-domain), or `ac` (small-signal frquency sweeps), ngspice offers a script-like control interface, where many different simulation controls and result evaluations can be done. For detailed information please refer to the latest online manual.

Integrated IC Design Environment (IIC-OSIC-TOOLS)

In order to make use of the various required components (tools like Xschem and ngspice, PDKs like SG13G2) easier, we will use the **IIC-OSIC-TOOLS**. This is a pre-compiled Docker image which allows to do circuit design on a virtual machine on virtually any type of computing equipment (personal PC, Raspberry Pi, cloud server) on various operating systems (Windows, macOS, Linux). For further information like installed tools, how to setup a VM, etc. please look at IIC-OSIC-TOOLS GitHub page.

> **Tip**
>
> Please make sure to receive information about your personal VM access ahead of the course start.

Experienced users can install this image on their personal computer, for JKU students the IIC will host a VM on our compute cluster and provide personal login credentials.

> **Note**
>
> In this course, we assume that students have a basic knowledge of Linux and how to operate it using the terminal. If you are not yet familiar with Linux (which is basically a must when doing integrated circuit design as many tools are only available on Linux), then please check out a Linux introductory course or tutorial online, there are many ressources available.

First Steps

In this first chapter we will learn to use Xschem for schematic entry, and how to operate the ngspice SPICE simulator for circuit simulations. Further, we will make ourself familiar with the transistor and other passive components available in the IHP Microelectronics SG13G2 technology. While this is strictly speaking a BiCMOS technology offering MOSFETs as well as SiGe HBTs, we will use it as a pure CMOS technology.

The Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET)

In this course, we will not dive into semiconductor physics and derive the device operation bottom-up starting from a fundamental level governed by quantum mechanics. Instead, we will treat the MOSFET as a macroscopic by assuming we have a 4-terminal device, and the performance of this device regarding its terminal voltages and currents we will largely derive from the simulation model.

The circuit symbol that we will use for the n-channel MOSFET is shown in Figure 1, and for the p-channel MOSFET it is shown in Figure 2. A control voltage between gate ("G") and source ("S") causes a current to flow between drain ("D") and source. The MOSFET is a 4-terminal device, so the bulk ("B") can also control the drain-source current flow. Often, the bulk is connected to source, and then the bulk terminal is not shown to declutter the schematics.

> **Note**
>
> Strictly speaking is the drain-source current of a MOSFET controlled by the voltage between gate and bulk and the voltage between drain and source. Since bulk is often connected to source anyway, and many circuit designers historically were already familiar with the operation of the bipolar junction transistor, it is common to consider the gate-source voltage (besides the drain-source voltage) as the controlling voltage. This focus on gate-source implies that the source is special compared to the drain. In a typical physical MOSFET, however, the drain and source are constructed exactly the same, and which terminal is drain, and which terminal is source, is only determined by the applied voltage potentials, and can change dynamically during operation (think of a MOSFET operating as a switch… which side is the drain, which side is the source?). Unfortunately, this focus on a "special" source has made its way into some MOSFET compact models. The model that is used in SG13G2 luckily uses the PSP model, which is formulated symmetrically with regards to drain and source, and is thus very well suited for analog and RF circuit design. For a detailed understanding of the PSP model please refer to the model documentation.

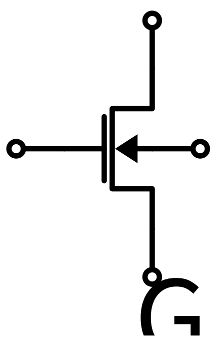

Figure 1: Circuit symbol of n-channel MOSFET.

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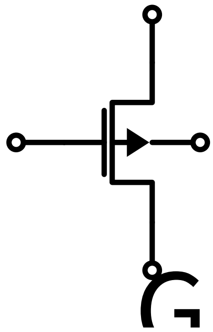

Figure 2: Circuit symbol of p-channel MOSFET.

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For hand calculations and theoretical discussions we will use the following simplified large-signal model, shown in Figure 3. A current source I_{DS} models the current flow between drain and source, and it is controlled by the three control voltages V_{GS}, V_{DS}, and V_{SB}. Note that in this way (since $I_{\text{DS}} = f(V_{\text{DS}})$) also a resistive behavior between D and S can be modelled. In case that B and S are shorted then simply $V_{\text{SB}} = 0$.

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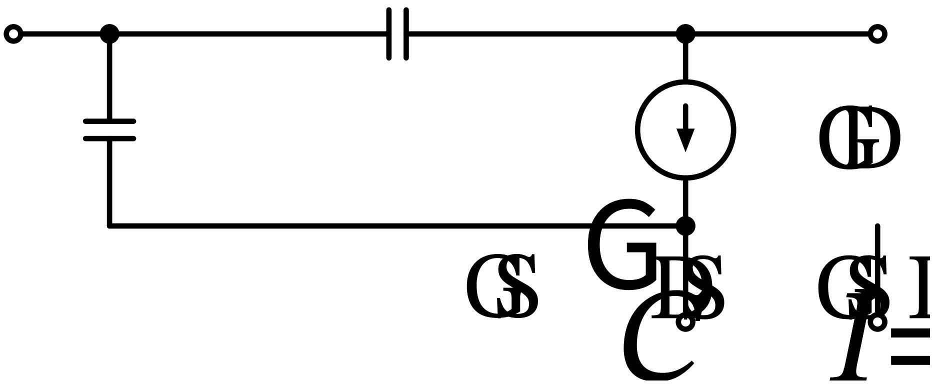

Figure 3: The MOSFET large-signal model.

Source: Article Notebook

In an ideal MOSFET no dc current is flowing into the gate, the behavior is purely capacitive. We model this by two capacitors: $C_{\text{GG}} = C_{\text{GS}} + C_{\text{GD}}$ is the total capacitance when looking into the gate of the MOSFET. C_{GS} is usually the dominant capacitance, and C_{GD} models the capacitive feedback between D and G, usually induced by a topological overlap capacitance in the physical construction of the MOSFET. This capacitance is often small compared to C_{GS}, but in situations where we have a large voltage swing at the drain this capacitance will be affected by the Miller effect. In hand calculations we will often set $C_{\mathrm{GD}} = 0$.

> **Note**
>
> The bulk connection in Figure 3 seems floating as we only consider it a control terminal, where the potential difference between source and bulk influences the behaviour of the MOSFET. However, we do not consider resistive or capacitive effects associated with this node, which is of course a gross simplification, but nevertheless one we will make in this course.

Now, as we are skipping the bottom-up approach of deriving the MOSFET large-signal behaviour from basic principles, we need to understand the behaviour of the elements of the large-signal model in Figure 3 by using a circuit simulator and observing what happens. And generally, a first step in any new IC technology should be to investigate basic MOSFET performance, by doing simple dc sweeps of V_{GS} and V_{DS} and looking at I_{DS} and other large- and small-signal parameters.

As a side note, the students who want to understand MOSFET behaviour from a physical angle should consult the MOSFET chapter from the JKU course "Design of Complex Integrated Circuits" (VL 336.048). A great introduction into MOSFET operation and fabrication is given in (Hu 2010), which is available freely online and is a recommended read. A very detailed description of the MOSFET (leaving usually no question unanswered) is provided in (Tsividis and McAndrew 2011).

Now, in order to get started, basic Xschem testbenches are prepared, and first simple dc sweeps of various voltages and currents will be done. But before that, please look at the import note below!

> **Important**
>
> Throughout this material, we will stick to the following notations:
>
> - A **dc quantity** is shown with an upper-case letter with upper-case subscripts, like V_{GS}.
> - Double-subscripts denote **dc sources**, like V_{DD} and V_{SS}.
> - An **ac (small-signal) quantity** is a lower-case letter with a lower-case subscript, like g_{m}.
> - A **total quantity** (dc plus ac) is shown as a lowercase letter with upper-case subscript, like i_{DS}.
> - A upper-case letter with a lower-case subscript is used to denote **RMS quantities**, like I_{ds}.

Large-Signal MOSFET Model

We start with an investigation into the large-signal MOSFET model shown in Figure 3 by using the simple testbench for the LV NMOS shown in Figure 4.

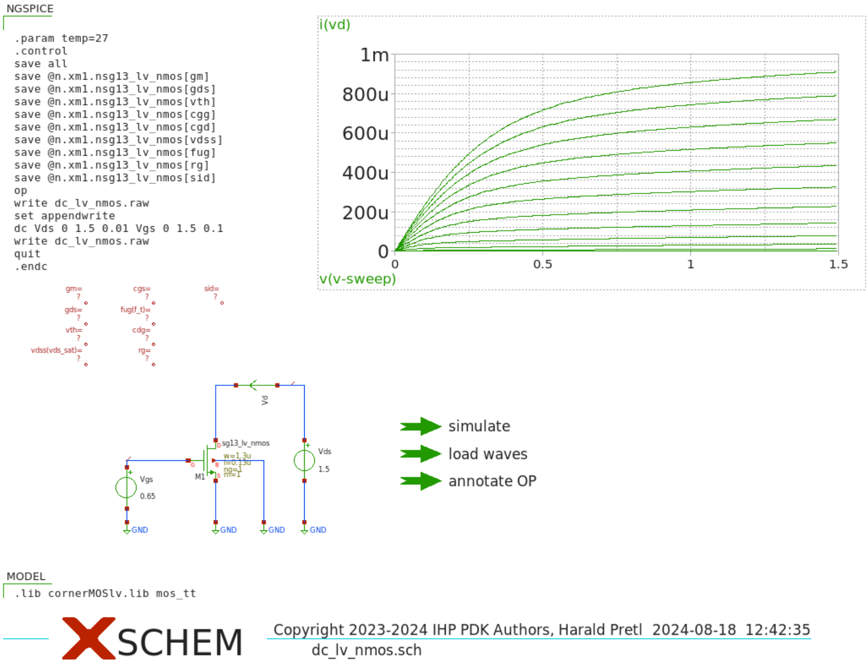

Figure 4: Testbench for NMOS dc sweeps.

Exercise

Please try to execute the following steps and answer these questions:

1. Get the LV NMOS testbench (available at https://github.com/iic-jku/analog-circuit-design/blob/main/xschem/dc_lv_nmos.sch) working in your IIC-OSIC-TOOLS environment.
2. Make yourself familiar with Xschem (change the schematic in various ways, run a simulation, graph the result).
3. Make youself familiar with ngspice (run various simulations, save nets and parameters, use the embedded Xschem graphing, explore the interactive ngspice shell to look at MOSFET model parameters).
4. Explore the LV NMOS `sg13_lv_nmos`:
    1. How is I_{DS} affected by V_{GS} and V_{DS}?
    2. Change W and L of the MOSFET. What is the impact on the above parameters? Can you explain the variations?
    3. When looking at the model parameters in ngspice, you see that there is a C_{GD} and a C_{DG}. Why is this, what could be the difference? Sometimes these capacitors show a negative value, why?
5. Build testbenches in Xschem for the LV PMOS, the HV NMOS, and the HV PMOS. Explore the different results.

    1. For a given W and L, which device provides more drain current? How are the capacitances related?
    2. If you would have to size an inverter, what would be the ideal ratio of W_p/W_n? Will you exactly design this ratio, or are the reasons to deviate?
    3. There are LV and HV MOSFETs, and you investigated the difference in performance. What is the rationale when designing circuits for selection either an LV type, and when to choose an HV type?

6. Build a test bench to explore the body effect, start with LV NMOS.

    1. What happens when $V_{\mathrm{BS}} \neq 0$?

Small-Signal MOSFET Model

As you have seen in the previous investigations, the large-signal model of Figure 3 describes the behaviour of the MOSFET across a wide range of voltages applied at the MOSFET terminals. Unfortunately, for hand analysis dealing with a nonlinear model is close to impossible, at the very least it is quite tedious.

However, for many practical situations, we bias a MOSFET with a set of dc voltages applied to its terminal, and only apply small signal excursions during operation. If we do this, we can linearize the large-signal model in this dc operating point, and resort to a small-signal model which can be very useful for hand calculations. Many experienced designers analyze their circuits by doing these kind of hand calculations and describing the circuit analytically, which is a great way to understand fundamental performance limits and relationships between parameters.

We will use the small-signal MOSFET model shown in Figure 5 for this course. The current-source $i_{\mathrm{ds}} = g_{\mathrm{m}} v_{\mathrm{gs}}$ models the drain current as a function of v_{gs}, and the resistor g_{ds} models the dependency of the drain current by v_{ds}. The drain current dependency on the source-bulk voltage (the so-called "body effect") is introduced by the current source $i_{\mathrm{ds}} = g_{\mathrm{mb}} v_{\mathrm{sb}}$.

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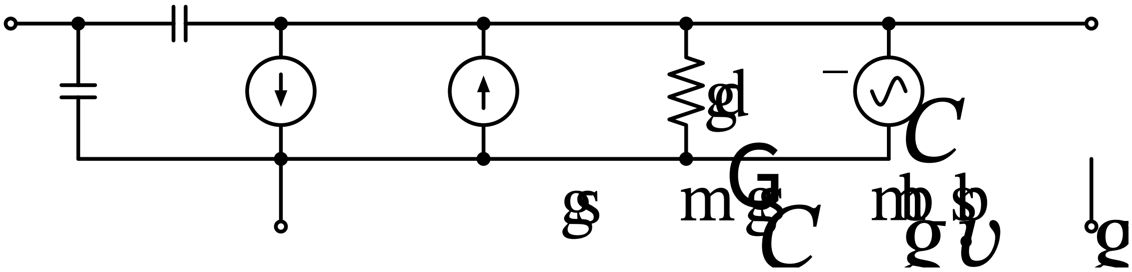


Figure 5: The MOSFET small-signal model.

Source: Article Notebook

As any electronic device the MOSFET introduces noise into the circuit. In this course we will only consider the drain-source current noise of the MOSFET, given by $\overline{I_\mathrm{n}^2} = 4kT\gamma g_\mathrm{d0}$ ($\overline{I_\mathrm{n}^2}$ is the power-spectral density of the noise in A^2/Hz; k is the Boltzmann constant; T is the absolute temperature; γ is a parameter in simplified theory changing between $\gamma = 2/3$ in saturation and $\gamma = 1$ for triode operation; g_d0 is equal to g_m in saturation and g_ds in triode).

Note

Sometimes we will refer to different operating modes of the MOSFET like "saturation" or "triode". Generally speaking, when the drain-source voltage is small, then the MOSFET acts as a resistor, and this mode of operation we call "triode" mode. When the drain-source voltage is increased, at some point the drain-source current saturates and is no longer a strong function of the drain-source voltage. This mode is called "saturation" mode. As you can see in the large-signal investigations, these transitions happen gradually, and it is difficult to define a precise point where one operating mode switches to the other one. In this sense we use terms like "triode" and "saturation" only in an approximative sense.

Now we need to see how the small-signal parameters seen in Figure 5 can be investigated and estimated using circuit simulation.

Exercise

Please try to execute the following steps and answer the following questions:

1. Reuse the LV NMOS testbench (available at https://github.com/iic-jku/analog-circuit-design/blob/main/xschem/dc_lv_nmos.sch).
2. Explore the LV NMOS `sg13_lv_nmos`:
    1. How are g_m and g_ds changing when you change the dc node voltages?
    2. What is the ratio of g_m to g_mb? What is the physical reason behind this ratio (you might want to revisit MOSFET device physics at this point)?
    3. Take a look at the device capacitances C_gs and C_gd. Why are they important? What is the relation to f_T? *Note: f_T is the transit frequency where the current gain of the MOSFET drops to 1, and can be approximated by* $2\pi f_\mathrm{T} = g_\mathrm{m}/C_\mathrm{gg}$.
    4. Look at the drain noise current according to the MOSFET model and compare with a hand calculation of the noise. In the noise equation there is the factor γ, which in triode is $\gamma = 1$ and in saturation is $\gamma = 2/3$ according to basic text books. Which value of γ are you calculating? Why might it be different?
3. Go back to your testbench for the LVS PMOS `sg13_lv_pmos`:
    1. What is the difference in g_m, g_ds, and other parameters between the NMOS and the PMOS? Why could they be different?

Conclusion

Congratulations for making it thus far! By now you should have a solid grasp of the tool handling of Xschem and ngspice, and you should be familiar with the large- and small-signal operation of both NMOS and PMOS, and the parameters describing these behaviours. If you feel you are not sufficiently fluent in these things, please go back to the beginning of Section and revisit the relevant sections, or dive into further reading about the MOSFET operation, like in (Hu 2010).

Transistor Sizing Using gm/ID Methodology

When designing integrated circuits it is an important question how to select various parameters of a MOSFET, like W, L, or the bias current I_D. In comparison to using discrete components in PCB design, or also compared to a bipolar junction transistor (BJT), we have these degrees of freedom, which make integrated circuit design so interesting.

Often, transistor sizing in entry-level courses is based on the square-law model, where a simple analytical equation for the drain current can be derived. However, in nanometer CMOS, the MOSFET behaviour is much more complex than these simple models. Also, this highly simplified derivations introduce concepts like the threshold voltage or the overdrive voltage, which are interesting from a theoretical viewpoint, but bear little practical use.

> **Note**
>
> One of the many simplifactions of the square-law model is that the mobility of the charge carriers is assumed constant (it is not). Further, the existance of a threshold voltage is assumed, but in fact this voltage is just existing given a certain definition, and depending on definition, its value changed. In addition, in nm CMOS, the threshold voltage is a function on many thing, like W and L.

An additional shortcoming of the square-law model is that it is only valid in strong inversion, i.e. for large V_GS where the drain current is dominated by the drift current. As soon as the gate-source voltage gets smaller, the square-law model breaks, as the drain current component based on diffusion currents gets dominant. Modern compact MOSFET models (like the PSP model used in SG13G2) use hundreds of parameters and fairly complex equations to somewhat properly describe MOSFET behaviour over a wide range of parameters like W, L, and temperature. A modern approach to MOSFET sizing is thus based on the thought to use exactly these MOSFET models, characterize them, put the resulting data into tables and charts, and thus learn about the complext MOSFET behaviour and use it for MOSFET sizing.

Being a well-established approach we select the $g_\mathrm{m}/I_\mathrm{D}$ methodology introduced by P. Jespers and B. Murmann in (Jespers and Murmann 2017). A brief introduction is available here as well.

The $g_\mathrm{m}/I_\mathrm{D}$ methodology has the huge advantage that is catches MOSFET behavior quite accurately over a wide range of operating conditions, and the curves look very similar for pretty much all CMOS technologies, form micrometer bulk CMOS down to nanometer FinFET devices. Of course the absolute values change, but the method applies universally.

MOSFET Characterization Testbench

In order to get the required tabulated data we use a testbench in Xschem which sweeps the terminal voltages, and records various large- and small-signal parameters, which are then stored in large tables. The testbench for the LV NMOS is shown in Figure 6, and the TB for the LV PMOS is shown in Figure 7.

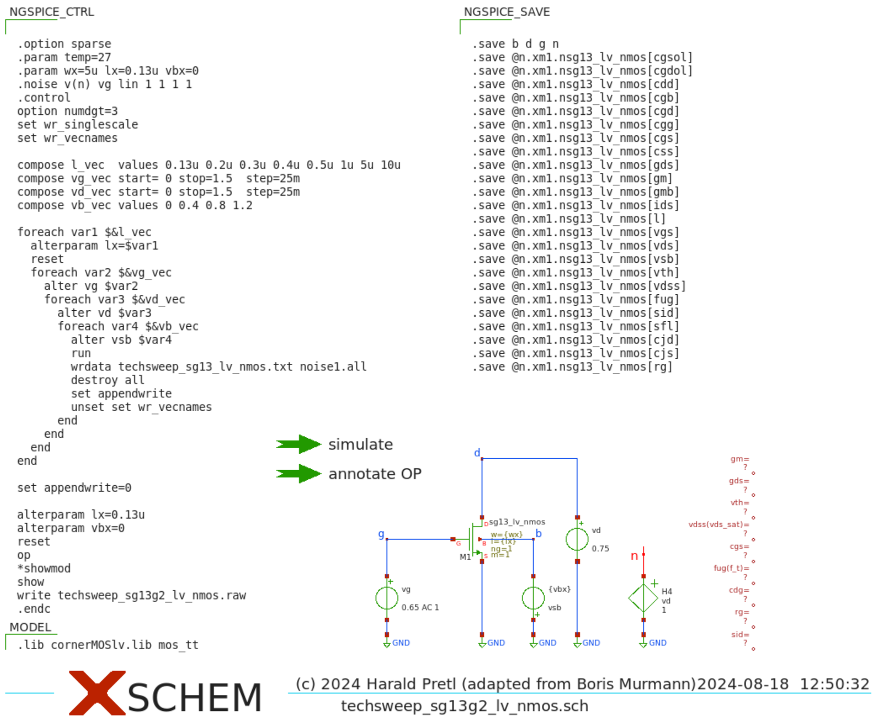


Figure 6: Testbench for LV NMOS $g_{\mathrm{m}}/I_{\mathrm{D}}$ characterization.

We will use Jupyter notebooks to inspect the resulting data, and interpret some important graphs. This will greatly help to understand the MOSFET behaviour.

NMOS Characterization

First, we will start looking at the LV NMOS. In Section we have the corresponding graphs for the LV PMOS. In this lecture, we will only use the LV MOSFETs. While there are also the HV types available, they are mainly used for high-voltage circuits, like circuits connecting to the outside world. Here, we only will design low-voltage circuits running at a nominal supply voltage of 1.5 V, so only the LV types are of interest to us.

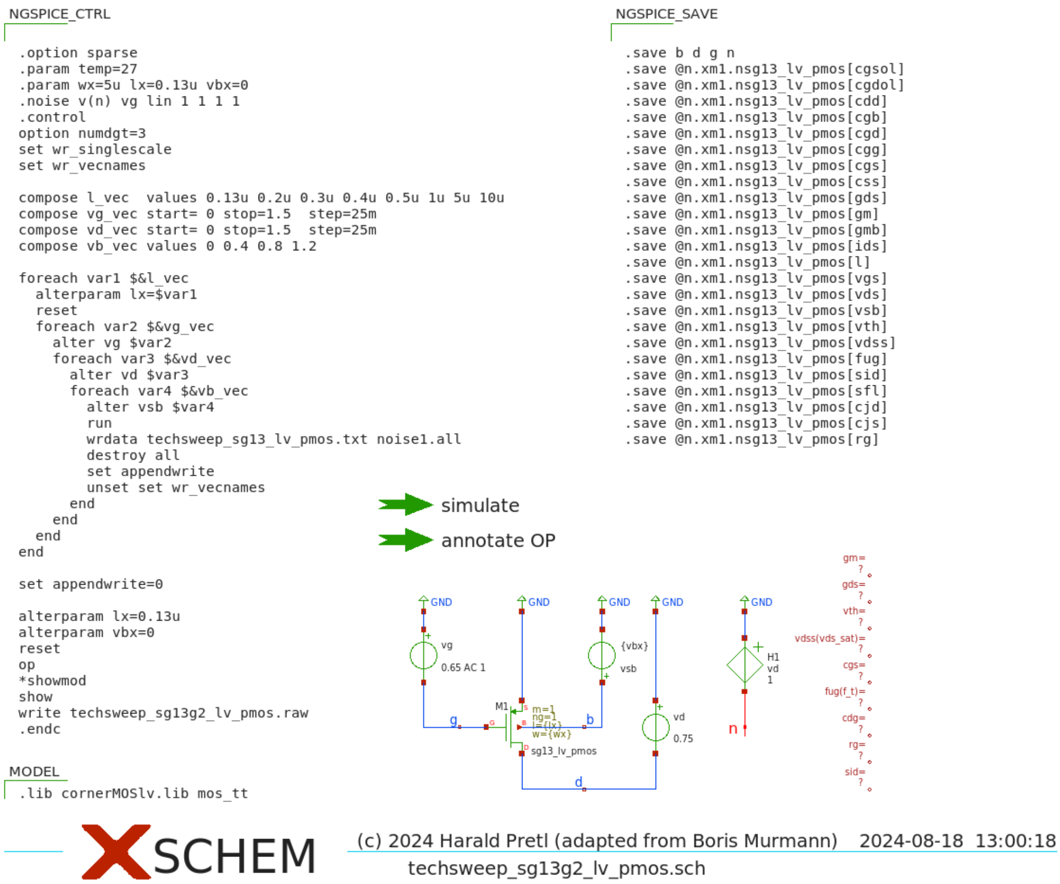


Figure 7: Testbench for LV PMOS $g_\mathrm{m}/I_\mathrm{D}$ characterization.

The first import graph is the plot of $g_\mathrm{m}/I_\mathrm{D}$ and f_T versus the gate-source voltage V_GS. First let us answer the question why $g_\mathrm{m}/I_\mathrm{D}$ is a good parameter to look at, and actually this is also the central parameter in the $g_\mathrm{m}/I_\mathrm{D}$ methodology. In many circuits that are biased in class-A (i.e., with a constant quiescent current that is larger than the largest signal excursion, see biasing) we want to get a large amplification from a MOSFET, which corresponds to a large g_m. We want this by spending the minimum biasing current possible (ideally zero), as we always design for minimum power consumption. Thus, a high $g_\mathrm{m}/I_\mathrm{D}$ ratio is good.

> **Note**
>
> Designing for minimum power consumption is pretty much always mandated. For battery-operated equipment it is a paramount requirement, but also in other equipment electrical energy consumption is a concern, and often severly limited by the cooling capabilities of the electrical system.

However, as can be seen in the below plot, there exists a strong and unfortunate trade-off with device speed, characterized here by the transit frequency f_T. It would be ideal if there exists a design point where we get high transconductance per bias current concurrently to having the fastest operation, but unfortunately, this is clearly not the case. The $g_\mathrm{m}/I_\mathrm{D}$ peaks for $V_\mathrm{GS} < 0.3\,\mathrm{V}$, and the highest speed we get at $V_\mathrm{GS} \approx 1.2\,\mathrm{V}$. The dashed vertical line plots the nominal threshold voltage, as you can see in this continuum of parameter space, it marks not a particularly special point.

Note that

$$\frac{g_\mathrm{m}}{I_\mathrm{D}} = \frac{1}{n V_\mathrm{T}} \tag{1}$$

for a MOSFET in weak inversion (i.e., small gate-source voltage). n is the subthreshold slope, and $V_\mathrm{T} = kT/q$ which is $25.8\,\mathrm{mV}$ at $300\,\mathrm{K}$. We thus have $n \approx 1.38$ for this LV NMOS, which falls nicely into the usual range for n of 1.3 to 1.5 for bulk CMOS (FinFET have n very close to 1).

For the classical square-law model of the MOSFET in strong inversion, $g_\mathrm{m}/I_\mathrm{D}$ is given as

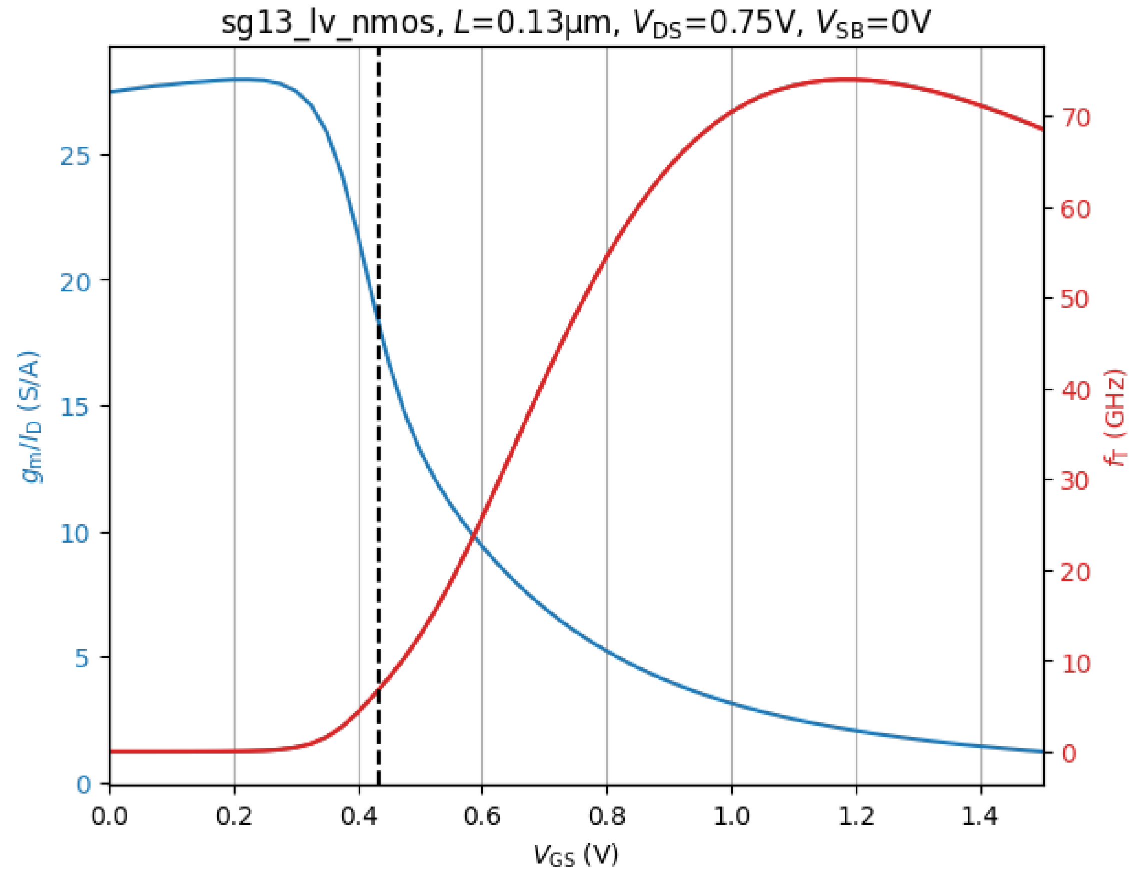
$$\frac{g_\mathrm{m}}{I_\mathrm{D}} = \frac{2}{V_\mathrm{GS} - V_\mathrm{th}} = \frac{2}{V_\mathrm{od}} \tag{2}$$

with V_th the threshold voltage and V_od the so-called “overdrive voltage.”

> **Note**
>
> Why are we so often using $300\,\mathrm{K}$ for a typical condition? As this corresponds to roughly 27°C, this accounts for some self heating compared to otherwise usual room temperatures. Further, engineers like round numbers which are easy to remember, so $300\,\mathrm{K}$ is used as a proxy for room temperature.

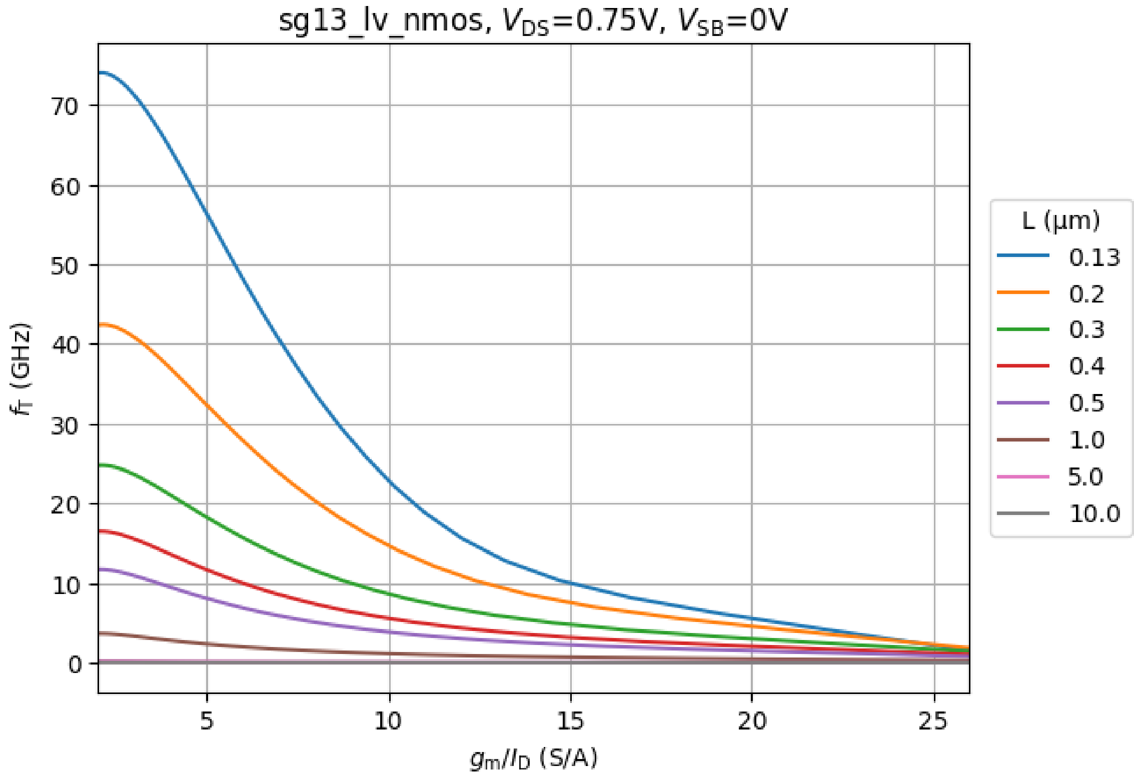
As we can also see from belows plot, the peak transit frequency of the LV NMOS is about $75\,\mathrm{GHz}$, which allows building radio-frequency circuits up to ca. $f_\mathrm{T}/10 = 7.5\,\mathrm{GHz}$, which is a respectible number. It is no coincidence, that the transition for RF design in the

GHz-range switched from BJT-based technologies to CMOS roughly in the timeframe when 130nm CMOS became available (ca. 2000).



Source: Article Notebook

The following figure plots f_T against g_m/I_D for several different L. As you can see, device speeds maximizes for a low g_m/I_D and a short L. As you can see the drain-source voltage is kept at $V_{DS} = 0.75\,\text{V} = V_{DD}/2$, which is a typical value keeping the MOSFET in saturation across the characterization sweeps. Further, the source-bulk voltage is kept at $V_{SB} = 0\,\text{V}$, which means bulk and source terminals are connected.



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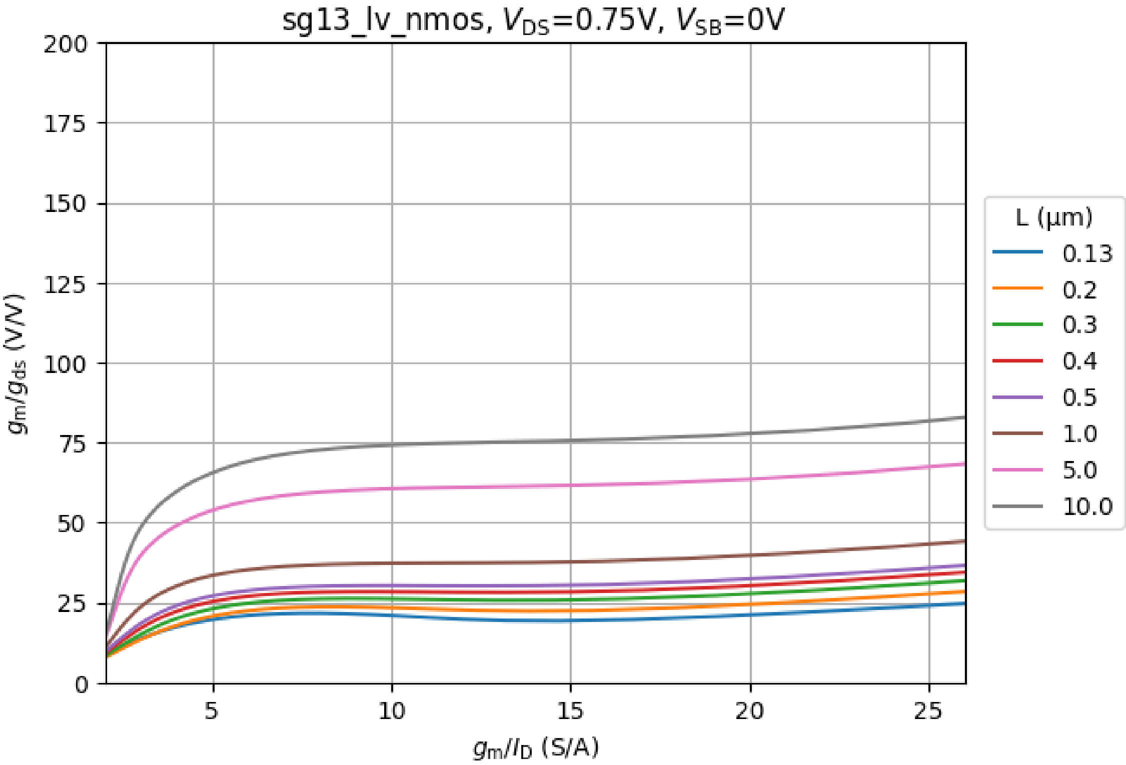
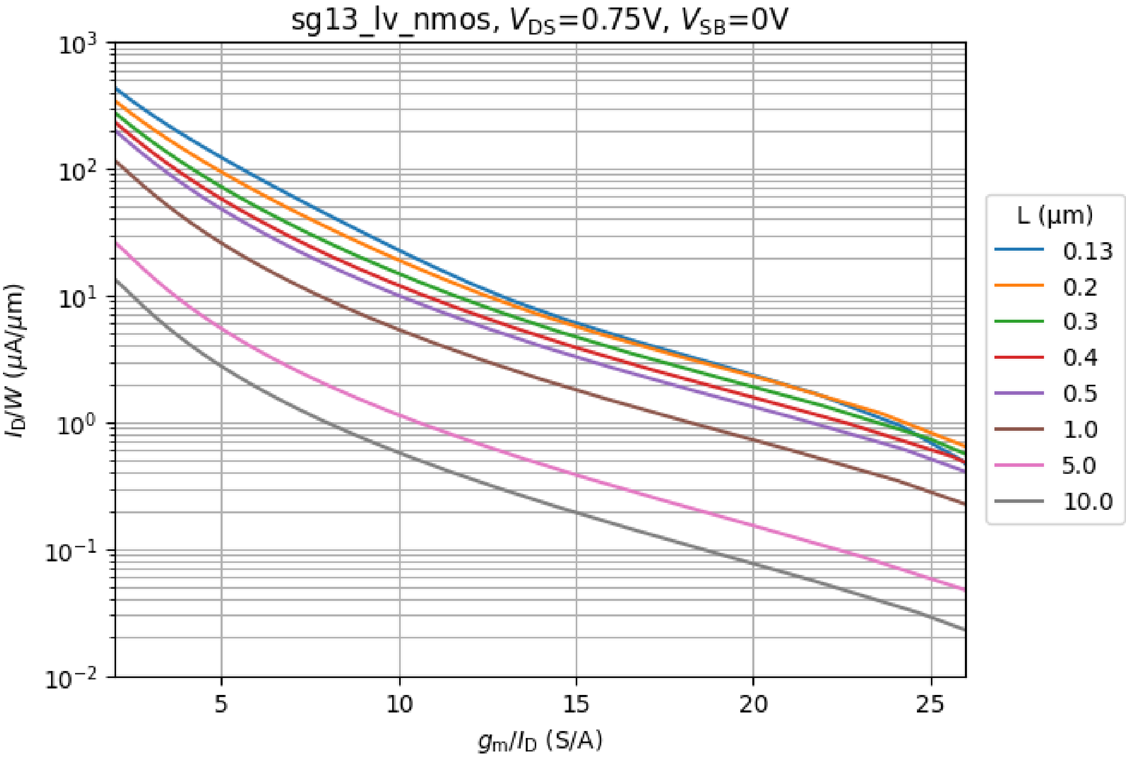
The next plot shows the ratio of $g_\mathrm{m}/g_\mathrm{ds}$ versus $g_\mathrm{m}/I_\mathrm{D}$. The ratio $g_\mathrm{m}/g_\mathrm{ds}$ is the so-called "self-gain" of the MOSFET, and shows the maximum voltage gain we can achieve in a single transistor configuration. As one can see the self gain increases for increasing L, but this also gives a slower transistor, so again there is a trade-off. This plot allows us to select the proper L of a MOSFET if we know which amount of self gain we need.



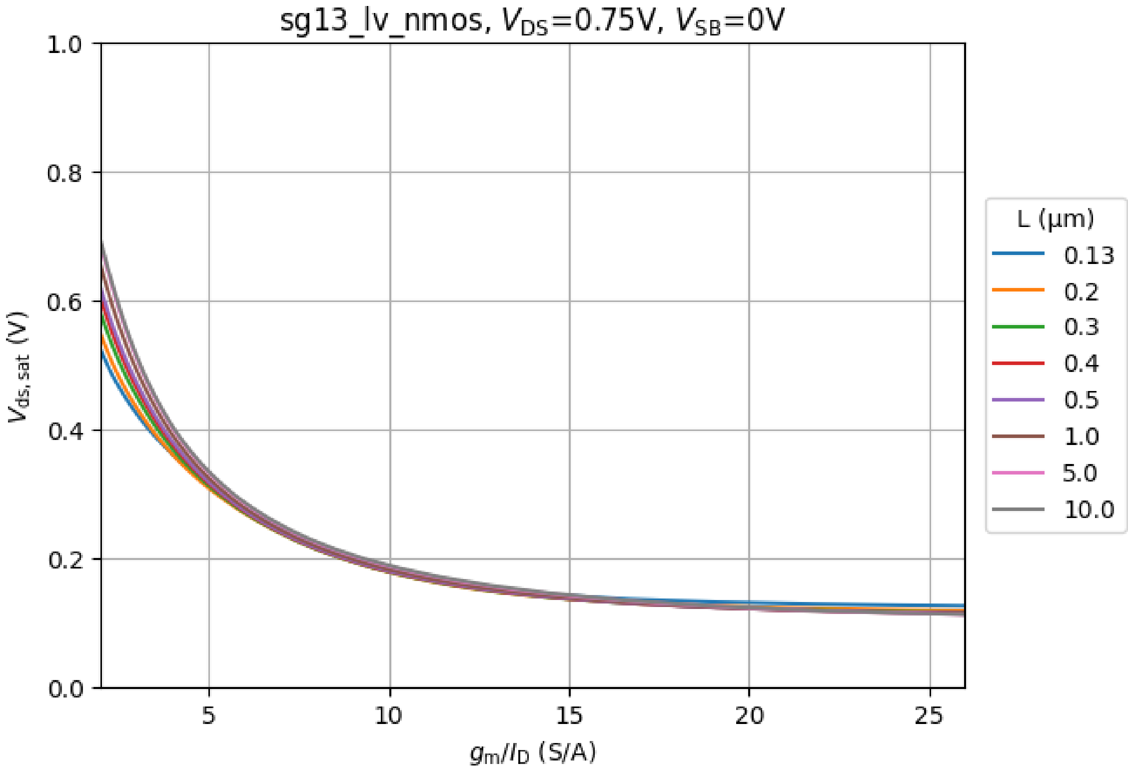
Source: Article Notebook

The following figure plots the drain current density I_D/W as a function of g_m/g_{ds} and L. With this plot we can find out how to set the W of a MOSFET once we know the biasing current I_D, the L (selected according to self gain, f_T, and other considerations) and the g_m/I_D design point we selected. The drain current density I_D/W is a very useful nomalized metric to use, because the physical action in the MOSFET establishes a charge density in the channel below the gate, and the changing of the W of the device merely transforms this charge density into an absolute parameter (together with L).



Source: Article Notebook

The following plot shows the minimum drain-source voltage $V_{\mathrm{ds,sat}}$ that we need to establish in order to keep the MOSFET in saturation. As you can see, this value is almost independent of L, and increases for small $g_{\mathrm{m}}/I_{\mathrm{D}}$. So for low-voltage circuits, where headroom is precious, we tend to bias at $g_{\mathrm{m}}/I_{\mathrm{D}} \geq 10$, wheres for fast circuits we need to go to small $g_{\mathrm{m}}/I_{\mathrm{D}} \leq 5$ requiring substantial voltage headroom per MOSFET stage that we stack on top of each other.



Source: Article Notebook

For analog circuits the noise performance is usually quite important. Thermal noise of a resistor (the Johnson-Nyquist noise) has a flat power-spectral density (PSD) given by $\overline{V_n^2}/\Delta f = 4kTR$, where k is Boltzmann's constant, T absolute temperature, and R the value of the resistor (the unit of $\overline{V_n^2}/df$ is V^2/Hz). This PSD is essentially flat until very high frequencies where quantum effects start to kick in.

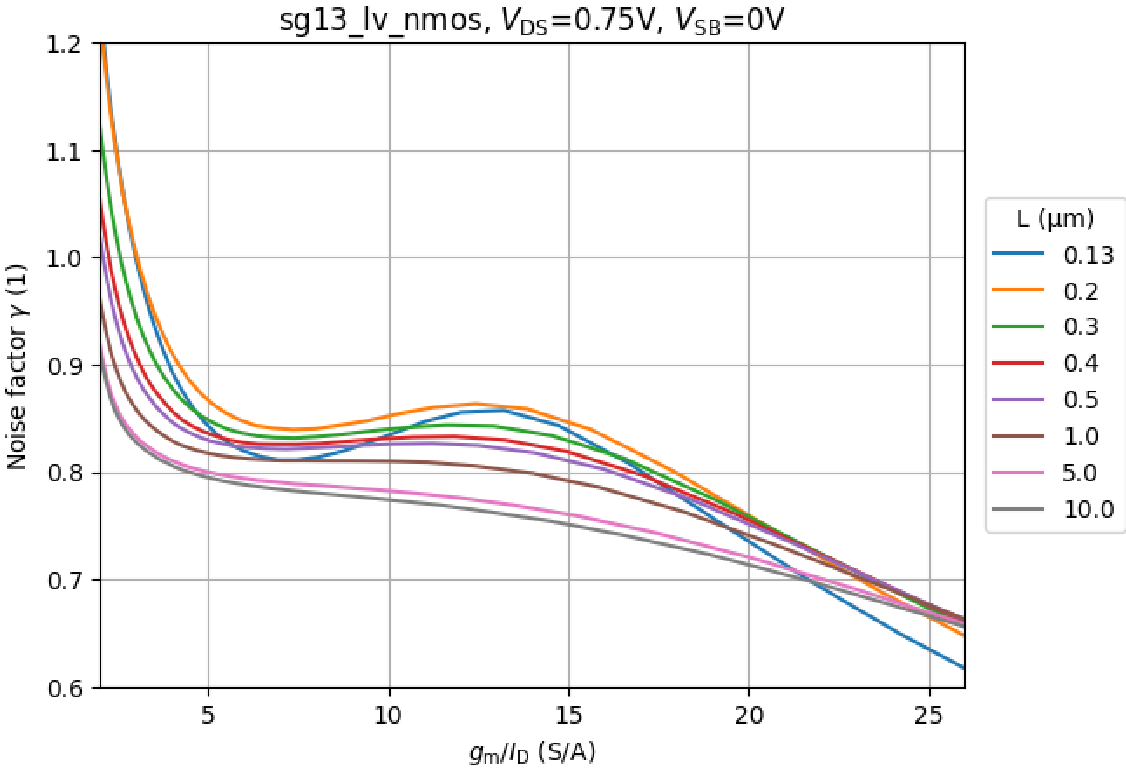
> **Note**
>
> We usually leave the Δf away for a shorter notation, so we write $\overline{V_n^2}$ when we actually mean $\overline{V_n^2}/\Delta f$.
> Please also note that the pair of kT pretty much always shows up together, so when you do a calculation and you miss the one or the other, that is often a sign for miscalculation.
> Fuerther, when working with PSD there is the usage of a one-sided (f runs from 0 to ∞) or two-sided PSD (f runs from $-\infty$ to ∞). The default in this lecture is the usage of a **one-sided PSD**.

In this lecture the only MOSFET noise we consider is the drain noise, showing up as a current noise between drain and source, and given by

$$\overline{I_{d,n}^2} = 4kT\gamma g_{d0} \tag{3}$$

In saturation (the MOSFET operating as a current source), $g_{\mathrm{d0}} = g_{\mathrm{m}}$, whereas in triode (the MOSFET operating as a switch), $g_{\mathrm{d0}} = g_{\mathrm{ds}}$.

The factor γ is a function of many things (in classical theory, $\gamma = 2/3$ in saturation and $\gamma = 1$ in triode), and it is characterized in the following plot as a function of $g_{\mathrm{m}}/I_{\mathrm{D}}$ and L. So when calculating MOSFET noise we can lookup γ in the below plot, and use Equation 3 to calculate the effective drain current noise.

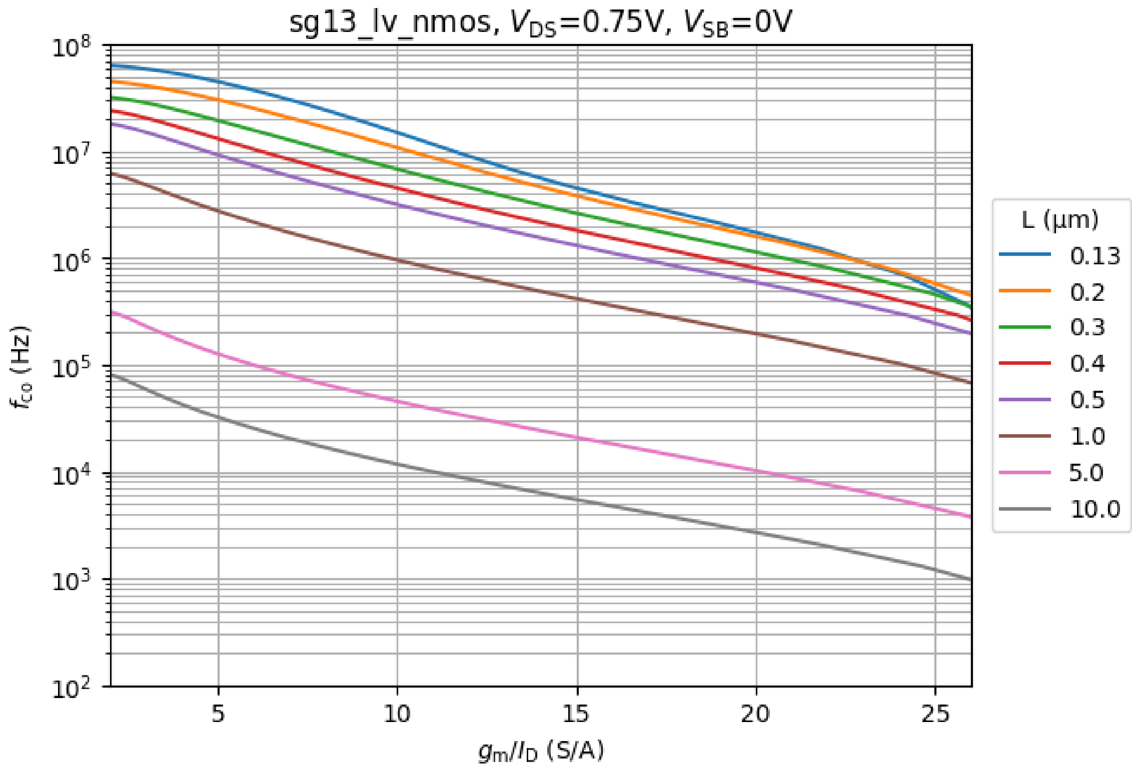


Source: Article Notebook

In a MOSFET, unfortunately, besides the thermal noise according to Equation 3, there is also a substantial low-frequency excess noise, called "flicker noise" due to its characteristic $\overline{I_{\mathrm{d,nf}}^2} = K_{\mathrm{f}}/f$ behaviour (this means that this noise PSD decreases versus frequency). In order to characterize this flicker noise the following plot shows the cross-over frequency f_{co}, where the flicker noise is as large as the thermal noise. As can be seen in the below plot, this frequency is a strong function of L and $g_{\mathrm{m}}/I_{\mathrm{D}}$. Generally, the flicker noise is proportional to $(WL)^{-1}$, so the larger the device is, the lower the flicker noise. The parameter $g_{\mathrm{m}}/I_{\mathrm{D}}$ largely stays constant when we keep W/L constant, so for a given $g_{\mathrm{m}}/I_{\mathrm{D}}$ flicker noise is proportional to $1/L^2$. However, increasing L lowers device speed dramatically, so here we have a trade-off between flicker-noise performance and MOSFET speed, and this can have dramatic consequences for high-speed circuits.

> **Note**
>
> The physical origin of flicker noise is the crystal interface between silicon (Si) and the silicondioxide (SiO_2). Since these are different materials, there are dangling bonds, which can capture charge charriers travelling in the channel. After a random time, these carriers are released, and flicker noise is the result. The amount of flicker noise is a function of the manufacturing process, and will generally be different between device types and wafer foundries.

As you can see in the following plot, f_{co} can reach well into the 10's of MHz for short MOSFETs, significantly degrading the noise performance of a circuit.



Source: Article Notebook

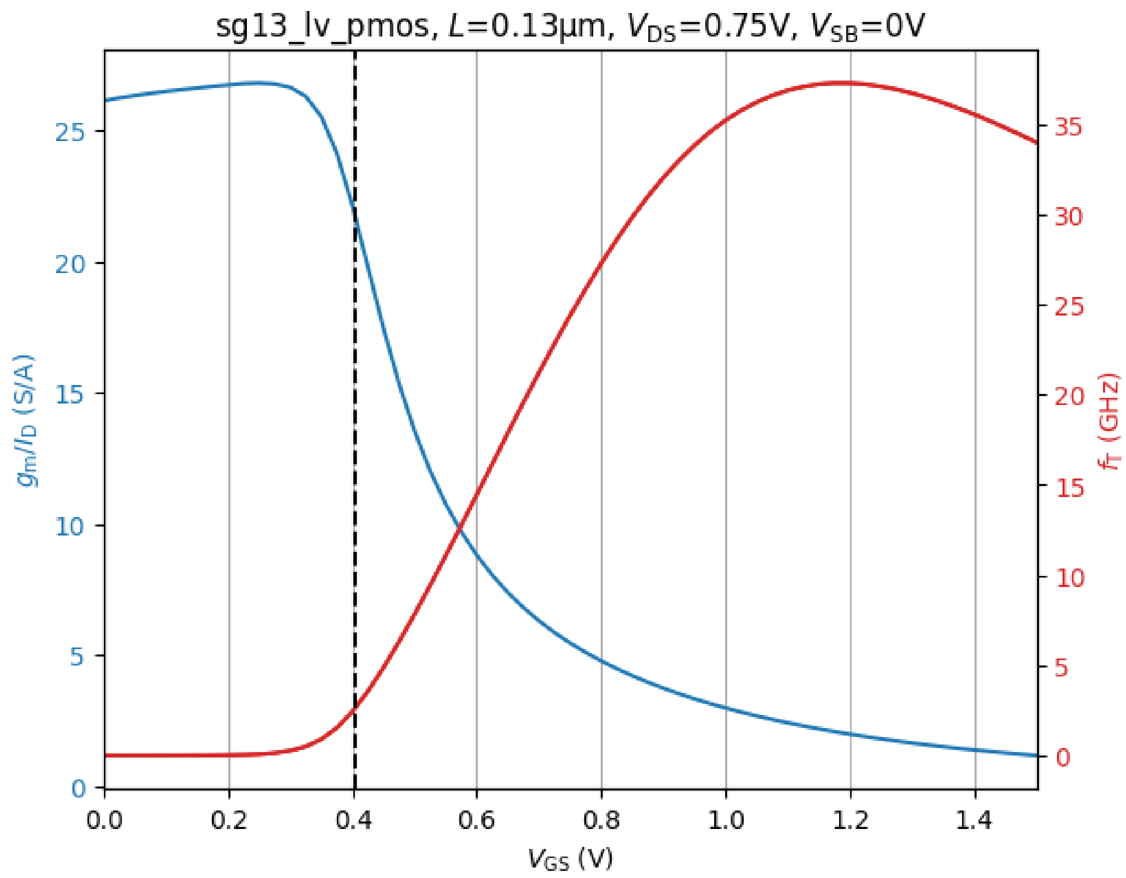
PMOS Characterization

In the following, we have the same plots as discussed in Section , but now for the PMOS.

> **Note**
>
> In all PMOS plots we plot positive values for voltages and currents, to have compatible plots to the NMOS. Of course, in a PMOS, voltages and currents have different polarity

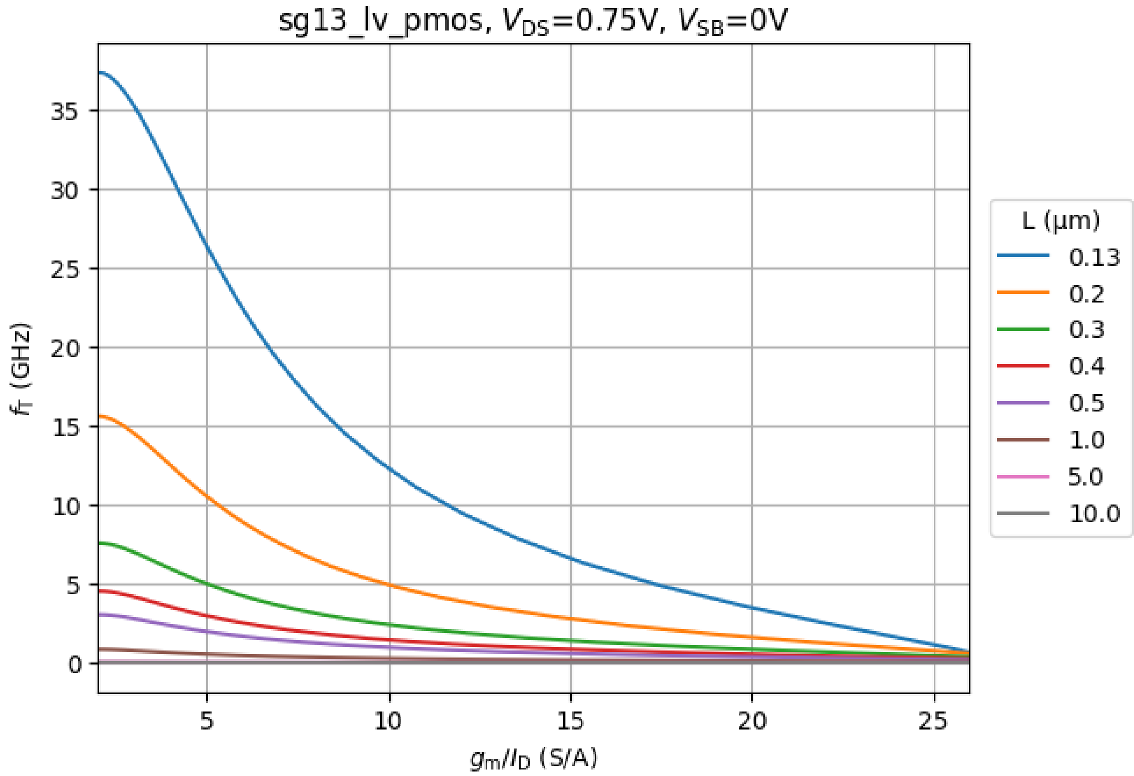
compared to the PMOS.

$g_{\mathrm{m}}/I_{\mathrm{D}}$ and f_{T} versus the gate-source voltage V_{GS}:



Source: Article Notebook

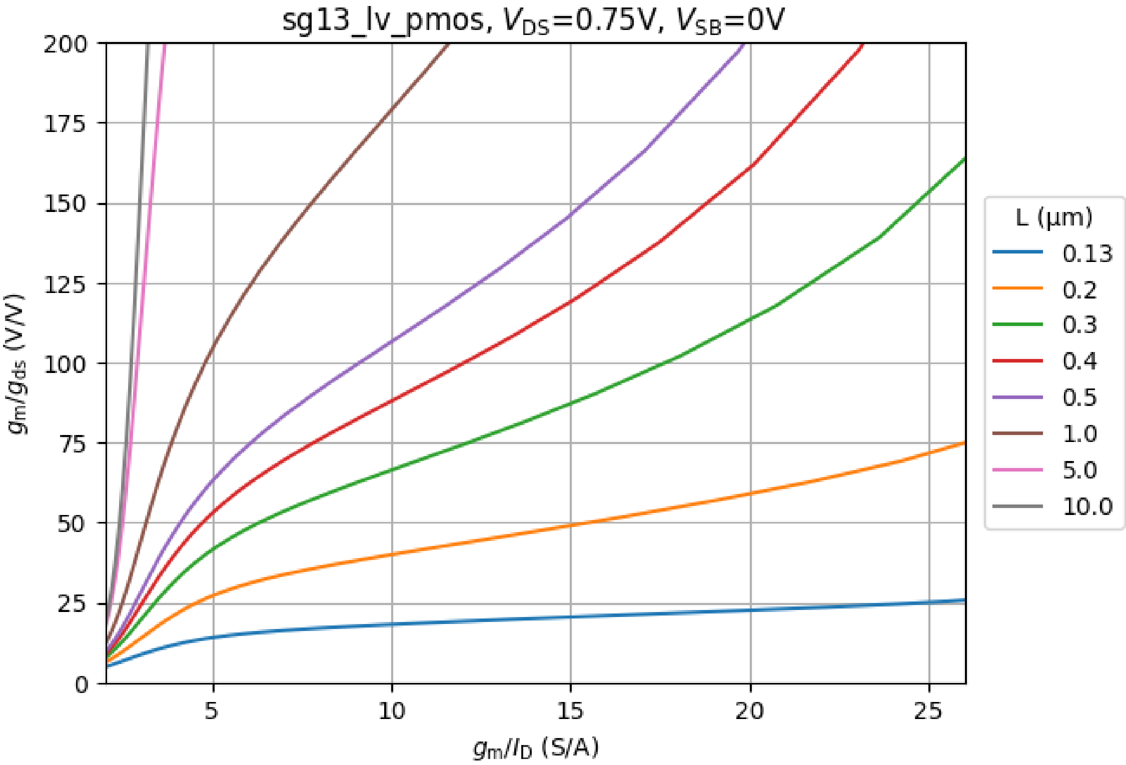
f_{T} against $g_{\mathrm{m}}/I_{\mathrm{D}}$ for several different L. One can see significantly lower top speed for the PMOS compared to the NMOS, which means for high-speed circuits the NMOS should be used.



Source: Article Notebook

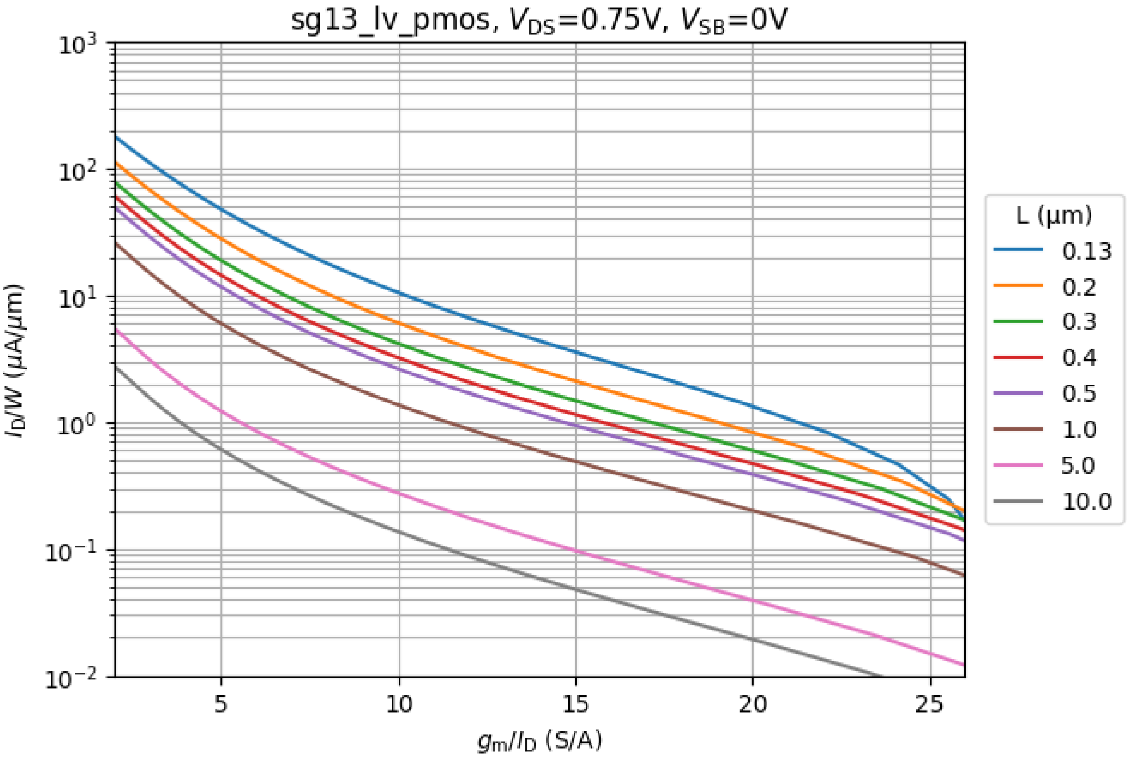
g_m/g_{ds} versus g_m/I_D. Unfortunately, one can see a modelling error for the PMOS in this plot. The self gain g_m/g_{ds} reaches non-physical values, which indicates an issue with the g_{ds} modelling for the PMOS. We can not use these values for our circuit sizing, so we will use the respective NMOS plots also for the PMOS.

> **! Important**
>
> This example shows how important it is to benchmark the device models when starting to use a new technology. Modelling artifacts like the one shown are quite often happening, as setting up the device compact models and parametrizing them according to measurement data is a very complex task. In any case, just be aware that modelling issues could exist in whatever PDK you are using!



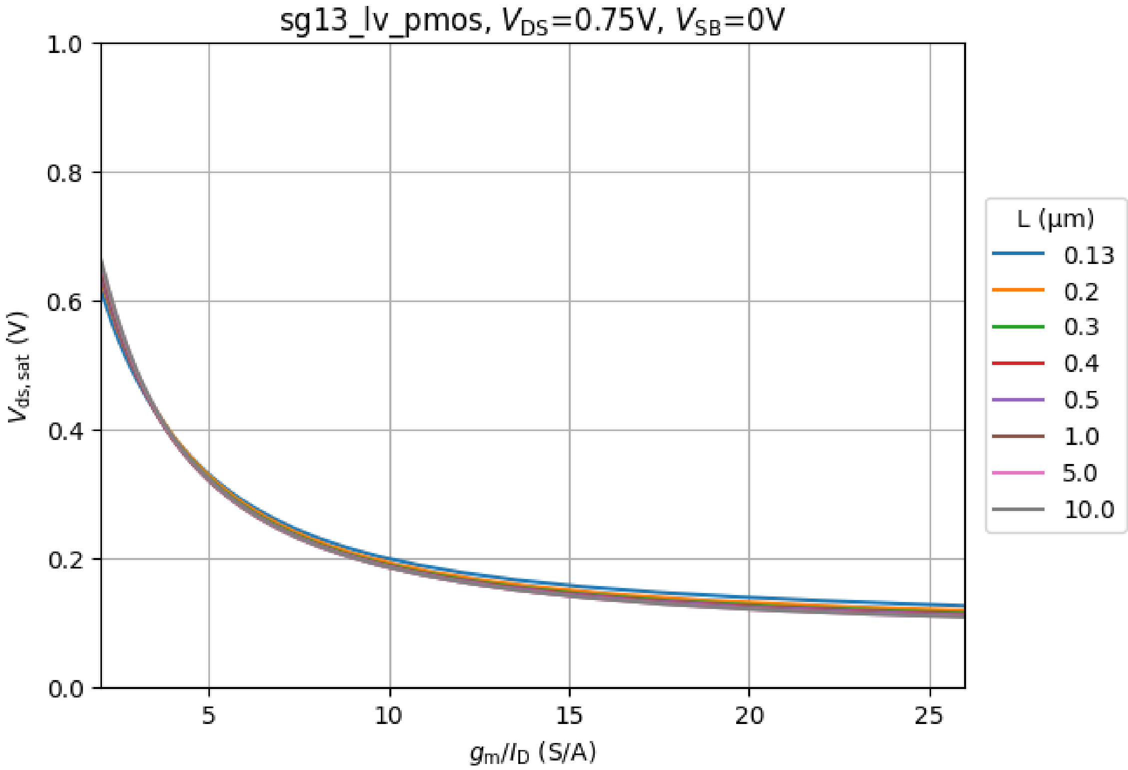
Source: Article Notebook

Drain current density I_D/W as a function of g_m/g_{ds} and L:



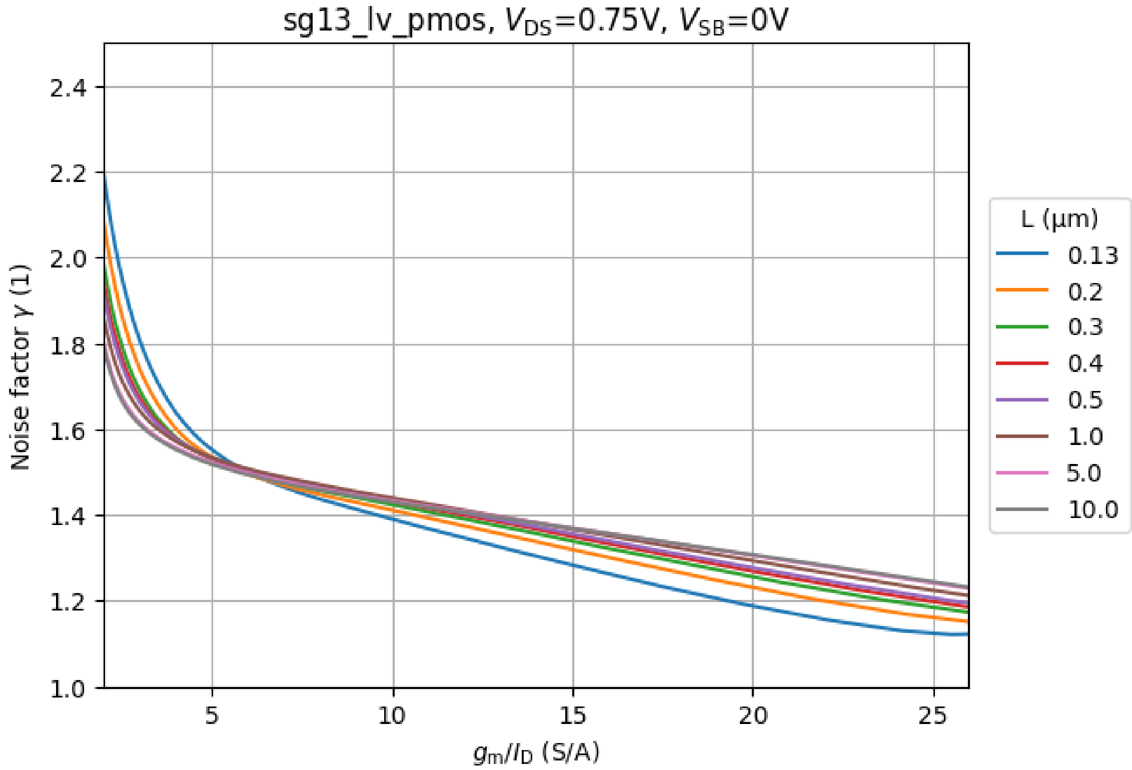
Source: Article Notebook

Minimum drain-source voltage $V_{\mathrm{ds,sat}}$ versus $g_{\mathrm{m}}/I_{\mathrm{D}}$ and L:



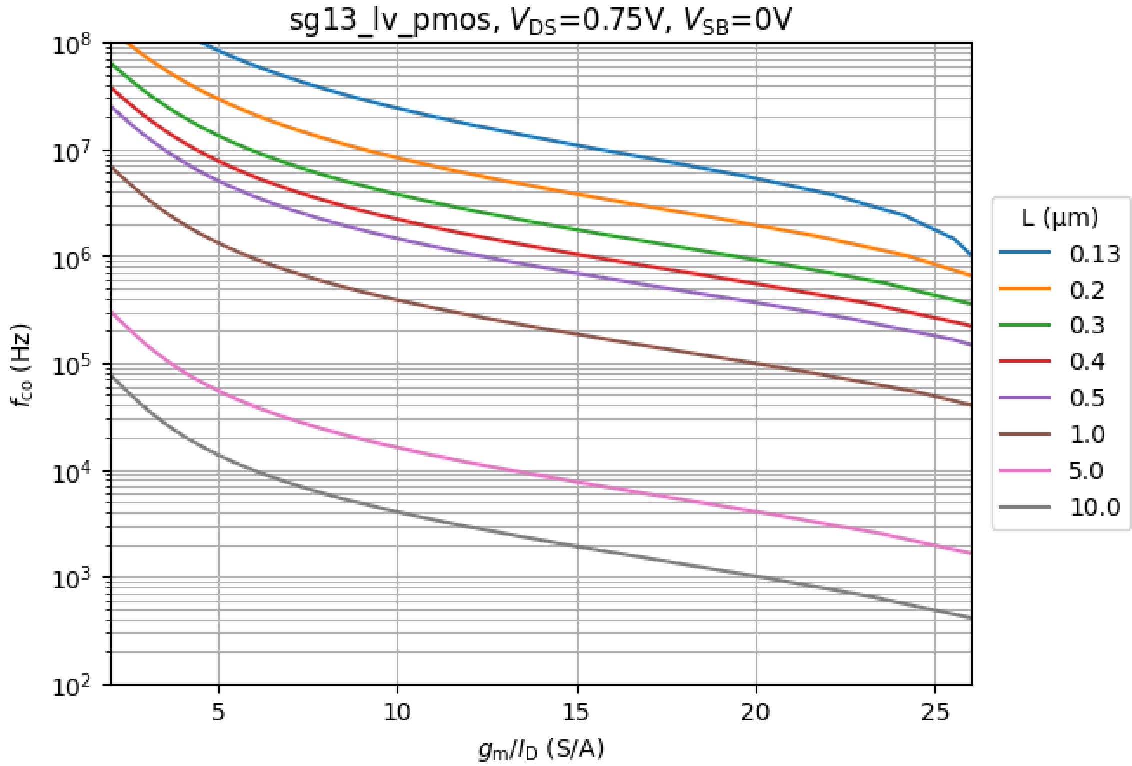
Source: Article Notebook

Noise factor γ versus $g_\mathrm{m}/I_\mathrm{D}$ and L:



Source: Article Notebook

Flicker noise corner frequency f_{co} versus g_m/I_D and L. If you compare this figure carefully with the NMOS figure you can see that for some operating points the flicker noise for the PMOS is lower than for the NMOS. This is often true for CMOS technologies, so it can be an advantage to use a PMOS transistor in places where flicker noise is critical, like an OTA input stage. Using PMOS has the further advantage that the bulk node can be tied to source (which for NMOS is only possible in a triple-well technology, which is often not available), which gets rid of the body effect.



Source: [Article Notebook]()

First Circuit: MOSFET Diode

This sections need to be written, but here is a first figure.

Source: [Article Notebook]()

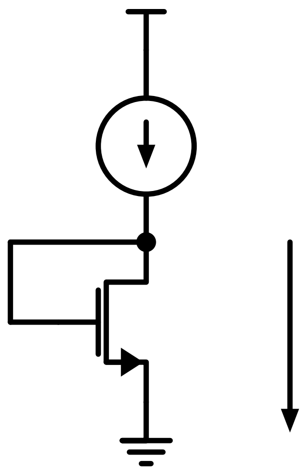


Figure 8: A MOSFET connected as a diode.

Source: Article Notebook

Current Mirror

Differential Pair

Cascode Stage

A Basic 5-Transistor OTA

A Fully-Differential OTA

Biasing the OTA

An RC-OPAMP Filter

Summary & Conclusion

Appendix: ngspice Cheat Sheet

Appendix: Xschem Cheat Sheet

Source: Article Notebook

Hu, Chenming. 2010. *Modern Semiconductor Devices for Integrated Circuits*. Pearson.

Jespers, Paul G. A., and Boris Murmann. 2017. *Systematic Design of Analog CMOS Circuits: Using Pre-Computed Lookup Tables*. Cambridge University Press.

Nagel, Laurence W. 1975. "SPICE2: A Computer Program to Simulate Semiconductor Circuits." PhD thesis, EECS Department, University of California, Berkeley. http://www2.eecs.berkeley.edu/Pubs/TechRpts/1975/9602.html.

Tsividis, Yannis, and Colin McAndrew. 2011. *Operation and Modeling of the MOS Transistor*. Oxford University Press.