

KLayout-PEX Documentation

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2025-02-06

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1 Introduction

1.1 Motivation

In Electronic Design and Automation (EDA) for Integrated Circuits (ICs), a schematic presents an abstraction in comparison to the layout that will eventually be taped-out and fabricated by the semiconductor foundry.

While in the schematic, a connection between device terminals is seen as an equipotential, the stacked geometries in a specific layout introduce parasitic effects, which can be thought of additional resistors, capacitors (and inductors), not modeled by and missing in the original schematic.

To be able to simulate these effects, a parasitic extraction tool (PEX) is used, to extract a netlist from the layout, which represents the original schematic (created from the layout active and passive elements) augmented with the additional parasitic devices.

1.2 Acknowledgements

Special thanks to the public funded German project FMD-QNC (16ME0831) <https://www.elektronikforschung.de/projekte/fmd-qnc> for financial support to this work.

1.3 About KLayout-PEX

[KLayout](#) is an open source VLSI layout viewer and editor.

[KLayout-PEX](#) (short KPEX) is a PEX tool, well integrated with [KLayout](#) by using its API.

There are multiple PEX engines supported, currently:

- [FasterCap](#) integration (field solver engine)
- [MAGIC](#) integration (wrapper calling `magic`)
- Analytical 2.5D engine (parasitic concepts and formulas of MAGIC, implemented using [KLayout](#) methods)

💡 Tip

KPEX *tool* source code itself is made publicly available on GitHub ([follow this link](#)) and shared under the GPL-3.0 license.

KPEX *documentation* source code is made publicly available on GitHub ([follow this link](#)) and shared under the Apache-2.0 license.

Please feel free to create issues and/or submit pull requests on GitHub to fix errors and omissions!

The production of the tool and this document would be impossible without these (and many more) great open-source software products: [KLayout](#), [FasterCap](#), [MAGIC](#), [protobuf](#), [Quarto](#), [Python](#), [ngspice](#), [Numpy](#), [Scipy](#), [Matplotlib](#), [Git](#), [Docker](#), [Ubuntu](#), [Linux](#)...

🔥 Caution

Currently, KPEX is developed as a Python prototype, using the [KLayout Python API](#). This allows for a faster development cycle during the current prototyping phase.

Eventually, critical parts will be re-implemented (in C++, and parallelized), to improve performance. As we're already using the KLayout API (which is pretty similar between Python, Ruby and C++), this will be relatively straight-forward.

1.4 Installation

Generally, KPEX is deployed using PyPi (Python Package Index), install via:

```
pip3 install --upgrade klayout-pex

kpex --version    # check the installed version
kpex --help       # this will help with command line arguments
```

As for the dependencies, there are multiple options available.

1.4.1 Option 1: Using IIC-OSIC-TOOLS Docker Image

We provide a comprehensive, low entry barrier Docker image that comes pre-installed with most relevant open source ASIC tools, as well as the open PDKs. This is a pre-compiled Docker image which allows to do circuit design on a virtual machine on virtually any type of computing equipment (personal PC, Raspberry Pi, cloud server) on various operating systems (Windows, macOS, Linux).

For further information please look at the [Docker Hub page](#) and for detailed instructions at the [IIC-OSIC-TOOLS GitHub page](#).



Linux

In this document, we assume that users have a basic knowledge of Linux and how to operate it using the terminal (shell). If you are not yet familiar with Linux (which is basically a must when doing integrated circuit design as many tools are only available on Linux), then please check out a Linux introductory course or tutorial online, there are many resources available.

A summary of important Linux shell commands is provided in [IIC-JKU Linux Cheatsheet](#).

1.4.2 Option 2: Standalone Installation

- [KLayout](#) layout tool:
 - is mandatory for all engines (besides the MAGIC-wrapper)
 - [get the latest pre-built package version](#)
 - or [follow the build instructions](#)
- [FasterCap](#) engine:
 - optional, required to run the FasterCap engine
 - either compile your own version from the [GitHub repository](#)
 - or use precompiled versions available at <https://github.com/martinjankoheler/FasterCap/releases>
- [MAGIC](#)-wrapper engine:
 - optional, required to run the MAGIC-wrapper engine
 - Follow the [installation instructions](#) at the [GitHub repository](#)
- [Skywater sky130A](#) PDK:
 - optional, for now, KPEX technology specific files are deployed within the `klayout-pex` Python package
 - `pip3 install --upgrade volare` (install PDK package manager)
 - `volare ls-remote` (retrieve available PDK releases)

- * for example PRE-RELEASE 0c1df35fd535299ea1ef74d1e9e15dedaeb34c32 (2024.12.11))
- `volare enable 0c1df35fd535299ea1ef74d1e9e15dedaeb34c32` (install a PDK version)
- PDK files now have been installed under `$HOME/.volare/sky130A`

- IHP SG13G2 PDK:

- optional, for now, KPEX technology specific files are deployed within the `klayout-pex` Python package
- `git clone https://github.com/IHP-GmbH/IHP-Open-PDK` (install PDK package manager)

1.4.3 Useful tools: `meshlab`

For previewing generated 3D geometries, representing the input to `FasterCap`, we recommend installing [MeshLab](#). The generated STL-files are located at `output/<design>/Geometries/*.stl`.

2 First Steps

- The command line tool `kplex` is used to trigger the parasitic extraction flow from the terminal.
- Get help calling `kplex --help`.

2.1 Example Layouts

Example layouts are included in the `testdata/designs` subdirectory of the KLayout-PEX source code:

```
git clone https://github.com/martinjankohler/klayout-pex.git

# for sky130A
find testdata/designs/sky130A -name "*.gds.gz"

# for IHP SG13G2
find testdata/designs/ihp_sg13g2 -name "*.gds.gz"
```

2.2 Running the KPLEX/FasterCap engine

Preconditions:

- `klayout-pex` was installed, see Section 1.4
- `FasterCap` was installed, see Section 1.4

i Note

Normally, devices with SPICE (Nagel 1975) simulation models (e.g. like MOM-capacitors¹ in the sky130A PDK) are ignored (“blackboxed”) during parasitic extraction.

`kplex` has an option `--blacklist n` to allow extraction of those devices (whiteboxing), which can be useful during development (during the prototype phase, whiteboxing is actually the default setting, so please use `--blacklist y` to explicitly configure blackboxing).

Let's try the following:

```
kplex --pdk sky130A --blackbox n --gds \
testdata/designs/sky130A/*/cap_vpp_04p4x04p6_l1m1m2_noshield.gds.gz
```

i Note

This will report an error that we have not activated one or more engines, and list the available engines:

Argument	Description
<code>--fastercap</code>	Run <code>kplex/FasterCap</code> engine
<code>--2.5D</code>	Run <code>kplex/2.5D</code> engine
<code>--magic</code>	Run <code>MAGIC</code> engine

Now, to run the FasterCap engine (might take a couple of minutes):

¹Metal-Oxide-Metal capacitors

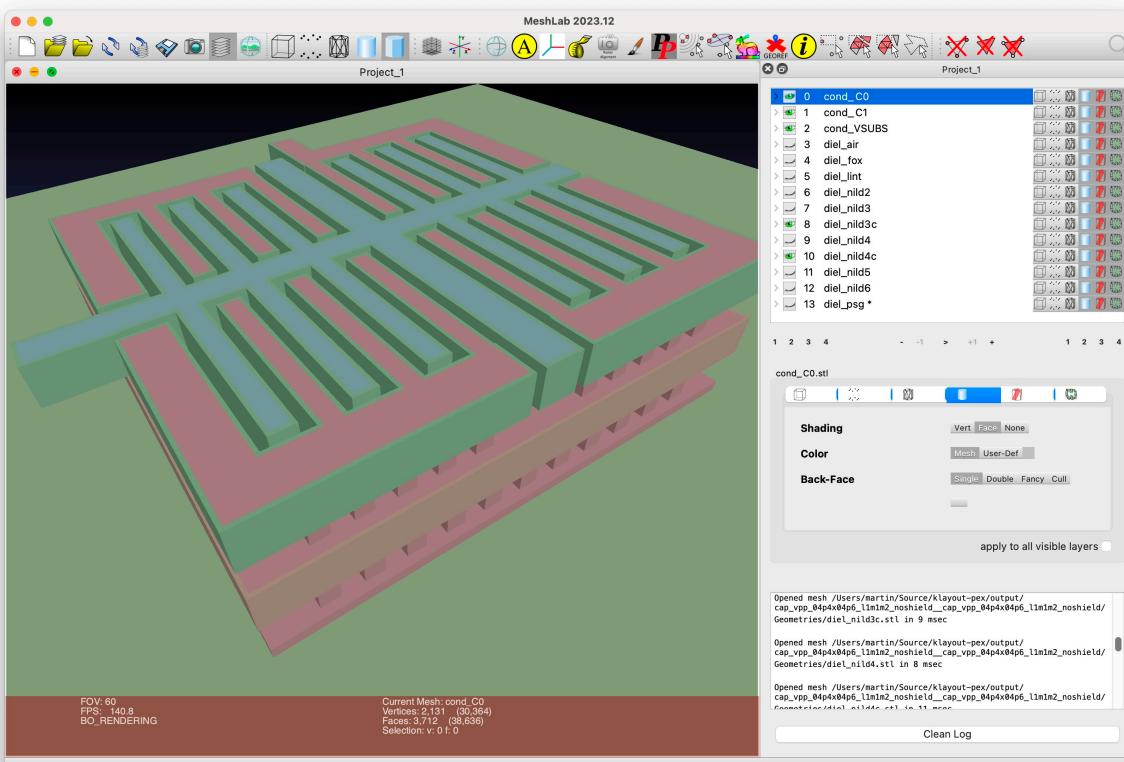
```
kpxe --pdk sky130A --blackbox n --fastercap --gds \
testdata/designs/sky130A/*/cap_vpp_04p4x04p6_11m1m2_noshield.gds.gz
```

Within the output directory (defaults to `output`), KPEX creates a subdirectory `Geometries`, containing STL-files that provide a preview of the FasterCap input geometries. Use MeshLab (see Section 1.4.3) to open and preview those files:

```
ls -d output/cap_vpp_04*/Geometries/*.stl
```

💡 Tip

- Open the `*.stl` files in MeshLab
- Use the eye buttons to hide and show each file/mesh
- Use the align tool (“A” in the toolbar) to assign different colors
- Start by showing only on the conductors (files named `cond_* .stl`)
- Then try showing different dielectrics (files named `diel_* .stl`), to see how they surround the conductors.



In the log file, we see the output of FasterCap including the Maxwell capacitance matrix:

Capacitance matrix is:

```
Dimension 3 x 3
g1_VSUBS  5.2959e-09 -4.46971e-10 -1.67304e-09
g2_C1    -5.56106e-10  1.5383e-08 -1.47213e-08
g3_C0    -1.69838e-09 -1.48846e-08  1.64502e-08
```

KPEX interprets this matrix and prints a CSV netlist, which can be pasted into a spreadsheet application:

```
Device;Net1;Net2;Capacitance [fF]
Cext_0_1;VSUBS;C1;0.5
Cext_0_2;VSUBS;C0;1.69
Cext_1_2;C1;C0;14.8
Cext_1_1;C1;VSUBS;0.08
```

In addition, a SPICE netlist is generated.

2.3 Running the KPEX/MAGIC engine

Preconditions:

- `klayout-pex` was installed, see Section 1.4
- `magic` was installed, see Section 1.4

The magic section of `kpx --help` describes the arguments and their defaults. Important arguments:

- `--magicrc`: specify location of the `magicrc` file
- `--gds`: path to the GDS input layout
- `--magic`: enable magic engine

```
kpx --pdk sky130A --magic --gds \
testdata/designs/sky130A/*cap_vpp_04p4x04p6_l1m1m2_noshield.gds.gz
```

3 Supporting new PDKs

For every supported PDK, a KPEX technology definition is required, as well as customized PEX-“LVS” scripts.

3.1 Technology Definition Files

The KPEX technology definition format uses [Google Protocol Buffers](#), so there is:

- formal schema files, defining the structure and data types involved
 - `protos/tech.proto`: main schema / entry point, includes the others
 - `protos/process_stack.proto`: describes details of the process stack, such as dielectrics and heights of layers
 - `protos/process_parasitics.proto`: parasitic tables, used to parametrize the 2.5D engine
- multiple concrete instantiations, that adhere to this schema (called *messages* in the `protobuf` lingo)
 - in the form of JSON files
 - Skywater 130A: `klayout_pex_protobuf/sky130A_tech.pb.json`
 - IHP SG13G2: `klayout_pex_protobuf/ihp_sg13g2_tech.pb.json`

 Note

The built-in JSON tech files are programmatically generated during the build process². Therefore they not part of the repository source code, but of course part of the deployed Python wheels. To review those, look into your Python `site-packages`³/`klayout_pex_protobuf`.

3.2 Customized PEX-“LVS” scripts

KLayout has built-in support for Layout-Versus-Schematic (LVS) scripts, based on its Ruby API. Customized “LVS” scripts are (“ab”) used in KPEX, not with the intent of comparing Layout-Versus-Schematic, but rather to extract the connectivity/net information for all polygons across multiple layers. The resulting net information is stored in a KLayout LVS Database (“LVSDB”).

²C++ generator scripts the built-in tech files are located in `cxx/gen_tech_pb/pdk/*.cpp`.

³To find the `site-packages` directory for the `klayout-pex` package, call `pip3 show klayout-pex`.

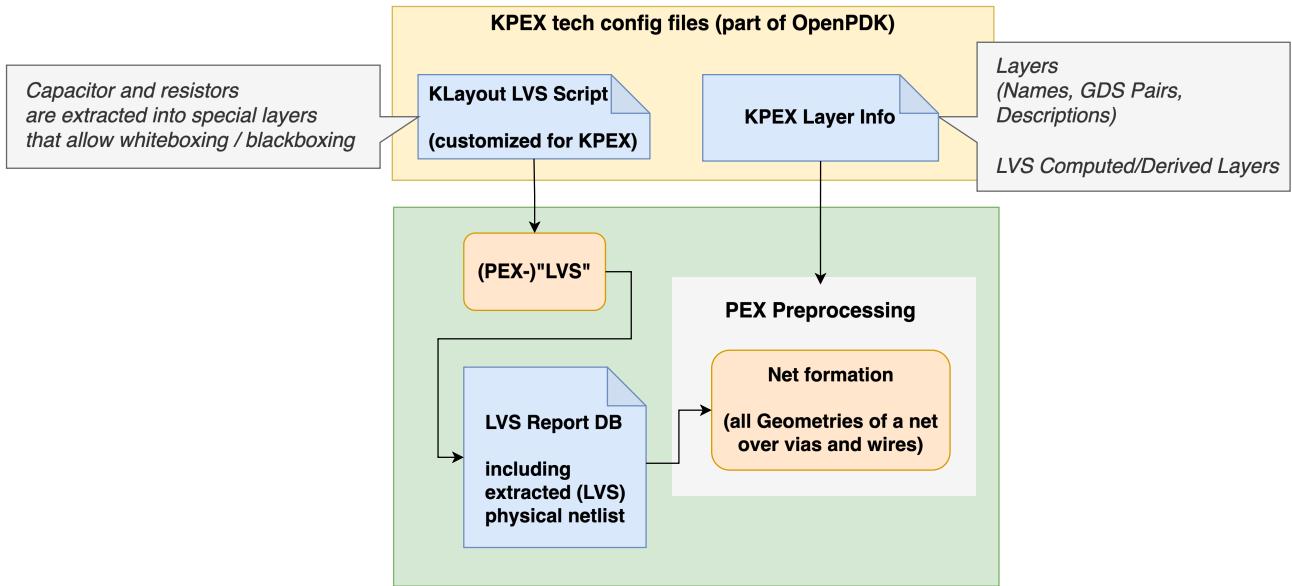


Figure 1: KPEX Net Formation

These customized “LVS” scripts are stored in:

- Skywater sky130A: [pdk/sky130A/libs.tech/kpex/sky130.lvs](#)
- IHP SG13G2: [pdk/ihp_sg13gs/libs.tech/kpex/sg13g2.lvs](#)

What's specific about this customization:

- Layers names must be assigned, using KLayout's `(name(layer, name))` function
- MOM⁴ capacitors, MIM⁵ capacitors and resistors should be extracted to separate layers, to enable blackboxing / whiteboxing.

The layer names in the script must correspond with the names configured in the tech JSON file.

⁴Metal-Oxide-Metal capacitors

⁵Metal-Insulator-Metal capacitors

4 KPEX/FasterCap Engine

FasterCap is a 3D and 2D parallel capacitance field solver, inspired by FastCap2. <https://www.fastfieldsolvers.com/fastercap.htm>

Starting from an input layout (e.g. GDS file) and a process stack-up (part of the Section 3.1), KPEX creates input geometries for FasterCap. After running FasterCap, the Maxwell capacitance matrix is parsed and interpreted to obtain the parasitic capacitances.

See Section 2.2 to get started with a first extraction example.

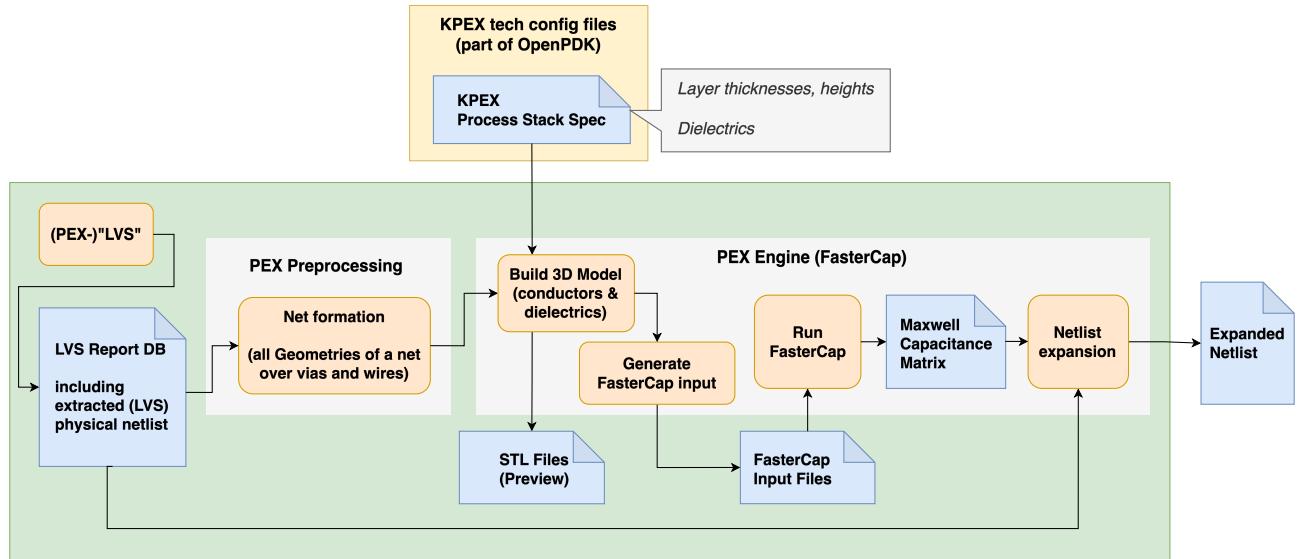


Figure 2: KPEX/FasterCap Engine

4.1 3D Input Geometries

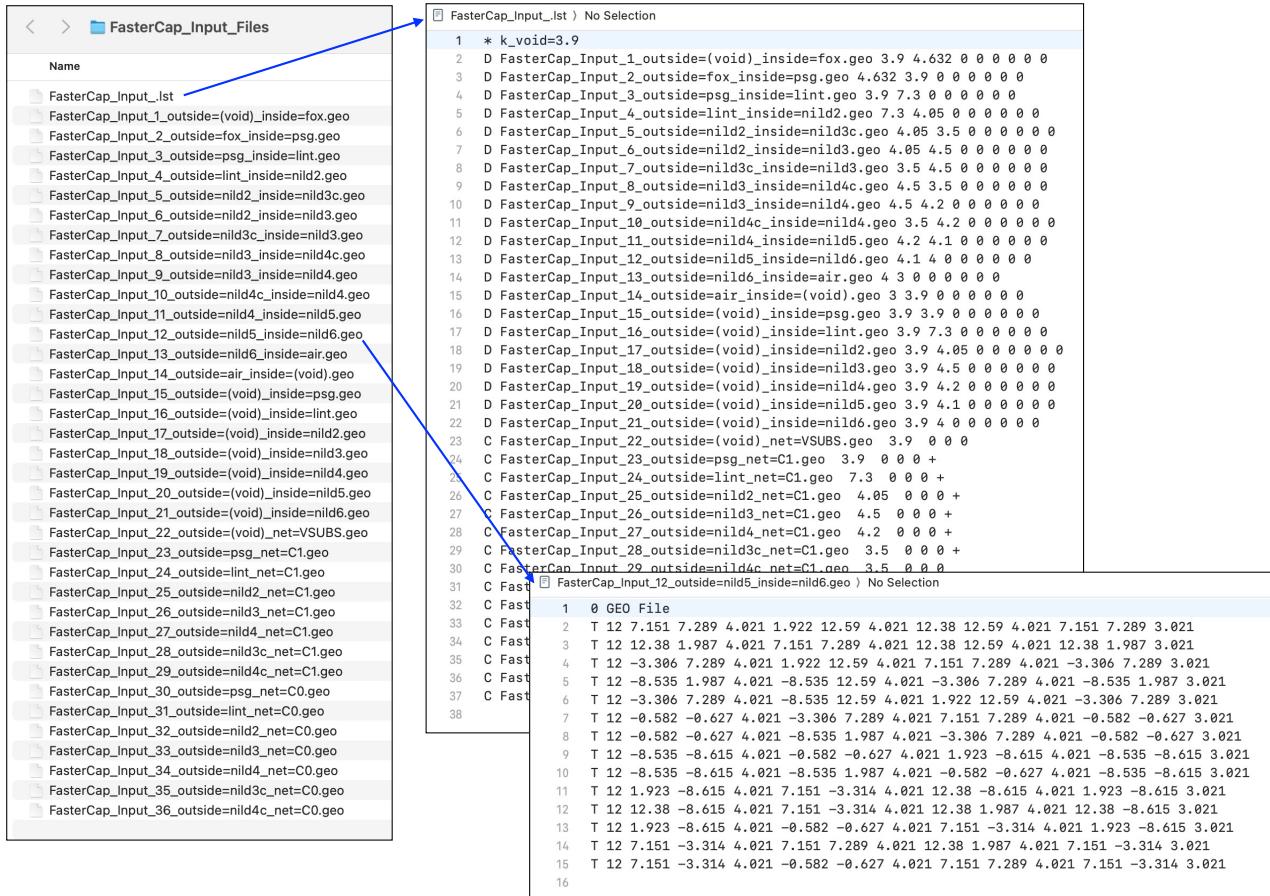


Figure 3: FasterCap 3D Input: File System Overview

The FasterCap input files and their format is documented in (Di Lorenzo 2019), a PDF version of the Windows-specific `*.chm` file is available at <https://github.com/martinjankoheler/FasterCap/tree/master/doc/pdf>.

KPEX generates 3D input geometries:

- `*.lst` file: Main input file
 - defines dielectric instances
 - defines conductor instances
 - each instance refers to a `*.geo` file
- `*.geo` files: Defines single geometry
 - defines shapes (e.g. triangles)
 - Each shape has a reference point to define inside/outsides

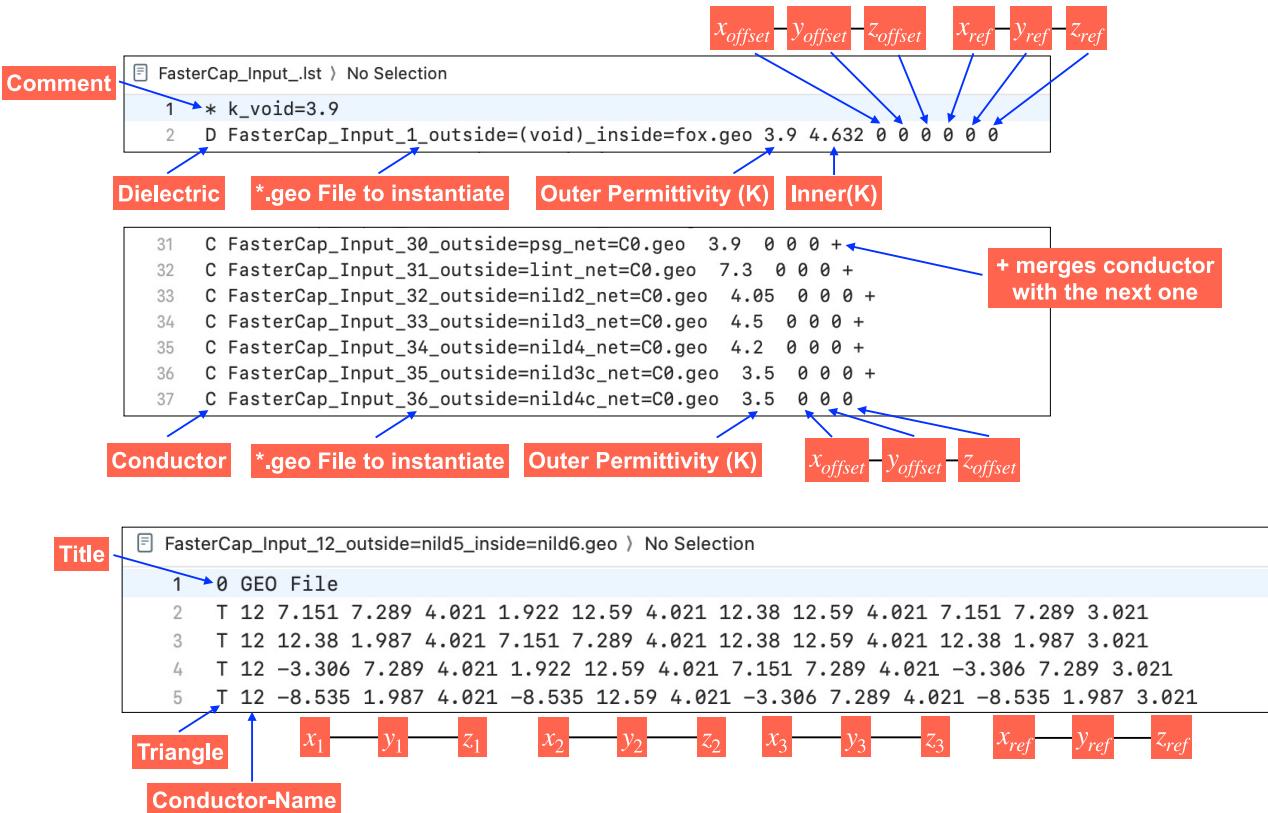


Figure 4: FasterCap 3D Input: File Format

4.2 Example: MOM Capacitor

Figure 5 depicts the MOM capacitor example of a from Section 2.2).

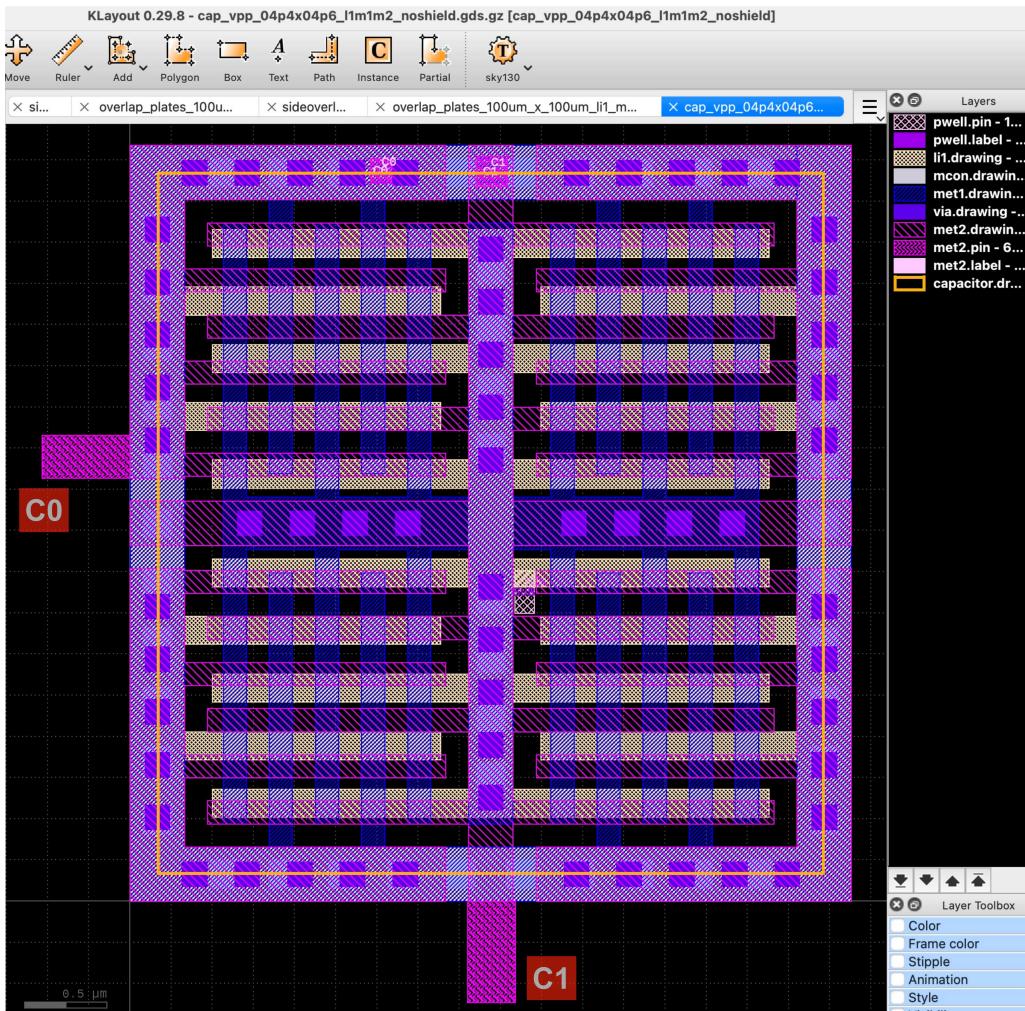
The corresponding schematic representation of Figure 6 contains 3 conductors (N_1 , N_2 and N_3), and coupling capacitances:

- Capacitances between conductors: C_{ij} where $i \neq j$
 - C_{23} is the capacitance “intended” by the MOM designer
- Capacitances between conductors and ground: C_{ii}

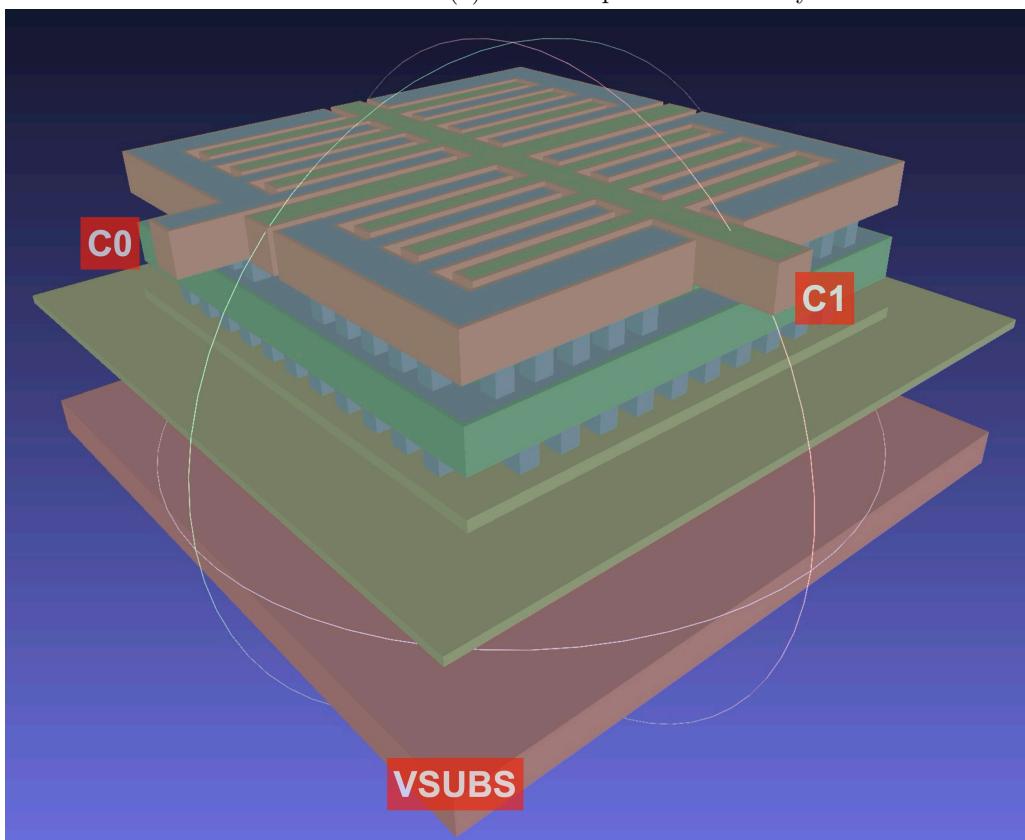
4.3 Output Maxwell Capacitance Matrix

A Maxwell capacitance matrix (Maxwell 1873) provides the relation between voltages on a set of conductors and the charges on these conductors, as described by the FasterCap author in the white paper (Di Lorenzo 2023).

FasterCap log output prints the Maxwell capacitance matrix (one for each iteration/refinement).



(a) MOM Capacitor: GDS Layout



(b) MOM Capacitor: MeshLab 3D Preview

Figure 5: MOM Capacitor

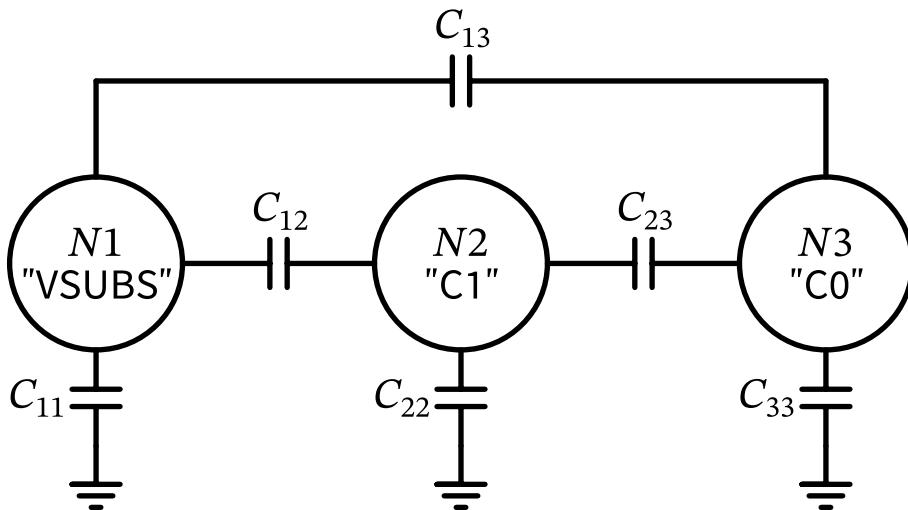


Figure 6: Schematic representation of the MOM capacitor.

```

Capacitance matrix is:
Dimension 3 x 3
g1_VSUBS  2.08888e-09 -1.46568e-10 -7.37007e-10
g2_C1    -1.64457e-10  1.47687e-08 -1.44368e-08
g3_C0    -7.68811e-10 -1.4528e-08  1.54806e-08

Weighted Frobenius norm of the difference between capacitance (auto option): 0.005031

Solve statistics:
Number of input panels: 18819 of which 5856 conductors and 12963 dielectric
Number of input panels to solver engine: 18819
Number of panels after refinement: 47371
Number of potential estimates: 6249961
Number of links: 19880193 (uncompressed 2244811641, compression ratio is 99.1%)
Max recursion level: 35
Max Mesh relative refinement value: 0.00126534
Time for reading input file: 0.014353s
Time for building super hierarchy: 0.001892s
Time for discretization: 0.562416s
Time for building potential matrix: 0.673007s
Time for precond calculation: 0.251937s
Time for gmres solving: 20.033398s

```

Figure 7: FasterCap Log Output: Maxwell Capacitance Matrix

- Matrix Properties:
 - Scaling: units have to be divided by 10^{-6}
 - rows and columns are the same (list of net names)
 - Row Cells:
 - * off diagonals cells contains the coupling between row/col nets (times -1)
 - * diagonal cells contains the sum of the absolute values of all other cells in the row
 - Matrix Symmetry:
 - * in theory (ideal world), the matrix would be symmetric
 - * in practice it's not
 - * therefore FastCap2 did average the off-diagonals
 - * FasterCap does not average, so it's done as part of KPEX

$$C_{3 \times 3} = \begin{bmatrix} \text{VSUBS} & \text{C0} & \text{C1} \\ c_{11} + c_{12} + c_{13} & -c_{12} & -c_{13} \\ -c_{21} & c_{22} + c_{23} + c_{23} & -c_{23} \\ -c_{31} & -c_{32} & c_{31} + c_{32} + c_{33} \end{bmatrix} \begin{bmatrix} \text{VSUBS} \\ \text{C0} \\ \text{C1} \end{bmatrix}$$

$$C_{avg} = \begin{bmatrix} c_{11} - |\text{avg}(c_{12}, c_{21})| - |\text{avg}(c_{13}, c_{31})| & |\text{avg}(c_{12}, c_{21})| & |\text{avg}(c_{13}, c_{31})| \\ |\text{avg}(c_{12}, c_{21})| & c_{22} - |\text{avg}(c_{12}, c_{21})| - |\text{avg}(c_{23}, c_{32})| & |\text{avg}(c_{23}, c_{32})| \\ |\text{avg}(c_{13}, c_{31})| & |\text{avg}(c_{23}, c_{32})| & c_{33} - |\text{avg}(c_{13}, c_{31})| - |\text{avg}(c_{23}, c_{32})| \end{bmatrix}$$

$$\begin{aligned} C_{femtofarad} &= \begin{bmatrix} 2.09 - \text{avg}(0.147, 0.164) - \text{avg}(0.74, 0.77) & \text{avg}(0.147, 0.164) & \text{avg}(0.74, 0.77) \\ \text{avg}(0.147, 0.164) & 14.77 - \text{avg}(0.147, 0.164) - \text{avg}(14.44, 14.52) & \text{avg}(14.44, 14.52) \\ \text{avg}(0.74, 0.77) & \text{avg}(14.44, 14.52) & 15.48 - \text{avg}(0.74, 0.77) - \text{avg}(14.44, 14.52) \end{bmatrix} \\ &= \begin{bmatrix} 1.18 & 0.16 & 0.75 \\ 0.16 & 0.13 & 14.48 \\ 0.75 & 14.48 & 0.25 \end{bmatrix} \end{aligned}$$

Result CSV

Device	Net1	Net2	Capacitance [F]	Capacitance [fF]
Cext_0_1	VSUBS	C1	1.555125e-16	0.16f
Cext_0_2	VSUBS	C0	7.52909e-16	0.75f
Cext_1_2	C1	C0	1.44824e-14	14.48f
Cext_1_1	C1	VSUBS	1.307875e-16	0.13f
Cext_2_2	C0	VSUBS	2.45291e-16	0.25f

Figure 8: FasterCap Maxwell Capacitance Matrix: Interpretation

5 KPEX/MAGIC Engine

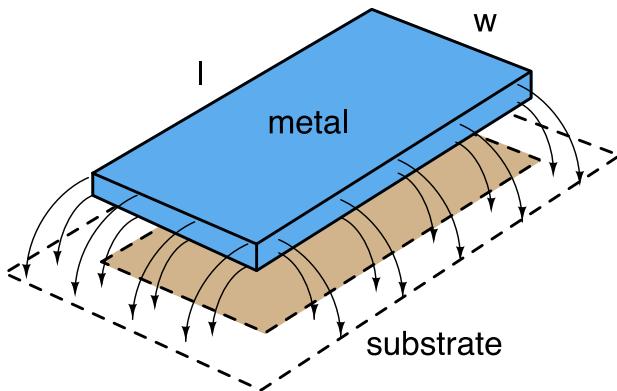
This engine is merely just a wrapper around `magic`, which prepares a TCL script that opens the layout file and starts MAGIC's PEX flow. See Section 2.3 to get started with a first extraction example.

5.1 Types of Parasitic Capacitances

MAGIC models multiple types of capacitances:

- *Substrate Overlap*: Overlap area of a metal with the substrate
- *Substrate Fringing*: Sidewall of a metal fringes out to substrate
- *Sidewall Capacitance*: Coupling between adjacent sidewalls on the same layer
- *Overlap Capacitance*: Overlap on different metal layers
- *Fringe Capacitance (“Side Overlap”)*: Sidewall of a metal fringes out other metal layers

5.2 Substrate Capacitance



- Overlapping area:

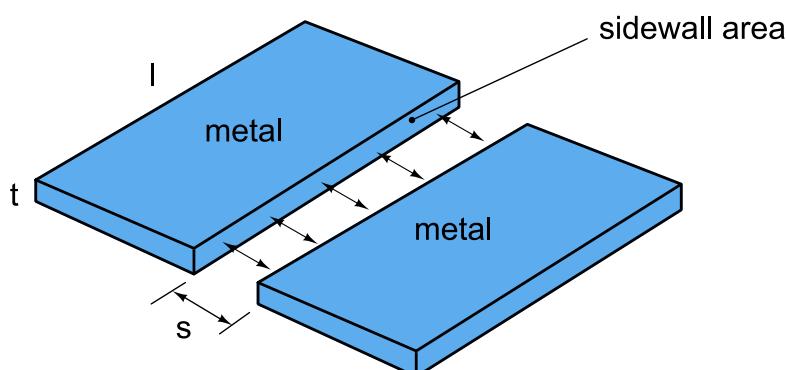
$$C_{area} = \frac{\epsilon_{si} * K}{d} * \text{area} \quad \left[\frac{F}{\mu m^2} * \mu m^2 \right]$$

- Fringe (“Perimeter”):

$$C_{fringe \text{ to } substrate} = \text{perimeter} * C_{perim} = (2l + 2w) * C_{perim}$$

- Coefficients like C_{perim} are part of the tech files (Parasitic Tables)

5.3 Sidewall Capacitance



$$\begin{aligned}
 C_{sidewall} &= \frac{\epsilon_{si} * K}{s} * \text{sidewall area} \quad \left[\frac{F}{\mu m^2} * \mu m^2 \right] \\
 &= \frac{\epsilon_{si} * K}{s} * t * l \quad \left[\frac{F}{\mu m^2} * \mu m * \mu m \right] \\
 C_{sidewall} &= \frac{C_{sidewall\ coeff}}{s} * l \quad \left[\frac{F}{\mu m} * \mu m \right]
 \end{aligned}$$

- Coefficients are part of the tech files (Parasitic Tables)
- Layer thickness t is normally multiplied into the coefficient
- Foundry tables give constant coefficient referenced to $s = 1$

5.4 Overlap Capacitance

- Overlapping area:

$$C_{area} = \frac{\epsilon_{si} * K}{d} * \text{area} \quad \left[\frac{F}{\mu m^2} * \mu m^2 \right]$$

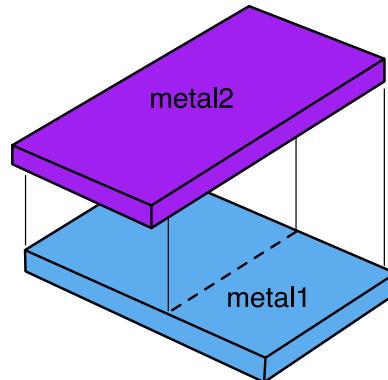


Figure 9: Overlap Capacitance

5.5 Fringe Capacitance

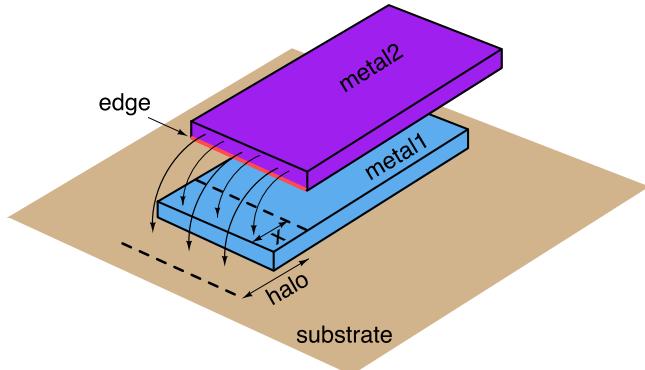


Figure 10: Fringe Capacitance: Overlapping (1)

- Causing sidewall (its bottom edge depicted red)
- Assume: Field is bounded by fringe halo (e.g. $8 \mu m$ away from edge)
- Fractions of fringe goes to metal1 or substrate

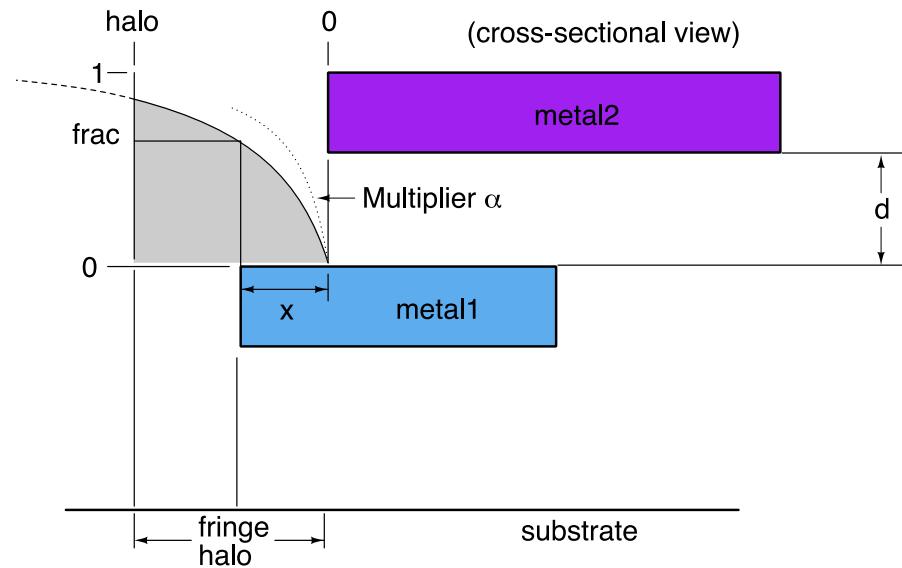


Figure 11: Fringe Capacitance: Overlapping (2)

- Multiplier α (comes from tech files: overlap table)
 - determines how quickly fringe capacitance drops with increasing distance
 - α is related to distance d between layers
 - α is proportional to $C_{overlap_{metal1 \leftrightarrow metal2}} = \frac{\epsilon_{si} * K}{d} * \text{area}$
(for fixed value of area $1 \mu\text{m}^2$)
- Fringe Fractions:
 - $\text{frac}_{metal1} = \frac{2}{\pi} * \text{atan}(\alpha_{metal2 \rightarrow metal1} * x)$
 - $\text{frac}_{sub} = \frac{2}{\pi} * \text{atan}(\alpha_{metal2 \rightarrow sub} * (\text{halo} - x))$
 - $\frac{2}{\pi}$ is multiplied because of scaling to interval $[0.0, 1.0]$, as $\text{atan}(\infty) = \frac{\pi}{2}$
- Overlap capacitance:
 - $C_{overlap} = \frac{\epsilon_{si} * K}{d} * \text{area}$ (with area = $1 \mu\text{m}^2$)
- Coupling capacitance $metal1 \leftrightarrow metal2$:
 - $\alpha_{metal1 \leftrightarrow metal2} = \alpha_{scalefac} * C_{overlap_{metal1 \leftrightarrow metal2}}$
 - $\text{frac}_{metal1} = \frac{2}{\pi} * \text{atan}(\alpha_{metal1 \leftrightarrow metal2} * x)$
 - effective length = edge length * frac_{metal1}
 - $C_{fringe_{metal2 \rightarrow metal1}} = \text{effective length} * C_{sideoverlap_{metal2 \rightarrow metal1}}$
- Coupling capacitance $metal1 \leftrightarrow sub$:
 - $\alpha_{metal1 \leftrightarrow sub} = \alpha_{scalefac} * C_{overlap_{metal1 \leftrightarrow sub}}$
 - $\text{frac}_{sub} = \frac{2}{\pi} * \text{atan}(\alpha_{metal1 \leftrightarrow sub} * (\text{halo} - x))$
 - effective length = edge length * frac_{sub}
 - $C_{fringe_{metal2 \rightarrow sub}} = \text{effective length} * C_{sideoverlap_{metal2 \rightarrow sub}}$

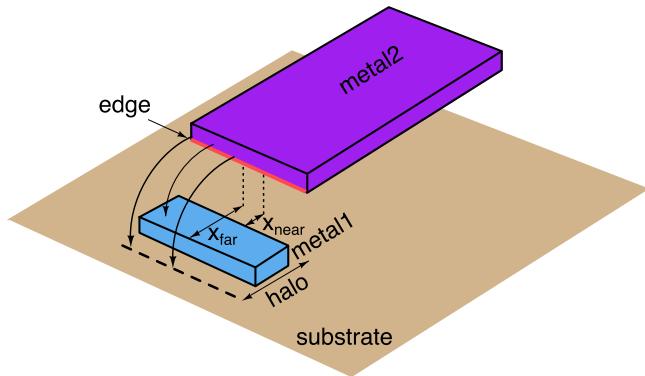


Figure 12: Fringe Capacitance: Non Overlapping (1)

- Partial side overlap
 - In case there is only a partial side overlap, the non-existing near fraction is subtracted from the far fraction
 - *metal1* wire is offset, starts at x_{near}
 - *metal1* ends at x_{far}

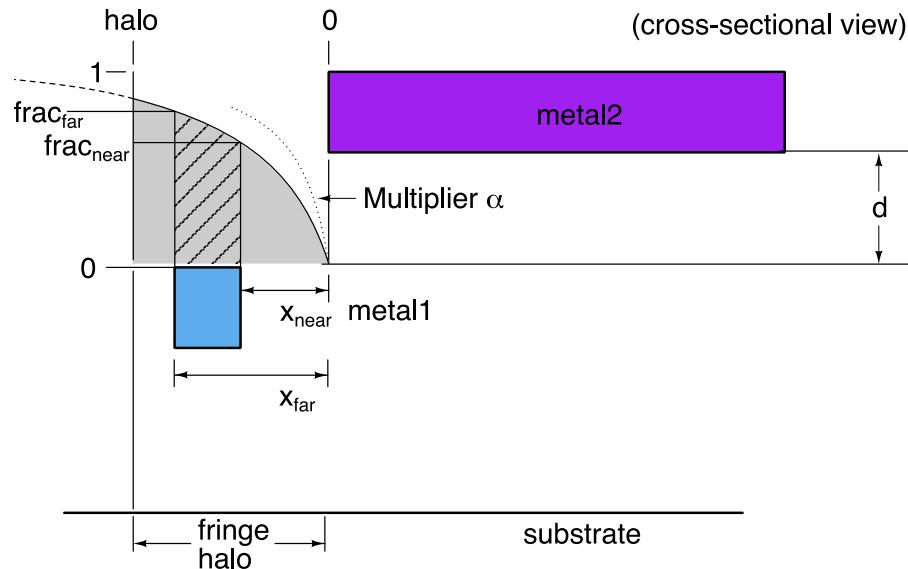


Figure 13: Fringe Capacitance: Non Overlapping (2)

- $\text{frac}_{near} = \frac{2}{\pi} * \text{atan}(\alpha * x_{near})$
- $\text{frac}_{far} = \frac{2}{\pi} * \text{atan}(\alpha * x_{far})$
- $\text{frac} = \text{frac}_{far} - \text{frac}_{near}$

5.6 Shielding Effects

Table 2: Shielding effects

Type	Shielding To Substrate	Between layers	On same layer
Overlap shielding	✓	✓	✗
Sidewall shielding	✗	✗	✓
Lateral fringe shielding	✗	✓	✓
Vertical fringe shielding	✓	✓	✗

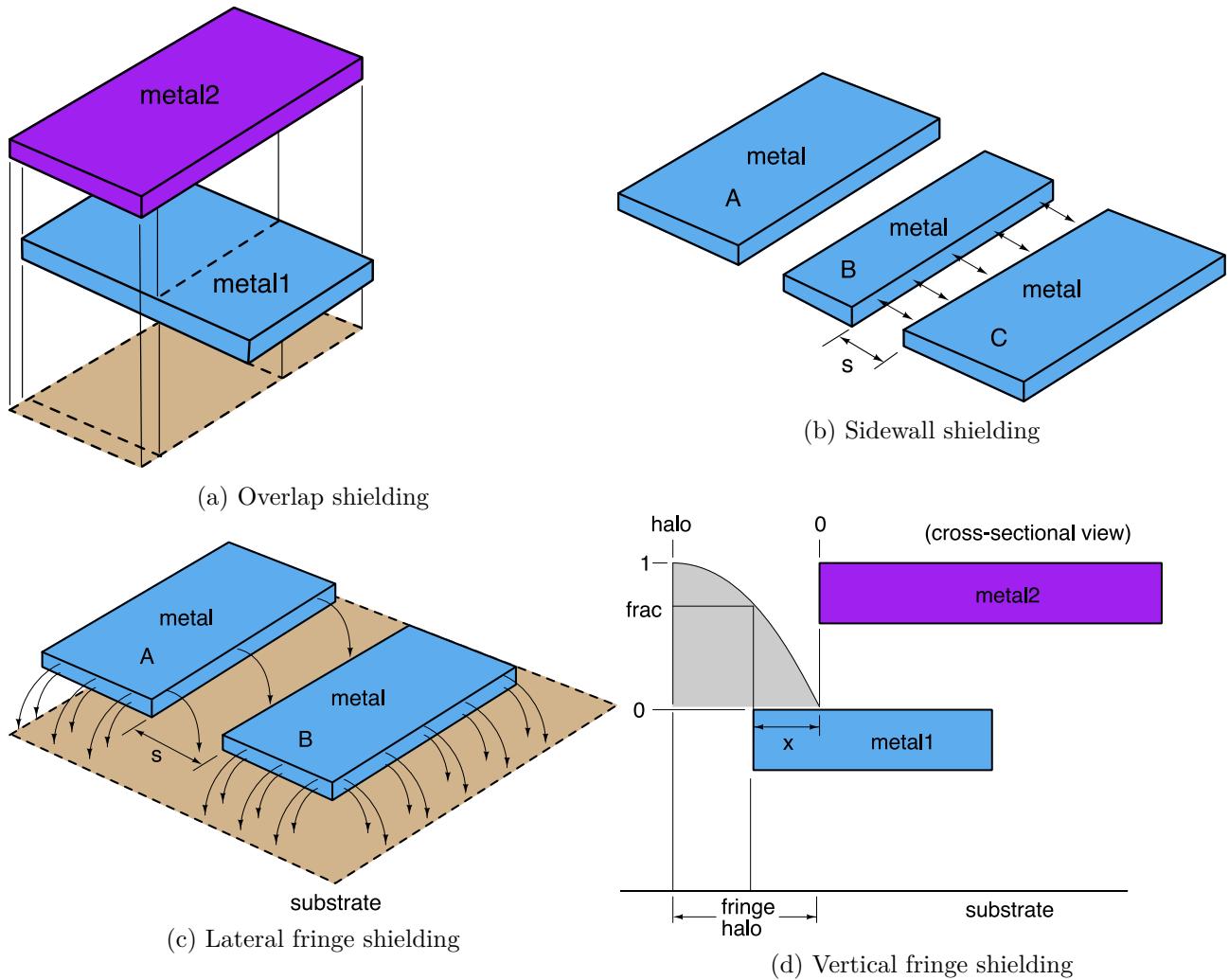


Figure 14: Shielding Effects

6 KPEX/2.5D Engine

Field solvers are precise, yet slow, they are useful to obtain a golden reference.

For most use cases, a faster engine is desirable-. KPEX/MAGIC is such an engine, but the MAGIC code is tightly coupled with the database, layer/via design choices, and user interface of MAGIC. For example, it runs single-threaded.

Therefore, the KPEX 2.5D Engine intends to implement the concepts and formulas of MAGIC (see Section 5.1), but in a way that is best suited to the KLayout API.

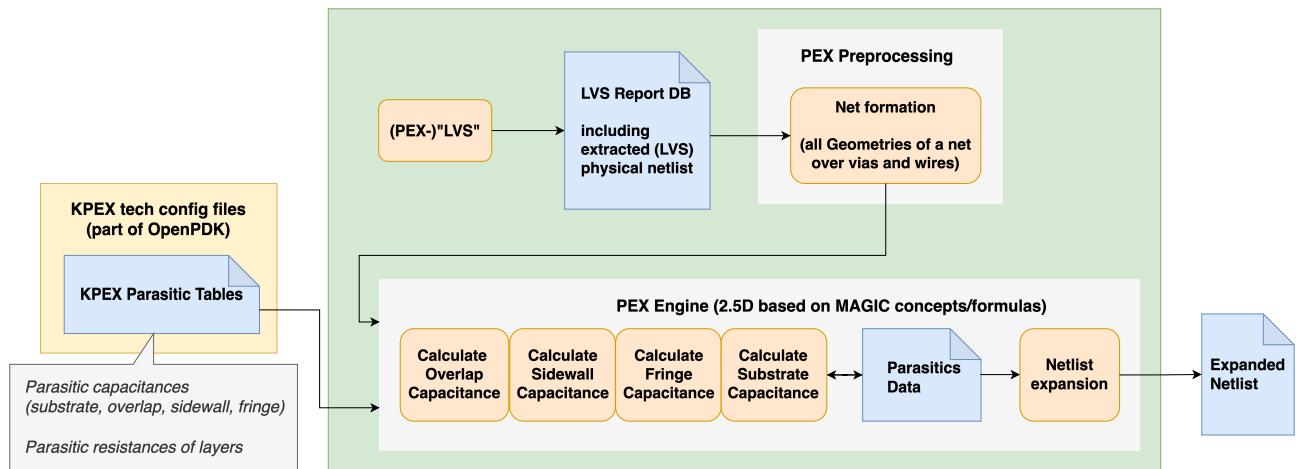


Figure 15: KPEX 2.5D Engine



This section is under heavy construction!



7 Footnotes

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