

CodeGen Overview and Focus on Selection DAGs

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What does CodeGen do?

- * A very large analysis
- * Input: LLVM IR
- * Output: Machine Code
 - * optimize for “efficient” generated code
 - * run quickly

CodeGen Phases

- * Preparation
- * Selection DAG
 - * Instruction Selection and Scheduling
- * Register Allocation
- * Output

Intro

Input: LLVM IR

bb:

```
%i = phi i32 [ 0, %entry ], [ %i.next, %bb ]  
%sum = phi double [ 0.0, %entry ], [ %sum.next, %bb ]
```

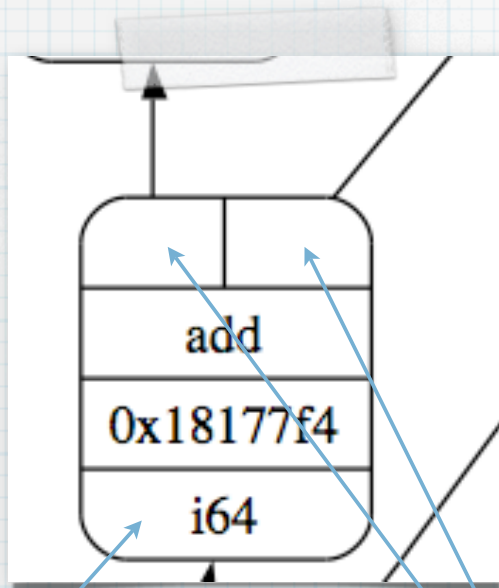
```
%t0 = getelementptr i64* %x, i32 %i  
%t1 = load i64* %t0  
%t2 = mul i64 %t1, 101  
%t3 = add i64 %t2, 3  
store i64 %t3, i64* %t0
```

```
%t4 = getelementptr double* %y, i32 %i  
%t5 = load double* %t4  
%sum.next = add double %sum, %t5
```

```
%i.next = add i32 %i, 1  
%exitcond = icmp eq i32 %i.next, %n  
br i1 %exitcond, label %return, label %bb
```

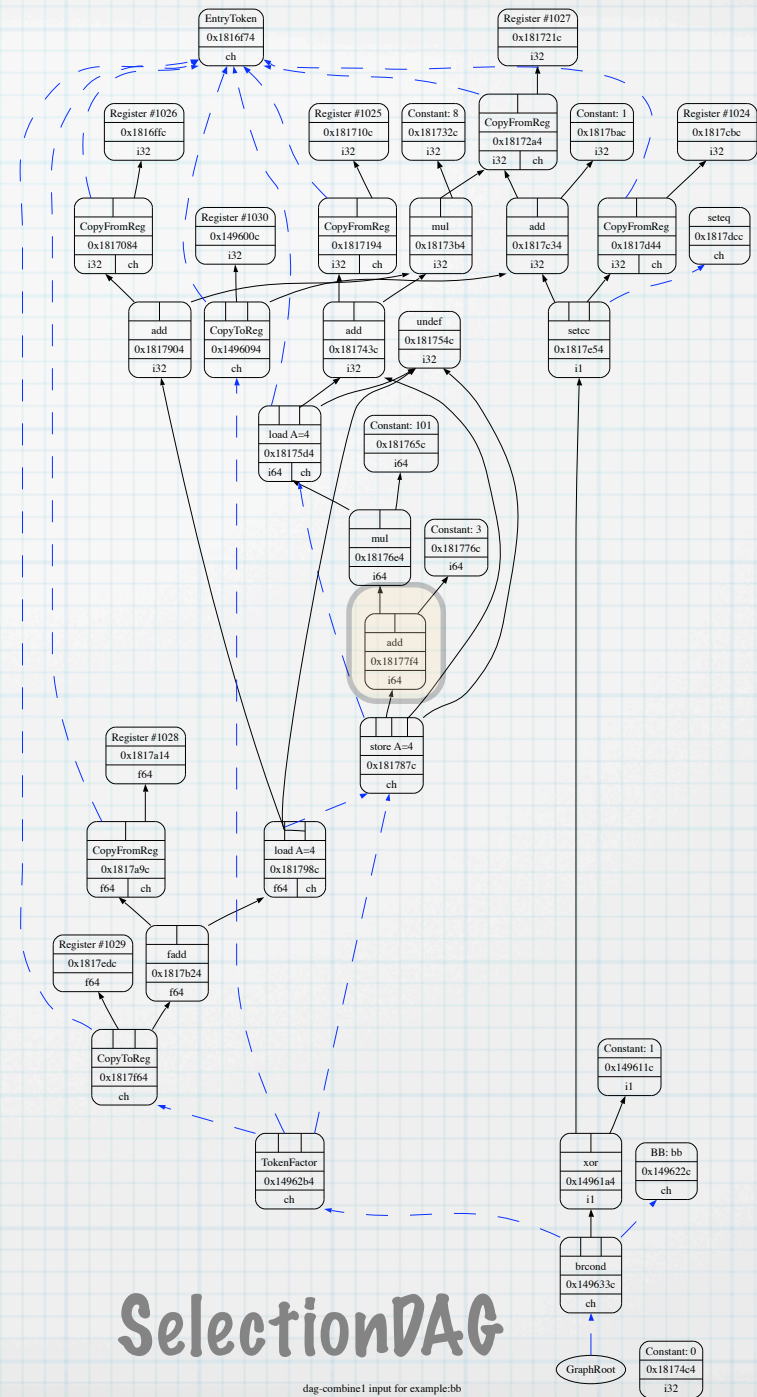
Intro

SDNode



SDValue

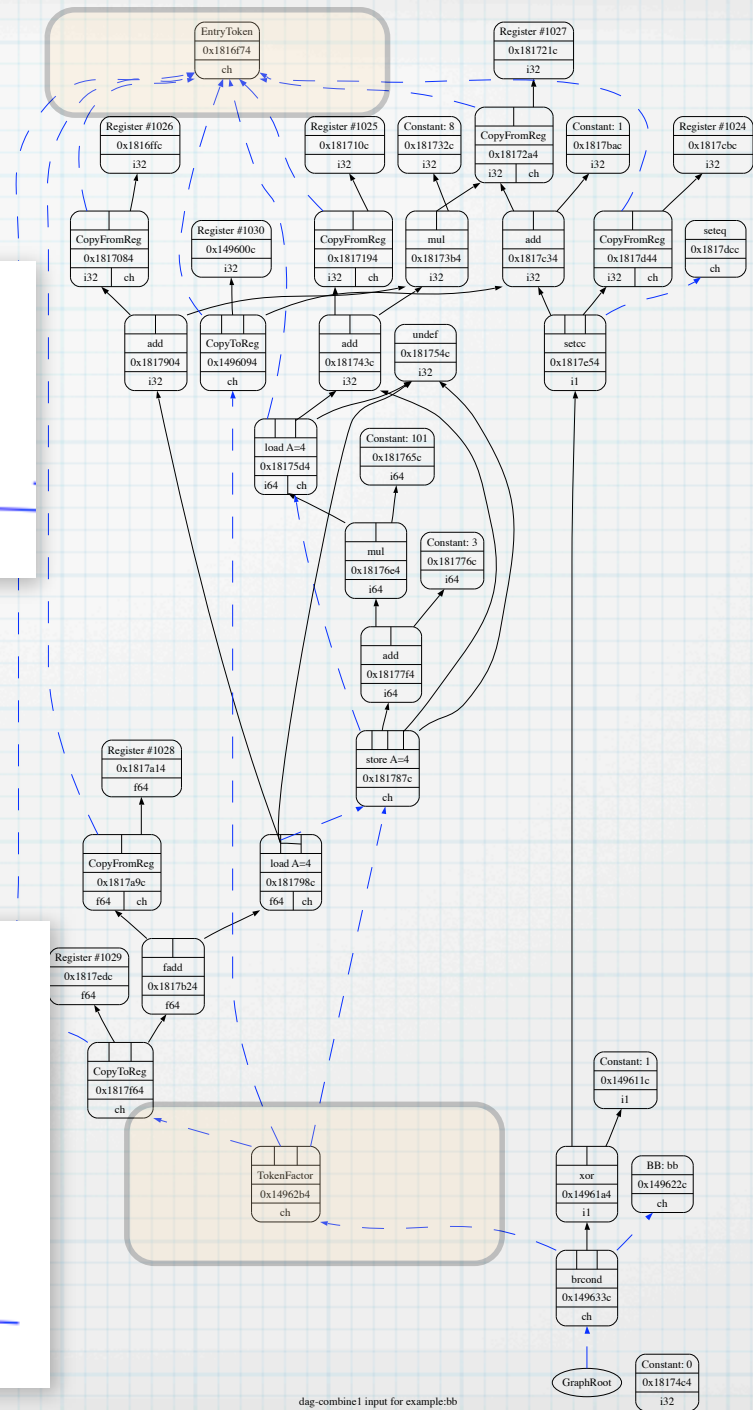
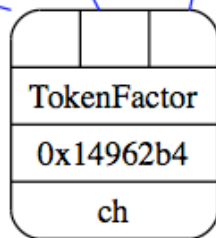
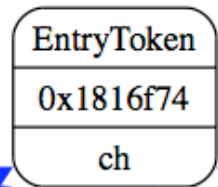
SDUse



SelectionDAG

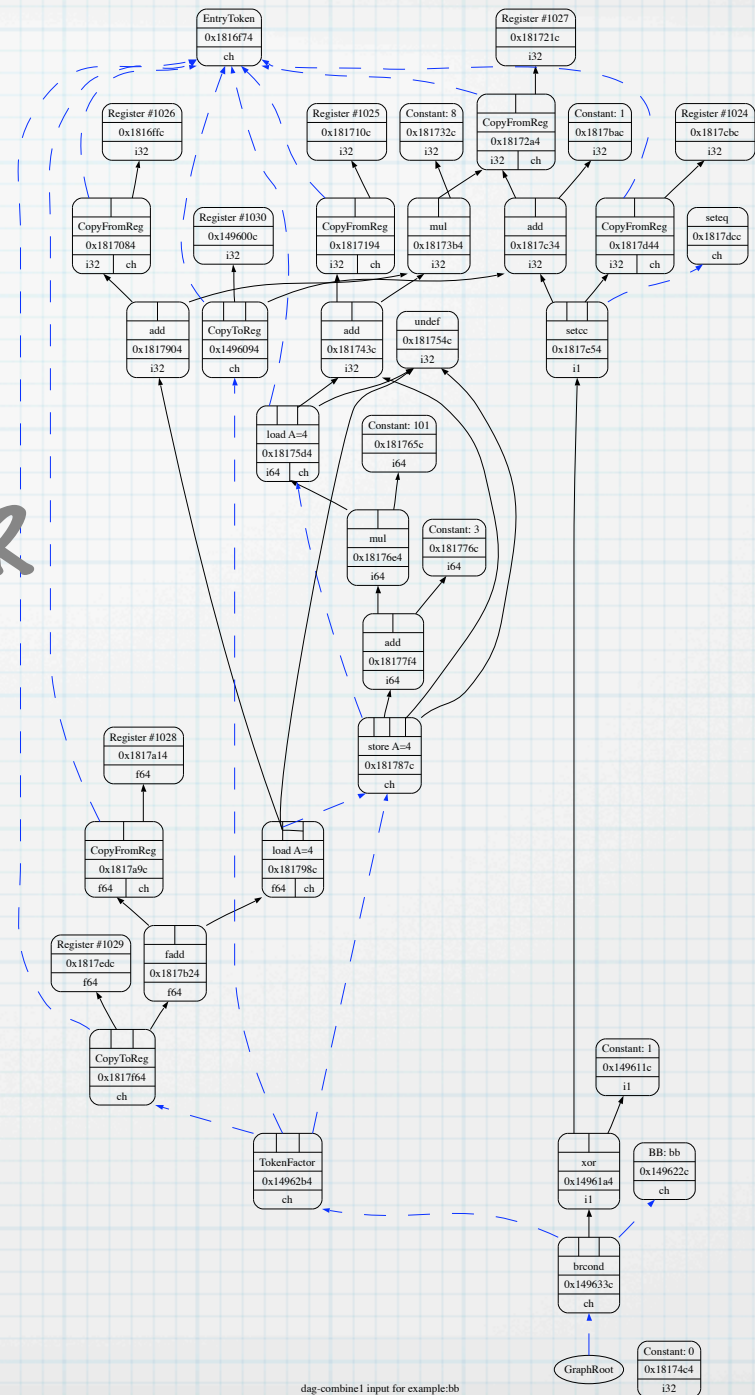
dag-combine! input for example:bb

Intro



Intro

- * Unique use of DAG-based IR
- * Automatic CSE
- * Lower Level than LLVM
- * `llc -view-*-dags`



dag-combine1 input for example:bb

Selection DAG Phases

Lower

Combine

Legalize

Combine

Select

Schedule

bb:

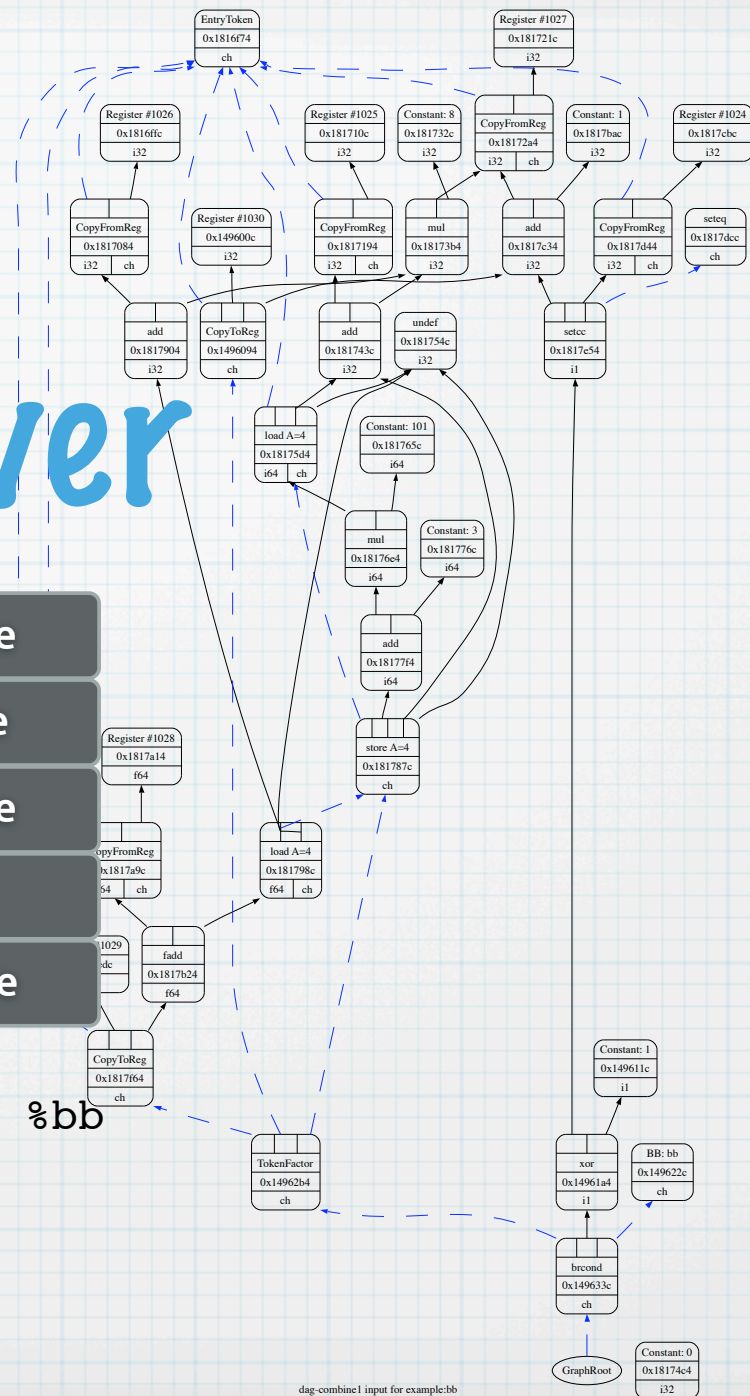
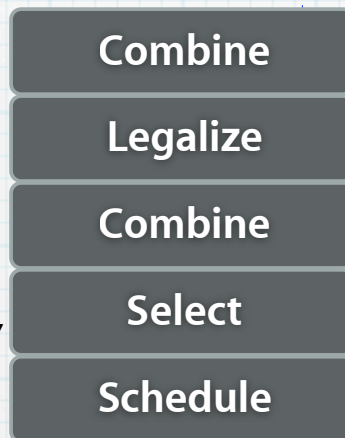
```
%i = phi i32 [ 0, %entry ],
          [ %i.next, %bb ]
%sum = phi double [ 0.0, %entry ],
                 [ %sum.next, %bb ]
```

```
%t0 = getelementptr i64* %x, i32 %i
%t1 = load i64* %t0
%t2 = mul i64 %t1, 101
%t3 = add i64 %t2, 3
store i64 %t3, i64* %t0
```

```
%t4 = getelementptr double*
%t5 = load double* %t4
%sum.next = add double %sum,
```

```
%i.next = add i32 %i, 1
%exitcond = icmp eq i32 %i.next, %n
br i1 %exitcond, label %return, label %bb
```

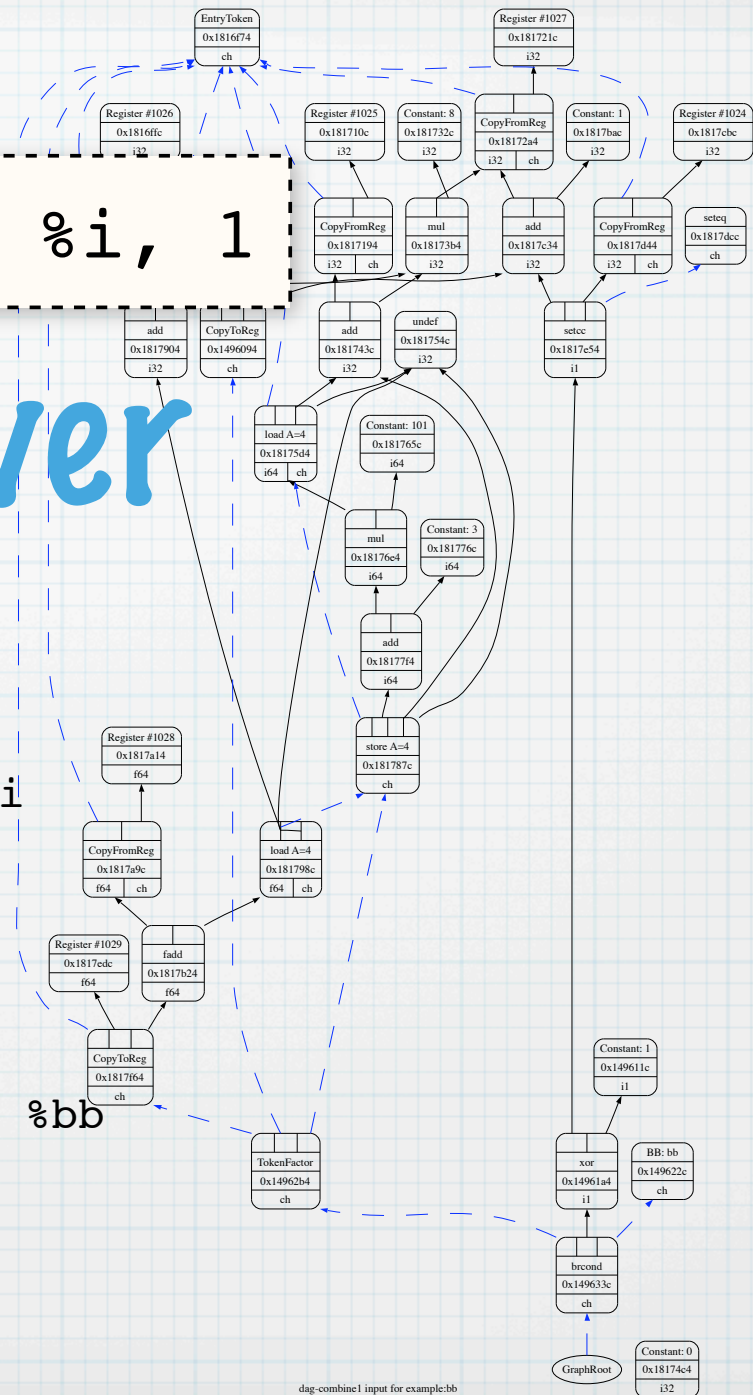
Lower



```
%i = phi i32 [ 0, %entry ], [ %i.next, %bb ]
%sum = phi double [ 0.0, %entry ], [ %sum.next, %bb ]
```

Lower

```
%i.next = add i32 %i, 1
%exitcond = icmp eq i32 %i.next, %n
br i1 %exitcond, label %return, label %bb
```



bb:

```
%i = phi i32 [ 0, %entry  
              [ %i.next,  
%sum = phi double [ 0.0, %entry ],  
                  [ %sum.next, %bb ]
```

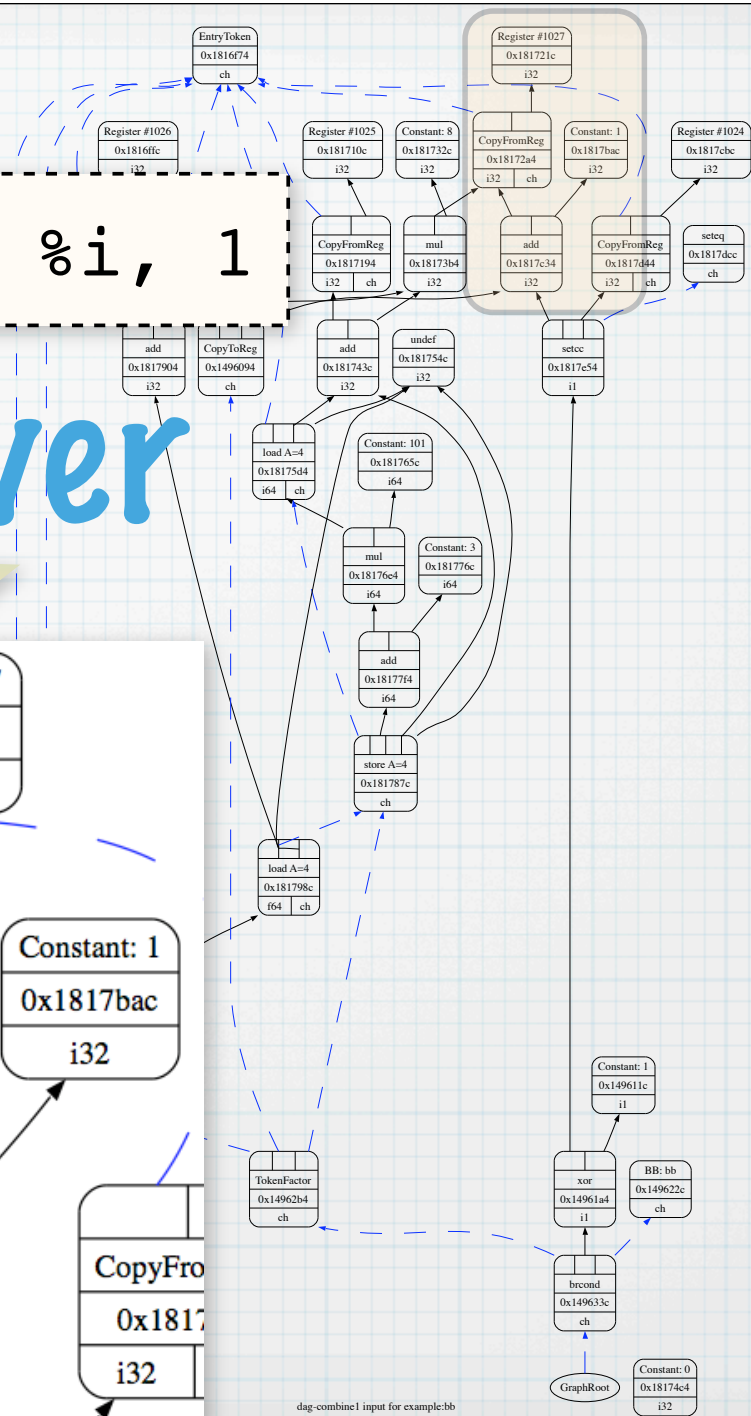
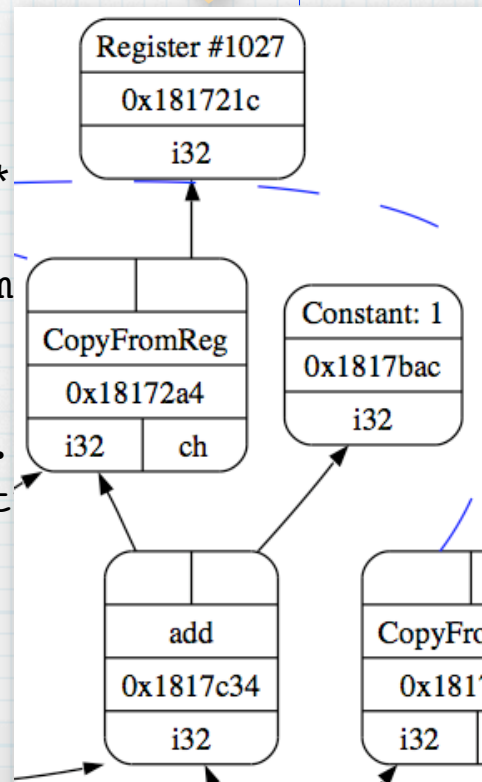
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%t1 = load i64* %t0  
%t2 = mul i64 %t1, 101  
%t3 = add i64 %t2, 3  
store i64 %t3, i64* %t0
```

```
%t4 = getelementptr double*  
%t5 = load double* %t4  
%sum.next = add double %sum
```

```
%i.next = add i32 %i, 1  
%exitcond = icmp eq i32 %i.  
br i1 %exitcond, label %ret
```

add i32 %i, 1

Lower



bb:

```
%i = phi i32 [ 0, %entry
               [ %i.next,
```

```
%sum = phi double [ 0.0, %entry ],
                  [ %sum.next, %bb ]
```

```
%t0 = getelementptr i64* %x, i32 %i
```

```
%t1 = load i64* %t0
```

```
%t2 = mul i64 %t1, 101
```

```
%t3 = add i64 %t2, 3
```

```
store i64 %t3, i64* %t0
```

```
%t4 = getelementptr double* %y, i32 %i
```

```
%t5 = load double* %t4
```

```
%sum.next = add double %sum, %t5
```

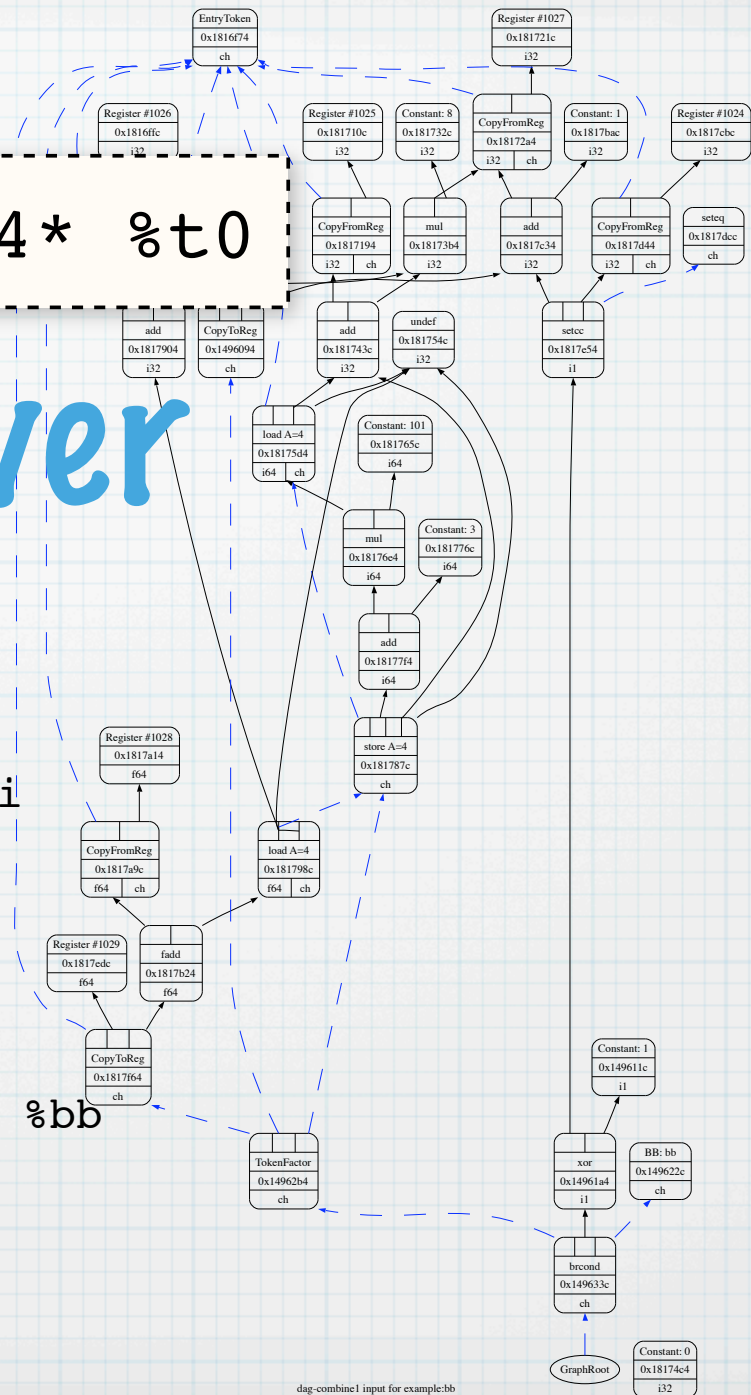
```
%i.next = add i32 %i, 1
```

```
%exitcond = icmp eq i32 %i.next, %n
```

```
br i1 %exitcond, label %return, label %bb
```

load i64* %t0

Lower



bb:

```
%i = phi i32 [ 0, %entry  
            [ %i.next,
```

```
%sum = phi double [ 0.0, %entry ],  
                [ %sum.next, %bb ]
```

```
%t0 = getelementptr i64* %x, i32 %i
```

```
%t1 = load i64* %t0
```

```
%t2 = mul i64 %t1, 101
```

```
%t3 = add i64 %t2, 3
```

```
store i64 %t3, i64* %t0
```

```
%t4 = getelementptr double*
```

```
%t5 = load double* %t4
```

```
%sum.next = add double %sum,
```

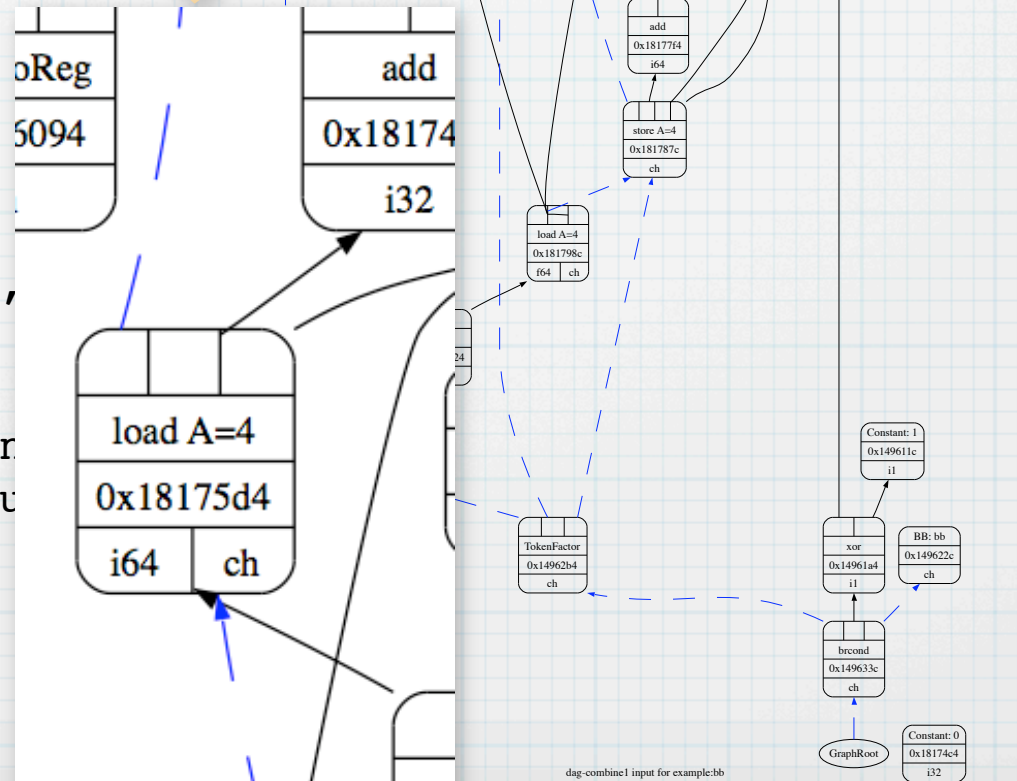
```
%i.next = add i32 %i, 1
```

```
%exitcond = icmp eq i32 %i.r
```

```
br i1 %exitcond, label %retu
```

load i64* %t0

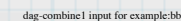
Lower




```
br i1 %exitcond, label %return, label %bb
```

```
%t0 = getelementptr i64* %x, i32 0, i32 0
%t1 = load i64* %t0
%t2 = mul i64 %t1, 101
%t3 = add i64 %t2, 3
store i64 %t3, i64* %t0
```

```
%i.next = add i32 %i, 1
%exitcond = icmp eq i32 %i.next, %n
br i1 %exitcond, label %return, label %bb
```



bb:

```
br i1 %exitcond, label %return, label %bb
```

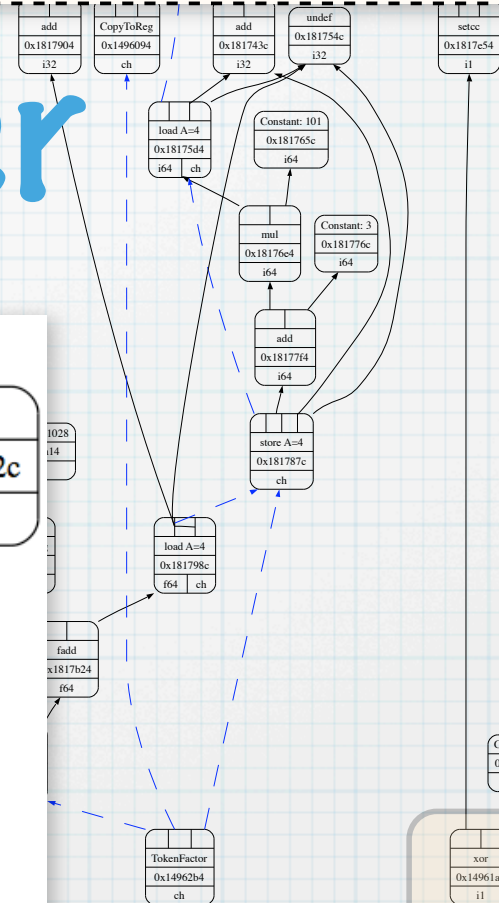
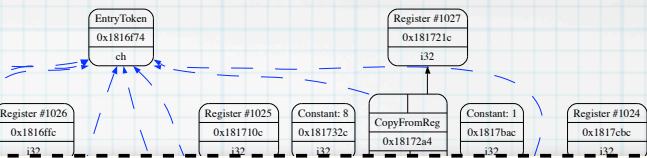
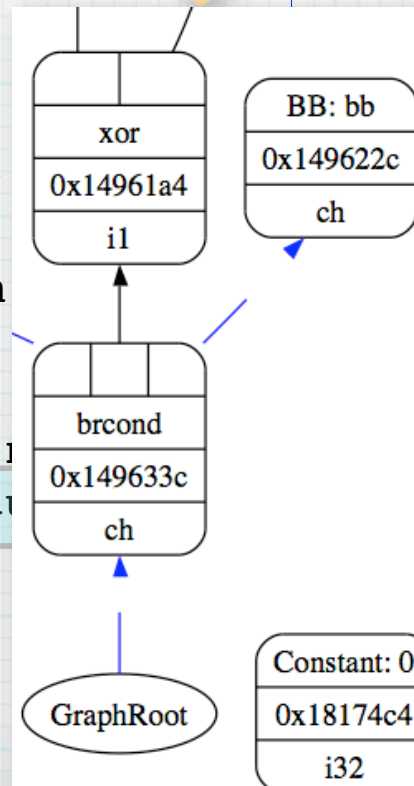
```
%sum = ptr_double [ 0.0, %entry ],  
[ %sum.next, %bb
```

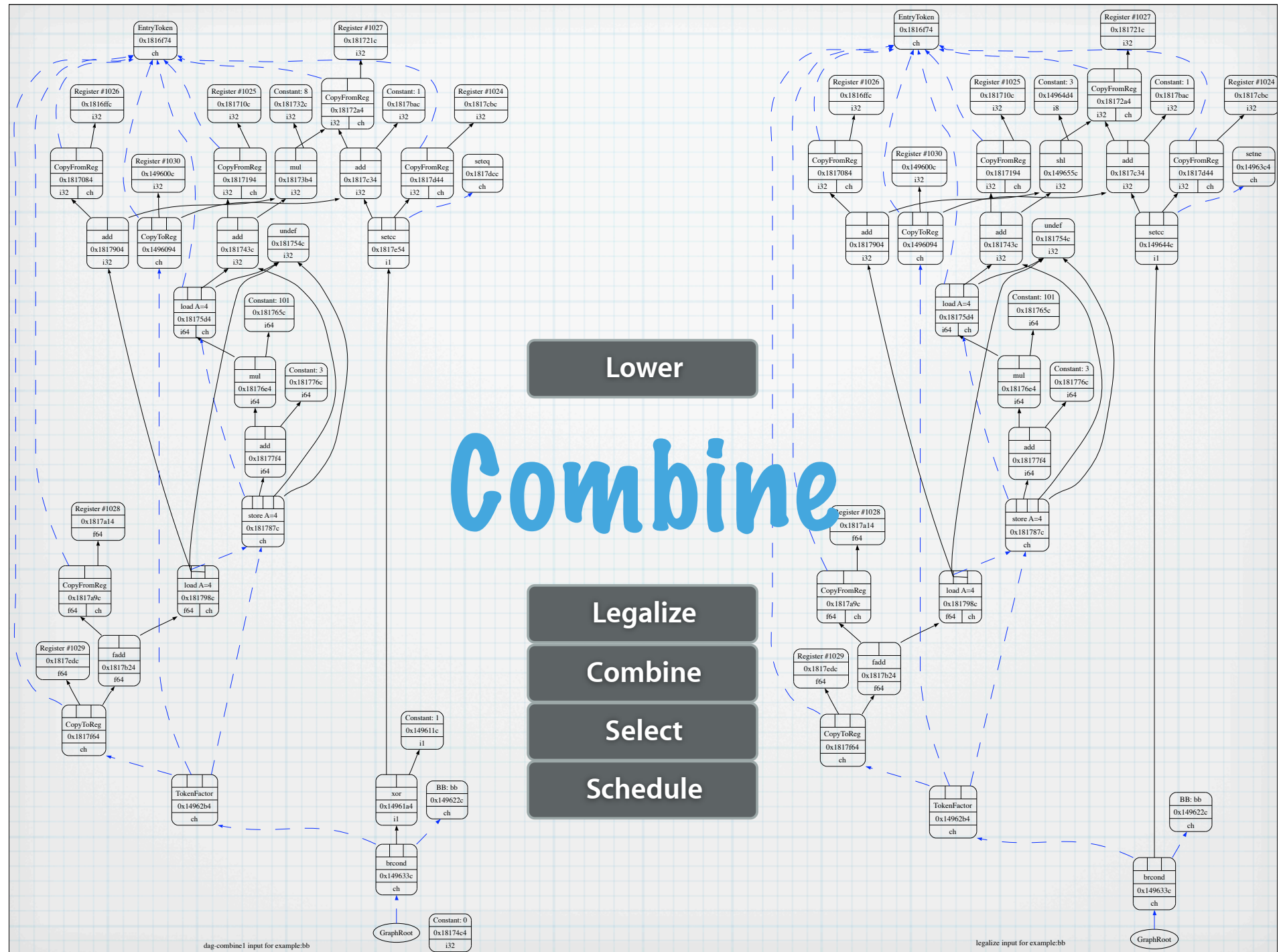
```
%t0 = getelementptr i64* %x, i32  
%t1 = load i64* %t0  
%t2 = mul i64 %t1, 101  
%t3 = add i64 %t2, 3  
store i64 %t3, i64* %t0
```

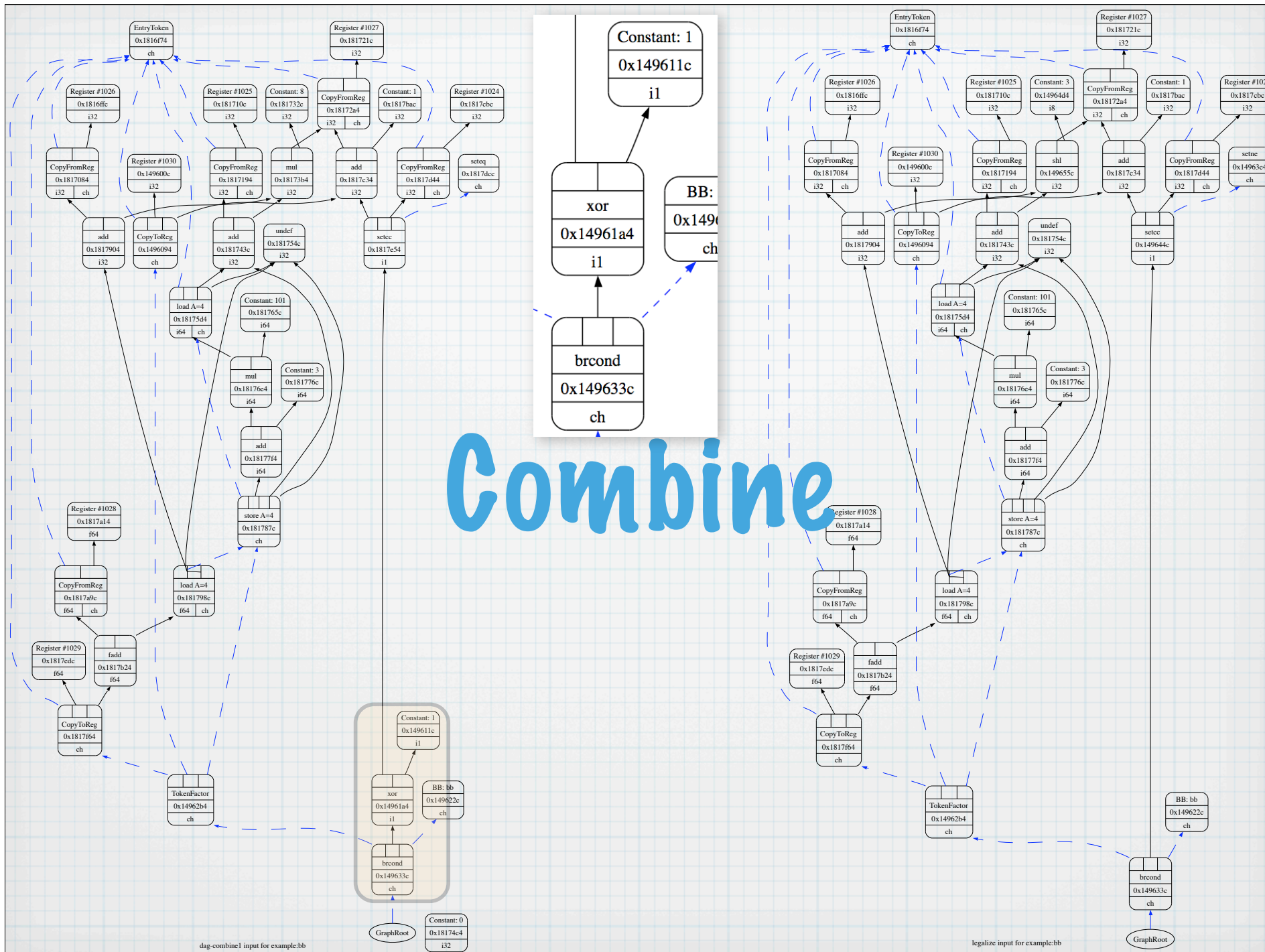
```
%t4 = getelementptr double*  
%t5 = load double* %t4  
%sum.next = add double %sum
```

```
%i.next = add i32 %i, 1  
%exitcond = icmp eq i32 %i,  
br i1 %exitcond, label %ret
```

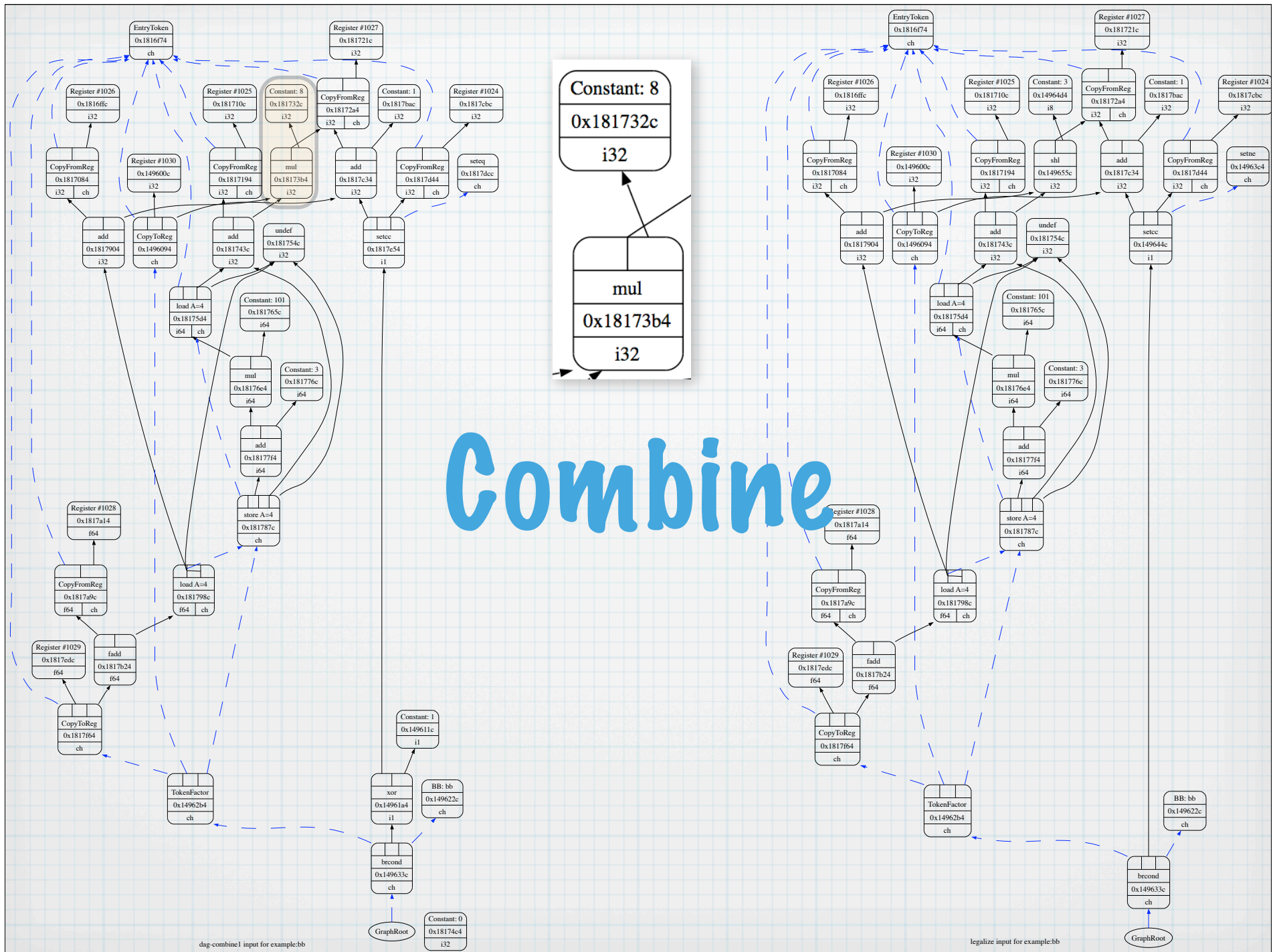
Lower

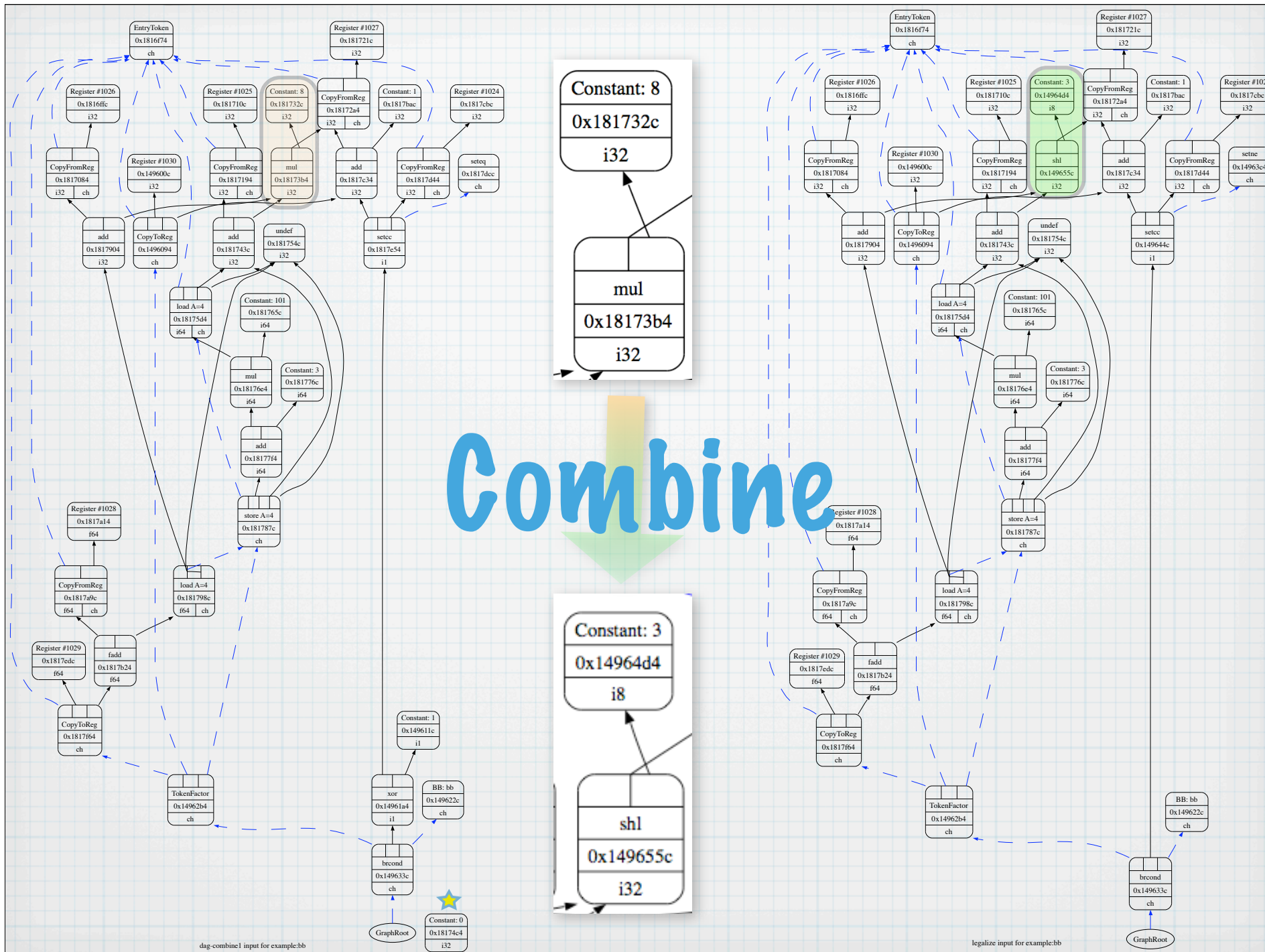


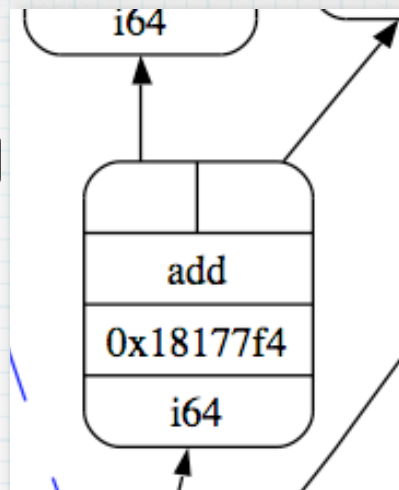




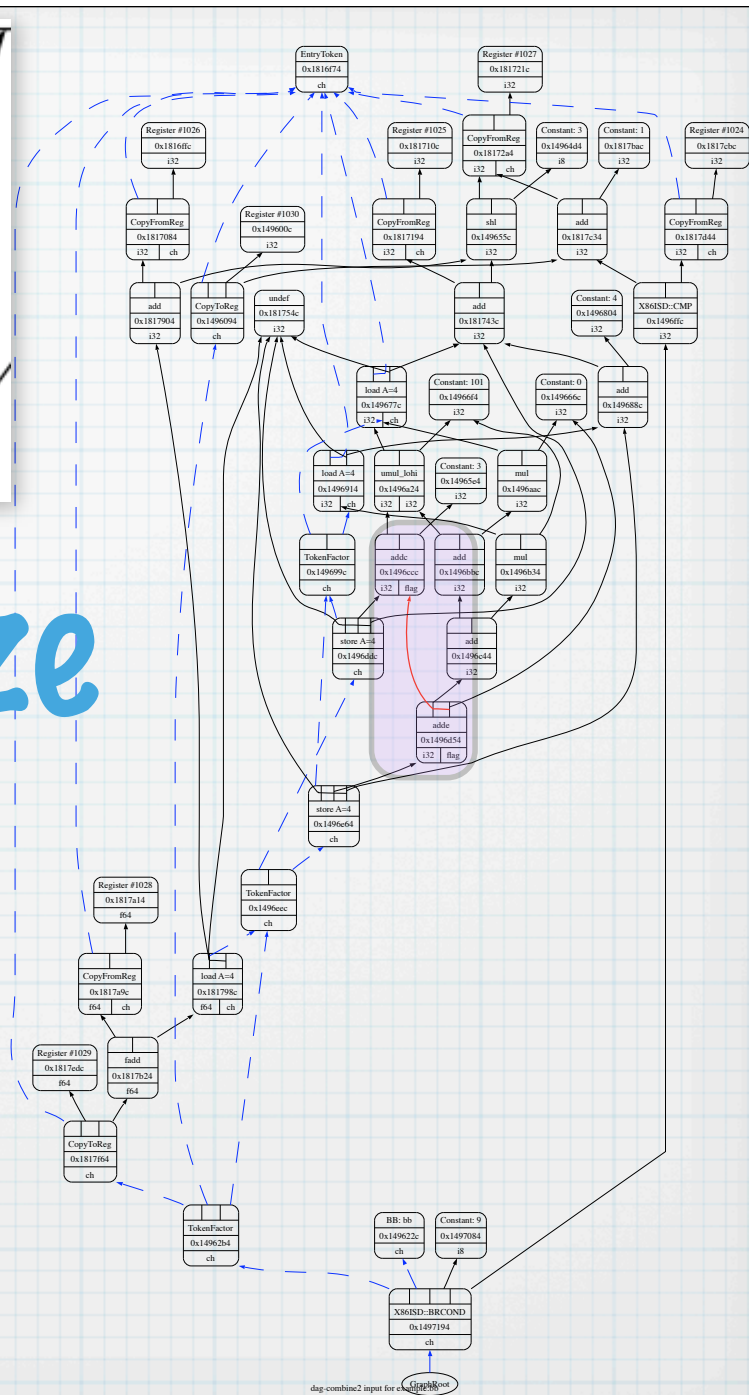
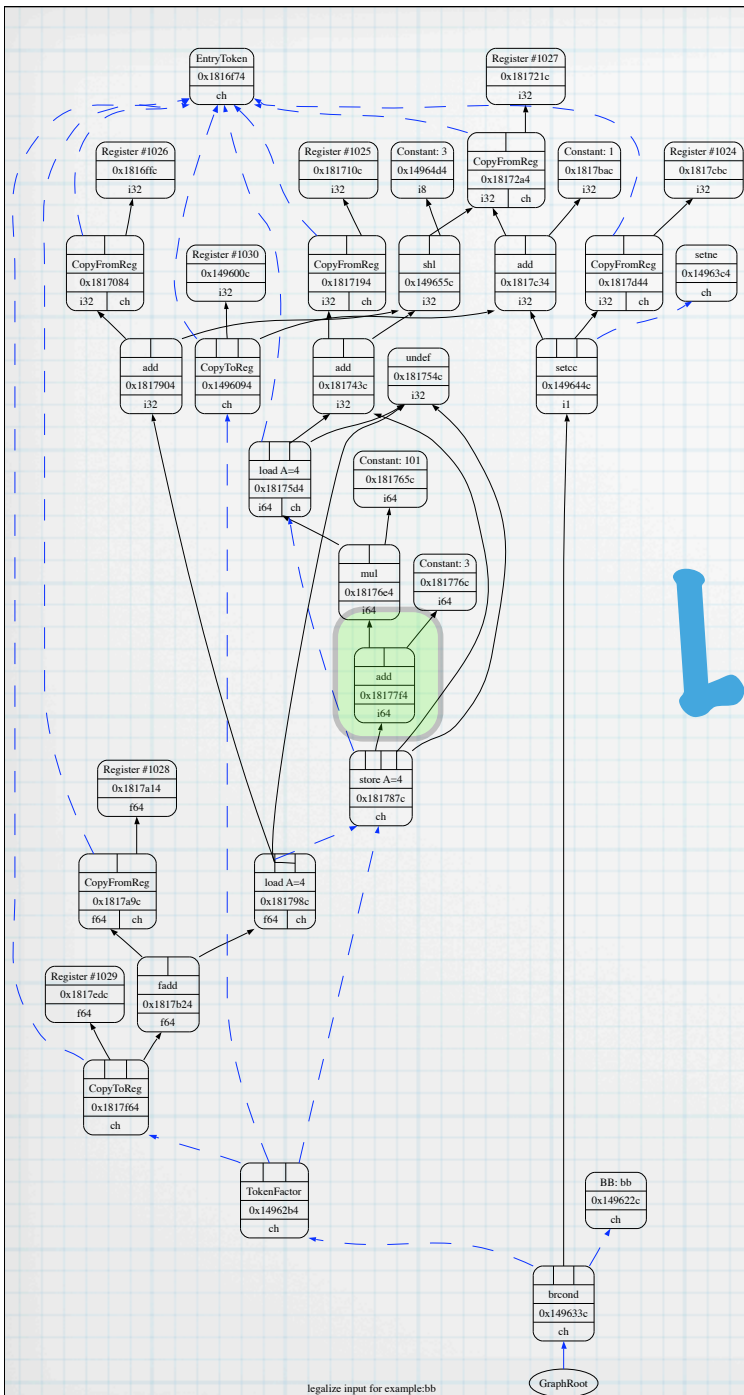
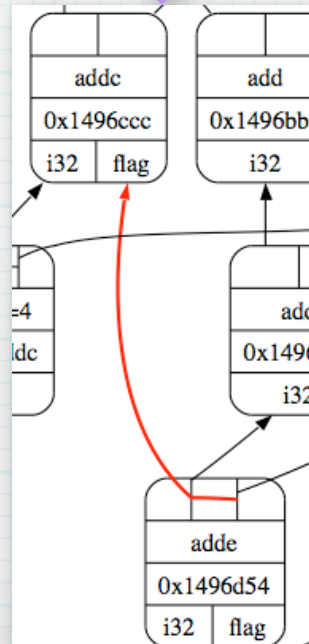


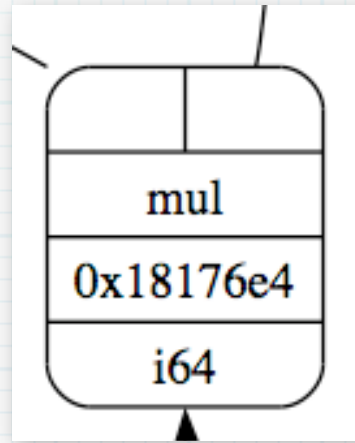




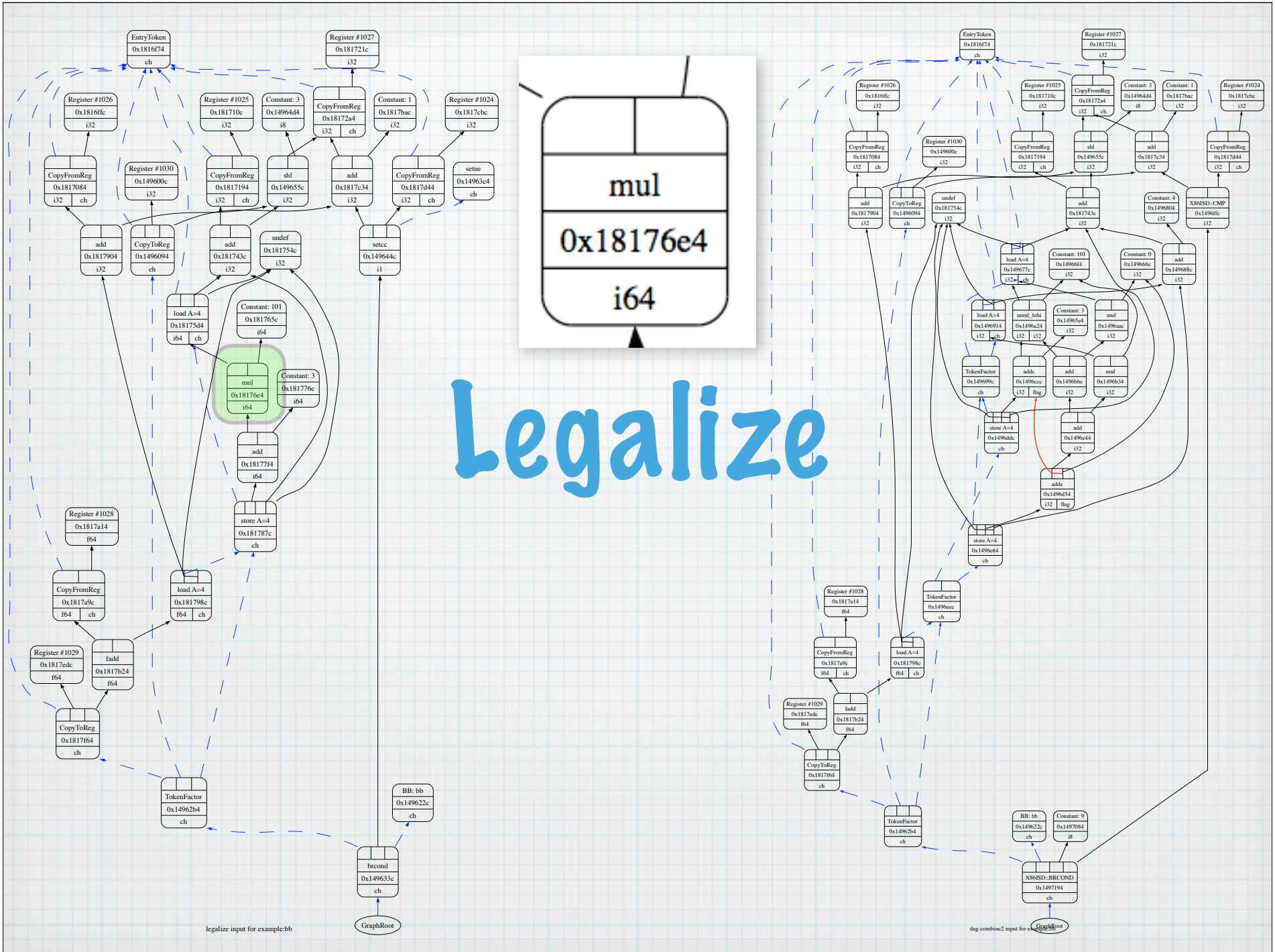


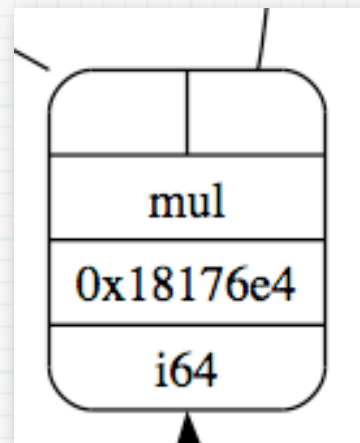
Legalize



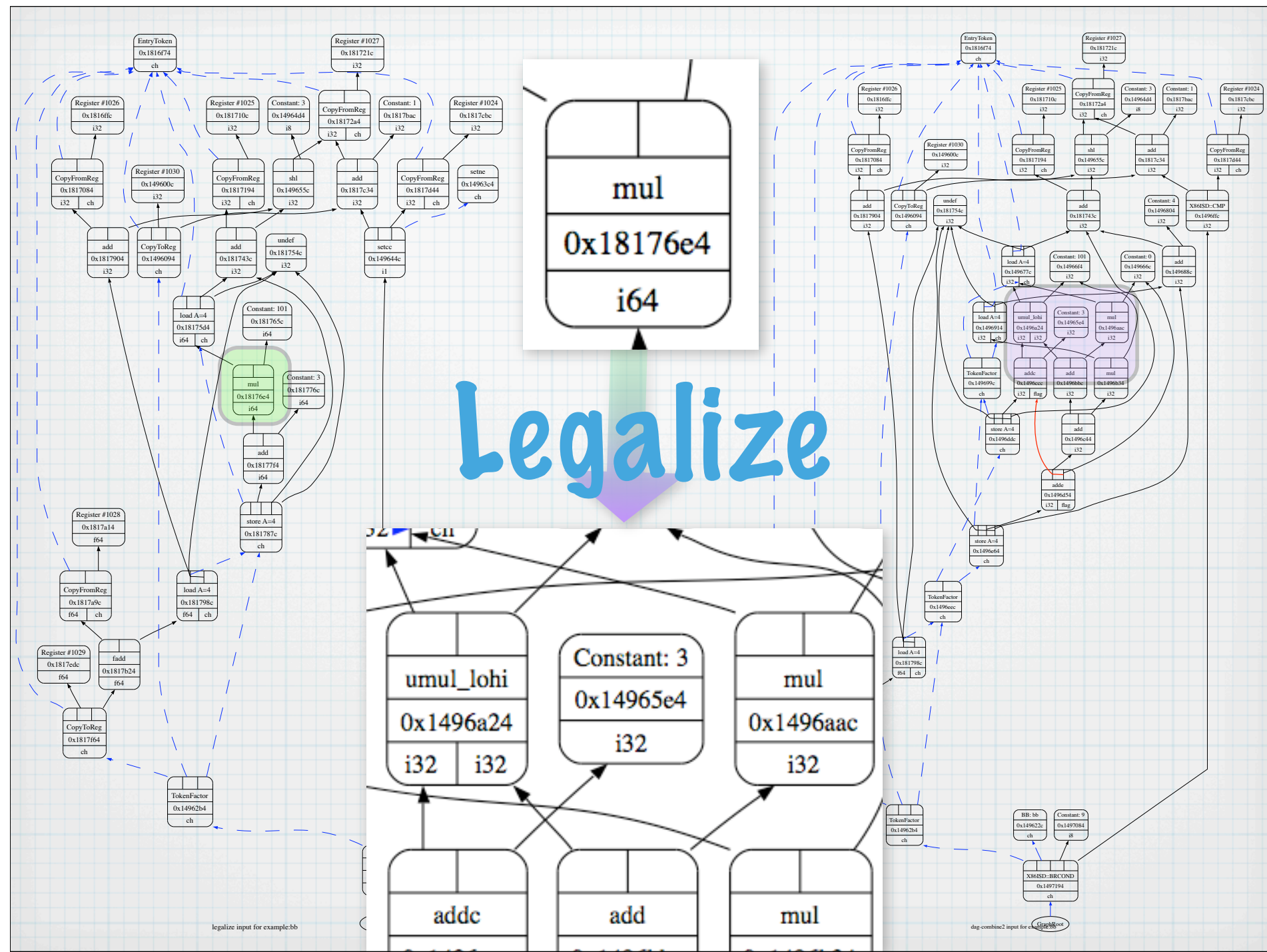


Legalize



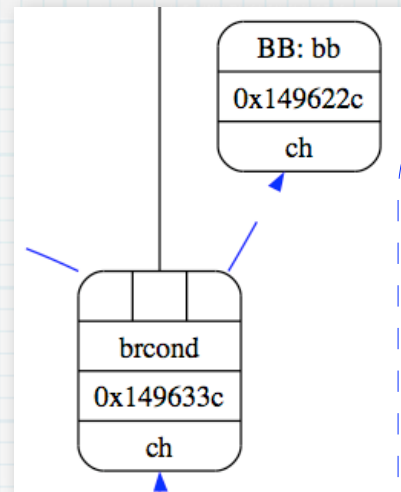


Legalize

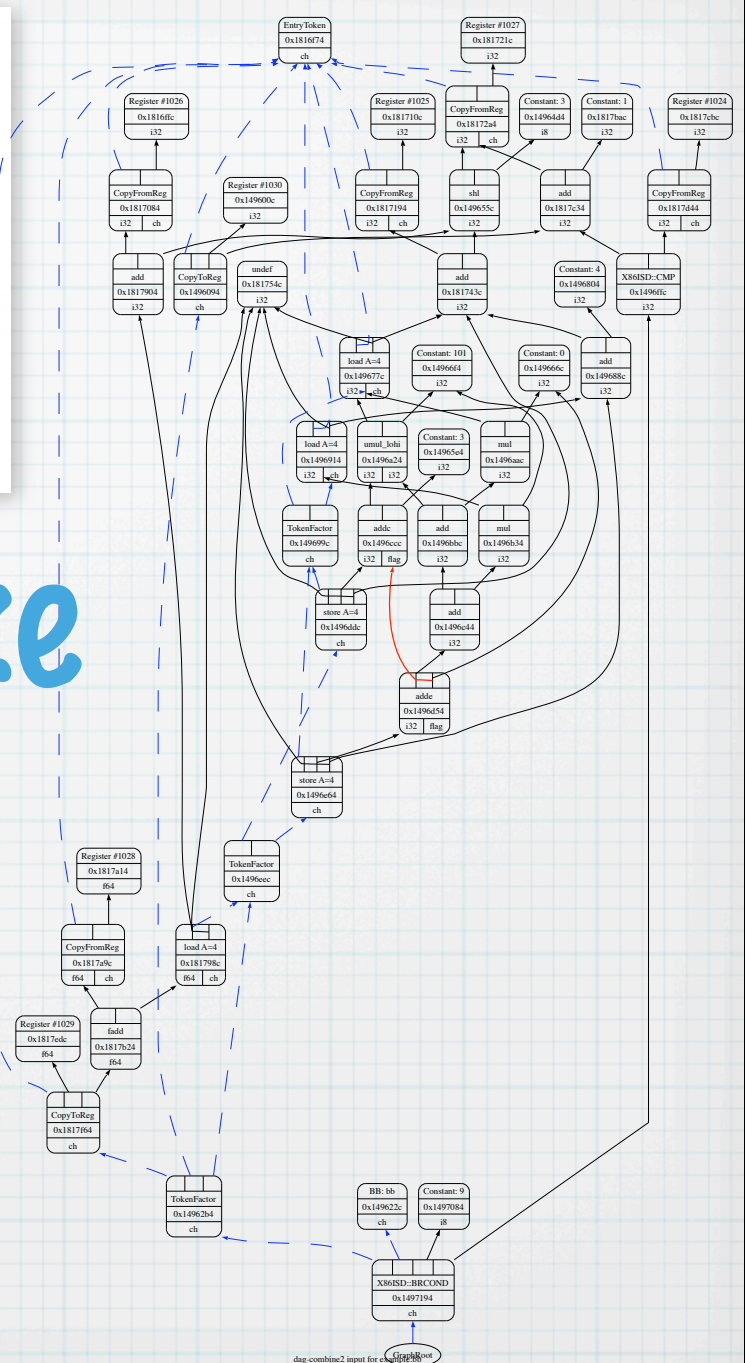
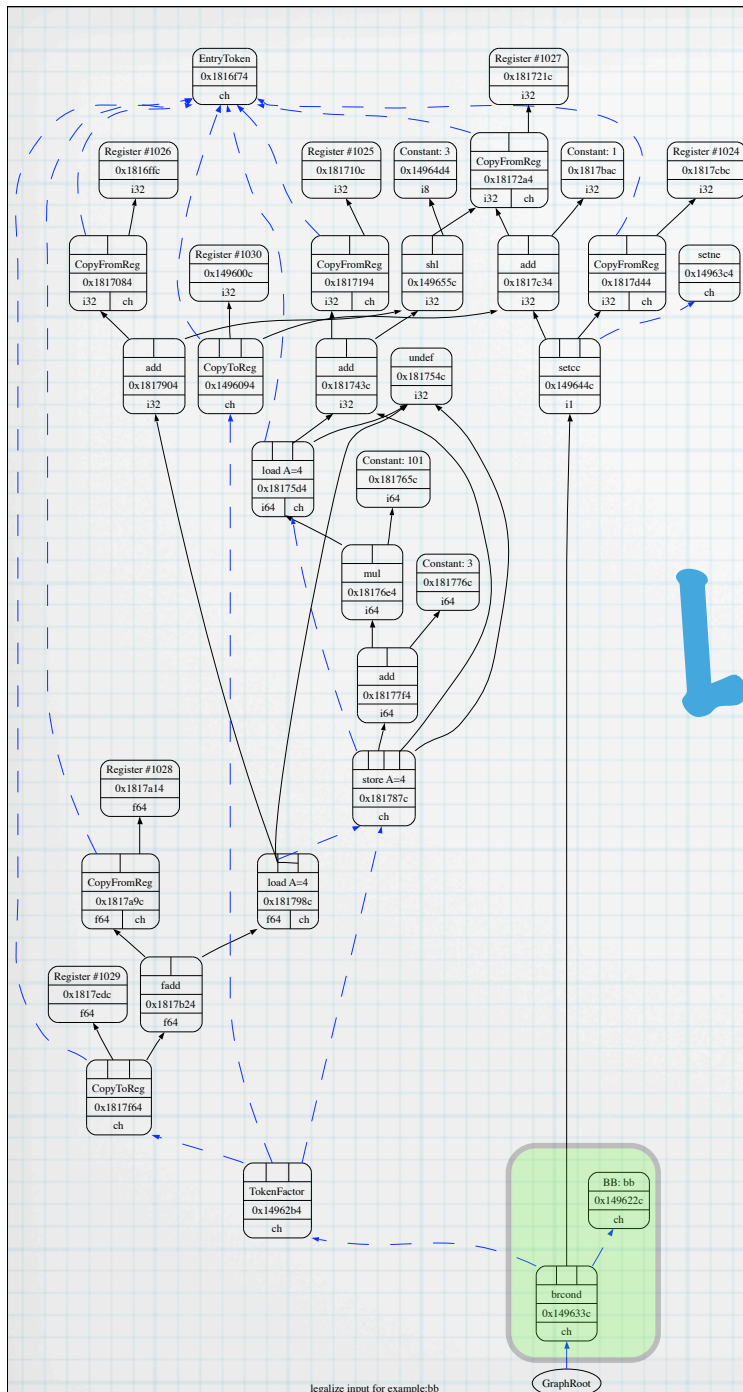


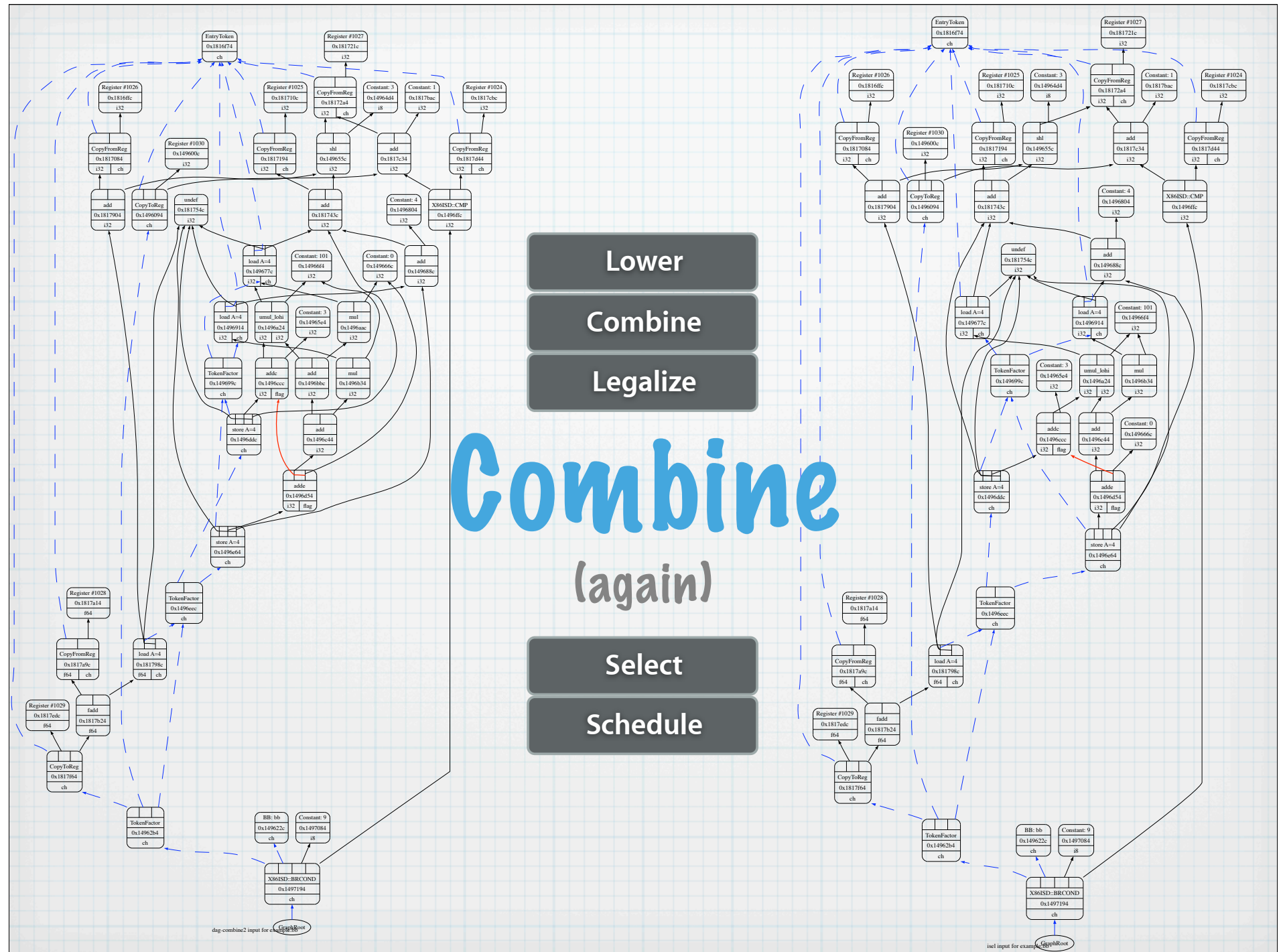
legalize input for example.bb

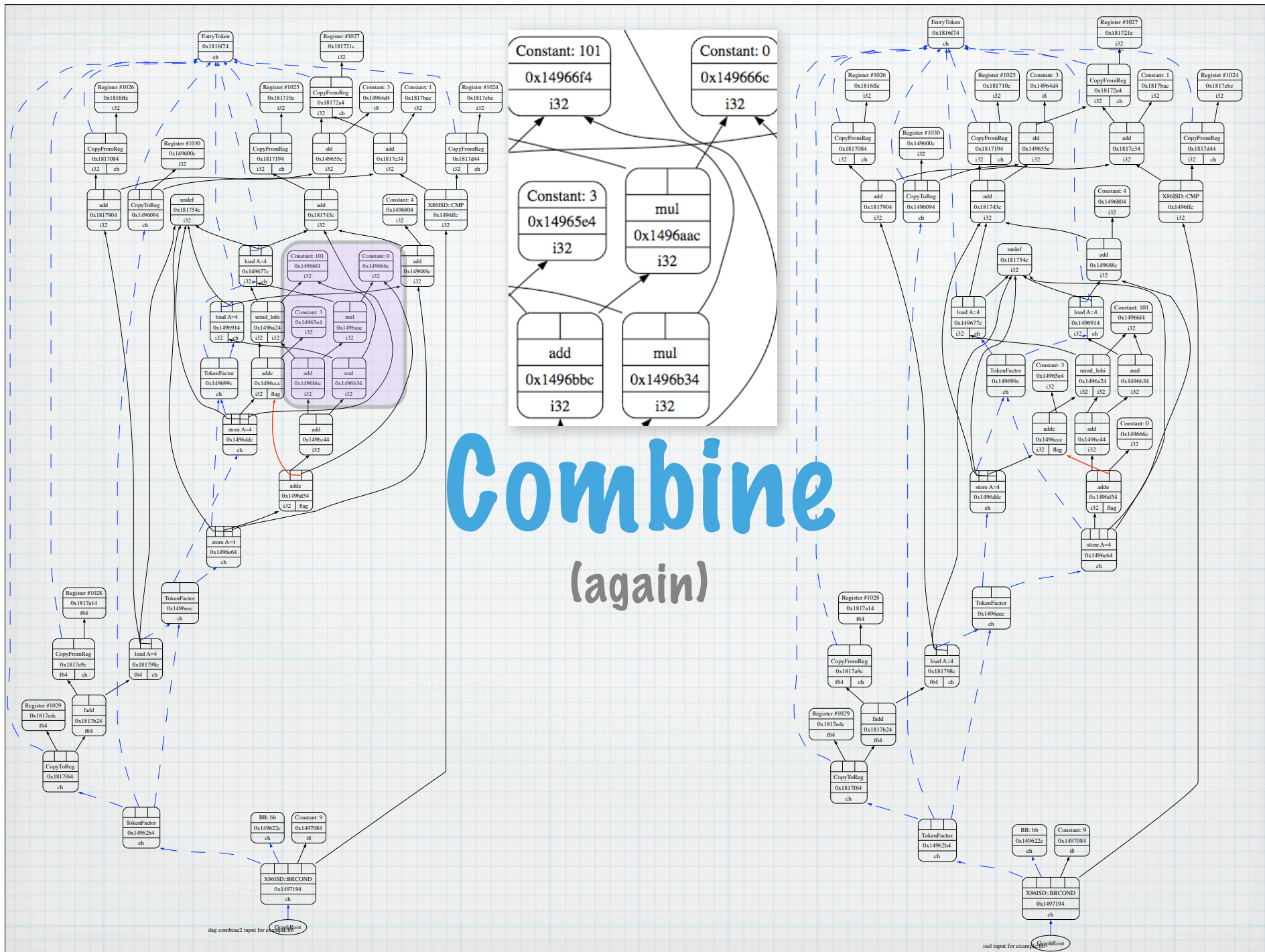
dag-combine2 input for example.bb

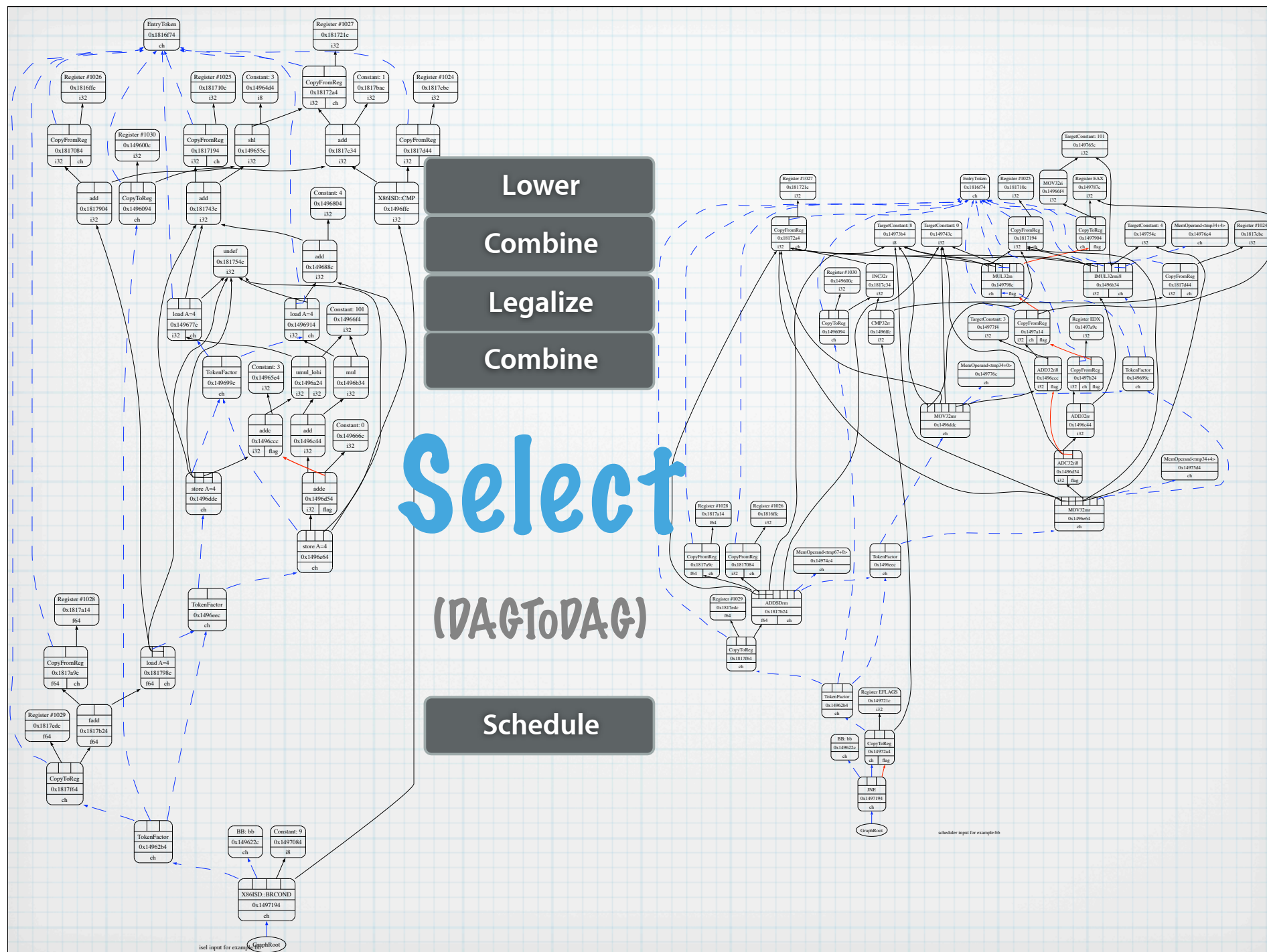


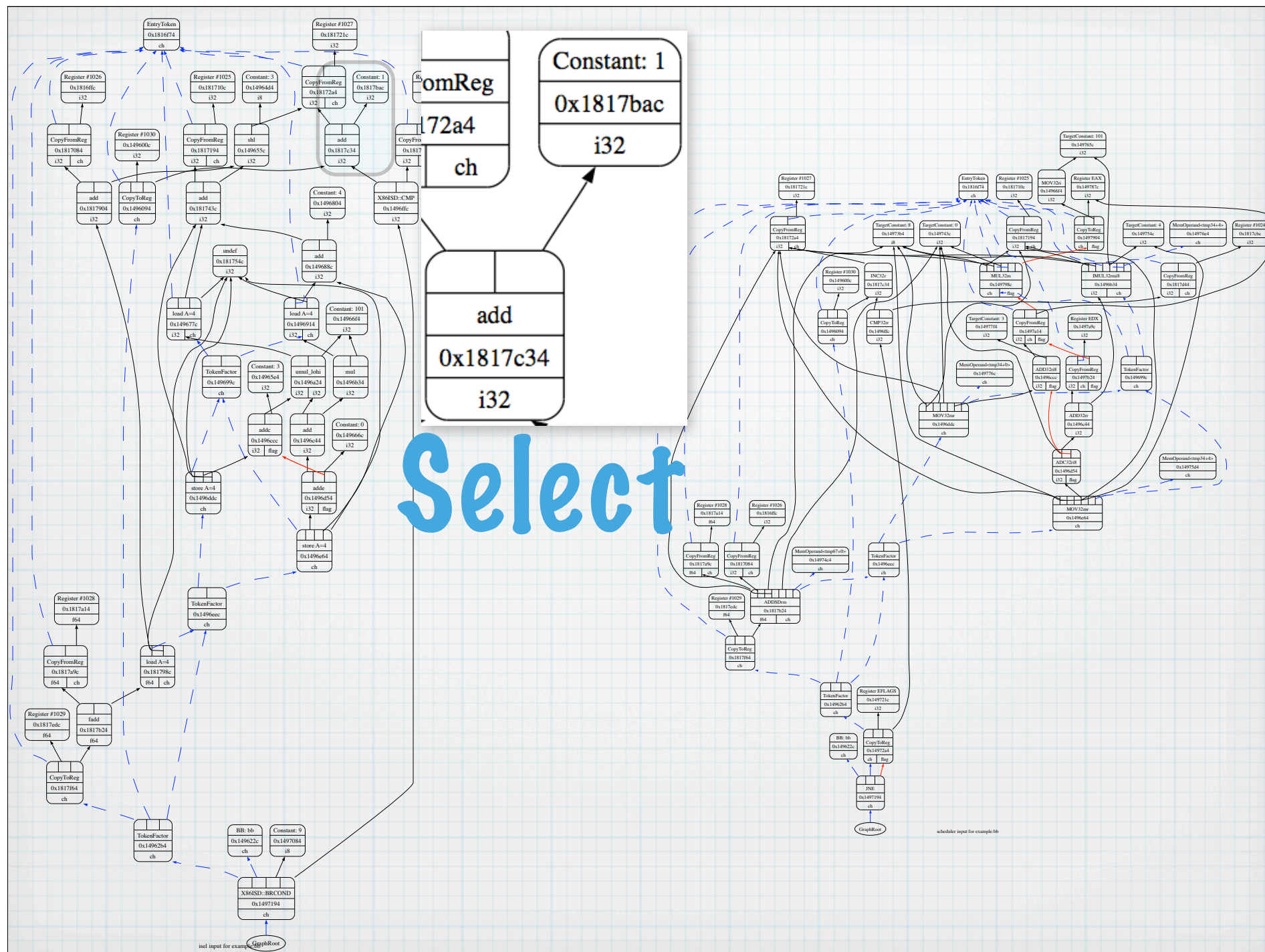
Legalize

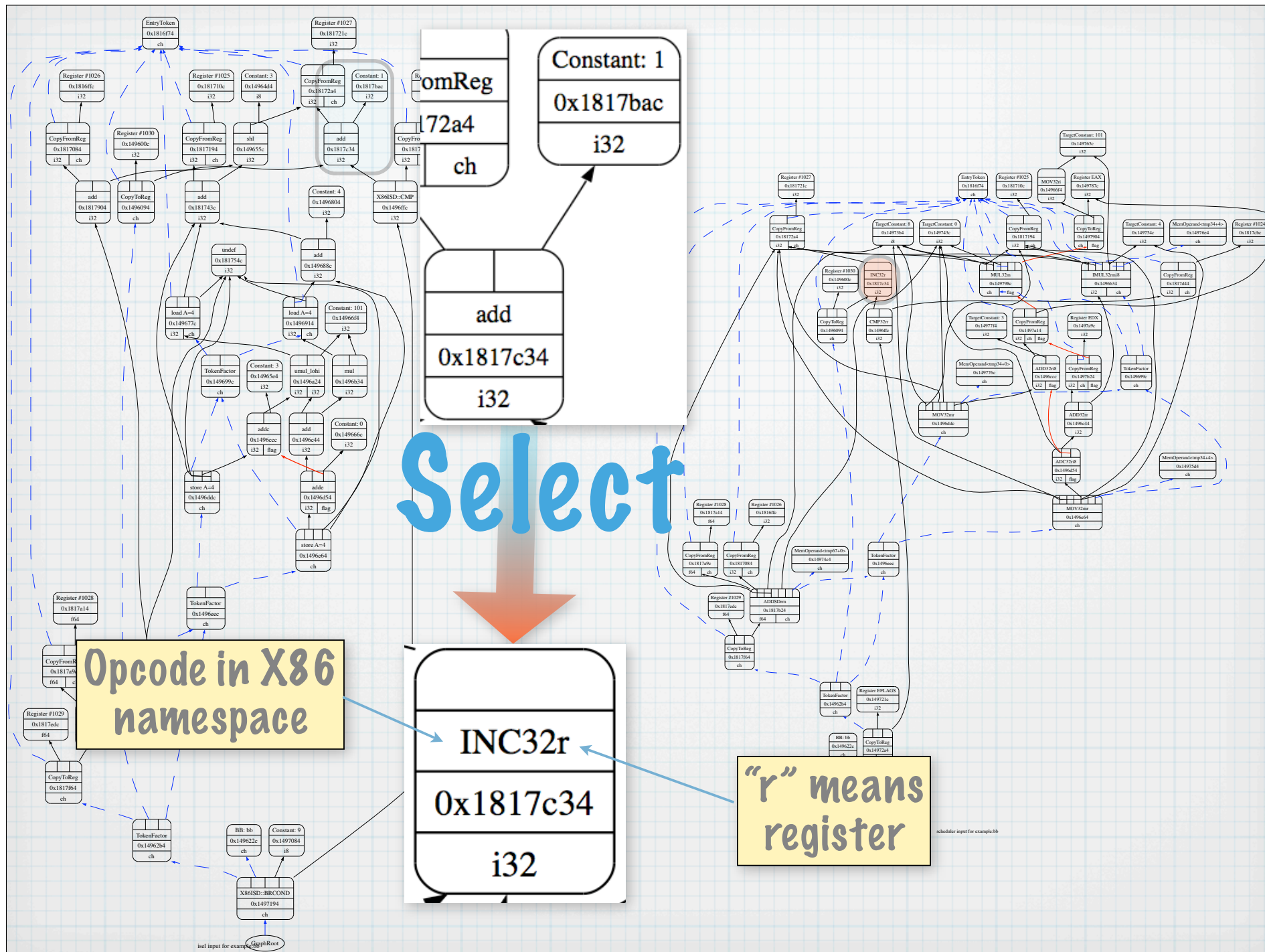


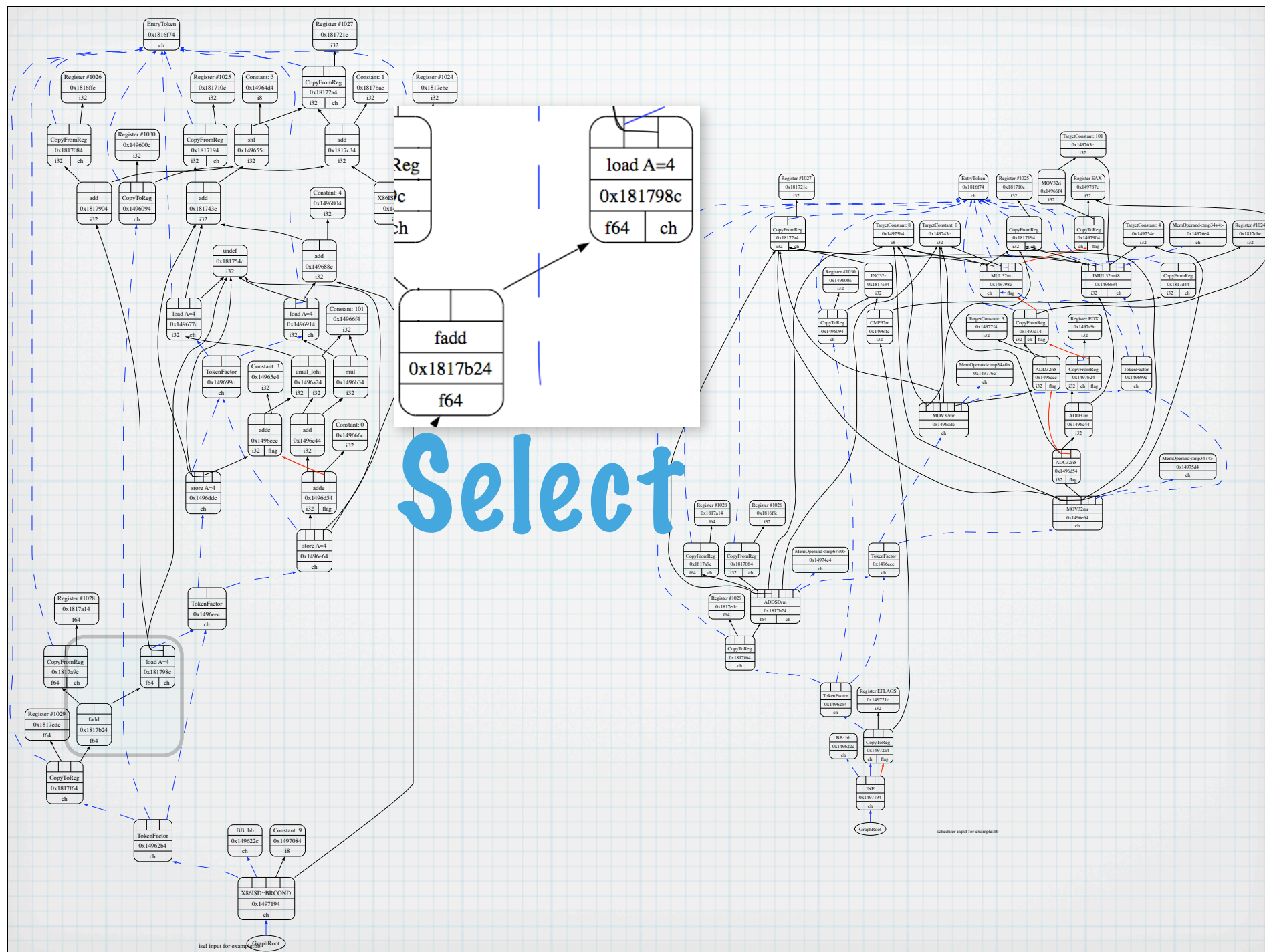


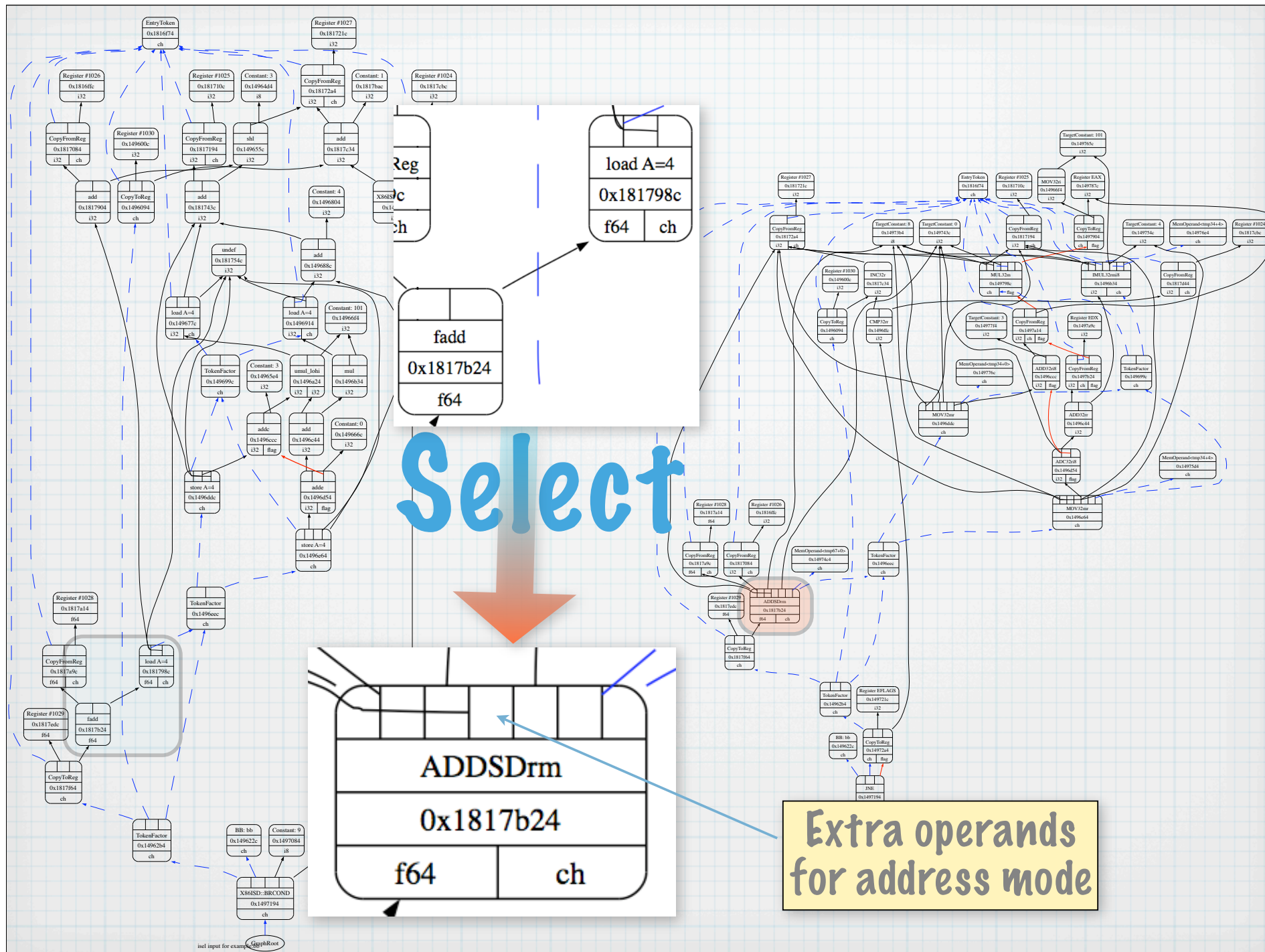












Instruction Patterns

```
def ADDI :  
    DForm_2<14,  
        (outs GPRC:$rD),  
        (ins GPRC:$rA, s16imm:$imm),  
        "addi $rD, $rA, $imm",  
        IntGeneral,  
        [(set GPRC:$rD,  
            (add GPRC:$rA,  
                immSExt16:$imm)) ]>;
```


Instruction Patterns

```
def ADDI :  
    DForm_2<14,  
        (outs GPRC:$rD),  
        (ins GPRC:$rA, s16imm:$imm),  
        "addi $rD, $rA, $imm",  
        IntGeneral,  
        [(set GPRC:$rD,  
            (add GPRC:$rA,  
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```

Instruction Patterns

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def ADDI :  
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        (ins GPRC:$rA, s16imm:$imm),  
        "addi $rD, $rA, $imm",  
        IntGeneral,  
        [(set GPRC:$rD,  
            (add GPRC:$rA,  
                immSExt16:$imm)) ]>;
```

Instruction Patterns

```
def ADDI :  
    DForm_2<14,  
        (outs GPRC:$rD),  
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        "addi $rD, $rA, $imm",  
        IntGeneral,  
        [ (set GPRC:$rD,  
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                immSExt16:$imm) ) ]>;
```

Instruction Patterns

```
def ADDI :  
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```


Instruction Patterns

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        (outs GPRC:$rD),  
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```

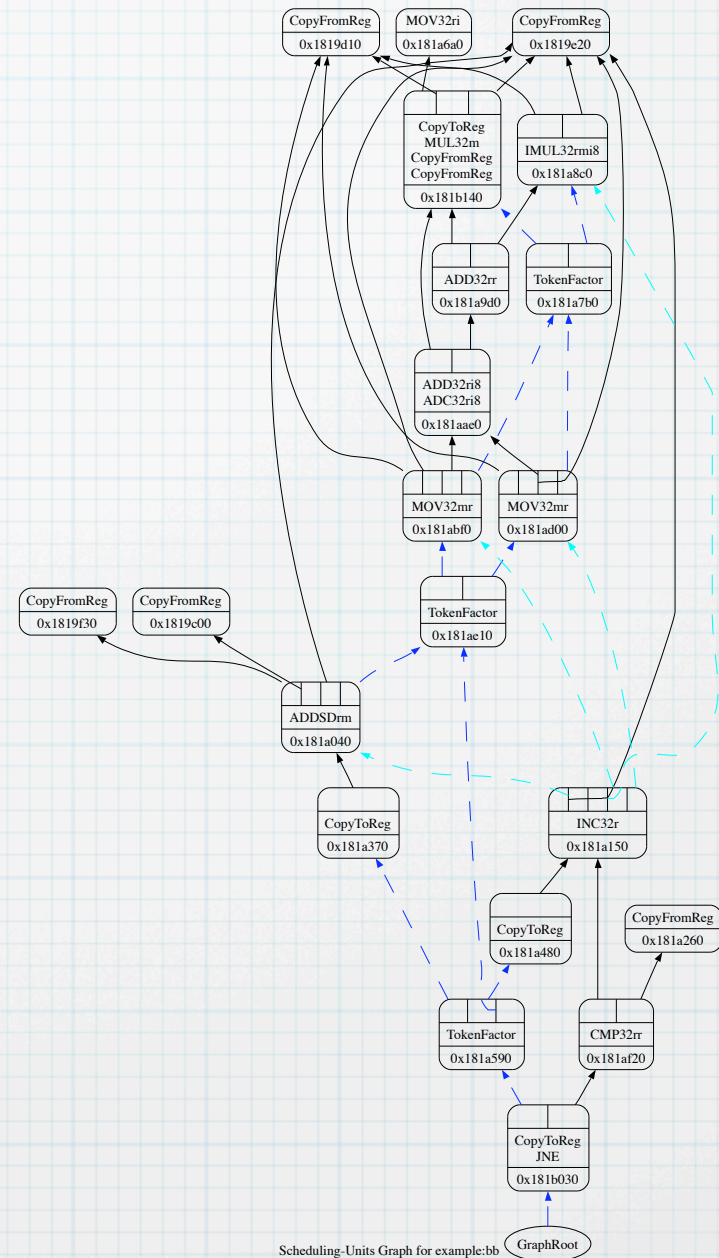
Instruction Patterns

```
def ADDI :  
    DForm_2<14,  
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        "addi $rD, $rA, $imm",  
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        [ (set GPRC:$rD,  
            (add GPRC:$rA,  
                immSExt16:$imm) ) ]>;
```

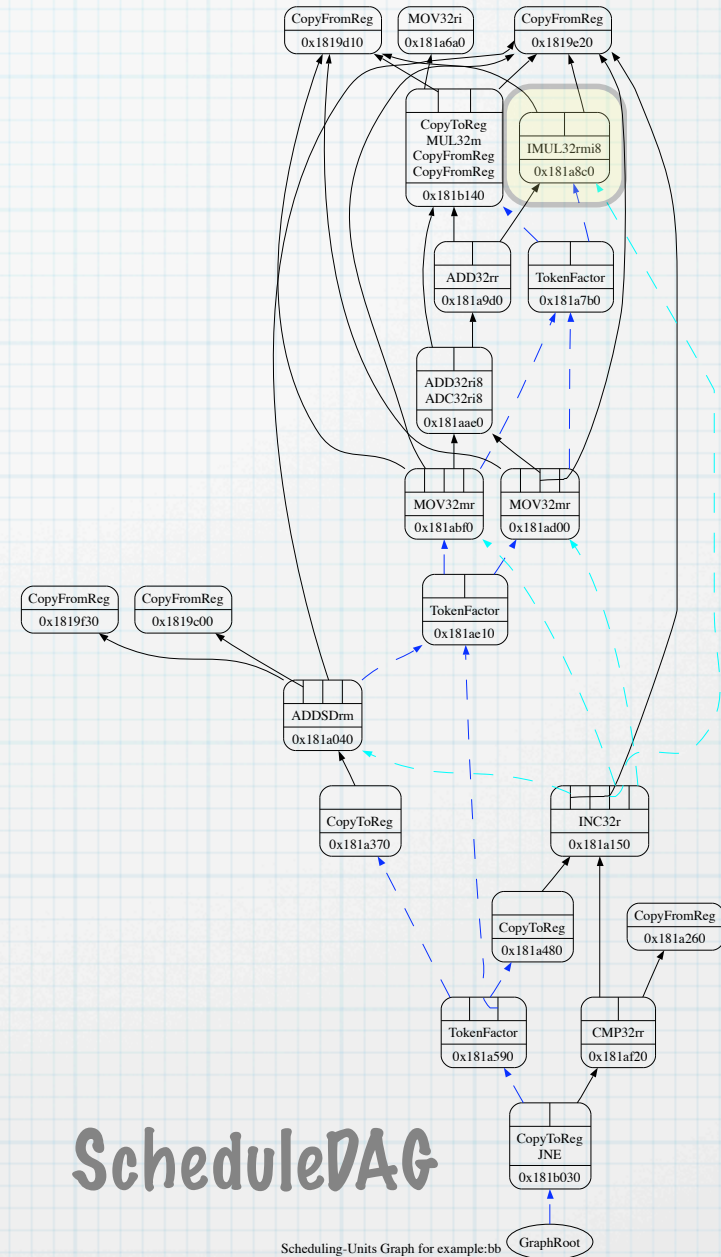
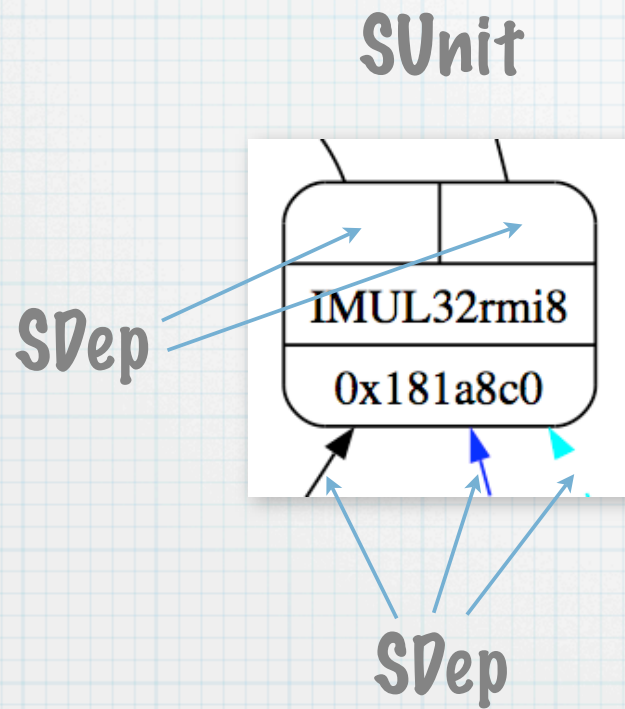
Instruction Patterns

```
def ADDI :  
    DForm_2<14,  
        (outs GPRC:$rD),  
        (ins GPRC:$rA, s16imm:$imm),  
        "addi $rD, $rA, $imm",  
        IntGeneral,  
        [ (set GPRC:$rD,  
            (add GPRC:$rA,  
                immSExt16:$imm) ) ]>;
```

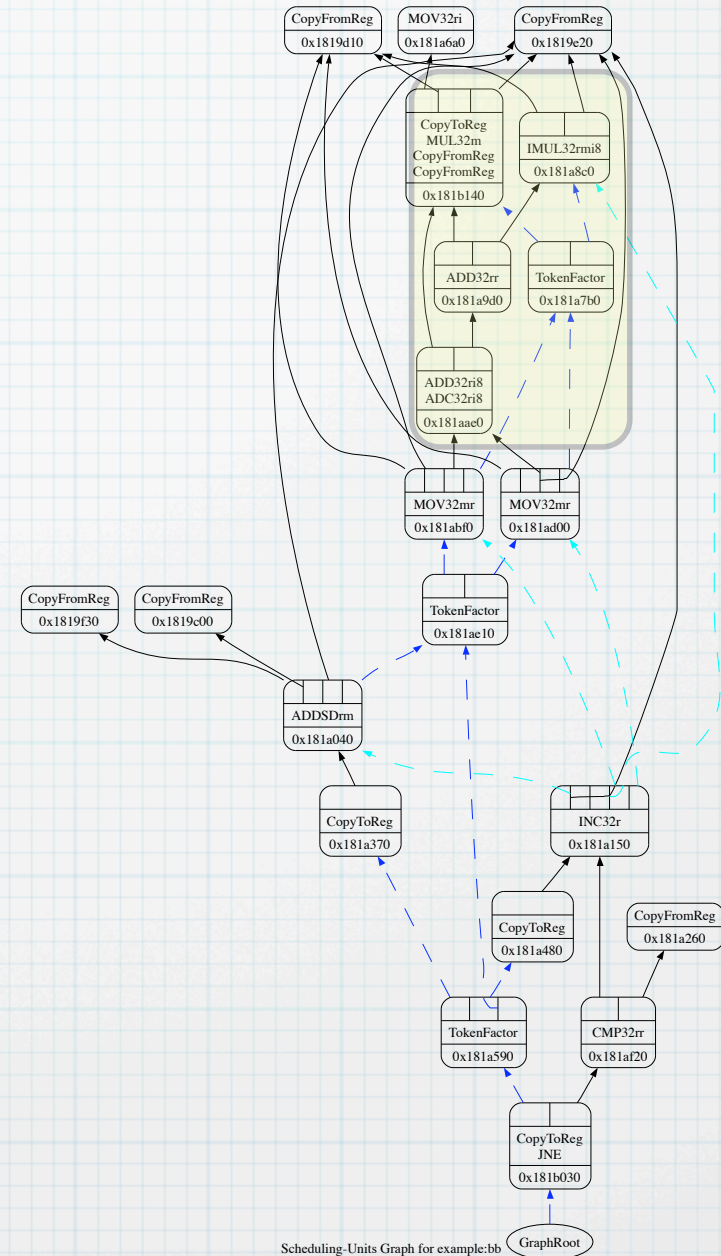
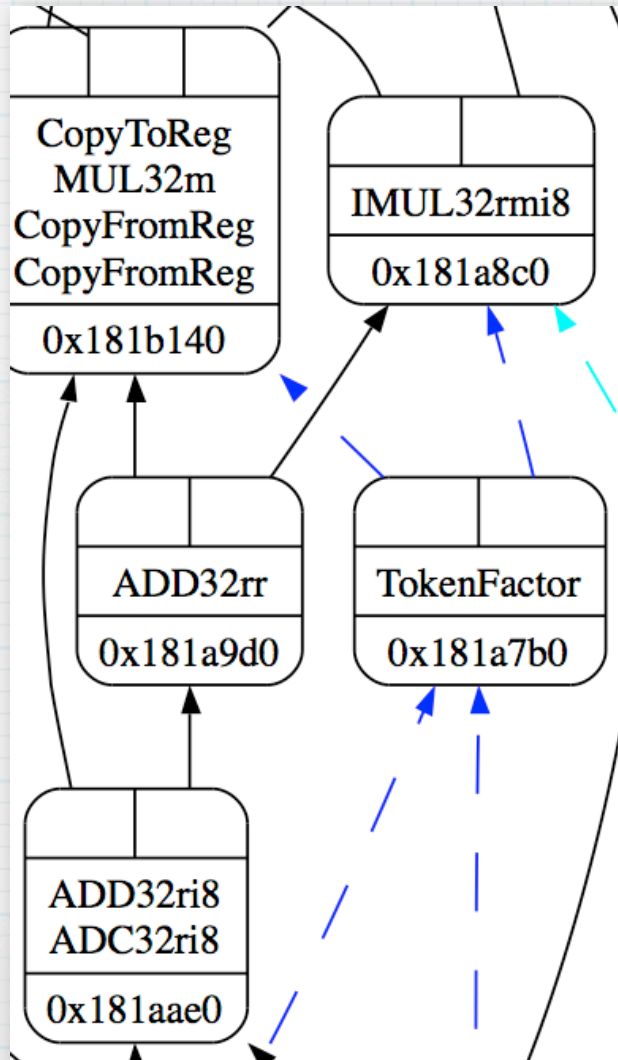
Schedule



Schedule

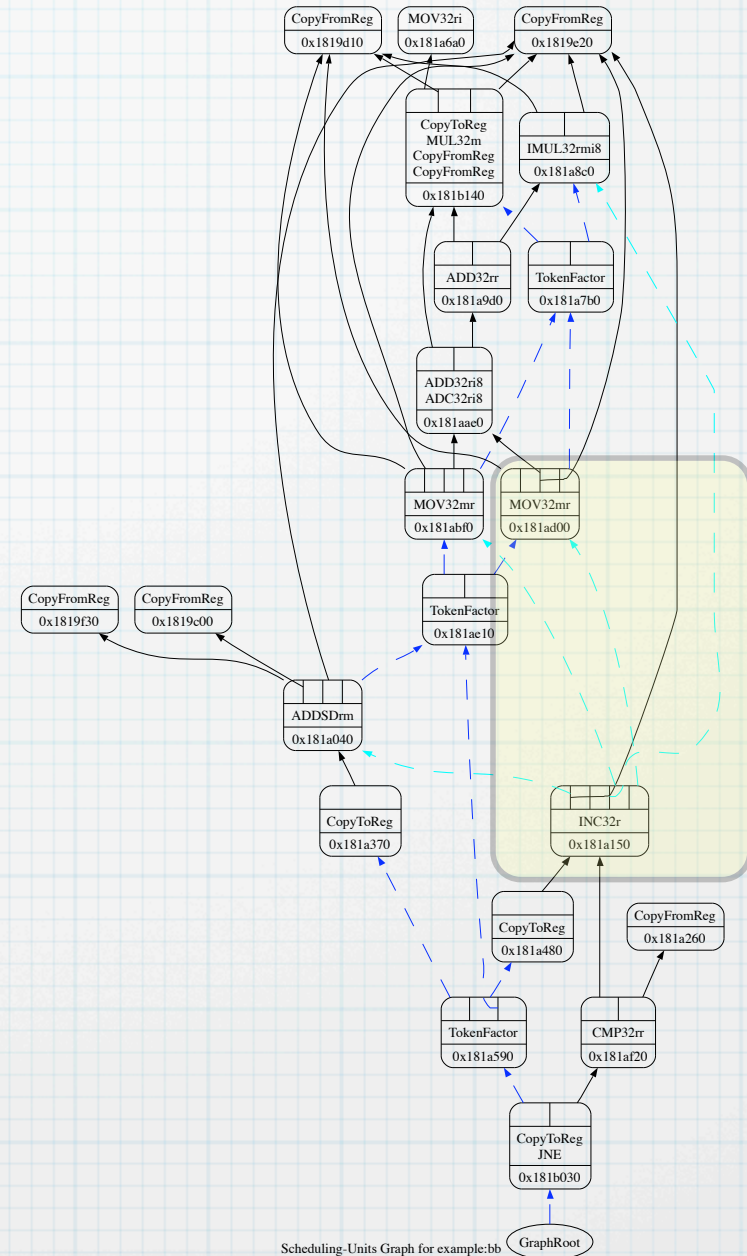
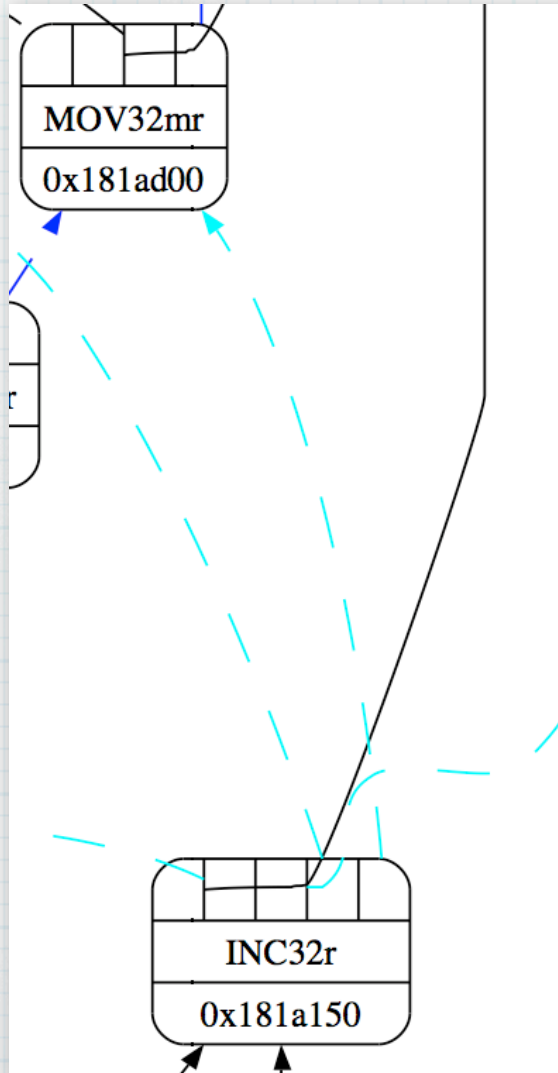


Schedule



Scheduling-Units Graph for example:bb

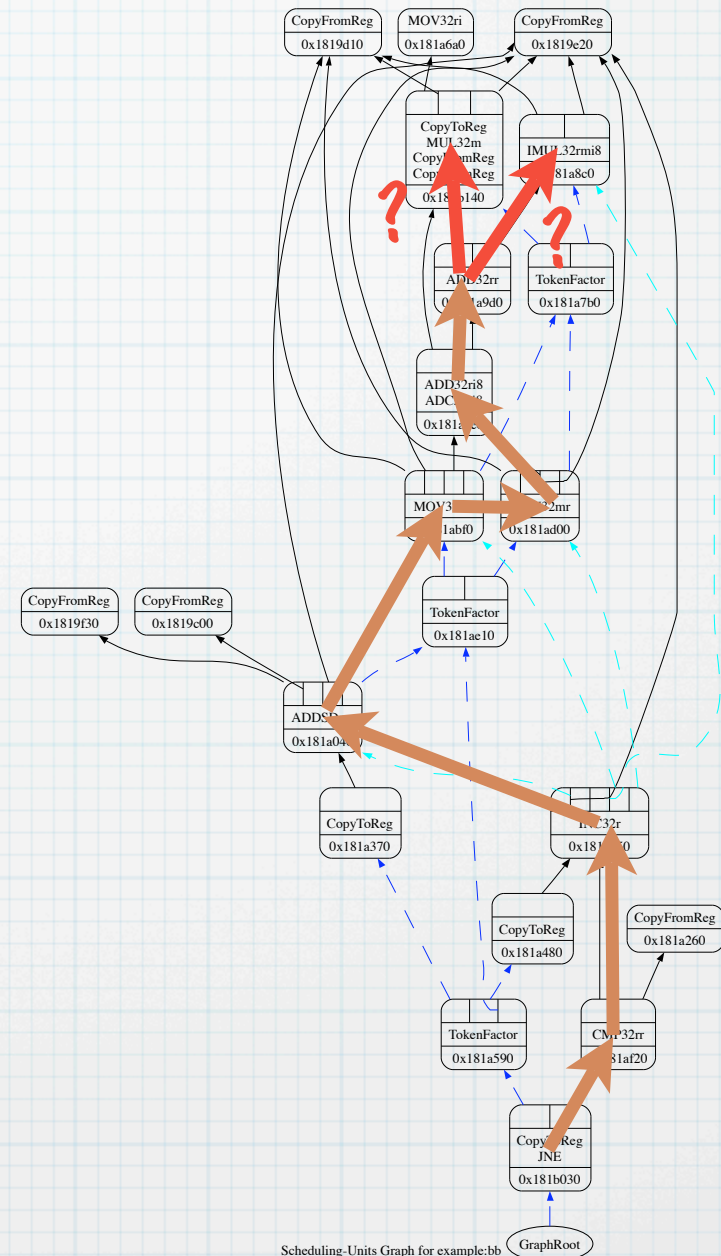
Schedule



Scheduling-Units Graph for example:bb

Schedule

- * Topological Sort
- * Schedule for register pressure
- * Schedule for latency
- * Preserve physical register dependencies



Scheduling-Units Graph for example:bb

Schedule

Output: A sequence of MachineInstrs

```
%reg1027 = PHI %reg1033, mbb<entry,0x1811988>, %reg1030, mbb<bb,0x18119f8>
%reg1028 = PHI %reg1034, mbb<entry,0x1811988>, %reg1029, mbb<bb,0x18119f8>
%reg1035 = MOV32ri 101
%EAX = MOV32rr %reg1035
MUL32m %reg1025, 8, %reg1027, 0, %EAX, %EDX, %EFLAGS, %EAX
%reg1036 = MOV32rr %EAX
%reg1037 = MOV32rr %EDX
%reg1038 = IMUL32rmi8 %reg1025, 8, %reg1027, 4, 101, %EFLAGS, Mem:LD(4,4)[t7+4]
%reg1039 = ADD32rr %reg1038, %reg1037, %EFLAGS
...
```

SelectionDAG Future

- * LegalizeTypes
- * SEME regions, whole-functions
- * More precise dependencies
- * Fast -O0 isel?
- * BURG-style isel?

CodeGen continues...

- * Late Code Motion
- * Register Allocation
- * Output

Questions?