1[a] Draw the block digram for the hardware implementation of digital serial, bit parallel BCD subtraction.

[b] Design a hardware circuit to implement logical shift, arithmetic shift and circular shift operations. State your design specifications.

2[a] What is difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

[b] Explain in brief how a digital computer system works in a interrupt driven input-output programming.

3[a] Give the flow table for register contents used in implementing booth's algorithm for the multiplier = - 6 and multiplicant = + 5.

[b] Give the flow chart of division of two signed magnitude data. Discuss the logic of the flow chart.

4[a] Define addressing mode. With the help of example explain different addressing modes.

[b] Explain stack organisation used in processors. Differentiate between a register stack and a memory stack.

5[a] Explain DMA based data transfer. Give the respective block diagram.

[b] Explain in brief with the help of a diagram the working of daisy chaining with multiple priority levels and multiple devices in each level.

6 [a] Show the memory organization (1024 bytes) of a computer with four 128x8 RAM Chips and 512x8 ROM Chip. How many address lines are required to access memory.

[b] Explain in detail the different mappings used for cache memory. Compare them.

7 Write short notes:-

[a] CISC and RISC architectures.

[b] First Pass in assembly language.

[c] Status Register.

[d] Micro Program Controller.