Assignment 2
Analog Electronics (EC-261)

Max. Marks: 10

Note: All questions are compulsory.

Q.1 The amplifier of Fig. 1 utilizes an n-channel JFET for which V_p= -2.0 V, I_{DSS} =1.65 mA. It is desired to bias the circuit at I_D =0.8 mA, using V_{DD} = 24 V. Assume r_d >> R_D. Find (a) V_{GS} (b) g_m (c) R_s and (d) R_d, such that voltage gain at least 20 db, with R_S bypassed with a very large capacitance C_s.

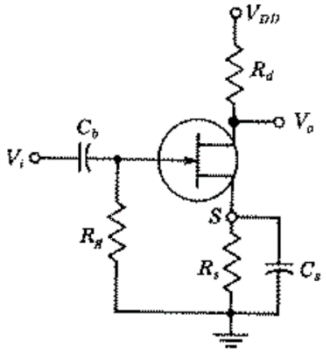

Fig. 1

Q.2 For the network of Fig. 2:
(a) Determine A_{vNL}, Z_i, and Z_o.
(b) Determine A_v and A_{vs}.
(c) Change R_L to 4.7 kΩ and calculate A_v and A_{vs}. What was the effect of increasing levels of R_L on both voltage gains?
(d) Change R_{sig} to 1 kΩ (with R_L at 2.2 kΩ) and calculate A_v and A_{vs}. What was the effect of increasing levels of R_{sig} on both voltage gains?
(e) Change R_L to 4.7 k Ω and R_{sig} to 1 k Ω and calculate Z_i and Z_o. What was the effect on both parameters?

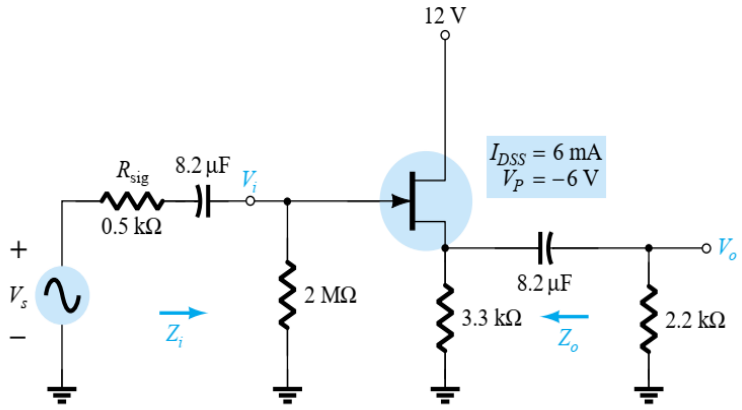

Fig. 2

Q.3 The self-bias configuration has an operating point defined by V_{GSQ} = -2.6 V and I_{DQ} = 2.6 mA, with I_{DSS} = 8 mA and V_P =- 6 V. The network is redrawn as Fig. 3 with an applied signal V_i. The value of y_{os} is given as 20 S.

(a) Determine g_m, r_d, Z_i.

(b) Calculate Z_O with and without the effects of r_d. Compare the results.

(c) Calculate A_V with and without the effects of r_d. Compare the results.

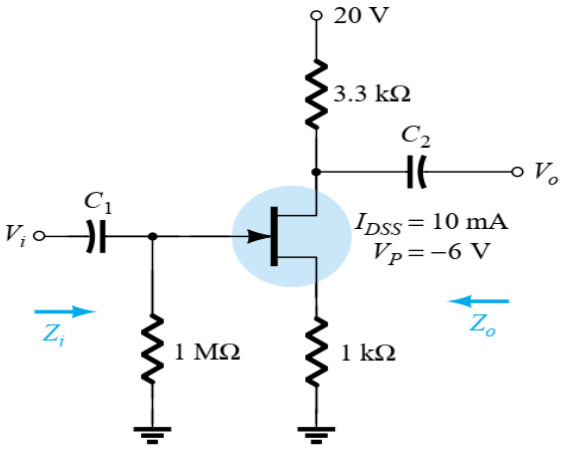

Fig. 3

Q.4 Determine the following for the network of Fig. 4.

(a) I_{DQ} and V_{GSQ}

(b) V_{DS}

(c) V_D

(d)V_S

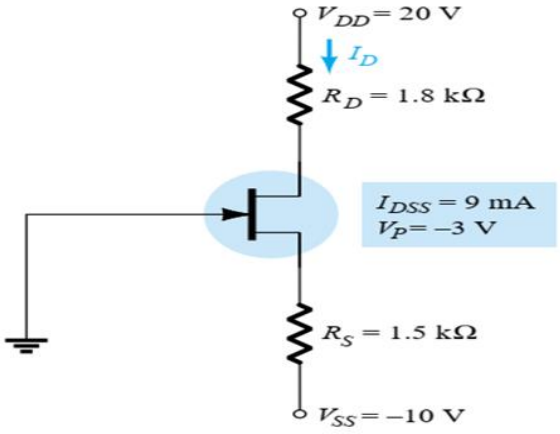

Fig. 4