Total No. of Pages 01 *Roll No. .....*

Forth SEMESTER B.Tech(ECE)

SUPPLEMETARY EXAMINATION SEPT-2019

EC262 DIGITAL ELECTRONICS

TIME: 03 Hrs MaximumMarks:40

Note: Attempt any five questions. Assume suitable missing data if any.

1.(a) Convert the given expression in to SOP form using Boolean laws 4

(i) $(X+YZ)(\bar{X}+Y)(Y+Z)$

(ii) $(\bar{A}+\bar{C})(A+\bar{B}+C)$

(b) Simplify the followings by using of Boolean algebra 4

(i) $A\bar{C}D + \bar{A}\bar{B}D + BC\bar{D} + A\bar{B} + AB\bar{C}$

(ii) $f = \pi M(1,3,5,7,10,13,14)$

2. (a)Simplify the following Boolean function using K-map technique 4

$F(A,B,C,D,E) = \pi M(0,4,7,8,9,10,11,16,24,25,26,27,29,31)$

(b) Using the tabular method, Simplify the Boolean expression 4

$F(A,B,C,D,E) = \Sigma m(1,4,7,9,10,12,15) + \Sigma\, d(6,8,13)$.

3.(a) Design a four bit gray to Binary converter . 4

(b)Implement a binary full subtractor logic using suitable size Multiplexer and Decoder. 4

4.(a) Design a 5-4-2-1 to Ex-3 BCD code converter. 4

(b) Implement the following Boolean function using PLA

$f_1(A,B,C,D) = \Sigma M(0,2,6,9,10,12,13)$

$f_2(A,B,C,D) = \Sigma M(1,3;5,8,10,14)$ 4

5.(a) Discuss the followings:

(i) Locking of states in counter

(ii) Resolution of DAC 4

Locking states in a counter typically refers to preventing further changes to the counter's value once a desired state has been reached.

(b) With neat block diagram discuss the working of Successive approximation A/D converter and state its advantages. 4

6. (a) With neat block diagram discuss the working of ECL NOR gate circuit. State the advantage of ECL over TTL logic family. 4

(b) Design a synchronous counter for counting the sequence 0,2,4,6,9,10,12,13 & repeat by using SR-FF. 4