Digital Logic families

A group of compactible ICs with same logic levels & supply voltages for performing various logic functions have been fabricated using a specific circuit configuration is called as logic family.

- Bipolar
- Unipolar
  - PMOS
  - NMOS
  - CMOS

Saturated
Unsaturated
- Schottky TTL
- ECL
- RTL — Register - Transistor Logic
- DCTL — Direct coupled Transistor Logic
- IIL, I^2L — Integrated Injection Logic
- RCTL — Resistor - Capacitor - Transistor Logic
- DTL
- HTL — High Threshold Logic
- TTL
  - ① Standard SN 54/74
  - ② High Speed - SN54H / SN74H
  - ③ Low Power SN54L/74L
  - ④ Schottky diode clamped SN54S/74S
  - ⑤ Low power Schottky SN54LS/SN74LS

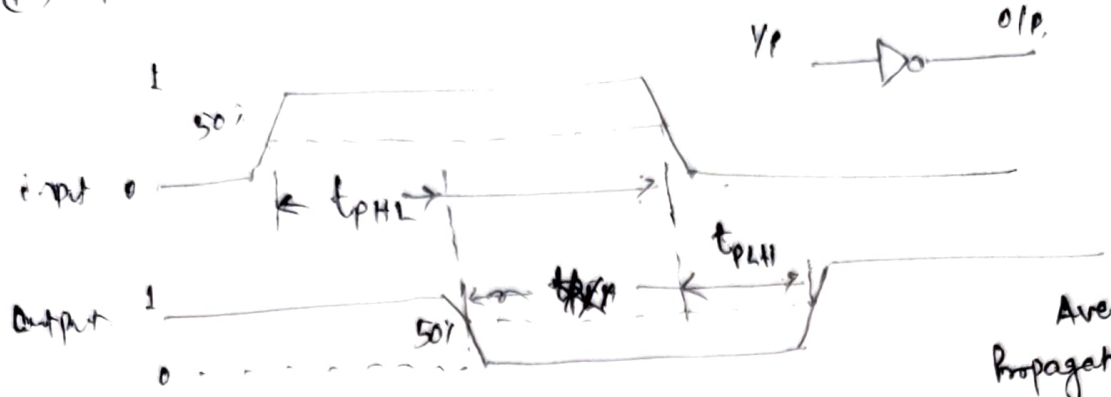
Bi CMOS → Use CMOS for input & Logic operation and Bipolar for output.

Characteristics :-

	No. of Logic Gates	No. of Components / Transistors
SSI —	< 12	< 100
MSI —	12 - 99	100 — 999
LSI —	100 - 999	1000 — 9999
VLSI —	> 1000	> 10,000

(i) Speed of operation
(ii) Power dissipation
(iii) Figure of merit
(iv) Fan-out
(v) Current - voltage Parameter

(vi) Noise immunity
(vii) operating temperature range
(viii) Power supply requirement
(ix) flexibilities available



Average Propagation delay

Propagation delay of Gate = $\frac{t_{pHL} + t_{pLH}}{2}$

Power dissipation: $V_{cc} \times I_{average}$, $I_{average} = \frac{I_{cc}(0) + I_{cc}(1)}{2}$

→ in milli watts (mW)

[average of input Collector current & o/p transistor Collector current]

F.O.M :- P.D (in nanosec) x Power (mW)
(Fig of merit)

ns x mW = Pico Joule

A low value of FOM is desirable.

Speed ↑ ⟶ PD ↑ & vice versa.
(Power dissipation)

fan-out : No of similar gates which can be driven by a gate.
High fanout is advantageous as it reduces the need of additional drivers to drive more gates.

V_{IH} — maximum input voltage recognised by the gate as logic 1.
V_{IL} — " " " " " " 0

V_{oH}
V_{oL}

FAN IN No of inputs that can be connected to the input of a gate without degradation in the output voltage level.

I_{IL} I_{IH}

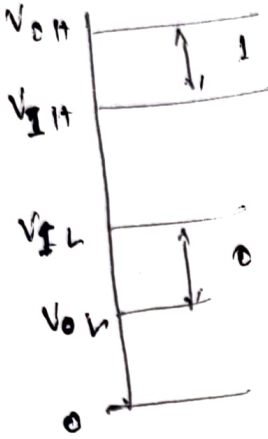
I_{OL} — Max. current gate can sink at 0 Level.

I_{OH} — Maximum current which the gate can sink in 1 level.

Noise immunity

Stray Electric & magnetic field may induce Unwanted voltage in the circuit is called noise (glitch, transients)

A quantitative measure of Noise immunity of a Logic family is called NOISE MARGIN.

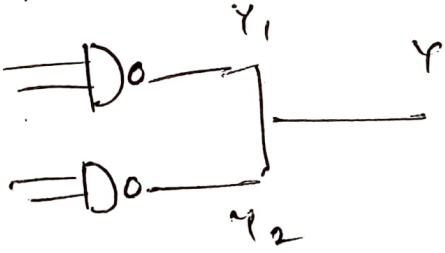


Circuits ability to tolerate noise signals is referred as Noise immunity.

Temperature: $0 \rightarrow +70^{\circ}C$ — Consumer Appliances & Industrial Appl.

$-55^{\circ}C \rightarrow 125^{\circ}C$ — Military Applications

wired Logic -



without additional gate

TTL

Supply voltage - 5 V.

Logic 0 o/p → 0 to 0.4 V

Logic 1 o/p - 2.4 to 5 V.

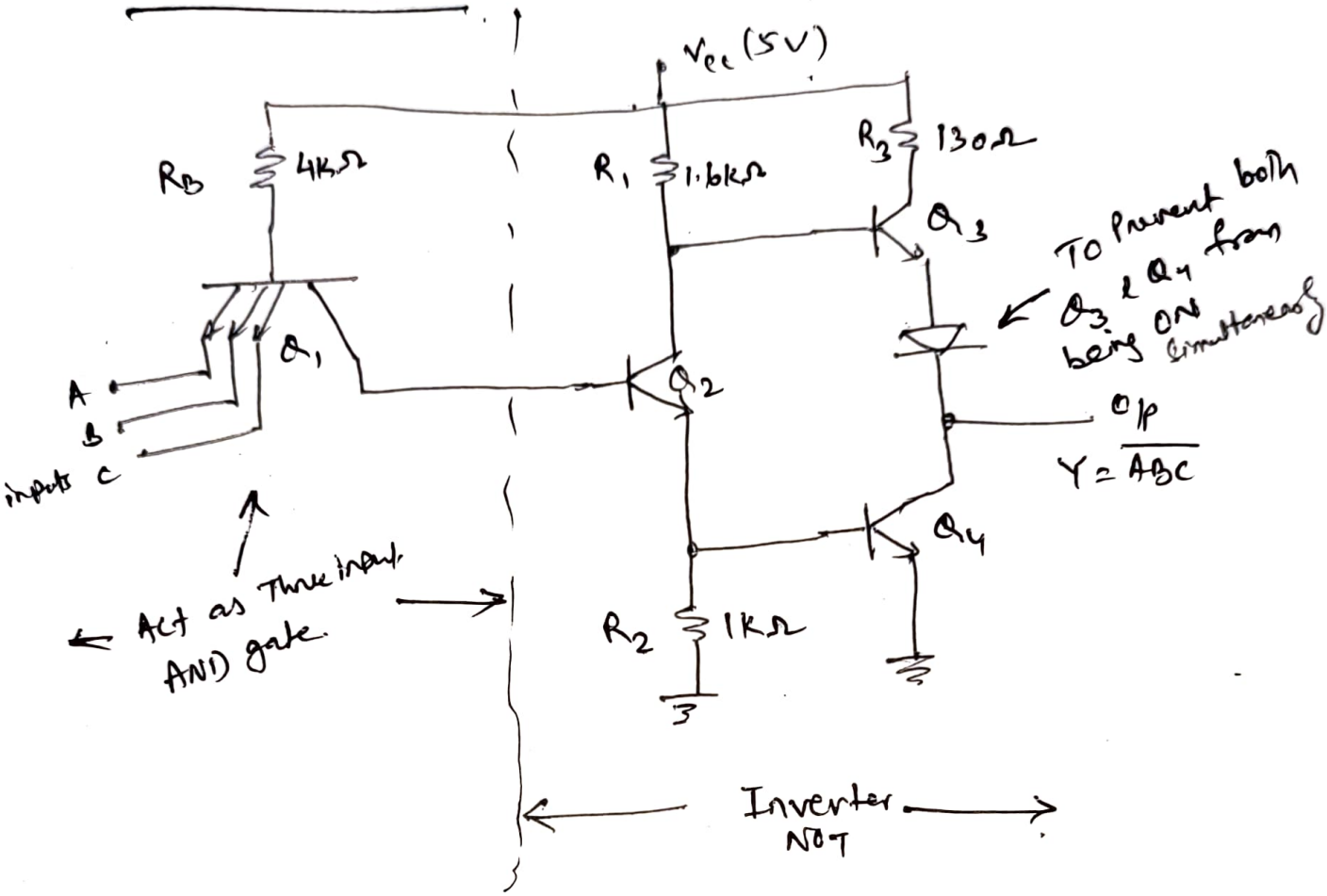
Logic 0 I/P - 0 to 0.8

Logic 1 input - 2 to 5

Noise immunity - 0.4 V

The basic circuit for TTL Logic family is the NAND gate.

TTL NAND Gate



- When Q_1 is ON, i.e all inputs are zero (Ground)
  Q_2 is OFF & Q_4 is off. so $o/p = V_{cc}$ = Logic - 1
- When all inputs are 1, Then Q_1 is reverse biased, so OFF however, CB junction of Q_1 is forward biased to supply necessary base current to Q_2. so Q_2 - Saturates (ON)
- Drop across R_2 is sufficient to make Q_4 ON.
  so o/p = Low.

. In absence of diode, ~~transis~~ Q_3 will conduct slightly when the o/p is low. In order to prevent this, a diode is connected between Q_3 & Q_4.

The voltage drop across the diode keeps the base-emitter junction of Q_3 reverse biased. So Q_4 will conduct when o/p is low.

(70)

Version	Propagation delay (ns)	Power dissipation (mW)	Max^m clock MHz	Fan out
Standard TTL	10	10	35	10
Low power LTTL	33	1	3	10
High speed HTTL	6	22	50	10
Schottky STTL	3	19	125	10
Low power Schottky LSTTL	9.5	2	45	10.

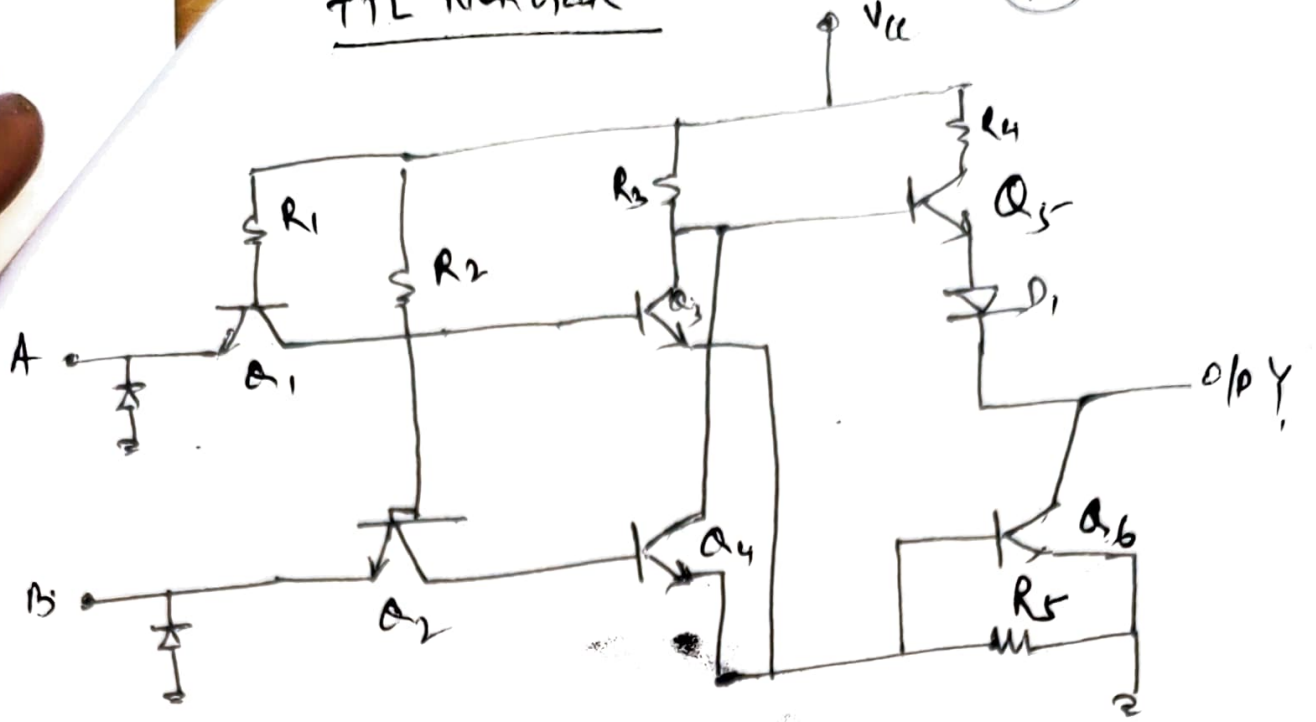
Output Connections in TTL

(1) Totem pole o/p. (2) Open collector o/p (3) Tri-state o/p

Totem pole o/p

- Standard o/p of a TTL gate.
- Designed to reduce propagation delay.
- Provide sufficient o/p power for high fan out
- Low o/p impedence in both logical state.
  - when Q_3 ON - 70 Ω. - Logic-1.
  - when Q_4 ON - 12 Ω - Logic-0
- Totem pole o/p s can't be connected together for wired AND

TTL NOR Gate



Operation

① A=0, B=0, Q_1 & Q_2 forward biased. and full current away from transistor Q_3 & Q_4.

So Q_3-Q_4 — OFF, O/p — High.

Q_5 - ON, Q_6 = OFF.

② A=0, B=1, Q_1 - Forward biased - ON.
Q_2 - Reverse biased. - OFF

Q_3 - OFF, Q_4 - ON.

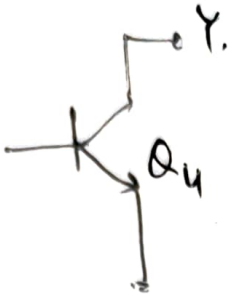
Q_6 ON, Q_5 - OF — O/p = Low

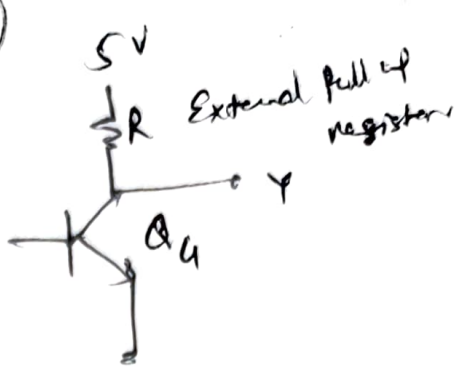
③ A=1, B=0, Q_1 - OFF, Q_2 - ON, Q_3 - ON, Q_4 = OFF

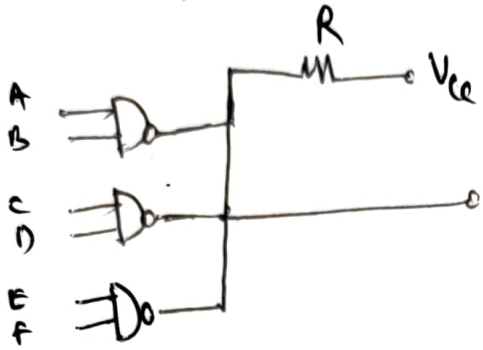
Q_6 - ON, Q_5 - off. O/p = Low.

④ A=1, B=1, Q_3 - ON
Q_4 - ON
Q_6 - ON, — op = Low.
Q_5 - OFF

Open collector O/P







& R_3

- Q_3 & Diode D_1 is removed from standard circuit
- External pull-up register is required to be connected.
- Provides wired AND operation
- O/p is Low when Q_4 – ON, O/p is high when Q_4 is off.
- Increase in switching time delay because of pull-up register with resistance of few KΩ.
  So slow switching speed.

Note ① Floating TTL input is equivalent to high input.
as when input is high, there is no emitter current.
Similarly, when open, no emitter current.

② Un used input may pick up stray noise voltage.
leading to erroneous operation, so it should be connected to either Vcc or ground.