2K22/CO/427 Sandesh Shrestha

assignment 2 COA

Date : / /
Page No.

4-2. The outputs of 4 registers, R0, R1, R2, R3 are connected through 4 to 1 line multiplexers to the inputs of a fifth register, R5. Each register is eight bits long. The required number of transfers are dictated by four timing variables T0 through T3 as follows:

T0 : R5 ← R0

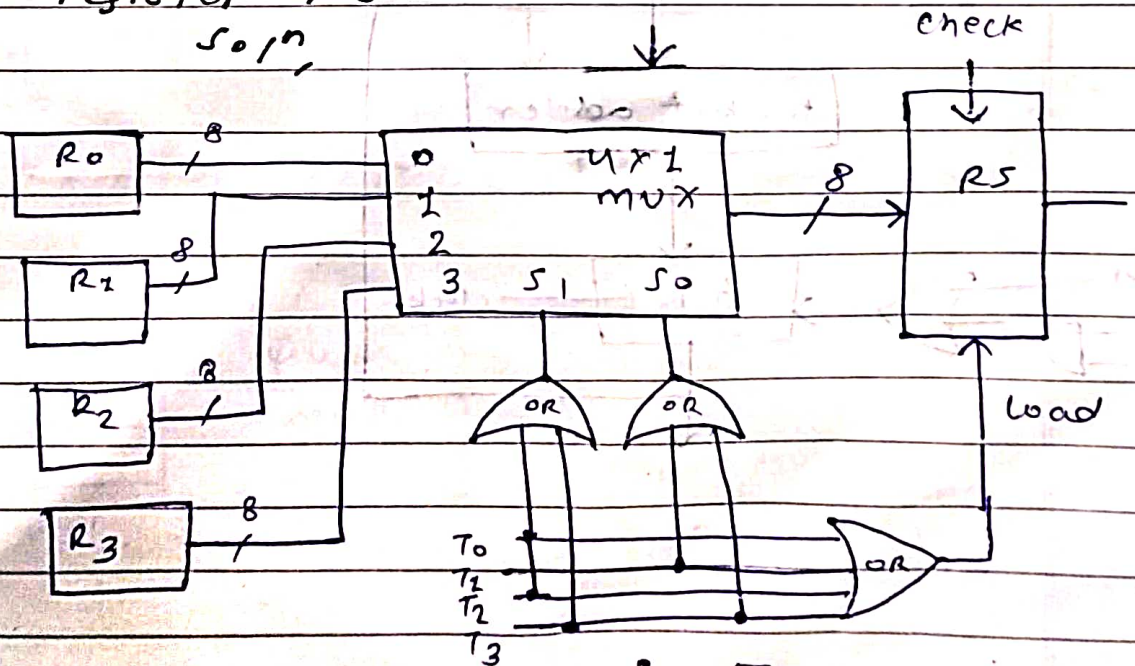
T1 : R5 ← R1

T2 : R5 ← R2

T3 : R5 ← R3

The timing variables are mutually exclusive which means that only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block diagram showing the hardware implementation of the register transfers. Include connections necessary from 4 timing variables to ~~obtain~~ selection inputs of multiplexers and to the load input of register R5.

Soln,



$S_1 = T_2 + T_3$

$S_0 = T_1 + T_3$

$load = T_0 + T_1 + T_2 + T_3$

Date : / /
Page No.

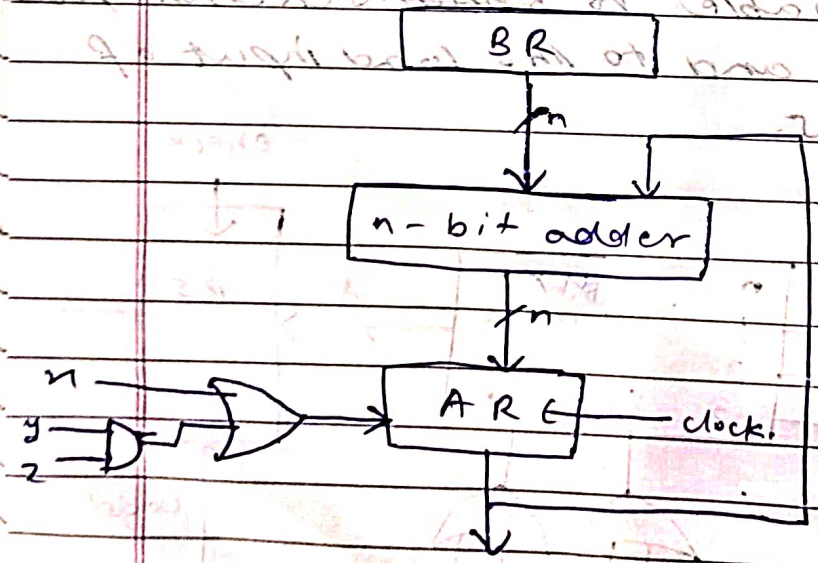
T_0	T_1	T_2	T_3	S_1	S_0	Load
0	0	0	0	x	x	0
1	0	0	0	0	0	1
0	1	0	0	0	1	1
0	0	1	0	1	0	1
0	0	0	1	0	1	1

4-8. Draw the block diagram for hardware that implements the following statements:

$x+yz$: $AR \leftarrow AR + BR$

where AR and BR are 2 n-bit registers and x, y and z are control variables. Include the logic gates for control function.

$x+yz$: $AR \leftarrow AR + BR$



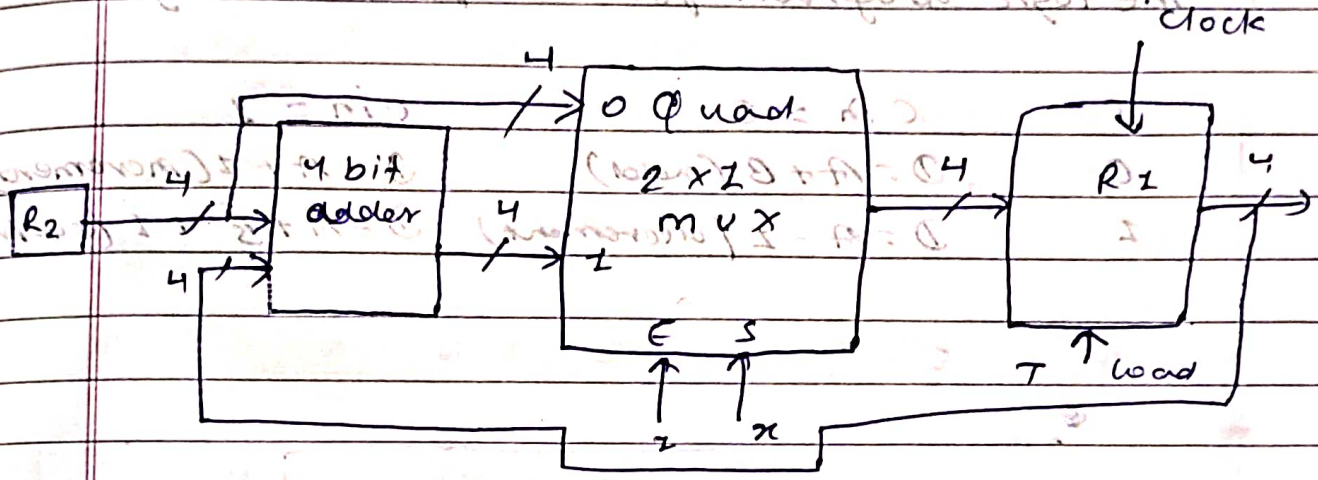
2K21/C0/412 Sandesh Shrestha

Date : / /
Page No.

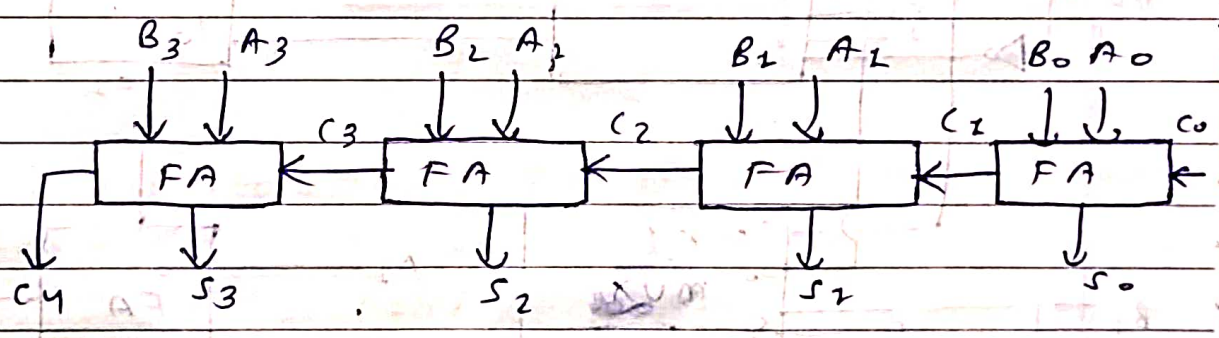
4-10: Solution,

$x'T: R1 \leftarrow R1 + R2$

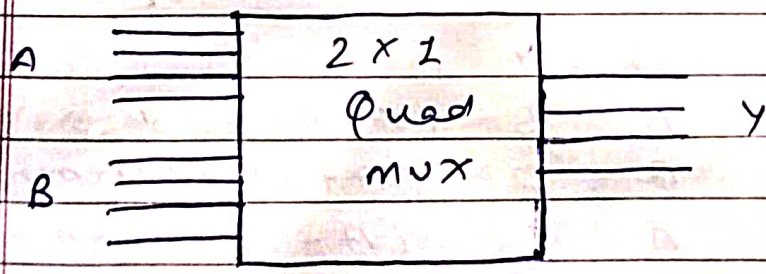
$x'T: R1 \leftarrow R2$



4 bit binary adder:



2x1 mux (Quad):

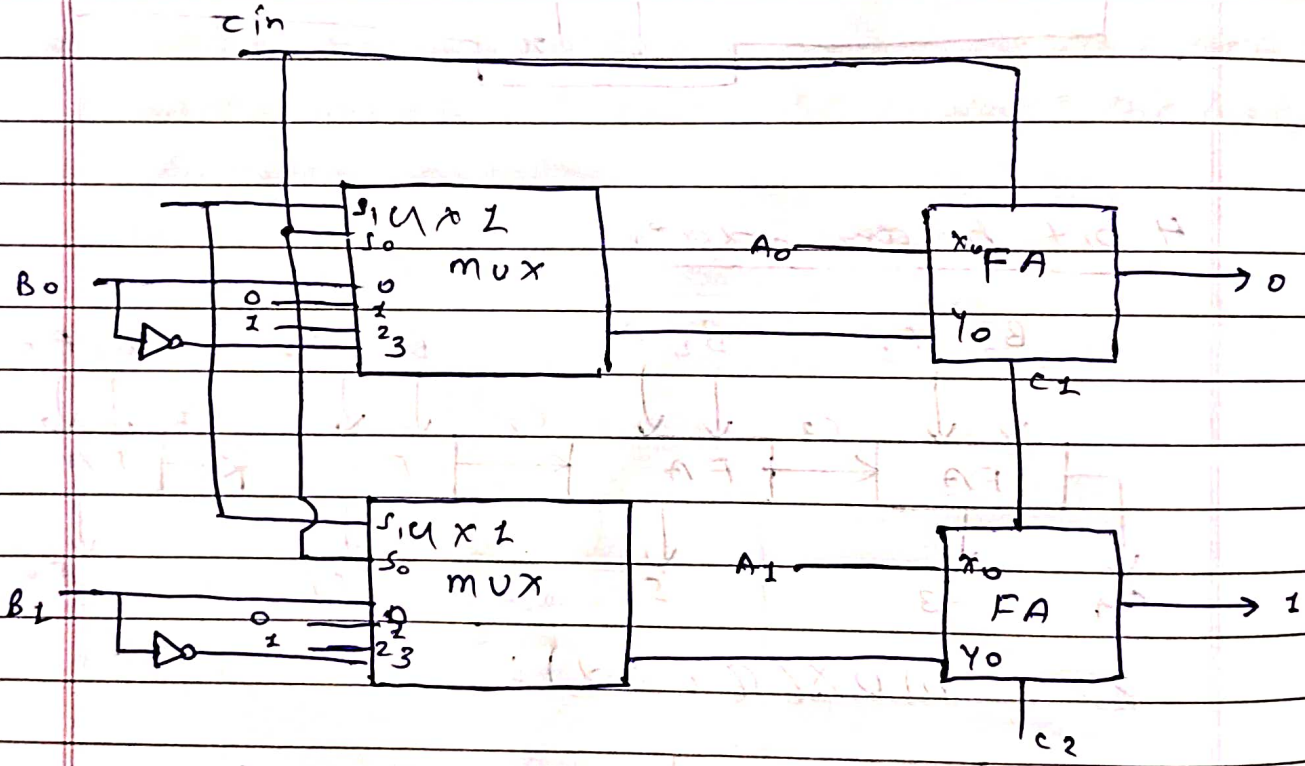


Date : / /
Page No.

4-15. design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjuction with input carry C_{in}. Draw the logic diagram for the first 2 stages.

S	$C_{in} = 0$	$C_{in} = 1$
0	$D = A + B$ (add)	$D = A + 1$ (increment)
1	$D = A - 1$ (decrement)	$D = A + \bar{B} + 1$ (subtract)

for,



S	C_{in}	X	Y	
0	0	A	B	(A+B) add
0	1	A	0	(A+1) Increment
1	0	A	1	(A-1) decrement
1	1	A	$\bar{B}$	(A-B) subtract

Date : / /
Page No.

4.18) Register A holds 8 bit binary 11011001. determine the B operand and the logic microoperations to be performed in order to change the value in A to

(a) 01101101

(b) 11111101

sol^n,

(a) A = 11011001 ⊕
B = 10110100

A ← A⊕B : 01101101

(b) A = 11011001
B = 10110100

A ← AVB : 11111101

4.19) The 8 bit registers AR, BR, CR, DR initially have following values.

AR = 11110010
BR = 11111111
CR = 10110001
DR = 11101010

determine 8 bit values in each register after the execution of following sequence of microoperations.

AR ← AR+BR add BR to AR

CR ← CR∧DR, BR ← BR+1 and DR to CR, increment BR

AR ← AR - CR subtract CR from AR

Date : / /
Page No.

Sol^n,

AR = 1 1 1 1 0 0 1 0

BR = 1 1 1 1 1 1 1 1

CR = 1 0 1 1 1 0 0 1

DR = 1 1 1 0 1 0 1 0

(a) Add BR to AR : AR ← AR + BR

AR = 1 1 1 1 0 0 1 0
BR = 1 1 1 1 1 1 1 1 (+)

AR : 1 1 1 1 0 0 0 1

(b) CR ← CR ∧ DR , BR ← BR + 1

CR = 1 0 1 1 1 0 0 1
DR = 1 0 1 0 1 0 1 0 (∧)

CR : 1 0 1 0 1 0 0 0

BR = 1 1 1 1 1 1 1 1
0 + 1

BR : 0 0 0 0 0 0 0 0

c) AR ← AR → CR

AR = 1 1 1 1 0 0 0 1
CR = 1 0 1 0 1 0 0 0 (−)

AR : 0 0 1 1 0 0 0 1

Thus, finally, AR = 0 0 1 1 0 0 0 1

BR = 0 0 0 0 0 0 0 0

CR = 1 0 1 0 1 0 0 0

DR = 1 1 1 0 1 0 1 0 #