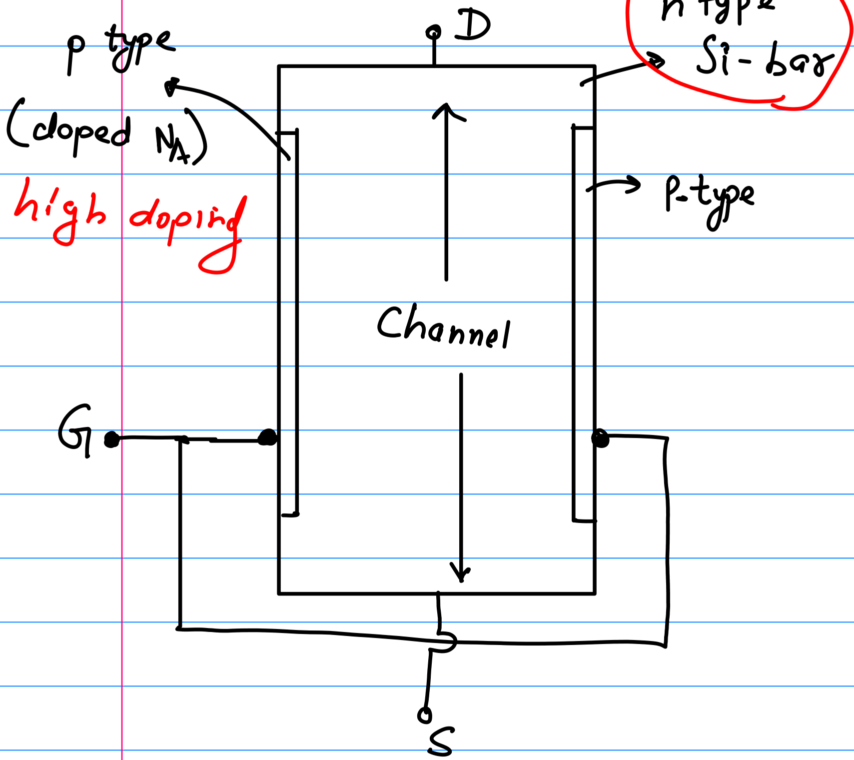
Junction Field Effect Transistor (JFET)

BJT : Bipolar → e^-s & holes both contribute to I in both NPN & PNP

JFET : Unipolar → only 1 type of carrier conduct
n-channel JFET : e^-
p-channel JFET : holes

3 terminals → Gate (G)
Drain (D) ≡ Collector in BJT
Source (S) ≡ Emitter in BJT

n-channel JFET



[doped(N_D), Si acts as a resistance]

$J = \sigma \vec{\mathcal{E}}$ — σ: conductivity

Ohm's law

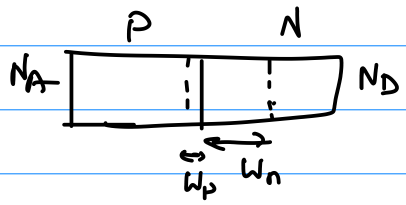
$V = IR$

$\sigma_n = q n \mu_n$

$\frac{I_{drift}}{Area} = J = \sigma \vec{\mathcal{E}} = q n \mu_n \vec{\mathcal{E}}$

Channel : Undepleted, doped Si region between S & D

$N_A >> N_D$
(p^+) (n)



$N_A >> N_D$

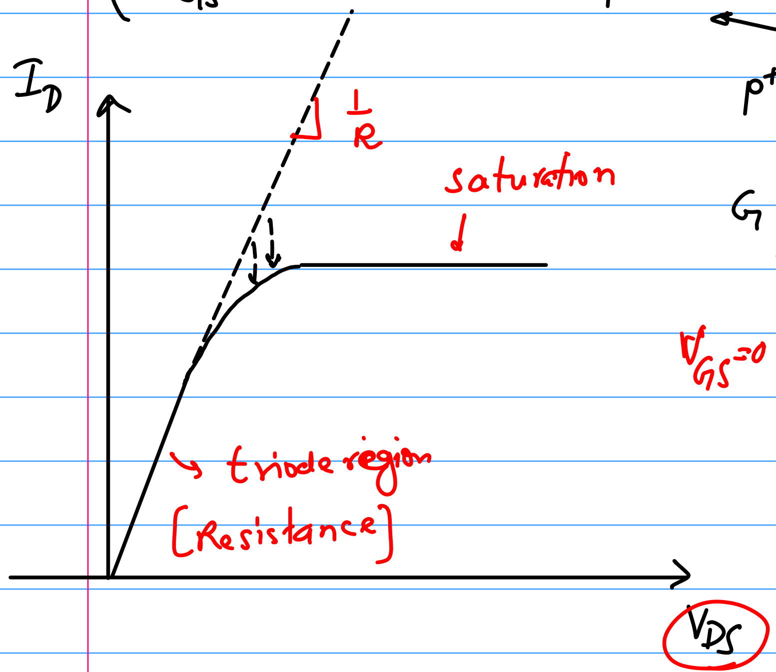
$W_n >> W_p$

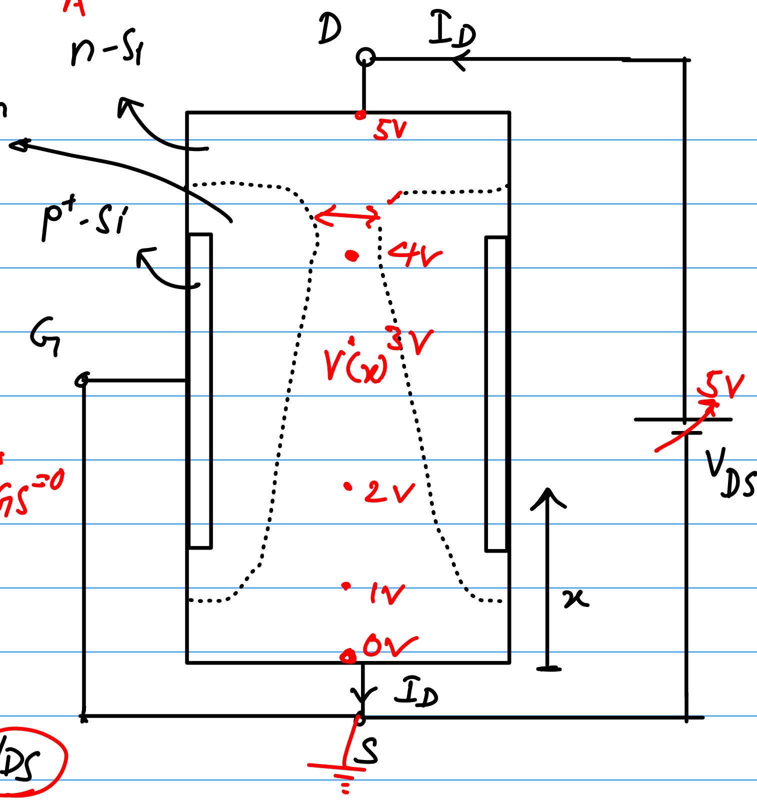
& $W_N + W_p = W$

$\Rightarrow \boxed{W_N \simeq W}$

Let $\begin{cases} V_{DS} > 0 \\ V_{GS} = 0 \end{cases}$

$R = \rho \frac{L}{A}$





(i) for V_{DS} = v. small, channel is a resistance (follows Ohm's law) so, I_D-V_{DS} curve is a straight.

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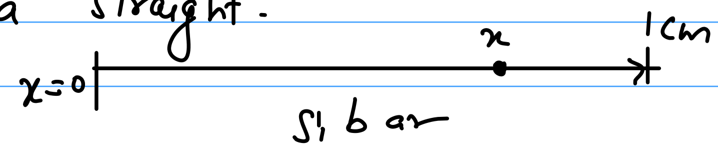
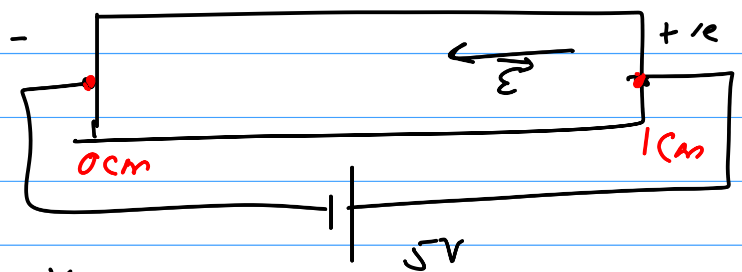
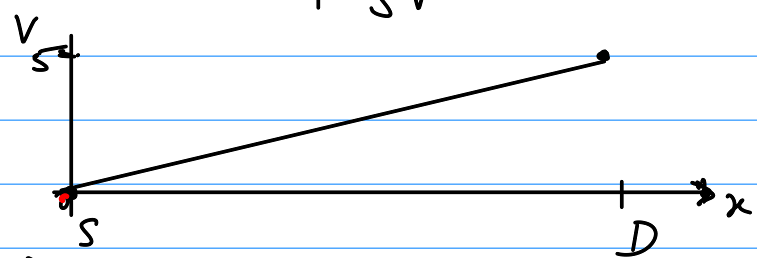
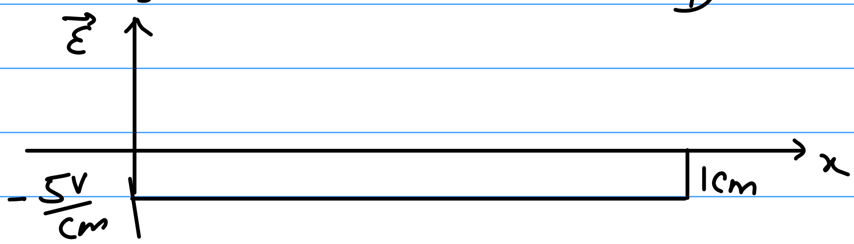




V(x) is a straight line

V(x) in-creases as x increases

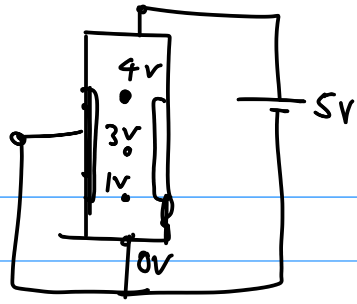




$V_D > V_S$ $\quad (V_D - V_G) > \underbrace{(V_S - V_G)}_{0}$ $\Rightarrow V_D - V_G > 0$

$V_{DG} > 0$

at any x $\underline{\underline{V(x) > 0}}$



$V_G = 0$ v,

$V(x) - V_G$ increases as x increases

→ R.B vol across the p-N junction

↓

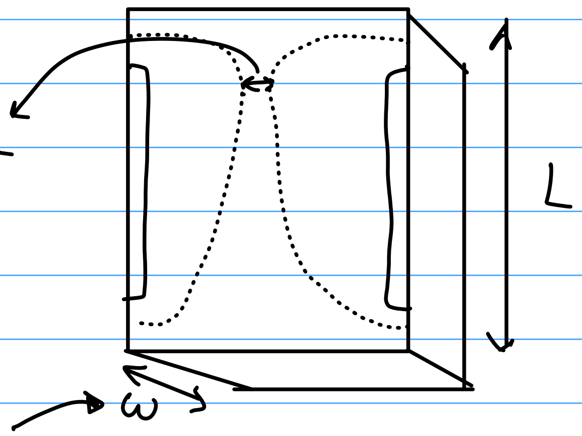
increases W

So, closer to drain $V(x)$ is more +ve, so, more R.B, more dep. width W

* If $V_{DS} \uparrow$, near D, $W \uparrow$, effective $\underbrace{\text{channel width} \downarrow}$.

↓

Channel resistance ↑



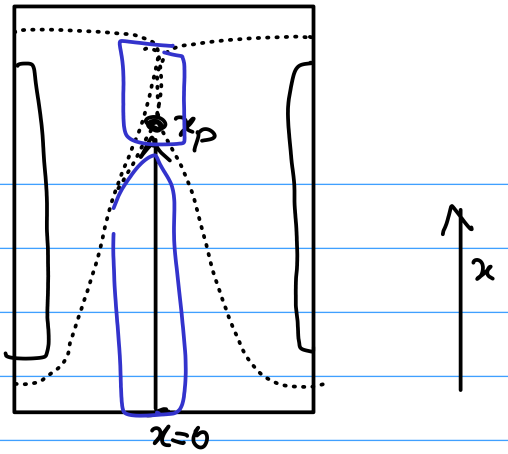
$\uparrow R = \rho \dfrac{L}{a \downarrow}$

$a = \downarrow$ channel width × thickness

→ I_D smaller than expected at that V_{DS}

At some V_{DS},

Depletions regions come in contact* with each other (Pinch Off)



$\sigma = qn\mu_n$ → $n = 0$, $\sigma = 0$

effective channel width ~ 0.V. small (~0)

there should be No Conductance. → $I_D = 0$ (not actually)

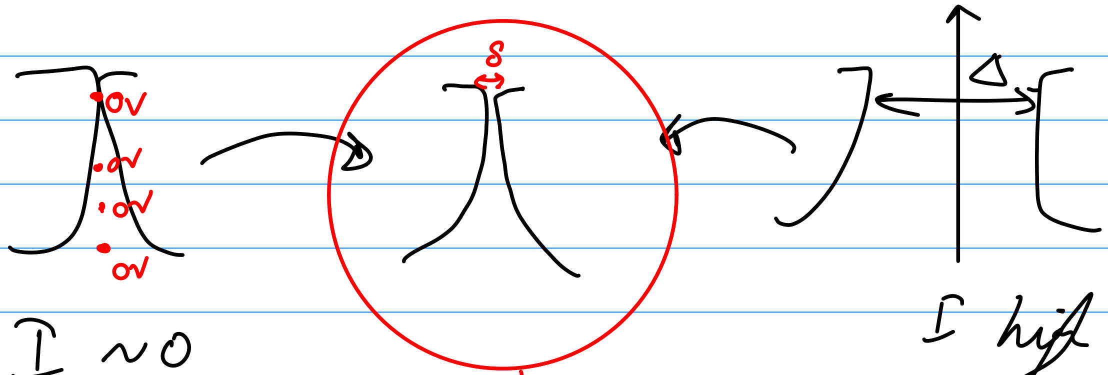
↓ no vol. drop in the resistive part → $V(x_p) = V_s = 0$

no R.B. at that point → dep. region shrinks back

↓

Dep doesn't touch each other

So in pinch-off there a v. tiny gap b/w the 2 dep regions ($\delta \to 0$)



$I \sim 0$

$\boxed{V \sim 0}$

$V(x_p) \sim 0$

$V_{RB} \sim 0$ → $W \downarrow$

Settling point

Pinch off point

I high

$V(x_p) \uparrow$

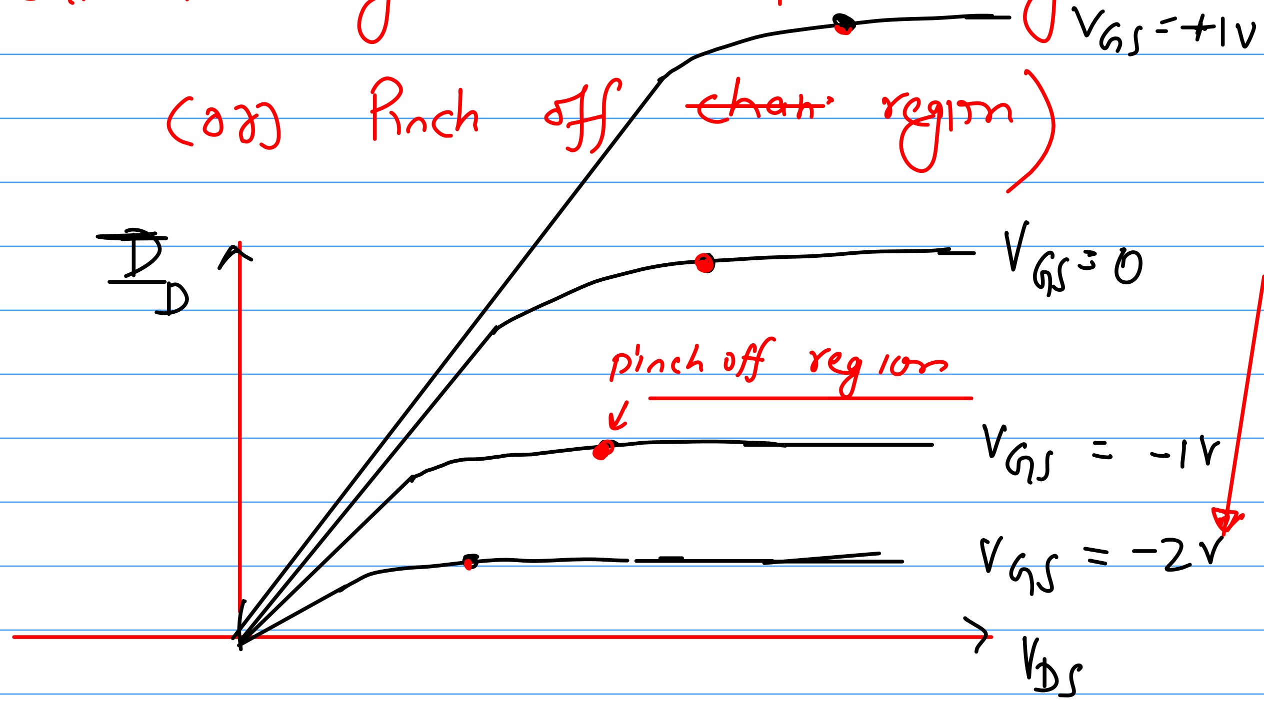
$V_{RB} \uparrow$

$W \uparrow$, $\Delta \downarrow$

$V = IR$

* after pinch off point I_D no longer increases with V_{DS}

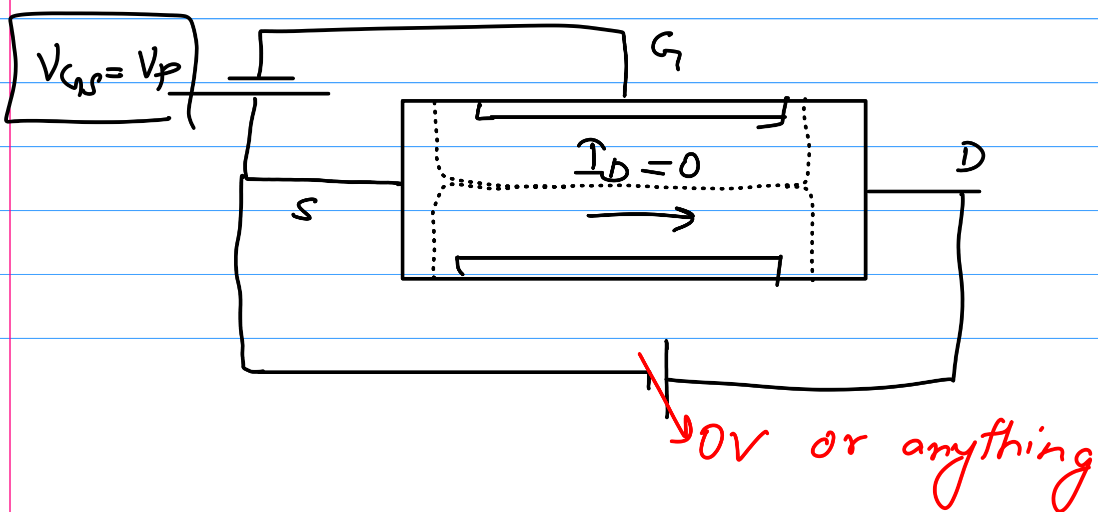
(Saturation region (or) Pentode region (or) Pinch off ~~chan~~ region)



* Pinch Off Voltage: (V_p) ! V_{GS} vol. at which channel width becomes 0 (i.e. for any V_{DS} bias, $\to V_{DS}=0V$ there is no drain current)

$$\boxed{I_D = 0 \quad \text{at} \quad \underbrace{V_{GS} = V_p}_{\text{R.B. vol.}}}$$

So, for n-channel JFET, V_p = −ve vol.



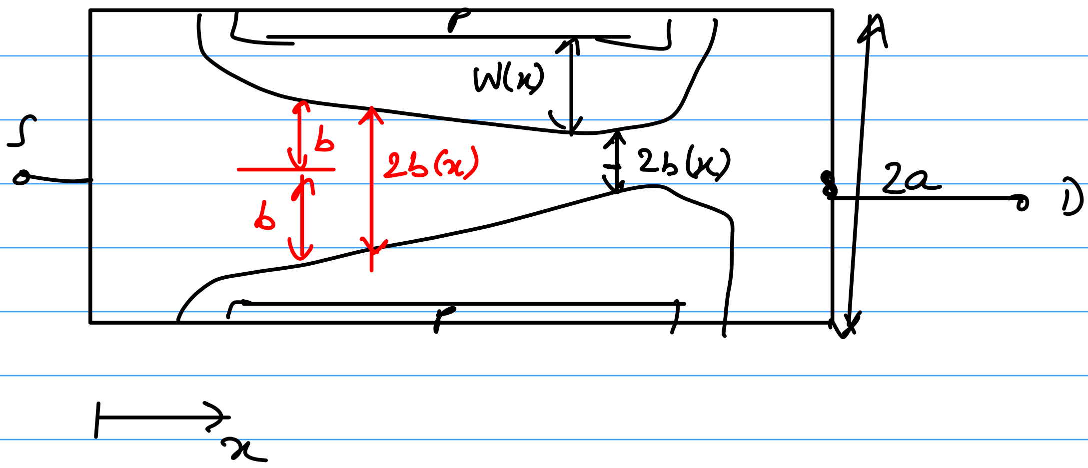
cut-off region

$W_p << W_N \quad \because \quad \underline{N_A >> N_D} \rightarrow$ channel doping

$\hookrightarrow \underline{W_n} \simeq \underline{W}$

$$\underline{W(x)} = a - b(x) = \sqrt{\frac{2\epsilon}{q}\left(\frac{1}{N_D}\right)\overbrace{(V_0 - \underline{V(x)})}^{V_{barrier}}}$$

$\hookrightarrow$ -ve



built-in pot.

Let $|V_0| << |V(x)|$

at pinch off vol. $\underline{(V_{GS} = V_p)}$, $I_D = 0$

$$V(x) = \underline{V}$$

$$\underline{b(x)} = \underline{b} = \underline{0}$$

So,

$$\boxed{|V_p| = \frac{qN_D}{2\epsilon} a^2}$$

**

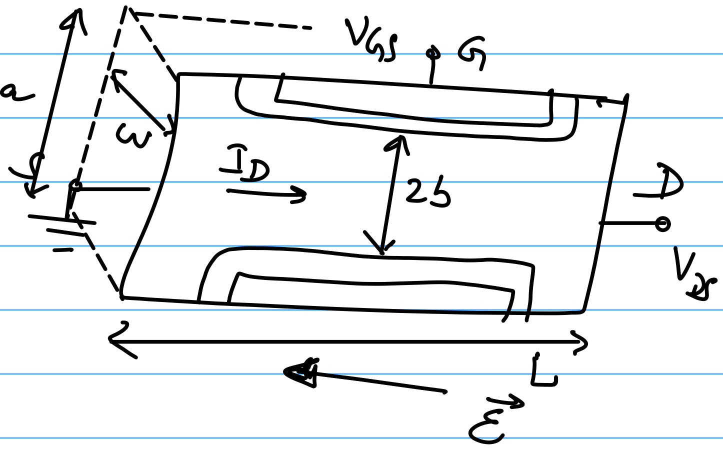
a = half width of JFET

Relation between reverse bias gate to source voltage and the effective channel width 2b

$$\boxed{V_{GS} = \left(1 - \frac{b}{a}\right)^2 V_p}$$

* I_D expression in different operating regions :

1) **Triode Region :** JFET acts a resistance.



drain current is drift current

$$I_D = qAnv_d$$

$A \rightarrow 2bw$

$n \rightarrow N_D$ (uniform doping)

$v_d \rightarrow$ drift vel

$$v_d = \mu_n \vec{E} = \mu_n \frac{V_{DS}}{L}$$

$\mu_n \rightarrow$ mobility

$$\boxed{I_D = 2bw\,q\,N_D\,\mu_n \frac{V_{DS}}{L}}$$

for low V_{DS}

$I_D \propto V_{DS}$

[Ohm's Law]

for Low V_{DS} (proper or deep triode region),

$b \sim a$ (low depletion)

$$\boxed{r_{D,ON} = \frac{L}{2aw\,q\,N_D\,\mu_n}} \rightarrow \text{for } V_{GS} = 0$$

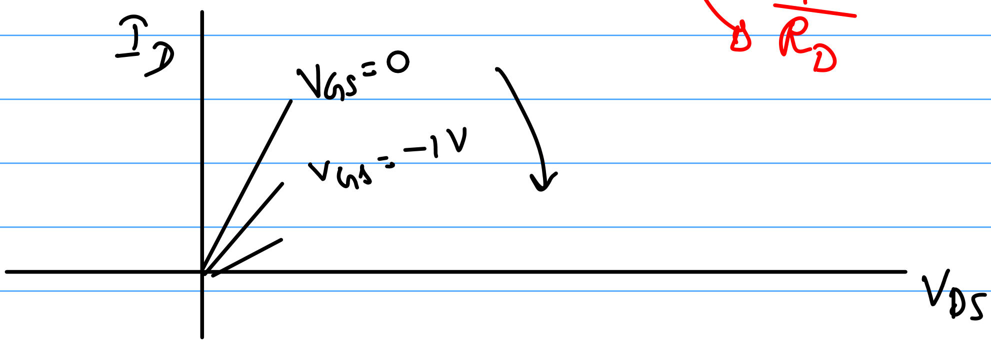
(from $V_{GS} = (1-\frac{b}{a})^2 V_P$)

Replacing b in I_D expression

$I_D \propto V_{DS}$ (Ohm's law)

$$\boxed{I_D = \frac{2awqN_D\mu_n}{L}\left[1-\left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]V_{DS}}$$

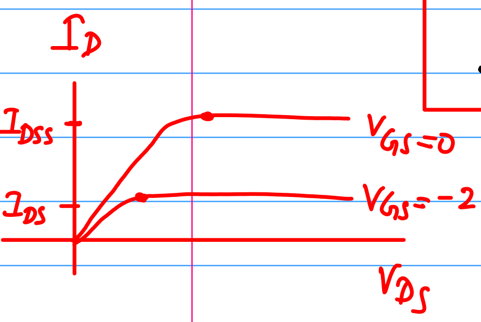
$\rightarrow \frac{1}{R_D}$



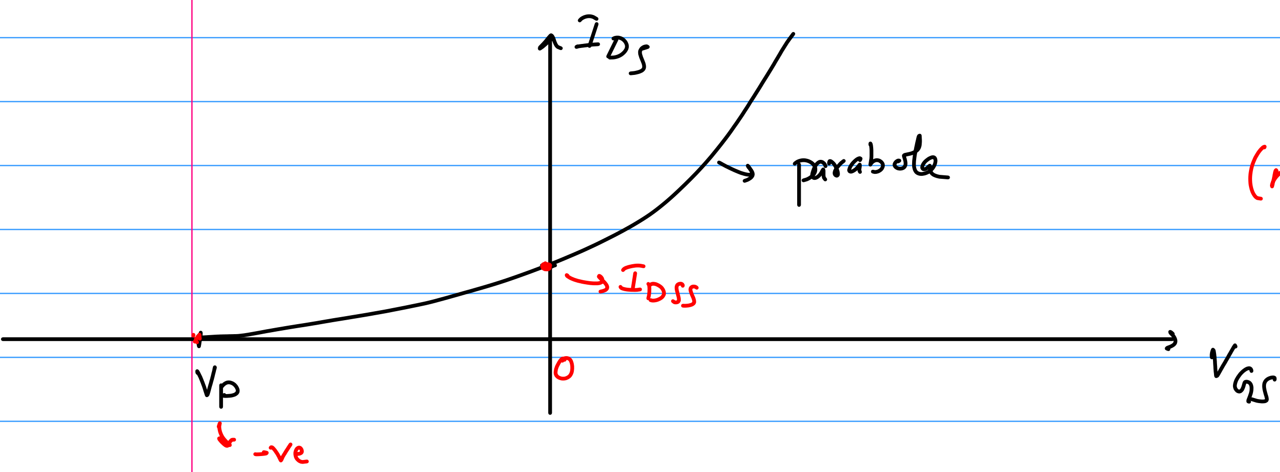
* ~~Pinch off region~~ : (Saturation region)

here, ideally I_D is independent of V_{DS}

$$\boxed{\underbrace{I_{DS}}_{\text{saturation}} = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2} \; *$$



I_{DSS} is saturation drain current when $V_{GS}=0$



(n-channel JFET)

Cut-off : $V_{GS} = V_P$ $\quad I_D = 0 \rightarrow$ negligible

$\rightarrow |V_{GS}| > |V_P|$

A1

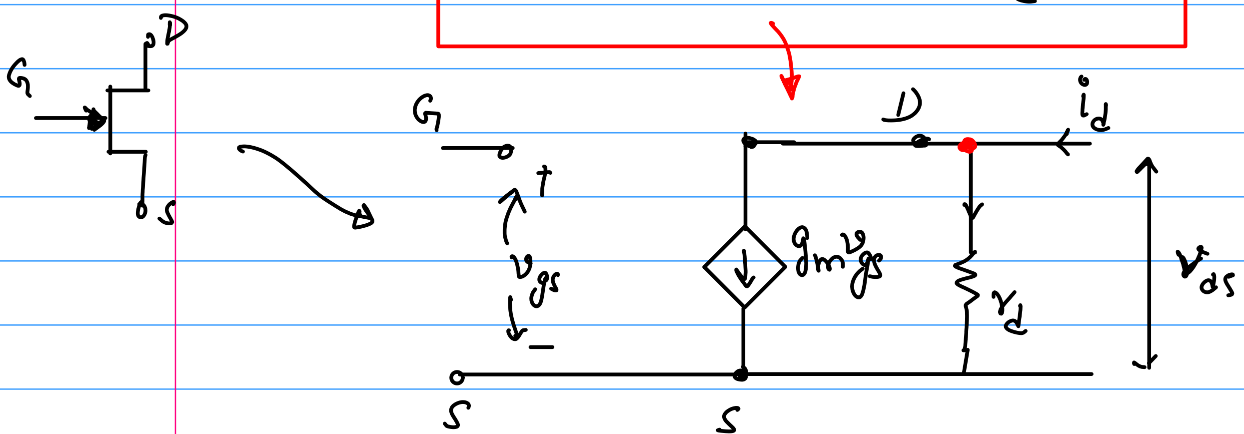
→ Small signal model :

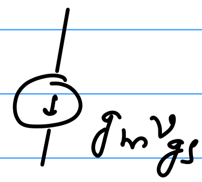
total $\leftarrow i_D = f(v_{GS}, v_{DS})$

$$\Delta i_D = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{DS}} \Delta v_{GS} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{GS}} \Delta v_{DS}$$

$\Delta i_D \rightarrow$ small signal; $\Delta v_{GS} \rightarrow v_{gs}$; $\Delta v_{DS} \rightarrow v_{ds}$

$$\boxed{i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds}}$$



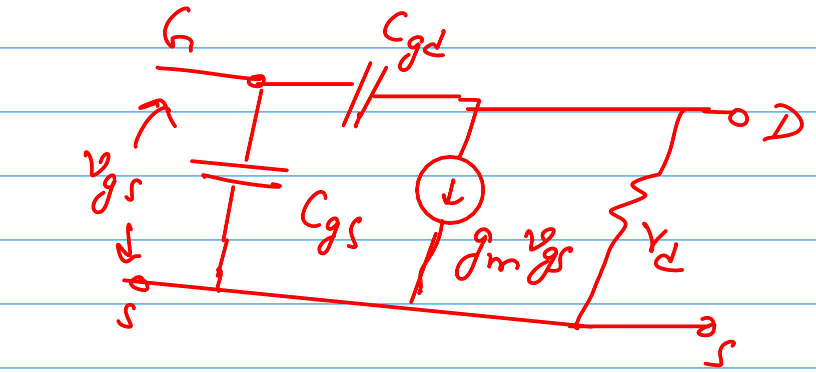


Low Frequency Small signal model

G-S is R.B. J^n → v.v. high resistance ≡ Open ckt.

high freq. small signal model

complete model



at low freq. cap $\rightarrow$ O.C.

* Transconductance:

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{v_{DS}}$$

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\boxed{g_m = -\frac{2}{V_P}\sqrt{I_{DSS}\, I_{DS}}}$$ $\rightarrow$ n-channel

$$\boxed{g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

g_{m_o} is trans-cond. when $V_{GS} = 0$

where $$\boxed{g_{mo} = \frac{-2 I_{DSS}}{V_P}}$$

$I_{DSS} \rightarrow$ +ve

$V_P \rightarrow$ -ve for n-channel

* Idss and Vp always have opposite signs. So, gmo will always be positive

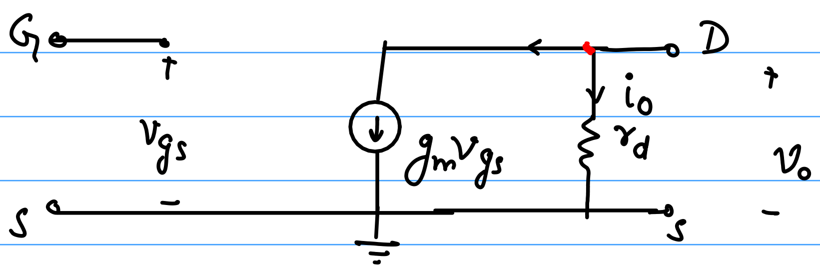
$$r_D = \left.\frac{\partial v_{DS}}{\partial i_{DS}}\right|_{v_{GS}} = \left.\frac{v_{ds}}{i_d}\right|_{v_{GS}}$$

O/p resistance

Amplification factor, $\mu \equiv -\left.\frac{\partial v_{DS}}{\partial v_{GS}}\right|_{I_D}$

$$\mu = -\left.\frac{v_{ds}}{v_{gs}}\right|_{I_D}$$

$$\boxed{\mu = g_m r_d}$$



If no load is connected :-

$$v_o = v_{ds} = i_o r_d$$

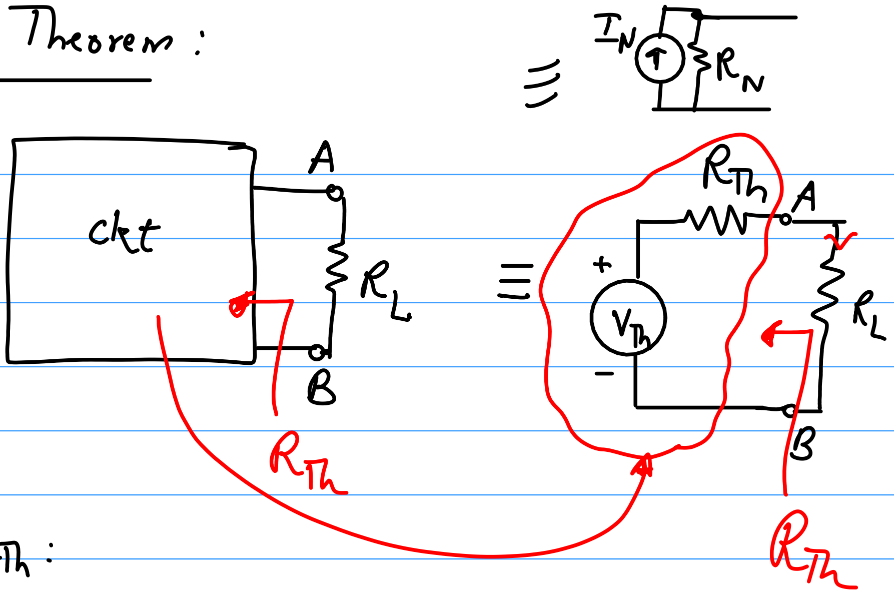
$$i_o = -g_m v_{gs}$$

$$v_o = -g_m v_{gs} r_d$$

$$\boxed{A_v = \frac{v_o}{v_{gs}} = -g_m r_d}$$

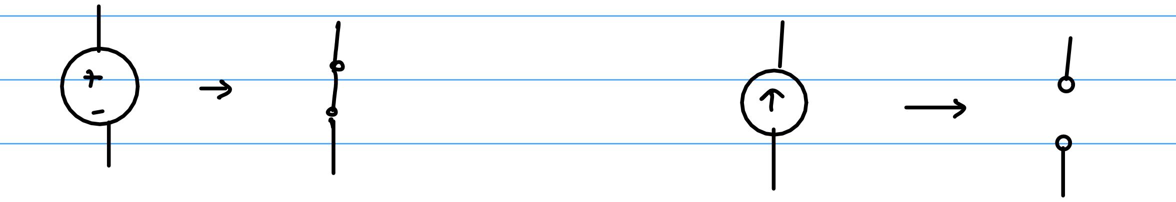
for Common source JFET amp.

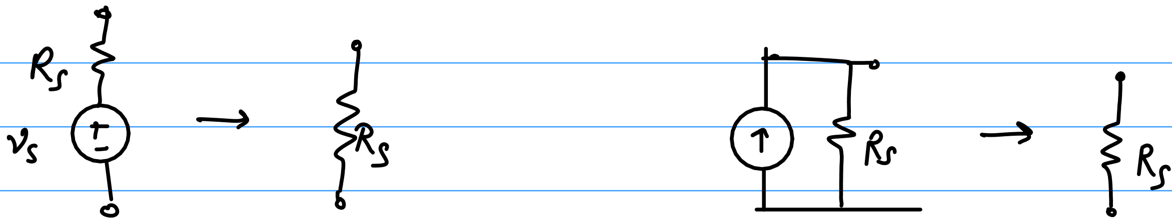
Thevenin's Theorem :



To find R_{Th} :

(1) Remove the external load.
(2) Replace all indep. sources by their internal (source) resistance :





(3) Find the equivalent resistance (Req) across the output terminals (A & B)

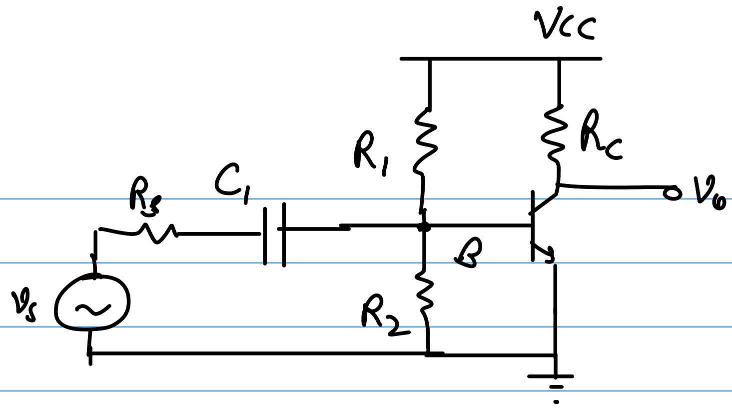
$$\boxed{R_{Th} = R_{eq}}$$

→ ## To find V_{Th} :

(1) Step 1 is same as above

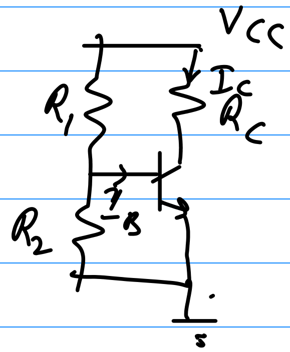
(2) Find the net vol. across the 2 output terminals (A, B). So, $V_{AB} = V_{Th}$

BJT CE amp :



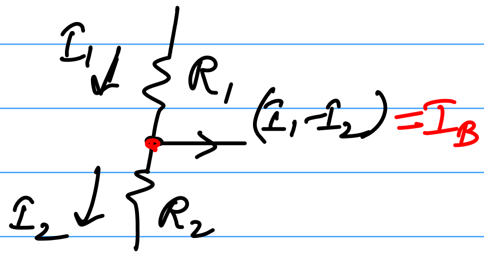
for DC :

$C_1 \rightarrow$ O.C.



Assumption − High 'β'. v. low I_B. (neglect)

then R_1 & R_2 are in series.

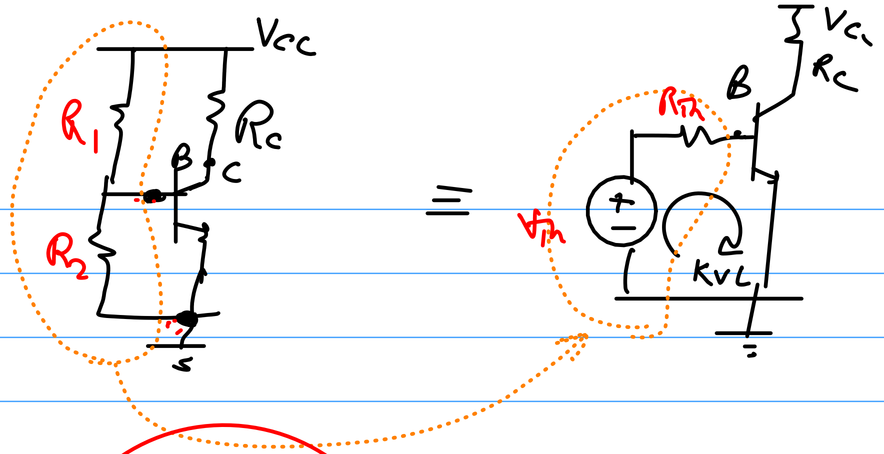


R_1 & R_2 Not in series

But if $I_1 - I_2 = I_B$ is negligible

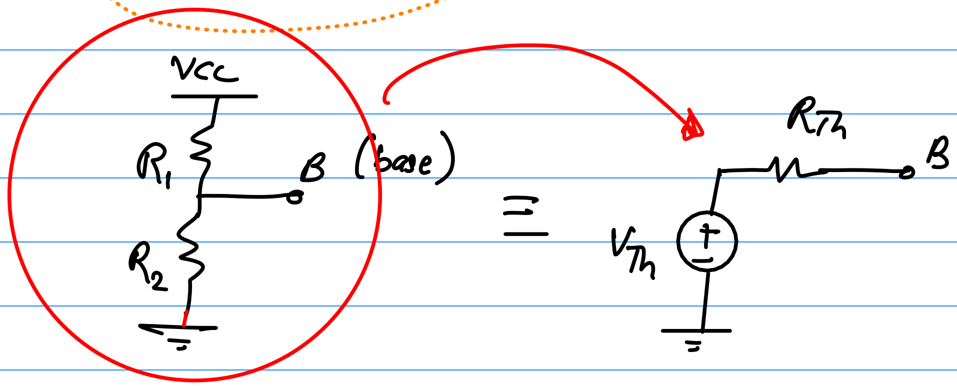
then R_1 & R_2 have roughly same current

They can be considered to be in series



$$V_{Th} = \frac{R_2}{R_1+R_2} V_{cc}$$

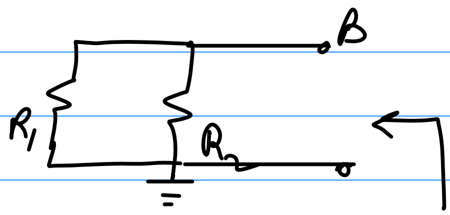
$$R_{Th} = \frac{R_1 R_2}{R_1+R_2}$$



BJT is the load to this network.

(1) So remove the BJT

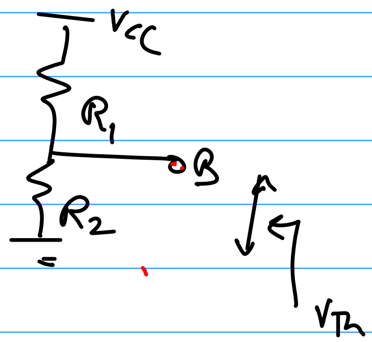
(2) S.C. Vcc



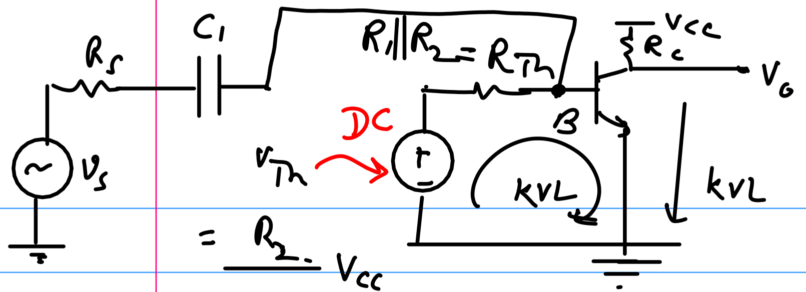
$R_{eq} = R_{Th} = R_1 \| R_2$

(3) $\boxed{R_{Th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2}}$

V_{Th} :

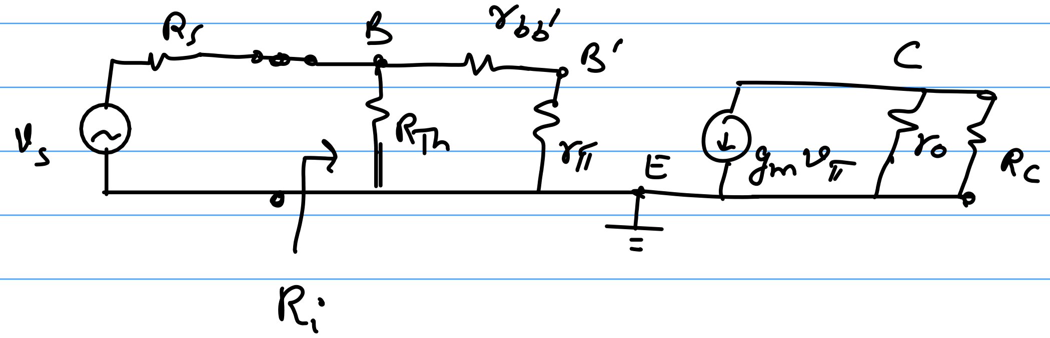


$$\boxed{V_{Th} = \frac{R_2}{R_1 + R_2} V_{cc}}$$



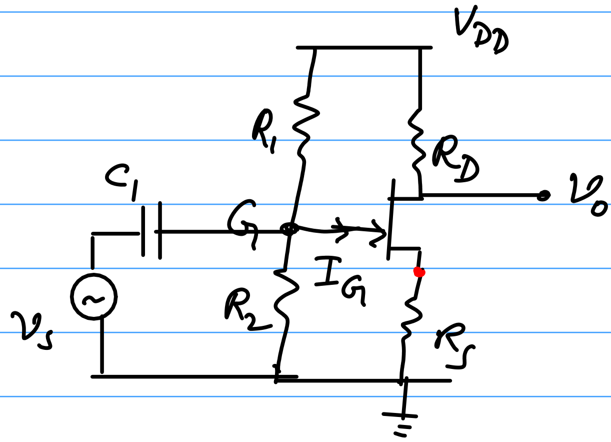
$$= \frac{R_2}{R_1 + R_2} V_{cc}$$

$\Downarrow$ small signal (low freq.)



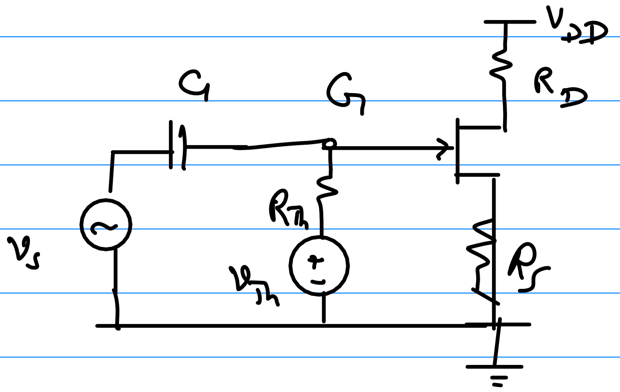
Common Source :

In saturation,
G junction is
R.B.
So, $I_G \simeq 0$



So R_1 & R_2 are in series.

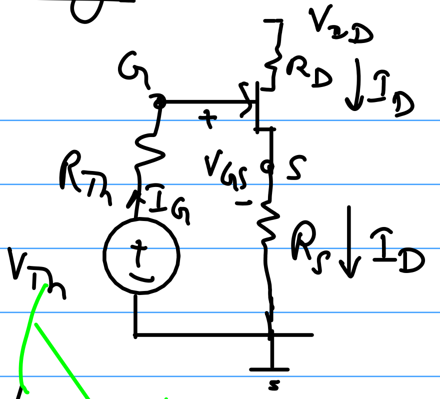
$\equiv$



$R_{Th} = R_1 \| R_2$

$$v_{Th} = \frac{R_2}{R_1 + R_2} V_{DD}$$

DC analysis - $C_1 \to$ O.C.



i/p KVL -

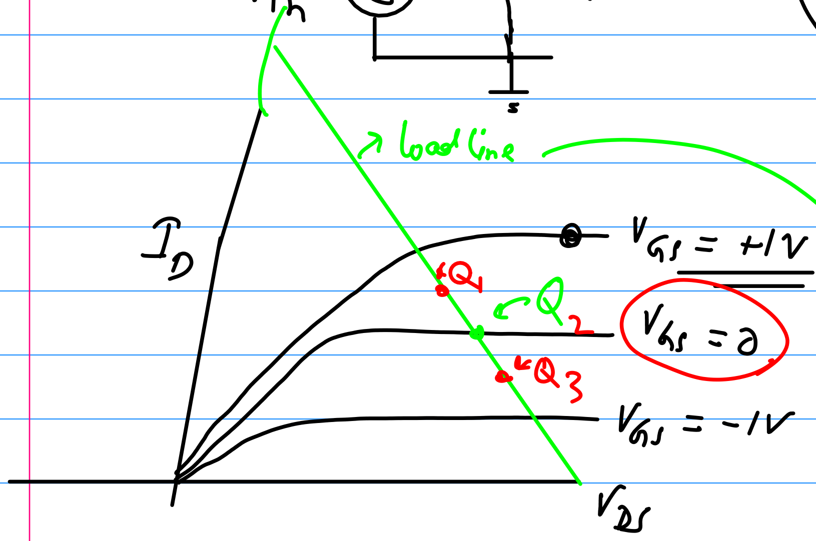
$$V_{Th} - \cancel{I_G R_{Th}}^{\,0} - V_{GS} - I_D R_S = 0$$

$$V_{GS} = V_{Th} - I_D R_S$$

o/p KVL -

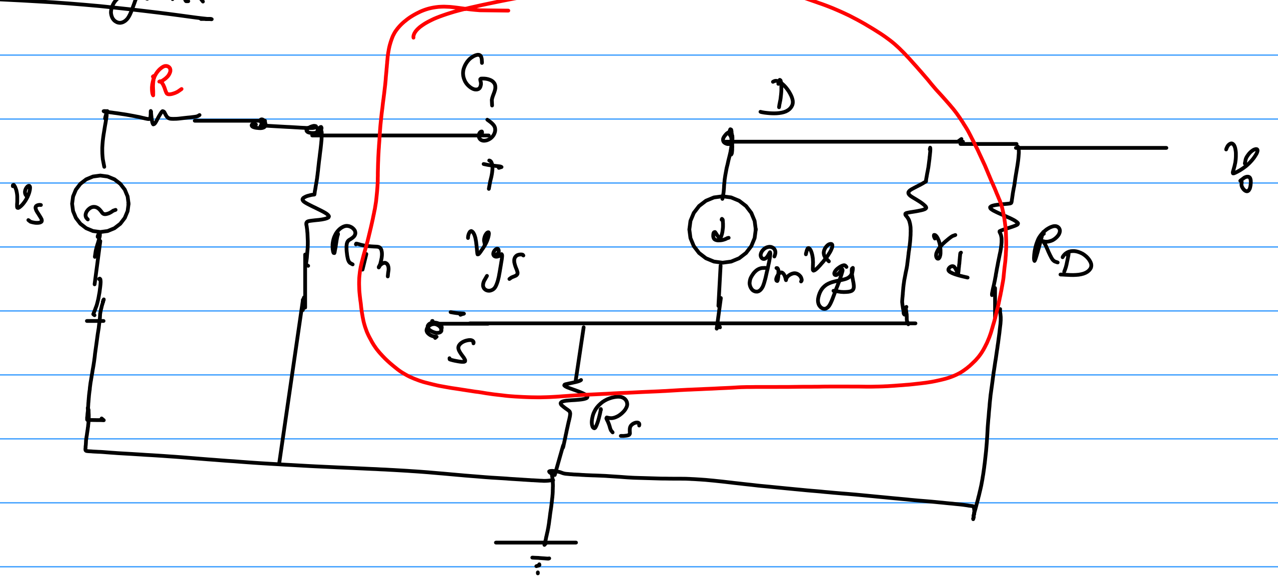
$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D + R_S}$$



$$\underset{\text{(saturation)}}{I_D} = I_{DS} = \underset{\text{given}}{I_{DSS}} \left[1 - \frac{V_{GS}}{\underset{\text{given}}{V_P}} \right]^2$$

Small signal -



HW : MOSFET

Depletion

Enhancement