Total No. of Pages 2

Roll No.....

FOURTH SEMESTER

B.TECH (CO/SE)

END SEMESTER EXAMINATION

(MAY – 2018)

CO/SE-212 COMPUTER SYSTEM & ORGANISATION

Time: 3:00Hours

Max. Marks: 70

Note: Attempt any 5 questions. All questions carry marks.

Assume suitable missing data, if any.

Q1 . (a) Design an array multiplier that multiply two 4-bit numbers. Use AND gates and binary adder.

(b) Differentiate between hard wired control unit and micro programmed control unit with suitable examples

Q2 .(a)What is instruction cycle? Differentiate between direct and indirect address instruction. How many references to memory are nedded for each type of instruction to bring an operand into a processor?

(b) Draw a flow chart for second pass assembler and explain with suitable example.

Q3.(a) Draw a three segment arithmetic pipeline for RISC processors. Differentiate between RISC and CISC processors.

(b) Design and draw a one stage of arithmetic logic shift unit with corresponding function table.

Q4 (a) Define Booth algorithm. Explain step by step multiplication process of (+14)*(+11) using Booth Algorithm.

(b) An instruction is stored at location 300 with its address field at location301.The field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect; (e) indirect with R1 as the index register

Q5 (a) A computer employs RAM chips of 256x8 and ROM chips os 1024x8. The computer system needs 2K bytes of RAM , 4k bytes of ROM, and for interface units, each with four registers. A memory mapped I/O configuration is used. The two highest order bits of the address bus are assigned 00 for RAM , 01 for ROM, and 10 for interface registers.

(i) How many RAM and ROM chips are needed?
(ii) Draw a memory – address map for the system.
(iii) Give the address range in hexadecimal for RAM, ROM and interface

(b) Using two address and zero address instruction format give an assembly language program to evaluate the following expression:

$$X = \frac{A-B+C*(B*E-F)}{G+H*K}$$

Q.6 (a)Design and explain a parallel priority interrupt hardware for a system with eight interrupt sources.

(b) Find the average memory access time if cache hit ratio is 0.9 for read operation. The access time for cache is 100ns and for memory is 8 times that of the cache.

Q.7 Write short notes n the following:

(i) BCD Adder.

(ii) Status Register

(iii)Daisy Chain priority interrupt.

(iv) DMA controller