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FOURTH SEMESTER B.Tech. (COE)

END SEMESTER EXAMINATION *MAY-2018*

CO-206 COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3:00 Hours *Max. Marks: 50*

Note: Answer **ANY FIVE** questions. All questions carry equal marks. Assume suitable missing data, if any.

1[a] Briefly discuss and write the uses of the following:-
i.Multiplexers ii. Counters iii. Registers iv. Decoders

[b] Design a Combinational circuit with three inputs x, y, z and three outputs A, B, C When the input is 0, 1, 2, 3 the output is one greater than the input, and when the input is 4, 5, 6 or 7, the output is one less than the input.

2[a] The following transfer statement specify a memory. Explain the memory operation in each case
1. R2 ← M[AR] 2. M[AR] ← R3 3. R5 ← M[R5]

[b] Register A holds the 8 bit binary 11011001.determine the B operand and logic micro operation to be performed in order to change the value in A to Starting from an initial value 11011101, determine the sequence of binary value in after a logical shift left, followed by circular shift right, followed by a logical shift right and a circular shift left.

3[a] Draw a flow chart for second pass assembler and explain with suitable example.

[b] What is address sequencing? Draw a suitable diagram for " Selection of address for control memory".

4[a] Explain step by step multiplication of (-2) x (-3) using booth's algorithm.

[b] Suppose a cache is 10 times faster than main memory and the cache can be used 90% of the time. How much speedup do we gain by using cache?

5[a] Explain the working of DMA . Why does DMA has priority over CPU? Who request a memory transfer?

[b] What is priority interrupt? Explain parallel priority interrupt technique with the help of block diagram.

6[a] Write a program to evaluate the arithmetic statement $X = (A+B)*(C+D)$

1. Using an accumulator type computer with one address instruction.
2. Using two and three address instructions and
3. Using stack-organised computer with zero address instructions.

[b] What are the various phases of instruction cycle? Draw the flow chart of instruction cycle.

7 Write short note on:-

[a] Storing and non-storing division method

[b] Direct associative memory mappings

[c] Virtual memory

[d] BCD substarctor.

END