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FOURTH SEMESTER B.Tech.[CO/IT/SE]

MID SEMESTER EXAMINATION MARCH-2020

EC262 DIGITAL ELECTRONICS

Time: 1 and 1/2 Hours Max. Marks: 20

Answer All Questions Assume suitable missing data, if any

1. (a) Design Full Subtractor by using two half subtractors and derive the expression also.
   (b) Express the switching circuit shown in the Fig.1. in binary logic notation [3+1]

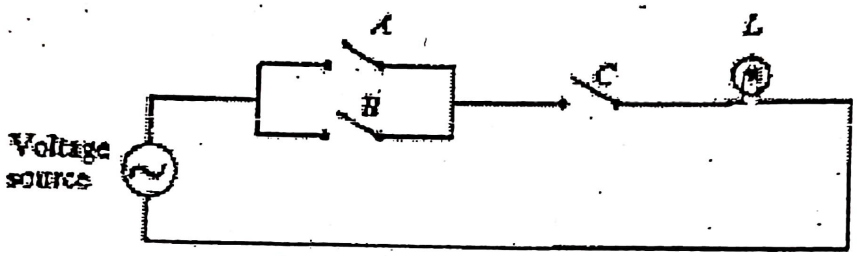

Fig.1.

2. Analyze the two output circuit shown in Fig. 2. Indicate the logic expression associated with every gate output [4]

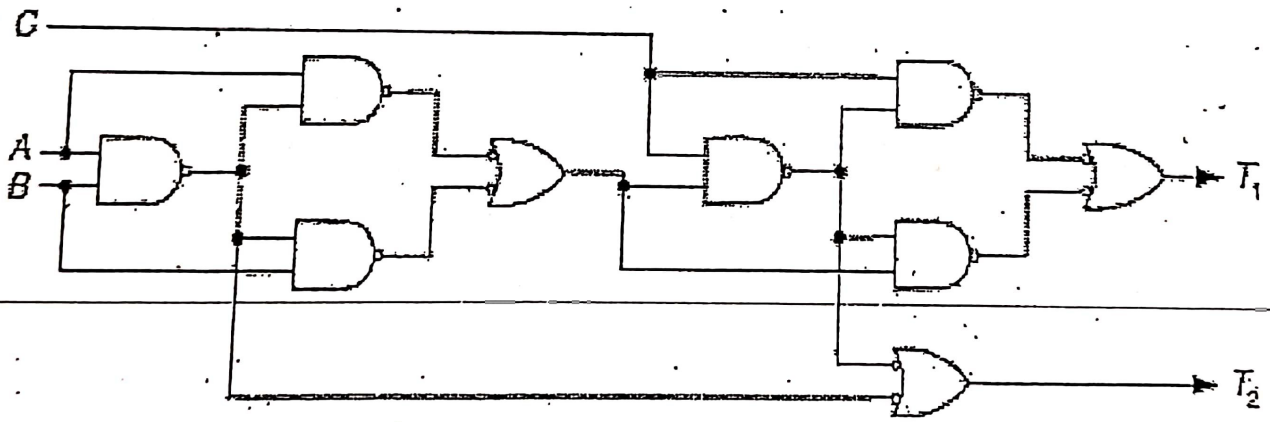

Fig. 2.

3. (a) Implement the Boolean following function by using 8:1 MUX
   $P(QWER)= \pi M(1,2,4,5,9,11,12,15)$
   (b) Minimize the given POS expression by using Karnaugh-Map method $F= \pi M(0,2,3,5,6,10,12)$ with M8, M13, M15 as don't care terms. [2+2]

4. (a) Design a circuit using De-Mux to convert 8421 BCD code to Ex code

(b) If X = 01110 and Y = 11001 are two 5-bit binary numbers represented in two's complement format. Represent the sum of X and Y in two's complement format using 6 bits. [2+2]

5. With neat circuit diagram, explain the working Master Slave JK flip-flop and show that it overcome racing condition. [4]

6. (a) Design a 32:1 Mux using 4:1 mux and a basic gate calculate how many 4:1 Mux are required? [2]

(b) Design an three even parity generator [2]