

Analog Electronics

Unit 1

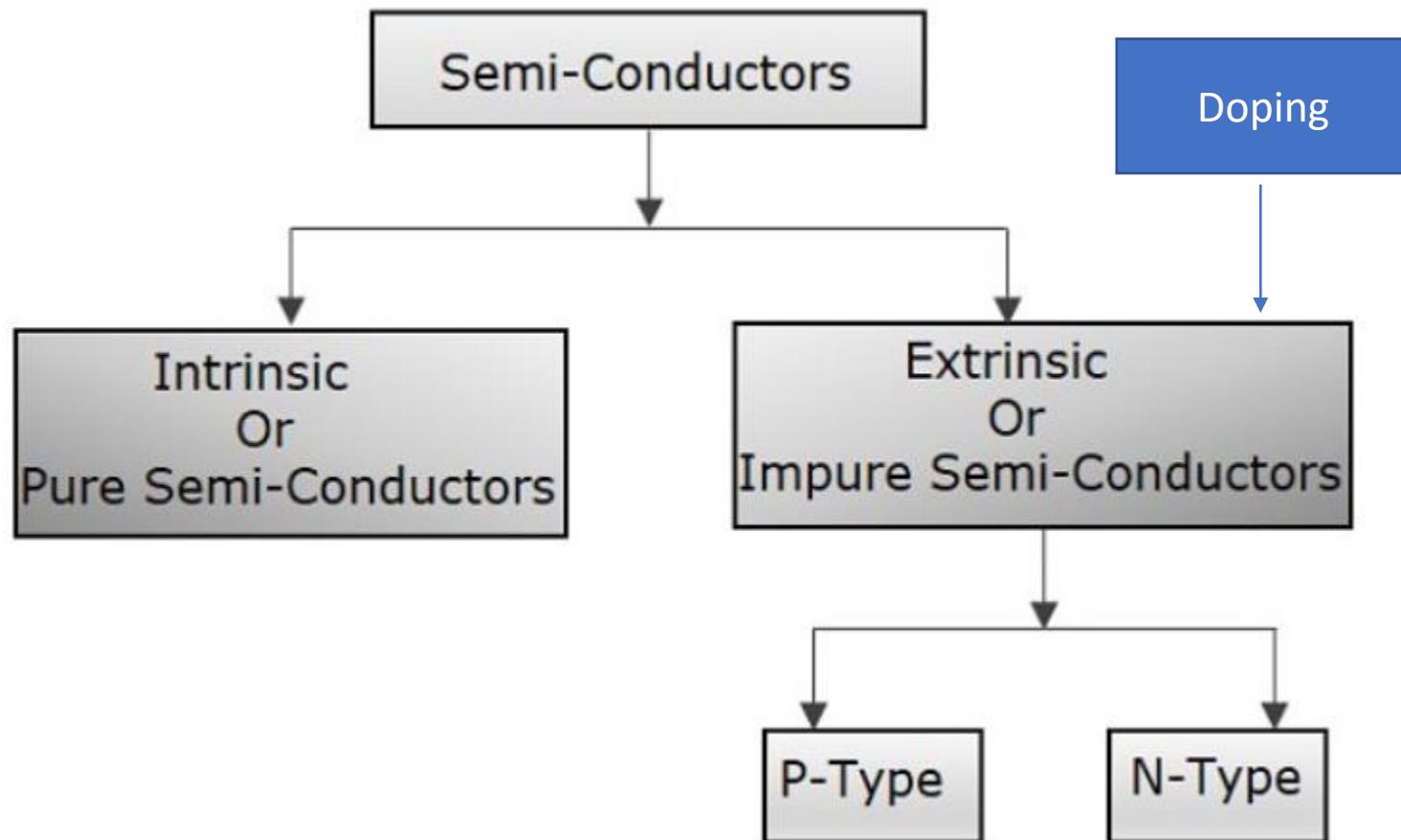
Review of Semiconductors: Energy band structure of Insulator, Semiconductor and Metal, Intrinsic and extrinsic semiconductor.

P-NJunction Diodes, and its application:, clipping and clamping circuits, Rectifiers and filters, Zener diode and regulators.

Semiconductors

- A **semiconductor** is a substance whose resistivity lies between the conductors and insulators.
 - Semiconductors have the resistivity which is less than insulators and more than conductors.
 - Semiconductors have **negative temperature co-efficient**.
 - The **resistance** in semiconductors, **increases with the decrease in temperature** and vice versa.
 - The **Conducting properties** of a Semiconductor **changes**, when a **suitable metallic impurity is added** to it, which is a very important property

Classification of semiconductors



Conduction in Semiconductors

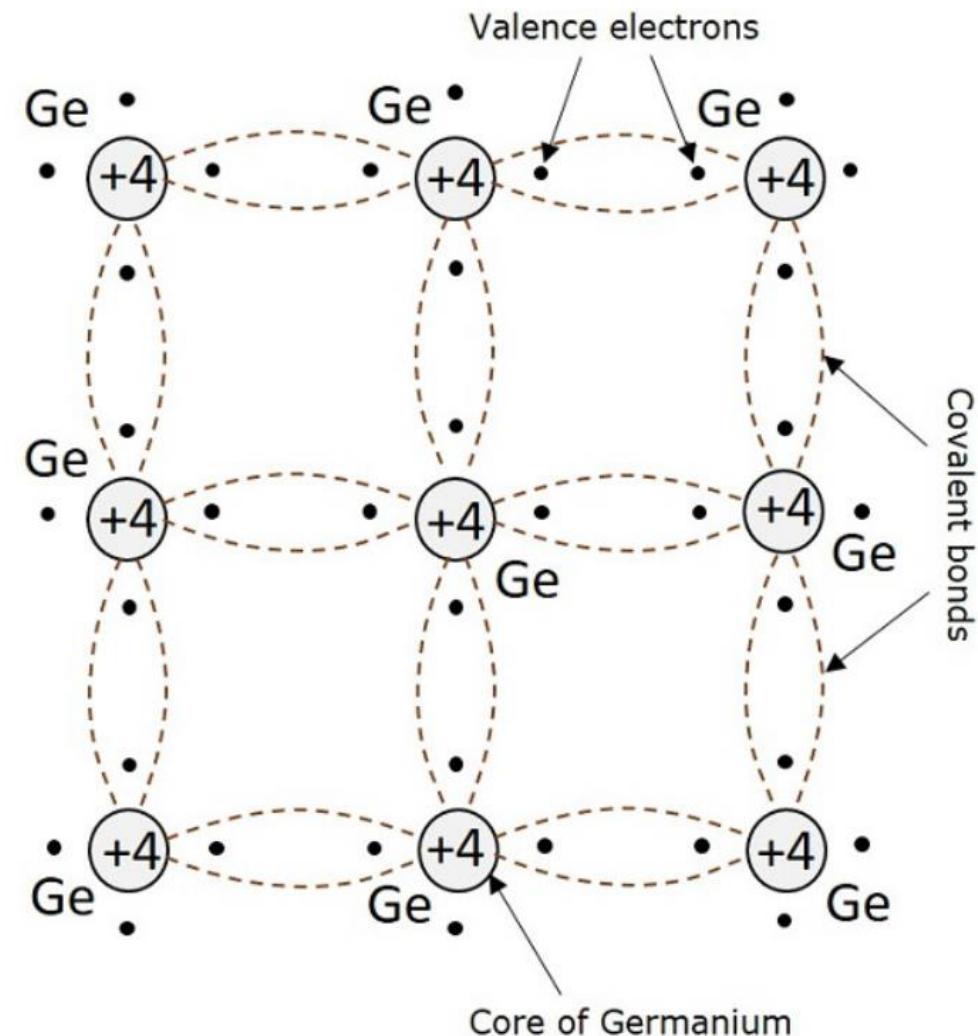
- **Valence electrons:** The outermost shell has the electron which are loosely attached to the nucleus
- Such an atom, having valence electrons when brought close to the other atom, the valence electrons of both these atoms combine to form “**Electron pairs**”
- This bonding is not so very strong and hence it is a **Covalent bond (Sharing)**

Germanium

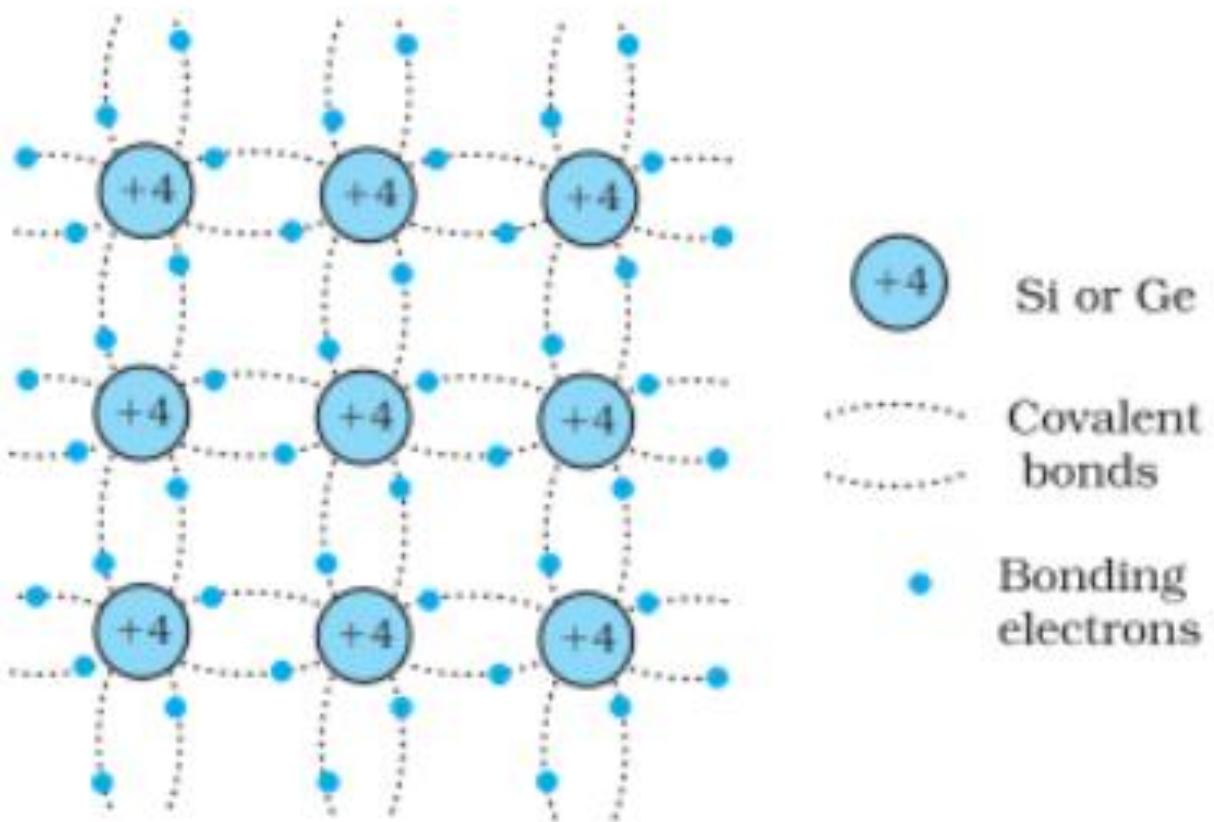
Electronic configuration:

2 (First orbit), 8, 18,
4 (Last orbit) (Valence els)

Stable Ge (8 els)



Hole generation and movement

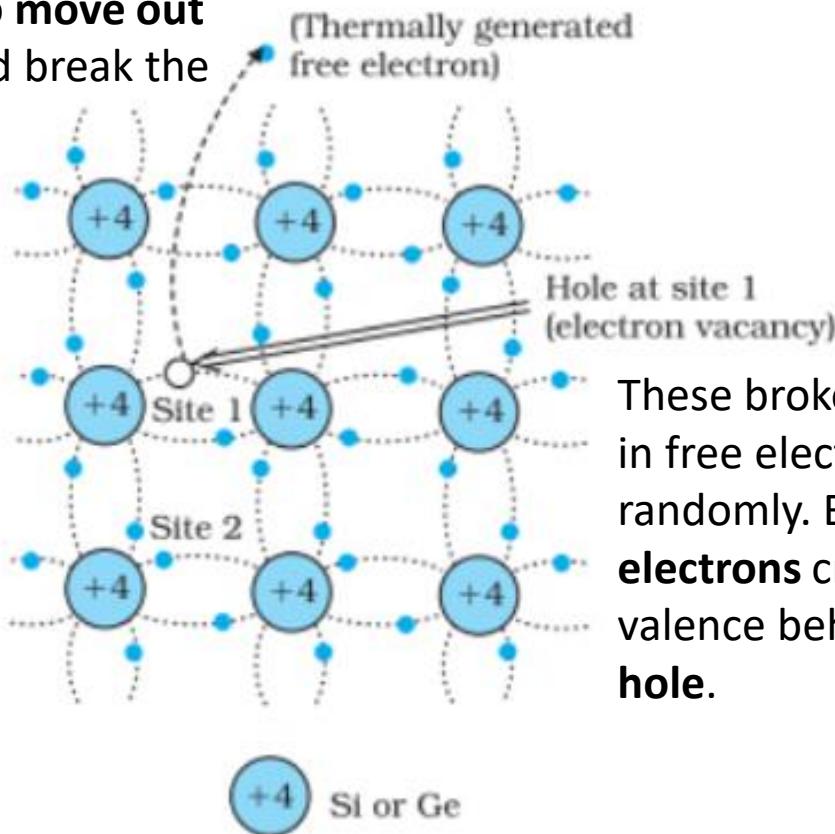


Schematic two-dimensional representation of Si or Ge structure showing covalent bonds at low temperature (all bonds intact). +4 symbol indicates inner cores of Si or Ge.

Cont.

Temperature (E₁-E₂)

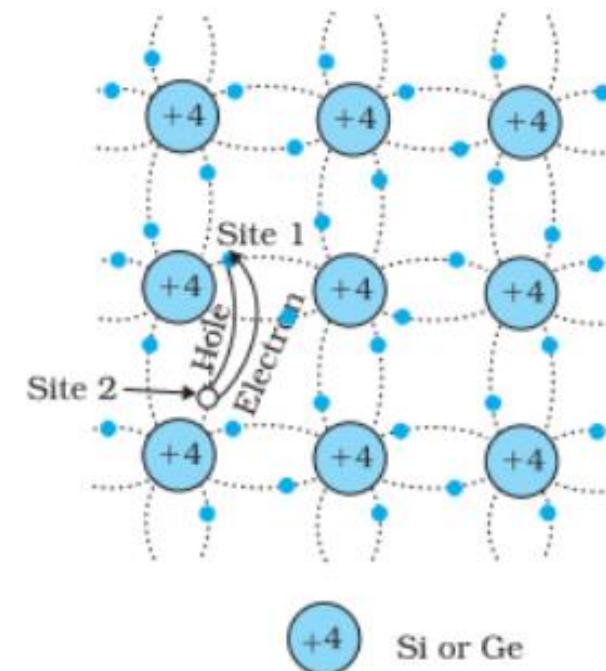
thermal energy
in the crystal, some
tend to move out
valence and break the
bonds.



(Higher Energy level)CB (Max Freedom) E₁

(Lower Energy level)VB (Bonded) E₂

This **hole** which represents a **missing electron** can be considered as a **unit positive charge** while the electron is considered as a unit negative charge.



model of generation of hole at site 1 and conduction electron due to thermal energy at moderate temperatures.

Simplified representation of possible thermal motion of a hole. The electron from the lower left hand covalent bond (site 2) goes to the earlier hole site 1, leaving a hole at its site indicating apparent movement of the hole from site 1 to site 2.

Current in semiconductor

Under an electric field, these holes move towards the negative potential generating hole current (I_h). Hence, the total current (I) is:

$$I = I_e + I_h$$

Cont.

Electron-hole generation and recombination

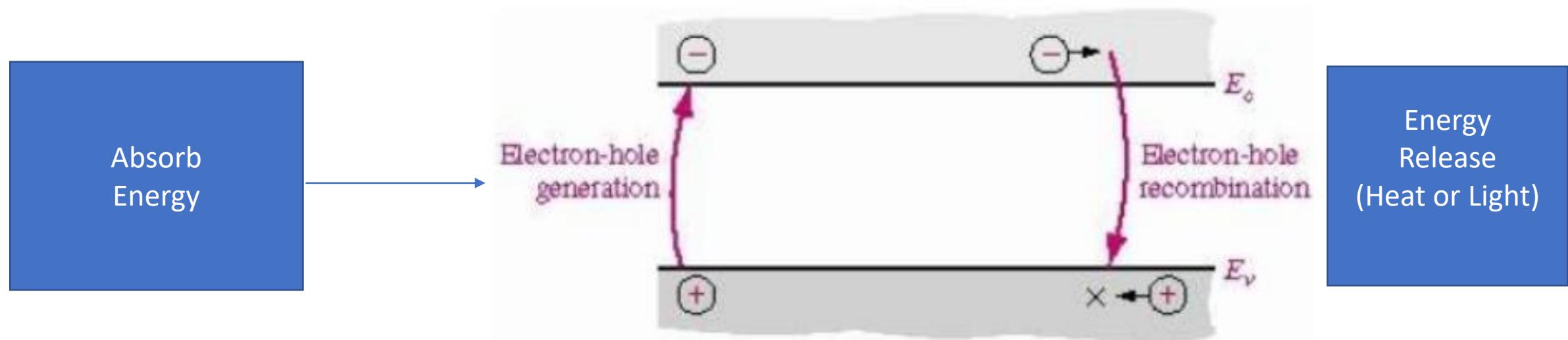
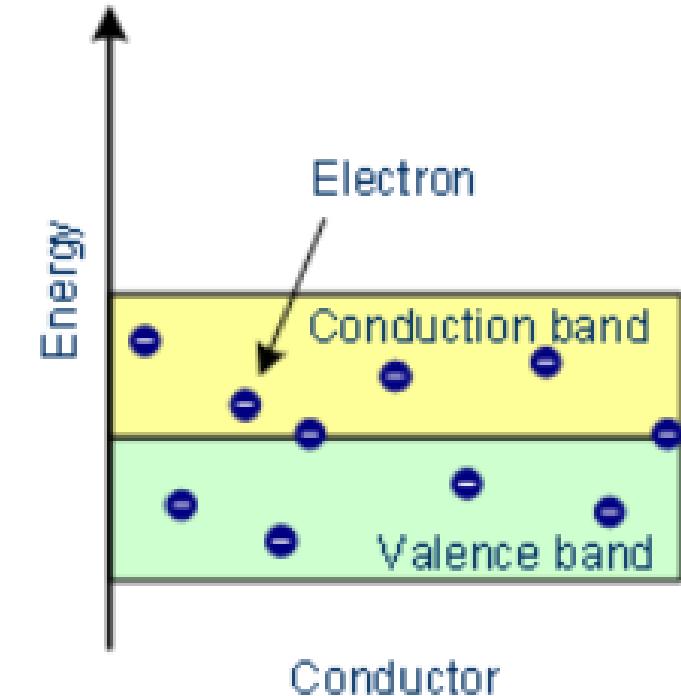
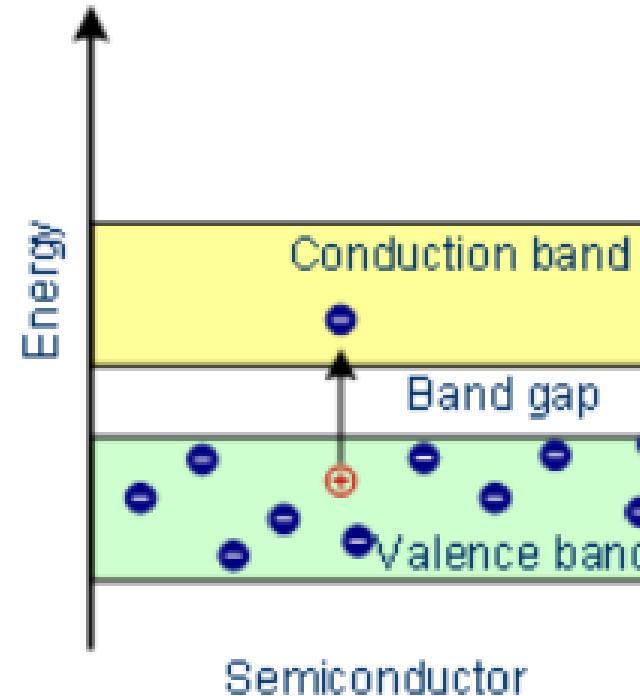
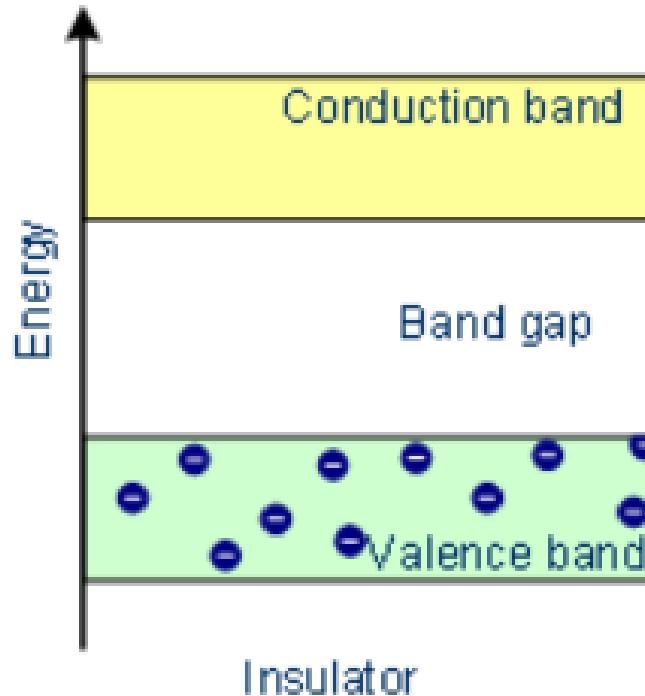


Figure 6.1 | Electron-hole generation and recombination.

In the **steady state**, the **thermal generation rate is balanced by the recombination rate**

Energy band structure of Insulator, Semiconductor and Metal



Intrinsic Semiconductors

- A Semiconductor in its extremely **pure form** is said to be an **intrinsic semiconductor**.
- The properties of this pure semiconductor are as follows –
 - The **electrons and holes are solely** created by **thermal excitation**.
 - The number of free **electrons is equal** to the number of **holes**.
 - The **conduction capability is small** at room temperature.
- In order to **increase** the **conduction** capability of intrinsic semiconductor, it is better to add some impurities.
- This process of adding impurities is called as **Doping**.
- Now, this **doped intrinsic semiconductor** is called as an **Extrinsic Semiconductor**

Doping

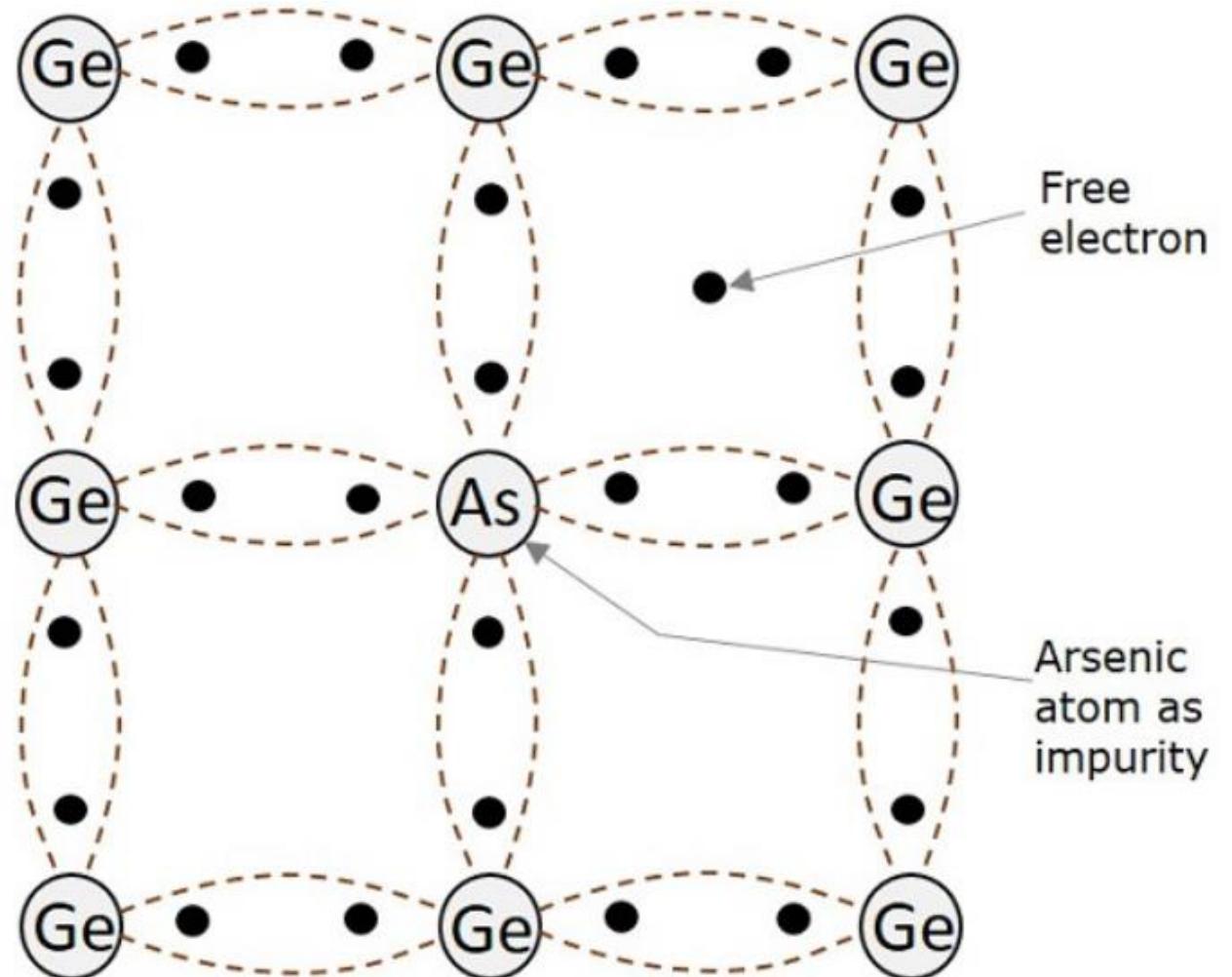
- Generally pentavalent and trivalent impurities
- **Pentavalent Impurities**
 - The **pentavalent** impurities are the ones which has **five valence electrons** in the outer most orbit. Example: Bismuth, Antimony, Arsenic, Phosphorus
 - The pentavalent atom is called as a **donor atom** because it **donates one electron to the conduction band** of pure semiconductor atom.
- **Trivalent Impurities**
 - The **trivalent** impurities are the ones which has **three valence electrons** in the outer most orbit. Example: Gallium, Indium, Aluminum, Boron
 - The trivalent atom is called as an **acceptor atom** because it accepts one electron from the semiconductor atom.

Extrinsic Semiconductor

- An impure semiconductor, which is formed by doping a pure semiconductor is called as an **extrinsic semiconductor**.
- There are two types of extrinsic semiconductors depending upon the type of impurity added.
- They are **N-type extrinsic semiconductor** and **P-Type extrinsic semiconductor**.

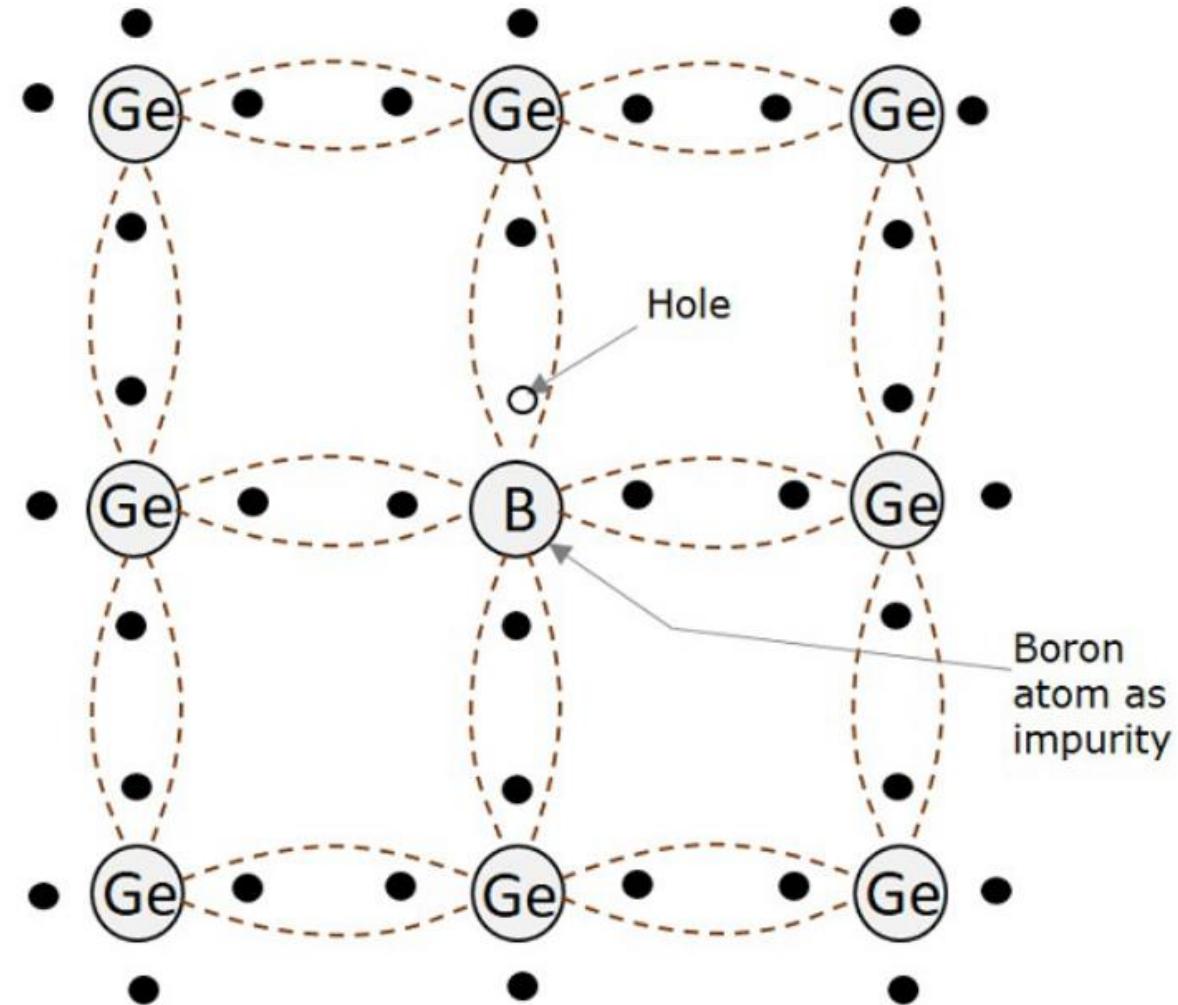
N-Type Extrinsic Semiconductor

- **N-type extrinsic semiconductor:** Conduction takes place through electrons, the **electrons are majority carriers**, and the **holes are minority carriers**.
- As there is no addition of positive or negative charges, the electrons are electrically neutral



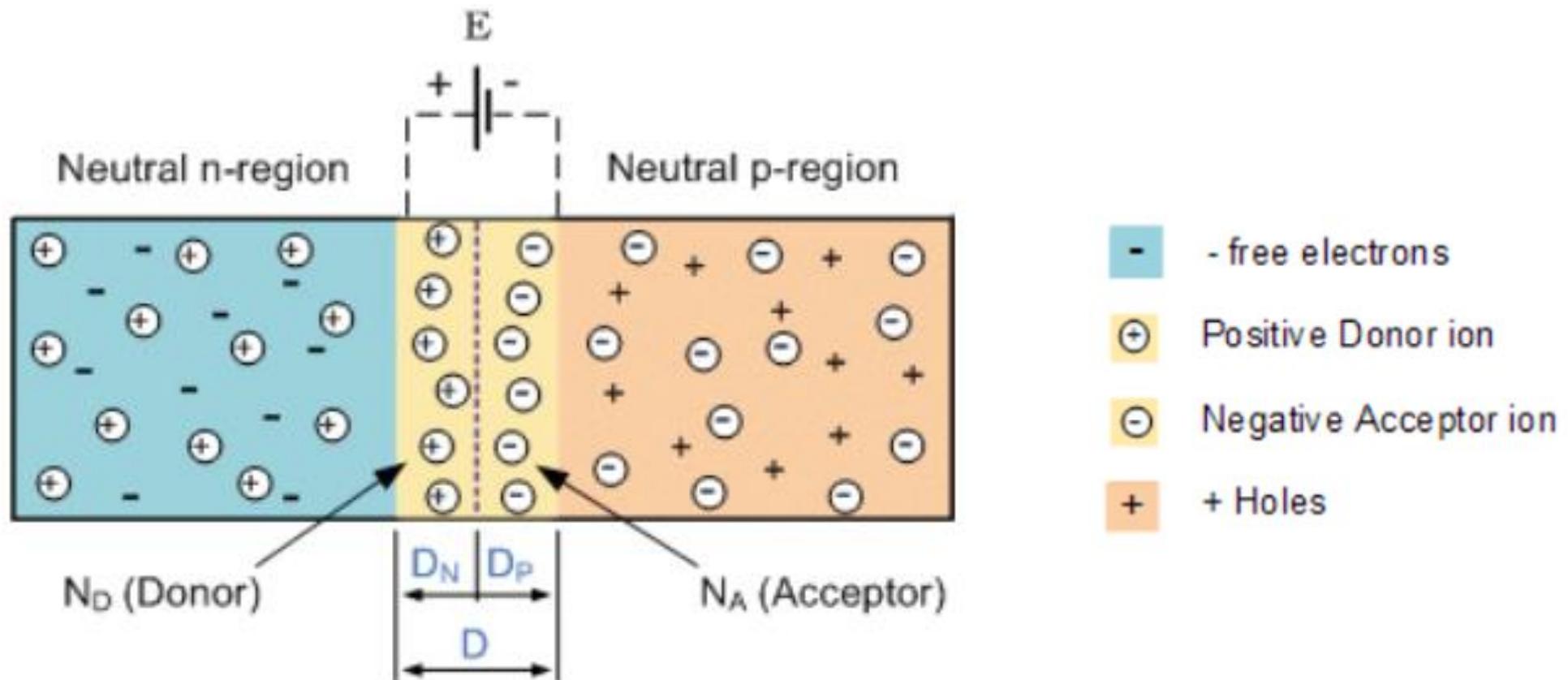
P-Type Extrinsic Semiconductor

- **P-type extrinsic semiconductor:** conduction takes place through holes; the **holes are majority carriers** while the **electrons are minority carriers**.
- The impurity added here provides holes which are called as **acceptors**, because they **accept electrons from the germanium atoms**.
- As the number of mobile holes remains equal to the number of acceptors, the P-type semiconductor remains electrically neutral.
- In this P-type conductivity, the **valence electrons move from one covalent bond to another**, unlike N-type

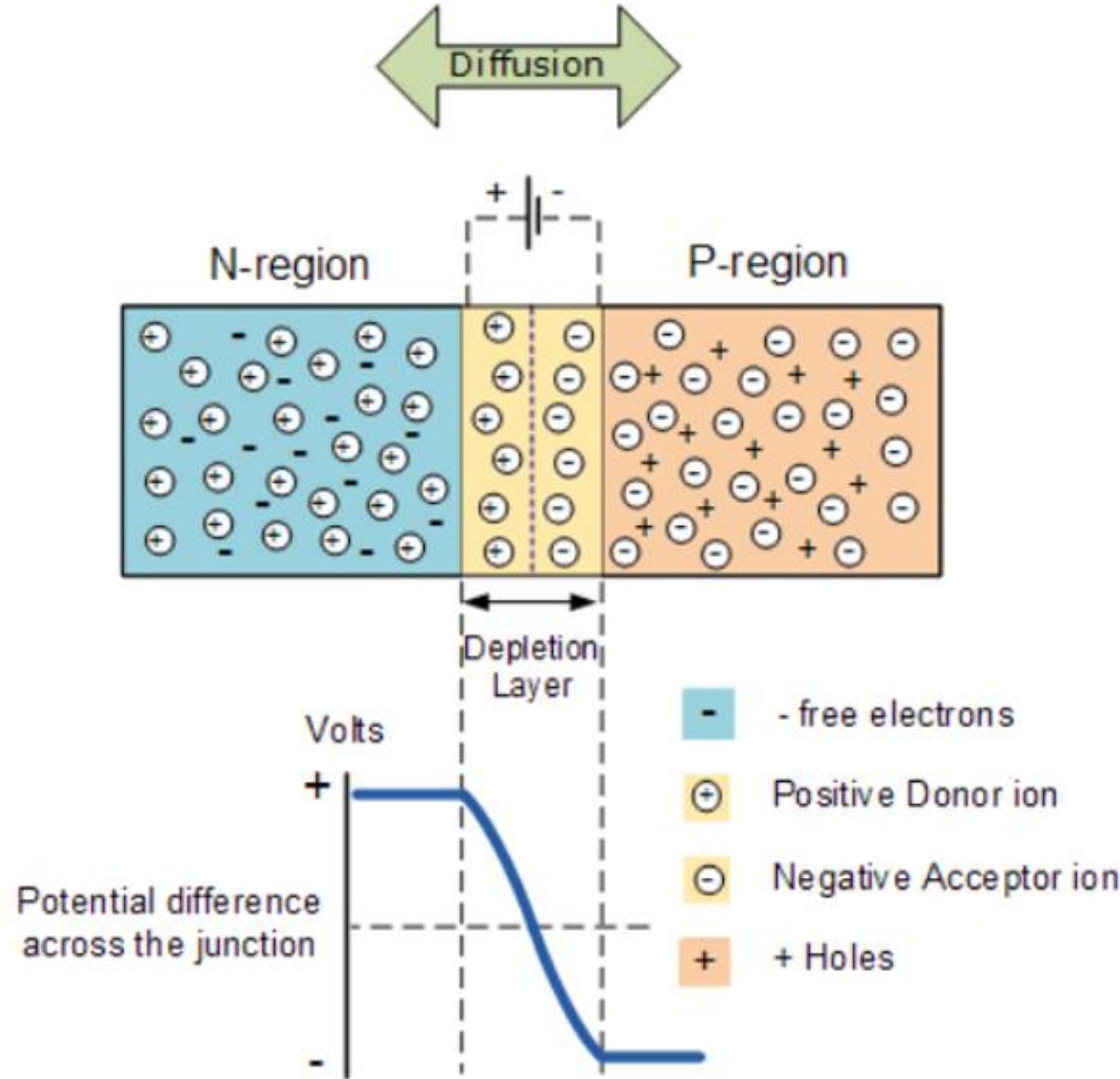


P-N Junction Diode

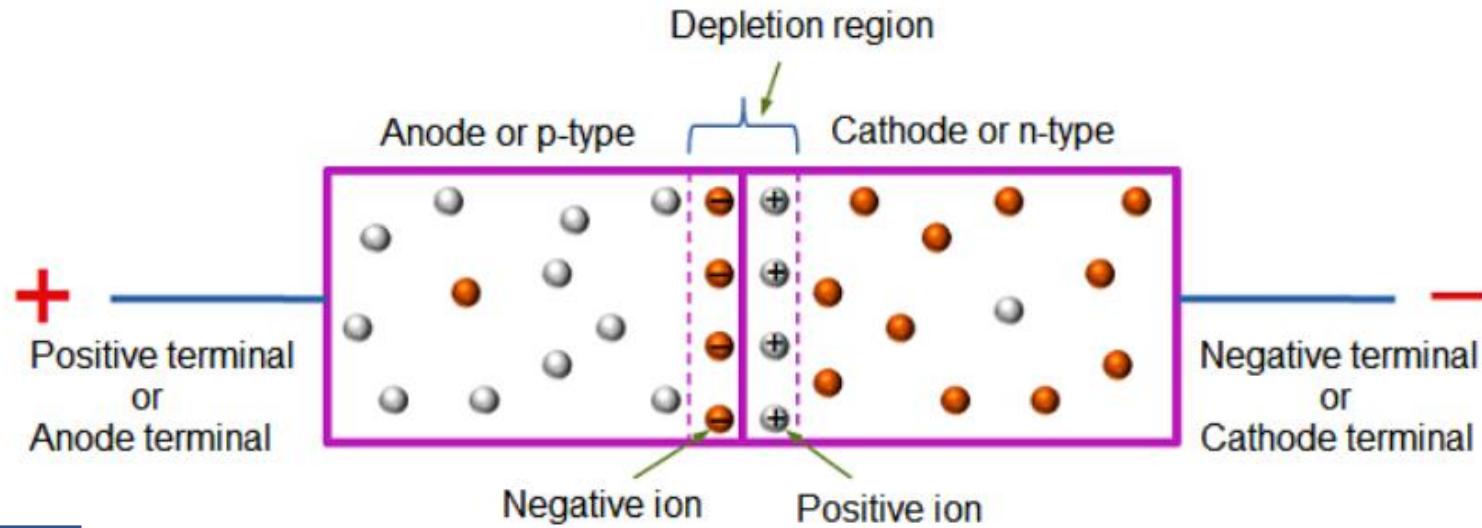
- A p-n junction diode is two-terminal or two-electrode semiconductor device, which allows the electric current in only one direction while blocks the electric current in opposite or reverse direction.



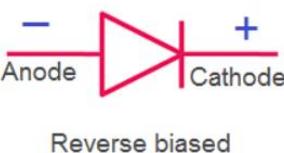
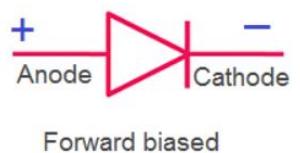
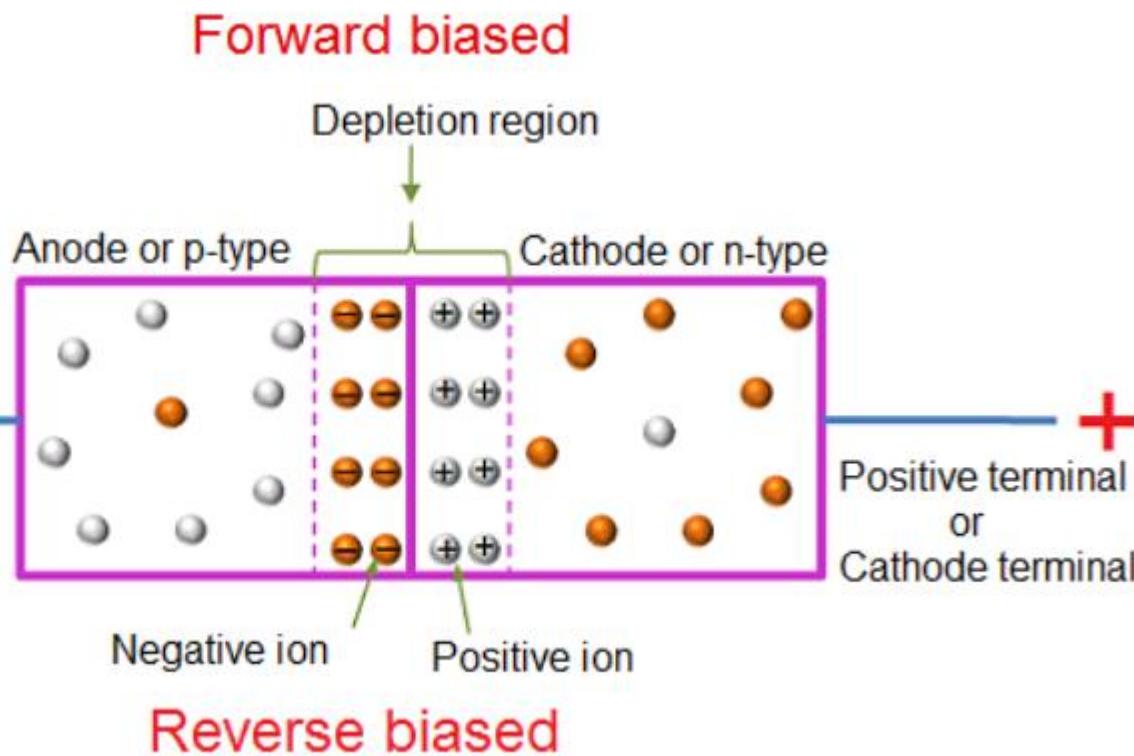
PN Junction



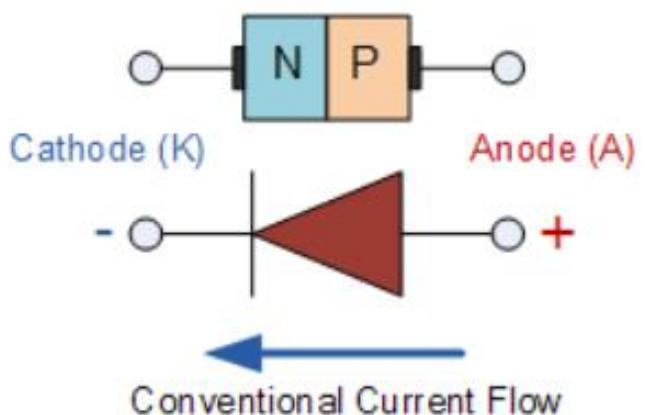
PN Junction biasing



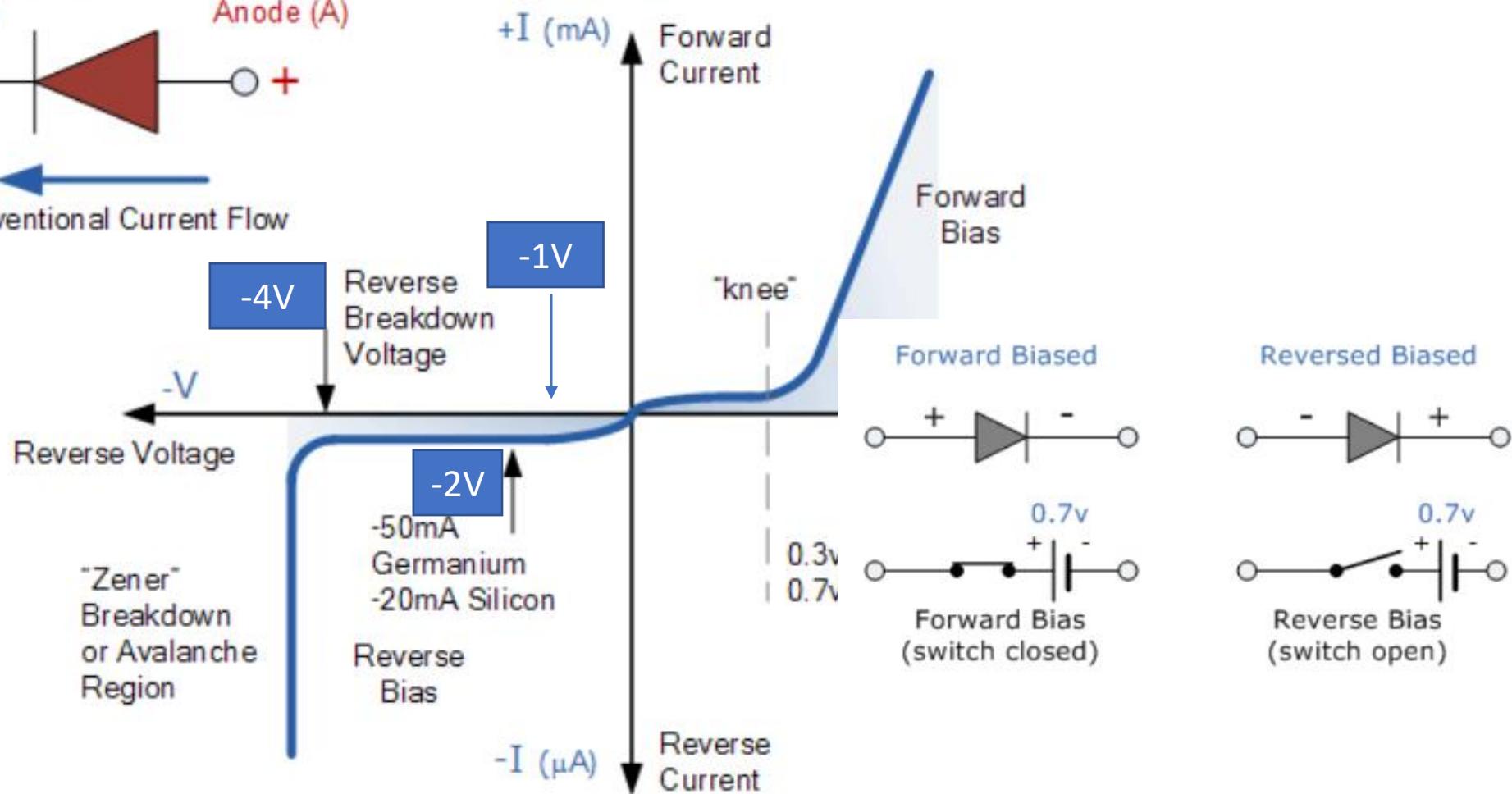
Higher Force = 1el and 1Hole
(KE) = A = EHP (KE) =A =
EHP(KE) = Sufficient Charges
= Current



PN Junction Diode V-I Characteristics

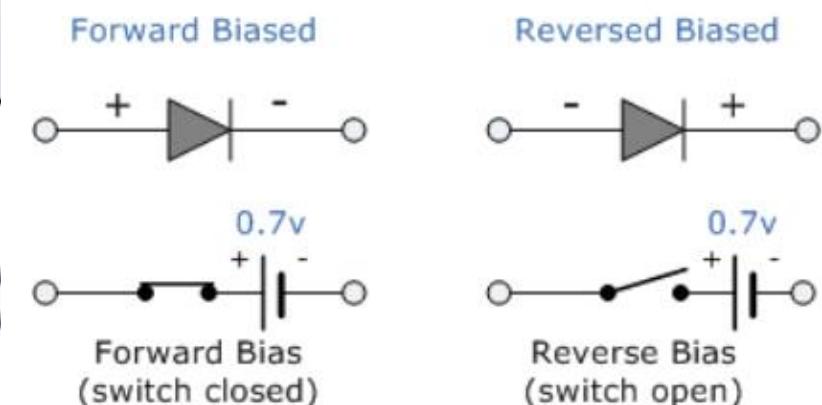


**Higher Force = 1el and
1 Hole (KE) = A = EHP (KE)
= A = EHP(KE) = Sufficient
Charges = Current**



$$E = -dV_r / dx$$

$$F = qE$$

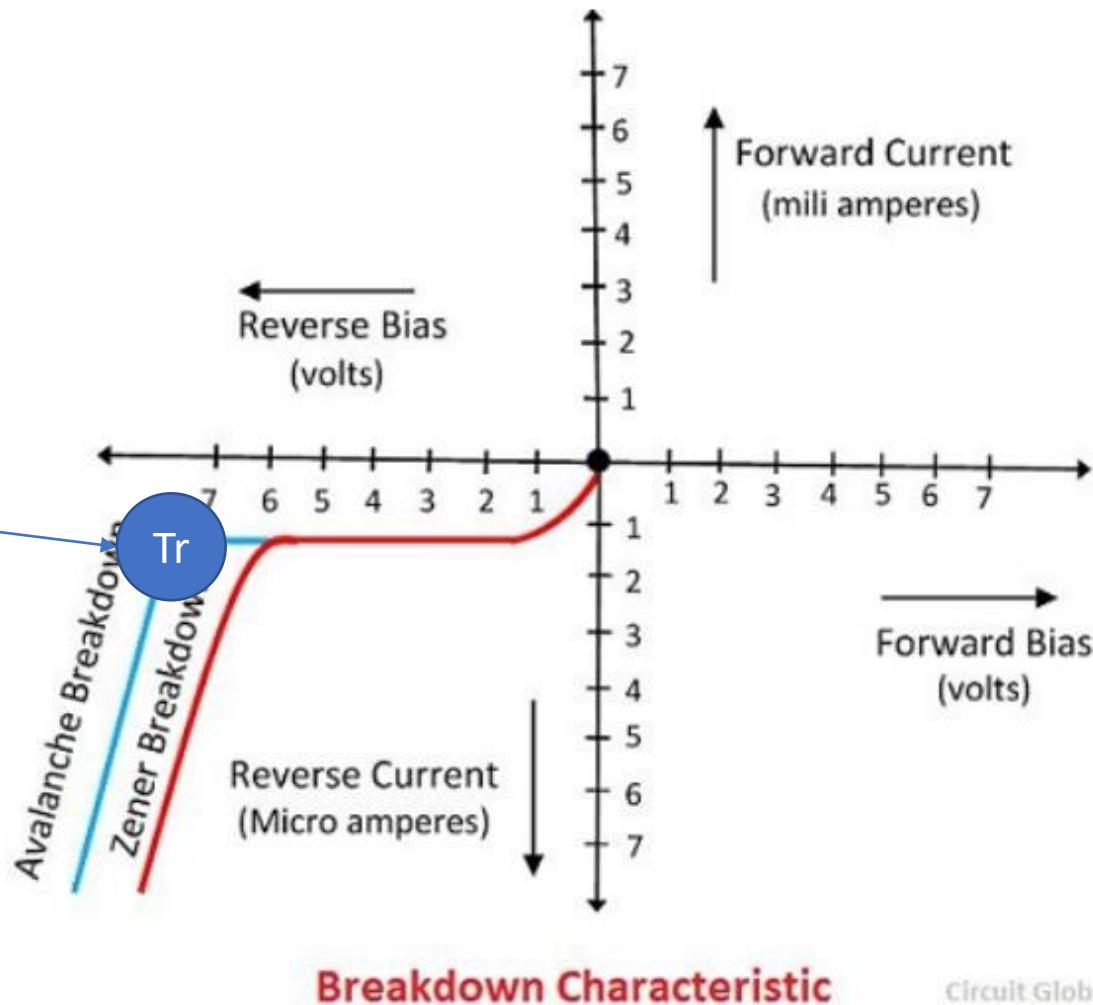


Breakdown

Breakdown Characteristic Graph

The graphical representation of the Avalanche and Zener breakdown is shown in the figure below.

Multiplicative Action (Chain reaction)

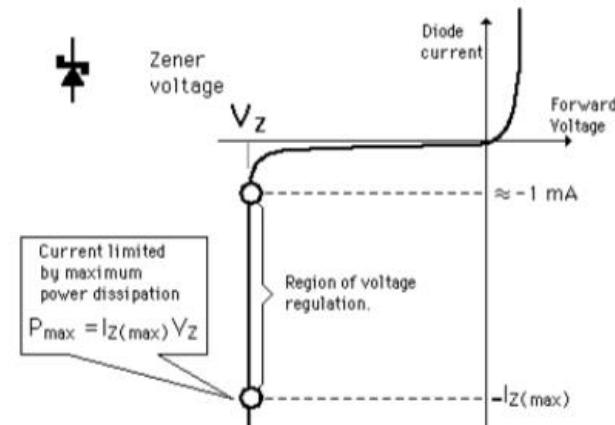


What is Breakdown?

- Deleterious effect that occurs in the presence of high electric field.
- Causes high resistance elements to allow flow of high current.

Avalanche/Zener Breakdown

- 'Zener diode' and 'avalanche diode' are terms often used interchangeably.
- Both refer to breakdown of a diode under reverse bias.



Avalanche/Zener Breakdown (con't)

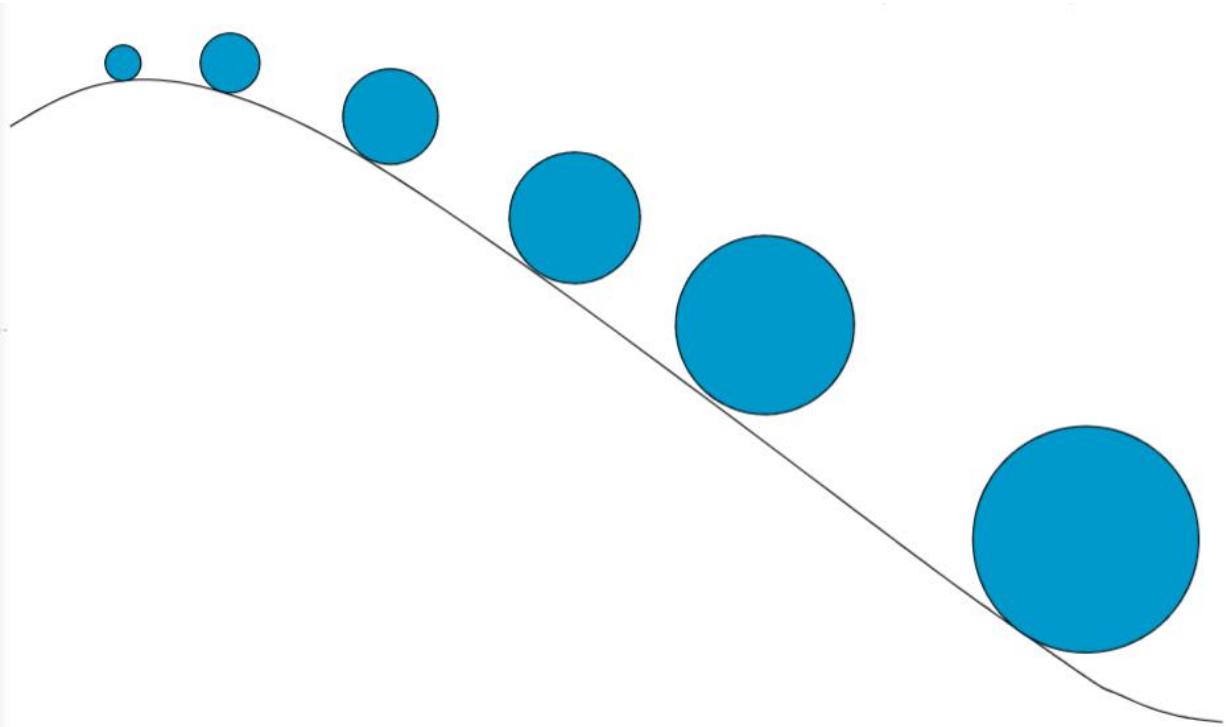
- **Reverse bias** = Very little current flow
= Open circuit

- As Reverse voltage ↑ a point is reached where current ↑ dramatically, therefore dynamic resistance ↓.
 - ➡ Very few electrons make it through depletion region with high velocity
 - ➡ These electrons collide with atoms in the depletion region and free more electrons (Process called Multiplication).
 - ➡ Results in higher and higher current flow

Avalanche Breakdown (con't)



By analogy, the process is named because a single carrier can spawn literally thousands of additional carriers through collisions, just as a single snowball can cause an avalanche.

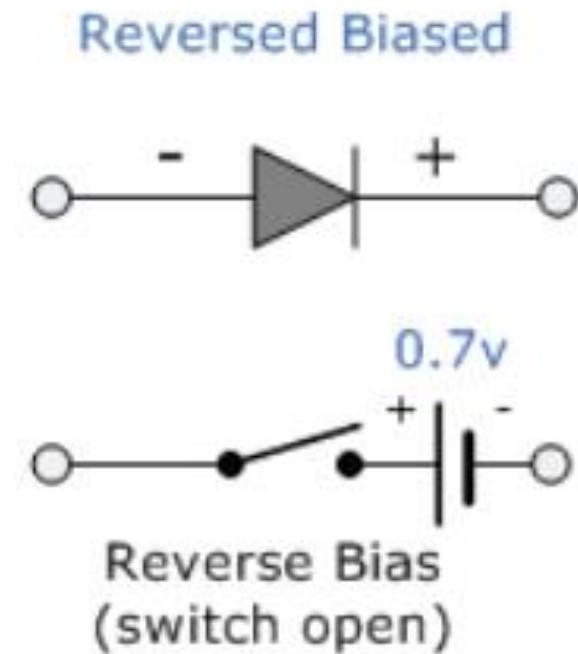
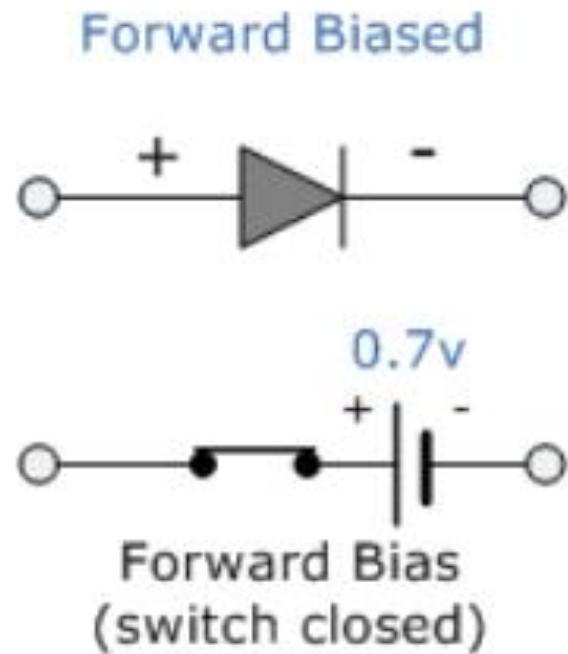


Zener Breakdown ($DR = 1:10^4$) ND($1:10^8$)

- The **width of the depletion region** depends on the **doping** of the P and N-type semiconductor material.
- If the material is **heavily doped**, the **width of the depletion region** becomes **very thin**.
- The phenomenon of the **Zener breakdown** occurs in the **very thin depletion region**.
- The thin depletion region has more numbers of free electrons. The reverse bias applies across the PN junction develops the electric field intensity across the depletion region.
- The **strength of the electric field intensity** becomes **very high**.

P-N Junction Diodes application

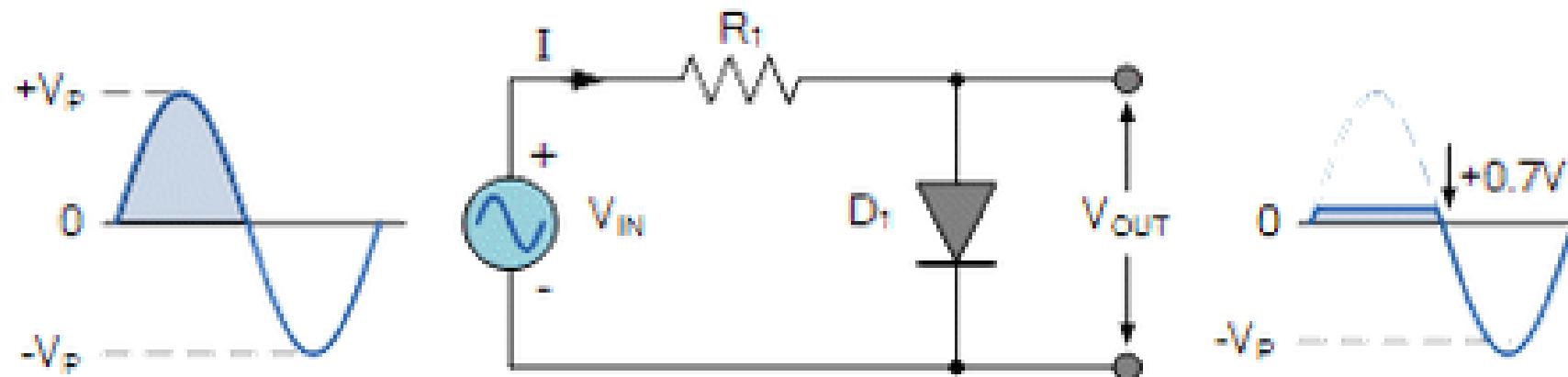
- Clipping and clamping circuits
- Rectifiers
- Filters
- Zener diode and regulators



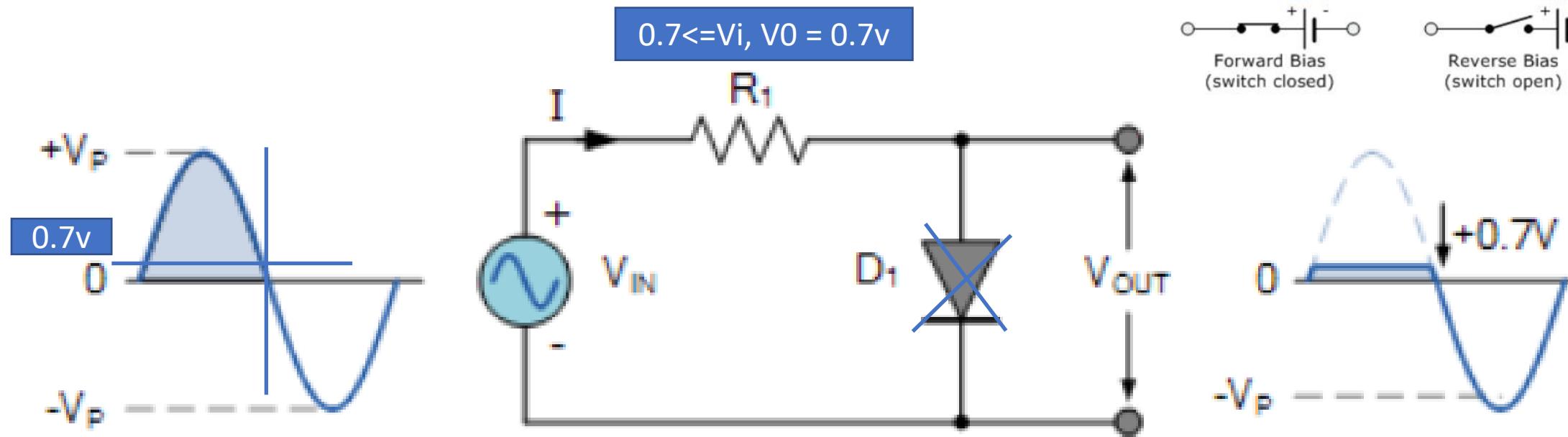
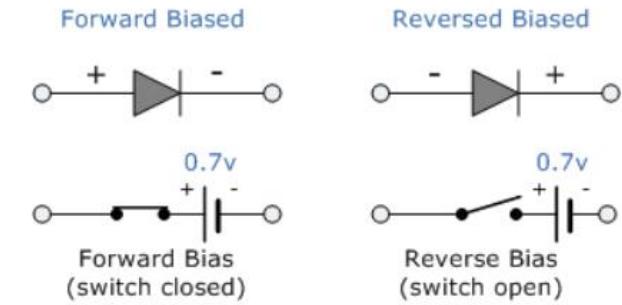
Clipping and clamping circuits (Clipper and Clamper)

Diode Clipping Circuits

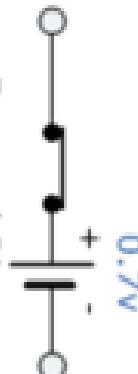
The **Diode Clipper**, also known as a *Diode Limiter*, is a **wave shaping circuit** that takes an input waveform and **clips or cuts off** its top half, bottom half or both halves together.



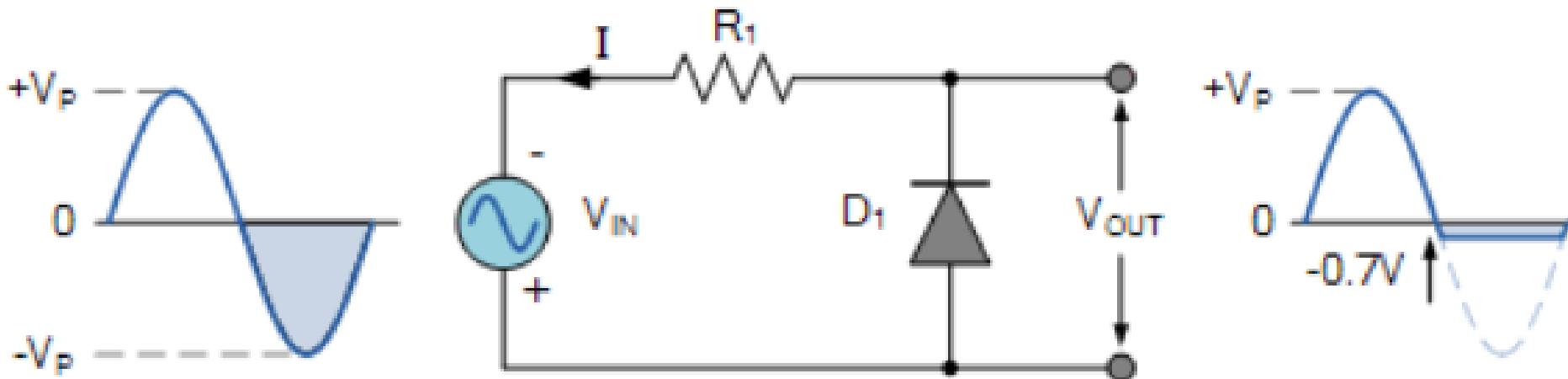
Positive Diode Clipping Circuits



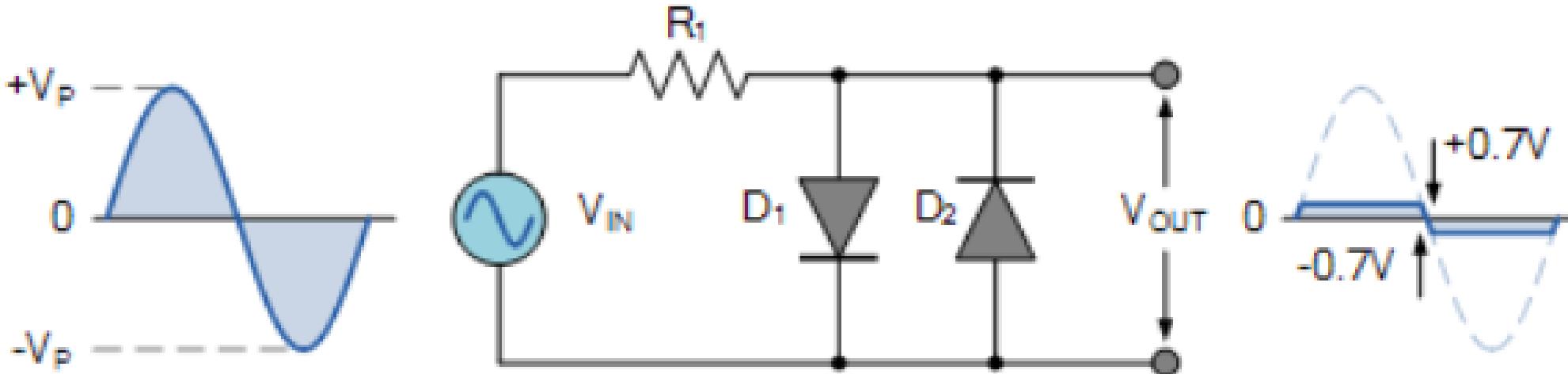
- In +ve cycle when IP voltage is greater than the 0.7(si) and 0.3ge the diodes begins to conduct and holds the voltage across itself constant at 0.7V until the sinusoidal waveform falls below this value.
- Thus the output voltage which is taken across the diode **can never exceed 0.7 volts** during the **positive half cycle**.



Negative Diode Clipping Circuits



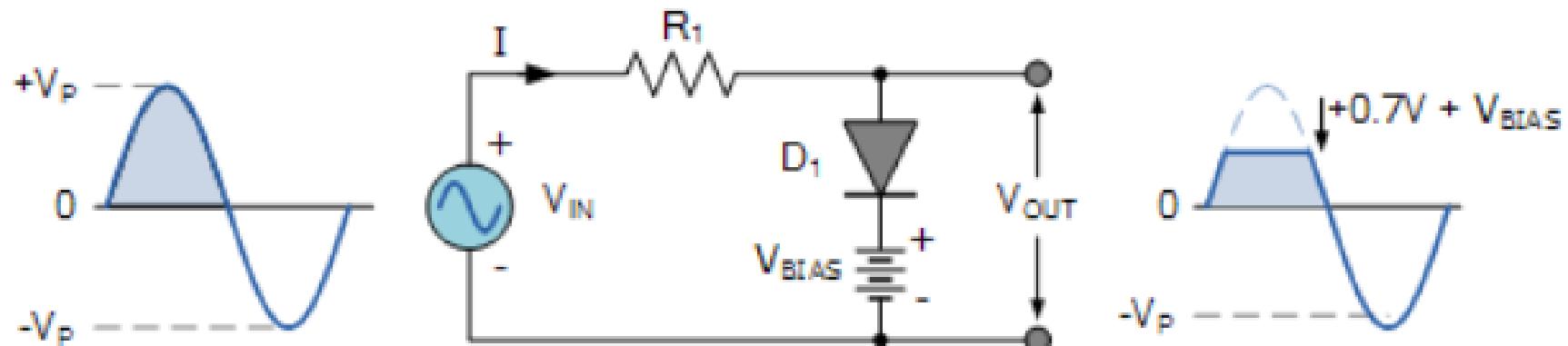
Clipping of Both Half Cycles



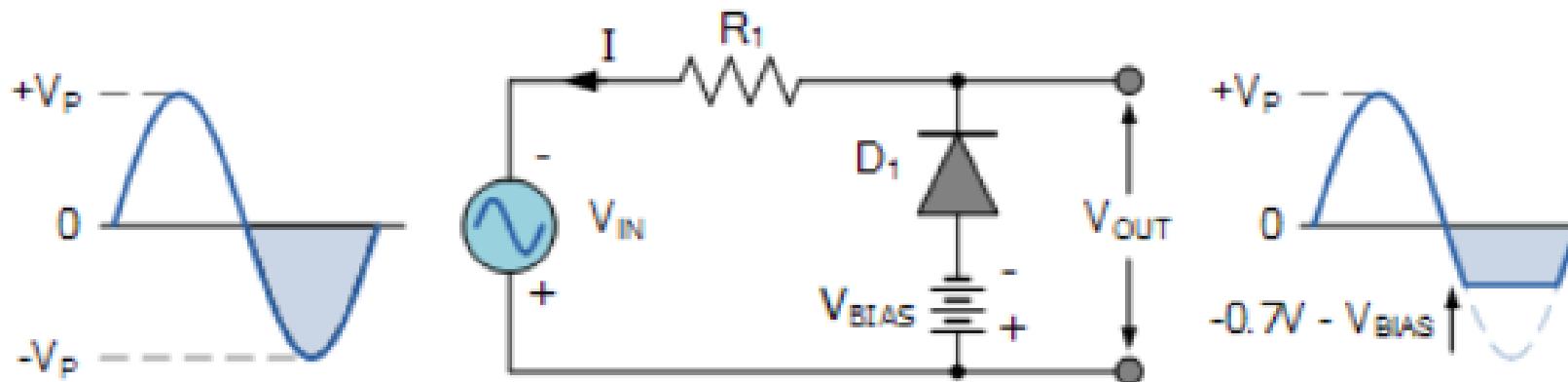
Biased Diode Clipping Circuits

To produce diode clipping circuits for **voltage waveforms at different levels**, a bias voltage, V_{BIAS} is added in series with the diode to produce a combination clipper as shown.

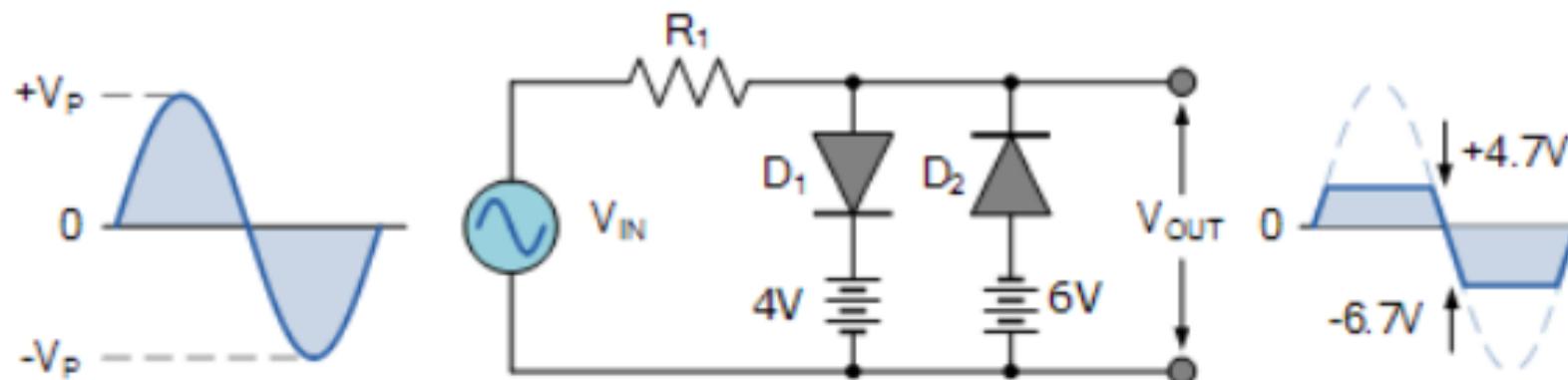
Positive Bias Diode Clipping



Negative Bias Diode Clipping

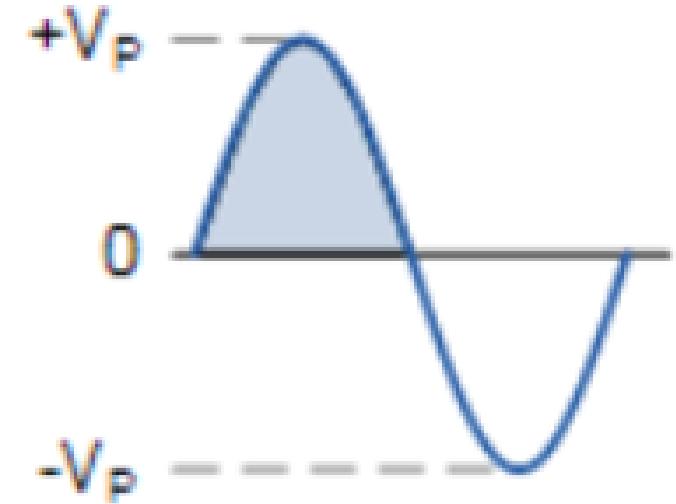


Diode Clipping of Different Bias levels



Clamper Circuits

- A Clamper Circuit is a circuit that **adds a DC level** to an **AC signal**.
- The positive and negative peaks of the signals can be placed at desired levels using the clamping circuits.
- As the DC level gets shifted, a clamper circuit is called as a **Level Shifter**.
- Clamper circuits consist of energy storage elements like **capacitors**. A simple clamper circuit comprises of a **capacitor, a diode, a resistor and a dc battery** if required.

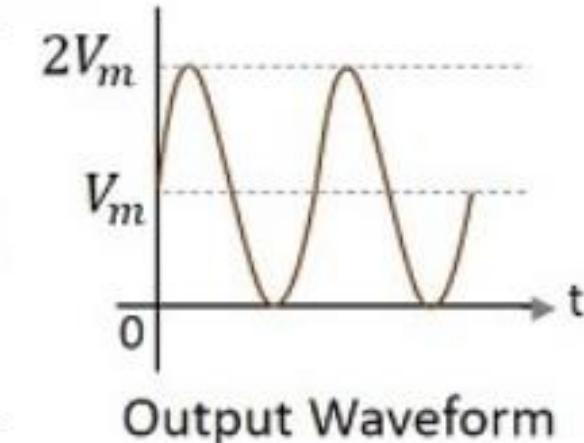
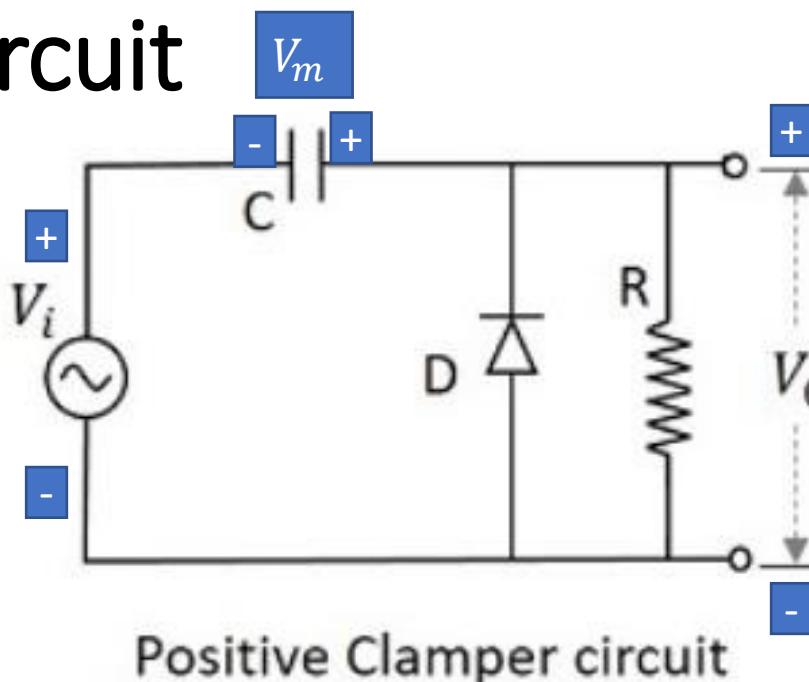
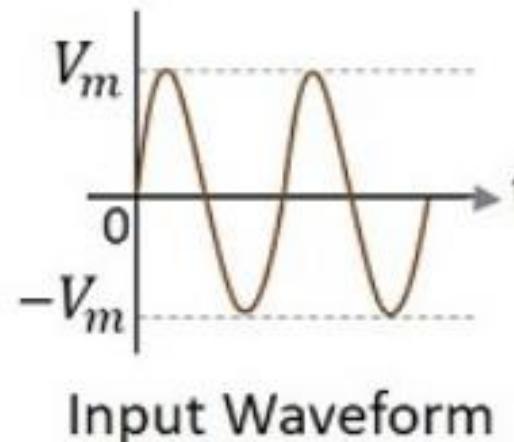


Types of Clampers

There are few types of clamper circuits, such as

- Positive Clamper
- Positive clamper with positive V_r
- Positive clamper with negative V_r
- Negative Clamper
- Negative clamper with positive V_r
- Negative clamper with negative V_r

Positive Clamper Circuit



$$+ - = - +$$
$$V_o = V_i + V_m$$

In order to maintain the time period of the wave form, the **tau** must be greater than, half the time period
Discharging time of the capacitor should be slow.

Where

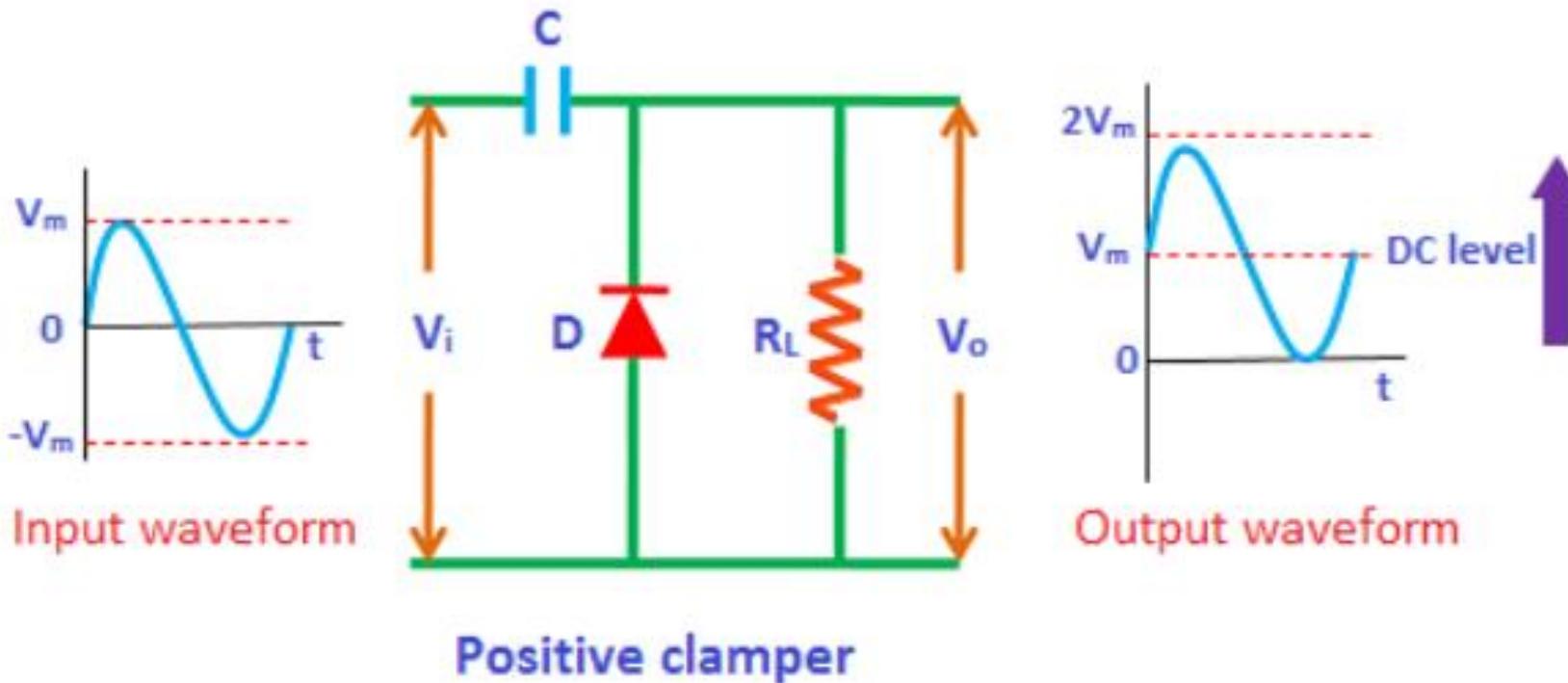
$$\tau = R C$$

- R is the resistance of the resistor employed
- C is the capacitance of the capacitor used

$$V_o = V_i + V_m$$

$$\begin{aligned} V_i &= 0 & V_o &= V_m, \\ V_i &= V_m & V_i &= V_m \\ V_o &= 2V_m & V_i &= -V_m \\ V_o &= 0 & V_o &= 0 \end{aligned}$$

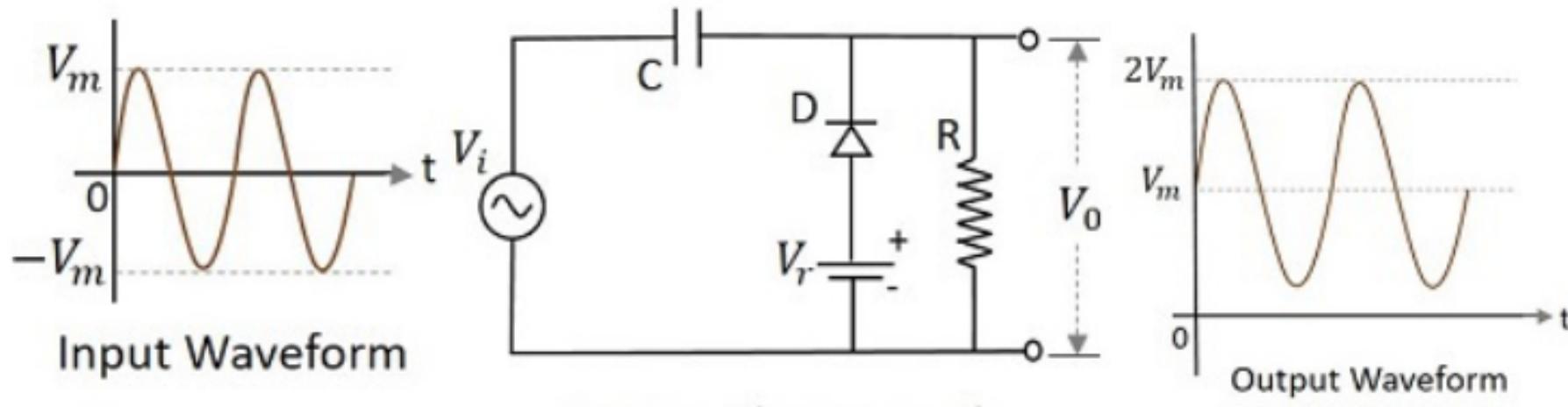
Cont.



Biased Clamper

Positive Clamper with Positive V_r

A Positive clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.

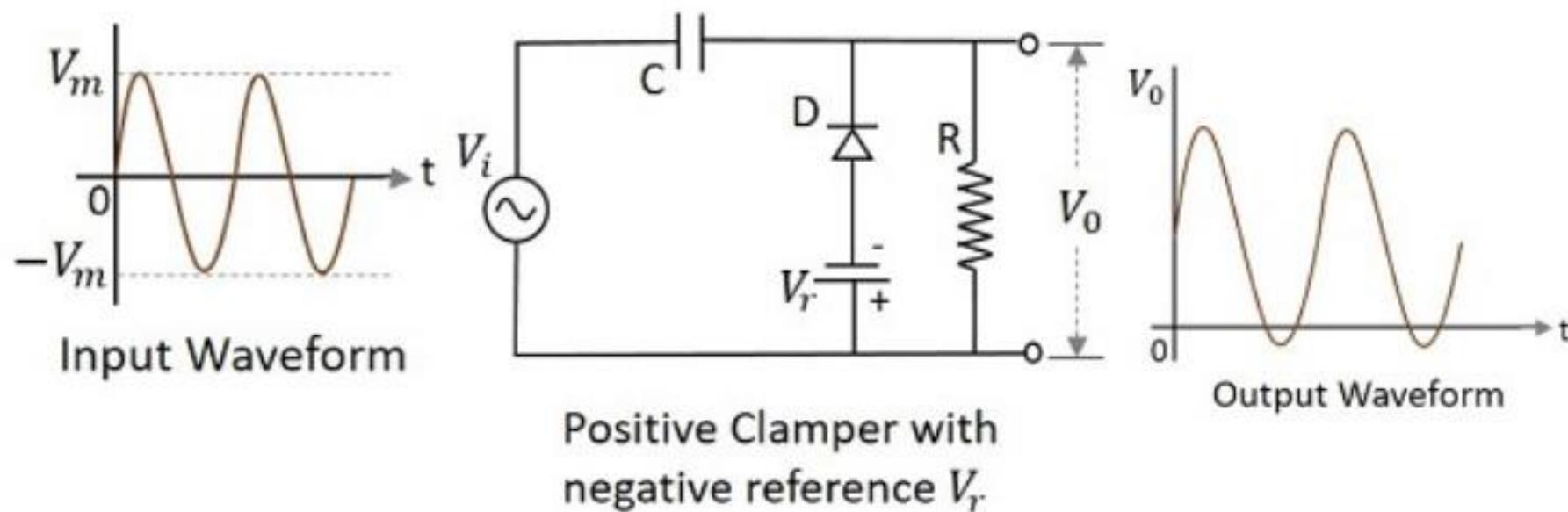


Positive Clamper with
positive reference V_r

FB Voltage for diode = $-V_m - V_r$

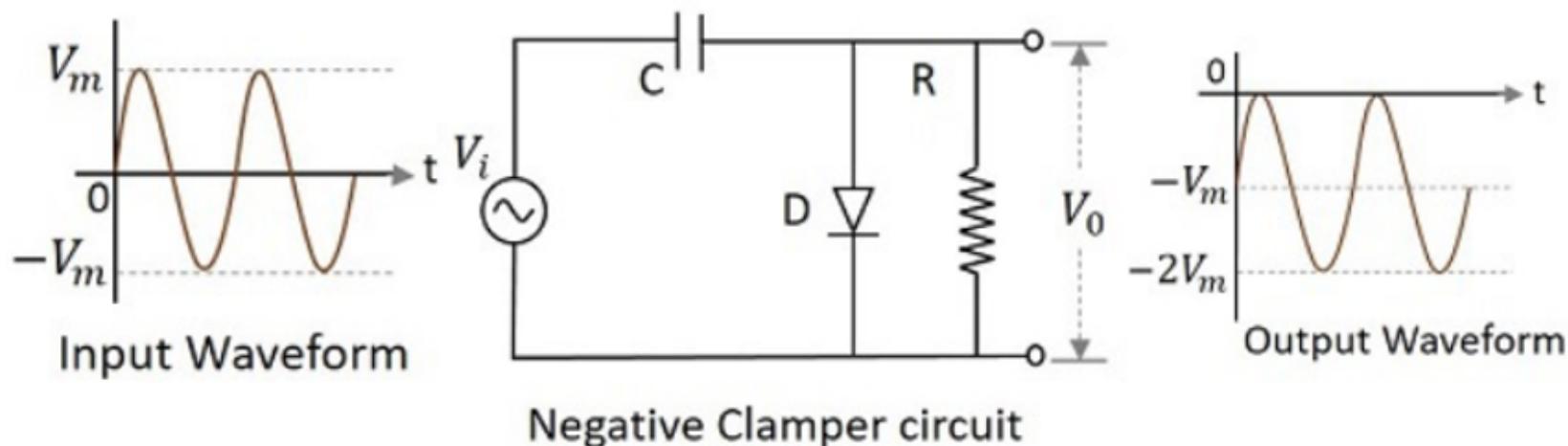
Positive Clamper with Negative V_r

A Positive clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.



Negative Clamper

A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. The figure below explains the construction of a negative clamper circuit.

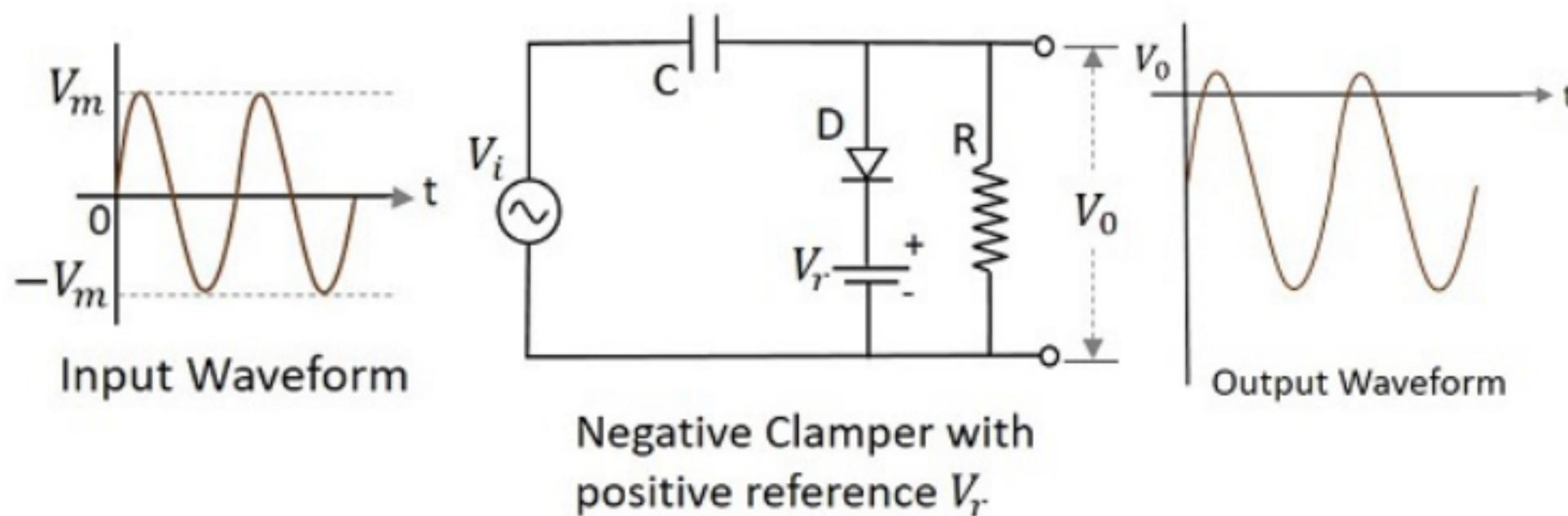


During the positive half cycle, the capacitor gets charged to its peak value v_m . The diode is forward biased and conducts. During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_o = V_i - V_m$$

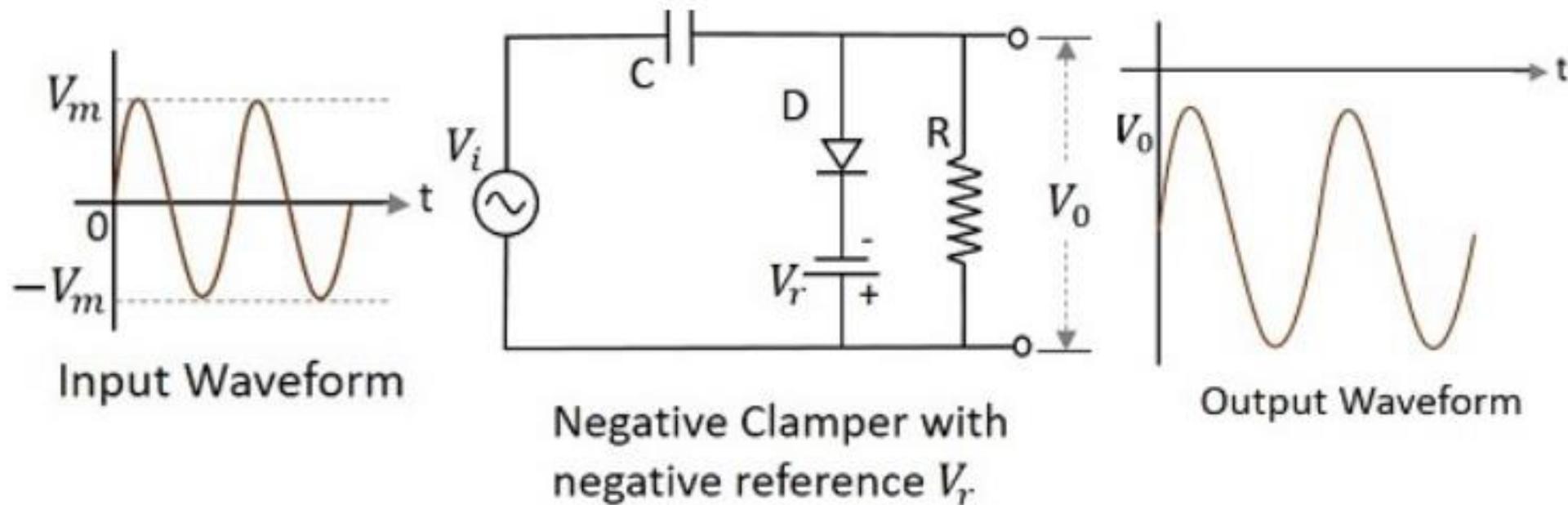
Negative clamper with positive V_r

A Negative clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with positive reference voltage is constructed as below.



Negative Clamper with Negative V_r

A Negative clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the negative clamper with negative reference voltage is constructed as below.



Applications

There are many applications for both Clippers and Clampers such as

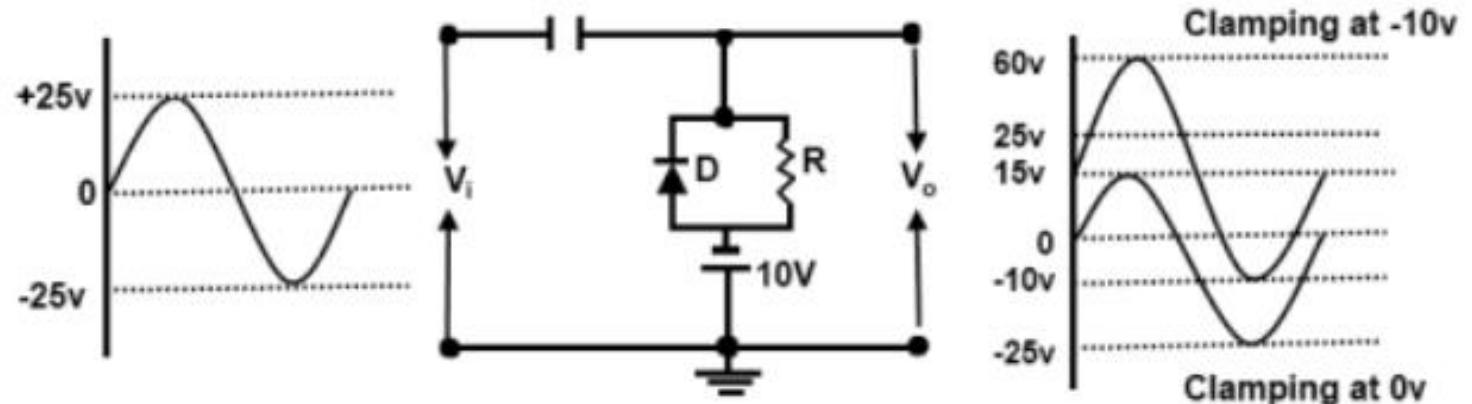
Clippers

- Used for the generation and shaping of waveforms
- Used for the protection of circuits from spikes
- Used for amplitude restorers
- Used as voltage limiters
- Used in television circuits
- Used in FM transmitters

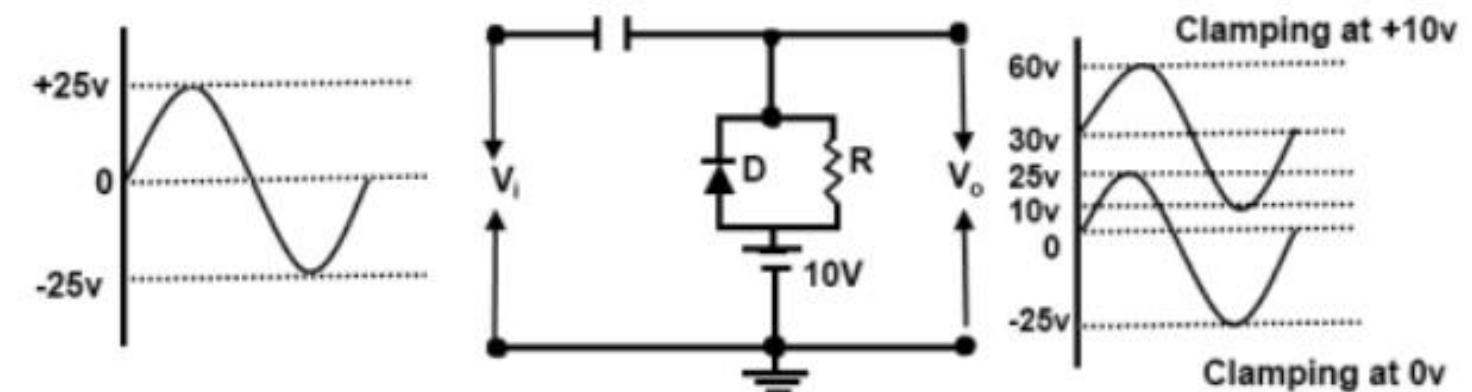
Clampers

- Used as direct current restorers
- Used to remove distortions
- Used as voltage multipliers
- Used for the protection of amplifiers
- Used as test equipment
- Used as base-line stabilizer

Examples

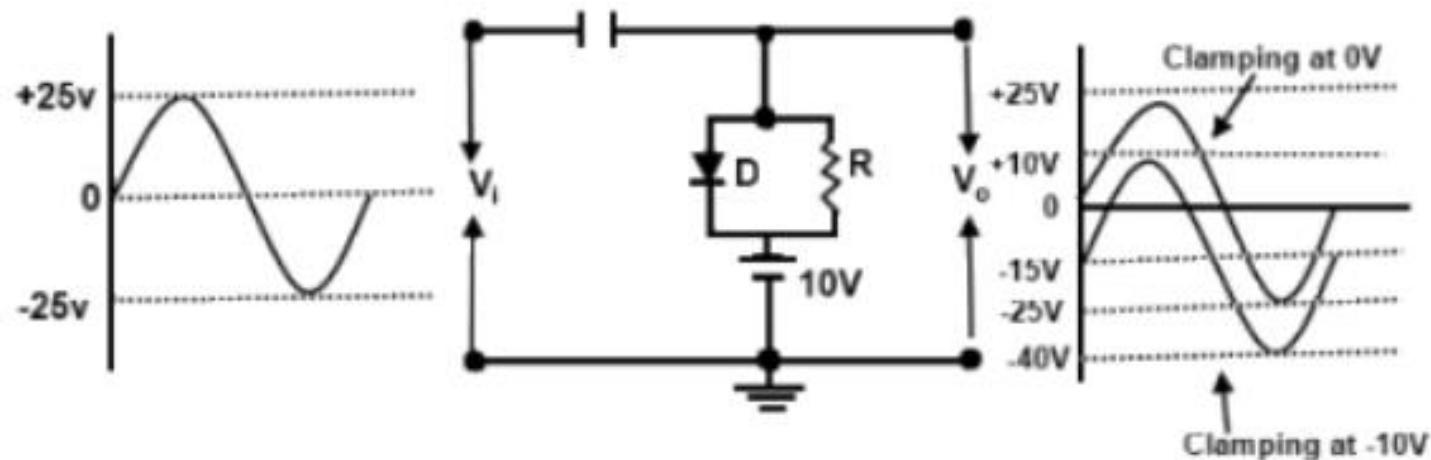


(a) Positive clamper with positive biased

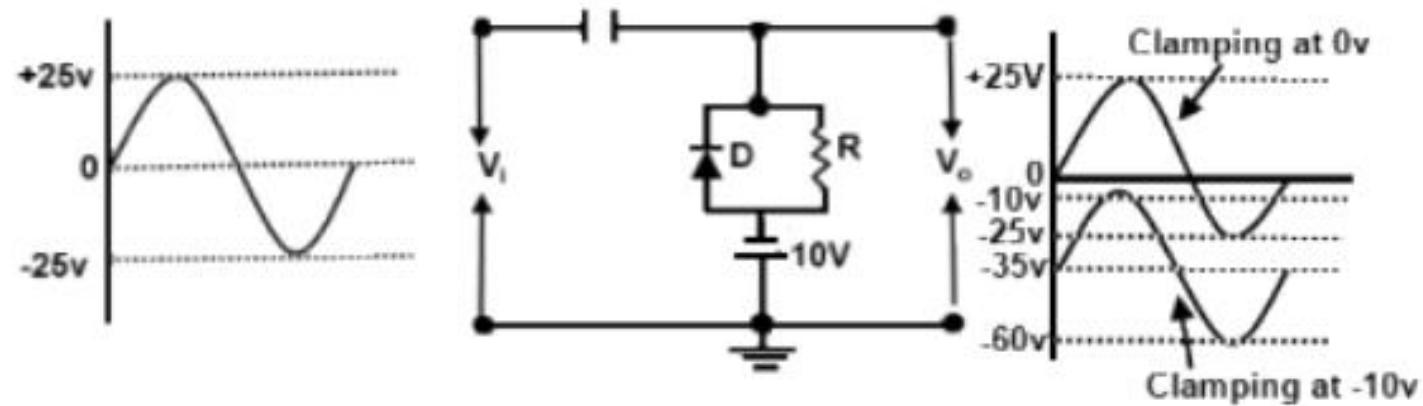


(b) Positive clamper with negative biased

Cont.

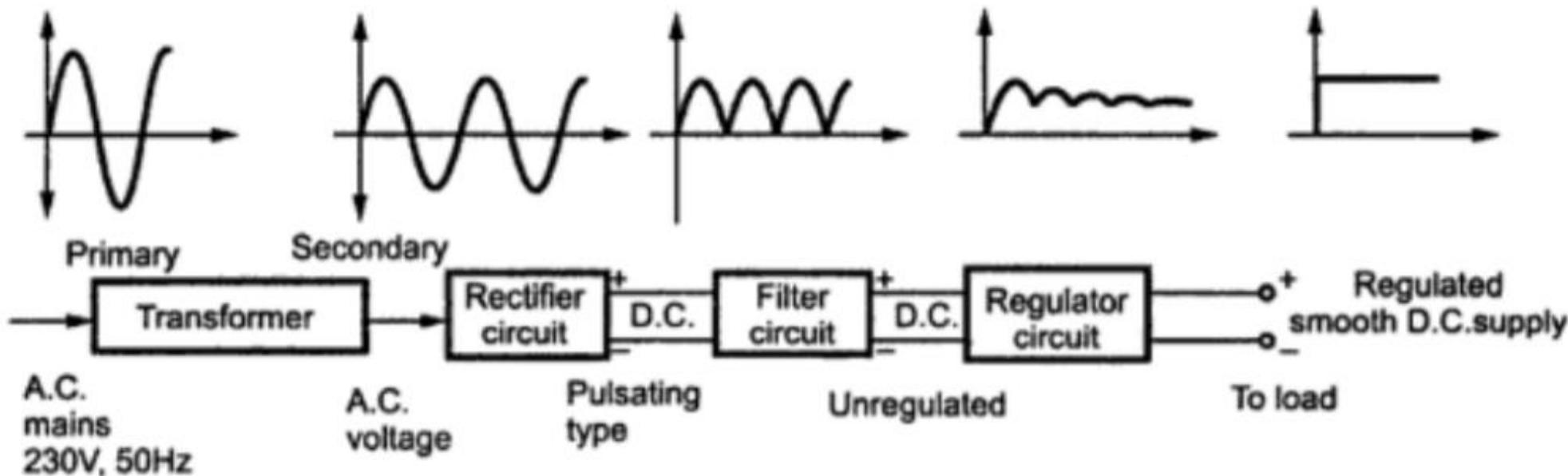


(a) Negative Clamper with positive biased



Rectifiers and filters

A rectifier is a device which converts a.c. voltage to pulsating d.c. voltage, using one or more p-n junction diode.

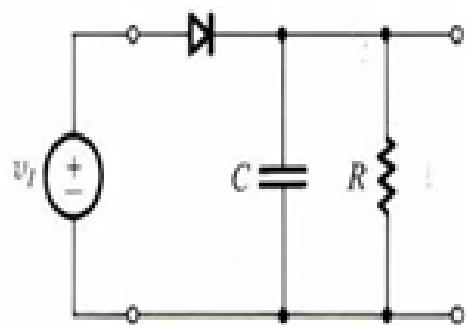


Block Diagram of a typical DC Power Supply

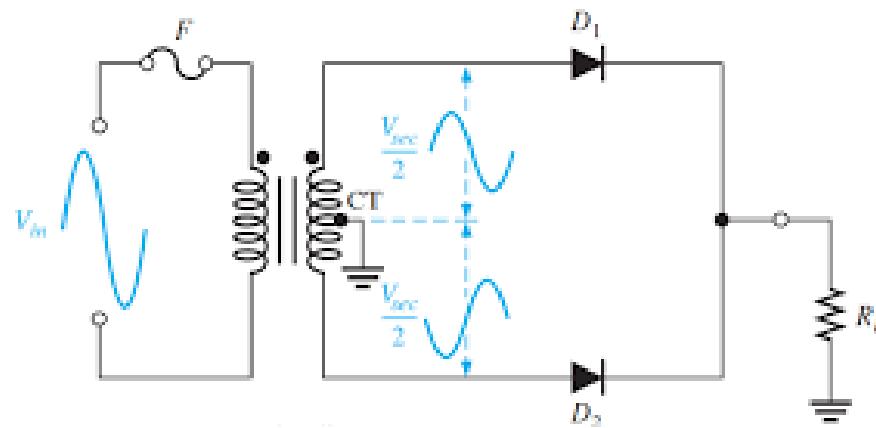
Types of Rectifier

Rectifier

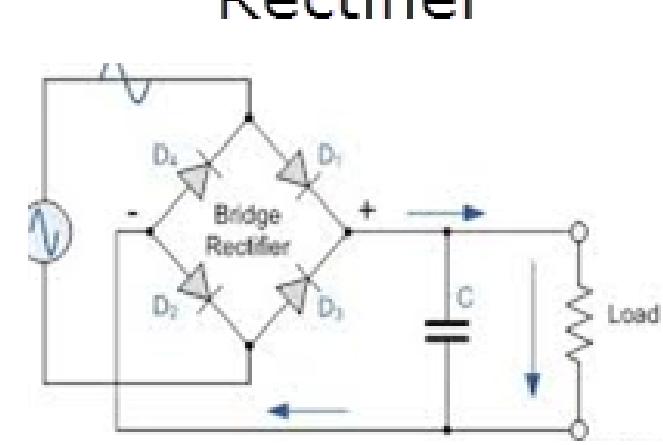
Half wave
rectifier



Center Tapped Full
Wave Rectifier



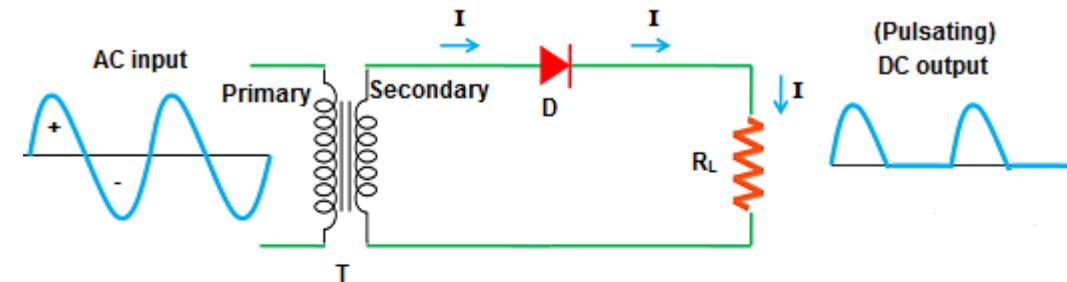
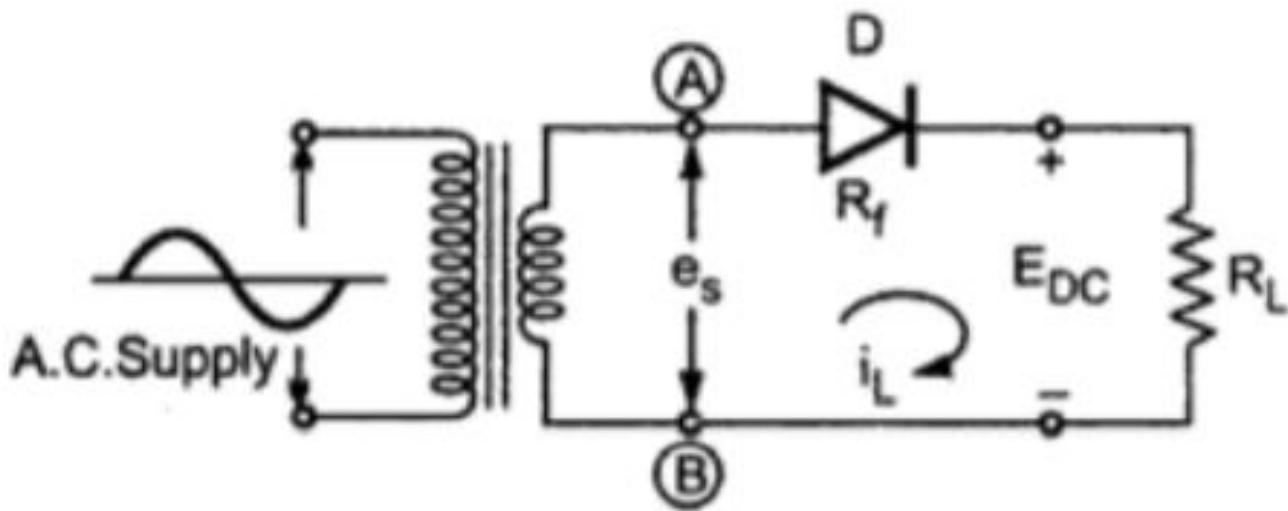
Full wave
rectifier



Bridge
Rectifier

Half Wave Rectifier:

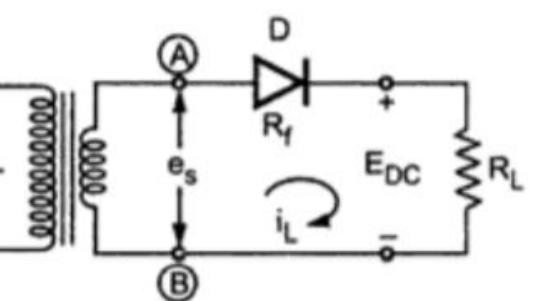
- A Type of rectifier that converts only the **half cycle** of the alternating current (AC) into direct current (DC) is known as halfwave rectifier



I = Current
D = Diode
 R_L = Load resistor
T = Transformer
+ = Positive half cycle
- = Negative half cycle

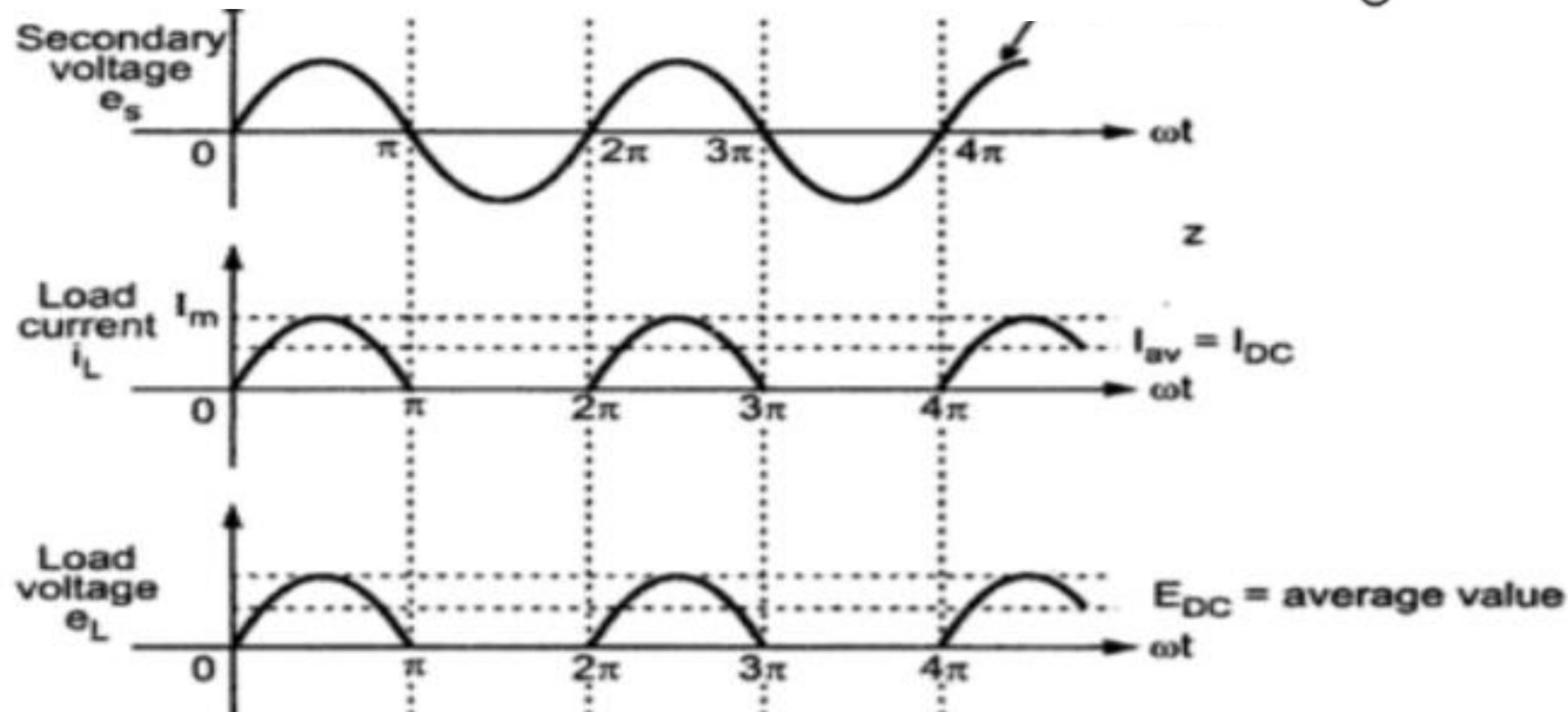
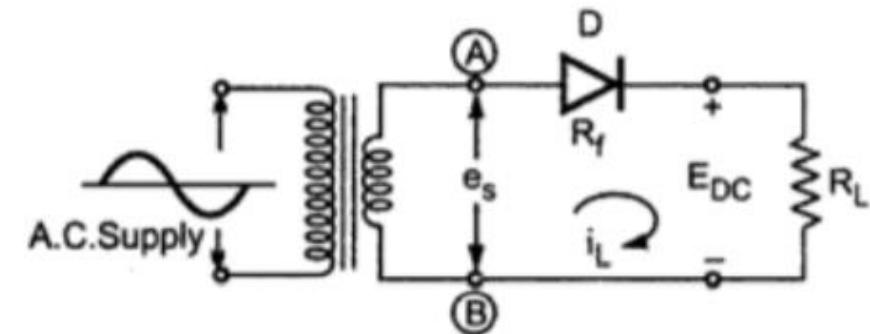
Half wave rectifier

Characteristic of Rectifier



- a) **Waveform of the load current :** As rectifier converts a.c. to pulsating d.c., it is important to analyze the nature of the current through load which ultimately determines the waveform of the load voltage.
- b) **Regulation of the output voltage :** As the load current changes, load voltage changes. Practically load voltage should remain constant. So concept of regulation is to study the effect of change in load current on the load voltage.
- c) **Rectifier efficiency :** It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.
- d) **Peak value of current in the rectifier circuit :** The peak value is the maximum value of an alternating current in the rectifier circuit. This decides the rating of the rectifier circuit element which is diode.
- e) **Peak value of voltage across the rectifier element in the reverse direction (PIV) :** When the diode is not conducting, the reverse voltage gets applied across the diode. The peak value of such voltage decides the peak inverse voltage i.e. PIV rating of a diode.
- f) **Ripple factor :** The output of the rectifier is of pulsating d.c. type. The amount of a.c. content in the output can be mathematically expressed by a factor called ripple factor.

Operation of the ckt



Cont.

The average or dc value of alternating current is obtained by integration.

For finding out the average value of an alternating waveform, we have to determine the area under the curve over one complete cycle i.e. from 0 to 2π and then dividing it by the base i.e. 2π .

Mathematically, current waveform can be described as,

$$i_L = I_m \sin \omega t \quad \text{for } 0 \leq \omega t \leq \pi$$

$$i_L = 0 \quad \text{for } \pi \leq \omega t \leq 2\pi$$

I_m = peak value of load current

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i_L d(\omega t) = \frac{1}{2\pi} \int_0^{2\pi} I_m \sin(\omega t) d(\omega t)$$

As no current flows during negative half cycle of ac input voltage, i.e. between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

∴

$$I_{DC} = \frac{1}{2\pi} \int_0^{\pi} I_m \sin(\omega t) d(\omega t)$$

$$= \frac{I_m}{2\pi} [-\cos(\omega t)]_0^{\pi} = -\frac{I_m}{2\pi} [\cos(\pi) - \cos(0)]$$

$$= -\frac{I_m}{2\pi} [-1 - 1] = \frac{I_m}{\pi}$$

∴

$$I_{DC} = \frac{I_m}{\pi} = \text{average value}$$

Average DC Load Current (I_{DC})

where

Cont.

Average DC Load Voltage (E_{DC})

It is the product of average D.C. load current and the load resistance R_L .

$$E_{DC} = I_{DC} R_L$$

Substituting value of I_{DC} ,

$$E_{DC} = \frac{I_m}{\pi} R_L = \frac{E_{sm}}{(R_f + R_L + R_s) \pi} R_L$$

$$I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

The winding resistance R_s and forward diode resistance R_f are practically very small compared to R_L .

∴

$$E_{DC} = \frac{E_{sm}}{\pi \left[\frac{R_f + R_s}{R_L} + 1 \right]}$$

But as R_f and R_s are small compared to R_L , $(R_f + R_s)/R_L$ is negligibly small compared to 1. So neglecting it we get,

∴

$$E_{DC} \approx \frac{E_{sm}}{\pi}$$

Cont.

R.M.S. Value of Load Current (I_{RMS})

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S. value of load current can be obtained as,

$$\begin{aligned}I_{RMS} &= \sqrt{\frac{1}{2\pi} \int_0^{\pi} (I_m \sin \omega t)^2 d(\omega t)} \\&= \sqrt{\frac{1}{2\pi} \int_0^{\pi} (I_m^2 \sin^2 \omega t d(\omega t))} \\&= I_m \sqrt{\frac{1}{2\pi} \int_0^{\pi} \frac{[1 - \cos(2\omega t)] d(\omega t)}{2}} \\&= I_m \sqrt{\frac{1}{2\pi} \left\{ \frac{\omega t}{2} - \frac{\sin(2\omega t)}{4} \right\}_0^{\pi}} \\&= I_m \sqrt{\frac{1}{2\pi} \left(\frac{\pi}{2} \right)} \quad \text{as } \sin(2\pi) = \sin(0) = 0 \\&= \frac{I_m}{2} \\I_{RMS} &= \frac{I_m}{2}\end{aligned}$$

Cont.

D.C. Power Output (P_{DC})

The d.c. power output can be obtained as,

$$P_{DC} = E_{DC} I_{DC} = I_{DC}^2 R_L$$

$$\text{D.C. Power output} = I_{DC}^2 R_L = \left[\frac{I_m}{\pi} \right]^2 R_L = \frac{I_m^2}{\pi^2} R_L$$

$$\therefore P_{DC} = \frac{I_m^2}{\pi^2} R_L$$

where

$$I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

$$\therefore P_{DC} = \frac{E_{sm}^2 R_L}{\pi^2 [R_f + R_L + R_s]^2}$$

Cont.

A.C. Power Input (P_{AC})

The power input taken from the secondary of transformer is the power supplied to three resistances namely load resistance R_L , the diode resistance R_f and winding resistance R_s . The a.c. power is given by,

$$P_{AC} = I_{RMS}^2 [R_L + R_f + R_s]$$

but

$$I_{RMS} = \frac{I_m}{2} \quad \text{for half wave,}$$

∴

$$P_{AC} = \frac{I_m^2}{4} [R_L + R_f + R_s]$$

Cont.

Rectifier Efficiency (η)

The rectifier efficiency is defined as the ratio of output d.c. power to input a.c. power.

∴

$$\eta = \frac{\text{D.C. output power}}{\text{A.C. input power}} = \frac{P_{DC}}{P_{AC}}$$

∴

$$\eta = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m^2}{4} [R_f + R_L + R_s]} = \frac{(4 / \pi^2) R_L}{(R_f + R_L + R_s)}$$

∴

$$\eta = \frac{0.406}{1 + \left(\frac{R_f + R_s}{R_L} \right)}$$

If $(R_f + R_s) \ll R_L$ as mentioned earlier, we get the maximum theoretical efficiency of half wave rectifier as,

$$\% \eta_{max} = 0.406 \times 100 = 40.6 \%$$

Cont.

Ripple Factor (γ)

$$\text{Ripple factor } \gamma = \frac{\text{R.M.S. value of a.c. component}}{\text{Average or d.c. component}}$$

Now the output current is composed of a.c. component as well as d.c. component.

Let

I_{ac} = r.m.s. value of a. c. component present
in output

I_{DC} = d.c. component present in output

I_{RMS} = R.M.S. value of total output current

$$\therefore I_{RMS} = \sqrt{I_{ac}^2 + I_{DC}^2}$$

$$\therefore I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

Now Ripple factor = $\frac{I_{ac}}{I_{DC}}$ as per definition

$$\therefore \gamma = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}}$$

$$\therefore \gamma = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

This is the general expression for ripple factor and can be used for any rectifier circuit.

Cont.

Now for a half wave circuit,

$$I_{RMS} = \frac{I_m}{2} \text{ while } I_{DC} = \frac{I_m}{\pi}$$

$$\therefore \gamma = \sqrt{\left[\frac{\left(\frac{I_m}{2} \right)^2}{\left(\frac{I_m}{\pi} \right)} \right] - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{1.4674}$$

$$\therefore \gamma = 1.211$$

This indicates that the ripple contents in the output are 1.211 times the d.c. component i.e. 121.1 % of d.c. component. The ripple factor for half wave is very high which indicates that the half wave circuit is a poor converter of a.c. to d.c. The ripple factor is minimised using filter circuits along with rectifiers.

Cont.

Peak Inverse Voltage (PIV)

The Peak Inverse Voltage is the peak voltage across the diode in the reverse direction i.e. when the diode is reverse biased. In half wave rectifier, the load current is ideally zero when the diode is reverse biased and hence the maximum value of the voltage that can exist across the diode is nothing but E_{sm} .

$$\therefore \text{PIV of diode} = E_{sm} = \text{Maximum value of secondary voltage}$$
$$= \pi E_{DC}|_{I_{DC}=0}$$

This is called PIV rating of a diode. So diode must be selected based on this PIV rating and the circuit specifications.

Cont.

Transformer Utilization Factor (T.U.F.)

The factor which indicates how much is the utilization of the transformer in the circuit is called Transformer Utilization Factor (T.U.F.)

The T.U.F. is defined as the ratio of d.c. power delivered to the load to the a.c power rating of the transformer. While calculating the a.c. power rating, it is necessary to consider r.m.s. value of a.c. voltage and current.

The T.U.F. for half wave rectifier can be obtained as,

$$\begin{aligned}\text{A.C. power rating of transformer} &= E_{\text{RMS}} I_{\text{RMS}} \\ &= \frac{E_{\text{sm}}}{\sqrt{2}} \cdot \frac{I_m}{2} = \frac{E_{\text{sm}} I_m}{2\sqrt{2}}\end{aligned}$$

Remember that the secondary voltage is purely sinusoidal hence its r.m.s. value is $1/\sqrt{2}$ times maximum while the current is half sinusoidal hence its r.m.s. value is $1/2$ of the maximum, as derived earlier.

$$\text{D.C. power delivered to the load} = I_{\text{DC}}^2 R_L$$

Cont.

$$= \left(\frac{I_m}{\pi} \right)^2 R_L$$

$$\therefore T.U.F. = \frac{\text{D.C. Power delivered to the load}}{\text{A.C. Power rating of the transformer}}$$

$$= \frac{\left(\frac{I_m}{\pi} \right)^2 R_L}{\left(\frac{E_{sm} I_m}{2\sqrt{2}} \right)}$$

Neglecting the drop across R_f and R_s we can write,

$$E_{sm} = I_m R_L$$

$$\therefore T.U.F. = \frac{I_m^2}{\pi^2} \cdot \frac{R_L \cdot 2\sqrt{2}}{I_m^2 R_L}$$

$$= \frac{2\sqrt{2}}{\pi^2}$$

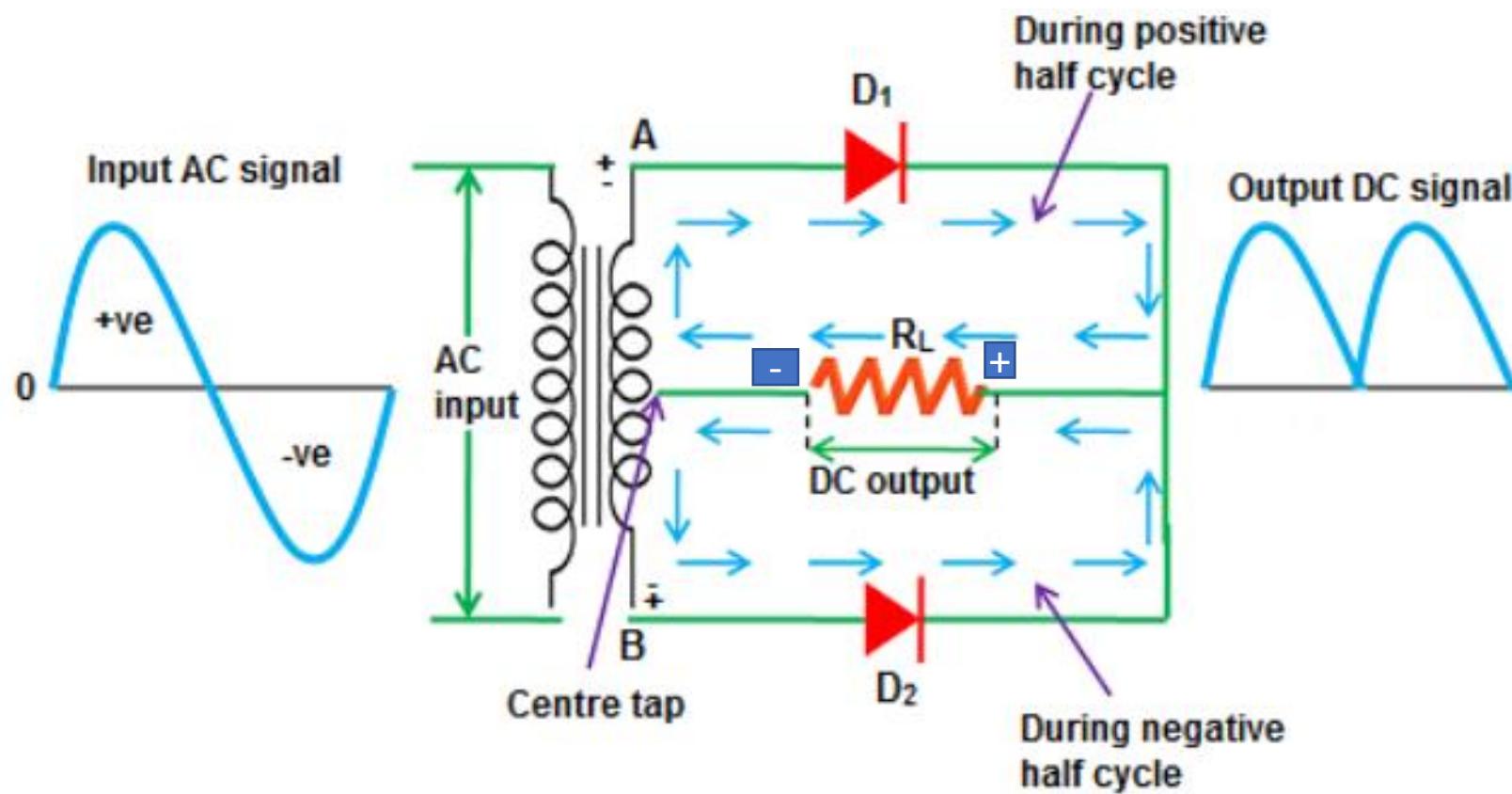
$$= 0.287$$

The value of T.U.F. is low which shows that in half wave circuit, the transformer is not fully utilized.

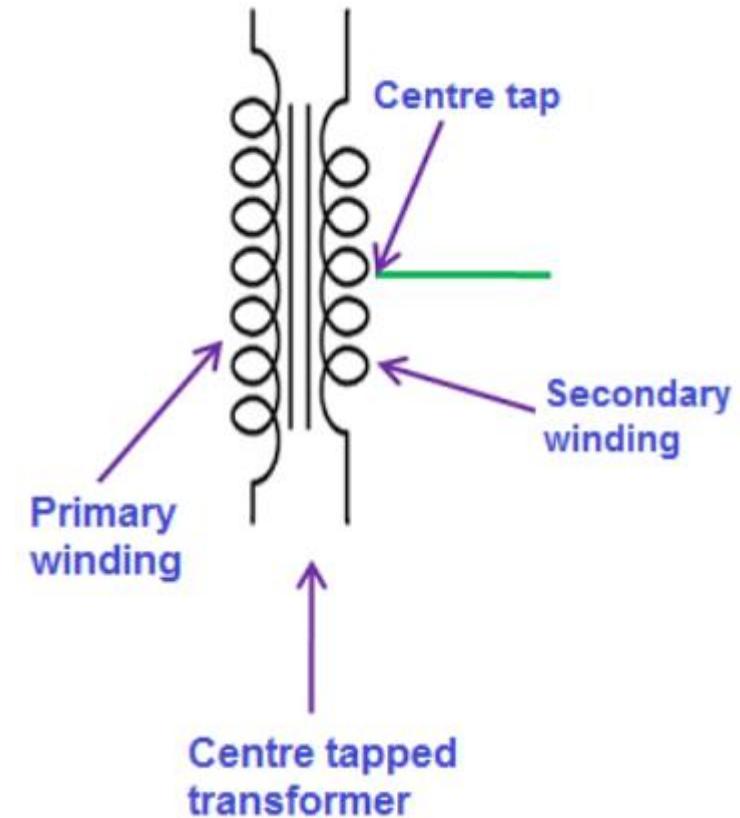
FULL WAVE RECTIFIER DEFINITION

A full wave rectifier is a type of rectifier which converts both half cycles of the AC signal into pulsating DC signal.

Centre tapped FWR

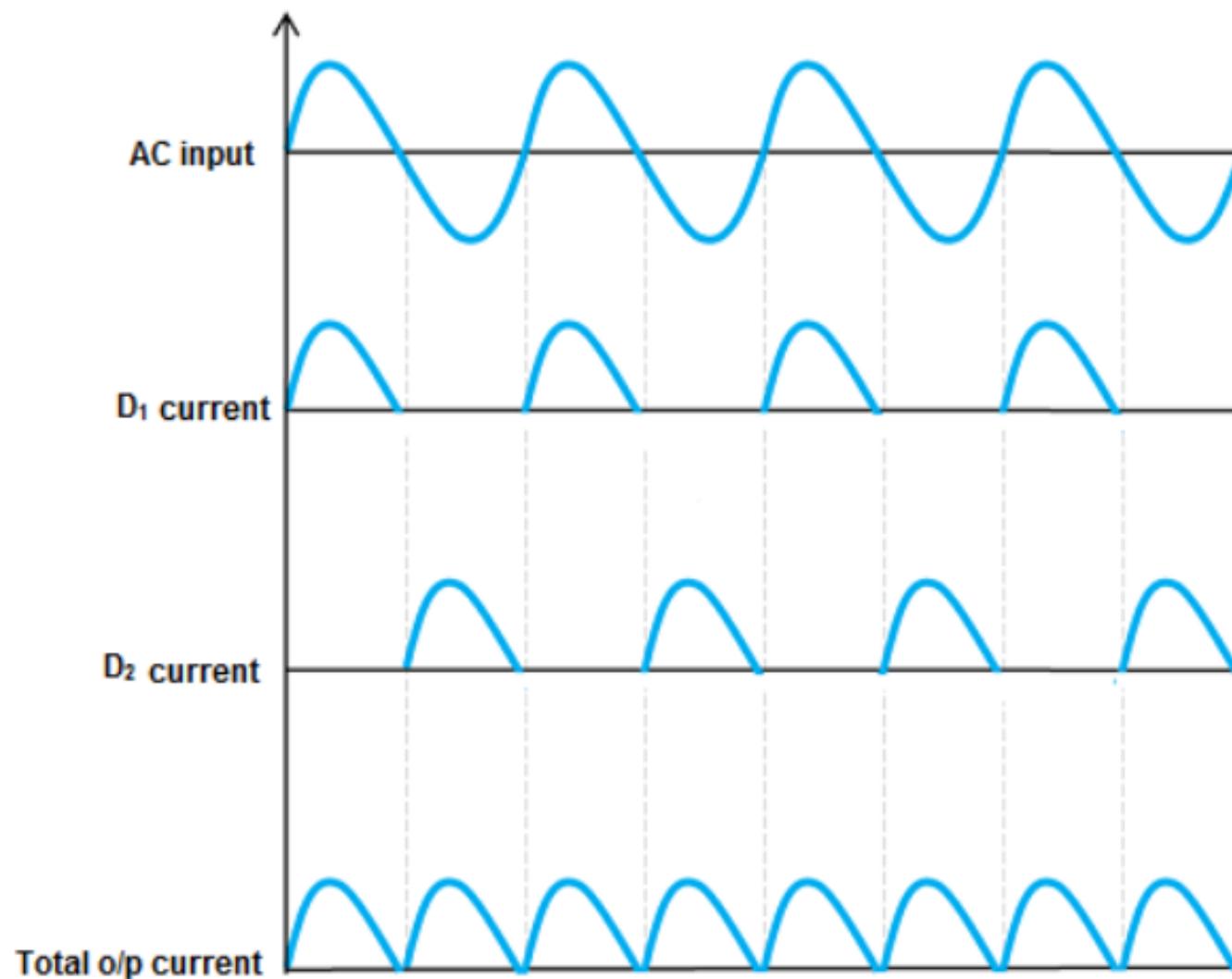


Centre tapped transformer



Cont.

Output waveforms of full wave rectifier



Cont.

Characteristics of full wave rectifier

Root mean square (RMS) value of load current I_{RMS}

The root mean square (RMS) value of load current in a full wave rectifier is

$$I_{RMS} = \frac{I_m}{\sqrt{2}}$$

Root mean square (RMS) value of the output load voltage V_{RMS}

The root mean square (RMS) value of output load voltage in a full wave rectifier is

$$V_{RMS} = I_{RMS} R_L = \frac{I_m}{\sqrt{2}} R_L$$

Cont.

DC output current

At the output load resistor R_L , both the diode D_1 and diode D_2 currents flow in the same direction. So the output current is the sum of D_1 and D_2 currents.

The current produced by D_1 is I_{max} / π and the current produced by D_2 is I_{max} / π .

So the output current $I_{DC} = 2I_{max} / \pi$

Where,

I_{max} = maximum DC load current

DC output voltage

The DC output voltage appeared at the load resistor R_L is given as

$$V_{DC} = 2V_{max} / \pi$$

Where,

V_{max} = maximum secondary voltage

Cont.

Rectifier efficiency

Rectifier efficiency indicates how efficiently the rectifier converts AC into DC. A high percentage of rectifier efficiency indicates a good rectifier while a low percentage of rectifier efficiency indicates an inefficient rectifier.

Rectifier efficiency is defined as the ratio of DC output power to the AC input power.

It can be mathematically written as

$$\eta = \text{output } P_{DC} / \text{input } P_{AC}$$

The rectifier efficiency of a full wave rectifier is 81.2%.

The rectifier efficiency of a full wave rectifier is twice that of the half wave rectifier. So the full wave rectifier is more efficient than a half wave rectifier

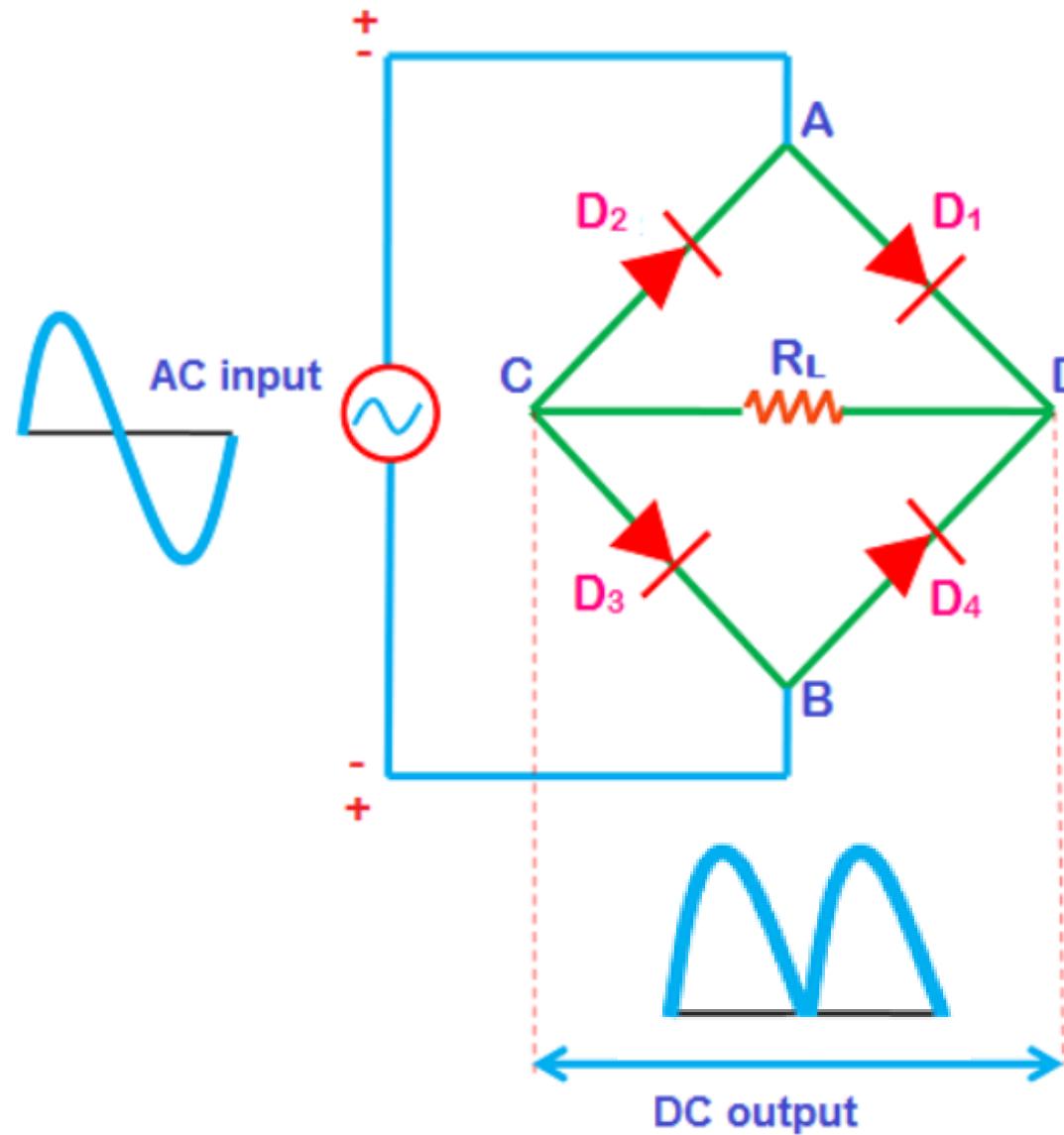
Cont.

Peak inverse voltage (PIV)

Peak inverse voltage or peak reverse voltage is the maximum voltage a diode can withstand in the reverse bias condition. If the applied voltage is greater than the peak inverse voltage, the diode will be permanently destroyed.

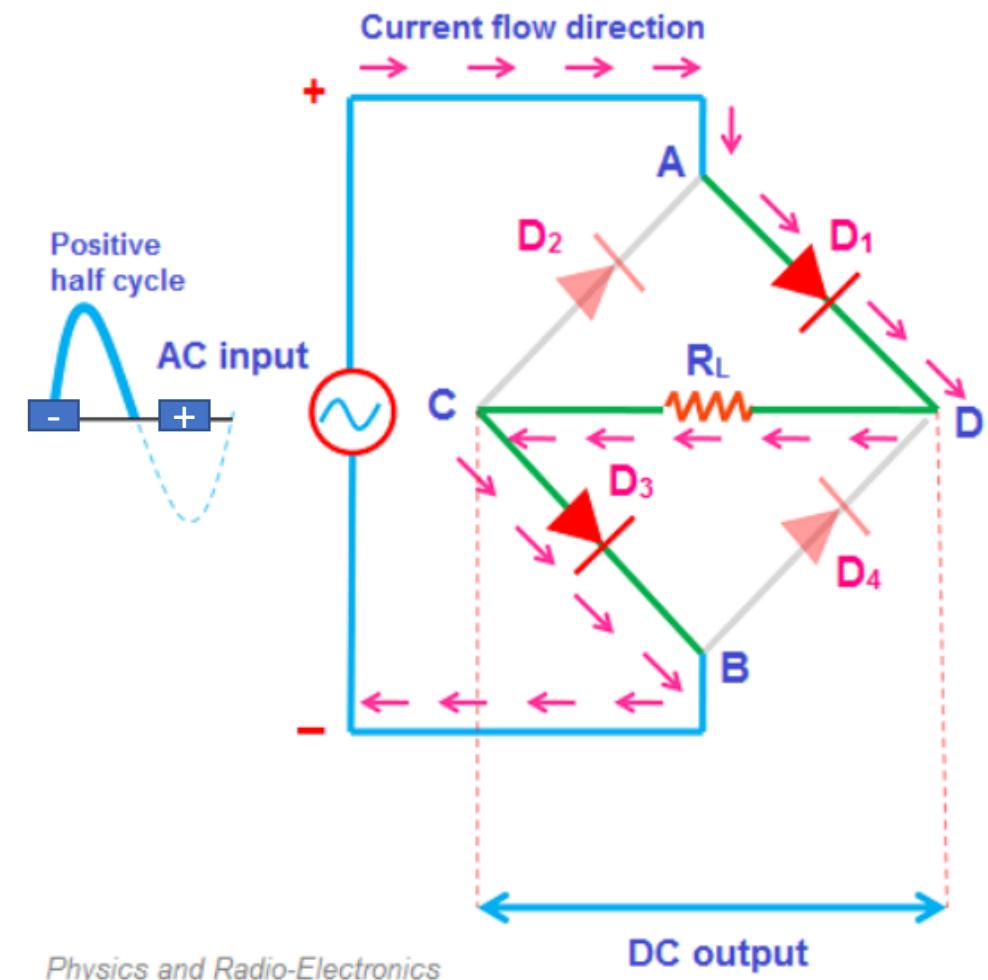
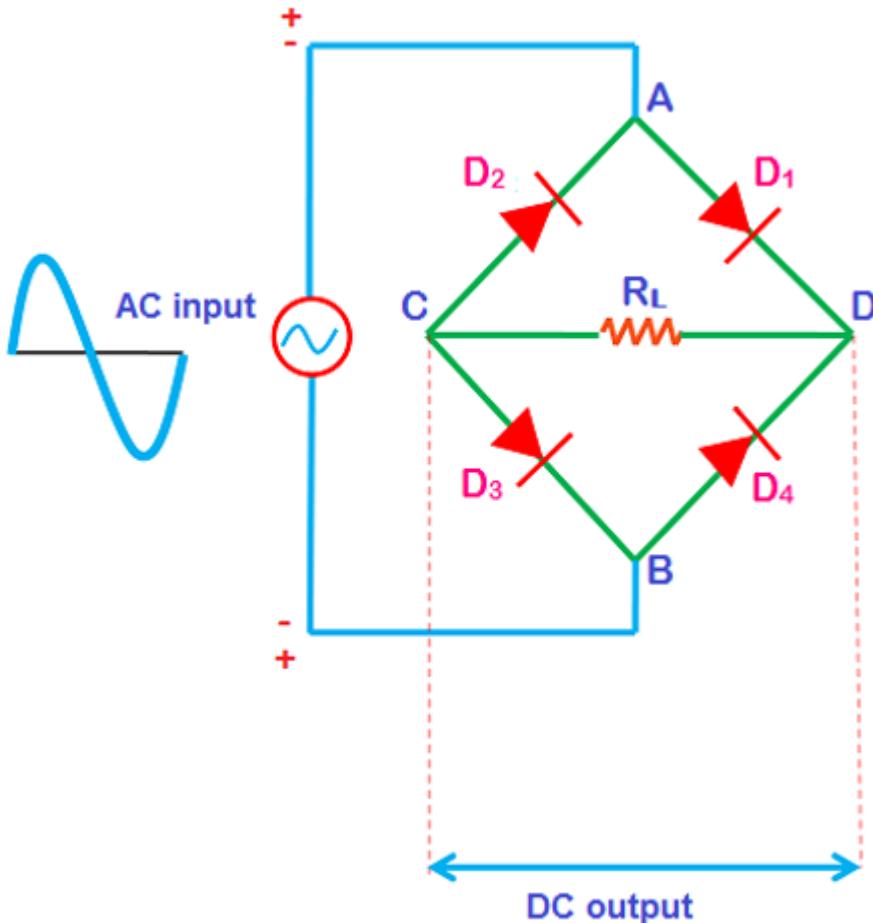
The peak inverse voltage (PIV) = $2V_{smax}$

Bridge Rectifier



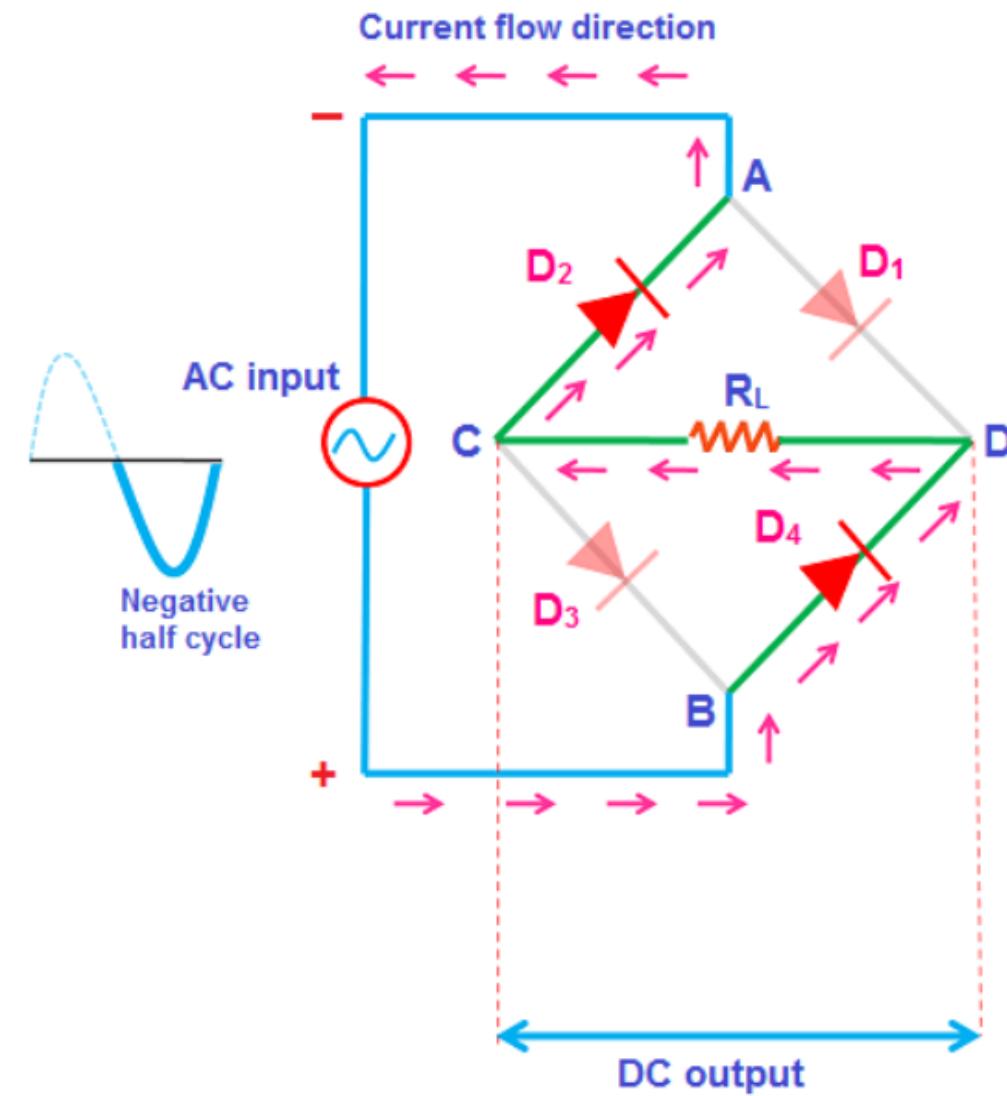
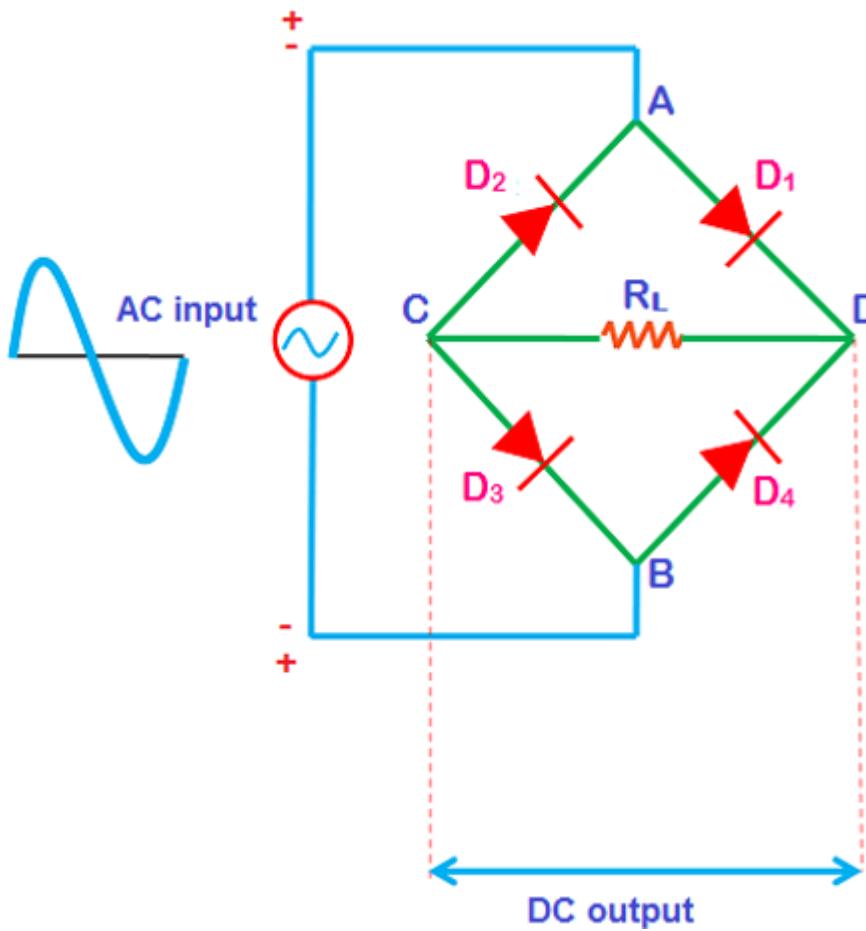
Cont.

The current flow direction during the positive half cycle is shown in the figure A (I.e. A to D to C to B).



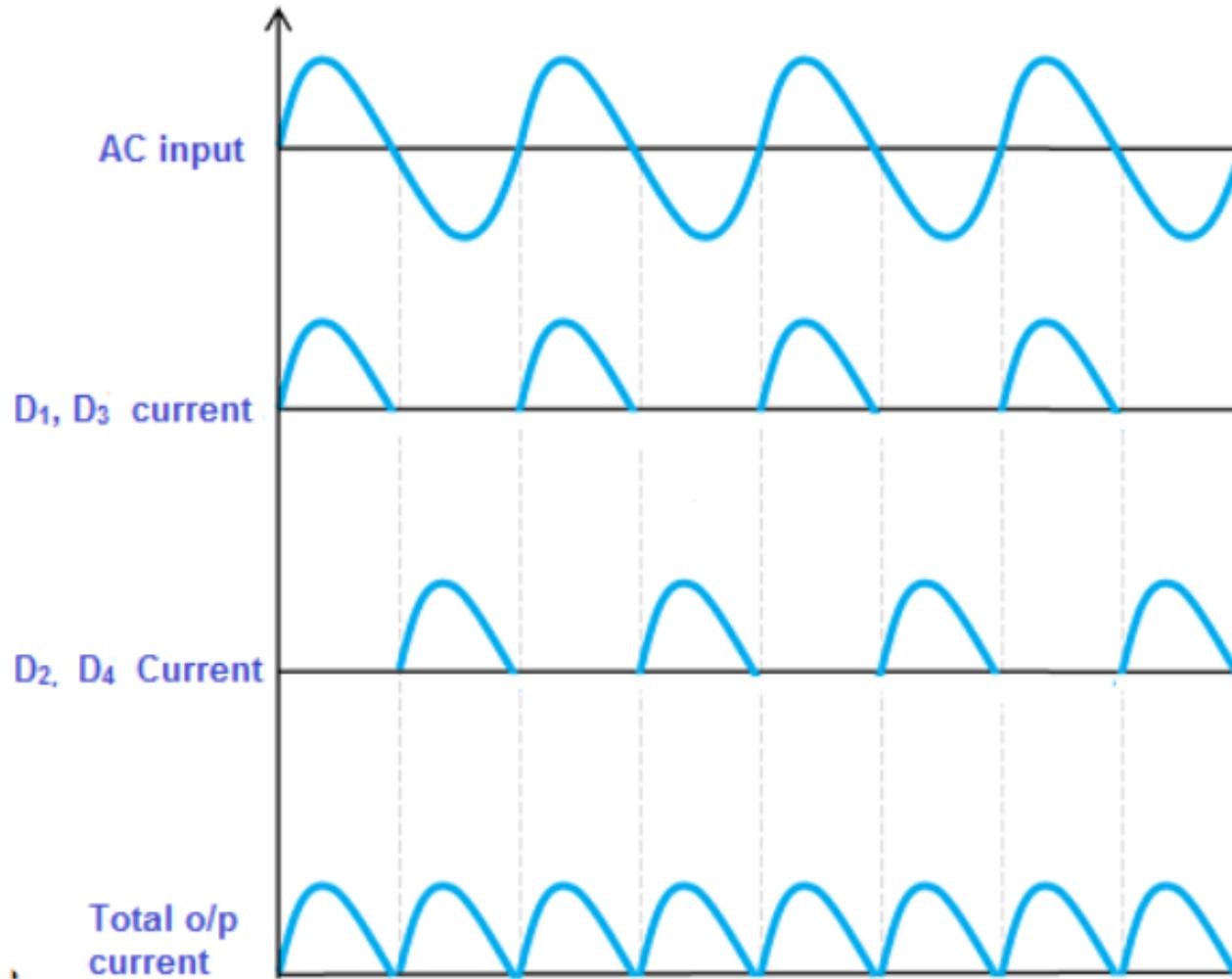
Cont.

The current flow direction during negative half cycle is shown in the figure B (i.e. B to D to C to A).



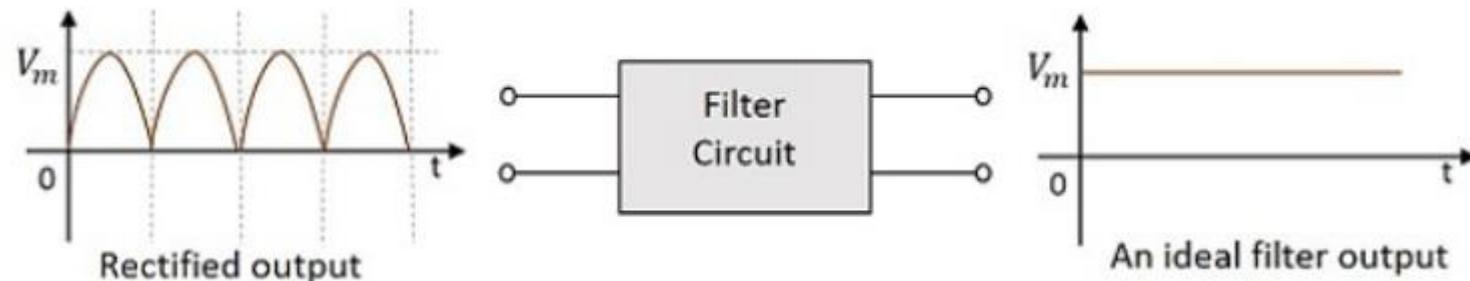
Cont.

The output waveforms of the bridge rectifier is shown in the below figure.



Filters

- The ripple in the signal denotes the presence of some AC component. This ac component has to be completely removed in order to get pure dc output. So, we need a circuit that **smoothens** the rectified output into a pure dc signal.
- A **filter circuit** is one which removes the ac component present in the rectified output and allows the dc component to reach the load.
- The following figure shows the functionality of a filter circuit.



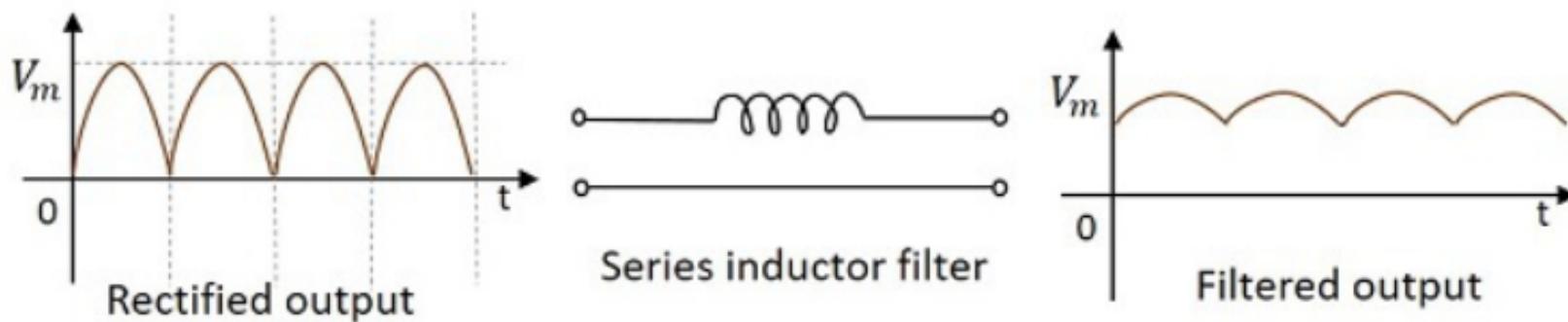
Cont.

- A filter circuit is constructed using two main components, inductor and capacitor. We have already studied in Basic Electronics tutorial that
- An inductor allows **dc** and blocks **ac**.
- A capacitor allows **ac** and blocks **dc**.

Cont.

Series Inductor Filter

As an inductor allows dc and blocks ac, a filter called **Series Inductor Filter** can be constructed by connecting the inductor in series, between the rectifier and the load. The figure below shows the circuit of a series inductor filter.

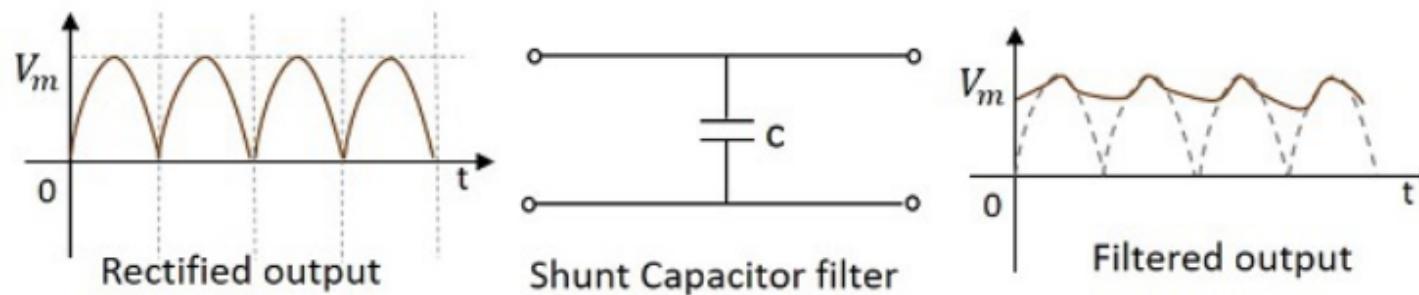


The rectified output when passed through this filter, the inductor blocks the ac components that are present in the signal, in order to provide a pure dc. This is a simple primary filter.

Cont.

Shunt Capacitor Filter

As a capacitor allows ac through it and blocks dc, a filter called **Shunt Capacitor Filter** can be constructed using a capacitor, connected in shunt, as shown in the following figure.



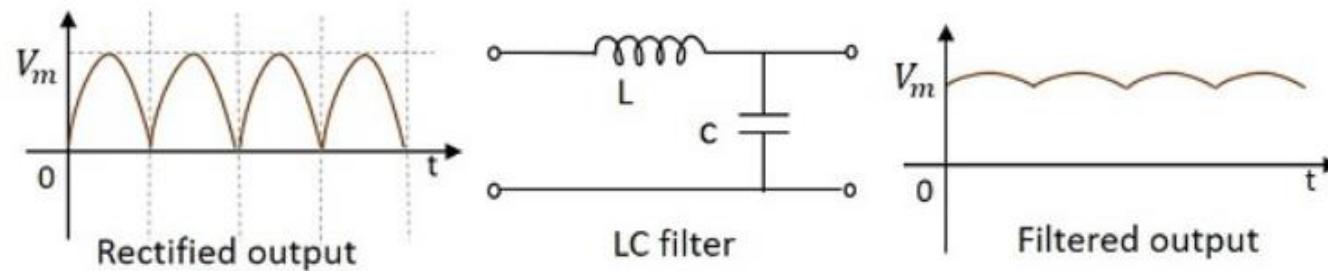
The rectified output when passed through this filter, the ac components present in the signal are grounded through the capacitor which allows ac components. The remaining dc components present in the signal are collected at the output.

The above filter types discussed are constructed using an inductor or a capacitor. Now, let's try to use both of them to make a better filter. These are combinational filters.

Cont.

L-C Filter

A filter circuit can be constructed using both inductor and capacitor in order to obtain a better output where the efficiencies of both inductor and capacitor can be used. The figure below shows the circuit diagram of a LC filter.



The rectified output when given to this circuit, the inductor allows dc components to pass through it, blocking the ac components in the signal. Now, from that signal, few more ac components if any present are grounded so that we get a pure dc output.

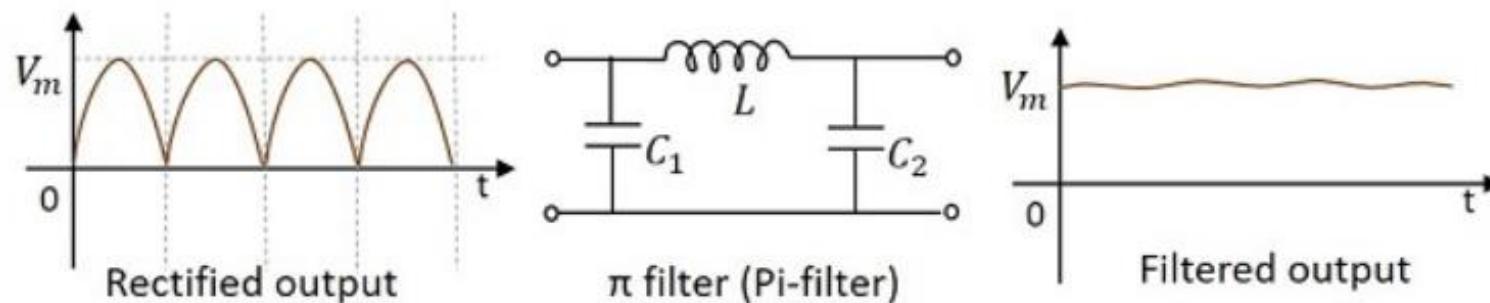
This filter is also called as a **Choke Input Filter** as the input signal first enters the inductor. The output of this filter is a better one than the previous ones.

Cont.

Π - Filter *Pi filter*

This is another type of filter circuit which is very commonly used. It has capacitor at its input and hence it is also called as a **Capacitor Input Filter**. Here, two capacitors and one inductor are connected in the form of π shaped network. A capacitor in parallel, then an inductor in series, followed by another capacitor in parallel makes this circuit.

If needed, several identical sections can also be added to this, according to the requirement. The figure below shows a circuit for π filter *Pi – filter* .



Cont.

Working of a Pi filter

In this circuit, we have a capacitor in parallel, then an inductor in series, followed by another capacitor in parallel.

- **Capacitor C₁** – This filter capacitor offers high reactance to dc and low reactance to ac signal. After grounding the ac components present in the signal, the signal passes to the inductor for further filtration.
- **Inductor L** – This inductor offers low reactance to dc components, while blocking the ac components if any got managed to pass, through the capacitor C₁.
- **Capacitor C₂** – Now the signal is further smoothed using this capacitor so that it allows any ac component present in the signal, which the inductor has failed to block.

Thus we, get the desired pure dc output at the load.

Assignment 1

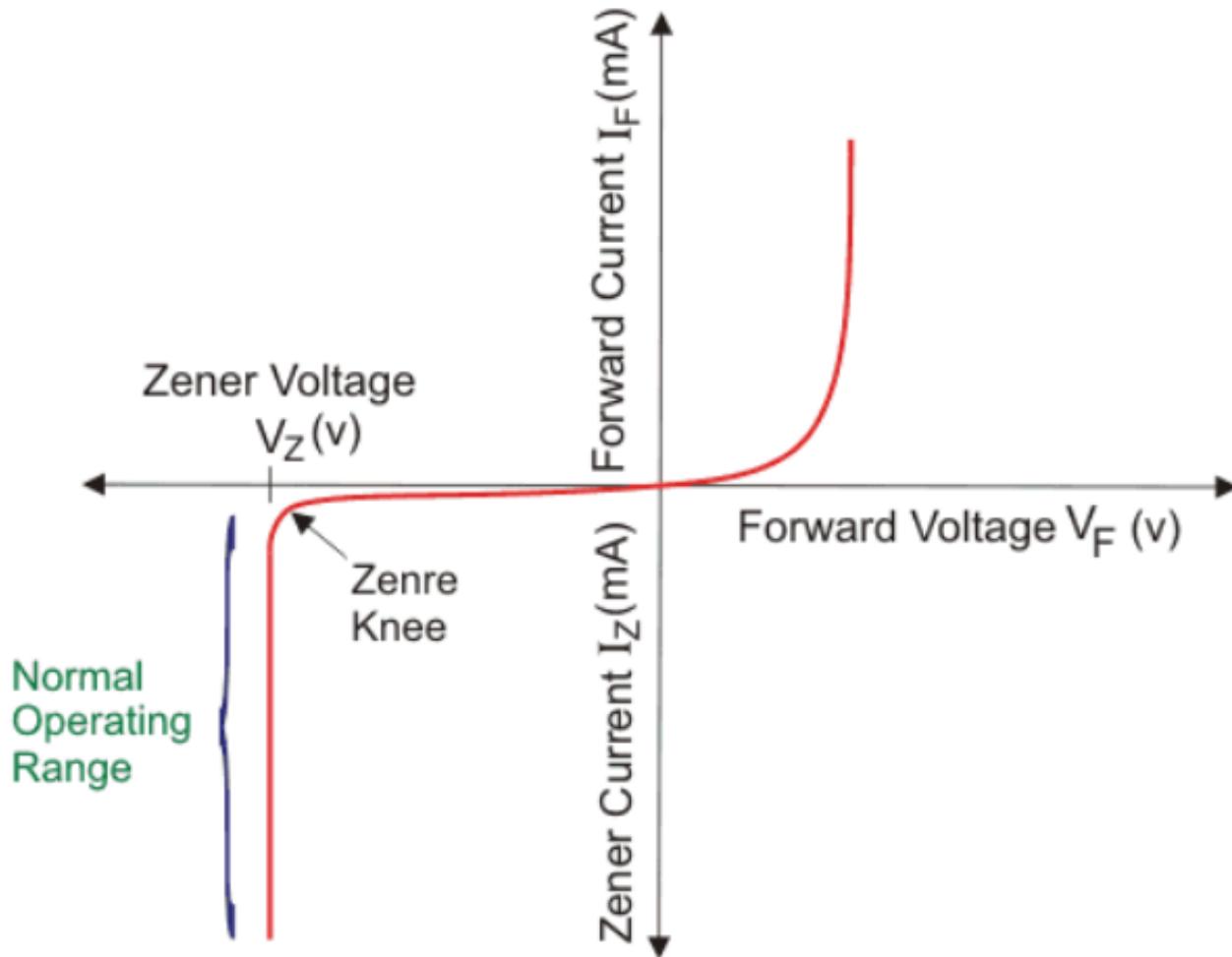
1. Define Characteristics of Centre Taped rectifier with derivations
2. Define Characteristics of bridge rectifier with derivations

Zener Diode as Voltage Regulator

- A Zener diode is one of the specially designed diodes that predominately works in reverse biased conditions.
- They are more heavily doped than ordinary diodes, due to which they have narrow depletion region.
- While regular diodes get damaged when the voltage across them exceeds the reverse breakdown voltage, Zener diodes work exclusively in this region.
- The depletion region in Zener diode goes back to its normal state when the reverse voltage gets removed.
- This particular property of Zener diodes makes it useful as a **voltage regulator**.

Zener diode Characteristics

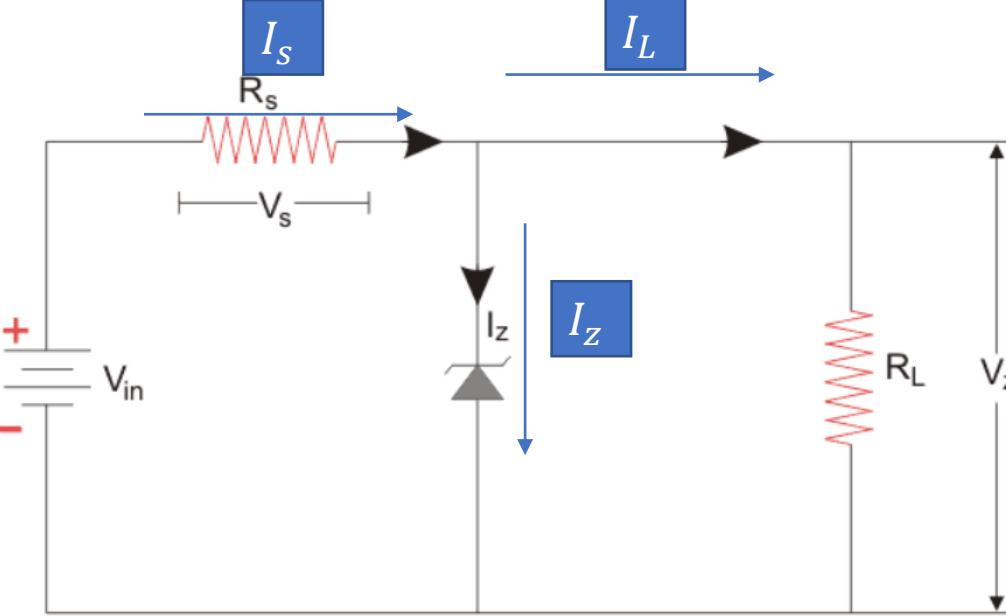
- When we apply a reverse voltage to a Zener diode, a negligible amount of current flows through the circuit.
- When a voltage higher than Zener breakdown voltage is applied, Zener breakdown occurs.
- Zener breakdown is a phenomenon where a significant amount of current flows through the diode with a negligible drop in voltage.
- When we increase the reverse voltage further, the voltage across the diode remains at the same value of Zener breakdown voltage whereas the current through it keeps on rising as seen in the graph above.
- Here in the graph V_z refers to the Zener breakdown voltage. Zener breakdown voltage typically can range from 1.2 V to 200 V depending on its application.



Zener Diode as Voltage Regulator

For example, we want that the voltage across a load in our circuit does not exceed, let's say, 12 volts. Then we can select a Zener diode with a breakdown voltage of 12 volts and connect it across the load. Then even if the input voltage exceeds that value, the voltage across the load will never exceed 12 volts.

$$I_s = I_L + I_z$$
$$(V_{in} - V_z)/R_s = V_z/R_L + I_z$$



Here the Zener diode is connected across the load R_L . We want the voltage across the load to be regulated and not cross the value of V_z . Depending on our requirement, we choose the suitable Zener diode with a Zener breakdown voltage near to the voltage we require across the load. We connect the Zener diode in reverse bias condition. When the voltage across the diode exceeds the Zener breakdown voltage, a significant amount of current starts flowing through the diode. As the load is in parallel to the diode, the voltage drop across the load is also equal to the Zener breakdown voltage. The Zener diode provides a path for the current to flow and hence the load gets protected from excessive currents. Thus the Zener diode serves two purposes here: **Zener diode as a voltage regulator** as well as it protects the load from excessive current.

a). The maximum current flowing through the zener diode.

$$\text{Maximum Current} = \frac{\text{Watts}}{\text{Voltage}} = \frac{2\text{w}}{5\text{v}} = 400\text{mA}$$

Zener Diode Example

A 5.0V stabilized power supply is required to be produced from a 12V DC power supply input source. The maximum power rating P_Z of the zener diode is 2W. Using the zener regulator circuit above calculate:

b). The minimum value of the series resistor, R_S

$$R_S = \frac{V_S - V_Z}{I_Z} = \frac{12 - 5}{400\text{mA}} = 17.5\Omega$$

c). The load current I_L if a load resistor of $1k\Omega$ is connected across the zener diode.

$$I_L = \frac{V_Z}{R_L} = \frac{5\text{v}}{1000\Omega} = 5\text{mA}$$

d). The zener current I_Z at full load.

$$I_Z = I_S - I_L = 400\text{mA} - 5\text{mA} = 395\text{mA}$$

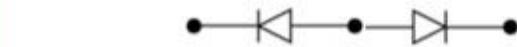
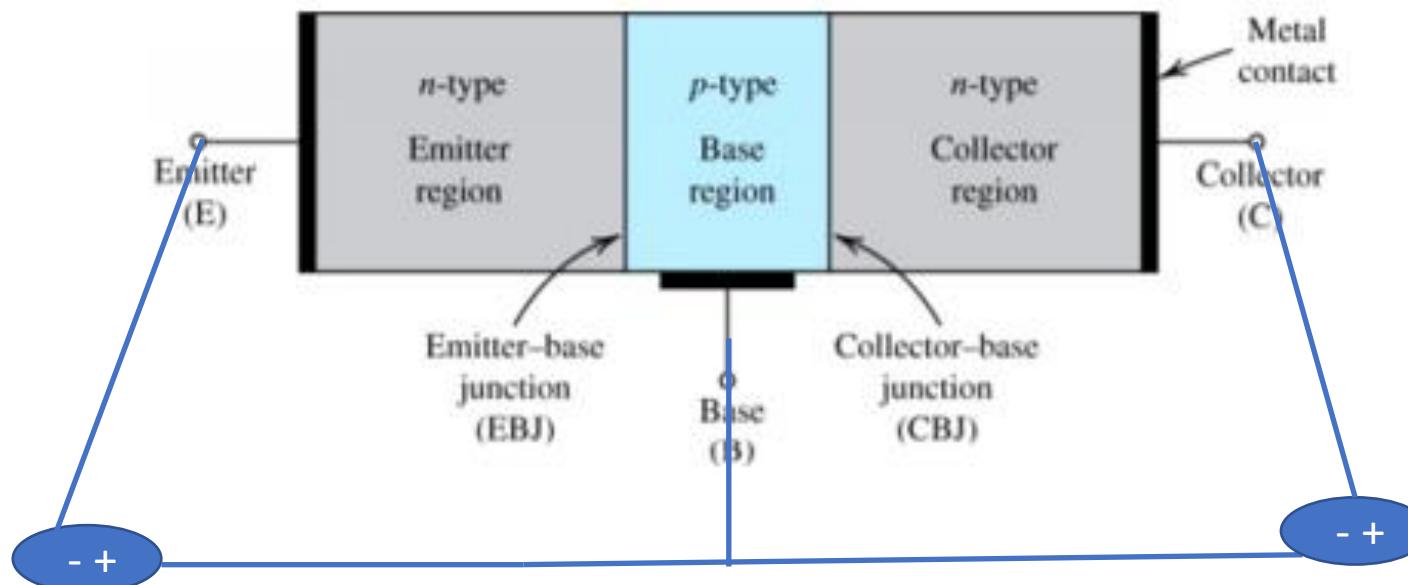
Chapter 2



Bipolar Junction Transistor (BJT): Introduction, Physical behavior, ~~Ebers-Moll model~~, Common Base and Common Emitter characteristics, load line, operation point, active, saturation and cut off mode of operations. DC Model. ~~Bias stabilization: Need for stabilization, fixed bias and self bias circuits,~~

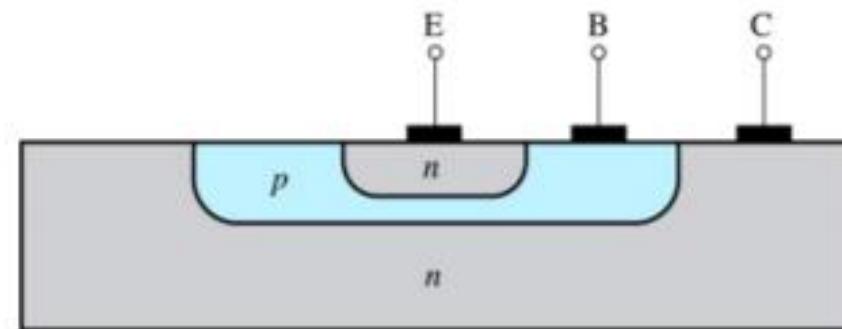
Bipolar Junction Transistor (BJT)

Simplified physical structure



➤ Device is constructed such that BJT does NOT act as two diodes back to back (when voltages are applied to all three terminals).

An implementation on an IC



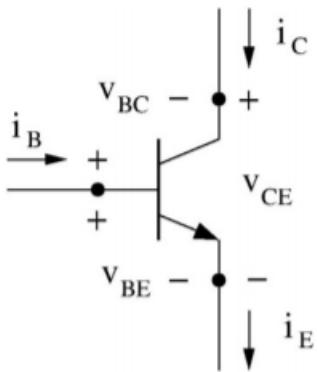
- Device construction is NOT symmetric
 - “Thin” base region (between E & C)
 - Heavily doped emitter
 - Large area collector

Cont.

BJT iv characteristics includes four parameters

NPN transistor

$$V_{bc} + V_{ce} = V_{be}$$



Circuit symbol and
Convention for current directions
(Note: $v_{CE} = v_C - v_E$)

- Six circuit variables: (3 i and 3 v)
- Two can be written in terms of the other four:

$$\text{KCL: } i_E = i_C + i_B$$

$$\text{KVL: } v_{BC} = v_{BE} - v_{CE}$$

- BJT iv characteristics is the relationship among (i_B , i_C , v_{BE} , and v_{CE})
 - It is typically derived as

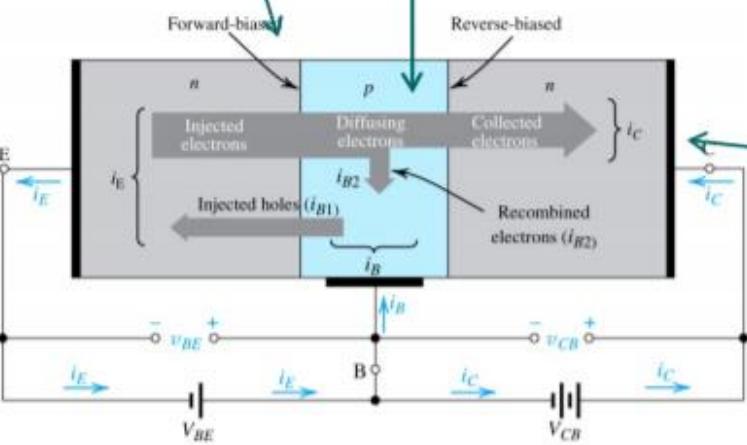
$$i_B = f(v_{BE})$$

$$i_C = g(i_B, v_{CE})$$

Cont.

BJT operation in the “active” mode

BE junction is forward biased
 $(v_{BE} = V_{D0})$



As Emitter is heavily doped, a large number of electrons diffuse into the base (only a small fraction combine with holes)

The number of these electrons scales as e^{v_{BE}/V_T}

- If the base is “thin” these electrons get near the depletion region of BC junction and are swept into the collector if $v_{CB} \geq 0$
($v_{BC} \leq 0$: BC junction is reverse biased!)

$$i_C = I_S e^{v_{BE}/V_T}$$

- In this picture, i_C is independent of v_{BC} (and v_{CE}) as long as

$$\begin{aligned} v_{BC} &= v_{BE} - v_{CE} = V_{D0} - v_{CE} \leq 0 \\ v_{CE} &\geq V_{D0} \end{aligned}$$

Active mode:

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

$$i_C = I_S e^{v_{BE}/V_T}$$

$$v_{CE} \geq V_{D0}$$

- Base current is also proportional to

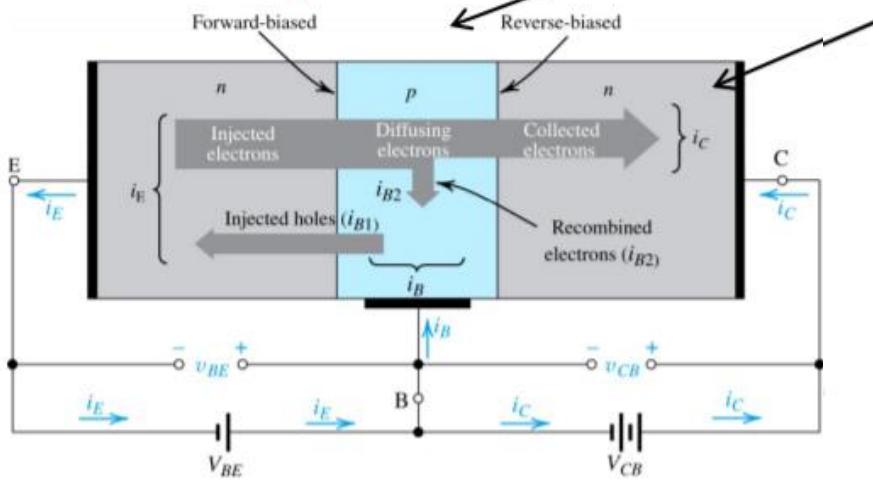
$$e^{v_{BE}/V_T} \text{ and therefore, } i_C : i_B = i_C / \beta$$

Cont.

BJT operation in saturation mode

BE junction is forward biased
($v_{BE} = V_{D0}$)

Similar to the active mode, a large number of electrons diffuse into the base.



“Deep” Saturation mode:

$$i_B = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

$$i_C < \beta i_B$$

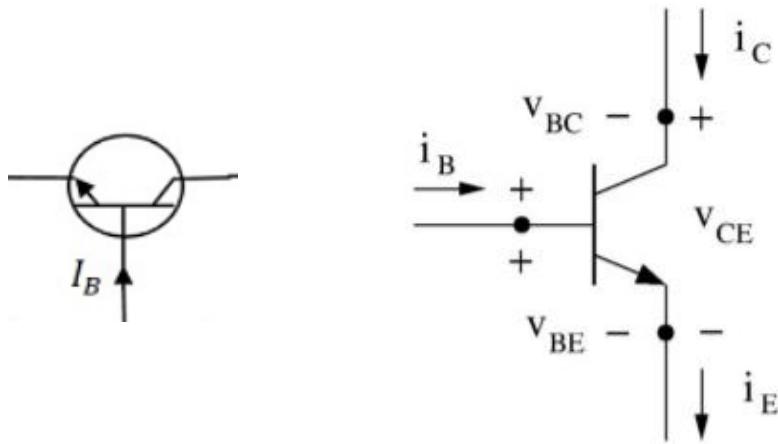
$$v_{CE} \approx V_{sat}$$

➤ For $v_{BC} \geq 0$ BC junction is forward biased and a diffusion current will set up, reducing i_C .

1. **Soft saturation:** $v_{CE} \geq 0.3$ V (Si)*
 $v_{BC} \leq 0.4$ V (Si), diffusion current is small and i_C is very close to its active-mode level.
2. **Deep saturation region:** $0.1 < v_{CE} < 0.3$ V (Si) or $v_{CE} \approx 0.2$ V = V_{sat} (Si), i_C is smaller than its active-mode level ($i_C < \beta i_B$).
 - Called saturation as i_C is set by outside circuit & does not respond to changes in i_B .
3. **Near cut-off:** $v_{CE} \leq 0.1$ V (Si)
Both i_C & i_B are close to zero.

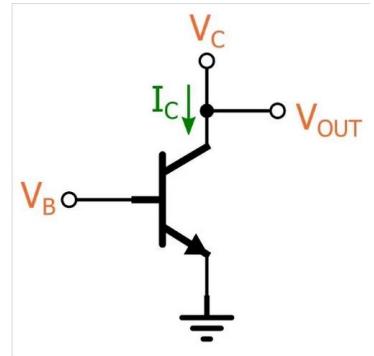
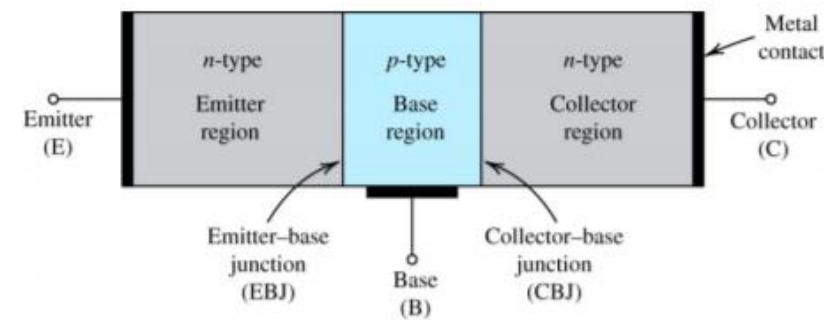
Cont.

BJT iv characteristics includes four parameters



Circuit symbol and
Convention for current directions
(Note: $v_{CE} = v_C - v_E$)

Simplified physical structure



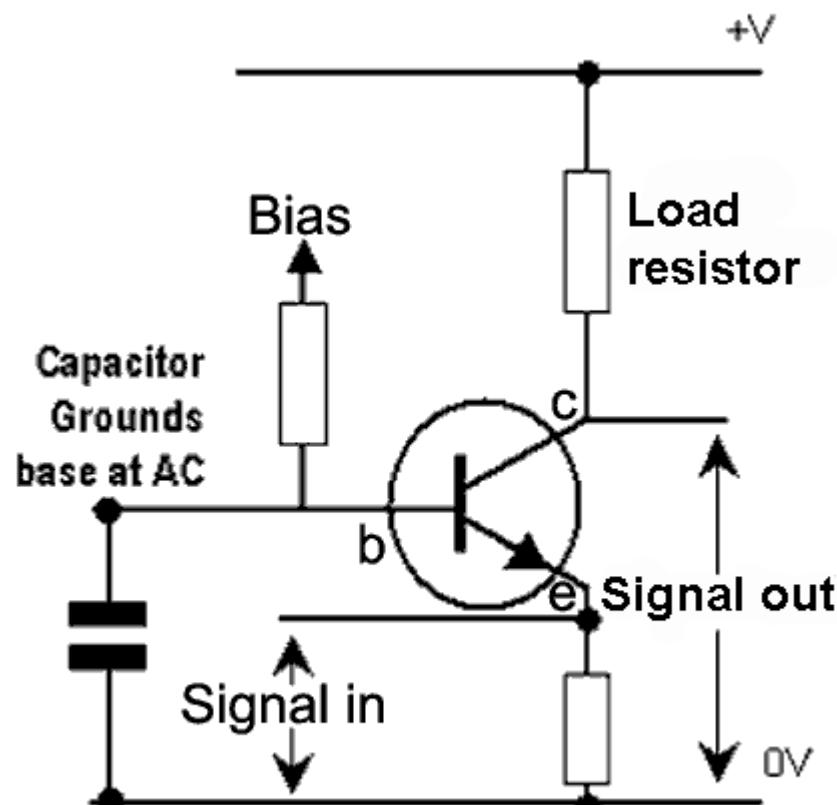
➤ BJT *iv* characteristics is the relationship among (i_B , i_C , v_{BE} , and v_{CE})

➤ It is typically derived as

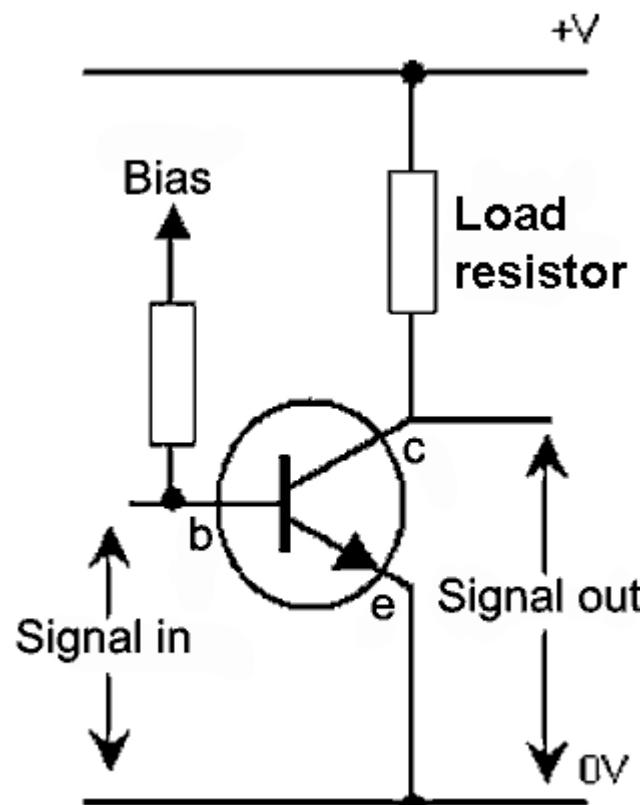
$$i_B = f(v_{BE})$$

$$i_C = g(i_B, v_{CE})$$

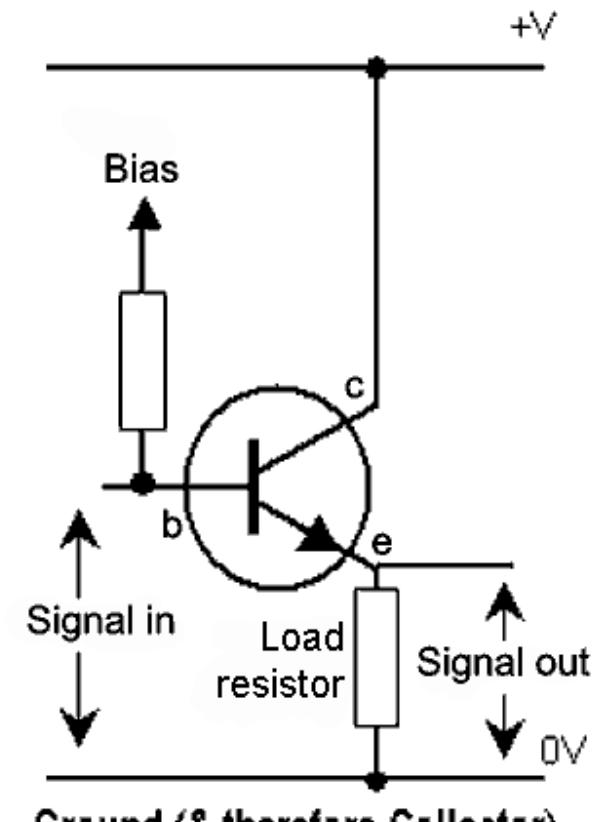
BJT Configurations



Ground (& Base) is Common to Input & Output



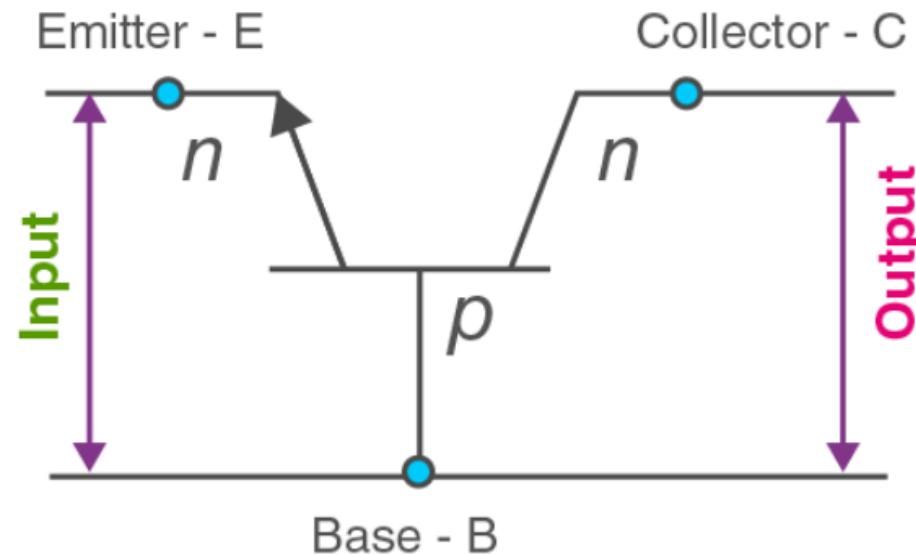
Emitter is common to input & Output



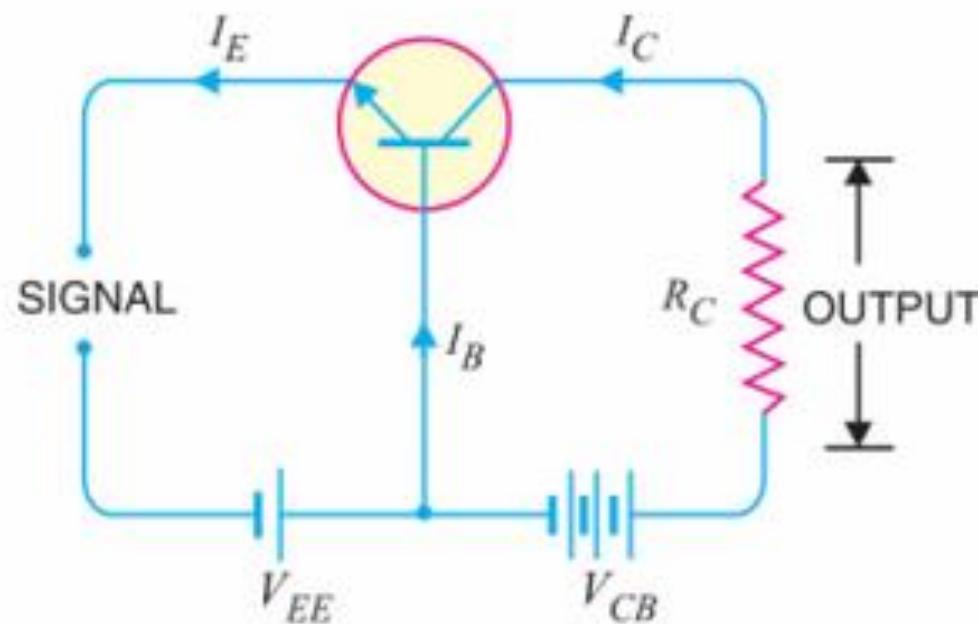
Ground (& therefore Collector)
is Common to Input & Output

Common Base (CB) Configuration of Transistor

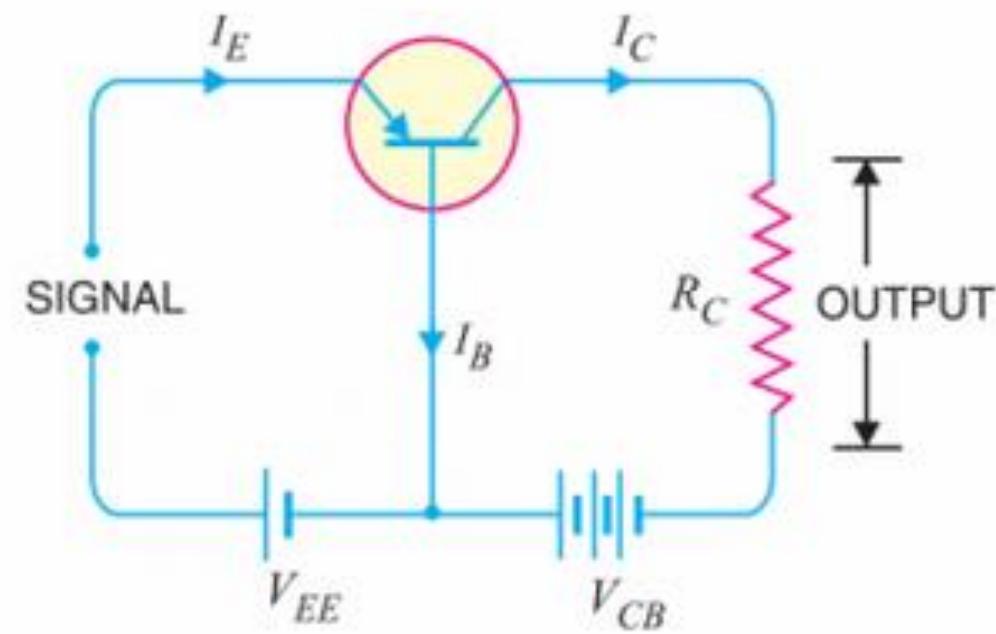
- In CB Configuration, the base terminal of the transistor will be connected common between the output and the input terminals.



Active Mode Biasing (NPN and PNP Tx)



(i)

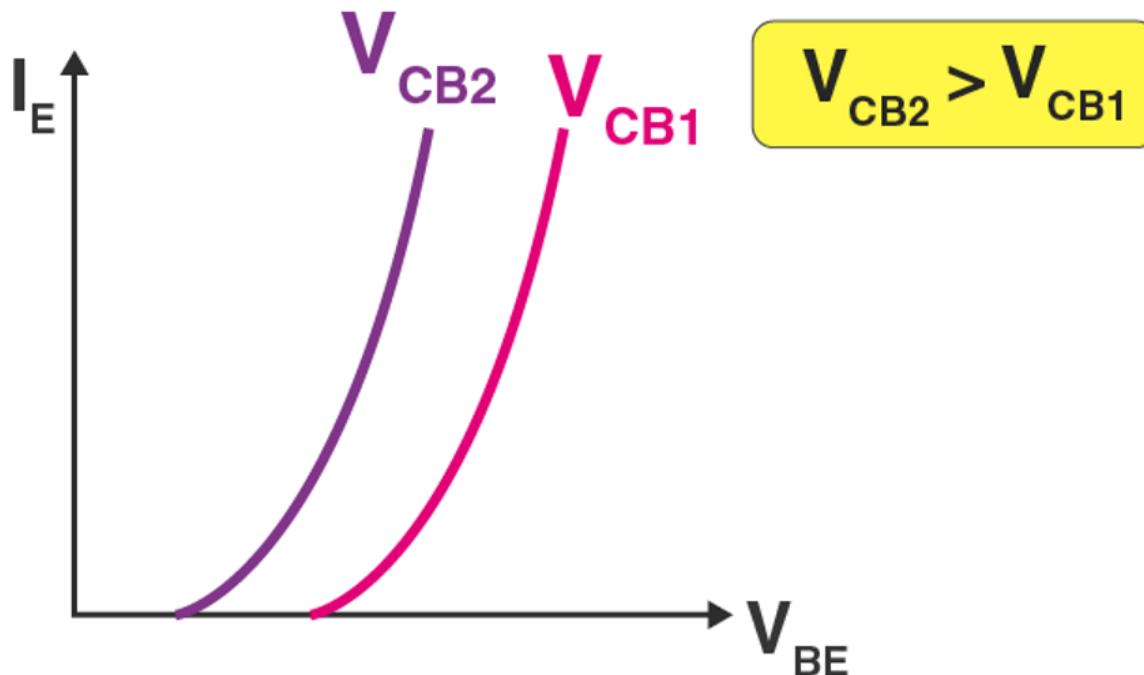


(ii)

Transistor Characteristics

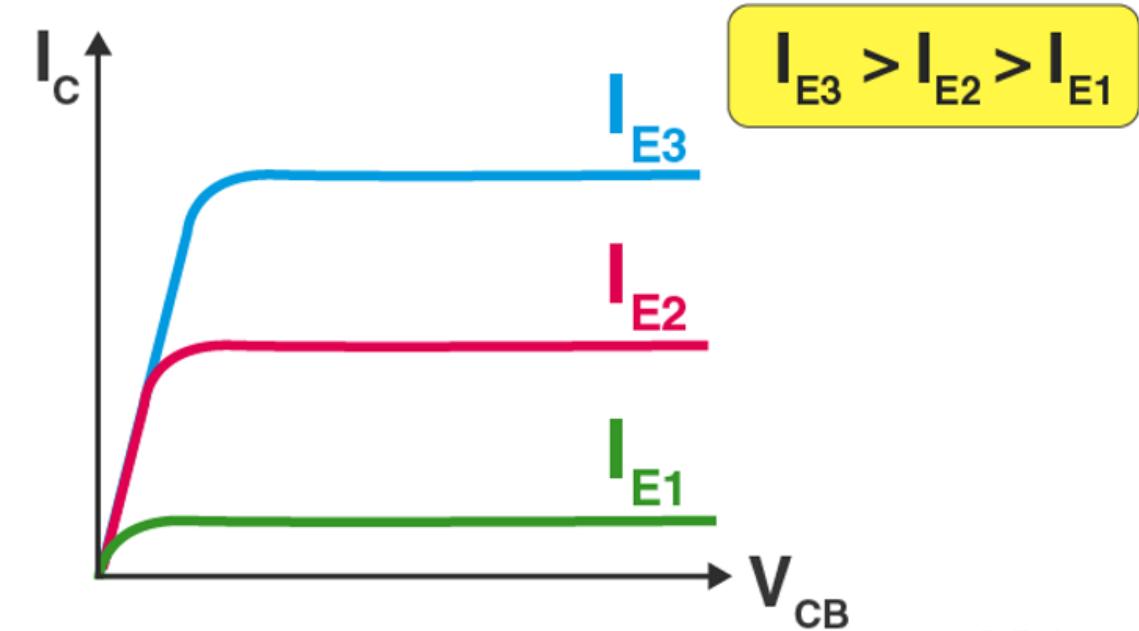
Input Characteristics

The variation of emitter current(I_E) with Base-Emitter voltage(V_{BE}), keeping Collector Base voltage(V_{CB}) constant.



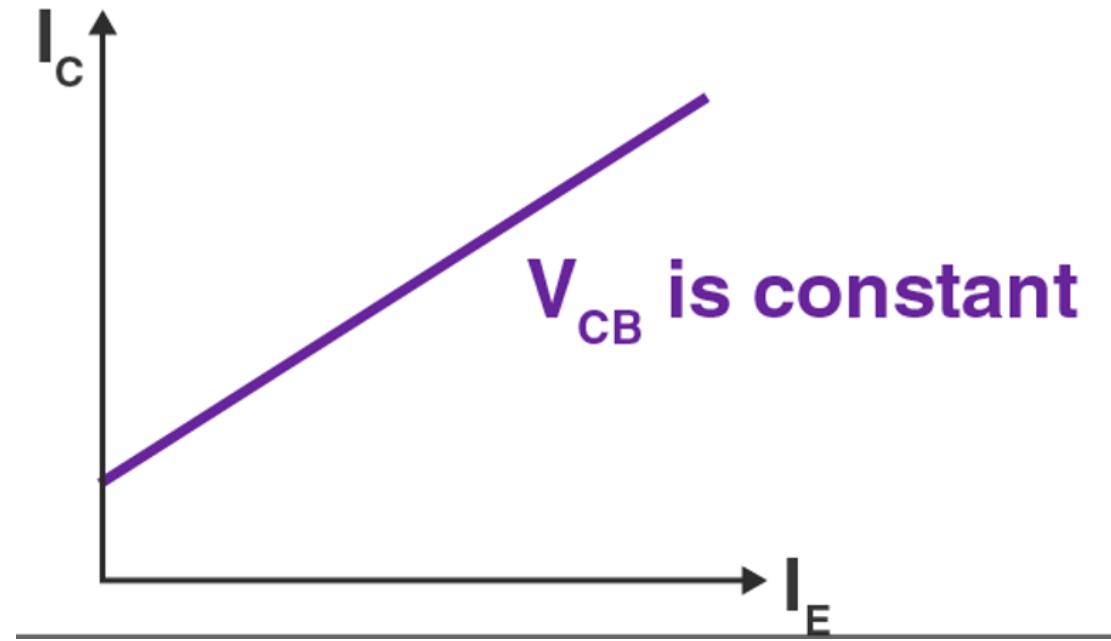
Output Characteristics

The variation of collector current(I_C) with Collector-Base voltage(V_{CB}), keeping the emitter current(I_E) constant



Cont.

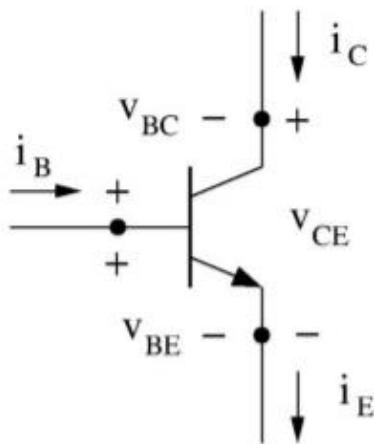
- **Current Transfer Characteristics**
- The variation of collector current(I_C) with the emitter current(I_E), keeping Collector Base voltage(V_{CB}) constant



$$\alpha = \frac{\Delta I_C}{\Delta I_B} | V_{CB} = Constant$$

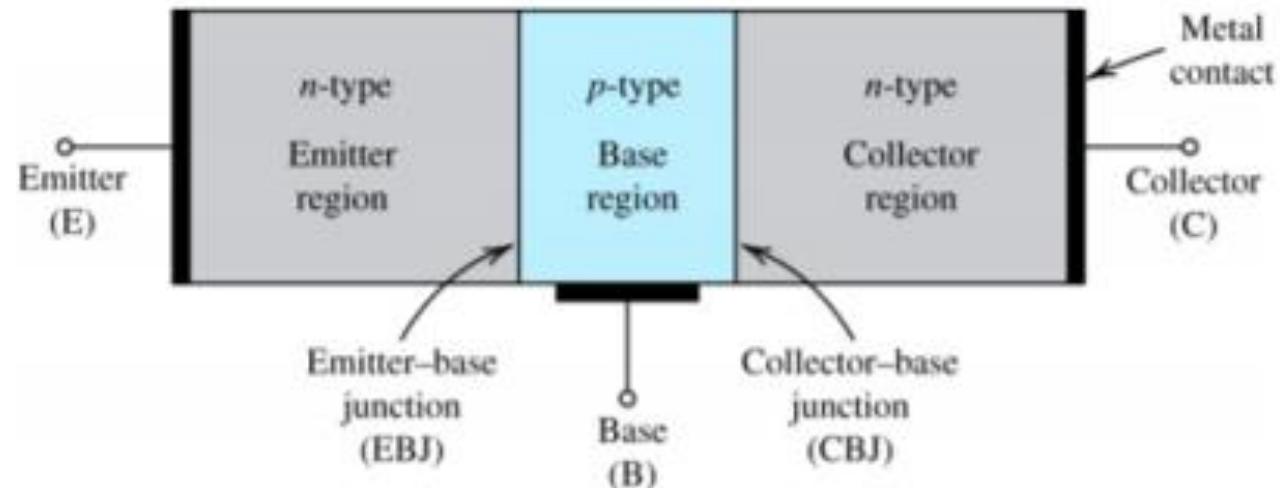
CE Configuration

BJT iv characteristics includes four parameters



Circuit symbol and Convention for current directions
(Note: $v_{CE} = v_C - v_E$)

Simplified physical structure



➤ BJT *iv* characteristics is the relationship among (i_B , i_C , v_{BE} , and v_{CE})

➤ It is typically derived as

$$i_B = f(v_{BE})$$

$$i_C = g(i_B, v_{CE})$$

Cont.

BJT iv characteristics:

$$i_B = f(v_{BE}) \quad \& \quad i_C = g(i_B, v_{CE})$$

Saturation:

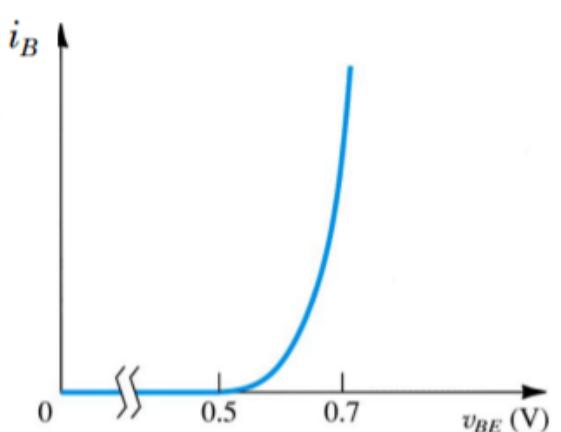
BE is forward biased, BC is forward biased

1. Soft saturation: $0.3 \leq v_{CE} \leq 0.7 \text{ V}$, $i_C \approx \beta i_B$
2. Deep saturation: $0.1 \leq v_{CE} \leq 0.3 \text{ V}$, $i_C < \beta i_B$
3. Near cut-off: $v_{CE} \leq 0.1 \text{ V}$, $i_C \approx 0$

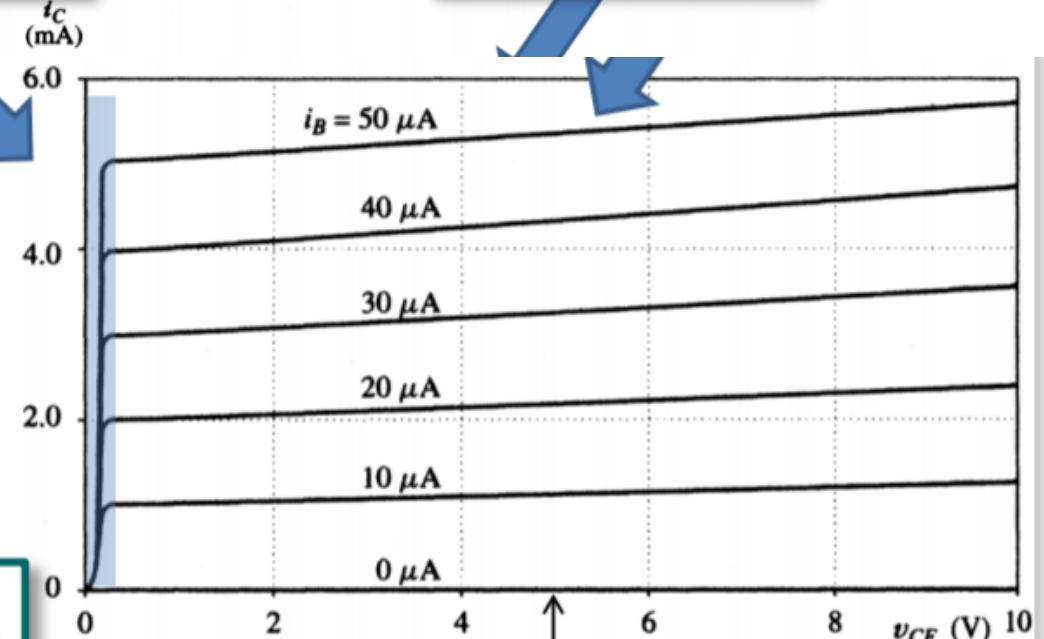
Active:

BE is forward biased
BC is reverse biased

$$i_C = \beta i_B$$



Cut-off :
BE is reverse biased
 $i_B = 0, \quad i_C = 0$



Cont.

NPN BJT iv equations

“Linear” model

Cut-off :
BE is reverse biased

$$i_B = 0, \quad i_C = 0$$

$$i_B = 0, \quad i_C = 0 \\ v_{BE} < V_{D0}$$

Active:
BE is forward biased
BC is reverse biased

$$i_B = \frac{i_C}{\beta} = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

$$i_C = I_S e^{v_{BE}/V_T} \left(1 + \frac{v_{CE}}{V_A} \right) \quad v_{BE} = V_{D0}, \quad i_B \geq 0 \\ i_C = \beta i_B, \quad v_{CE} \geq V_{D0}$$

(Deep) Saturation:
BE is forward biased
BC is reverse biased

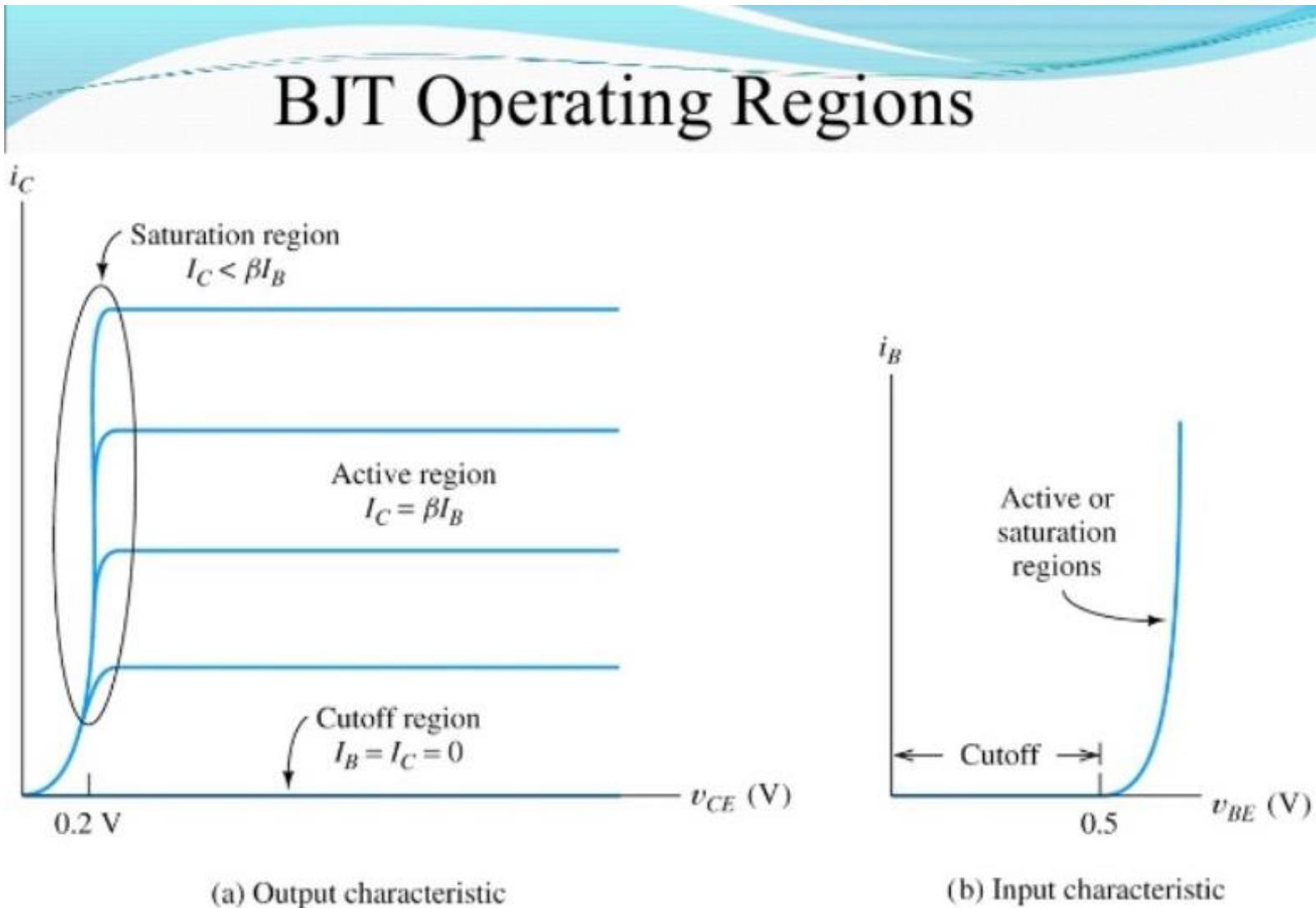
$$i_B = \frac{I_S}{\beta} e^{v_{BE}/V_T}$$

$$v_{CE} \approx V_{sat}, \quad i_C < \beta i_B$$

$$v_{BE} = V_{D0}, \quad i_B \geq 0 \\ v_{CE} = V_{sat}, \quad i_C < \beta i_B$$

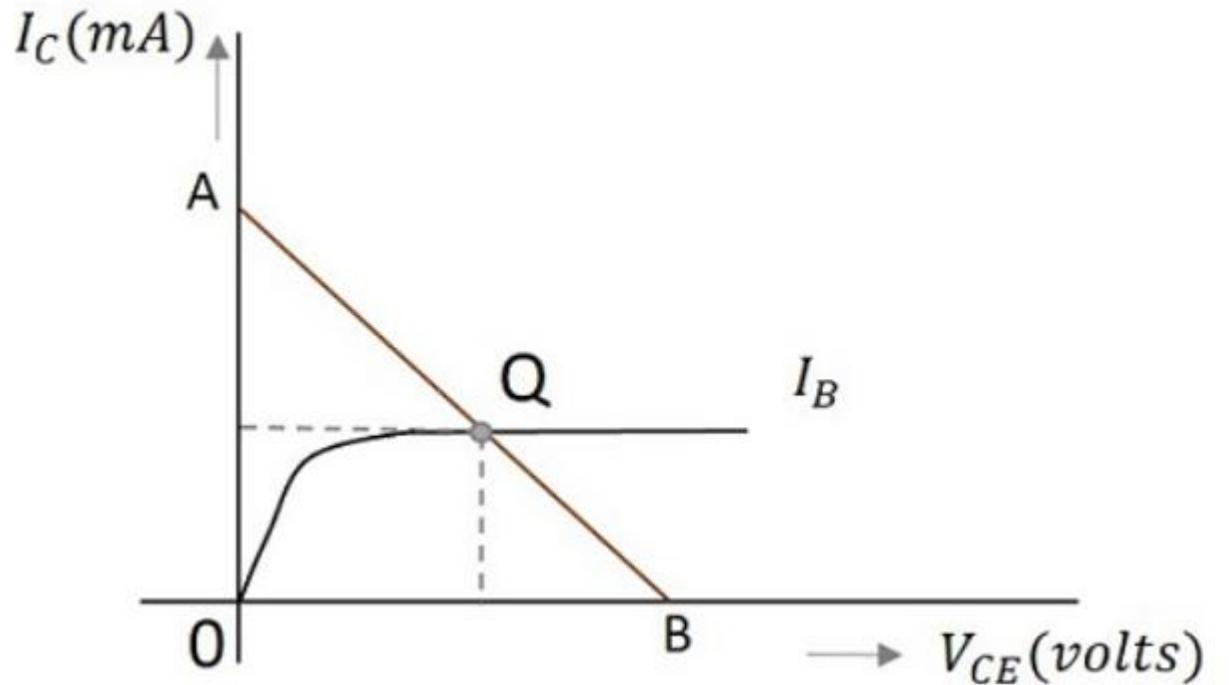
For Si, $V_{D0} = 0.7$ V, $V_{sat} = 0.2$ V

Load line and Operating point



Cont.

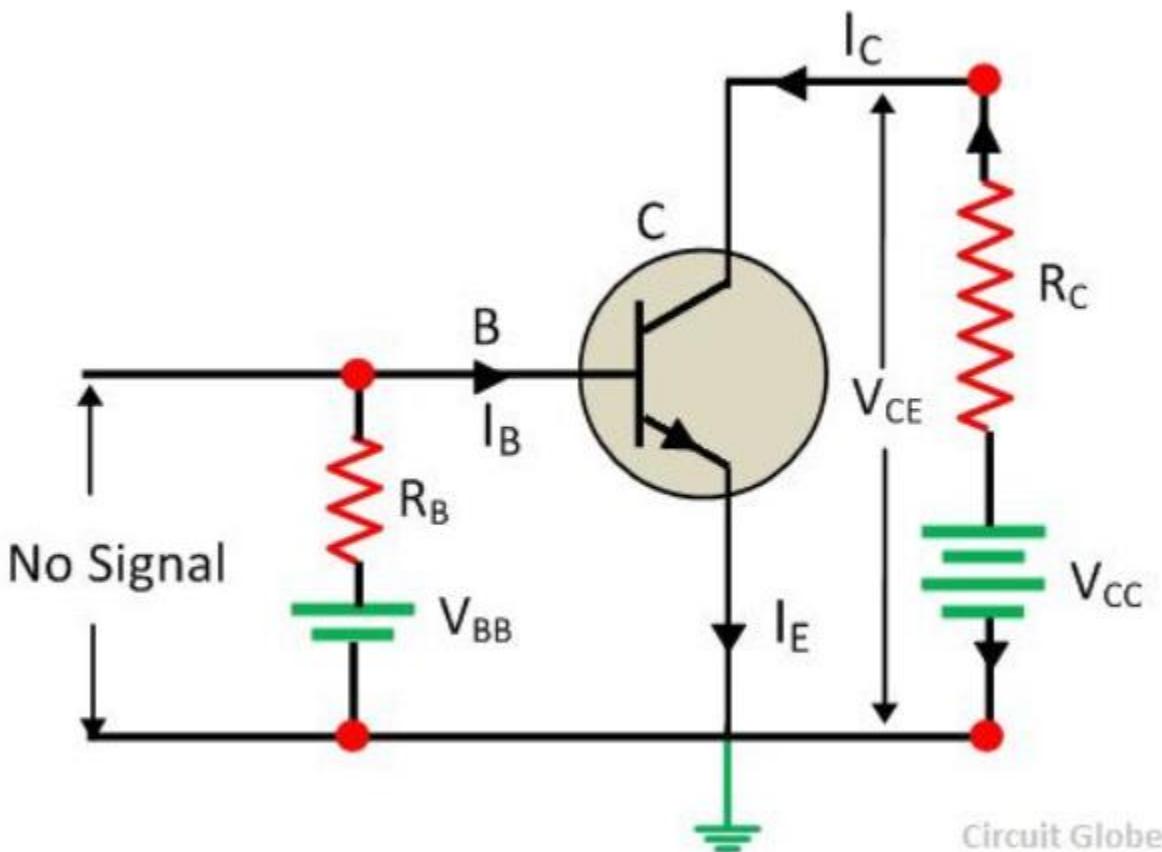
- When a value for the maximum possible collector current is considered, that point will be present on the Y-axis, which is nothing but the **saturation point**. As well, when a value for the maximum possible collector emitter voltage is considered, that point will be present on the X-axis, which is the **cutoff point**.
- When a line is drawn joining these two points, such a line can be called as **Load line**. This is called so as it symbolizes the output at the load. **This line, when drawn over the output characteristic curve, makes contact at a point called as Operating point.**
- This operating point is also called as **quiescent point** or simply **Q-point**. There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in active region. This can be better understood through the figure below.



- The load line has to be drawn in order to obtain the Q-point. A transistor acts as a good amplifier when it is in active region and when it is made to operate at Q-point, faithful amplification is achieved.

DC Load line

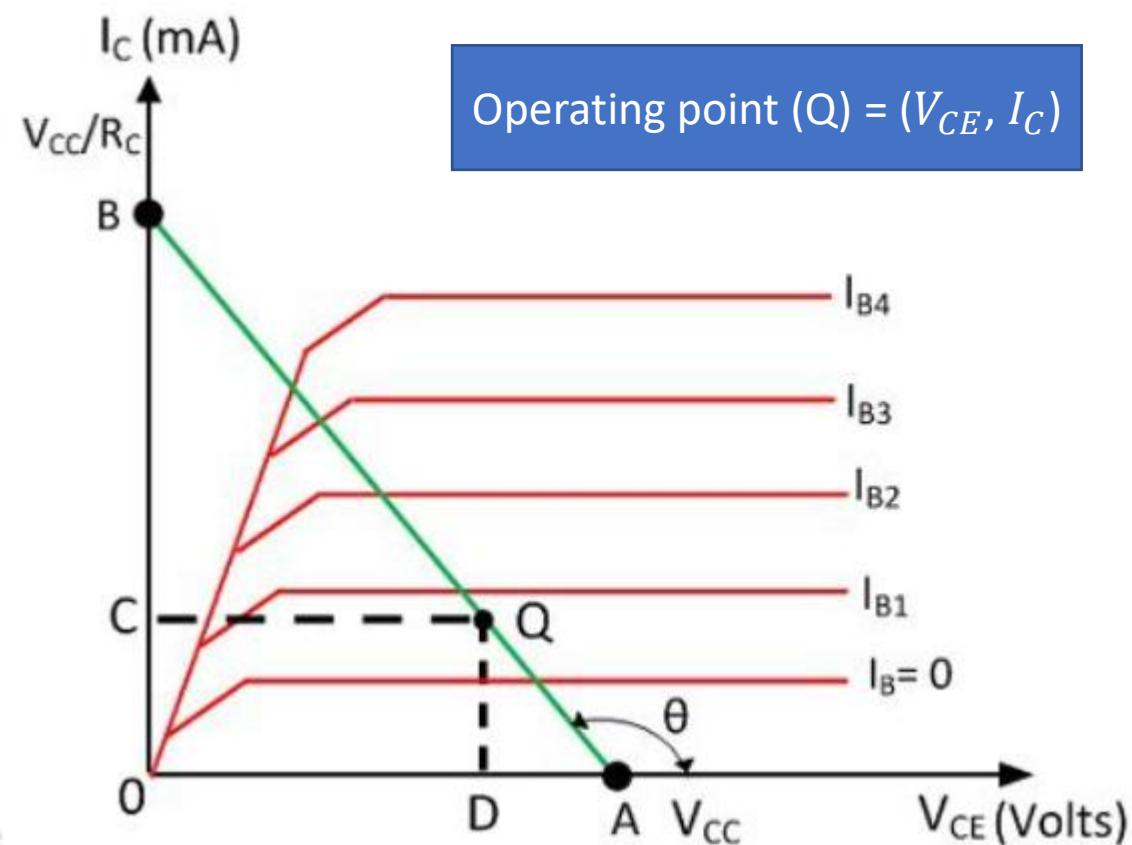
When the transistor is given the bias and no signal is applied at its input, the load line drawn at such condition, can be understood as **DC** condition.



The value of collector emitter voltage at any given time will be

$$V_{CE} = V_{CC} - I_C R_C$$

As V_{CC} and R_C are fixed values, the above one is a first-degree equation and hence will be a straight line on the output characteristics. This line is called as **D.C. Load line**. The figure below shows the DC load line.

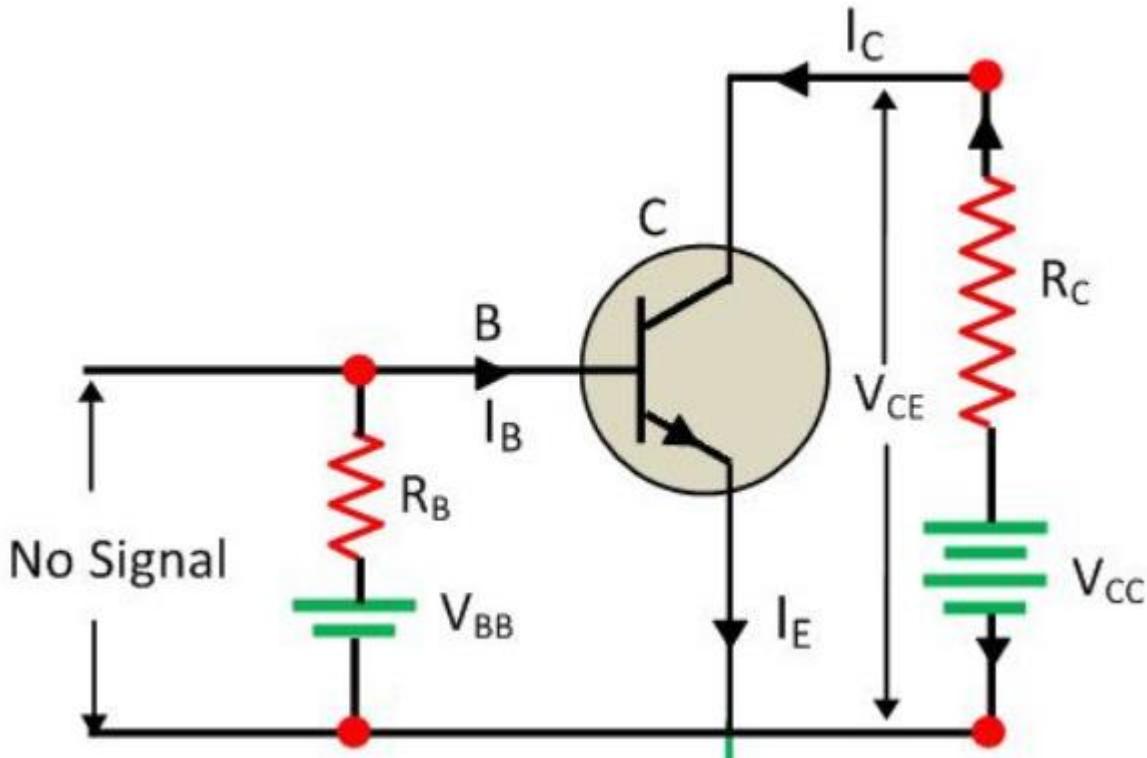


Cont.

By applying Kirchhoff's voltage law to the collector circuit, we get,

$$V_{CC} = V_{CE} + I_C R_C$$

$$V_{CE} = V_{CC} - I_C R_C \dots \text{equ(1)}$$



The above equation shows that the V_{CC} and R_C are the constant value, and it is the first-degree equation which is represented by the straight line on the output characteristic. This load line is known as a DC load line. The input characteristic is used to determine the locus of V_{CE} and I_C point for the given value of R_C . The end point of the line are located as

1. The collector-emitter voltage V_{CE} is maximum when the collector current $I_C = 0$ then from the equation (1) we get,

$$V_{CE} = V_{CC} - 0 \times R_C$$

$$V_{CE} = V_{CC}$$

The first point A ($OA = V_{CC}$) on the collector-emitter voltage axis shown in the figure above.

Cont.

- 2.** The collector current I_C becomes maximum when the collector-emitter voltage $V_{CE} = 0$ then from the equation (1) we get.

$$0 = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC}}{R_C}$$

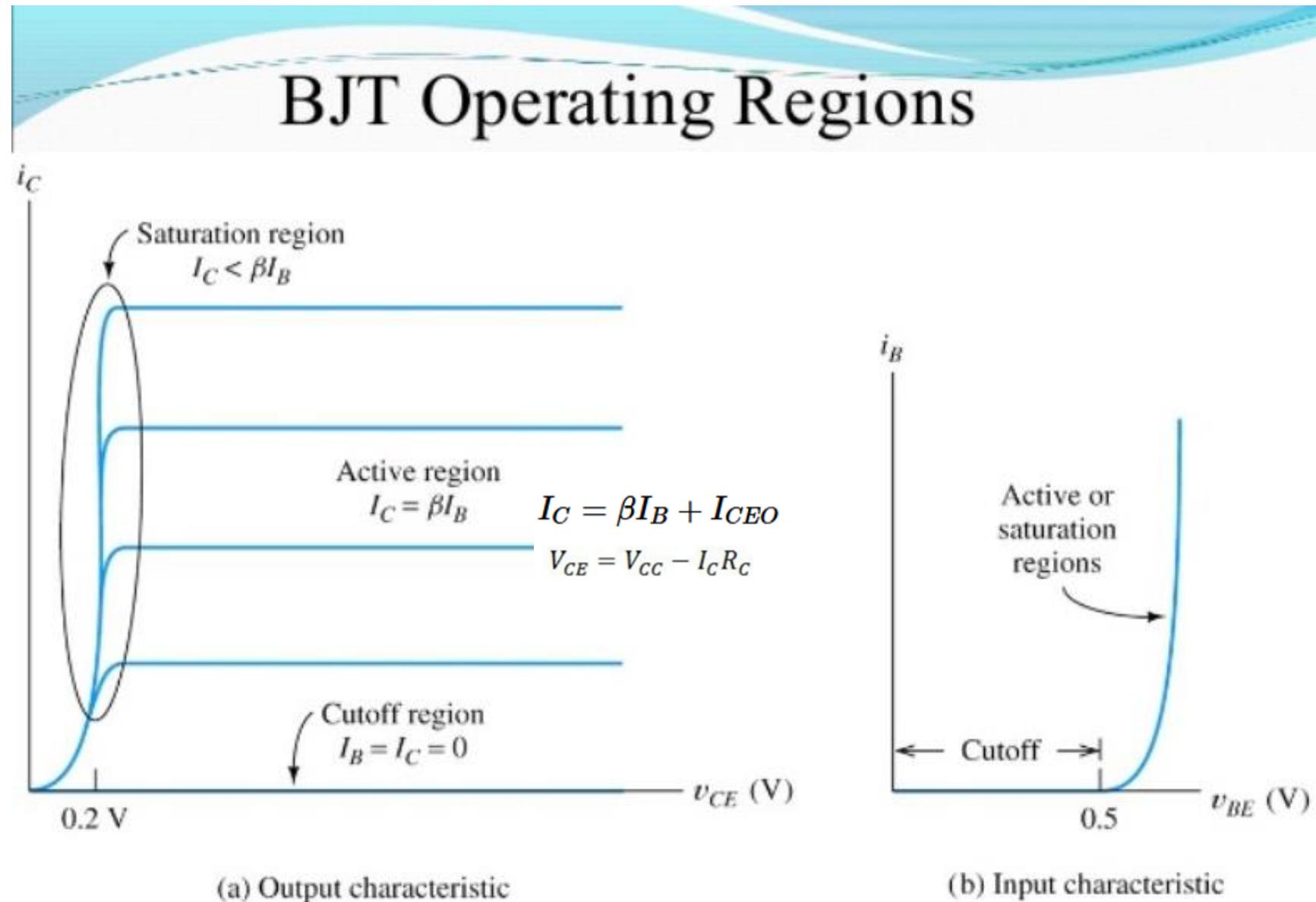
This gives the second point on the collector current axis as shown in the figure above.

By adding the points A and B, the DC load line is drawn. With the help of load line, any value of collector current can be determined.

Transistor Biasing

Biasing is the process of providing DC voltage which helps in the functioning of the circuit.

A transistor is biased in order to make the emitter base junction forward biased and collector base junction reverse biased, so that it maintains in active region, to work as an amplifier.



Cont.

Transistor Biasing

The proper flow of zero signal collector current and the maintenance of proper collectoremitter voltage during the passage of signal is known as **Transistor Biasing**. The circuit which provides transistor biasing is called as **Biasing Circuit**.

Need for DC biasing

If a signal of very small voltage is given to the input of BJT, it cannot be amplified. Because, for a BJT, to amplify a signal, two conditions have to be met.

- The input voltage should exceed **cut-in voltage** for the transistor to be **ON**.
- The BJT should be in the **active region**, to be operated as an **amplifier**.

If appropriate DC voltages and currents are given through BJT by external sources, so that BJT operates in active region and superimpose the AC signals to be amplified, then this problem can be avoided. The given DC voltage and currents are so chosen that the transistor remains in active region for entire input AC cycle. Hence DC biasing is needed.

Cont. As the expression for collector current I_C is

$$I_C = \beta I_B + I_{CEO} \quad V_{CE} = V_{cc} - I_c R_c$$

$$= \beta I_B + (\beta + 1)I_{CBO}$$

Factors affecting the operating point

The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.

$$V_{CE} = V_{cc} - I_c R_c$$

As temperature increases, the values of I_{CE} , β , V_{BE} gets affected.

- I_{CBO} gets doubled (for every 10° rise)
- V_{BE} decreases by 2.5mv (for every 1° rise)

So the main problem which affects the operating point is temperature. Hence operating point should be made independent of the temperature so as to achieve stability. To achieve this, biasing circuits are introduced.

Stabilization

The process of making the operating point independent of temperature changes or variations in transistor parameters is known as **Stabilization**.

Once the stabilization is achieved, the values of I_C and V_{CE} become independent of temperature variations or replacement of transistor. A good biasing circuit helps in the stabilization of operating point.

Need for Stabilization

Stabilization of the operating point has to be achieved due to the following reasons.

- Temperature dependence of I_C
- Individual variations
- Thermal runaway



Cont.

Temperature Dependence of I_C

As the expression for collector current I_C is

$$I_C = \beta I_B + I_{CEO}$$

$$= \beta I_B + (\beta + 1) I_{CBO}$$

The collector leakage current I_{CBO} is greatly influenced by temperature variations. To come out of this, the biasing conditions are set so that zero signal collector current $I_C = 1$ mA. Therefore, the operating point needs to be stabilized i.e. it is necessary to keep I_C constant.

Individual Variations

As the value of β and the value of V_{BE} are not same for every transistor, whenever a transistor is replaced, the operating point tends to change. Hence it is necessary to stabilize the operating point.

Cont.

Thermal Runaway

As the expression for collector current I_C is

$$I_C = \beta I_B + I_{CEO}$$

$$= \beta I_B + (\beta + 1)I_{CBO}$$

The flow of collector current and also the collector leakage current causes heat dissipation. If the operating point is not stabilized, there occurs a cumulative effect which increases this heat dissipation.

The self-destruction of such an unstabilized transistor is known as Thermal run away.

In order to avoid thermal runaway and the destruction of transistor, it is necessary to stabilize the operating point, i.e., to keep I_C constant.

Stability Factor

It is understood that I_C should be kept constant in spite of variations of I_{CBO} or I_{CO} . The extent to which a biasing circuit is successful in maintaining this is measured by **Stability factor**. It is denoted by **S**.

By definition, the rate of change of collector current I_C with respect to the collector leakage current I_{CO} at constant β and I_B is called **Stability factor**.

$$S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

Hence we can understand that any change in collector leakage current changes the collector current to a great extent. The stability factor should be as low as possible so that the collector current doesn't get affected. **S=1** is the ideal value.

Cont.

The general expression of stability factor for a CE configuration can be obtained as under.

$$I_C = \beta I_B + (\beta + 1) I_{CO}$$

Differentiating above expression with respect to I_C , we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

Differentiating above expression with respect to I_C , we get

$$1 = \beta \frac{dI_B}{dI_C} + (\beta + 1) \frac{dI_{CO}}{dI_C}$$

$$1 = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S}$$

$$\text{Since } \frac{dI_{CO}}{dI_C} = \frac{1}{S}$$

$$S = \frac{\beta + 1}{1 - \beta \left(\frac{dI_B}{dI_C} \right)}$$

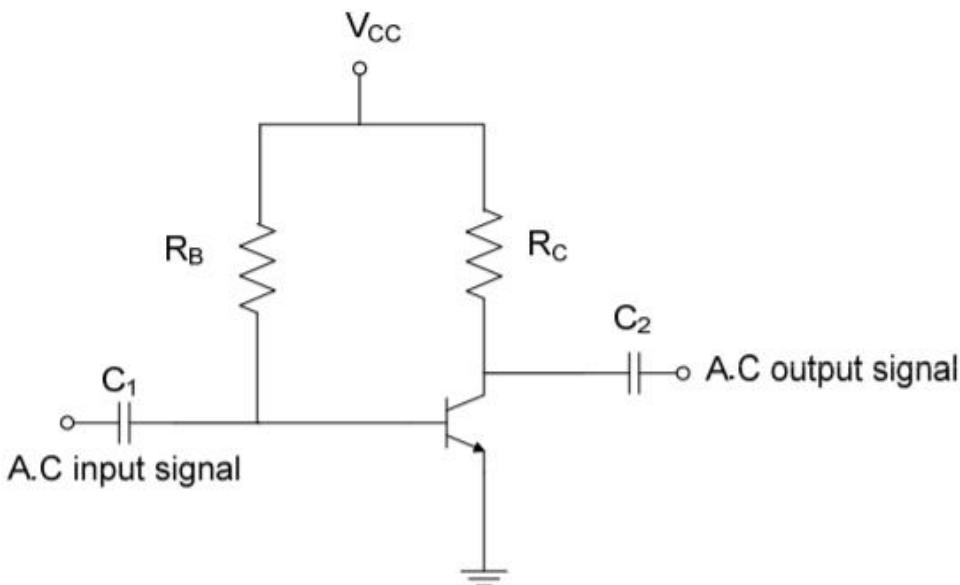
Hence the stability factor S depends on β , I_B and I_C .

Biassing method for Transistor

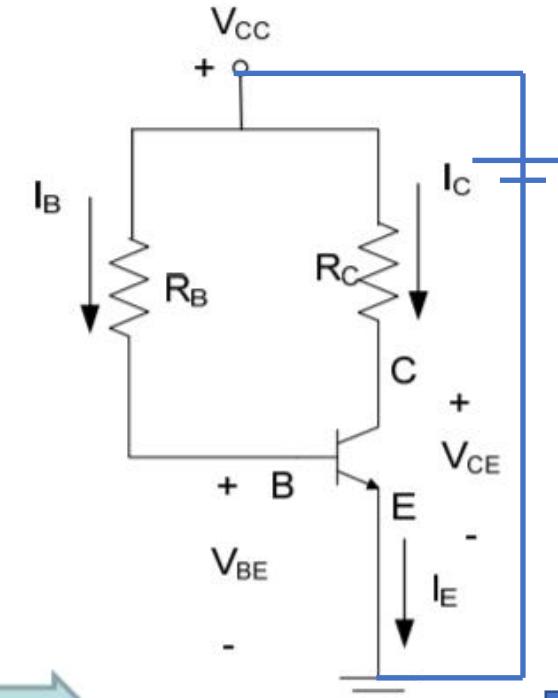
- **Fixed Bias**
- **Collector to base bias (Self Bias)**
- Voltage divider bias (Combinational Bias of Above two)

Fixed Bias

- This form of biasing is also called *base bias*. The single power source is used for both collector and base of transistor, although separate batteries can also be used.



D.C. Equivalent



Using KVL in the base-emitter loop

$$V_{CC} - I_B R_B - V_{BE} = 0 ; I_B = (V_{CC} - V_{BE}) / R_B$$

$$I_C = \beta I_B = \beta (V_{CC} - V_{BE}) / R_B$$

Using KVL in the collector-emitter loop

$$V_{CC} - I_C R_C - V_{CE} = 0 ; V_{CE} = V_{CC} - I_C R_C$$

$Q(V_{CE}, I_C)$ is set

- + = + -

$$V_{CC} = I_C R_C + V_{CE}$$

Fixed Bias

Advantages:

- Operating point can be shifted easily anywhere in the active region by merely changing the base resistor (R_B).
- A very small number of components are required.

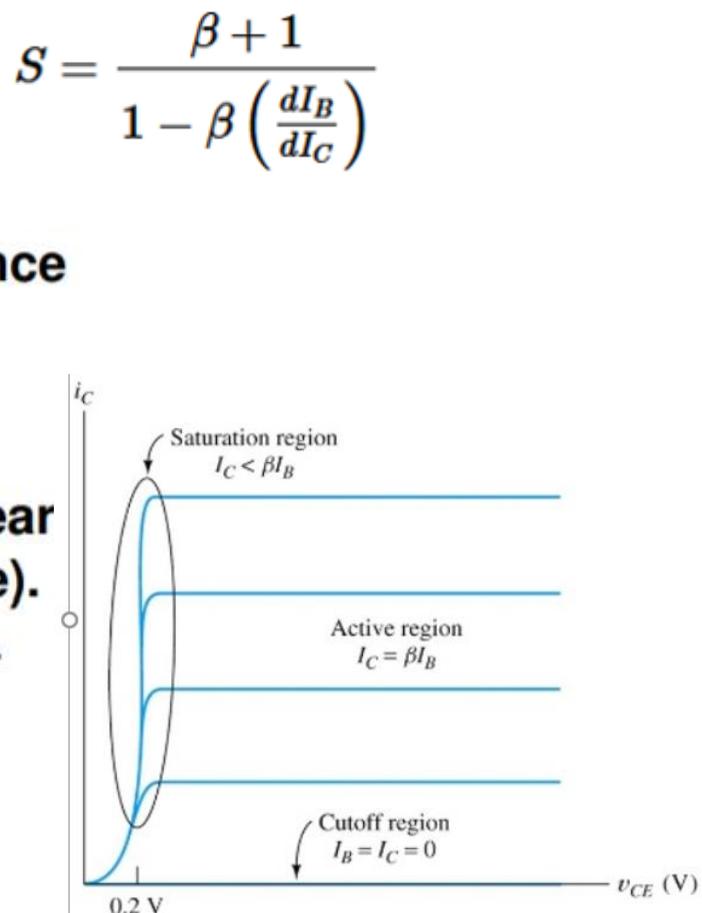
Disadvantages:

- Poor stabilization
- High stability factor ($S = \beta + 1$ because I_B is constant so $dI_B/dI_C = 0$), hence prone to thermal runaway

Usage:

- Due to the above inherent drawbacks, fixed bias is rarely used in linear circuits (i.e., those circuits which use the transistor as a current source). Instead, it is often used in circuits where transistor is used as a switch.

How the Q point is affected by changes in V_{BE} and I_{CBO} in fixed bias?



$$I_B = (V_{CC} - V_{BE}) / R_B \quad I_C = \beta I_B$$

Collector base bias (Self Bias)

- This configuration employs negative feedback to prevent thermal runaway and stabilize the operating point.
- In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{cc} .
- So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current.

Applying KVL

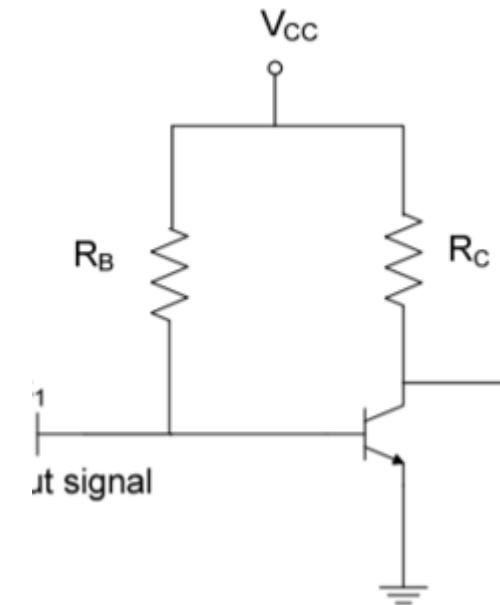
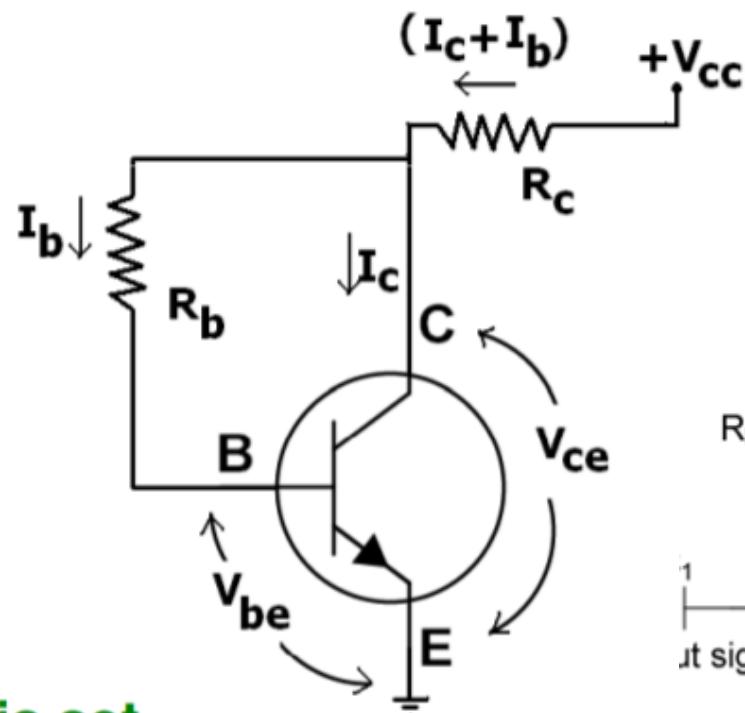
$$V_{cc} = (I_C + I_B)R_C + V_{CE} \quad (1)$$

$$V_{CE} = I_B R_B + V_{BE} \quad (2)$$

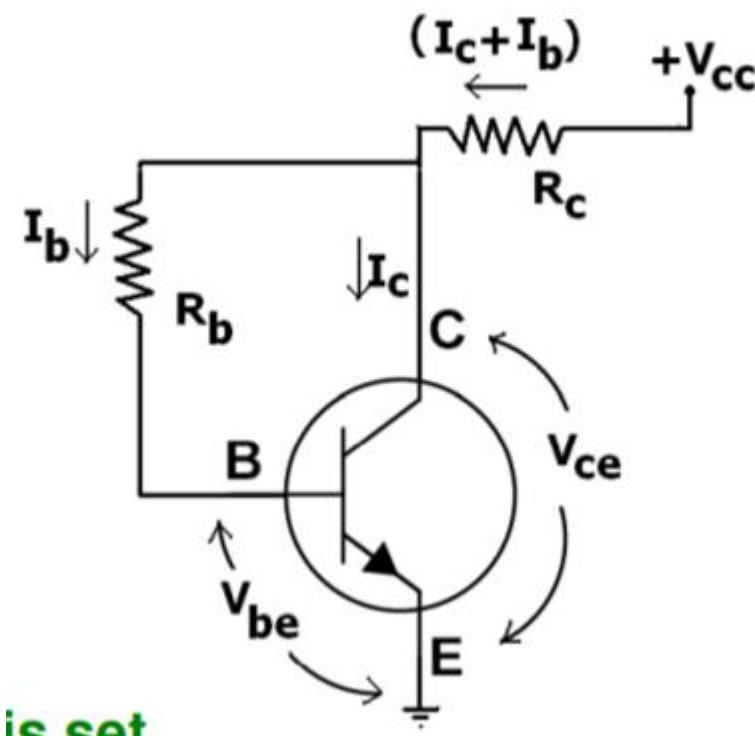
Since, $I_C = \beta I_B$ so from equation (1) & (2)

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (1 + \beta)R_C}$$

Q(V_{CE} , I_C) is set



Stability Factor



KVL to input loop:

$$V_{CC} = R_C (I_B + I_C) + I_B R_B + V_{BE}$$

$$V_{CC} = I_B (R_B + R_C) + I_C R_C + V_{BE}$$

$$I_B (R_B + R_C) = V_{CC} - V_{BE} - I_C R_C$$

$$(or) \quad I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C} \quad \text{--- ①}$$

Stability factor $s = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}}$

\therefore Differentiating eqn ① w.r.t. I_C , we get

$$\frac{dI_B}{dI_C} = - \frac{R_C}{R_B + R_C}$$

$$\therefore \boxed{S = \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_B + R_C} \right)}}$$

Cont.

Comment:

✓ If $R_B \ll \beta R_C$,

$$s \approx \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_C} \right)} \approx 1$$

✓ Provides better thermal stability by making $R_B \ll \beta R_C$

✓ Stability factor is very much less than that of fixed bias circuit //

Cont.

Advantages:

- Better stabilization compared to fixed bias

Disadvantages:

- This circuit provides negative feedback which reduces the gain of the amplifier.

Usage:

- The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

How the bias stability is improved in collector base bias?

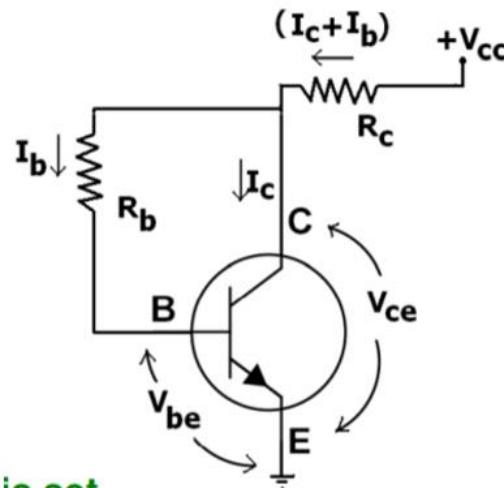
If I_C becomes larger than design value, it causes an increase voltage drop across R_C hence smaller value of V_{CE} which in turn causes I_B to be smaller than its design value. Since $I_C = \beta I_B$ thus I_C will also tend to be reduced towards its original value.

For bias Stabilization : $R_B \ll \beta R_C$

$$I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_C} \right]$$

If $R_B \ll \beta R_C$

$$I_C = \frac{V_{CC} - V_{BE}}{R_C}$$

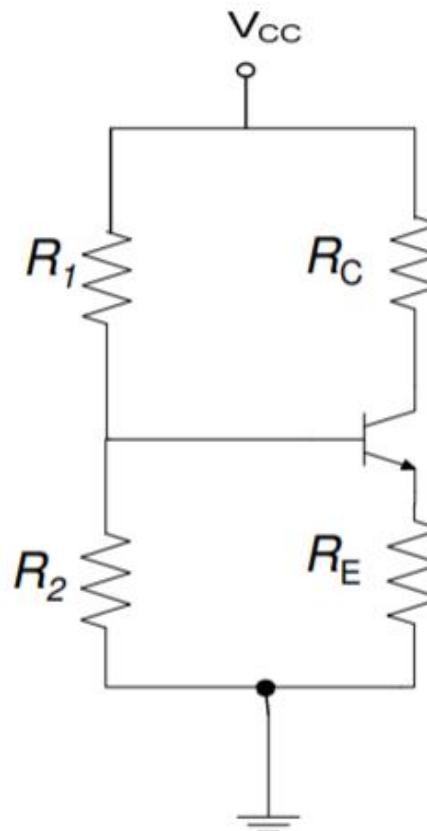
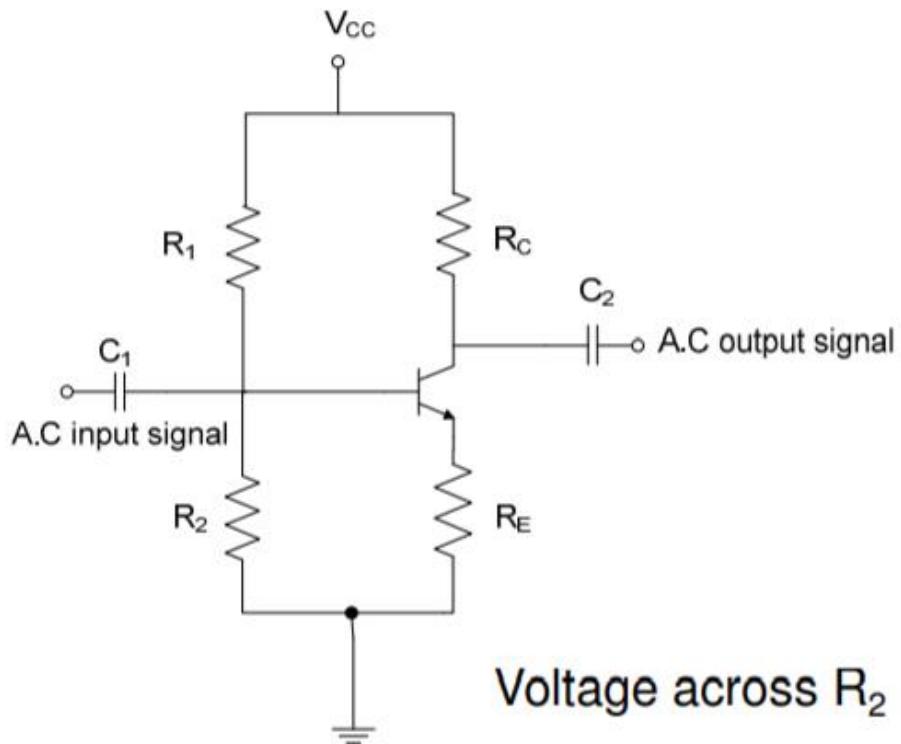


$$V_{CC} = (I_C + I_B)R_C + V_{CE}$$

$$V_{CE} = I_B R_B + V_{BE}$$

Voltage Divider Bias

- This is the most widely used method to provide biasing and stabilization to a transistor.
- In this form of biasing, R_1 and R_2 divide the supply voltage V_{CC} and voltage across R_2 provide fixed bias voltage V_B at the transistor base.
- Also a resistance R_E is included in series with the emitter that provides the stabilization.



V_B = Voltage across R_2
(ignoring base current)

$$V_B = V_{CC} \frac{R_2}{(R_1 + R_2)}$$

Cont.

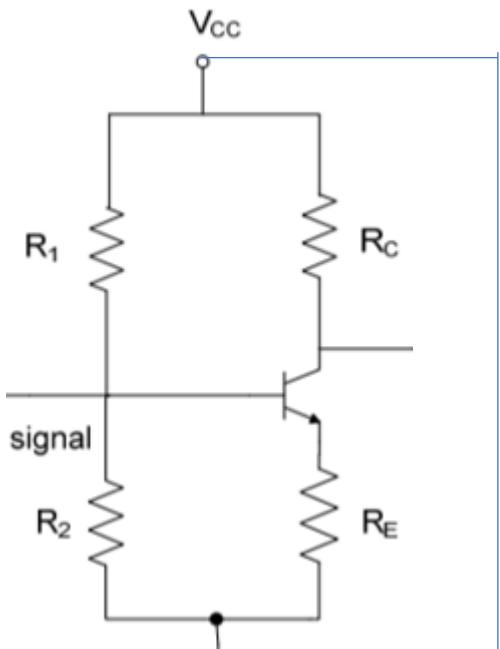
Voltage Divider Bias

$$V_B = V_{Th} = V_{CC} \frac{R_2}{(R_1 + R_2)} \quad R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{(R_1 + R_2)}$$

Base-Emitter Loop

$$V_{Th} - I_B R_{Th} - V_{BE} - (\beta + 1) I_B R_E = 0$$

$$\text{or, } I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$



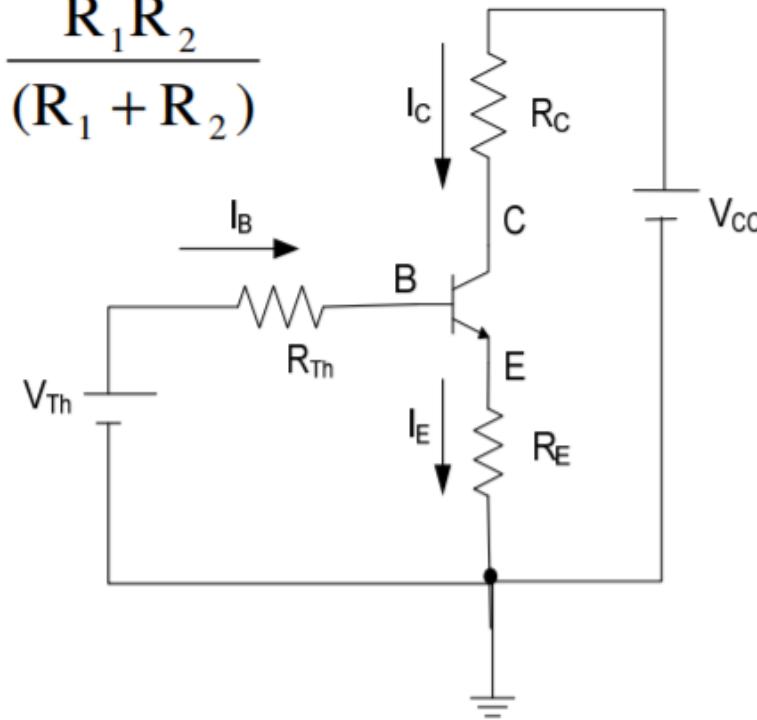
Collector- Emitter Loop

$$I_C = \beta I_B = \frac{\beta(V_{Th} - V_{BE})}{R_{Th} + (\beta + 1) R_E}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = V_{CC} - I_C R_C - (I_C + I_B) R_E$$

For bias Stabilization : $R_{Th} \ll (\beta+1)R_E$

$$I_C \approx \frac{V_{Th} - V_{BE}}{R_E}$$



Cont.

Stability factor for Voltage Divider Bias

$$S = \frac{(\beta + 1)}{1 - \beta \left(\frac{dI_B}{dI_C} \right)} \quad V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

(1) $V_{Th} = I_B R_{Th} - V_{BE} - (I_B + I_C) R_E$

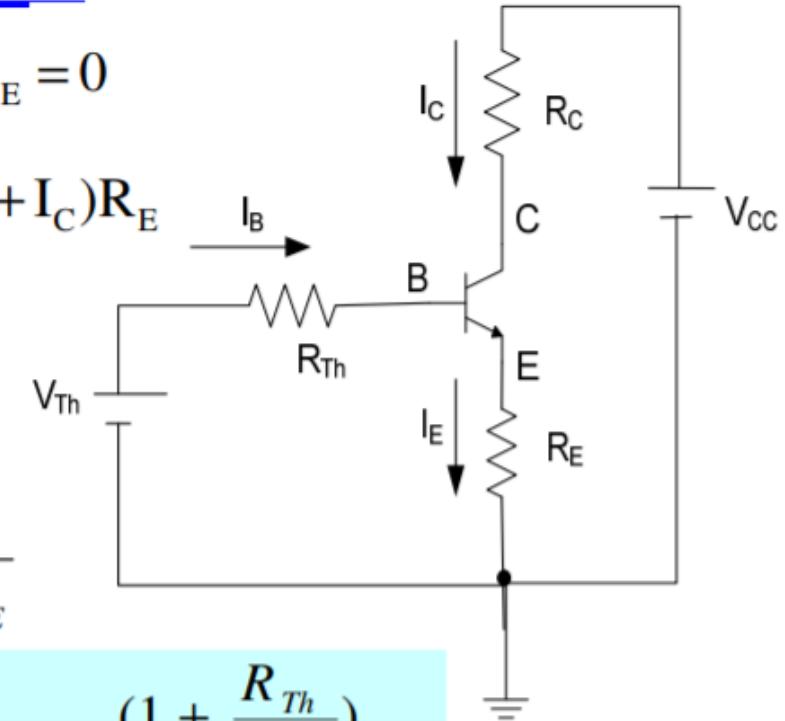
Differentiating equation (1) w.r.t I_C

$$V_{Th} = I_B R_{Th} - V_{BE} - (I_B + I_C) R_E$$

$$0 = R_{Th} \left(\frac{dI_B}{dI_C} \right) + (1 + \frac{dI_B}{dI_C}) R_E \quad \frac{dI_B}{dI_C} = -\frac{R_E}{R_{Th} + R_E}$$

$$S = (\beta + 1) \frac{(R_{Th} + R_E)}{R_E (\beta + 1) + R_{Th}}$$

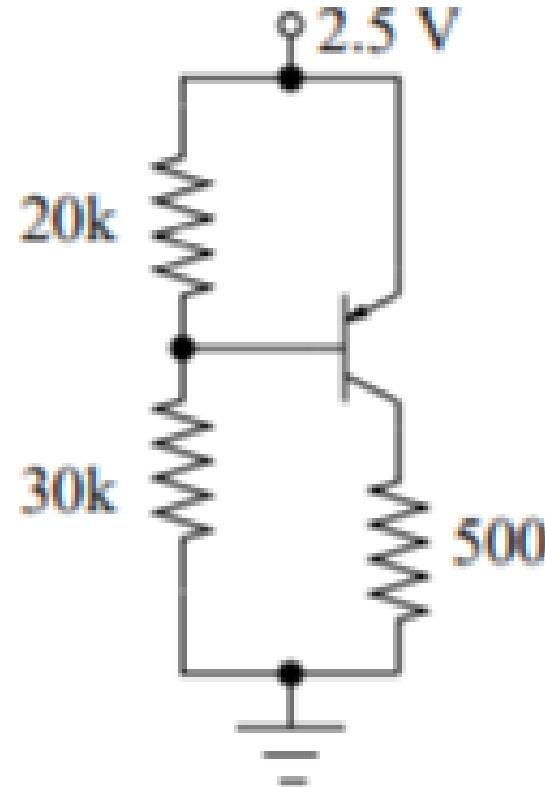
$$S = (\beta + 1) \frac{\left(1 + \frac{R_{Th}}{R_E}\right)}{(\beta + 1) + \frac{R_{Th}}{R_E}}$$



➤ For stability, S should be small which can be achieved by making R_{Th}/R_E small. For very small R_{Th}/R_E ; $S = 1$ (ideal case)

➤ For very small R_{Th}/R_E : $R_2 \downarrow \longrightarrow R_{Th}$ current drawn by R_2 will be large.
 $R_E \uparrow \longrightarrow$ Large V_{cc} required. Hence compromise is made in selection.

Problem 1. Find the bias point of the transistor (Si BJT with $\beta = 100$ and $V_A \rightarrow \infty$).



Solution

This is a fixed bias scheme (because there is no R_E) with a voltage divider providing V_{BB} (It is unstable to temperature changes, see problem 2).

Assuming BJT (PNP) in the active state and replacing R2/R1 voltage divider with its Thevenin equivalent:

$$R_B = 30 \text{ k} \parallel 20 \text{ k} = 12 \text{ k}, \quad V_{BB} = \frac{30}{30 + 20} \times 2.5 = 1.5 \text{ V}$$

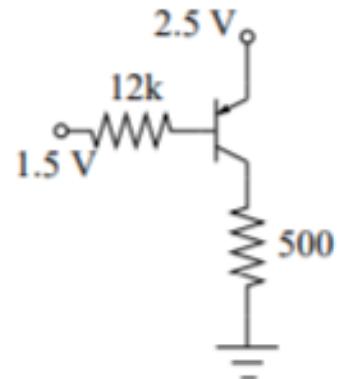
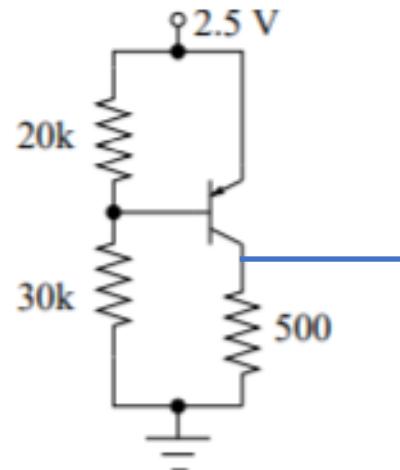
$$\text{EB-KVL: } 2.5 = V_{EB} + 12 \times 10^3 I_B + 1.5$$

$$I_B = (2.5 - 1.5 - 0.7)/(12 \times 10^3) = 25 \mu\text{A}$$

$$I_C = \beta I_B = 2.5 \text{ mA}$$

$$\text{EC-KVL: } 2.5 = V_{EC} + 500 I_C$$

$$V_{EC} = 2.5 - 500 \times 2.5 \times 10^{-3} = 1.25 \text{ V}$$

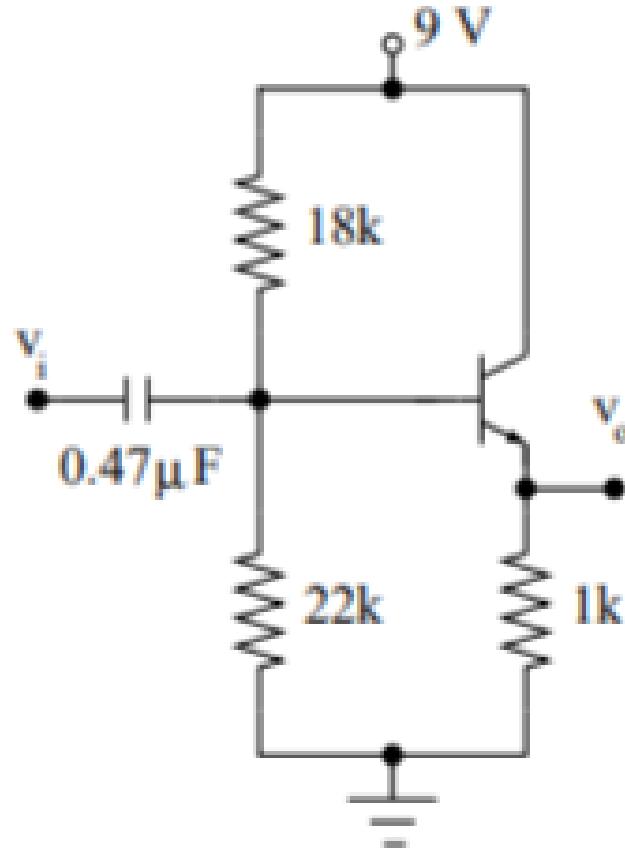


Since $V_{EC} \geq 0.7 \text{ V}$ and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{EC} = 1.25 \text{ V}$, $I_C = 2.5 \text{ mA}$, and $I_B = 25 \mu\text{A}$.

Problem 2

Find the bias point (Si BJT with $\beta = 200$ and $V_A \rightarrow \infty$).



Solution

Assume BJT (NPN) in active. Replace R_1/R_2 voltage divider with its Thevenin equivalent (note capacitors are open):

$$R_B = 18 \text{ k} \parallel 22 \text{ k} = 9.9 \text{ k}, \quad V_{BB} = \frac{22}{18+22} \times 9 = 4.95 \text{ V}$$

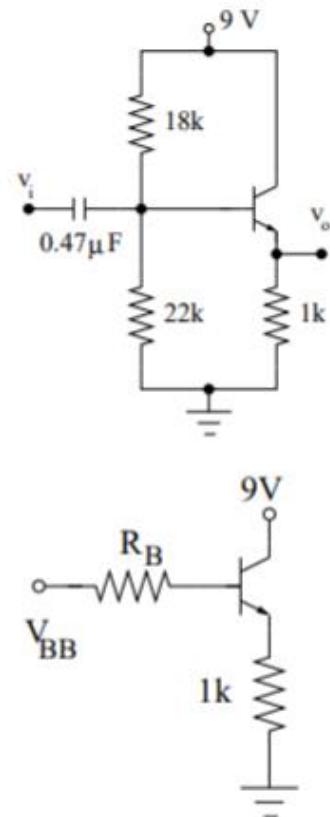
$$\text{BE-KVL: } V_{BB} = R_B I_B + V_{BE} + 10^3 I_E \quad I_B = \frac{I_E}{1+\beta} = \frac{I_E}{201}$$

$$4.95 - 0.7 = I_E \left(\frac{9.9 \times 10^3}{201} + 10^3 \right)$$

$$I_E = 4 \text{ mA} \approx I_C, \quad I_B = \frac{I_C}{\beta} = 20 \mu\text{A}$$

$$\text{CE-KVL: } V_{CC} = V_{CE} + 10^3 I_E$$

$$V_{CE} = 9 - 10^3 \times 4 \times 10^{-3} = 5 \text{ V}$$



Since $V_{CE} \geq 0.7 \text{ V}$ and $I_C > 0$, assumption of BJT in active is justified.

Bias Summary: $V_{CE} = 5 \text{ V}$, $I_C = 4 \text{ mA}$, and $I_B = 20 \mu\text{A}$.

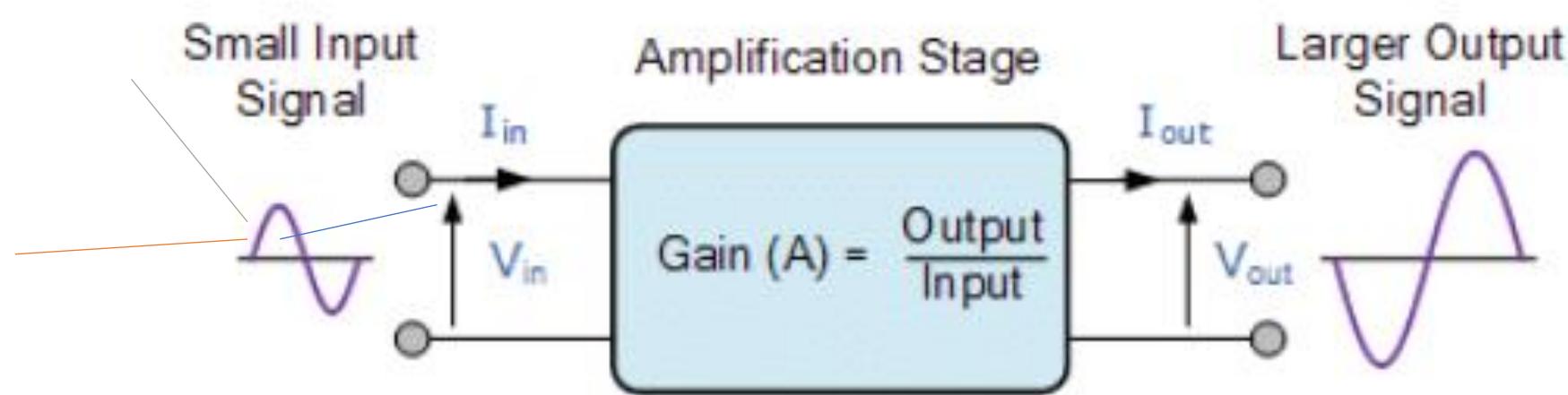
BJT Amplifiers:

Transistor as an amplifier, BJT
Low frequency small signal
hybrid- π model, AC analysis of
CB, CE, CC configurations.



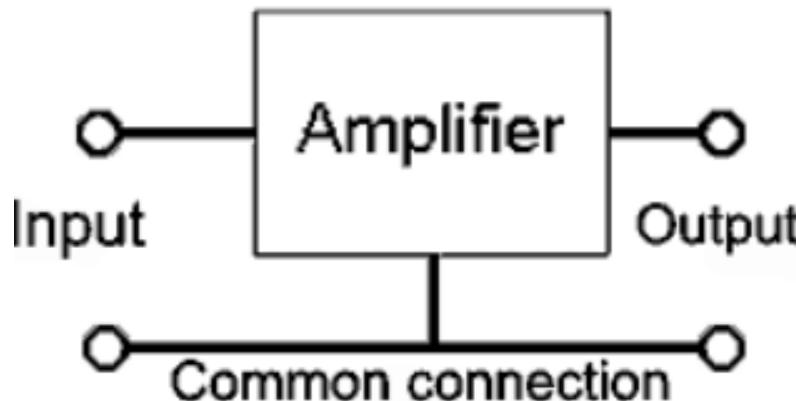
Introduction to the Amplifier

An amplifier is an electronic device or circuit which is used to increase the magnitude of the **weak signal** applied to its input



How a transistor is connected to make an amplifier

- Because an amplifier must have two input and two output terminals, a transistor used as an amplifier must have one of its three terminals common to both input and output as shown in Fig .
- The choice of which terminal is used as the common connection has a marked effect on the performance of the amplifier.



Recognise basic transistor amplifier connection modes.

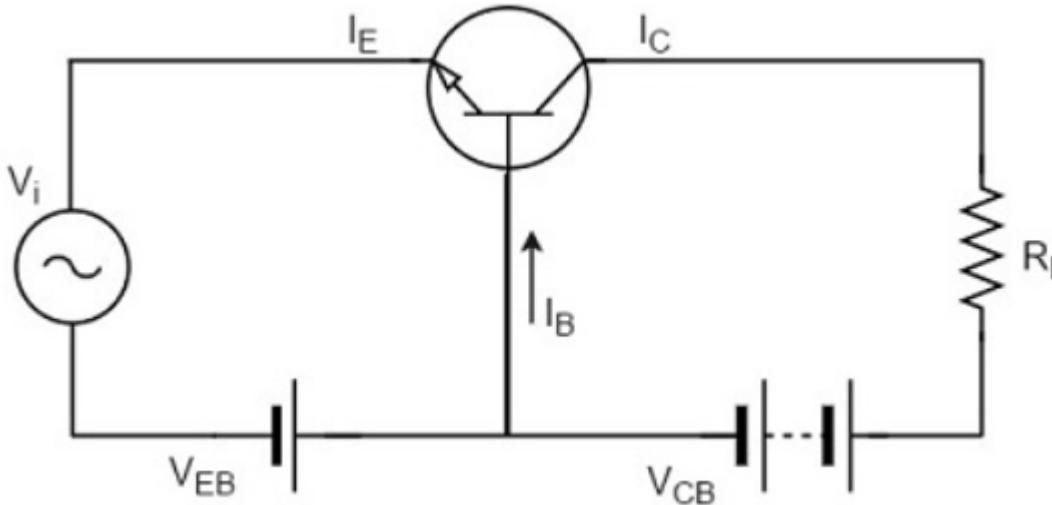
- Common emitter.
- Common collector.
- Common base.

Describe the basic parameters of each amplifier mode.

- Voltage gain.
- Current gain.
- Input & output impedances.

Example

Example



Let there be a change of 0.1v in the input voltage being applied, which further produces a change of 1mA in the emitter current. This emitter current will obviously produce a change in collector current, which would also be 1mA.

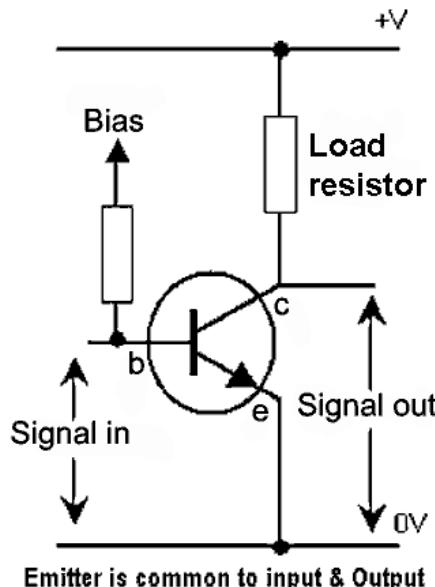
A load resistance of $5\text{k}\Omega$ placed in the collector would produce a voltage of

$$5 \text{ k}\Omega \times 1 \text{ mA} = 5\text{V}$$

Hence it is observed that a change of 0.1v in the input gives a change of 5v in the output, which means the voltage level of the signal is amplified.

Performance of Amplifier

As the common emitter mode of connection is mostly adopted, let us first understand a few important terms with reference to this mode of connection



Input Resistance

As the input circuit is forward biased, the input resistance will be low. The input resistance is the opposition offered by the base-emitter junction to the signal flow.

By definition, it is the ratio of small change in base-emitter voltage (ΔV_{BE}) to the resulting change in base current (ΔI_B) at constant collector-emitter voltage.

$$\text{Input resistance, } R_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

Where R_i = input resistance, V_{BE} = base-emitter voltage, and I_B = base current.

Output Resistance

The output resistance of a transistor amplifier is very high. The collector current changes very slightly with the change in collector-emitter voltage.

By definition, it is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the resulting change in collector current (ΔI_C) at constant base current.

$$\text{Output resistance} = R_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

Where R_o = Output resistance, V_{CE} = Collector-emitter voltage, and I_C = Collector-emitter current.

Cont.

Effective Collector Load

The load is connected at the collector of a transistor and for a single-stage amplifier, the output voltage is taken from the collector of the transistor and for a multi-stage amplifier, the same is collected from a cascaded stages of transistor circuit.

By definition, it is the total load as seen by the a.c. collector current. In case of single stage amplifiers, the effective collector load is a parallel combination of R_C and R_o .

$$\begin{aligned}\text{Effective Collector Load, } R_{AC} &= R_C // R_o \\ &= \frac{R_C \times R_o}{R_C + R_o} = R_{AC}\end{aligned}$$

Current Gain

The gain in terms of current when the changes in input and output currents are observed, is called as **Current gain**. By definition, it is the ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B).

$$\text{Current gain, } \beta = \frac{\Delta I_C}{\Delta I_B}$$

The value of β ranges from 20 to 500. The current gain indicates that input current becomes β times in the collector current.

Cont.

Voltage Gain

The gain in terms of voltage when the changes in input and output currents are observed, is called as **Voltage gain**. By definition, it is the ratio of change in output voltage (ΔV_{CE}) to the change in input voltage (ΔV_{BE}).

$$\text{Voltage gain, } A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

$$= \frac{\text{Change in output current} \times \text{effective load}}{\text{Change in input current} \times \text{input resistance}}$$

$$= \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i} = \frac{\Delta I_C}{\Delta I_B} \times \frac{R_{AC}}{R_i} = \beta \times \frac{R_{AC}}{R_i}$$

Cont.

Power Gain

The gain in terms of power when the changes in input and output currents are observed, is called as **Power gain**.

By definition, it is the ratio of output signal power to the input signal power.

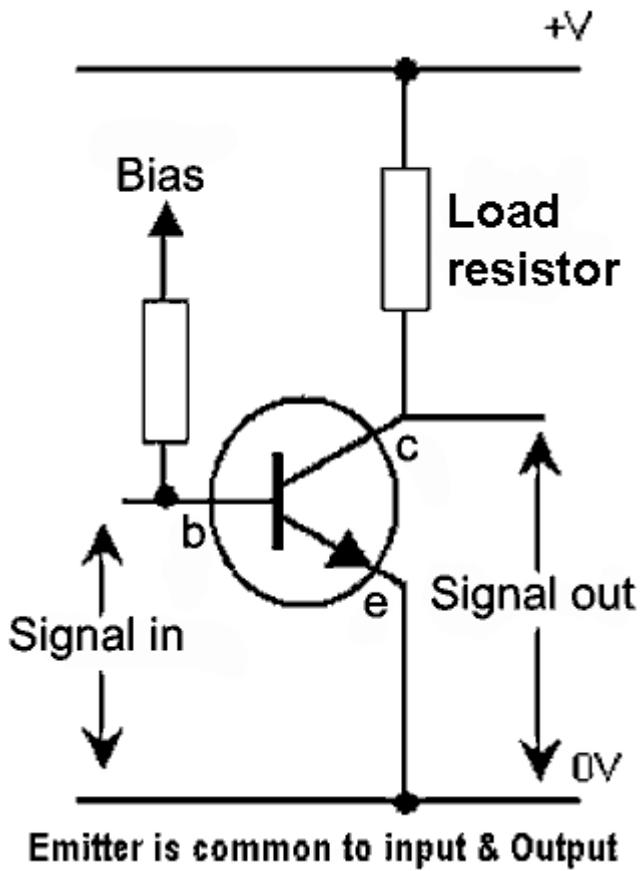
$$\text{Power gain, } A_P = \frac{(\Delta I_C)^2 \times R_{AC}}{(\Delta I_B)^2 \times R_i}$$

$$= \left(\frac{\Delta I_C}{\Delta I_B} \right) \times \frac{\Delta I_C \times R_{AC}}{\Delta I_B \times R_i}$$

$$= \text{Current gain} \times \text{Voltage gain}$$

Hence these are all the important terms which refer the performance of amplifiers.

Common Emitter Mode



Common Emitter Parameters

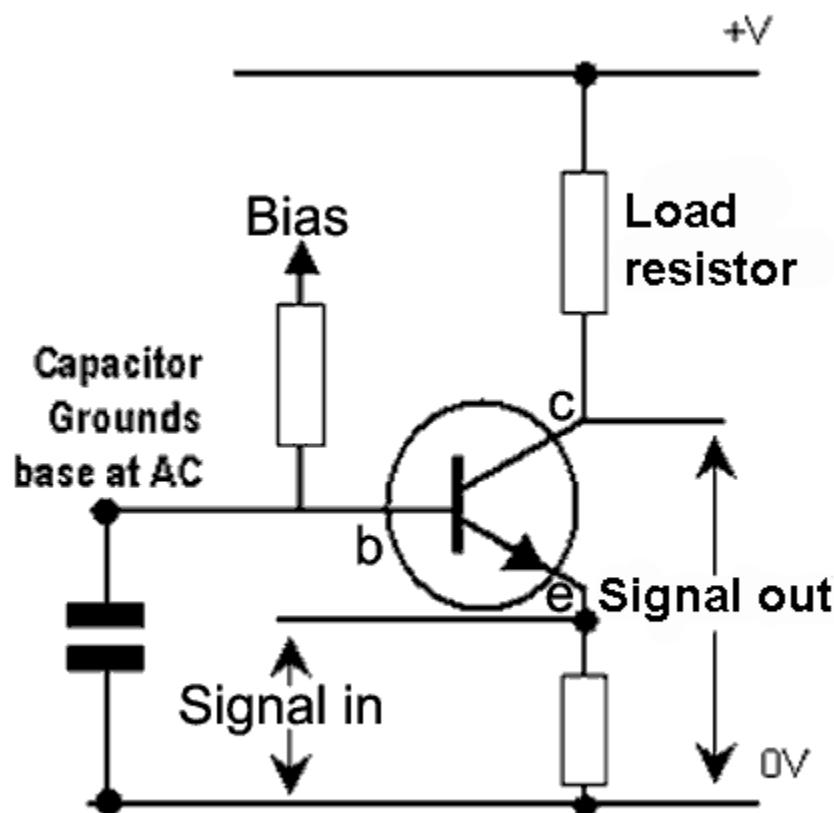
Voltage Gain: High (about 100).

Current Gain: High (about 50 to 800).

Input Impedance: Medium (about $3k\Omega$ to $5k\Omega$).

Output Impedance: Medium (Approximately the load resistor value).

Common Base Mode



Ground (& Base) is Common to Input & Output

Common Base Parameters

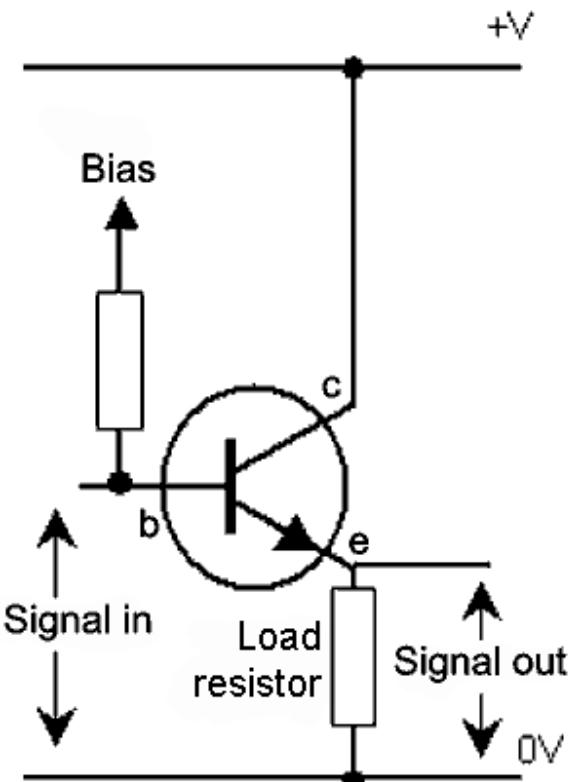
Voltage Gain: Medium (about 10 to 50).

Current Gain: Less than unity (<1)

Input Impedance: Low (about 50Ω)

Output Impedance: High (about $1M\Omega$)

Common Collector Mode or Emitter Follower



**Ground (& therefore Collector)
is Common to Input & Output**

Common Collector Parameters

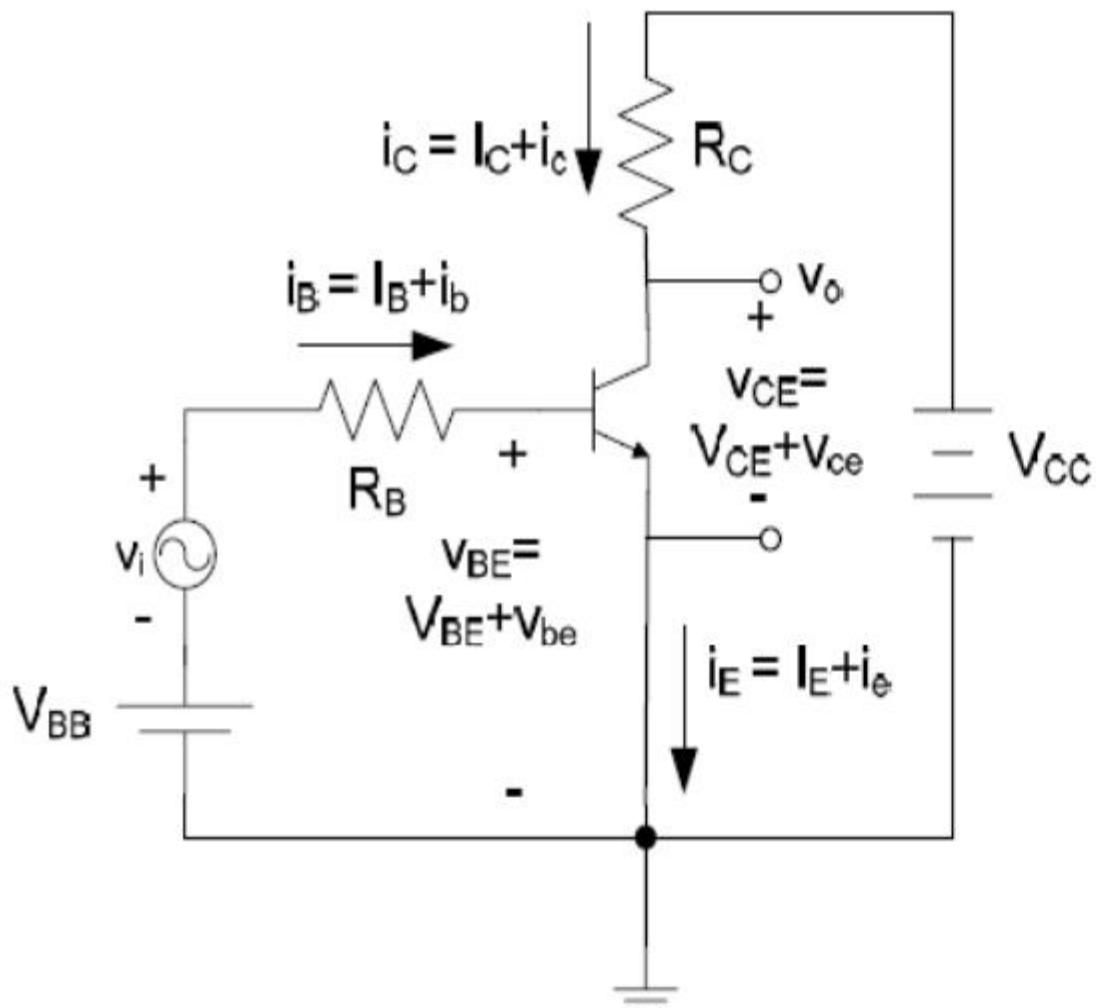
Voltage Gain: Slightly less than unity (1).

Current Gain: High (about 50 to 800)

Input Impedance: High (Several kΩ)

Output Impedance: Low (A few ohms)

BJT with input ac signal



$$i_B = I_B + i_b$$

$$i_E = I_E + i_e$$

$$i_C = I_C + i_c$$

I_B, I_C, I_E - D.C. currents

i_b, i_c, i_e - A.C. currents

i_B, i_C, i_E - D.C + A.C. currents

Similarly,

V_{BE}, V_{CE} - D.C. Voltages

v_{be}, v_{ce} - A.C. Voltages

V_{BE}, V_{CE} - D.C+ A.C Voltages

Cont.

BJT with small ac input signal

Small ac signal refers to the input signal (v_{be}) whose magnitude is much smaller than thermal voltage (V_T) i.e. $v_{be} \ll V_T$

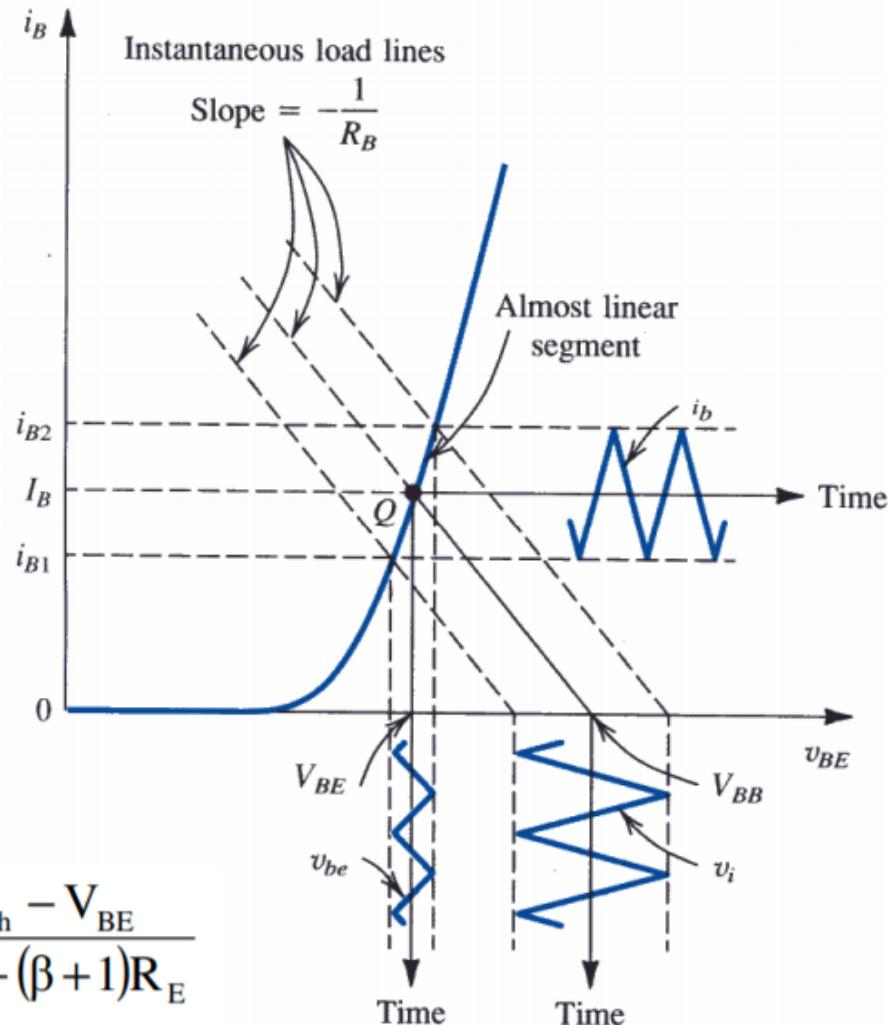
Magnitude of the ac signal applied for amplification must be small so that

- the transistor operates in the linear region for the whole cycle of input (called as a linear amplifier)
- the transistor is never driven into saturation or cut-off region

- On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off. This clips the peaks of the input and the amplifier is no longer linear.

Cont.

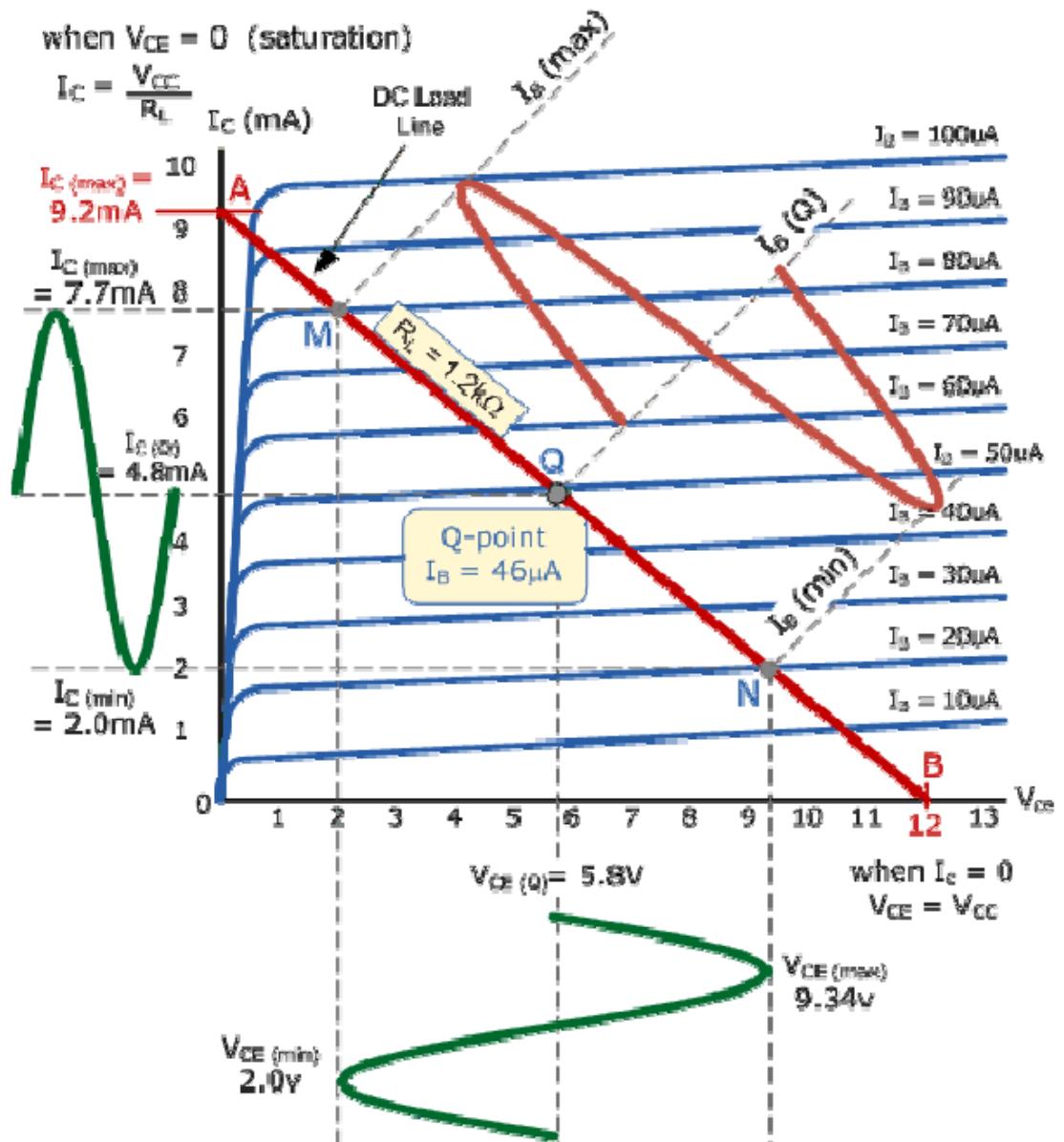
Graphical Analysis: Load Line



$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$I_C = \beta I_B = \frac{\beta(V_{Th} - V_{BE})}{R_{Th} + (\beta + 1)R_E}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$



Cont.

Small Signal Analysis

If an ac+dc input signal the total v_{BE} becomes

$$V_{BE} = v_{be} + V_{BE}$$

The collector current becomes

$$i_C = I_S \exp(v_{be} + V_{BE}) / V_T$$

$$\underline{i_C = I_S \exp(V_{BE} / V_T) \exp(v_{be} / V_T)}$$

$$\underline{i_C = I_C \exp(v_{be} / V_T)}$$

For small signal $v_{be} \ll V_T$ (10mV) hence

$$i_C = I_C (1 + v_{be} / V_T)$$

$$i_C = I_C + I_C v_{be} / V_T$$

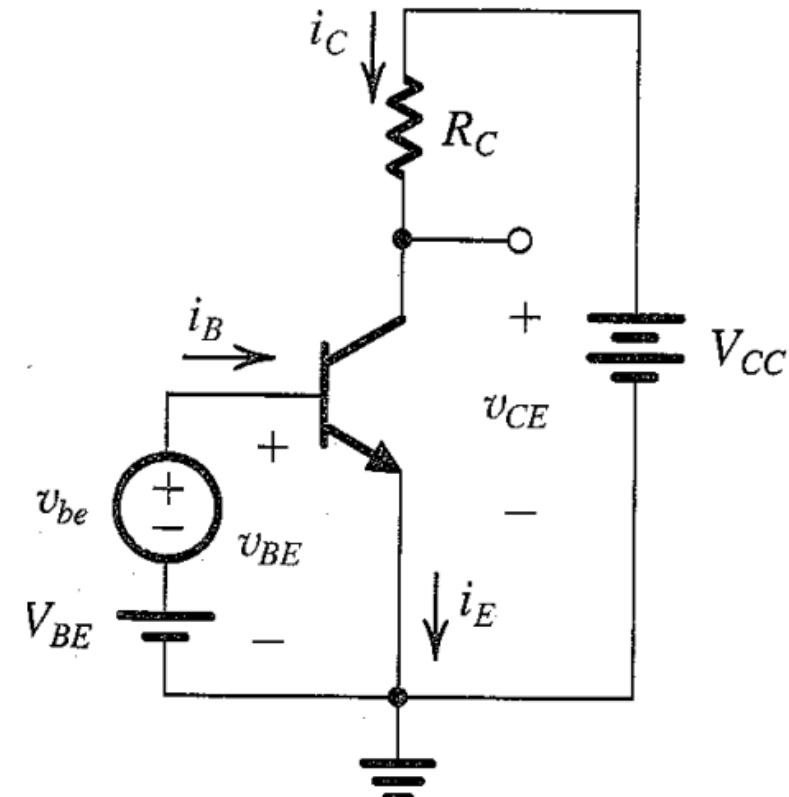
The ac component of the collector current is: $i_c = I_C v_{be} / V_T$

$$g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$$

g_m is called the small signal **transconductance**

It represents the slope of i_C-v_{BE} curve at the Q point.

$$I = I_0 \left(e^{\frac{qV}{kT}} - 1 \right) \dots\dots (1)$$



$$i_c = g_m v_{be}$$

Cont.

Small-signal Analysis: Current and input resistance

The total base current: $i_B = I_B + i_b$

$$i_B = \frac{i_c}{\beta} = \frac{I_c}{\beta} + \frac{1}{\beta} \frac{I_c}{V_T} v_{be}$$

$$g_m = \frac{i_c}{v_{be}} = \frac{I_c}{V_T}$$

Signal component of base current: $i_b = \frac{1}{\beta} \frac{I_c}{V_T} v_{be} = \frac{g_m}{\beta} v_{be}$

$$r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

r_π is the small-signal input resistance between base and emitter,
looking into the base.

The total emitter current: $i_E = I_E + i_e$ $i_E = \frac{i_c}{\alpha} = \frac{I_c}{\alpha} + \frac{i_c}{\alpha}$

$$i_e = \frac{i_c}{\alpha} = \frac{I_c}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be}$$

$$r_e = \frac{v_{be}}{i_e} = \frac{\alpha}{g_m} = \frac{V_T}{I_E}$$

$$i_e = i_b + i_c$$

r_e is the small-signal input resistance between base and emitter,
looking into the emitter.

$$v_{be} = i_b r_\pi = i_e r_e$$

$$r_\pi = (\beta + 1) r_e$$

Cont.

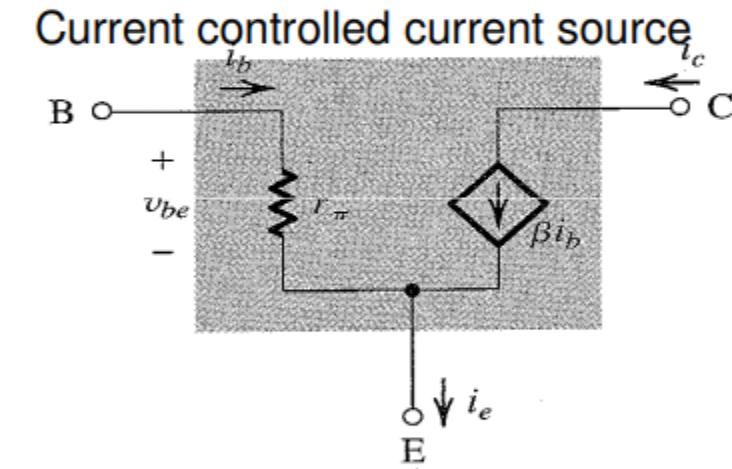
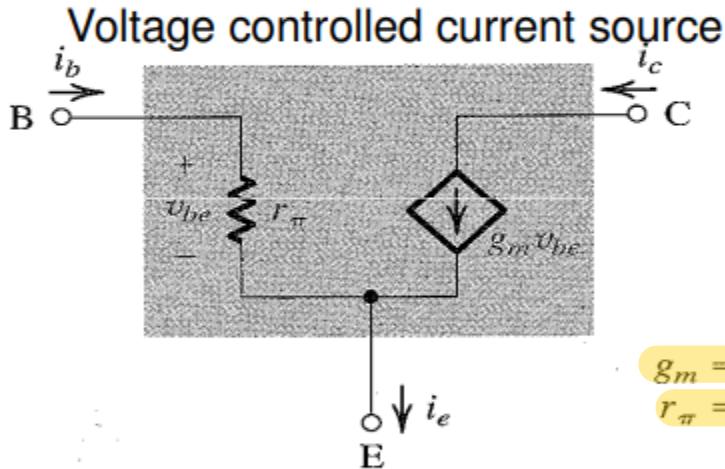
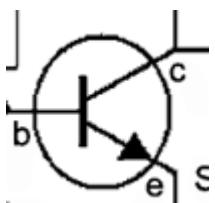
Hybrid- π small signal model of BJT

This model represents that transistor as a voltage controlled current source with control voltage v_{be} and include the input resistance looking into the base.

$$r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

$$r_e = \frac{v_{be}}{i_e} = \frac{\alpha}{g_m} = \frac{V_T}{I_E}$$

$$g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$$



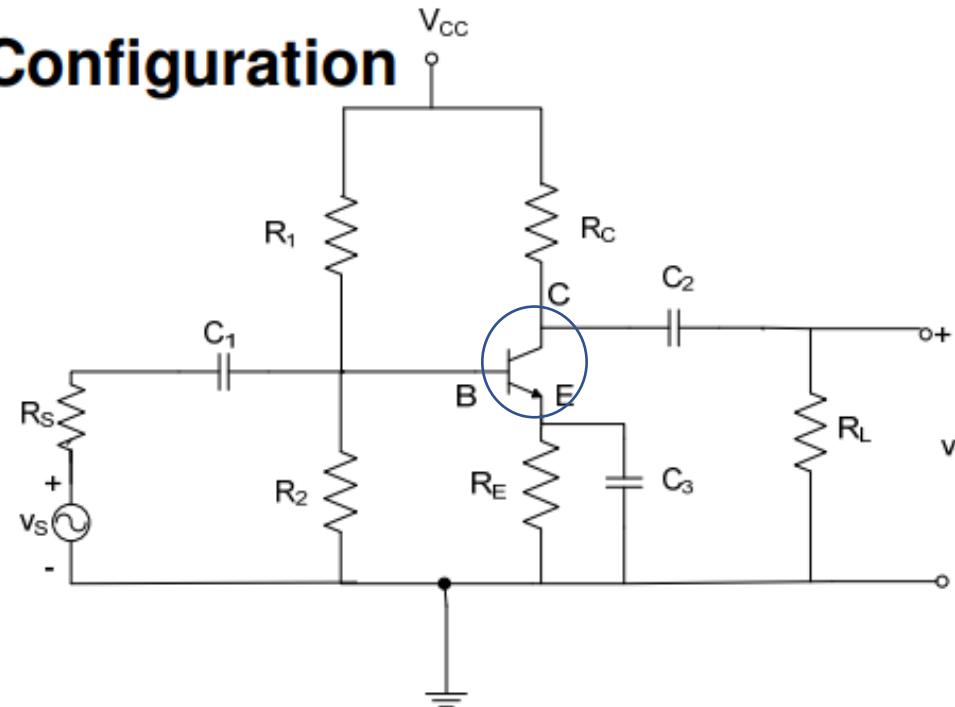
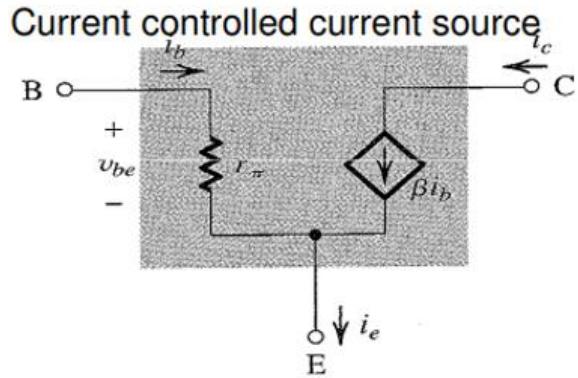
$$\begin{aligned} i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi} (1 + g_m r_\pi) \\ &= \frac{v_{be}}{r_\pi} (1 + \beta) = v_{be} \left(\frac{r_\pi}{1 + \beta} \right) \\ &= v_{be} / r_e \end{aligned}$$

$$\begin{aligned} g_m v_{be} &= g_m (i_b r_\pi) \\ &= (g_m r_\pi) i_b = \beta i_b \end{aligned}$$

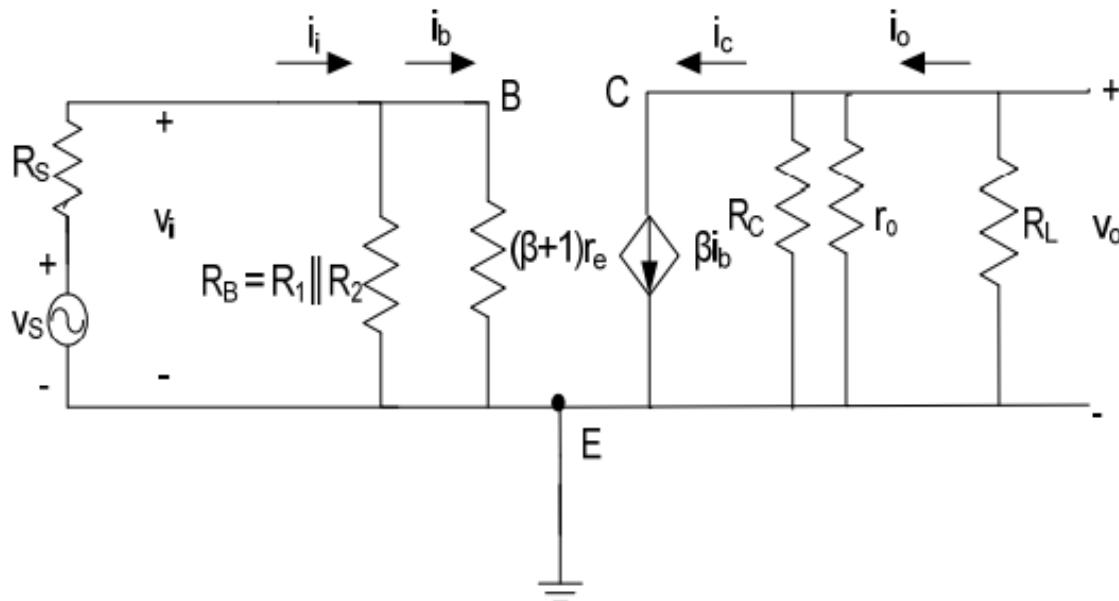
BJT Circuit Analysis using Small Signal Model:

1. Determine the DC operating point of the BJT and in particular, the collector current I_C
2. Calculate small-signal model parameters g_m , r_{π} , & r_e for this DC operating point
3. Eliminate DC sources
 - ❖ Replace DC voltage sources with short circuits
 - ❖ Replace DC current sources with open circuits
4. Replacing all capacitors by a short circuit equivalent and remove all elements bypassed by the short circuit equivalents.
5. Replace BJT with an equivalent small-signal model
6. Analyze the resulting circuit to determine the required quantities e.g. voltage gain, input resistance...etc.

CE Voltage-Divider Bias Configuration



A.C. Equivalent Circuit



Cont.

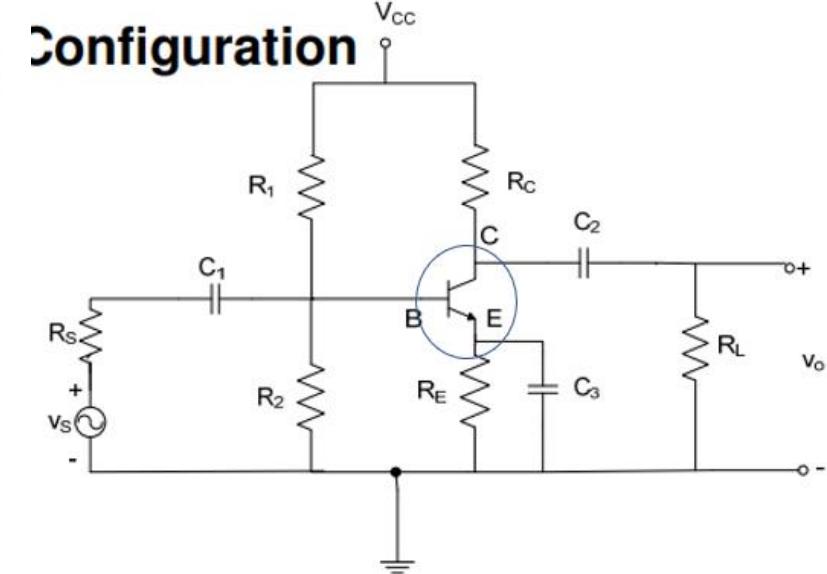
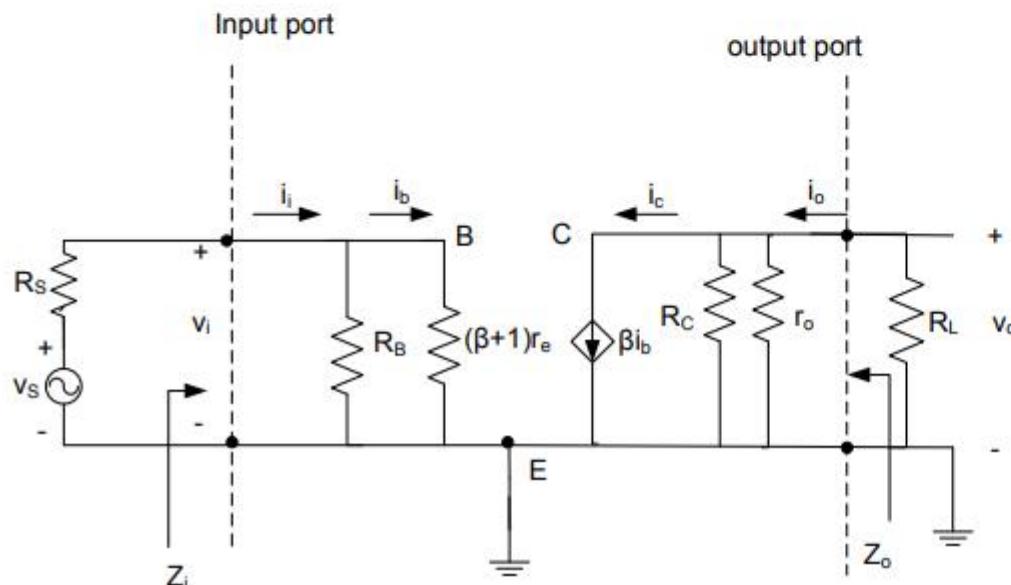
Small Signal Performance Parameters

In AC analysis, we are interested to find

- ❖ Input resistance or impedance
- ❖ Output resistance or impedance
- ❖ Voltage gain

Input resistance

The total resistance looking into the amplifier at coupling capacitor C_1 , represents total resistance of the amplifier presented to signal source



$$Z_i = \frac{V_i}{I}; I = i_1 + i_b$$

$$V_i = I [R_B \parallel (\beta + 1)r_e]$$

$$Z_i = [R_B \parallel (\beta + 1)r_e]$$

$$Z_i = [R_1 \parallel R_2 \parallel (\beta + 1)r_e]$$

Cont.

Output resistance

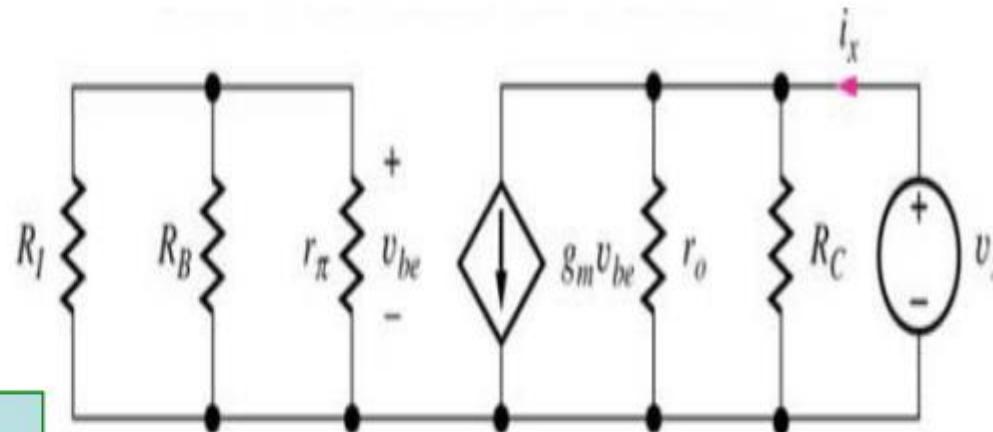
The total resistance looking into the output of the amplifier at coupling capacitor C_2 represents output resistance of the amplifier.

To find Z_{out} , input source is set to 0 and test source is applied at output

$$i_x = \frac{v_x}{R_c} + \frac{v_x}{r_o} + g_m v_{be}$$

But v_{be} is zero . Therefore

$$Z_{out} = \frac{v_x}{i_x} = (R_C // r_o)$$



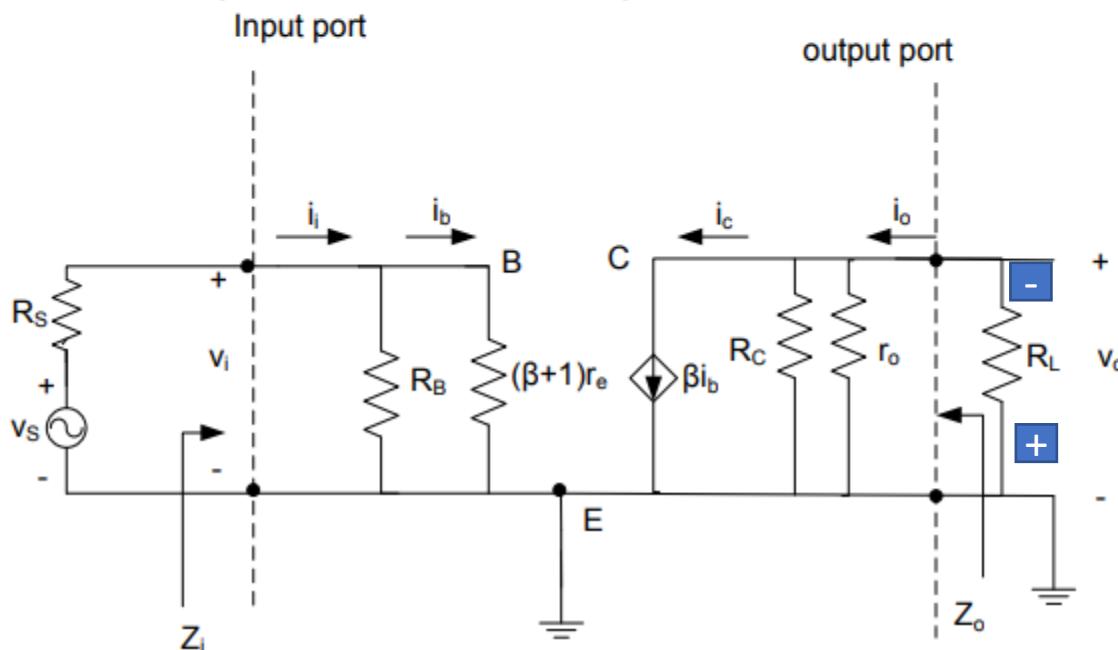
$$Z_{out} = R_C \quad \text{Because } r_o \gg R_C$$

Cont.

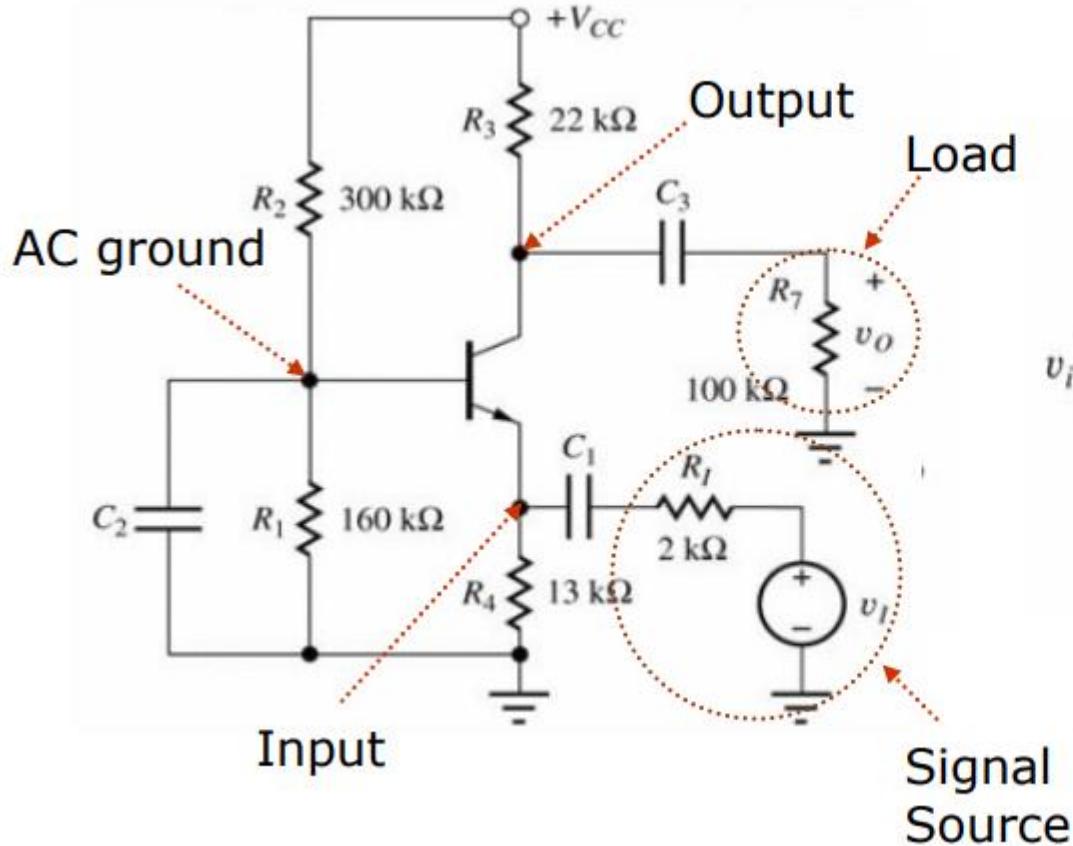
Voltage Gain

$$A_v = \frac{v_o}{v_i} = \frac{-i_o R_L}{i_b (\beta + 1) r_e} = \frac{-\beta i_b \left(\frac{R_C \| r_o}{R_C \| r_o + R_L} \right) R_L}{i_b (\beta + 1) r_e}$$

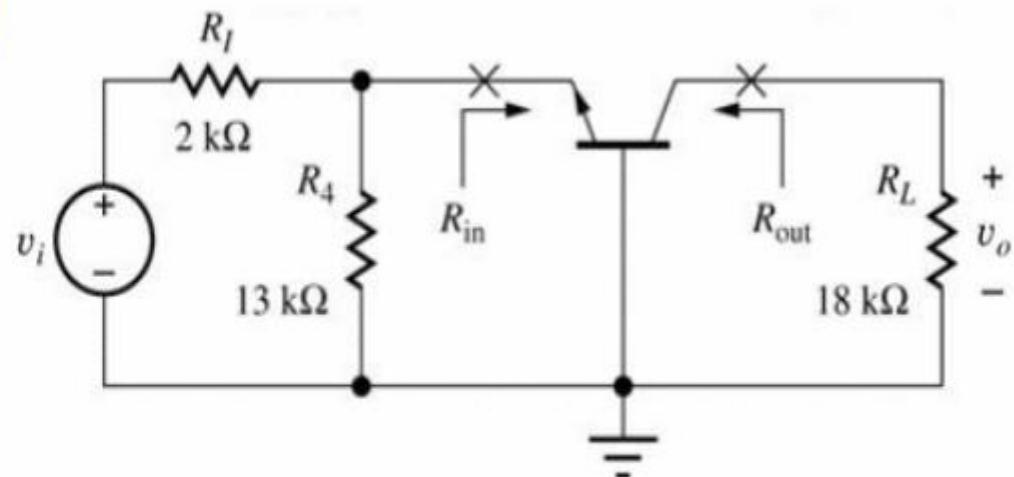
$$\text{or, } A_v = \frac{-\beta R_C \| r_o \| R_L}{(\beta + 1) r_e} \approx \frac{-R_C \| r_o \| R_L}{r_e}$$



AC analysis of CB configuration



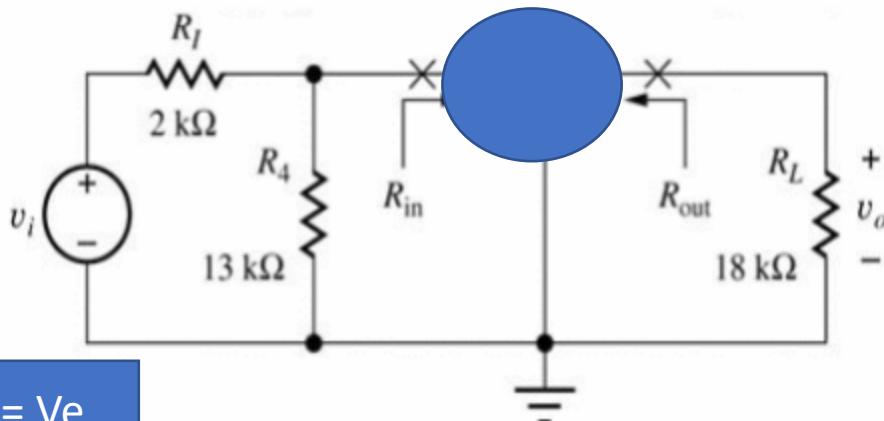
AC/Small-signal equivalent:



$$R_L = R_3 \parallel R_7$$

Cont.

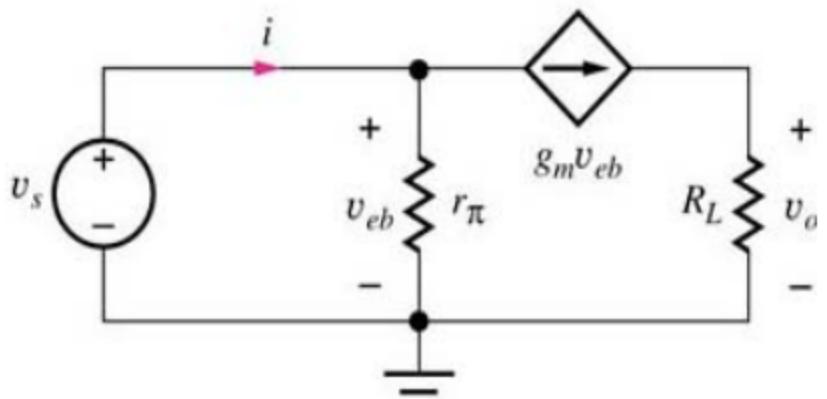
Terminal Voltage Gain



$$V_{eb} = V_e - V_b = V_e$$

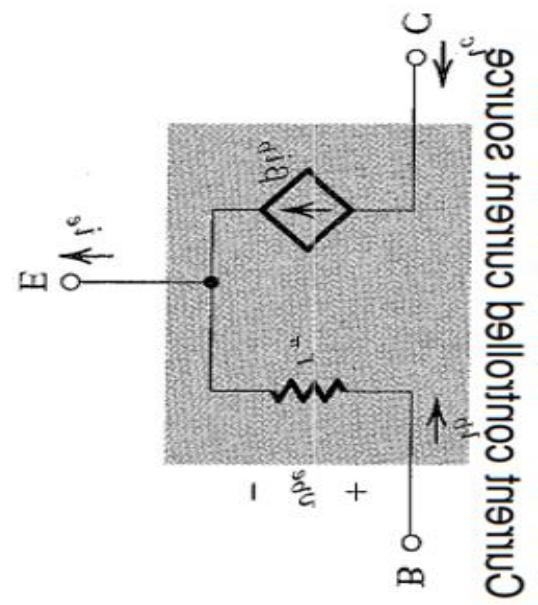
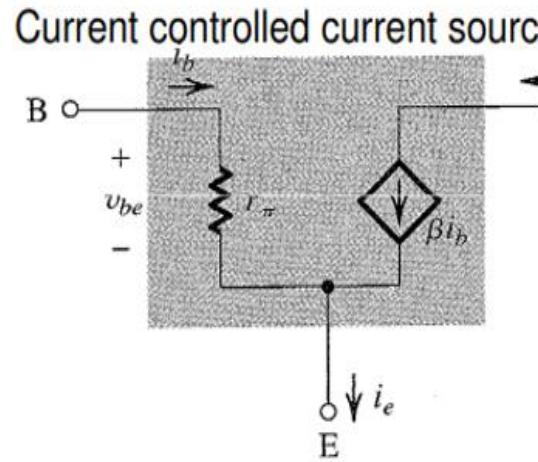
$$V_o = g_m * V_{eb} * R_L$$

Apply test source to input (E)
And use BJT small signal model:



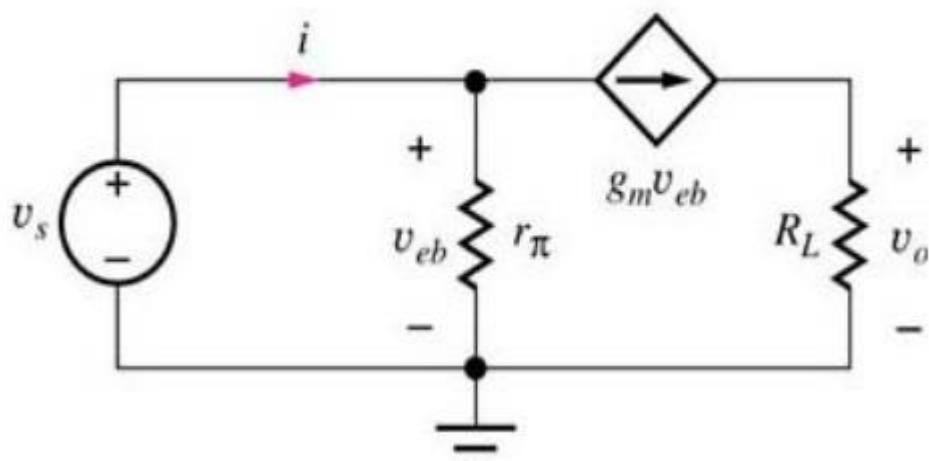
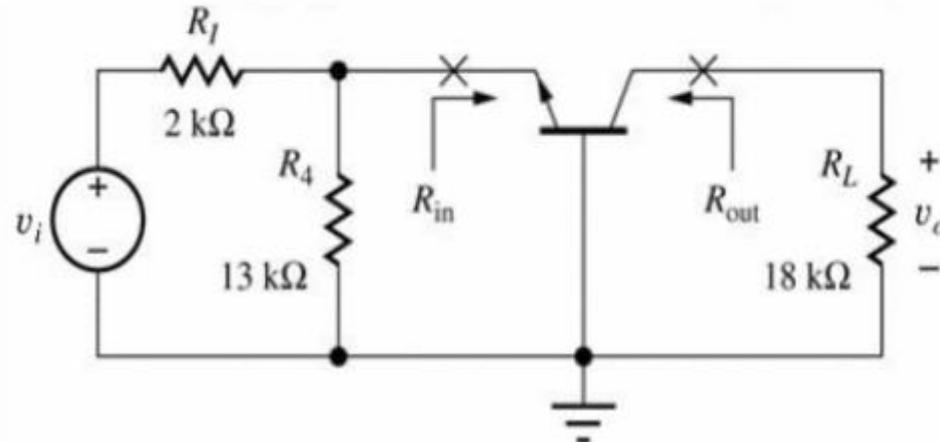
$$A_{vt}^{CB} \equiv \frac{v_o}{v_e} = +g_m R_L$$

- Non-inverting!
- Magnitude same as the CE amplifier with $R_E=0$.



Cont.

Input Resistance



KCL at emitter:

$$i = \frac{v_e}{r_\pi} + g_m v_e$$

$V_{eb} = V_e - V_b = V_e$
Because base is GND

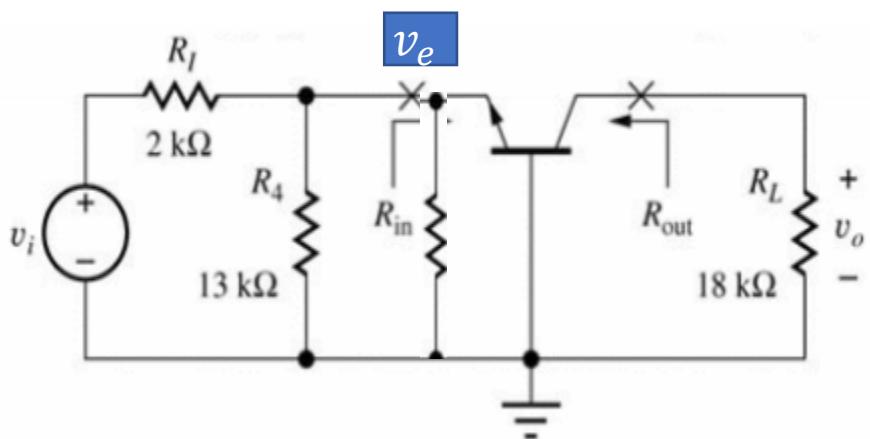
$$R_{in}^{CB} = \frac{v_e}{i} = \frac{r_\pi}{r_\pi g_m + 1} = r_\pi // \left(\frac{1}{g_m} \right) \approx \frac{1}{g_m}$$

- R_{in} is small (as g_m is usually large)!

$$(g_m = I_C / V_T)$$

Cont.

Overall Voltage Gain



Overall voltage gain is

$$\begin{aligned}A_V^{CB} &= \frac{v_o}{v_i} = \left(\frac{v_o}{v_e} \right) \left(\frac{v_e}{v_i} \right) = A_{vt} \left[\frac{R_4 // R_{in}}{R_I + (R_4 // R_{in})} \right] \\&= \frac{g_m R_L}{1 + g_m (R_4 // R_I)} \left(\frac{R_4}{R_I + R_4} \right) \\&\approx \frac{g_m R_L}{1 + g_m R_I} \quad \text{for} \quad R_4 \gg R_I\end{aligned}$$

$$v_e = \left[\frac{R_4 // R_{in}}{R_I + (R_4 // R_{in})} \right] v_i$$

For $g_m R_I \ll 1$,

$$A_V^{CB} = +g_m R_L$$

This is the upper bound.

For $g_m R_I \gg 1$,

$$A_V^{CB} = +\frac{R_L}{R_I}$$

- For large voltage gain, a very small R_I is required!
- Not a good candidate for voltage amplifier

Cont.

Example

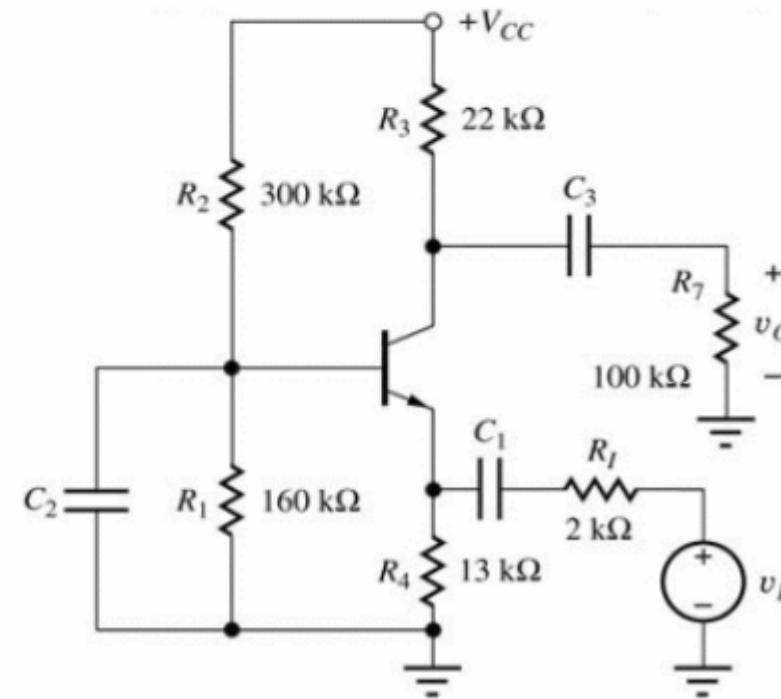
- **Problem:** Find overall voltage gain.
- **Given data:** $\beta=100$, Q-point values: $I_C=245\mu A$, $V_{CE}=3.64V$, $g_m=9.8mS$, $r_\pi=10.2k\Omega$, $r_o=219k\Omega$.
- **Assumptions:** Small-signal operating conditions.
- **Analysis:**

$$R_{in}^{CB} \approx 1/g_m = 102\Omega$$

$$R_L = R_3 \parallel R_7 = 18k\Omega$$

$$A_{vt}^{CB} = +g_m R_L = 176$$

$$A_v^{CB} = \frac{A_{vt}^{CB}}{1 + g_m (R_I \parallel R_4)} \left(\frac{R_4}{R_I + R_4} \right) = +8.59$$



Cont.

Output Resistance

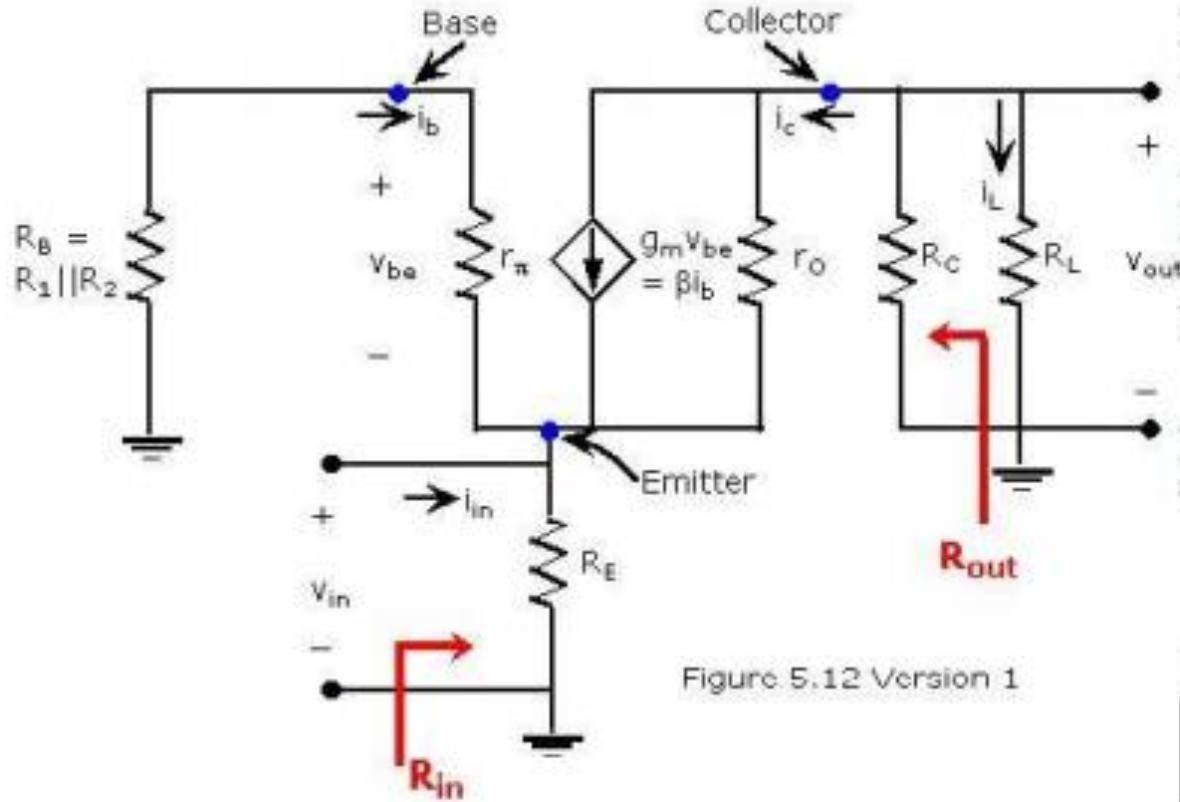


Figure 5.12 Version 1

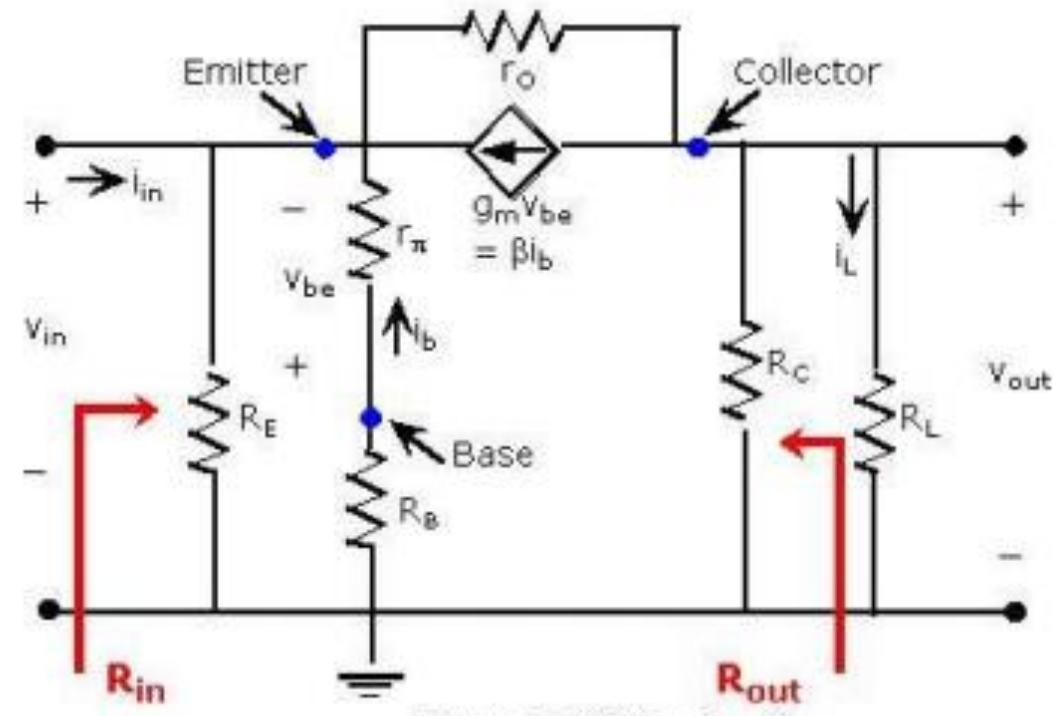


Figure 5.12 Version 2

If we assume that r_o is very large, it may be neglected in the calculation of output resistance. This simplification leaves only R_C in the output circuit so, like the common-emitter amplifier, the output resistance for the common-base configuration is

$$R_o = R_C .$$

Cont.

Output resistance

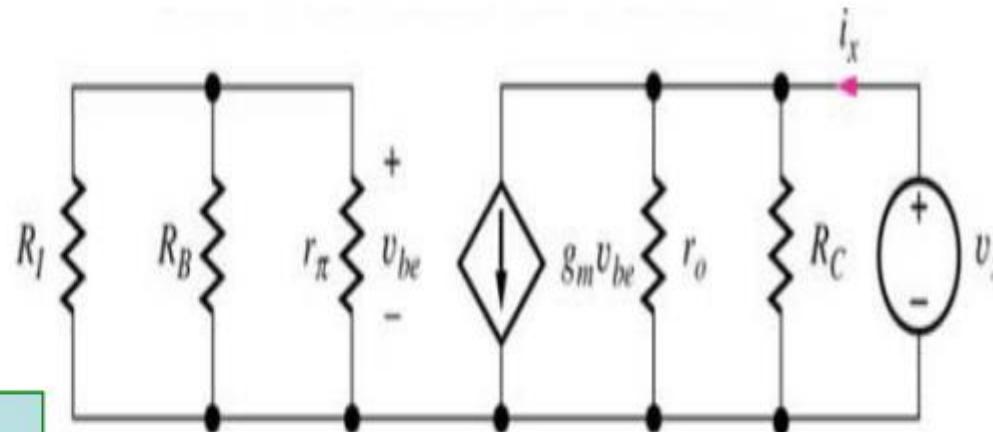
The total resistance looking into the output of the amplifier at coupling capacitor C_2 represents output resistance of the amplifier.

To find Z_{out} , input source is set to 0 and test source is applied at output

$$i_x = \frac{v_x}{R_c} + \frac{v_x}{r_o} + g_m v_{be}$$

But v_{be} is zero . Therefore

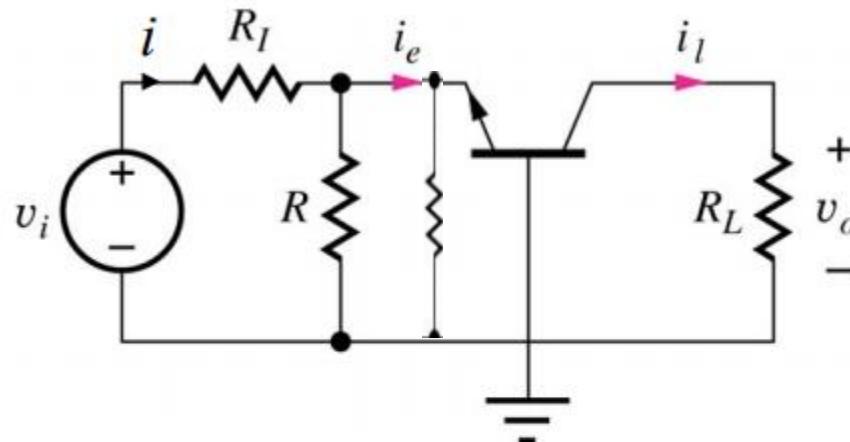
$$Z_{out} = \frac{v_x}{i_x} = (R_C // r_o)$$



$$Z_{out} = R_C \quad \text{Because } r_o \gg R_C$$

Cont.

Current Gain



- Terminal current gain: $A_{it}^{CB} = \frac{i_l}{i_e} = \alpha \approx +1$
- Current gain from source to load:

$$A_i^{CB} = \frac{i_l}{i} = \left(\frac{i_l}{i_e} \right) \left(\frac{i_e}{i} \right) = A_{it} \frac{R}{R_{in} + R} \approx A_{it} = 1 \text{ for } R \gg R_{in}$$

Cont.

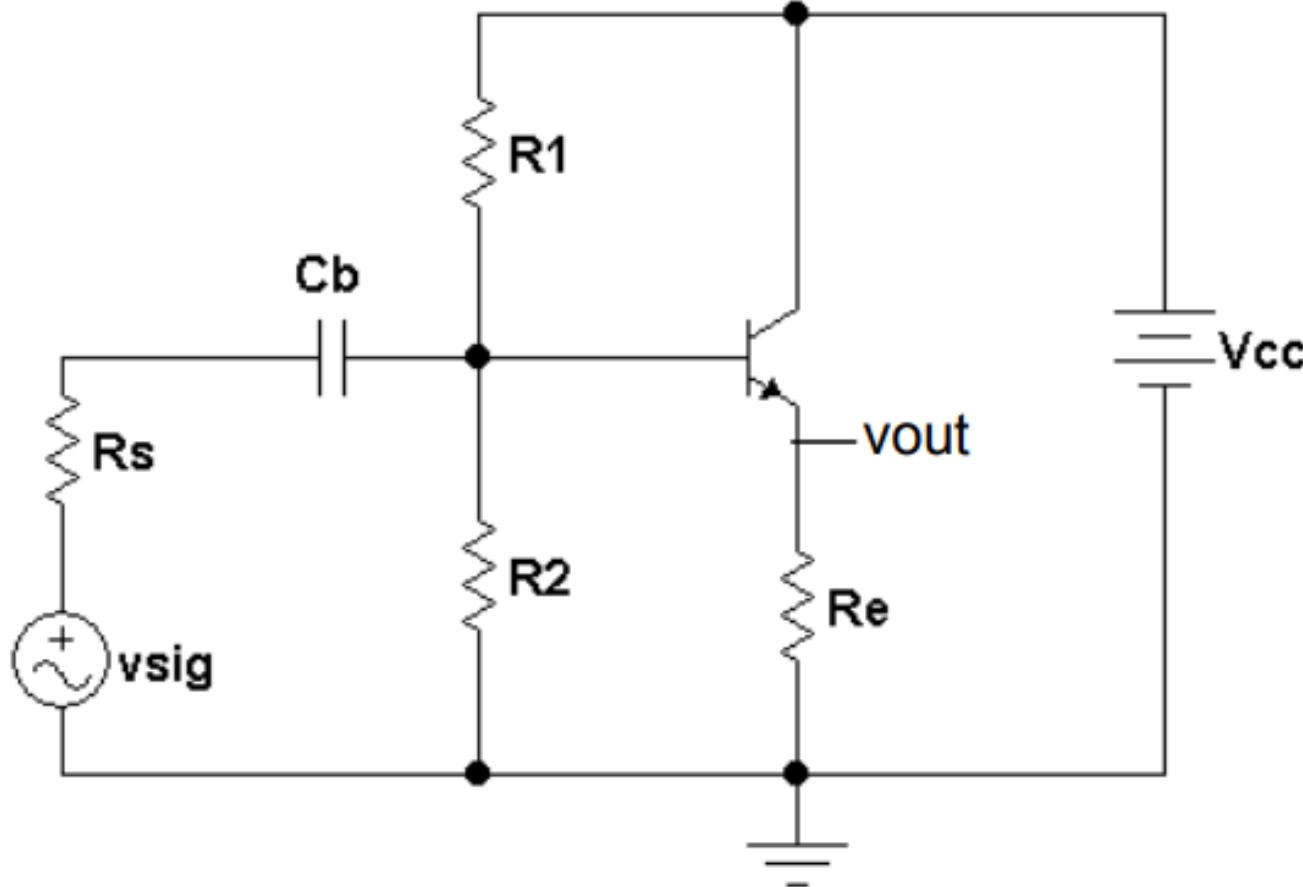
Summary of Common Base Amplifier

- *Terminal voltage gain*: Non-inverting and Large
- *Input resistance*: Low
- *Output resistance*: High
- *Current gain*: close to Unity
- *Input range*: determined by $g_m R_{th}$

- Excellent for use as a current buffer

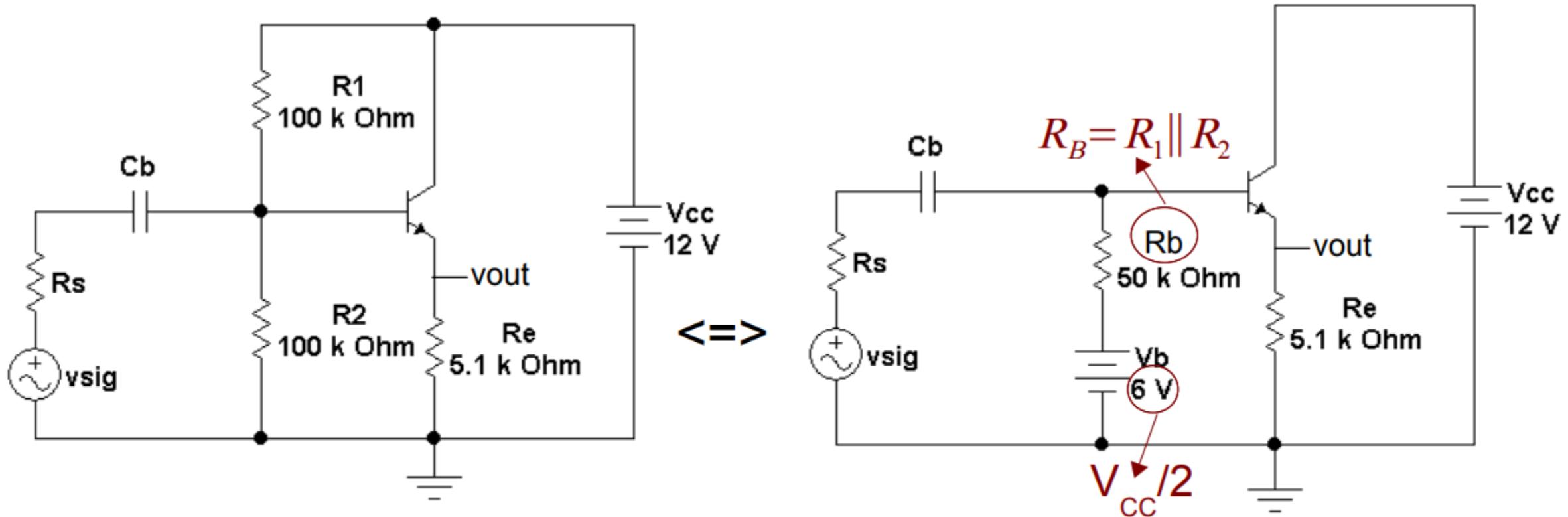
AC analysis of CC configuration

Common Collector (Emitter Follower) Amplifier



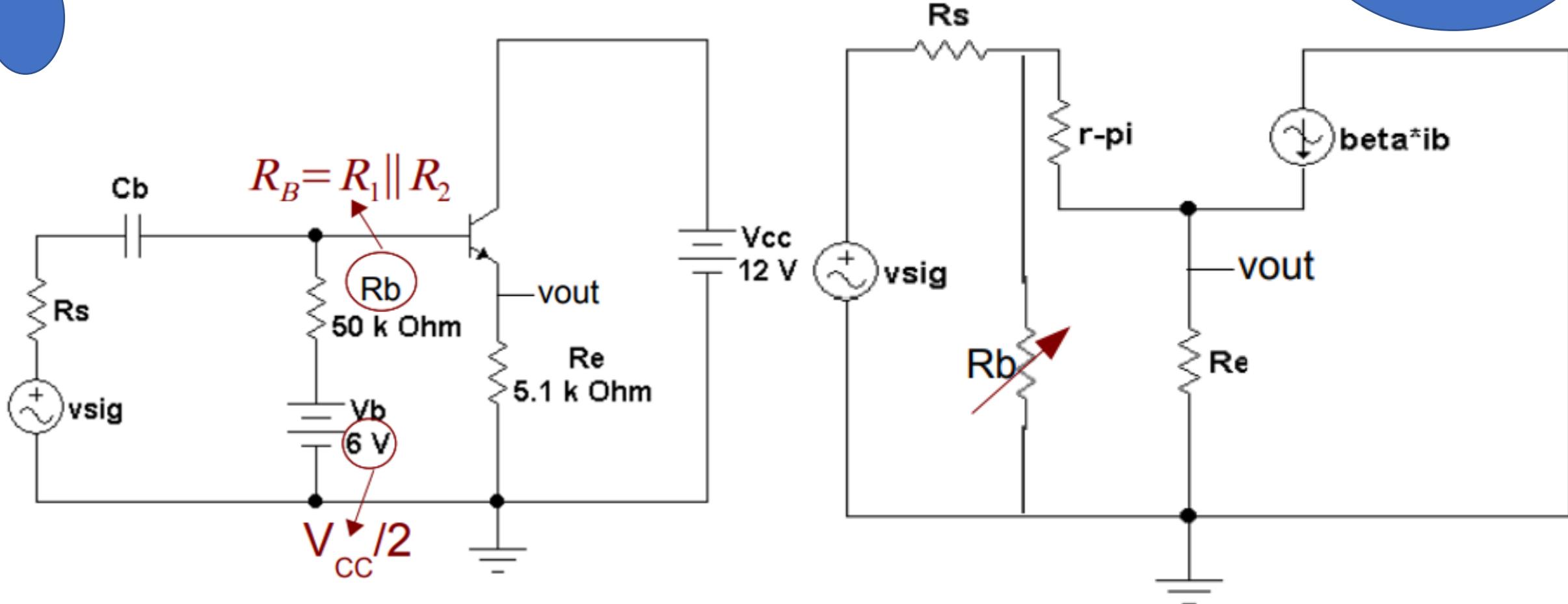
Cont.

Equivalent Circuits



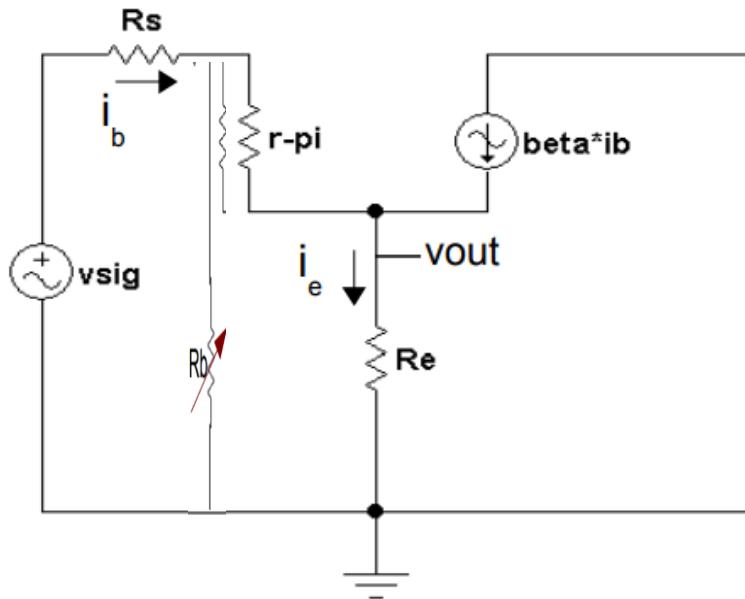
Cont.

Emitter Follower Small Signal Circuit



Cont.

Follower Small Signal Analysis - Voltage Gain



Circuit analysis:

$$v_{sig} = (R_s + r_\pi + (\beta + 1) R_E) i_b$$

Solving for i_b

$$i_b = \frac{v_{sig}}{R_s + r_\pi + (\beta + 1) R_E}$$

$$v_{out} = R_E i_e = R_E (1 + \beta) i_b$$

$$v_{out} = \frac{R_E (\beta + 1) v_{sig}}{R_s + r_\pi + (\beta + 1) R_E}$$

$$A_V = \frac{v_{out}}{v_{sig}} = \frac{R_E v_{sig}}{\frac{R_s + r_\pi}{(\beta + 1)} + R_E} \approx 1$$

$$\frac{v_{out}}{v_{sig}} = \frac{R_E}{\frac{R_s + r_\pi}{(\beta + 1)} + R_E}$$

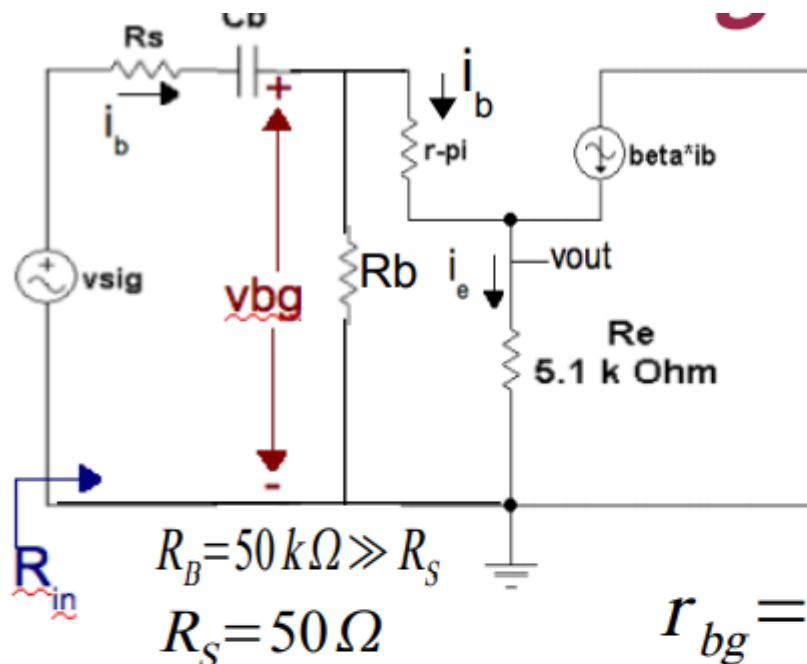
Since, typically:

$$\frac{R_s + r_\pi}{(\beta + 1)} \ll R_E$$

$$A_V = \frac{v_{out}}{v_{sig}} \approx \frac{R_E}{R_E} = 1$$

Note: A_V is non-inverting

Input Resistance



Use the base current expression:

$$v_{bg} = r_\pi i_b + R_E i_E = (r_\pi + (\beta + 1)) i_b$$

$$i_b = \frac{v_{bg}}{r_\pi + (\beta + 1) R_E}$$

$$r_{bg} = \frac{v_{bg}}{i_b} = r_\pi + (\beta + 1) R_E \approx (\beta + 1) R_E = 101 \cdot 5.1 \text{ k} = 515 \text{ k}\Omega$$

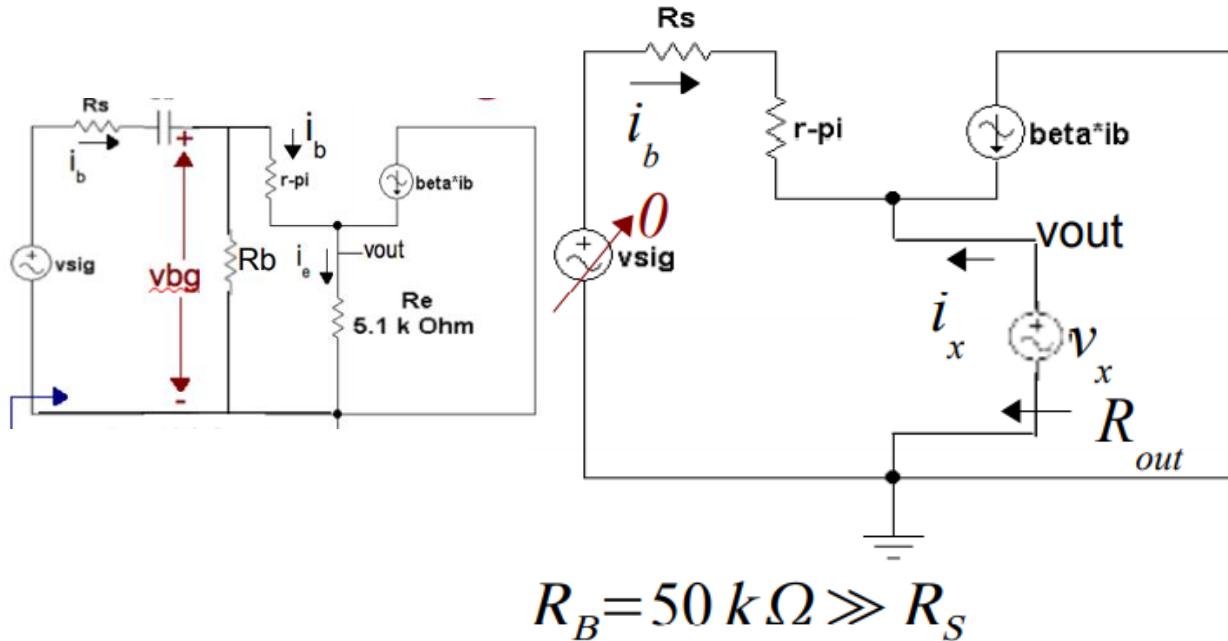
To obtain the base to ground resistance of the transistor:

This transistor input resistance is in parallel with the $50\text{k}\Omega$ R_B , forming the total amplifier input resistance:

$$R_{in} = R_s + R_B \parallel r_{bg} \approx R_B \parallel r_{bg} = \frac{515}{(515+50)} 50\text{k}\Omega = 45.6\text{k}\Omega$$

Cont.

Emitter Follower Output Resistance



$$R_B = 50 \text{ k}\Omega \gg R_s$$

Assume:

$$I_C = 1 \text{ mA} \Rightarrow r_\pi = \frac{V_T}{I_B} = \beta \frac{V_T}{I_C} = 2500 \Omega$$

$$\beta = 100 \quad R_s = 50 \Omega$$

$$i_x = -i_b - \beta i_b = -(1 + \beta) i_b \Rightarrow i_b = \frac{-i_x}{1 + \beta}$$

$$v_x = -i_b (R_s + r_\pi) = \frac{R_s + r_\pi}{1 + \beta} i_x$$

$$R_{out} = \frac{v_x}{i_x} = \frac{R_s + r_\pi}{1 + \beta} \approx \frac{r_\pi}{1 + \beta}$$

R_{out} is the Thevenin resistance looking into the open-circuit output.

$$R_{out} \approx \frac{2550}{100} = 25.5 \Omega$$

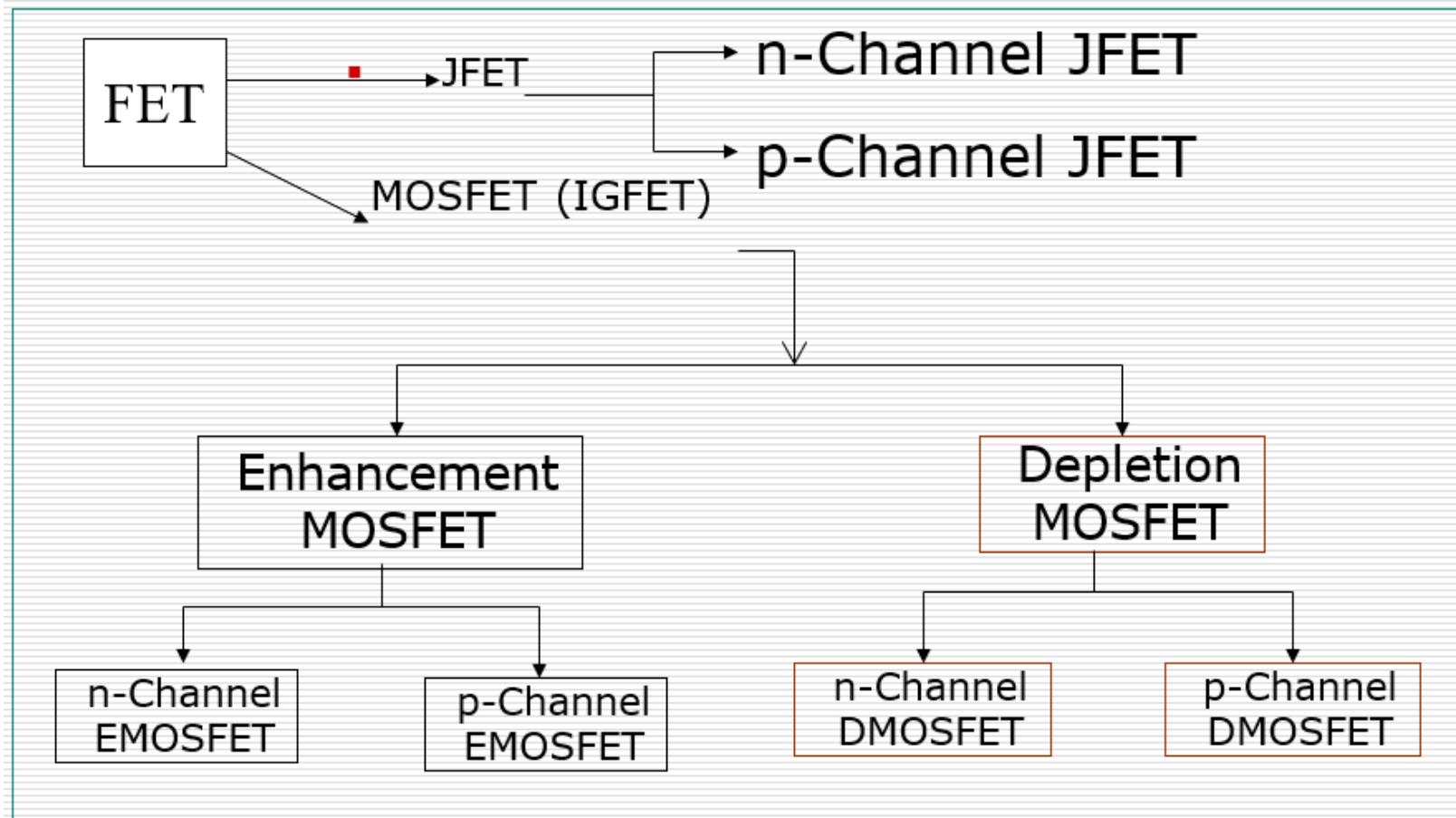
chapter 4

- **FET: Junction Field Effect Transistors (JFET): Introduction, Common source drain characteristics, operating point, biasing, MOSFETS (enhancement & depletion type). FET Amplifier: Low frequency small signal model, AC analysis of Common Source and Common Drain configurations.**

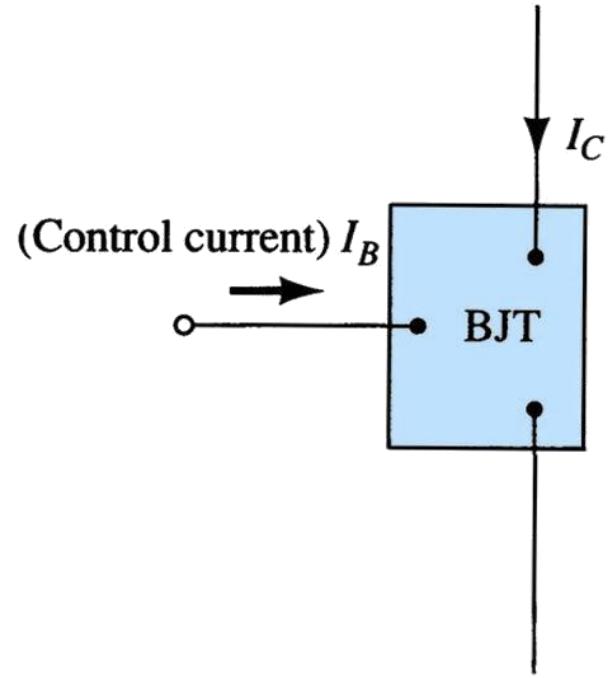
Introduction (FET)

- Field-effect transistor (FET) are important devices such as BJTs
- Also used as amplifier and logic switches
- Types of FET:
 - MOSFET (metal-oxide-semiconductor field-effect transistor)
 - Depletion-mode MOSFET
 - JFET (junction field-effect transistor)

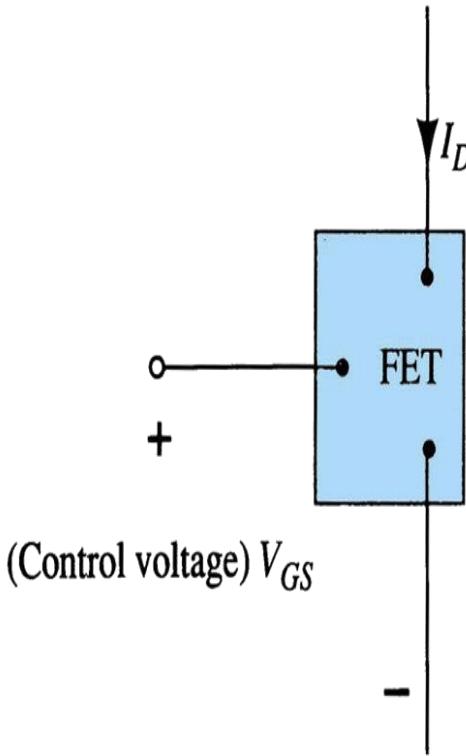
Types of Field Effect Transistors (The Classification)



BJT-Current-controlled device Vs FET –voltage-controlled device

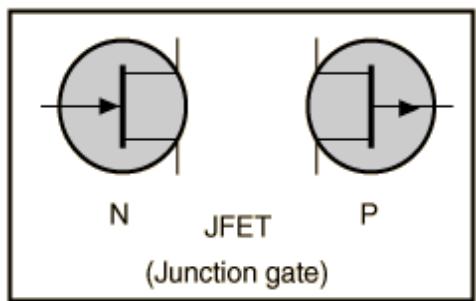


(a)

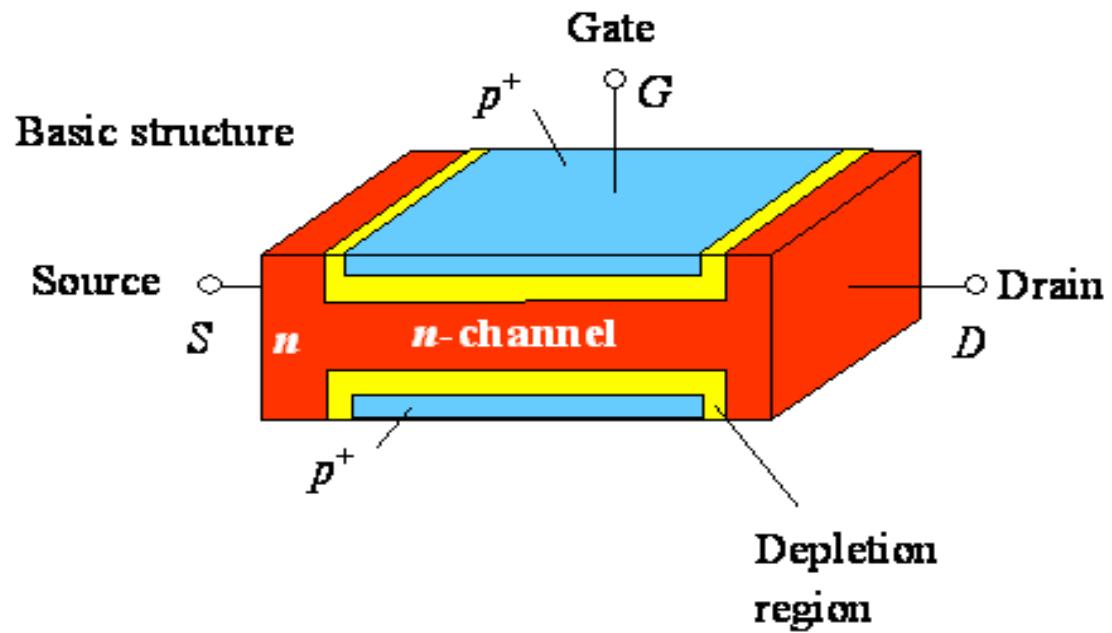
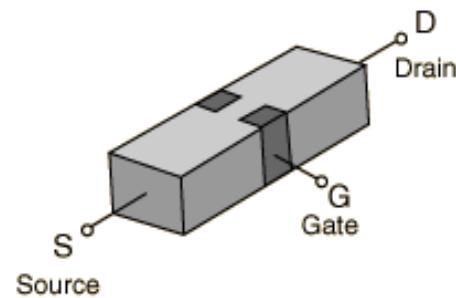


(b)

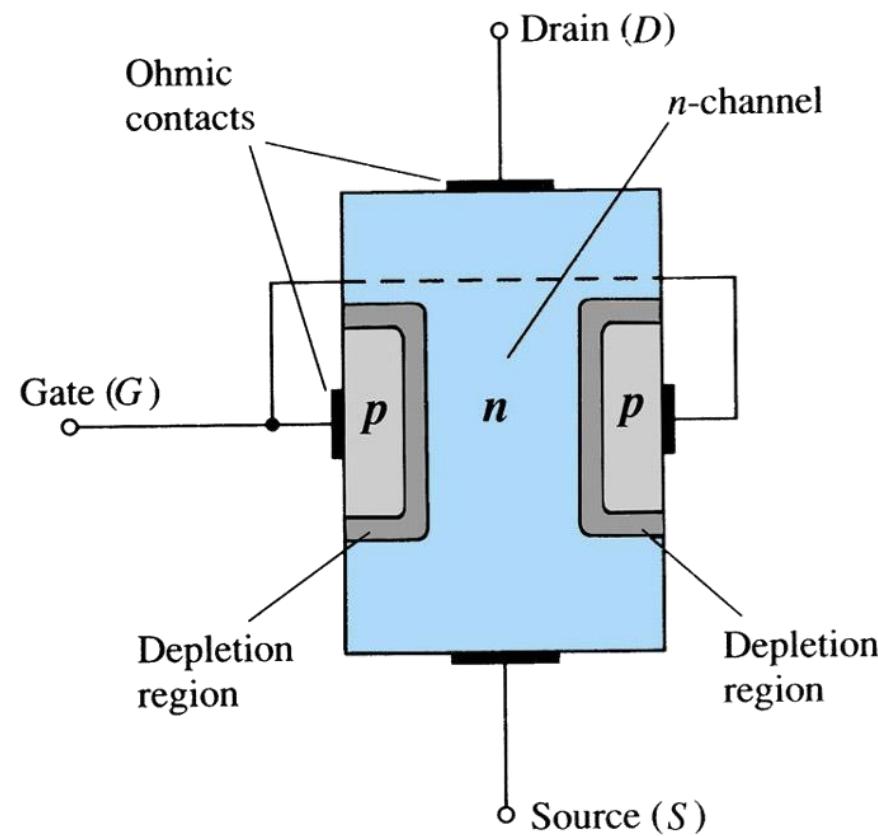
Junction FETs (JFETs)



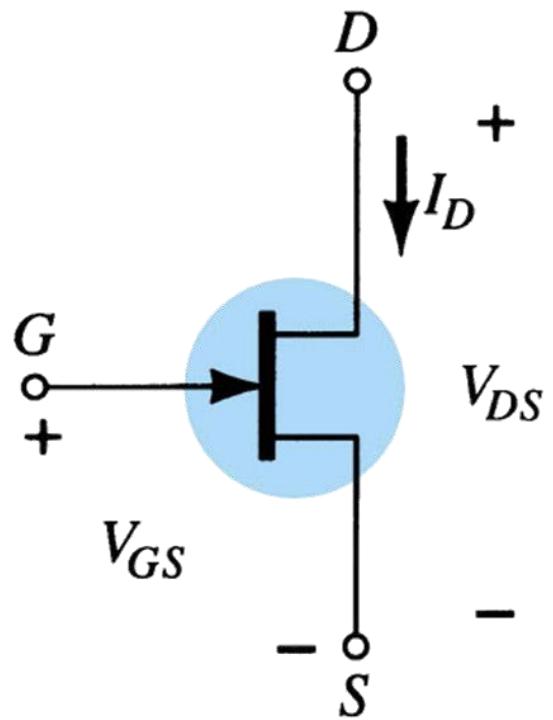
- JFETs consists of a piece of high-resistivity semiconductor material (usually Si) which constitutes a **channel** for the majority carrier flow.
- Conducting semiconductor channel between two ohmic contacts – **source & drain**



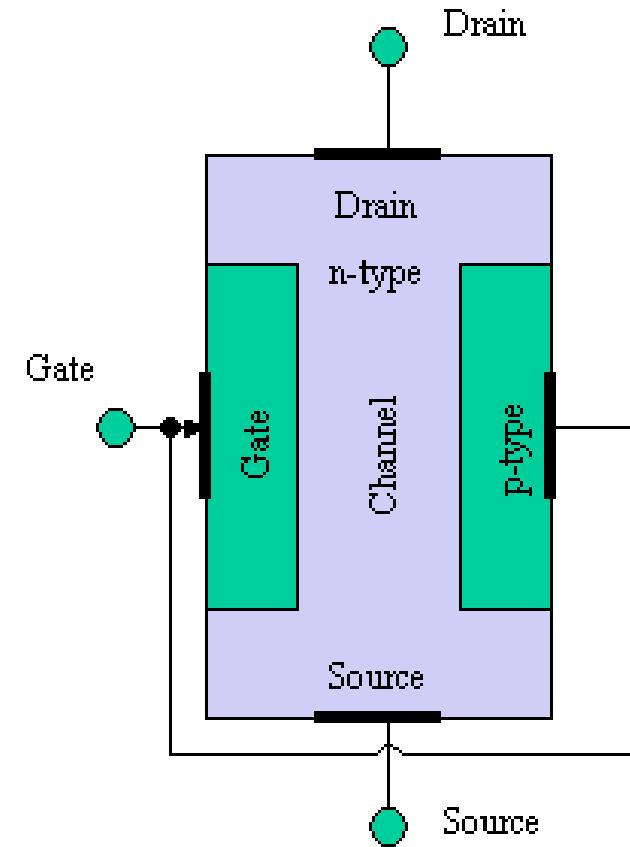
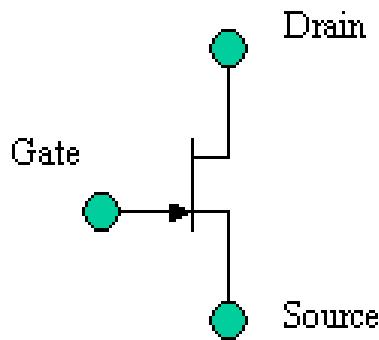
Junction field-effect transistor (JFET)



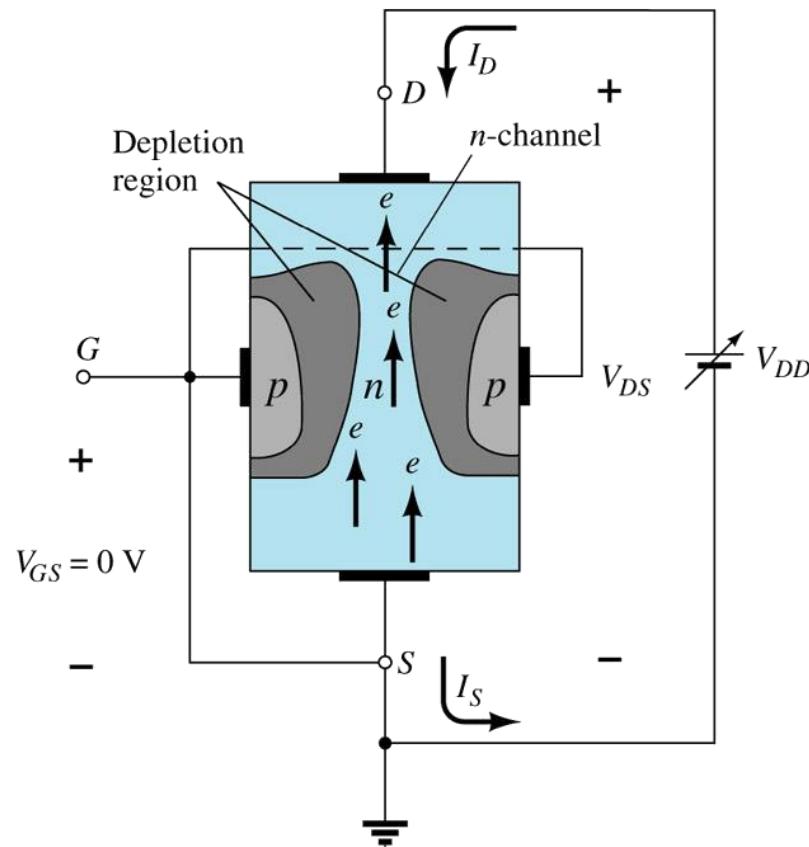
N-channel JFET..



(a)

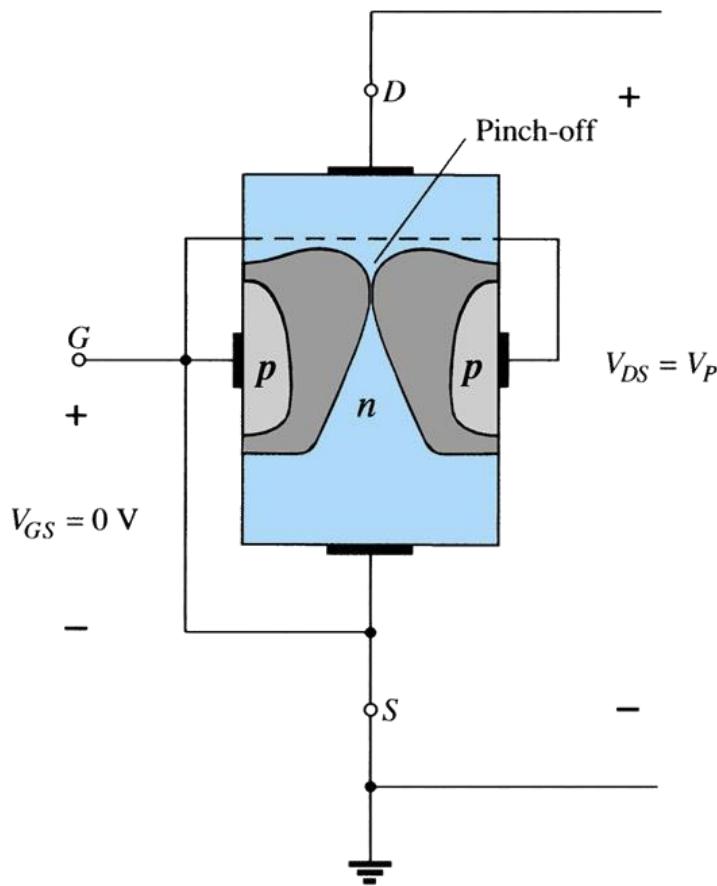


JFET for $V_{GS} = 0 \text{ V}$ and $0 < V_{DS} < |V_p|$

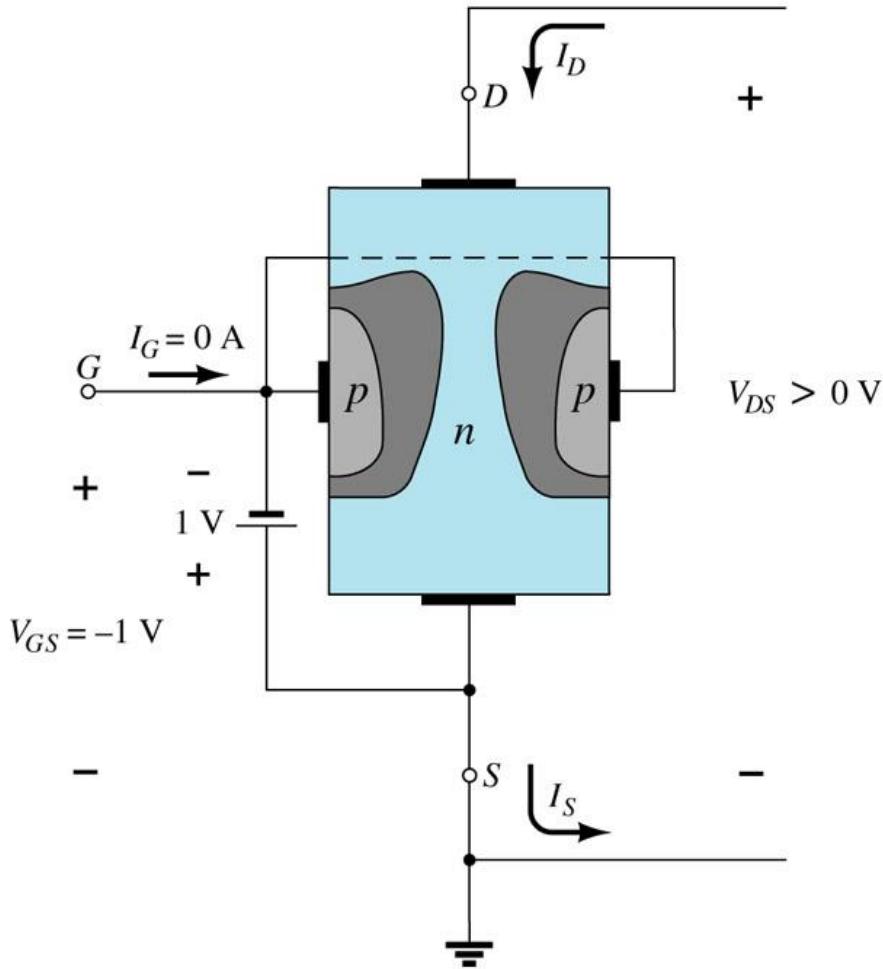


Channel becomes narrower as V_{DS} is increased

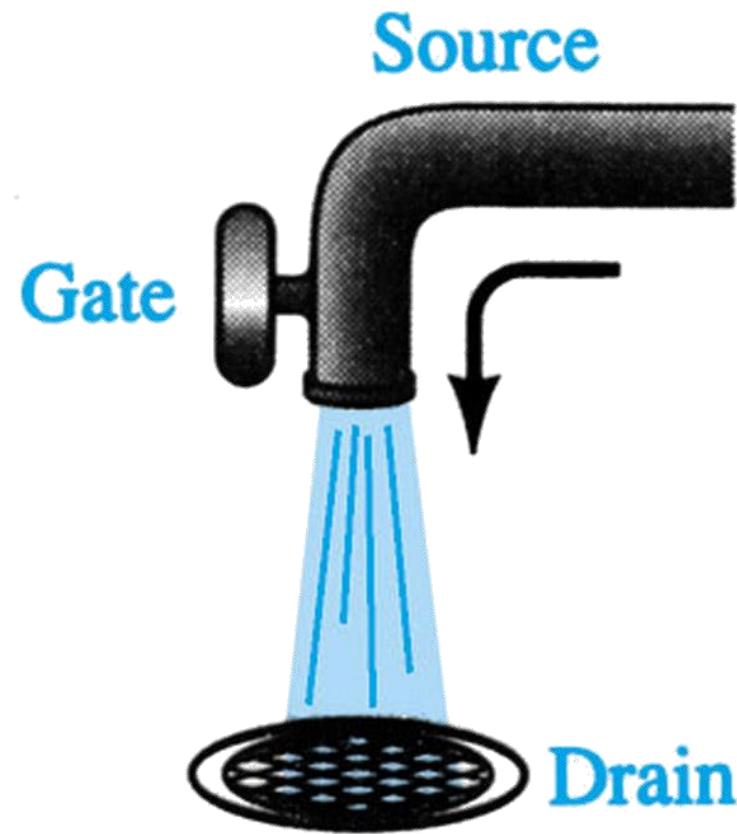
Pinch-off ($V_{GS} = 0 \text{ V}$, $V_{DS} = V_P$).



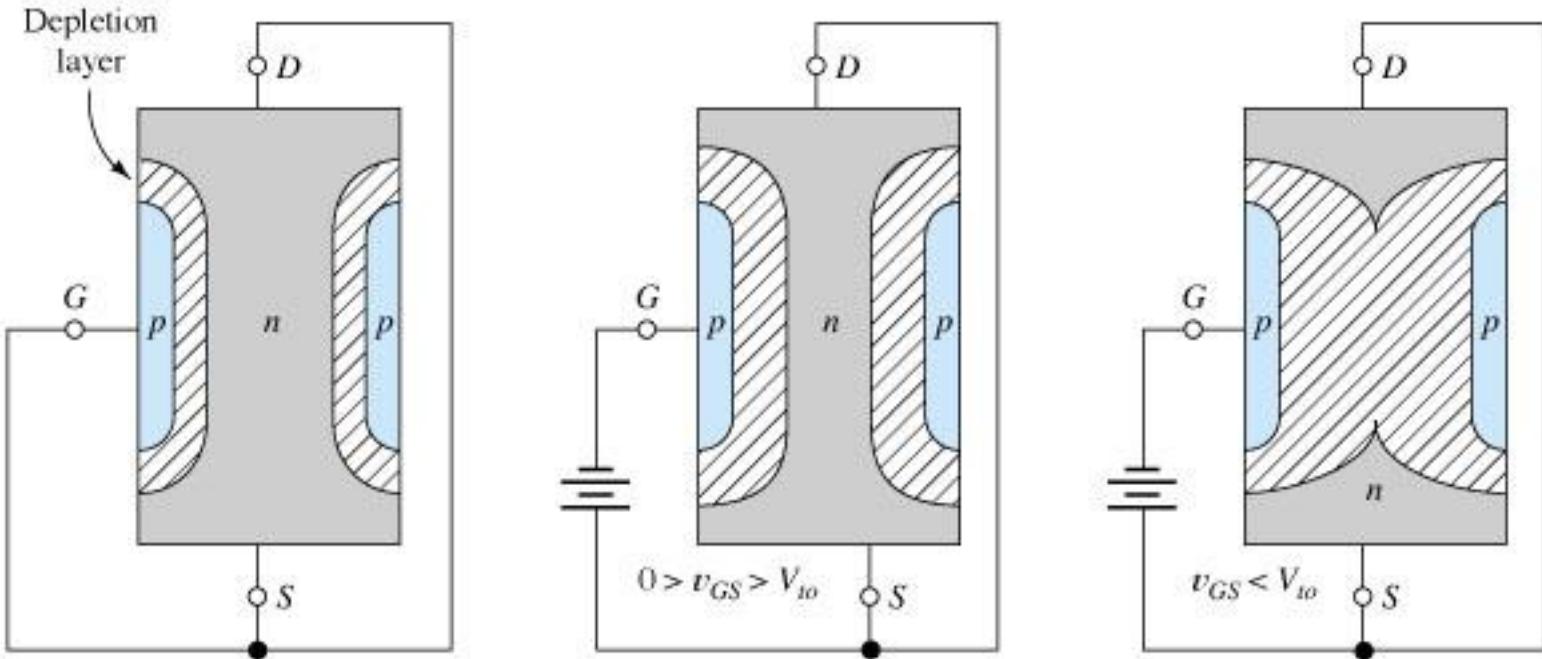
Application of
a negative
voltage to the
gate of a JFET.



Water analogy for the JFET control mechanism



Operation of JFET at Various Gate Bias Potentials



(a) Bias is zero and depletion layer is thin; low-resistance channel exists between the drain and the source

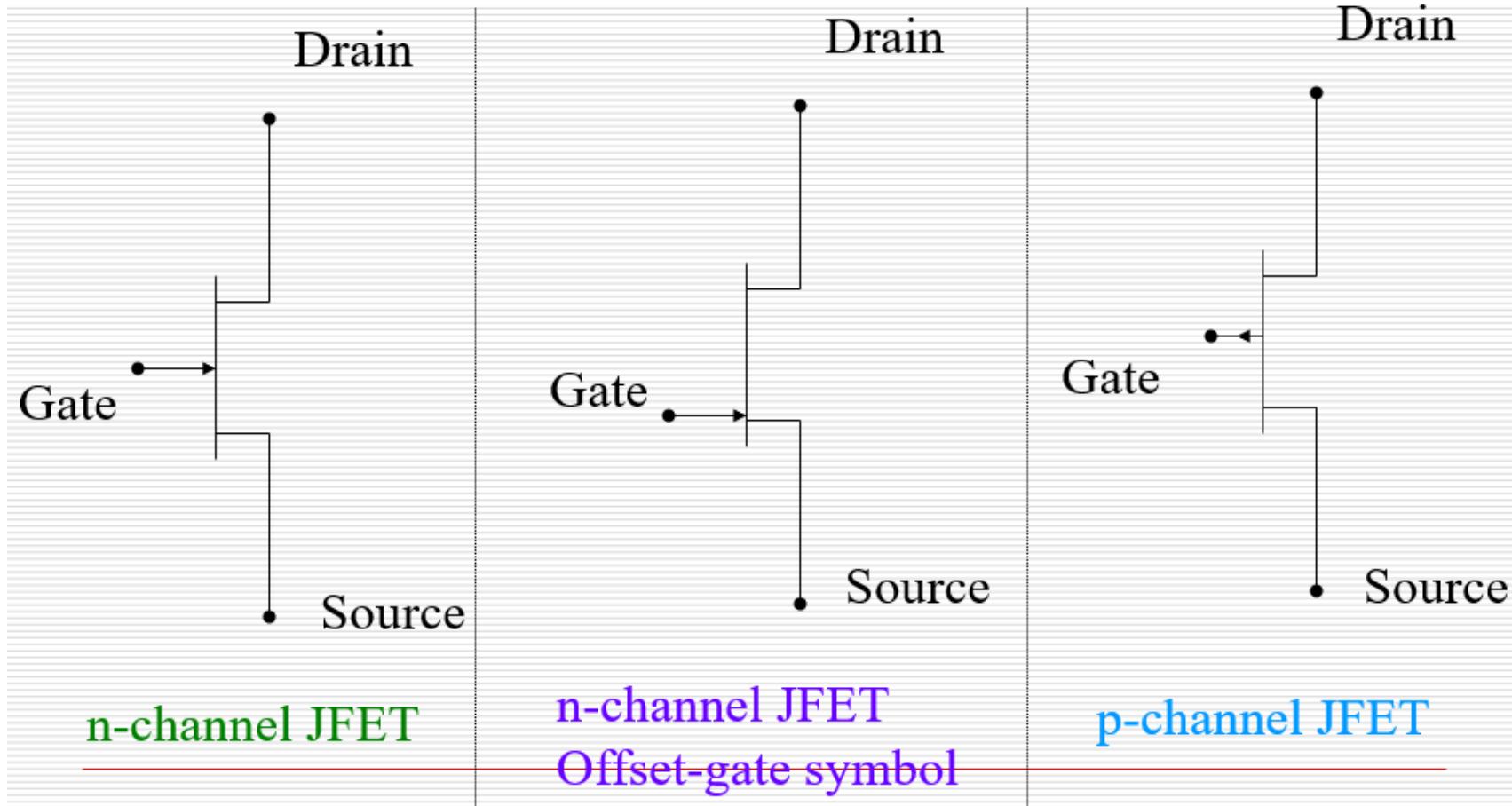
(b) Moderate gate-to-channel reverse bias results in narrower channel

(c) Bias greater than pinch-off voltage; no conductive path from drain to source

Figure: The nonconductive depletion region becomes broader with increased reverse bias.

(Note: The two gate regions of each FET are connected to each other.)

SYMBOLS



Junction FETs

- JFET is a high-input resistance device, while the BJT is comparatively low.
- If the channel is doped with a **donor impurity**, n-type material is formed and the channel current will consist of electrons.
- If the channel is doped with an **acceptor impurity**, p-type material will be formed and the channel current will consist of holes.
- N-channel devices have greater conductivity than p-channel types, since electrons have higher mobility than do holes; **thus n-channel JFETs are approximately twice as efficient conductors compared to their p-channel counterparts.**

N-channel JFET

- N channel JFET:
 - Major structure is n-type material (channel) between embedded p-type material to form 2 p-n junction.
 - In the normal operation of an n-channel device, the Drain (D) is positive with respect to the Source (S). Current flows into the Drain (D), through the channel, and out of the Source (S)
 - Because the resistance of the channel depends on the gate-to-source voltage (V_{GS}), the drain current (I_D) is controlled by that voltage

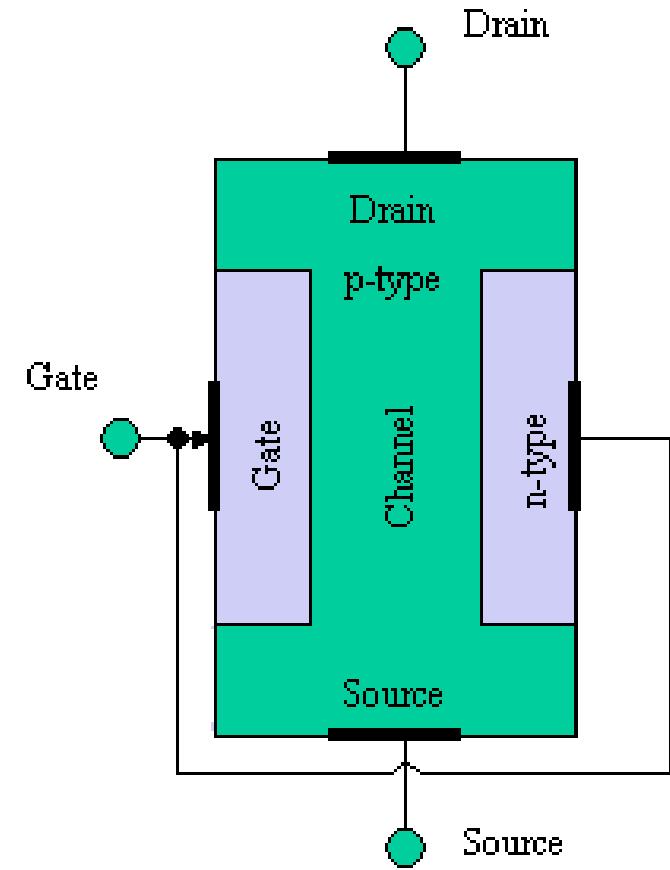
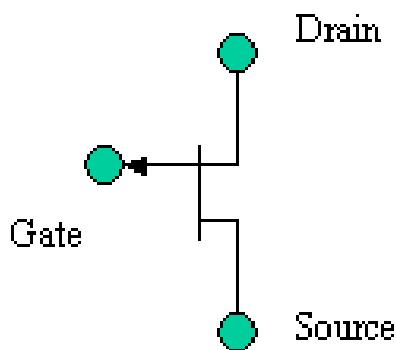
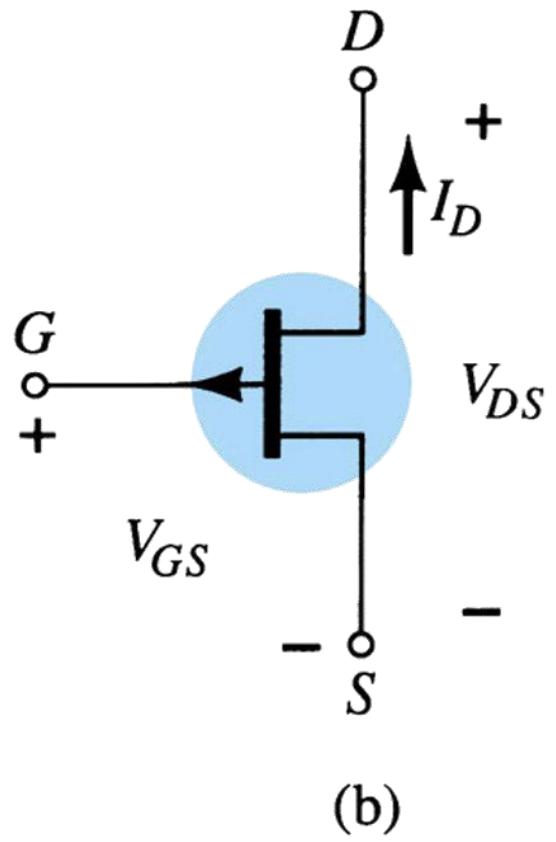
Advantages of FET

- High input impedance ($M\Omega$)
(Linear AC amplifier system)
- Temperature **stable** than BJT
- **Smaller** than BJT
- Can be fabricated with fewer processing
- BJT is bipolar – conduction both hole and electron
- FET is **unipolar** – uses only one type of current carrier
- Less noise compare to BJT
- Usually use as logic switch

Disadvantages of FET

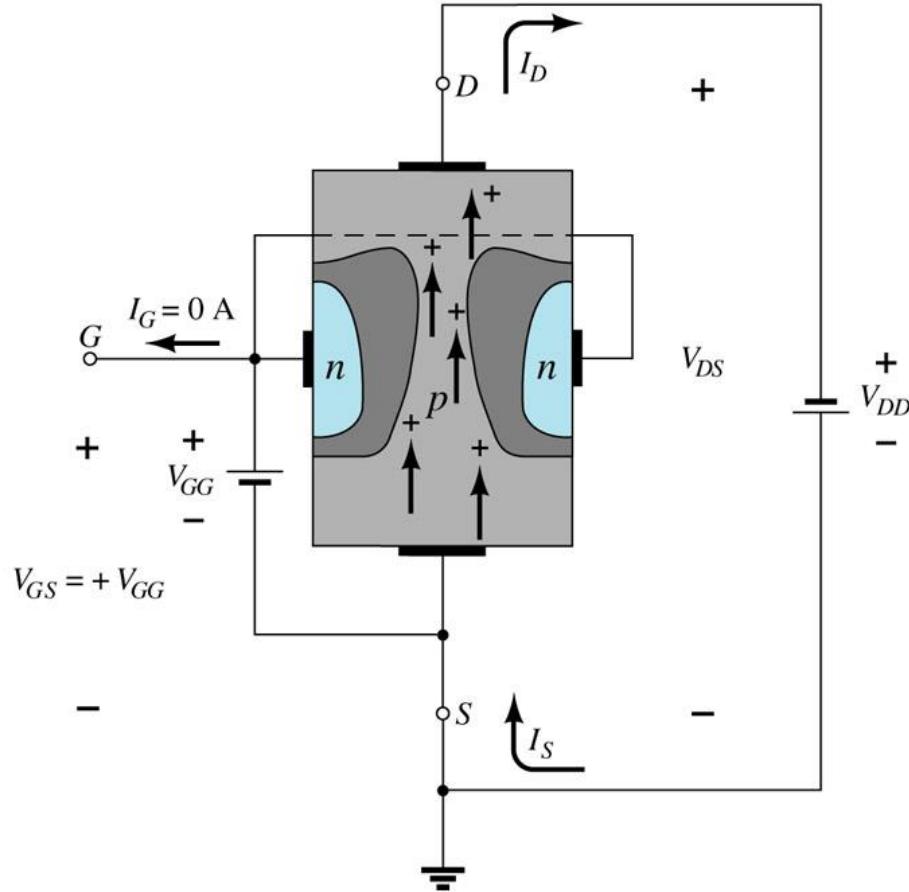
- Easy to damage compare to BJT

P-channel JFET



Cont.

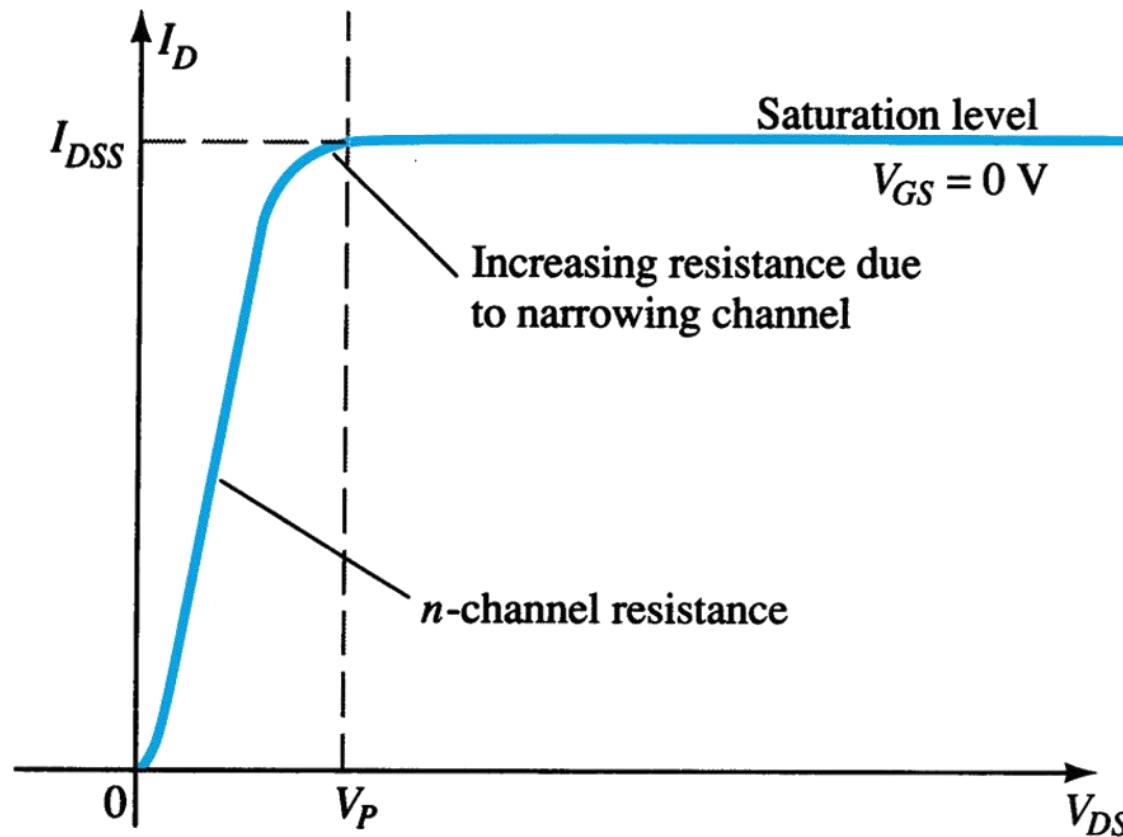
p-Channel JFET Biasing



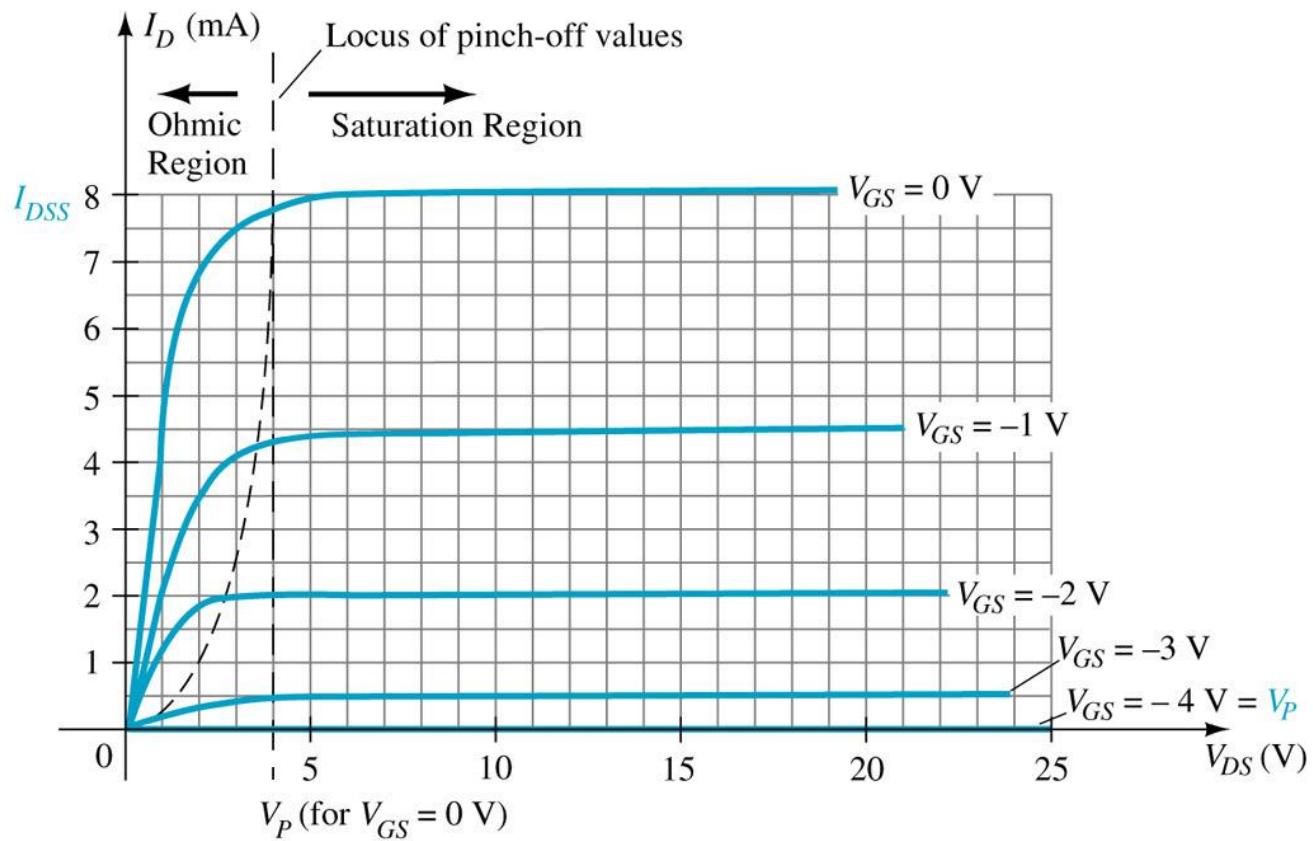
JFET Characteristic Curve

- To start, suppose $V_{GS}=0$
- Then, when V_{DS} is increased, I_D increases. Therefore, I_D is proportional to V_{DS} for small values of V_{DS}
- For larger value of V_{DS} , as V_{DS} increases, the depletion layer become wider, causing the resistance of channel increases.
- After the pinch-off voltage (V_p) is reached, the I_D becomes nearly constant (called as I_D maximum, I_{DSS} -Drain to Source current with Gate Shorted)

I_D versus V_{DS} for $V_{GS} = 0$ V.



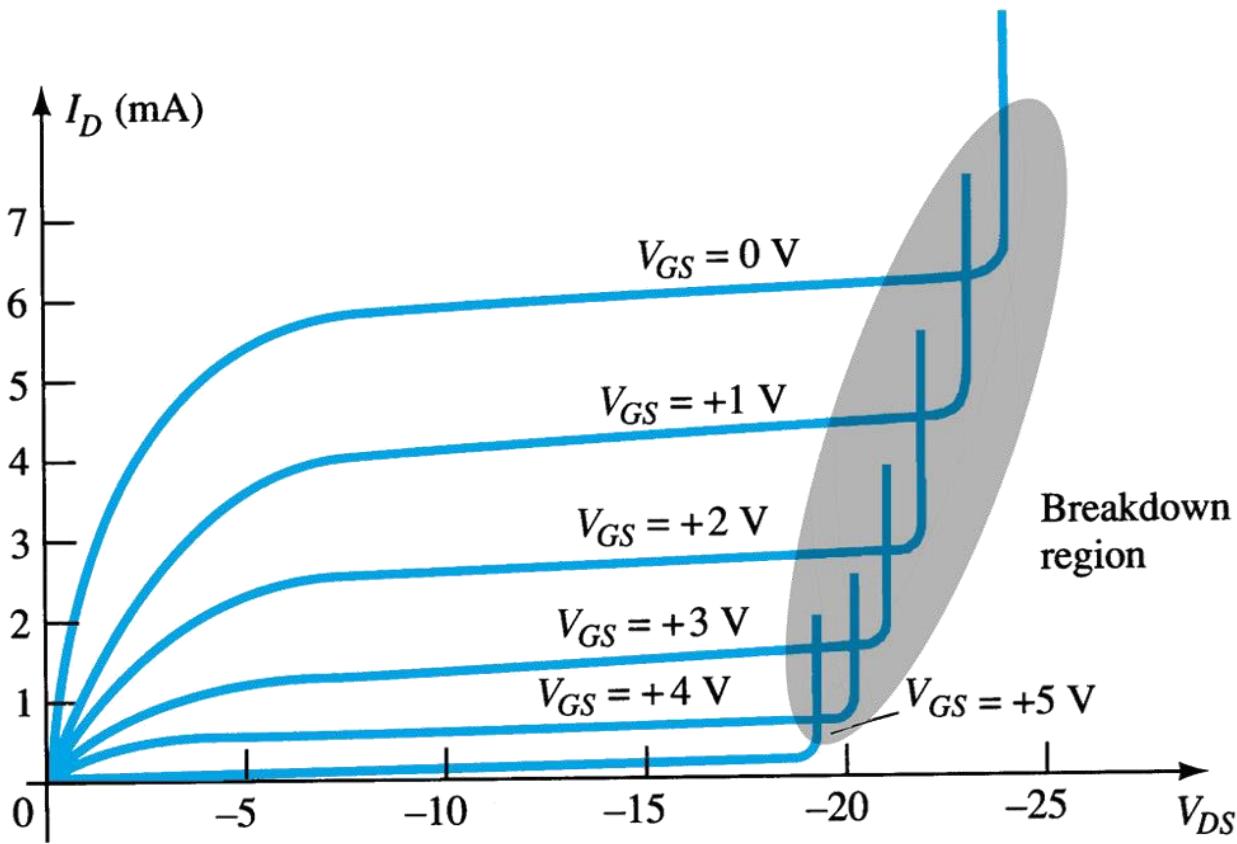
n-Channel JFET characteristics curve with $I_{DSS} = 8 \text{ mA}$ and $V_P = -4 \text{ V}$.



JFET Characteristic Curve..

- For negative values of V_{GS} , the gate-to-channel junction is reverse biased even with $V_{DS}=0$
- Thus, the initial channel resistance is higher (in which the initial slope of the curves is smaller for values of V_{GS} closer to the pinch-off voltage (V_p)
- The resistance value is under the control of V_{GS}
- If V_{GS} is less than pinch-off voltage, the resistance becomes an open-circuit ;therefore the device is in **cutoff ($V_{GS}=V_{GS(off)}$)**
- The region where I_D constant – The **saturation/pinch-off region**
- The region where I_D depends on V_{DS} is called the **linear/triode/ohmic region**

p-Channel JFET characteristics with $I_{DSS} = 6 \text{ mA}$ and $V_P = +6 \text{ V}$.



Operation of n-channel JFET

- JFET is biased with two voltage sources:
 - V_{DD}
 - V_{GG}
- V_{DD} generate voltage bias between Drain (D) and Source (S) – V_{DS}
- V_{DD} causes drain current, I_D flows from Drain (D) to Source (S)
- V_{GG} generate voltage bias between Gate (G) and Source (S) with negative polarity source is connected to the Gate Junction (G) – reverse-biases the gate; therefore gate current, $I_G = 0$.
- V_{GG} is to produce depletion region in N channel so that it can control the amount of drain current, I_D that flows through the channel

Transfer Characteristics

- The input-output transfer characteristic of the JFET is not as straight forward as it is for the BJT.
- In BJT:

$$I_C = \beta I_B$$

- which β is defined as the relationship between I_B (input current) and I_C (output current).
- In JFET, the relationship between V_{GS} (input voltage) and I_D (output current) is used to define the transfer characteristics. It is called as Shockley's Equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

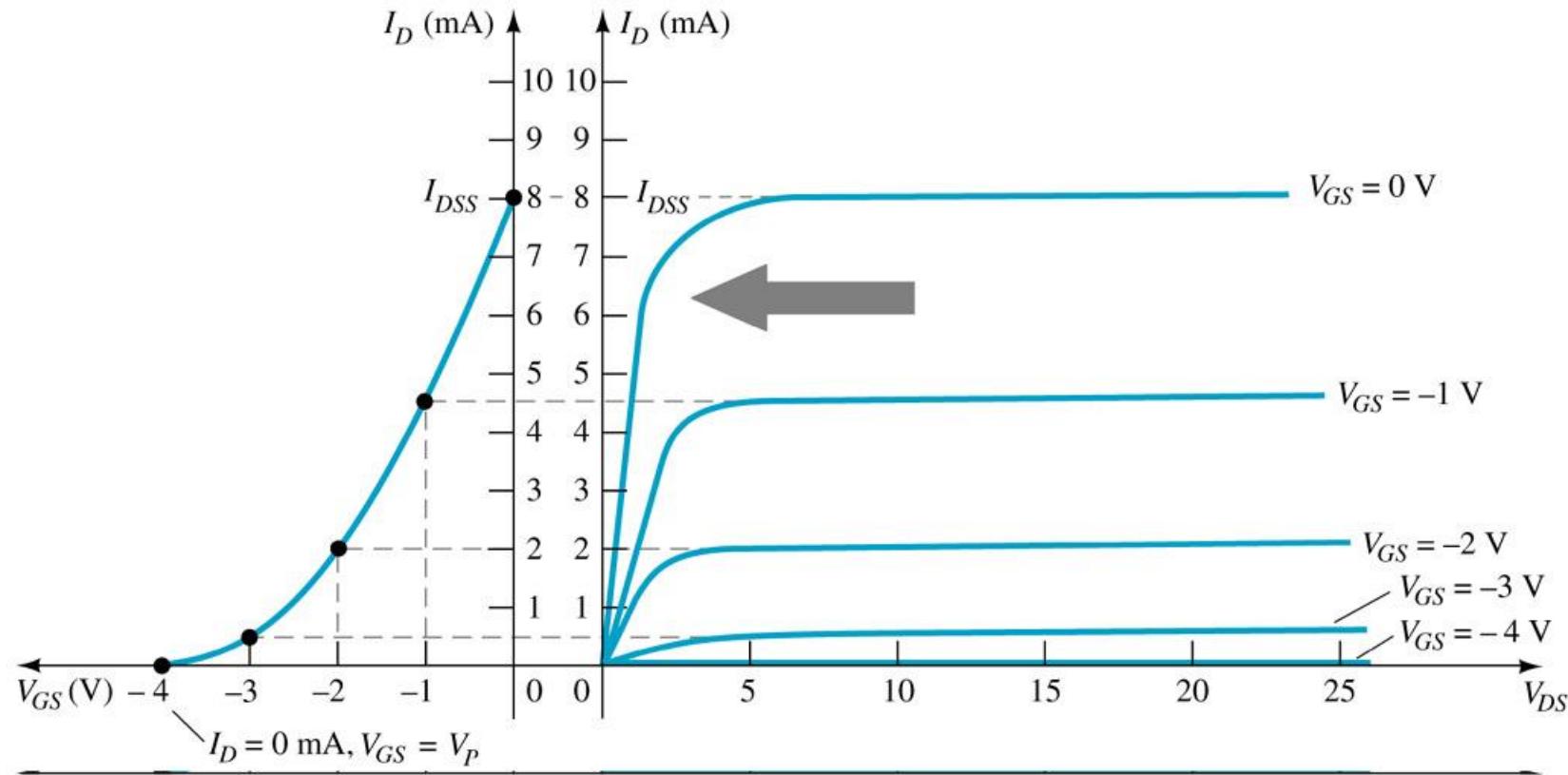
$V_P = V_{GS(\text{OFF})}$

- The relationship is more complicated (and not linear)
- As a result, FET's are often referred to as square law devices

Cont.

- Defined by Shockley's equation:
- $$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$
 $V_P = V_{GS(off)}$
- Relationship between I_D and V_{GS} .
- Obtaining transfer characteristic curve axis point from Shockley:
 - When $V_{GS} = 0$ V, $I_D = I_{DSS}$
 - When $V_{GS} = V_{GS(off)}$ or V_p , $I_D = 0$ mA

Cont.



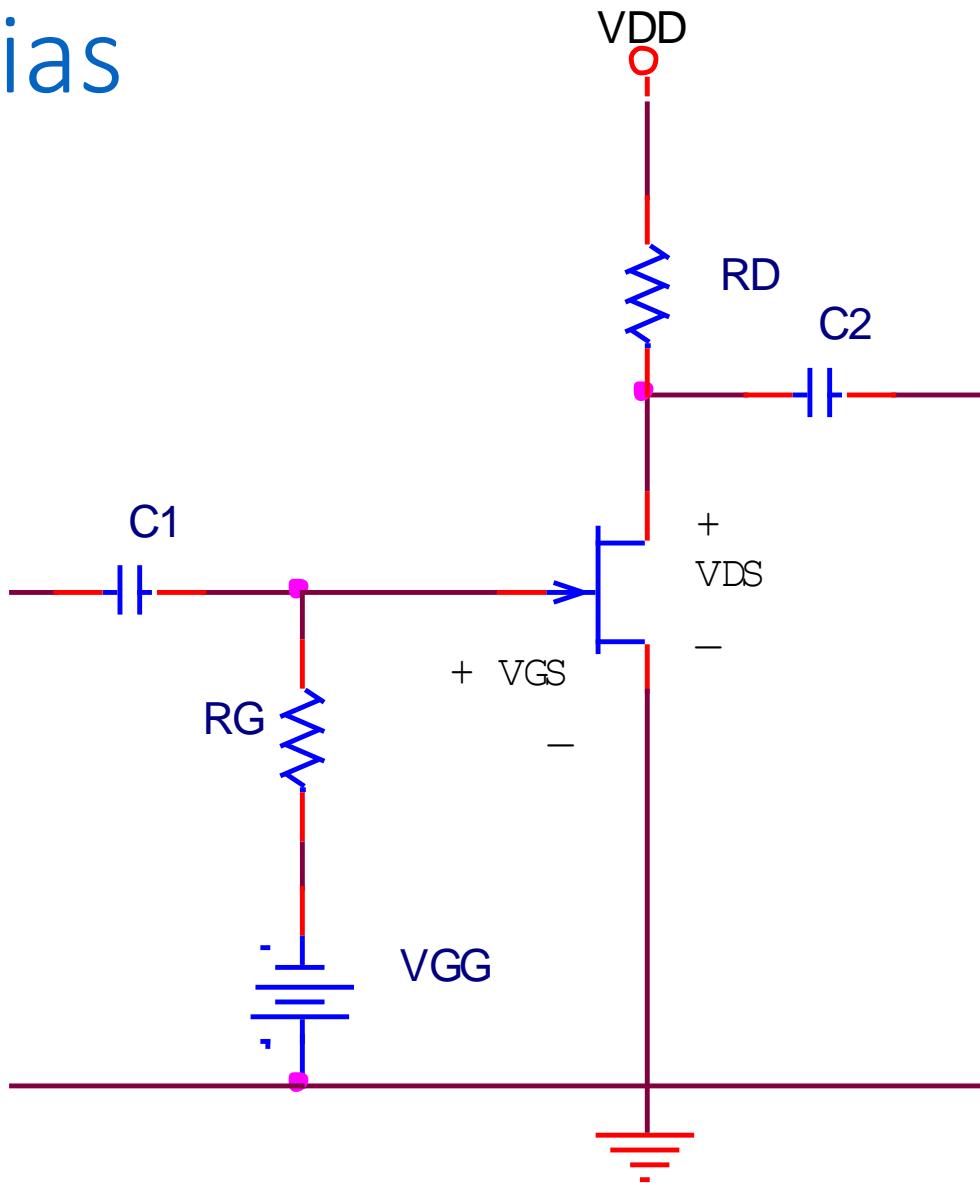
JFET Transfer Characteristic Curve

JFET Characteristic Curve

DC JFET Biasing

- Just as we learned that the BJT must be biased for proper operation, the JFET also must be biased for operation point (I_D , V_{GS} , V_{DS})
- In most cases the ideal Q-point will be at the **middle** of the transfer characteristic curve, which is **about half of the I_{DSS}** .
- 3 types of DC JFET biasing configurations :
 - Fixed-bias
 - Self-bias
 - Voltage-Divider Bias

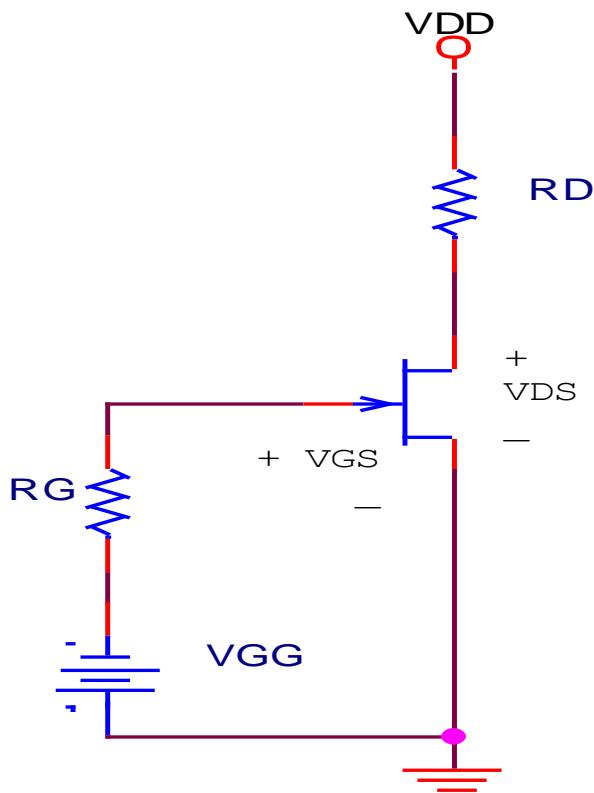
Fixed-bias



- Use two voltage sources: V_{GG} , V_{DD}
- V_{GG} is reverse-biased at the Gate – Source (G-S) terminal, thus no current flows through R_G ($I_G = 0$).

Cont.

- DC analysis
 - All capacitors replaced with open-circuit



1. Input Loop

By using KVL at loop 1:

$$V_{GG} + V_{GS} = 0$$
$$V_{GS} = -V_{GG}$$

For graphical solution, use $V_{GS} = -V_{GG}$ to draw the load line

For mathematical solution, replace $V_{GS} = -V_{GG}$ in Shockley's Eq., therefore:

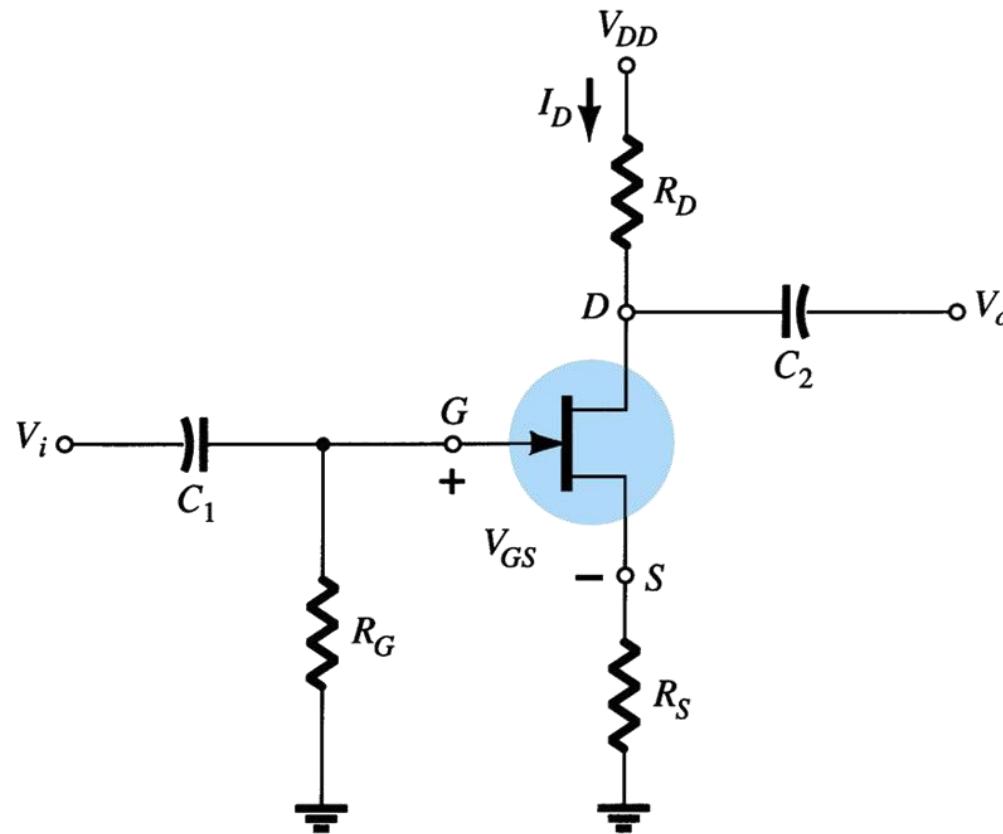
2. Output loop

$$-V_{DD} + I_D R_D + V_{DS} = 0$$
$$V_{DS} = V_{DD} - I_D R_D$$

3. Then, plot transfer characteristic curve by using Shockley's Equation

Self-bias

- Using only one voltage source



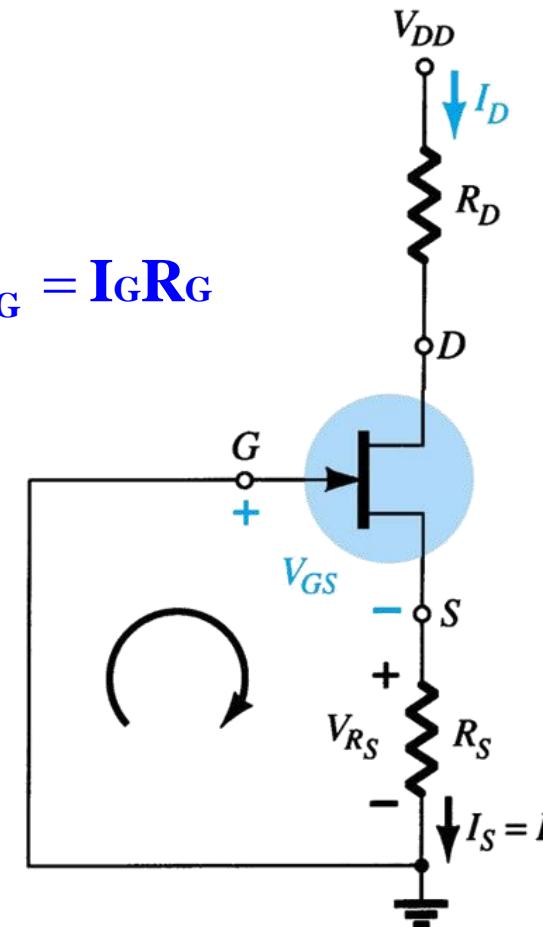
DC analysis of the self-bias configuration.

Since $I_G \approx 0A$, $V_{RG} = I_G R_G$
thus $V_{RG} = 0A$,

$$V_{RS} = I_D R_S$$

$$V_{GS} + V_{RS} = 0$$

$$\begin{aligned} V_{GS} &= -V_{RS} \\ &= -I_D R_S \end{aligned}$$



Q point for V_{GS}

Mathematical Solutions:

- Replace

$$V_{GS} = -I_D R_s \quad \text{in the Shockley's Equation:}$$

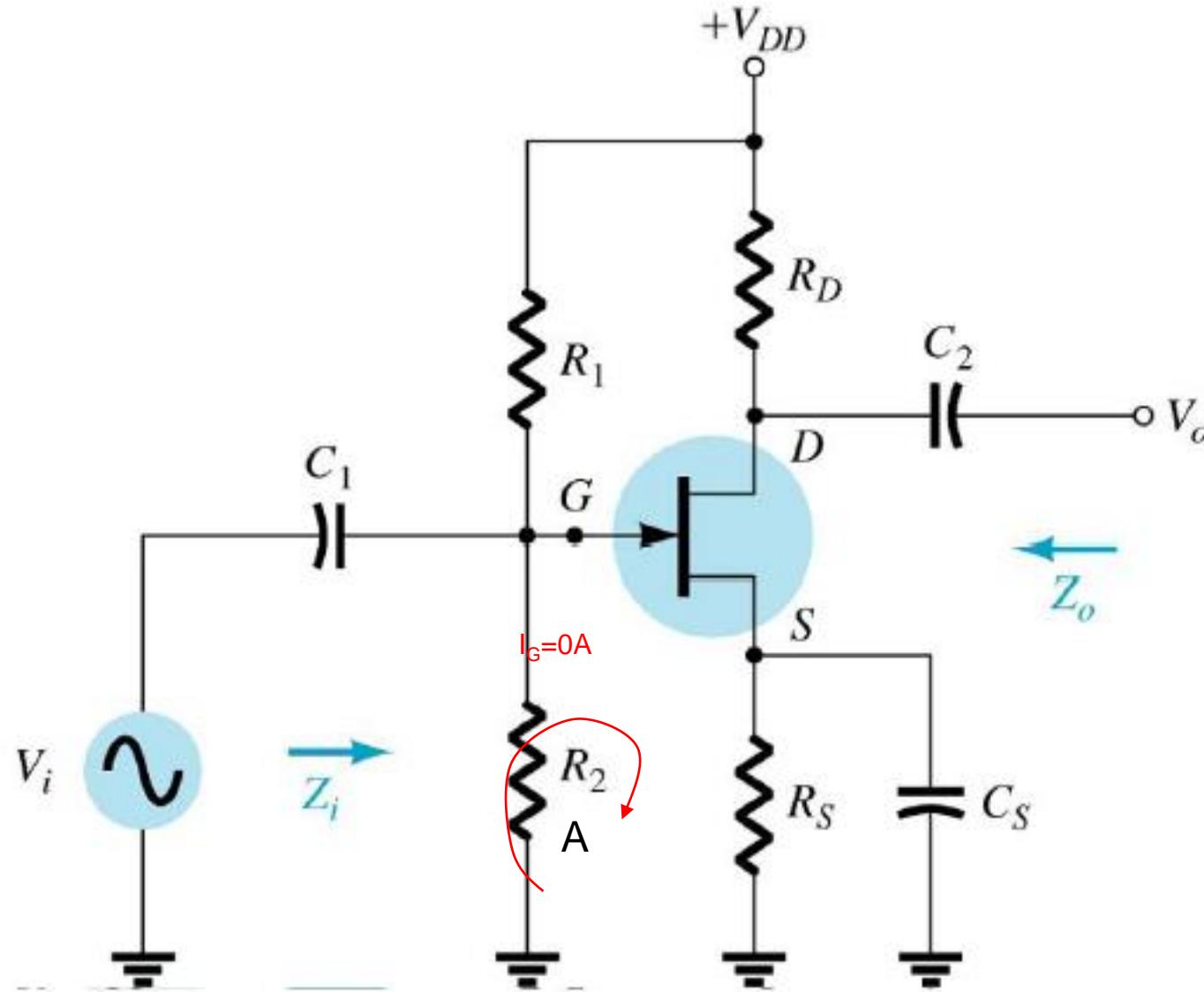
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad V_P = V_{GS(off)}$$

therefore,

$$I_D = I_{DSS} \left(1 - \frac{(-I_D R_s)}{V_P} \right)^2$$

- By using, quadratic equation and formula, choose value of I_D that relevant within the range (0 to I_{DSS}): nearly to $I_{DSS}/2$
- Find V_{GS} by using $V_{GS} = -I_D R_s$ also choose V_{GS} that within the range (0 to V_P)

Voltage-divider bias

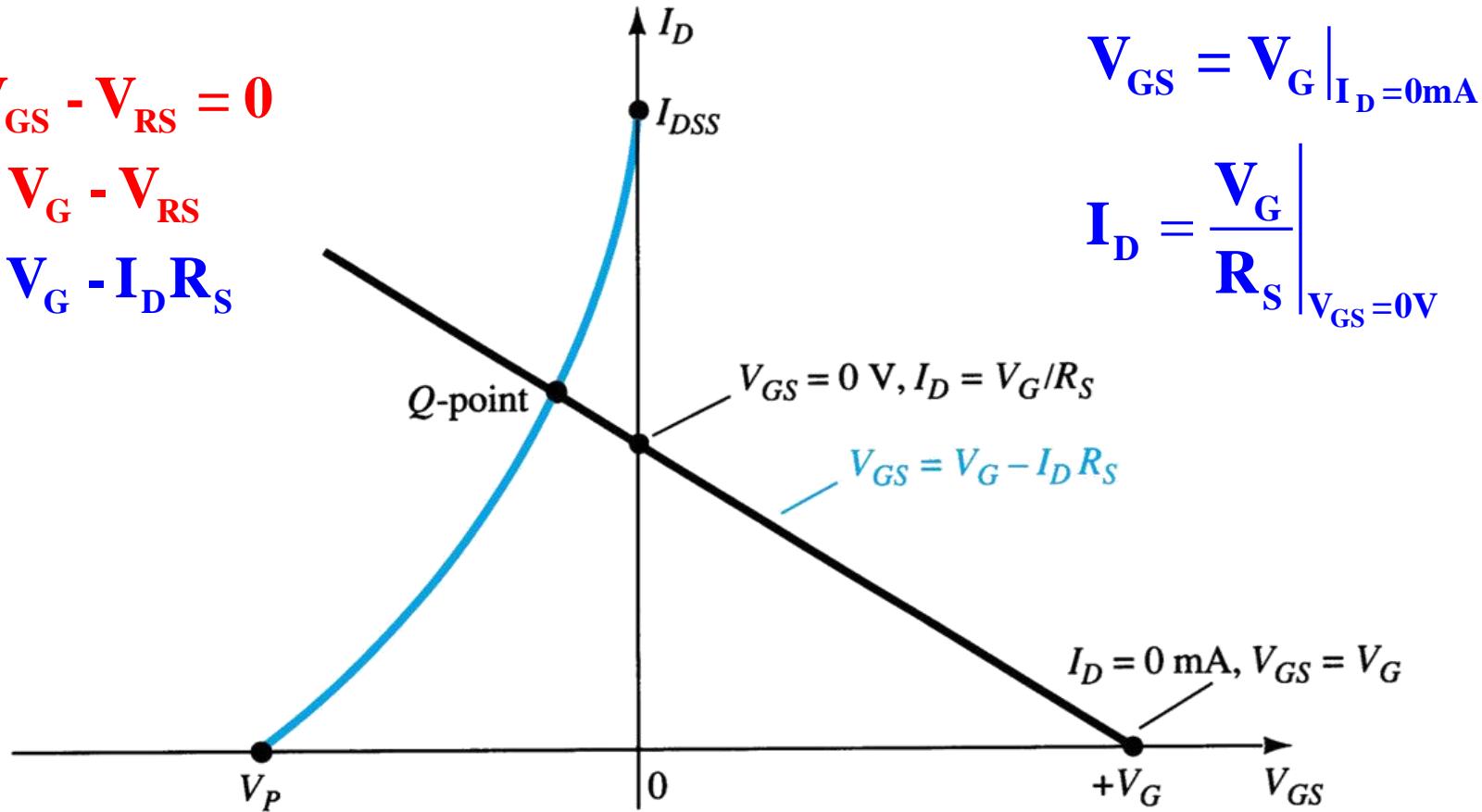


Sketching the network equation for the voltage-divider configuration.

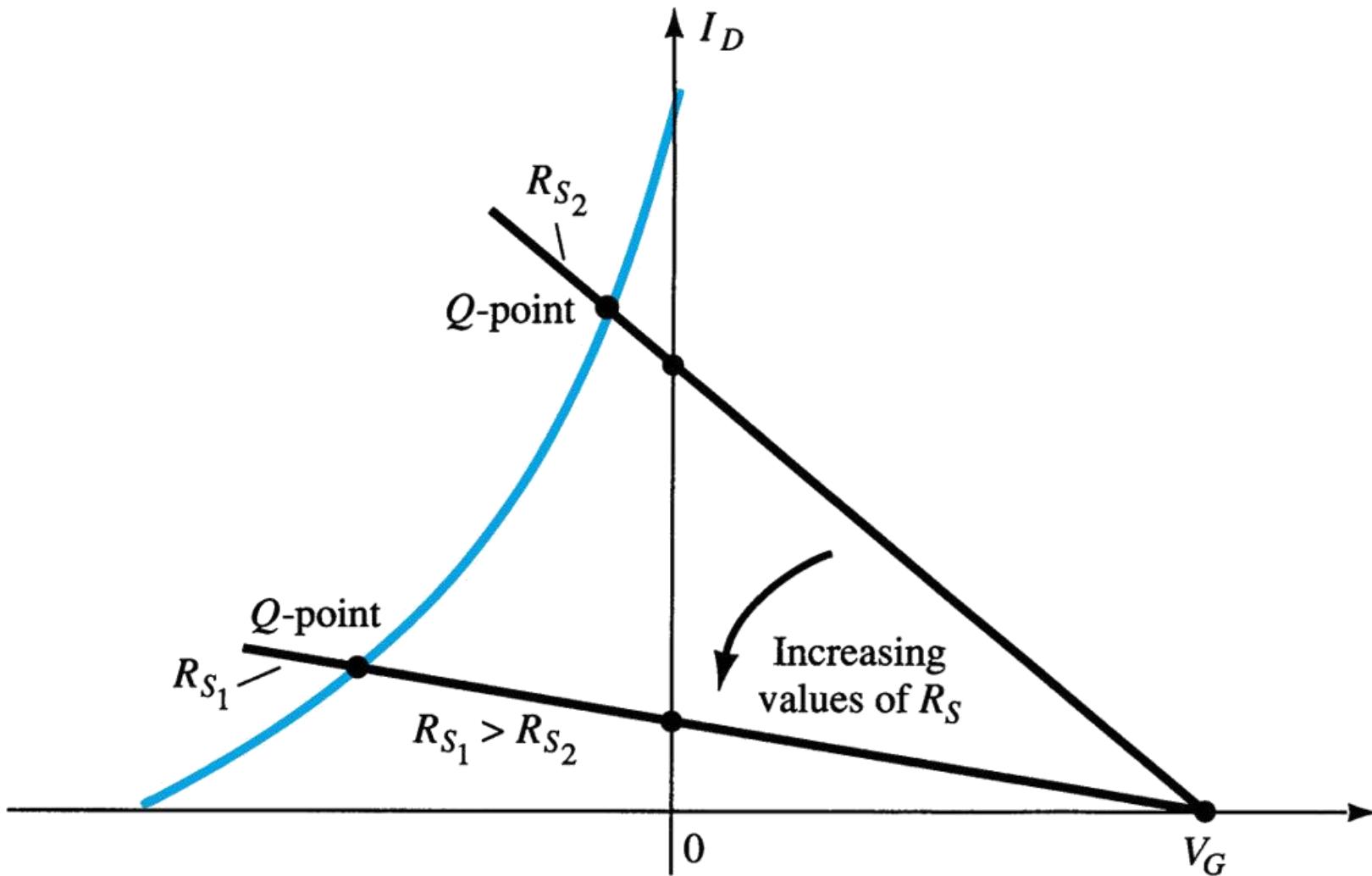
$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - V_{RS}$$

$$V_{GS} = V_G - I_D R_S$$

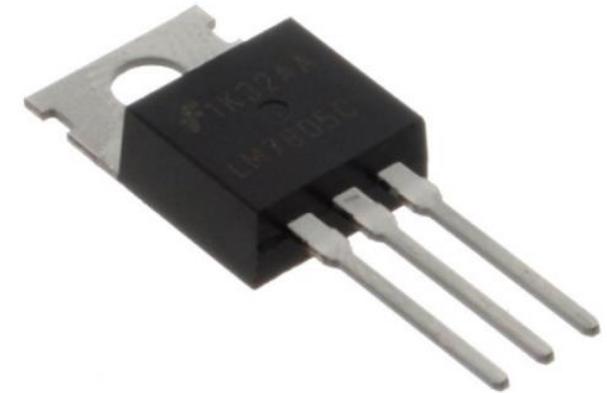


Effect of R_S on the resulting Q-point.



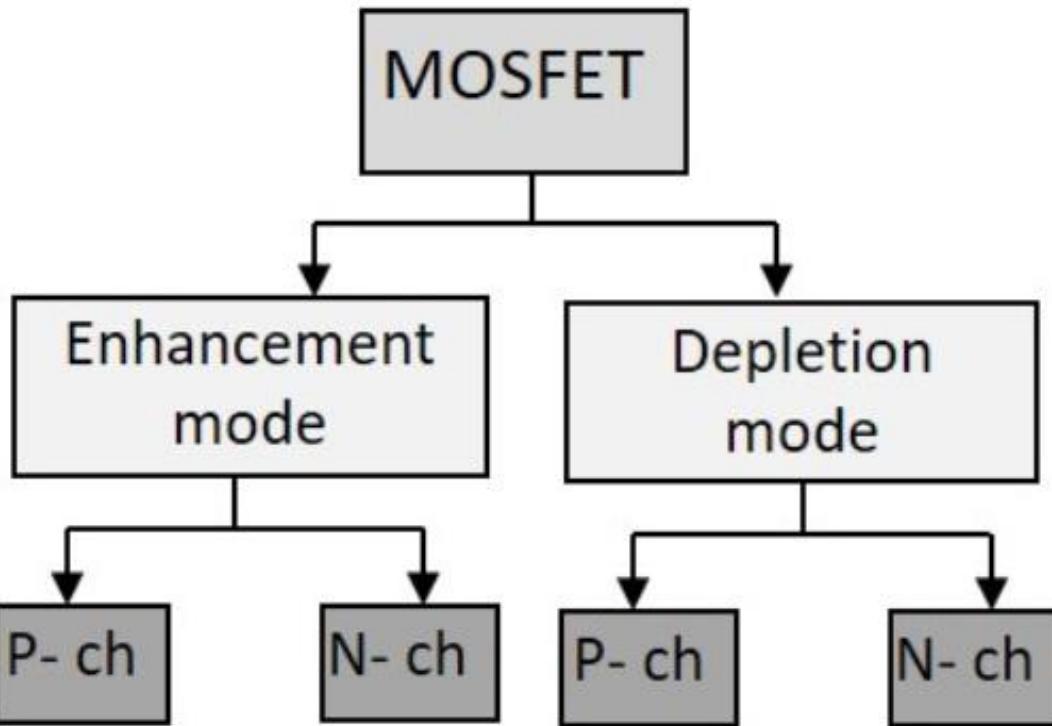
MOSFET

- FETs have a few disadvantages:
- High drain resistance, moderate input impedance and slower operation.
- To overcome these disadvantages, the MOSFET which is an advanced FET is invented.
- MOSFET stands for **Metal Oxide Silicon Field Effect Transistor** or Metal Oxide Semiconductor Field Effect Transistor.
- This is also called as **IGFET** meaning **Insulated Gate Field Effect Transistor**.
- The FET is operated in both **depletion and enhancement modes** of operation. The following figure shows how a practical MOSFET looks like



Classification of MOSFETs

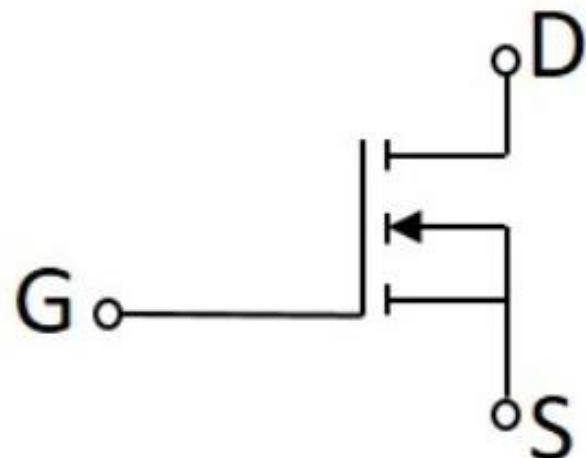
Depending upon the type of materials used in the construction, and the type of operation, MOSFETs are classified as in the following figure.



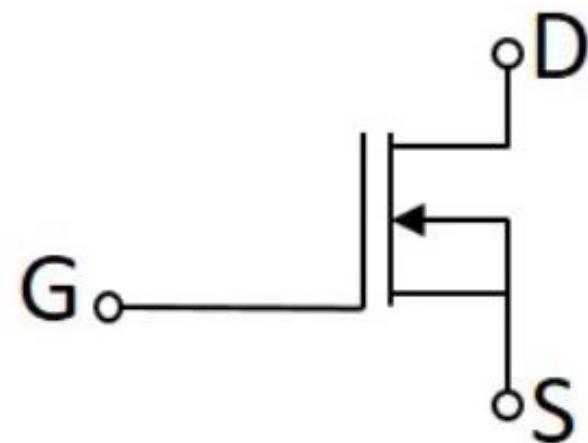
- P- ch = P- channel
- N- ch = N- channel

The **N-channel MOSFETs** are simply called as **NMOS**. The symbols for N-channel MOSFET are as given below.

Symbols of N-Channel MOSFET



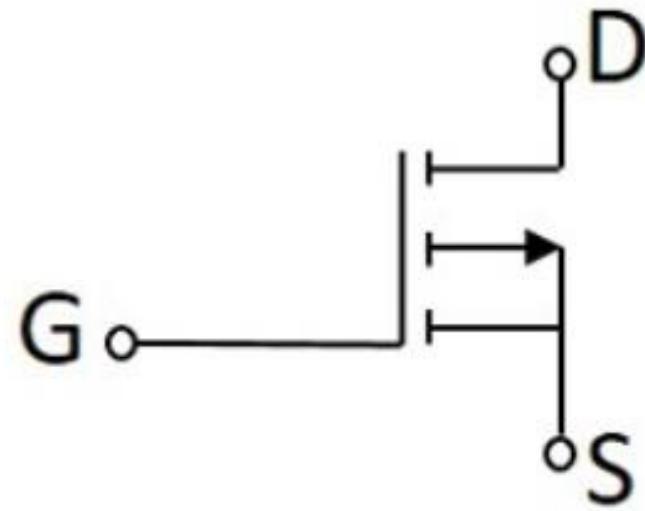
Enhancement Mode



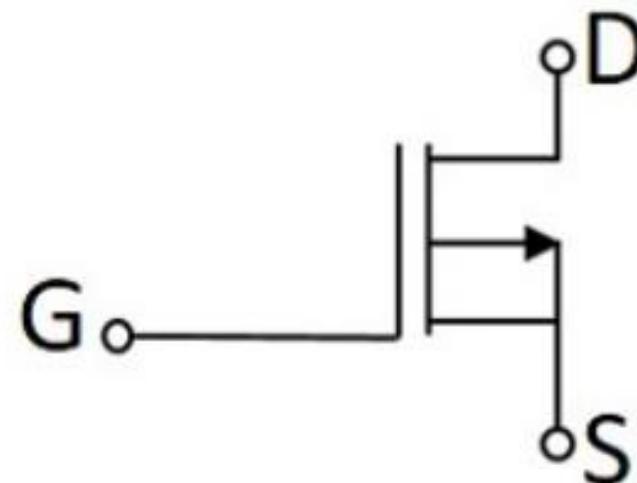
Depletion Mode

The **P-channel MOSFETs** are simply called as **PMOS**. The symbols for P-channel MOSFET are as given below.

Symbols of P-Channel MOSFET

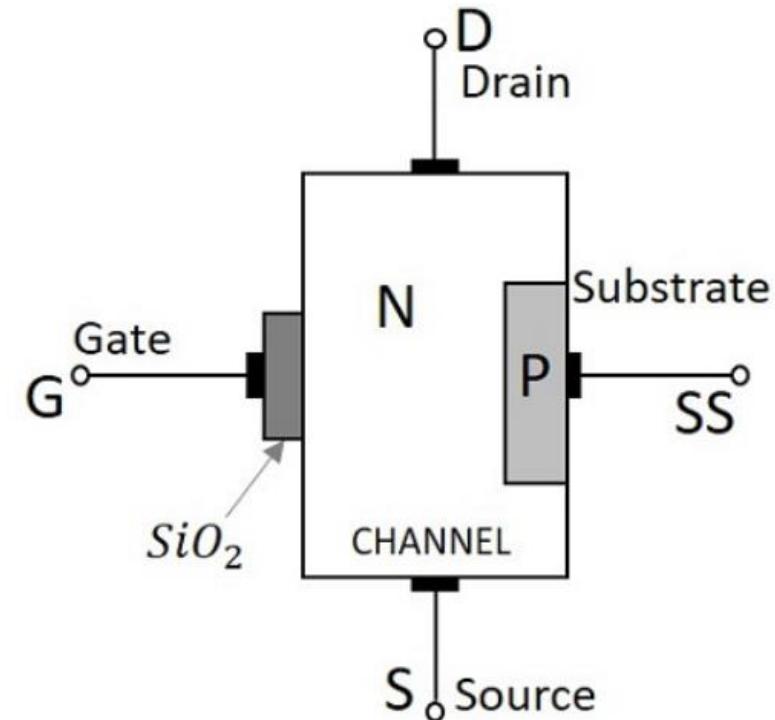
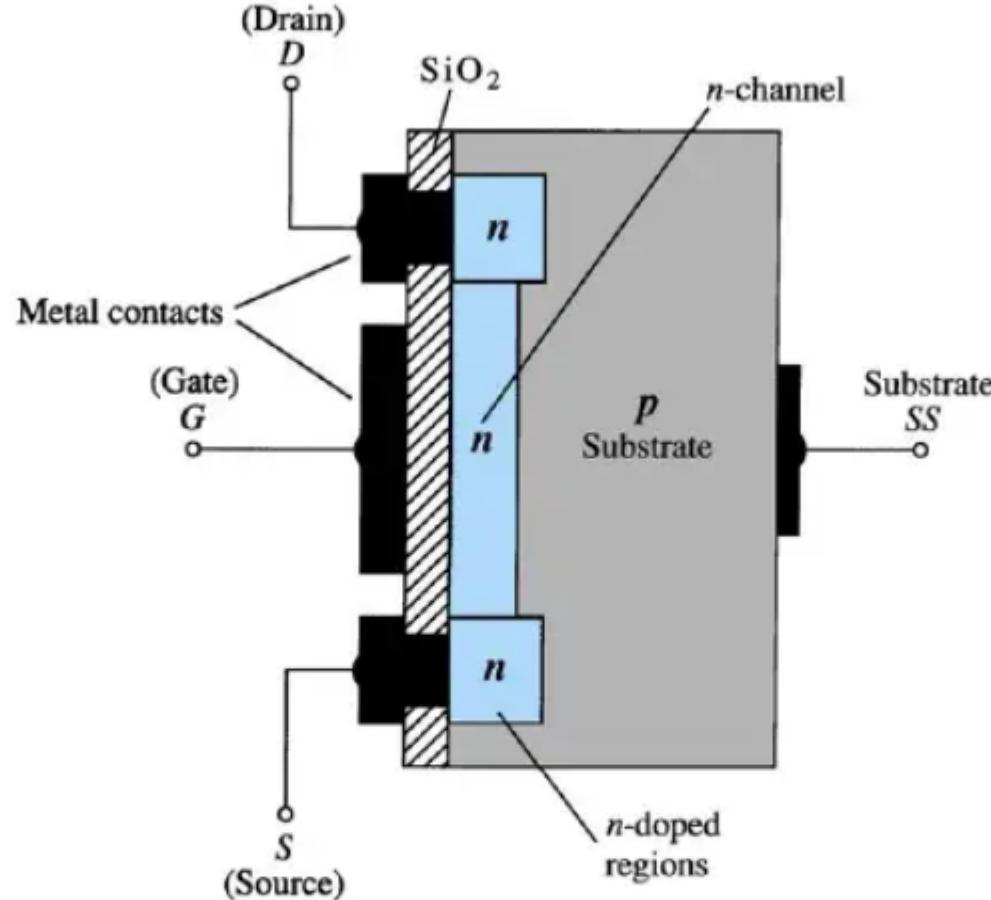


Enhancement Mode



Depletion Mode

Depletion Mode MOSFET Construction



The Drain (D) and Source (S) leads connect to the to n-doped regions

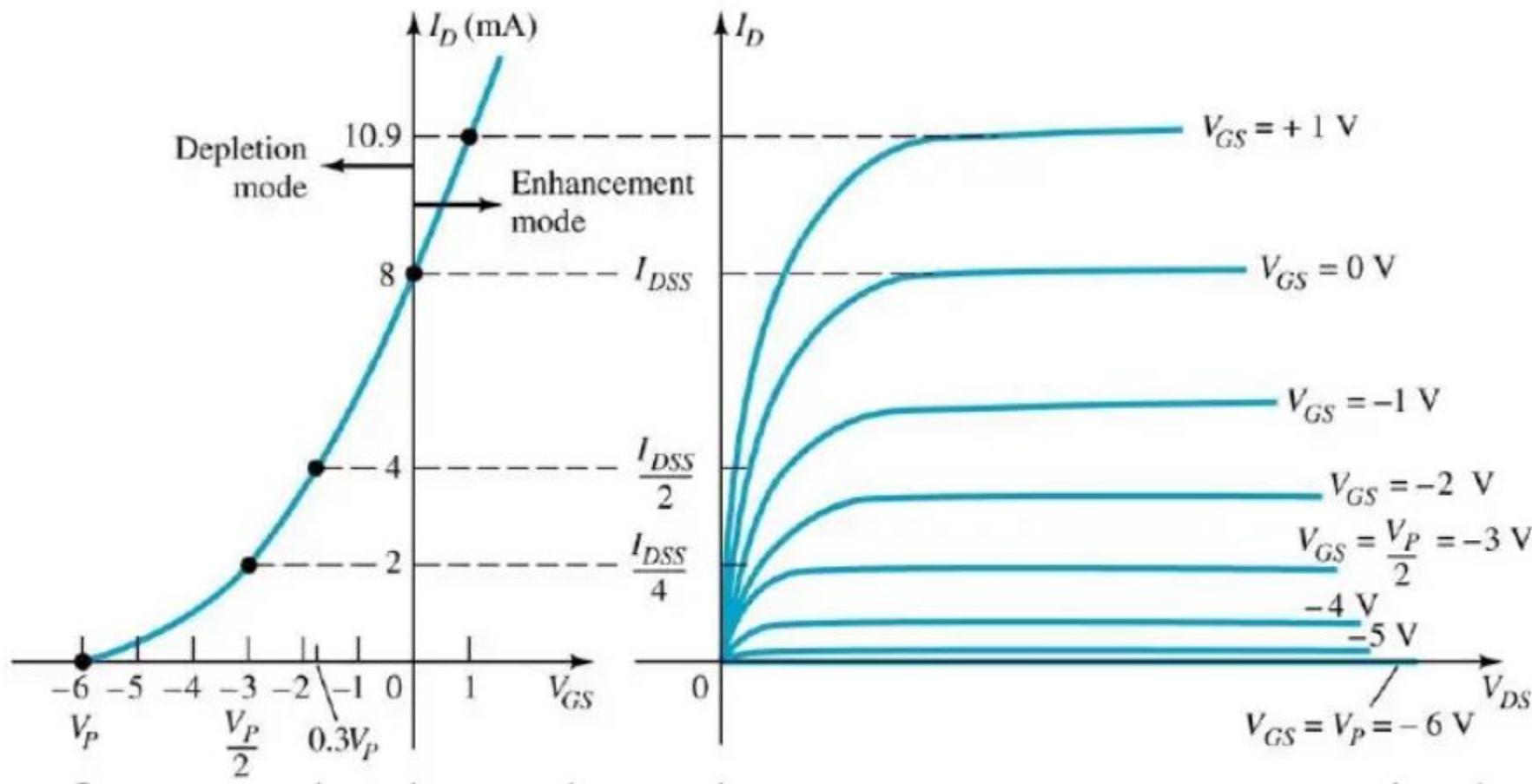
These N-doped regions are connected via an n-channel

This n-channel is connected to the Gate (G) via a thin insulating layer of SiO_2

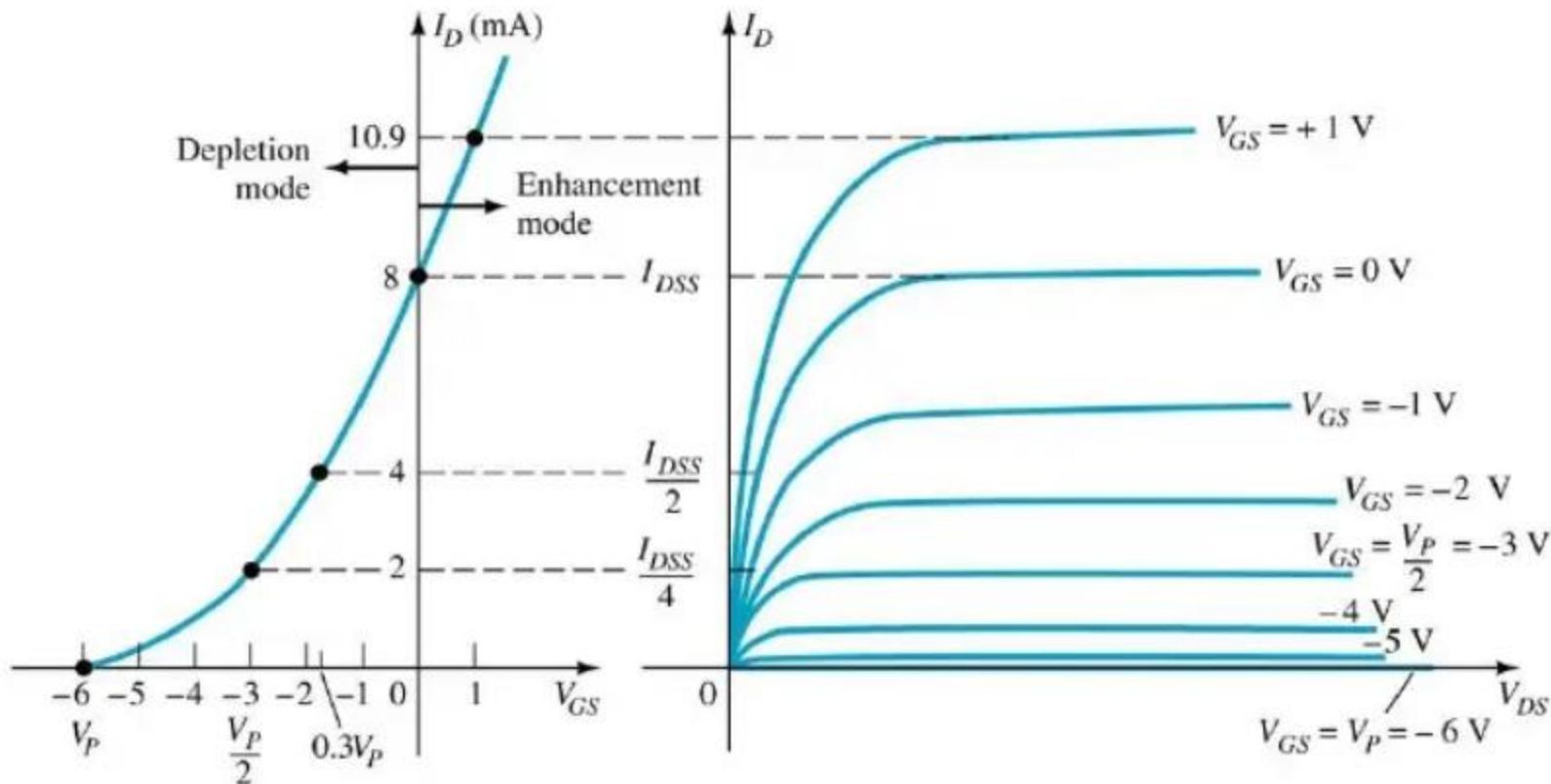
The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Basic Operation

A D-MOSFET may be biased to operate in two modes:
the **Depletion mode** or the **Enhancement mode**



D-MOSFET Depletion Mode Operation



The transfer characteristics are similar to the JFET

In Depletion Mode operation:

When V_{GS} = 0V, I_D = I_{DSS}

When V_{GS} < 0V, I_D < I_{DSS}

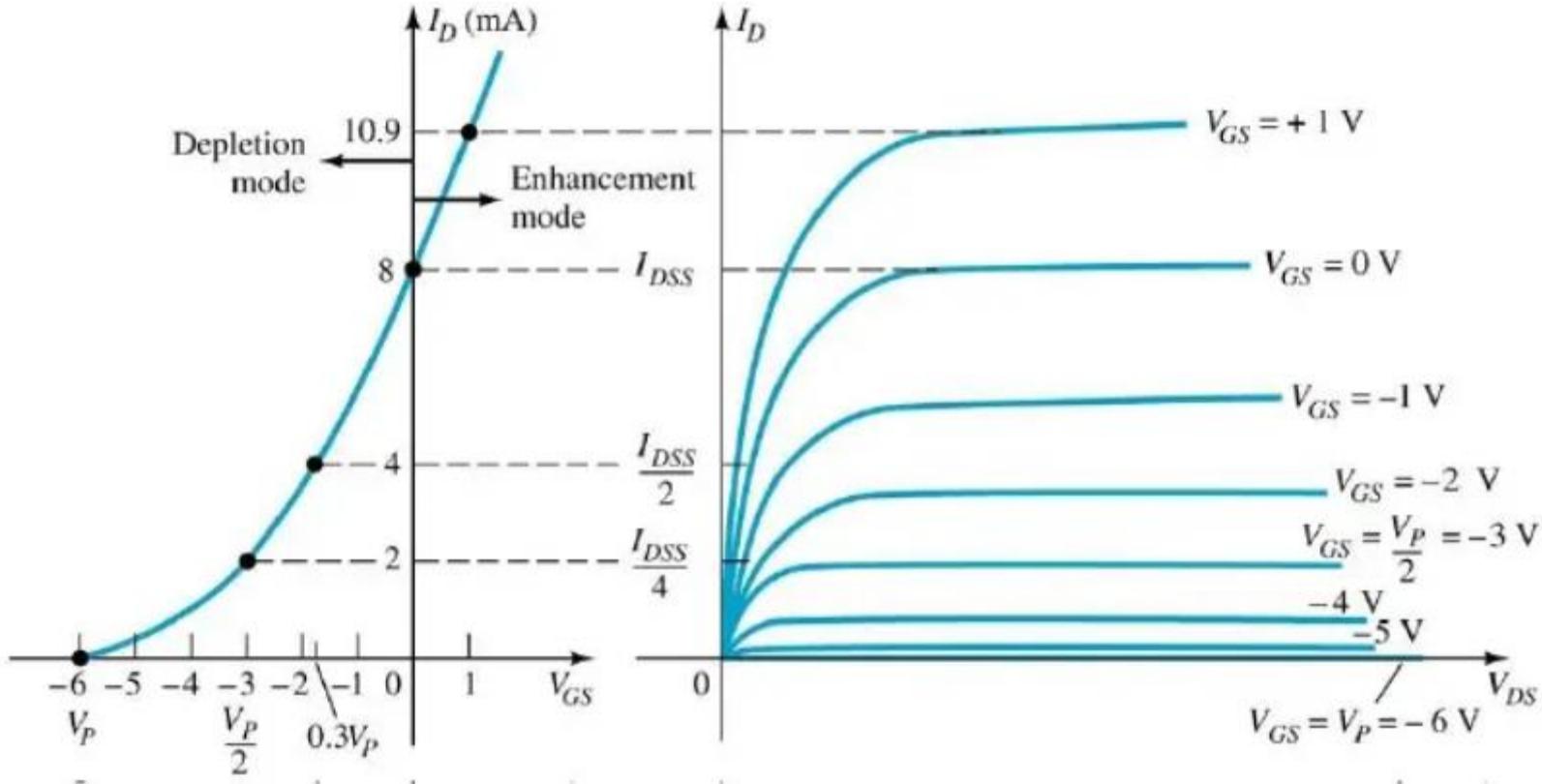
When V_{GS} > 0V, I_D > I_{DSS}

The formula used to plot the Transfer Curve, is:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Cont.

D-MOSFET Enhancement Mode Operation

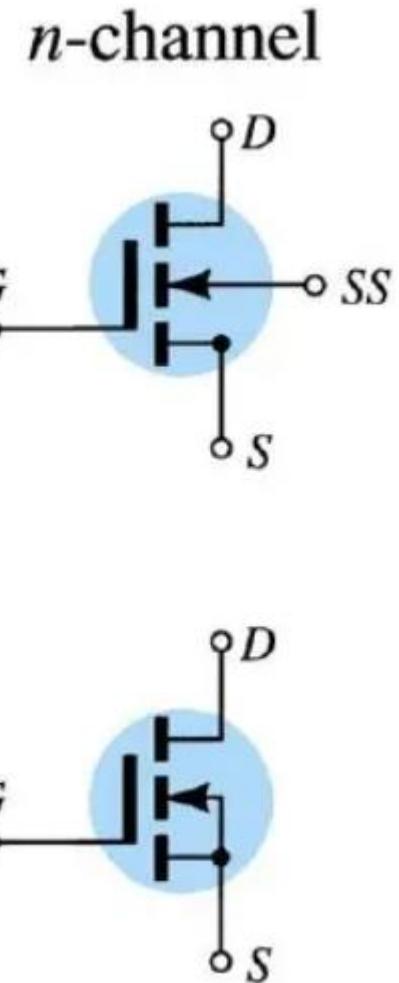
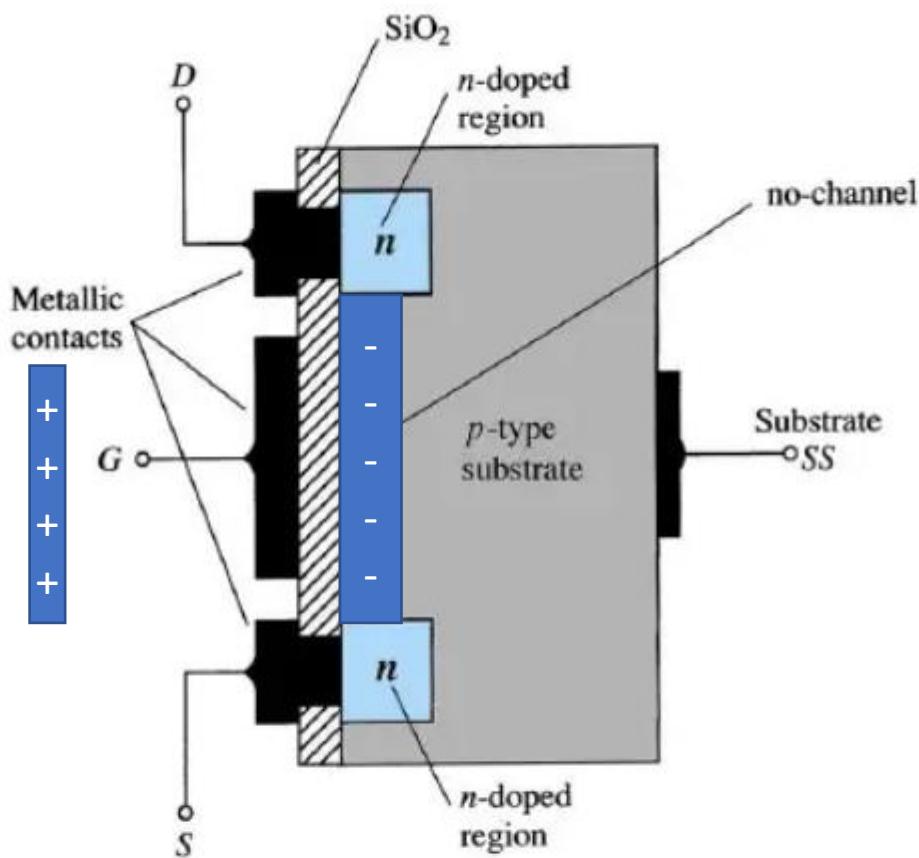


Enhancement Mode operation

In this mode, the transistor operates with $V_{GS} > 0\text{V}$, and I_D increases above I_{DSS} . Shockley's equation, the formula used to plot the Transfer Curve, still applies but V_{GS} is positive:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Enhancement Mode MOSFET Construction



The Drain (D) and Source (S) connect to the n-doped regions

These n-doped regions are not connected via an n-channel without an external voltage

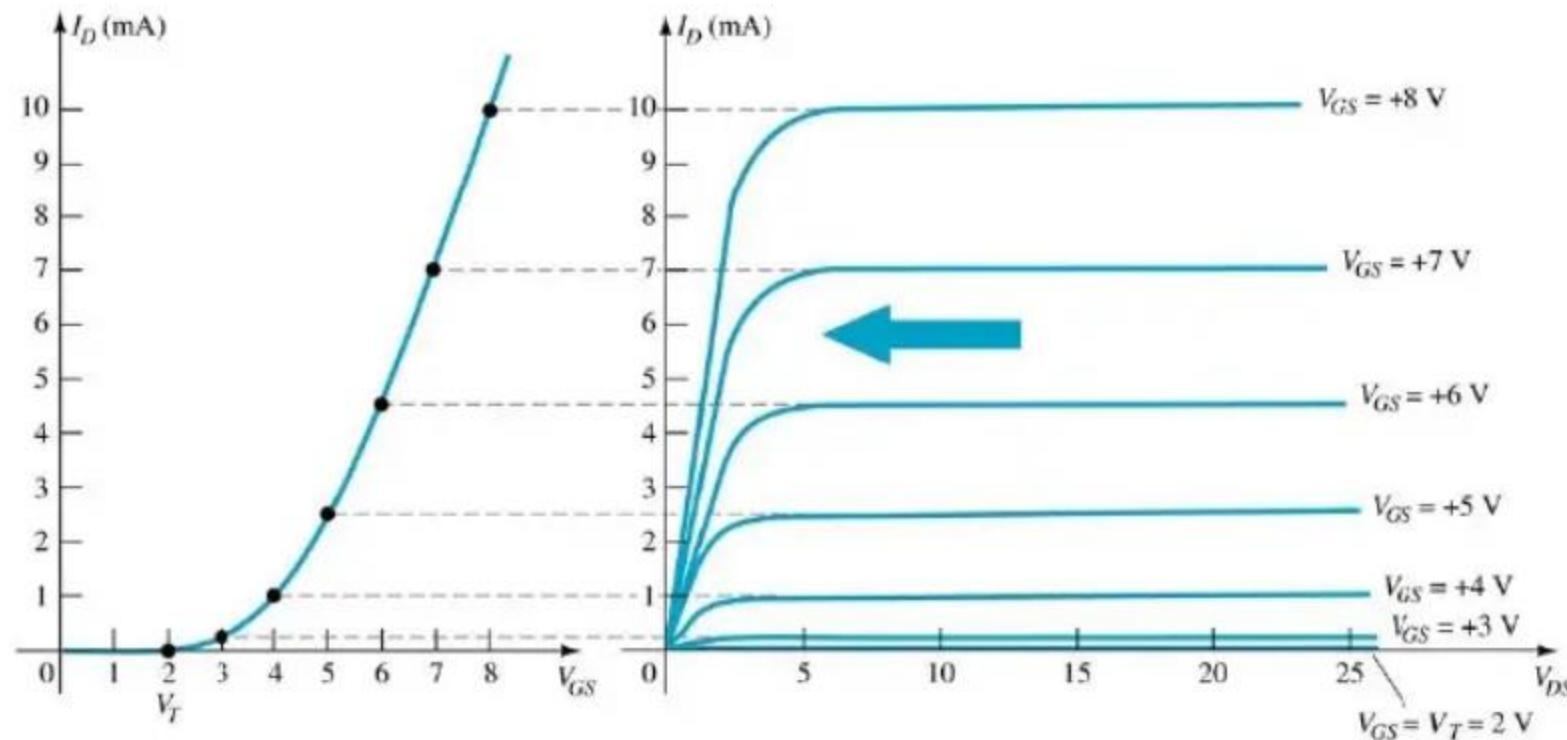
The Gate (G) connects to the p-doped substrate via a thin insulating layer of SiO_2

The n-doped material lies on a p-doped substrate that may have an additional terminal connection called SS

Cont.

Basic Operation

The Enhancement mode MOSFET only operates in the enhancement mode.



V_{GS} is always positive

$I_{DSS} = 0$ when $V_{GS} < V_T$

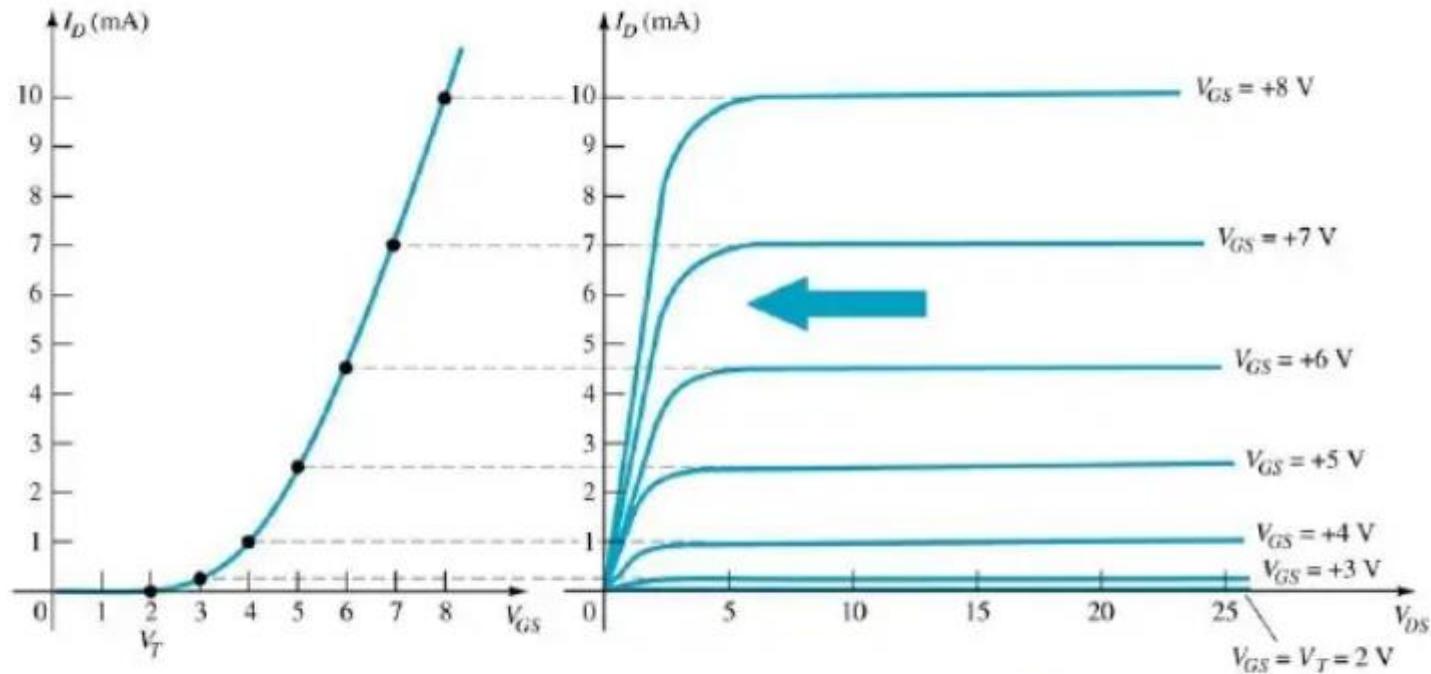
As V_{GS} increases above V_T , I_D increases

If V_{GS} is kept constant and V_{DS} is increased, then I_D saturates (I_{DSS})

The saturation level, V_{DSsat} is reached.

Cont.

Transfer Curve



To determine I_D given V_{GS} : $I_D = k (V_{GS} - V_T)^2$

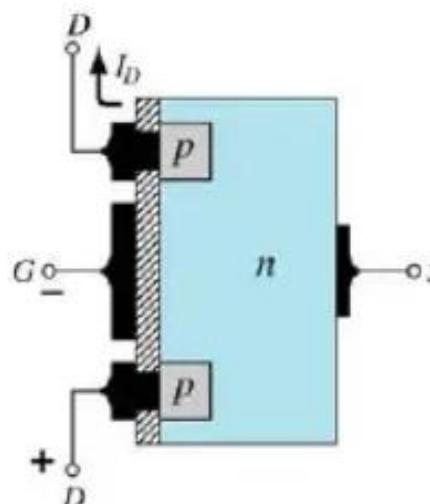
where V_T = threshold voltage or voltage at which the MOSFET turns on.

k = constant found in the specification sheet

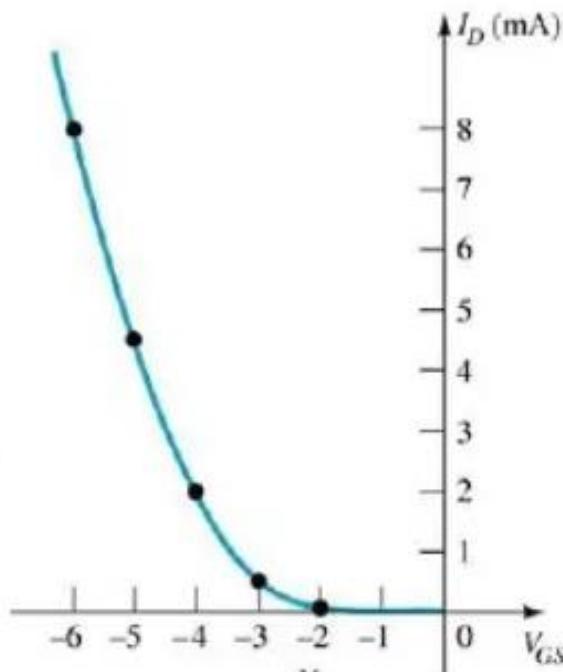
$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

p-Channel Enhancement Mode MOSFETs

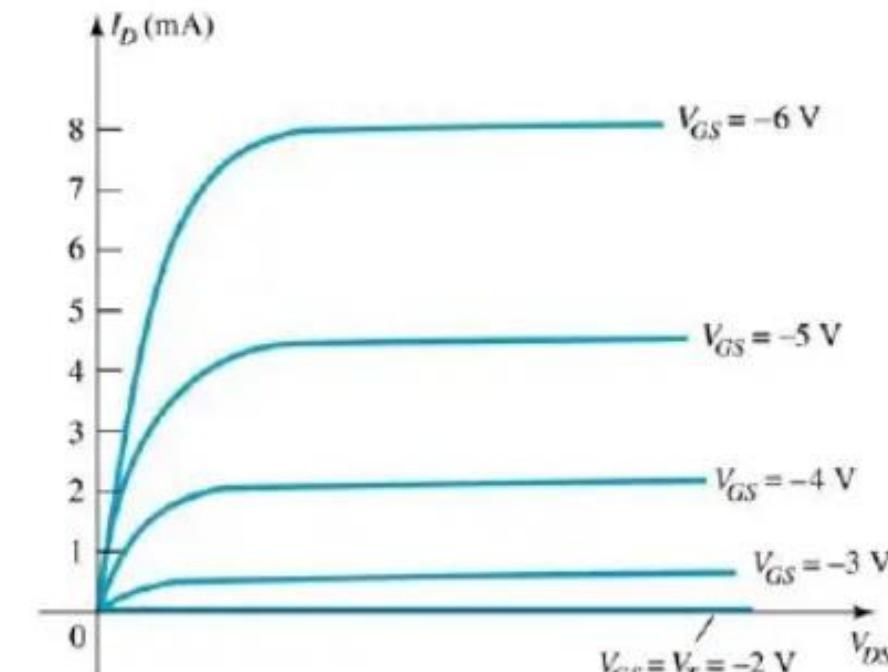
The p-channel Enhancement mode MOSFET is similar to the n-channel except that the voltage polarities and current directions are reversed.



(a)



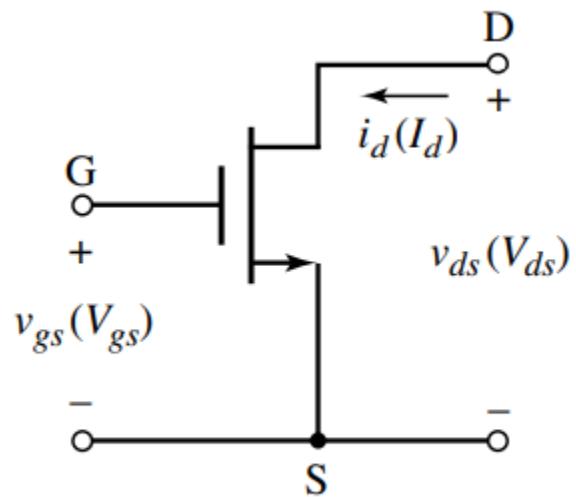
(b)



(c)

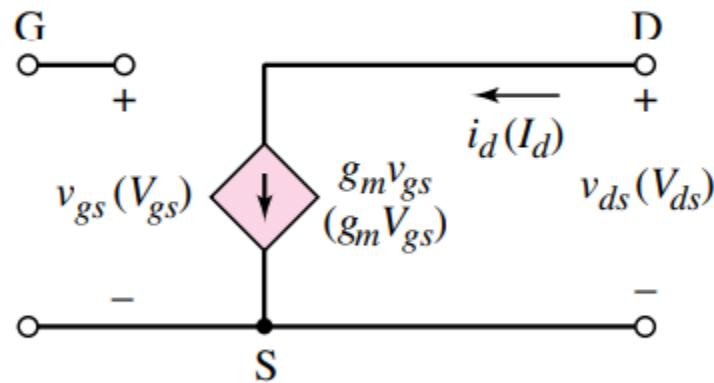
FET Amplifier

Small Signal Equivalent Circuit



The instantaneous drain current

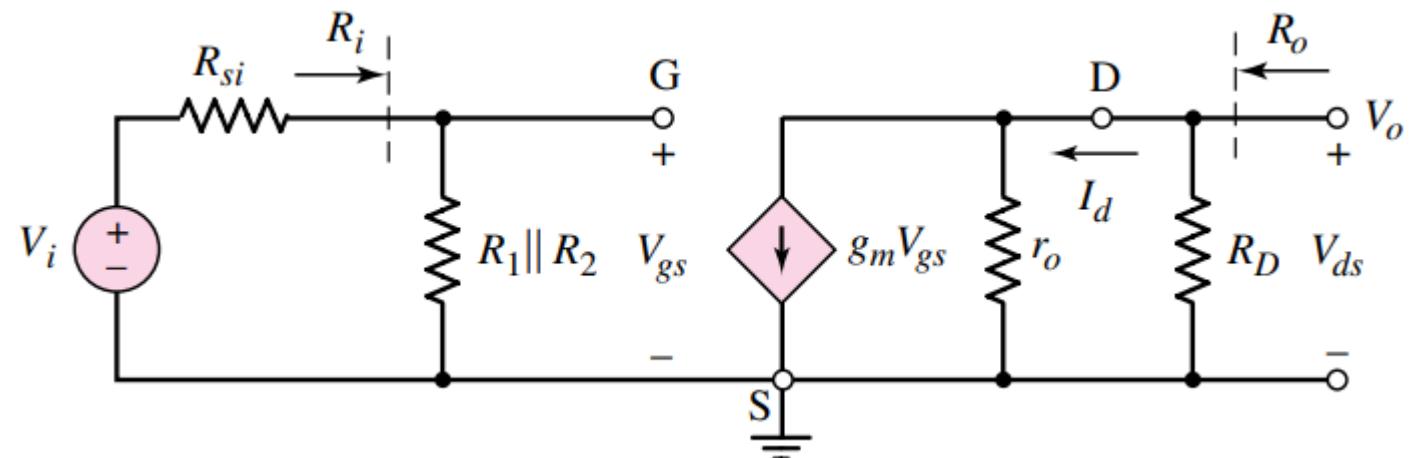
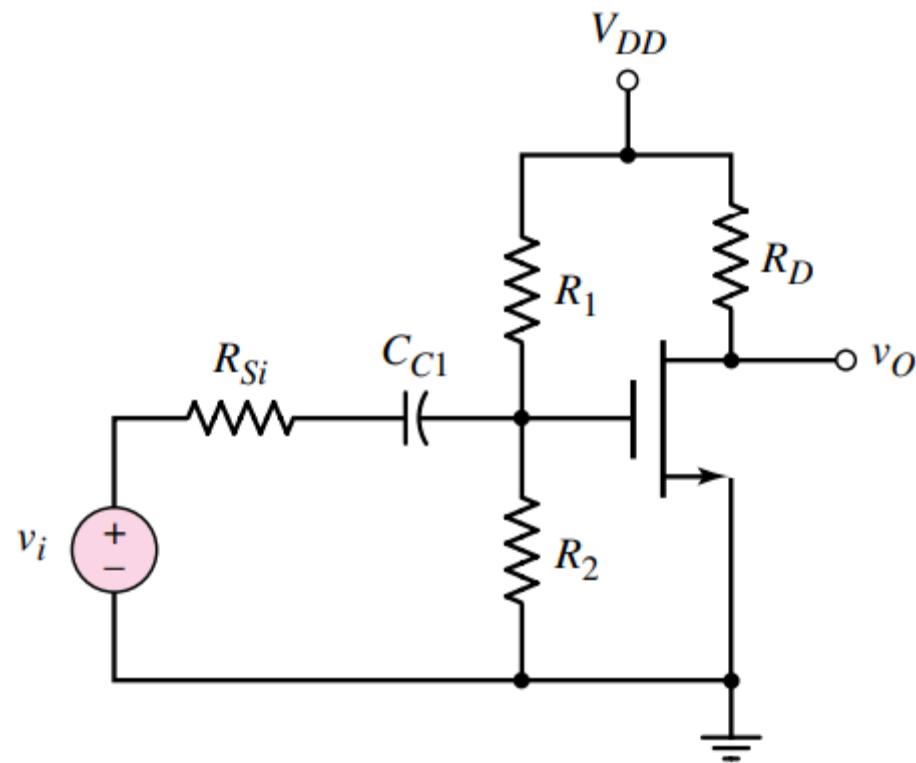
$$i_D = K_n(v_{GS} - V_{TN})^2$$



The small-signal drain current is related to the small-signal gate-to-source voltage by the transconductance g_m . The relationship is

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \Big|_{v_{GS}=V_{GSQ}=\text{const.}} = 2K_n(V_{GSQ} - V_{TN})$$

Common Source Amplifier for nMOS



Cont.

Voltage Gain

The output voltage is

$$V_o = -g_m V_{gs} (r_o \parallel R_D)$$

The input gate-to-source voltage is

$$V_{gs} = \left(\frac{R_i}{R_i + R_{Si}} \right) \cdot V_i$$

Input Resistance

so the small-signal voltage gain is

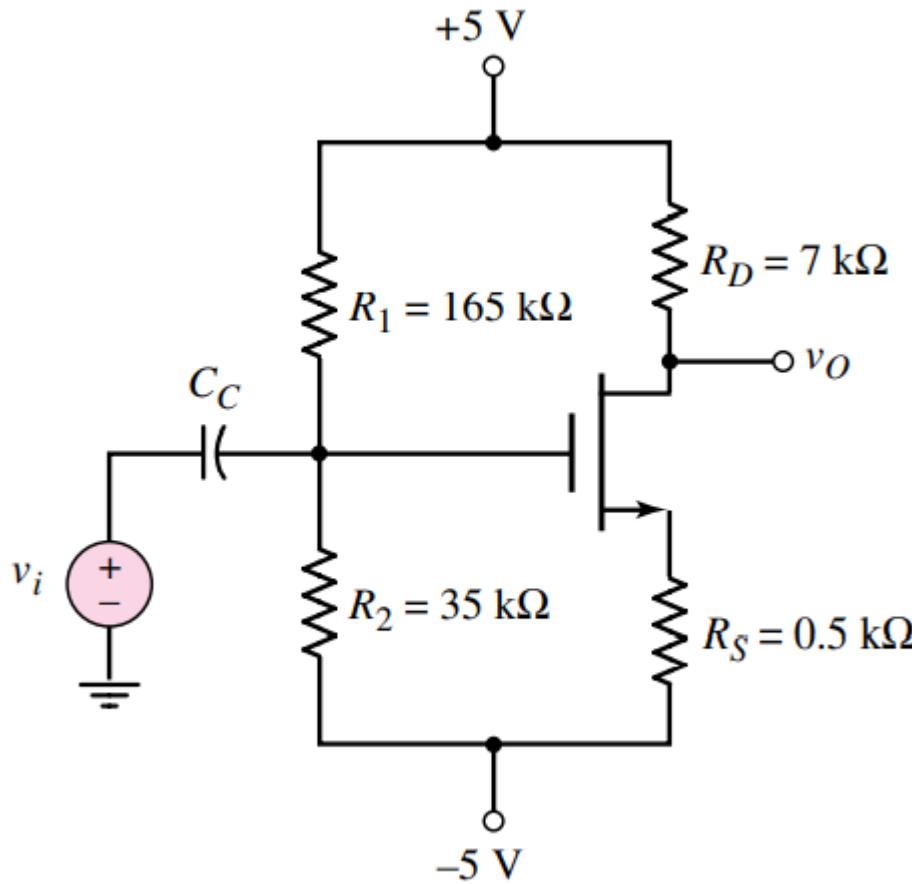
The input resistance to the amplifier is $R_{is} = R_1 \parallel R_2$.

$$A_v = \frac{V_o}{V_i} = -g_m (r_o \parallel R_D) \cdot \left(\frac{R_i}{R_i + R_{Si}} \right)$$

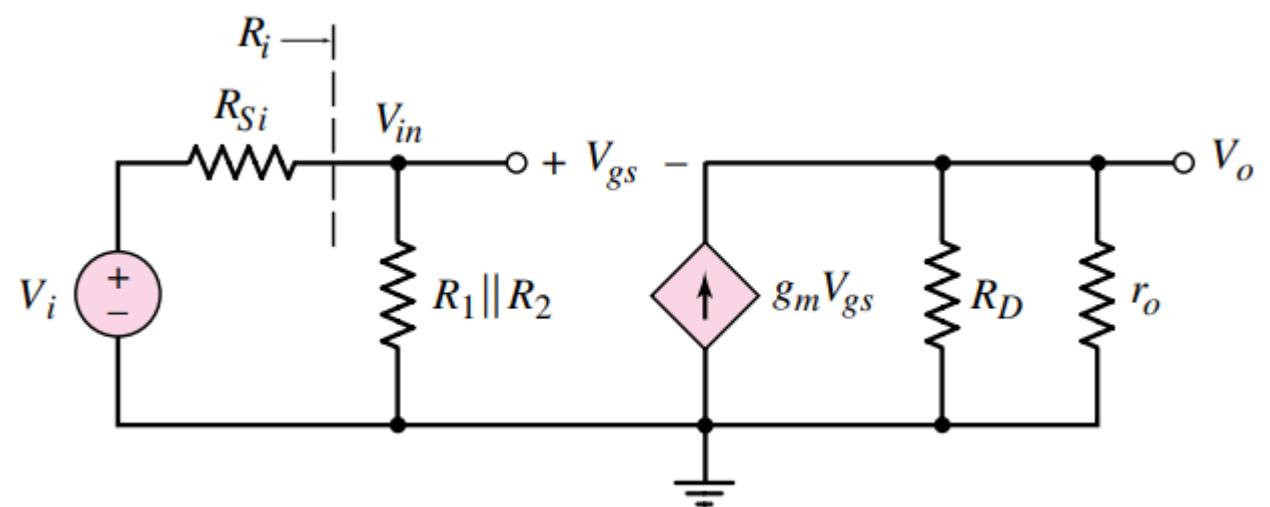
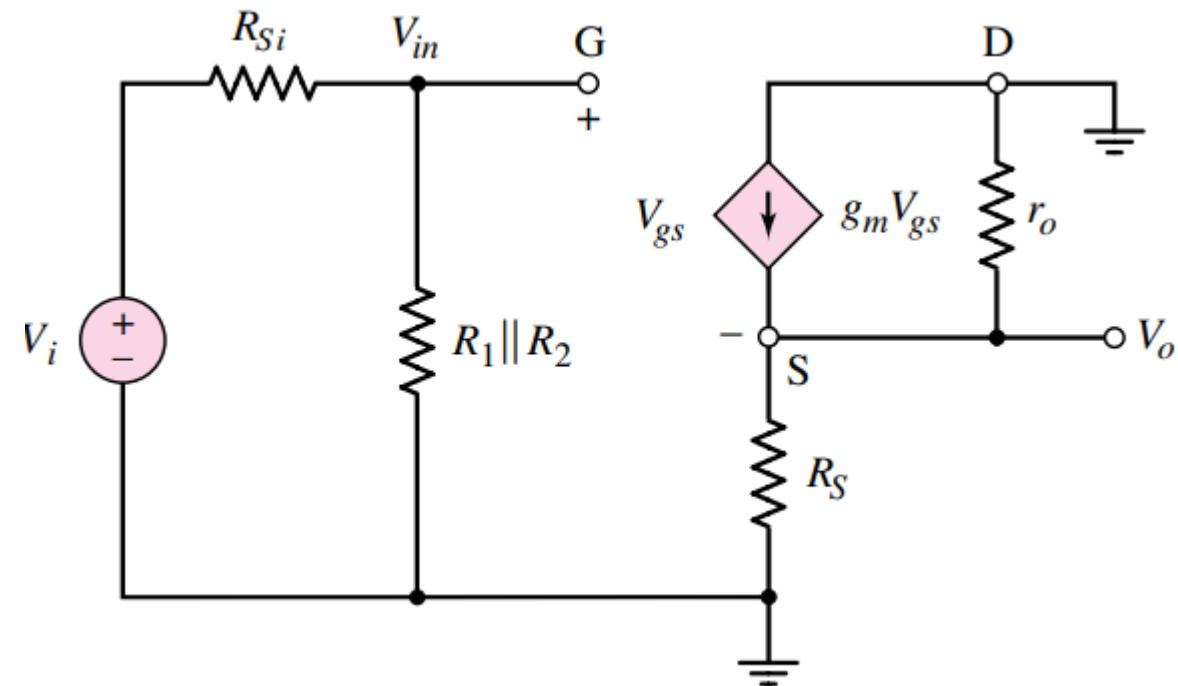
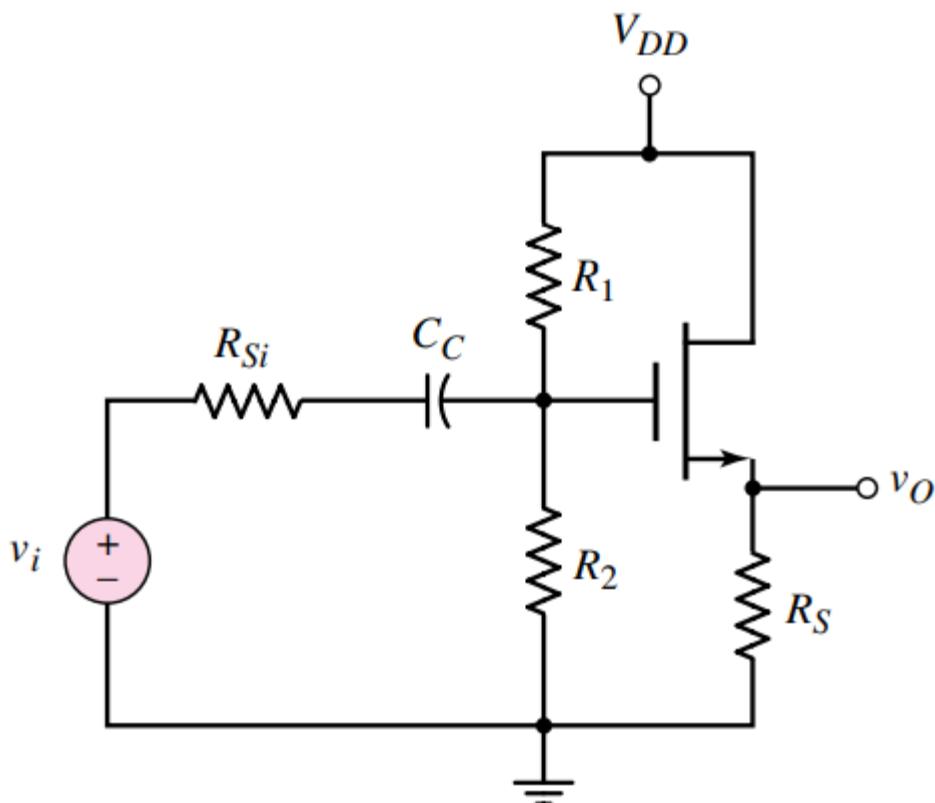
Output Resistance

resistance looking back into the output terminals is found by setting the independent input source V_i equal to zero, which means that $V_{gs} = 0$. The output resistance is therefore $R_o = R_D \parallel r_o$.

Common-Source Amplifier with Source Resistor



Common Drain Amplifier (Source Follower)



Cont.

Voltage Gain

The output voltage is

$$V_o = (g_m V_{gs})(R_s \| r_o)$$

Writing a KCL equation from input to output results in the following:

$$V_{in} = V_{gs} + V_o = V_{gs} + g_m V_{gs}(R_s \| r_o)$$

Therefore, the gate-to-source voltage is

$$v_{gs} = \frac{V_{in}}{1 + g_m(R_s \| r_o)} = \left[\frac{\frac{1}{g_m}}{\frac{1}{g_m} + (R_s \| r_o)} \right] \cdot V_{in}$$

Cont.

More accurately, the effective resistance looking into the source terminal (ignoring r_o) is $1/g_m$. The voltage V_{in} is related to the source input voltage V_i by

$$V_{\text{in}} = \left(\frac{R_i}{R_i + R_{Si}} \right) \cdot V_i$$

where $R_i = R_1 \parallel R_2$ is the input resistance to the amplifier.

$$A_v = \frac{V_o}{V_i} = \frac{g_m(R_S \parallel r_o)}{1 + g_m(R_S \parallel r_o)} \cdot \left(\frac{R_i}{R_i + R_{Si}} \right)$$

or

$$A_v = \frac{R_s \parallel r_o}{\frac{1}{g_m} + R_s \parallel r_o} \cdot \left(\frac{R_i}{R_i + R_{Si}} \right)$$