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Roll No.....049

...(IT/SE)

FOURTH SEMESTER

MID SEMESTER EXAMINATION Roll No..2015/Co/049

EC 262 DIGITAL ELECTRONICS B.Tech (CO /IT/SE)

TIME: 1.5 Hrs. MARCH-2017

Note:- All questions are compulsory. Max. Marks: 30

Assume suitable missing data, if any.

Q1. Write short notes on the following with reference to the various logic families: [1.5*4]

a. Noise Margin
b. Fan Out
c. Power Dissipation
d. Figure of Merit

Q2. Explain the operation of the TTL NAND gate with totem pole output. [4]

Q3. (i). Implement the Full Adder circuit with the help of minimum number of NAND gates [4]

(ii). Implement the Half Adder using CMOS logic family. [2]

Q4. (i). Express the following in the minimized sum of products form: [2*2]

a. $F(A,B,C,D)=\sum(0,2,6,11,13,14)$
b. $F(A,B,C)=\prod(0,3,6,7)$

(ii). Convert the following to the other canonical form [1*2]

a. $F(A,B,C,D)=\prod(0,1,2,3,4,6,12)$
b. $F(A,B,C)=\sum(1,3,7)$

Q5. (i). Convert the following numbers into their equivalent decimal numbers: [1*2]

a. $(6327.4051)_8$
b. $(B6.5)_{16}$

(ii). Represent following decimal numbers in two's compliment form [1*2]

a. -11
b. ±25

(iii). Perform the following arithmetic operations using two's complement method [2*2]

a. $4-7$
b. $-5-4$