DTU/2K15/CO/

Total no. of pages:02

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FOURTH SEMESTER **B.Tech (CO /IT/SE)**

END SEMESTER EXAMINATION **MAY-2017**

EC 262 DIGITAL ELECTRONICS

TIME: 3 Hrs. **Maximum Marks: 40**

Note:- Attempt total five questions out of the following questions, Q1. is compulsory.
Assume suitable missing data, if any.

Q1. Write short notes on the following with reference to the various logic families: **[2*4]**

a. Volatile and Non-volatile memory.
b. Different types of ROM.
c. Flash type Analog to Digital Converter.
d. Difference between latches and flip-flops.

Q2. (i). Design a Gray to BCD converter using one 1:16 demultiplexer with complemented outputs and NAND gates. **[4]**

(ii). Explain the working of a 4 bit R-2R ladder type Digital to Analog Converter with suitable example. **[4]**

Q3. *(i).* Design a combinational circuit that generates the 9's complement of a BCD digit. **[4]**

(ii). Realize $F(A,B,C,D)=\prod(0,1,3,7,9,10,11,13,14,15)$ using: **[4]**

a. 4 to 16 line decoder with complemented outputs and AND gates.
b. 4 : 1 Multiplexer

Q4. (i). Implement the BCD counter using JK flip-flop. **[4]**

(ii). Explain the working principle of the Master Slave flip-flop with suitable diagram. **[4]**

Q5. (i). Find the equivalent analog output, for the circuit shown in Fig.5(i), if digital input is 1101 and the reference voltage for logic 1 is 5Volts. **[4]**

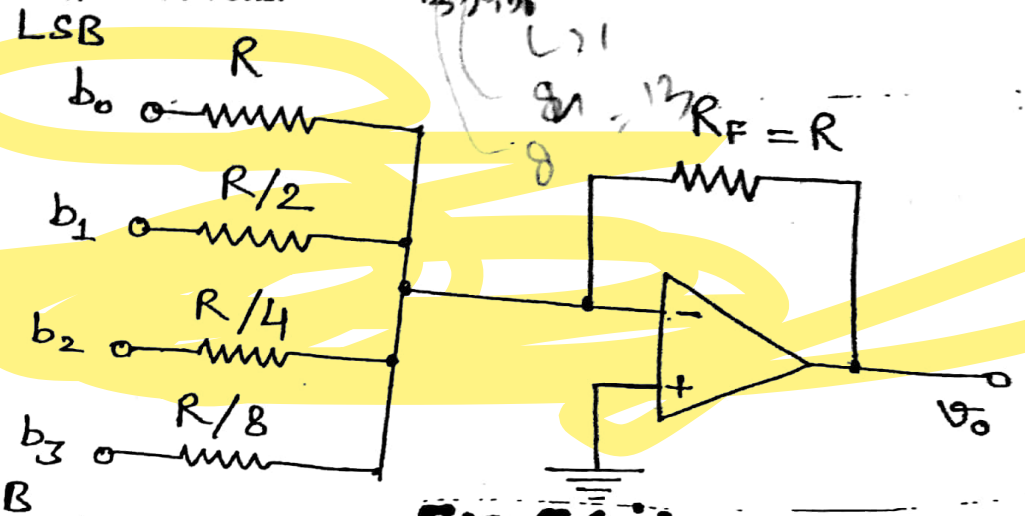

Fig-5(i)

(ii). Assuming that all flip-flops are in reset condition initially, for the circuit shown in Fig.5(ii), find the count sequence observed at Q_A till the seventh clock pulse. **[4]**