

## MID TERM EXAMINATION

Sept-2019

## EC-201 ANALOG ELECTRONICS-I

Time: 1:30 Hours

Max. Marks : 20

Note: Answer all questions. Assume suitable missing data, if any. All abbreviations have their usual meaning.

Unless otherwise stated, use:  $kT/q = 25 \text{ mV}$  at room temperature (300K),  $n_i = 1.5 \times 10^{10} / \text{cm}^3$  for silicon at room temperature and  $\epsilon_{Si} = 10^{-12} \text{ F/cm}$ , Si has  $5.0 \times 10^{22} \text{ atoms/cm}^3$ ,  $\mu_n = 1500 \text{ cm}^2/\text{V-s}$ .

- Q1. [a] Determine the current flowing through  $4 \text{ k}\Omega$  resistor and the voltage drop across points A and B in the circuit shown in Fig.1. Assume that the diode is represented by  $V_F = 0.7\text{V}$  and  $R_F = 0$ . 2

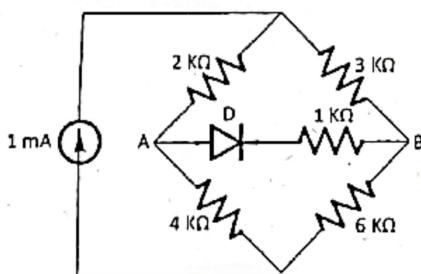


Fig. 1

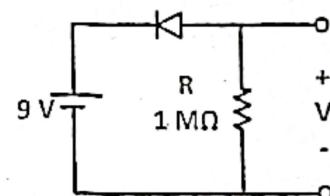


Fig. 2

- [b] For the circuit shown in Fig.2 if  $V=1 \text{ V}$  at  $20^\circ \text{C}$  find the value of  $V$  at  $40^\circ \text{C}$ . 2

- Q2. [a] You are given a step graded pn junction diode with heavily doped n-type region as compared to p-type region. The junction area is given as  $10^{-4} \text{ cm}^2$ . You have access to a capacitance-voltage measurement system and have measured following data:

V	C
-1.0 V	0.68 pF
0 V	1 pF

Using the measured data calculate the built-in potential for this diode  
and the depletion width at thermal equilibrium.

2

[b] If in a Si substrate donor type impurity is added to the extent of  
1 part in  $10^8$  Si atoms, find the resistivity of the doped Si.

2

Q. 3. For the circuit shown in Fig.3 assume  $V_F = 0.7$  V and  $R_F = 0$  for the  
diode.

2

[a] Obtain the voltage transfer characteristic;

2

[b] Plot the output voltage for  $V_s = 10 \sin \omega t$ .

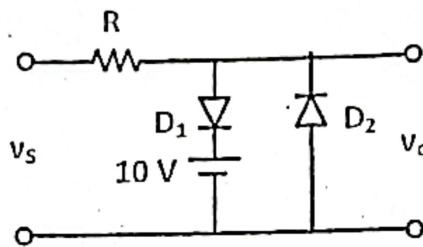


Fig.3

Q. 4. [a] Design a diode clamper circuit to negatively clamp a 20V peak to  
peak ( $V_{pp}$ ) symmetrical square wave at 4 V. Determine the average  
value of the clamped output.

2

[b] A Zener regulator is required to maintain the load voltage at 12V  
for all load currents between 0 and 200 mA. The unregulated source  
voltage ( $V_s$ ) is 16V and the Zener diode provides regulation for  
 $I_Z > 0$ . Calculate the source resistance ( $R_s$ ) needed and the power  
dissipation rating of Zener diode.

2

Q. 5. A full wave center tapped rectifier is to be designed to provide an  
average output of 20V when driven by 220V, 50 Hz AC mains.  
Select a suitable transformer turns ratio and load resistance ( $R_L$ ) so  
that the peak current ( $I_m$ ) does not exceed 31 mA. Draw the voltage  
wave forms across the diodes and also determine the RMS value  
of AC component of the load current.

4

Total No. of Pages 2

Roll No. ....

THIRD SEMESTER

B.Tech. [EC]

MID TERM EXAMINATION

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1. [a] For a step graded p-n junction the doping concentrations on p and n- side are  $1.98 \times 10^{17}$  and  $2 \times 10^{15}$  respectively. The p-n junction is reverse biased and total depletion width is  $5\mu\text{m}$ . Determine the depletion width on p-side. 2

- [b] In the circuit shown in Fig. 1 design the value of  $R_1$  such that this carries a current of  $0.5\text{mA}$ . Assume  $I_s=5 \times 10^{-16} \text{ A}$  for each diode. 3

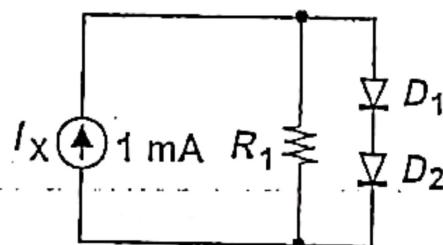


Fig.1

2. [a] A 7.2 V Zener diode is used in the circuit shown in Fig. 2. The load current is to vary from  $12\text{mA}$  to  $100 \text{ mA}$ . Find the value of series resistance R to maintain a voltage of  $7.2\text{V}$  across the load. The input voltage is constant at  $20\text{V}$  and the minimum Zener current is  $10 \text{ mA}$ . 2

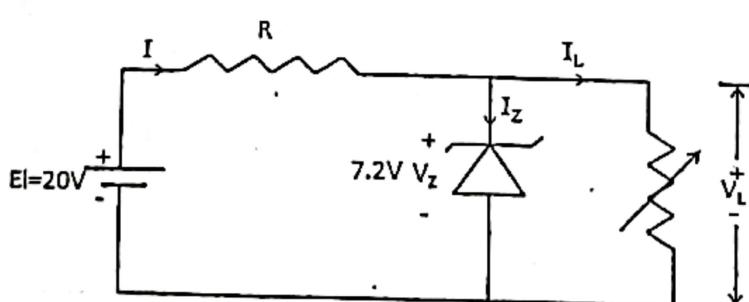


Fig. 2

P.T.O

[b] An LC tank circuit, where the tank capacitance is realized using a reverse biased p-n junction, resonates at 2GHz at a reverse voltage of 0 V. If the doping densities are  $N_A=2\times 10^{18}/\text{cm}^3$  and  $N_D=6\times 10^{12}/\text{cm}^3$  respectively and the junction area is  $2000\mu\text{m}^2$ , calculate the change in resonance frequency while reverse voltage goes from 0 to 3V. 3

3. [a] Determine dynamic resistance of a silicon diode having forward bias of 500 mV and reverse saturation current of 1pA at room temperature. 2

[b] Determine the diode currents and the voltage across  $D_2$  for the circuit shown in Fig. 3. Assume  $V_F = 0.7\text{V}$  and  $R_F = 0$  for both the diodes. 3

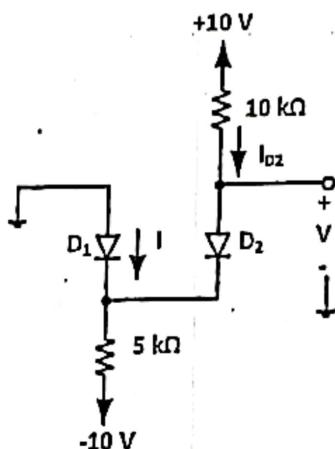


Fig.3

4. [a] For the circuit shown in Fig. 4 if the applied input voltage is represented as  $v_i = 10 \sin \omega t$ , draw the output voltage wave form ( $V_o$ ) and calculate the output DC voltage. 2

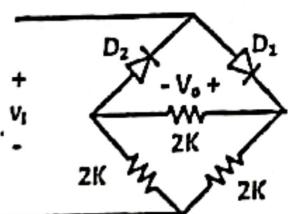


Fig. 4

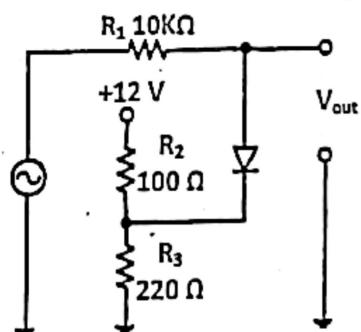


Fig. 5

- [b] For the circuit shown in Fig. 5 obtain the voltage transfer characteristic and plot the output voltage for  $V_i = 10 \sin \omega t$ . Assume  $V_F = 0.7\text{V}$  and  $R_F = 0$  for the diode. 3

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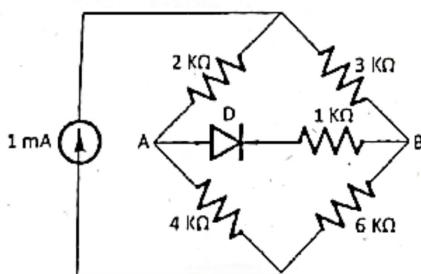


Fig. 1

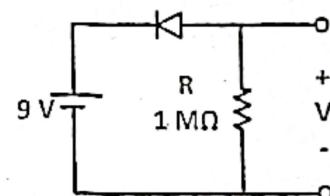


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- [b] For the circuit shown in Fig.2 if  $V=1 \text{ V}$  at  $20^\circ \text{C}$  find the value of  $V$  at  $40^\circ \text{C}$ . 2

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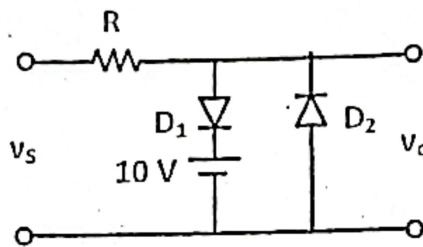


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of AC component of the load current.

4

## THIRD SEMESTER

B.Tech.(SE)

MID SEMESTER EXAMINATION

SEPTEMBER-2010

## SW- 202 ANALOG ELECTRONICS

Time: 1 Hour 30 Minutes

Max. Marks : 20

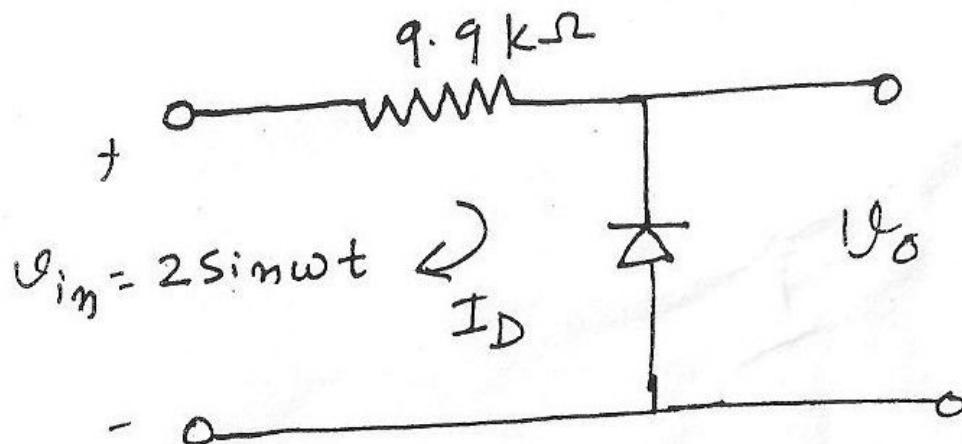
Note : Answer **ALL** questions.

Assume suitable missing data, if any.

1 [a] Explain Mass-Action Law. 1

[b] What is the concentration of holes in silicon crystal having donor concentration of  $1.4 \times 10^{24} /m^3$  when the intrinsic carrier concentration is  $1.4 \times 10^{18}/m^3$ ? Find the ratio of electron to hole concentration. 1.5

2 [a] Explain centre tapped Full-wave rectifier and also explain its merits and demerits. 1.5

[b] A centre-tapped transformer has a 220V primary winding and a secondary winding rated at 12-0-12 V and is used in a full-wave rectifier circuit with a load of  $100\Omega$ . What is the dc output voltage, dc load current and the PIV rating required for diode 1.53 Sketch the transfer characteristics an the output of the circuit shown in Fig.1 Assuming  $V_r = 0.6V$  and  $R_f = 100\Omega$ ,  $R_t = \infty$  2

THIRD SEMESTER

**B.Tech.(EC)**
**END TERM EXAMINATION**      **Nov-2019**  
**EC-201 ANALOG ELECTRONICS-I**

Time:3:00 Hours

Max. Marks : 40

**Note:** Question no.1 is compulsory. Answer any four from the rest.  
 Assume suitable missing data, if any. All abbreviations have their usual meaning.

- 1[a] A clamper circuit using an ideal diode is supplied with a sine wave of 10 V rms. What is the average value of resulting output? 2
- [b] For the circuit shown in Fig. 1 both the diodes are identical conducting 10 mA at 0.7 V and 100 mA at 0.8 V. Find the value of R for which  $V = 50 \text{ mV}$ . 2
- [c] Draw small signal model of the circuit shown in Fig.2 and derive expression for voltage gain  $V_o/V_{in}$ . 2
- [d] "For small  $V_{DS}$  an enhancement MOSFET behaves as a linear resistor" is a qualitative statement. Derive a quantitative expression for the "small  $V_{DS}$ ". 2

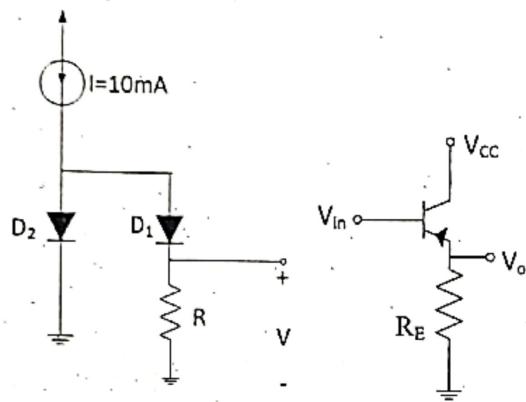


Fig. 1

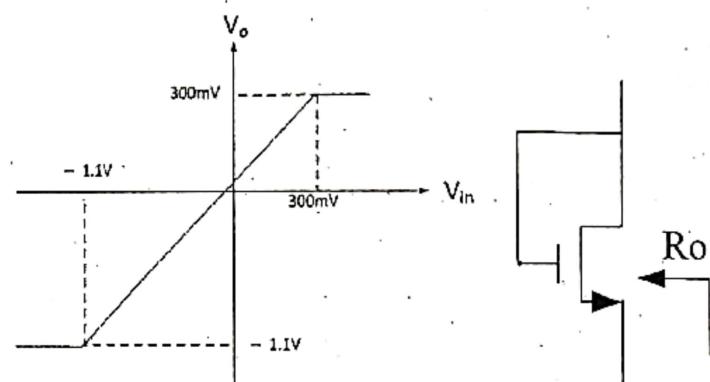


Fig. 2

Fig. 3

Fig. 4

- 2 [a] Design a two way shunt clipper having transfer characteristics as shown in Fig.3. Assume the diodes to be represented by a constant voltage model of  $V_\gamma = 0.7\text{V}$  and  $R_F=0$ . 3

- [b] Draw Ebers Moll model for pnp transistor and derive equation which explains the output characteristics of CB configuration. 3

- [c] If the gate and the drain of a MOSFET are tied together a two terminal device results as shown in Fig4. Determine the small signal resistance  $R_0$  of the device. 2

- 3 Draw the small signal model of a CC-CC multistage amplifier and hence determine its

- [a] voltage ( $A_v$ ) and current ( $A_i$ ) gains  
 [b] input ( $R_i$ ) and output ( $R_o$ ) resistances

4

4

4[a] The circuit shown in Fig. 5 provides constant current of  $I_0$  as long as the circuit to which collector is connected maintains the BJT in active region. Show that under active region operation the  $I_0$  is given by

$$I_0 = \alpha_F \frac{V_{CC} [R_2 / (R_1 + R_2)] - V_{BE}}{R_E + [R_1 || R_2] / (\beta_F + 1)}$$

4

[b] For the circuit of Fig. 6 measurement indicates  $V_B = -1.5$  V. Assuming  $V_{BE} = 0.7$  V calculate the values of  $V_E$ ,  $\alpha_F$ ,  $\beta_F$  and  $V_C$ .

4

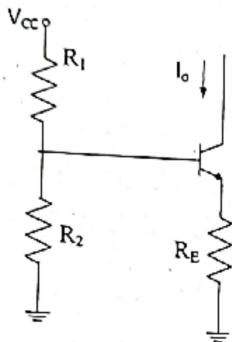


Fig. 5

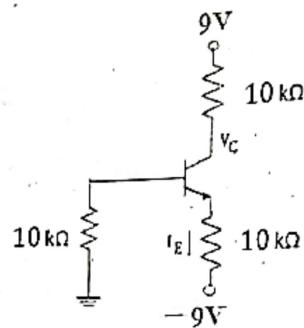


Fig. 6

5[a] Design the circuit of Fig. 7 so that the drain current of NMOS is 100  $\mu$ A if  $\mu_n C_{ox} = 100 \mu\text{A/V}^2$ ,  $V_t = 0.5$  V,  $\lambda = 0$  and  $W/L = 5\mu\text{m}/0.18\mu\text{m}$ .

4

[b] Draw the small signal model of the circuit of Fig. 7 and determine the voltage gain for the amplifier configuration when a small signal is applied at the gate and output is obtained from the drain terminal. Also enumerate the output resistance.

4

6[a] For the circuit shown in Fig. 8 determine the value of  $I_{C2}$  if the  $I_{ref}$  is given as 0.2 mA and  $A_E$  represents the area of unit transistor.

4

[b] What is channel length modulation? How would you determine the value of  $\lambda$  from the drain characteristics of an MOSFET?

4

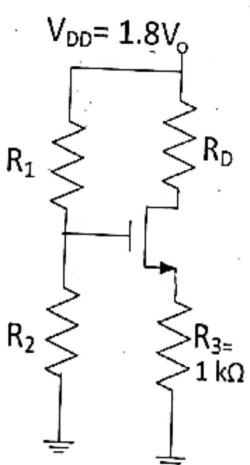


Fig. 7

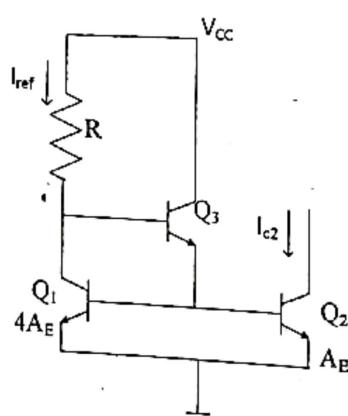


Fig. 8

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THIRD SEMESTER

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Roll No. .....

B.Tech. [COE/SE]

END TERM EXAMINATION

Nov-2018

COE/SE IT -261 ANALOG ELECTRONICS

Time: 3:00 Hours

Max. Marks : 40

Note : Question number 1 is compulsory. Answer any Four questions from the rest. Assume suitable missing data, if any. All abbreviations have their usual meaning.

Q1. (a) In a BJT what factors are responsible for shift of operating point? 2

(b) For a voltage amplifier what are the ideal values of input and output resistances respectively? Give justification. 2

(c) Justify that a JFET can be used as voltage variable resistor and give the expression for resistance. 2

(d) A negative feedback amplifier has a closed loop gain  $A_F = 100$  and an open loop gain  $A = 10^5$ . What is the feedback factor  $\beta$ ? If a manufacturing error results in reduction of  $A$  to  $10^3$  what closed loop gain results? 2

Q2.(a) Draw the input characteristics of CB configuration and explain it with the help of Early effect. 3

(b) A BJT has a value of  $\alpha_F = 0.99$  and is placed in a common base configuration. If the load resistance is  $4.5 \text{ k}\Omega$  and the dynamic resistance of the emitter base junction is  $50 \Omega$  find its voltage gain. 5

Q3.(a) Design a noninverting amplifier using op-amp, with a gain of 2. At the maximum output voltage of 10 V the current in the voltage divider circuit is to be  $10 \mu\text{A}$ . 3

(b) Giving circuit of FET base phase shift oscillator derive the condition and frequency of oscillation. 5

P.T.O.

Q4. (a) It is desired to bias an n channel JFET at  $I_D = 0.8\text{mA}$ . Determine the gate to source voltage needed if  $I_{DSS} = 1.65\text{mA}$  and  $V_P = -2\text{V}$  for the JFET. Also determine the transconductance ( $g_m$ ) for the JFET at given bias current. 3

(b) For the circuit shown in Fig. 1 derive expressions for voltage gain, input and output resistances. 2+1+2

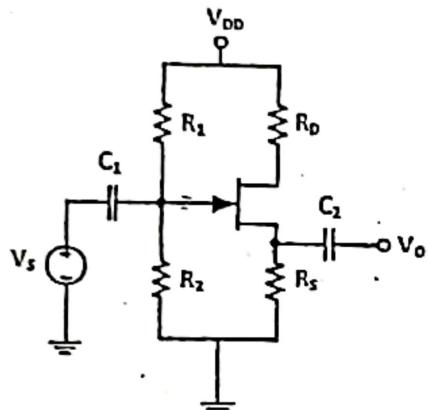


Fig. 1

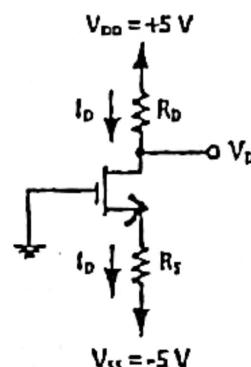


Fig. 2

Q5.(a) For the circuit shown in Fig.2 determine the drain current  $I_D$  and the values of resistance  $R_D$  and  $R_S$  if  $V_D = 1\text{ V}$ ,  $V_{GS} = 3\text{ V}$ ,  $V_t = 2\text{ V}$ ,  $\mu_n C_{ox} = 20\mu\text{A/V}^2$ ,  $L = 10\mu\text{m}$  and  $W = 400\mu\text{m}$ . 3

(b) List the advantages of negative feedback in an amplifier. Deduce the expression for output resistance for a series-series feedback amplifier in terms of output resistance of basic amplifier. 3+2

Q6.(a) Draw load line of a BJT amplifier if  $V_{CC} = 9\text{V}$ ,  $R_C = 1.8\text{ k}\Omega$  and  $R_E = 1.8\text{ k}\Omega$ . Also determine the value of base current at the verge of saturation if  $\beta_F = 10$ . 3

(b) Giving the circuit of an op-amp based adder derive expression for its output voltage. Design this adder circuit to produce an output  $v_o$  as weighted sum of two inputs  $v_1$  and  $v_2$  such that  $v_o = -(v_1 + 5v_2)$ . Choose the resistance values such that for a maximum output voltage of 10 V the current in feedback resistor will not exceed 1mA. (Note: This design problem does not have a unique solution.) 2+3

END

## END SEMESTER EXAMINATION

(Nov-2019)

## CO-202 Analog Electronics

Time: 03 Hours

Max. Marks: 70

**Note:** Answer any five questions.

Assume suitable missing data, if any.

**Q.1 (a)** Derive diode current equation and explain v-i characteristics of pn junction diode using the same equations. (7)

**(b)** A zener voltage regulator has variable load  $R_L$  requiring load current to vary 10mA to 85mA. Given that  $V_Z=10V$ ,  $I_{Z\min} = 15mA$ ,  $I_{Z\max} = 100mA$  and series resistance  $R_S = 40 \text{ ohm}$ . Calculate the range of DC variation permissible and zener power dissipation. (7)

**Q.2 (a)** A single phase full wave centre tapped rectifier having each secondary rms voltage value of 50V and load resistance is 980 ohm. Find (i) mean load current (ii) rms load current (iii) ripple factor and (iv) output efficiency. (7)

**(b)** Define ripple factor and explain its significance. Obtain an expression for the ripple factor of full wave bridge rectifier. (7)

**Q.3 (a)** What do you mean by  $\alpha$ ,  $\beta$  and  $\gamma$ . Derive the expressions for the same for each configuration using PNP transistor to provide the relation in between all these and also mention there significance. (7)

**(b)** A Self bias circuit of NPN transistor is used with  $\beta=50$ ,  $V_{BE} = 0.6V$ ,  $V_{CC} = 18V$  and  $R_C = 4.3K\Omega$ . It is desired to establish a quiescent point at  $I_C = 1.5mA$ ,  $V_{CE}=10V$  and stability factor of  $S \leq 4$ . Find  $R_E$ ,  $R_1$  and  $R_2$ . (7)

**Q.4 (a)** Differentiate in between depletion type and enhancement type MOSFET. Explain the working of n-channel JFET and define the parameters for the same and develop its equivalent circuit. (7)

**(b)** For the common source amplifier given that drain resistance,  $R_D = 5K\Omega$ , amplification factor,  $\mu=50$  and  $r_d = 35K\Omega$ . Evaluate voltage gain  $A_v$  and Output resistance  $R_o$ . (7)

**Q.5 (a)** Explain the concept of Barkhausen criterion of oscillation and RC phase shift oscillator working with the help of suitable diagram. (7)

**(b)** Discuss the concept of feedback in amplifiers and various topologies available. Explain the various advantages of negative feedback with suitable proofs and derivations. (7)

**Q.6 (a)** Explain characteristics and closed loop configurations of an Op-amp with suitable diagrams. (7)

**(b)** List various applications of an Op-amp. Explain op-amp as a v-i and i-v converter. (7)

**Q.7** Write a short note on any two of the following:

- (i) IC555 timer.
- (ii) Biasing and compensation techniques in BJT amplifiers.
- (iii) PLL and function generator.

(7x2 = 14)

Time: 3:00 Hours

Max. Marks : 40

Note: Question no. 1 is compulsory. Answer any four from the rest.  
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1. [a] Calculate the small-signal parameters of a MOSFET biased at a drain current of 0.5mA, if  $\mu_n C_{ox} = 100 \mu A/V^2$ ,  $\lambda = 0.1 V^{-1}$  and  $W/L = 10$ . 4

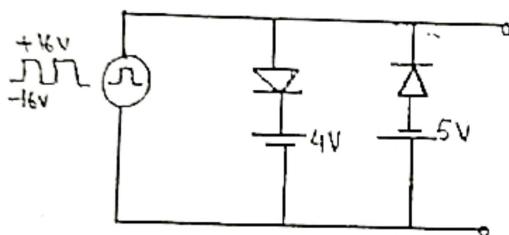


Fig. 1

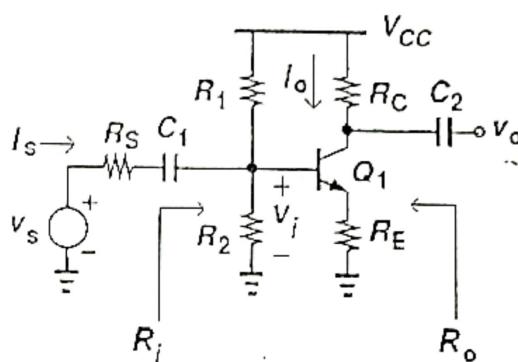


Fig. 2

- [b] Assuming the diodes to be ideal for the circuit shown in Fig.1, obtain and sketch the voltage transfer characteristics and the output voltage waveform. 4

2. For the transistor amplifier shown in Fig. 2 assume  $R_1 = 16 k\Omega$ ,  $R_2 = 9 k\Omega$ ,  $R_C = 1k\Omega$ , and  $R_E = 100 \Omega$ ,  $V_{CC} = 2.5V$  and  $\beta_F = 100$ .

- [a] Determine the Q point and identify the region of operation of transistor. 4

- [b] Derive an expression for input and output resistances of common base amplifier. 4

3. [a] Derive expressions for the voltage gains  $A_{Vs}$  ( $v_o/v_s$ ) and  $A_V$  ( $v_o/v_i$ ); current gain  $A_{Is}$  ( $I_o/I_s$ ), input and output impedances  $R_i$  and  $R_o$  respectively for the amplifier circuit of Fig. 2. 6

- [b] Why should the input impedance of an ideal voltage amplifier be infinity? 2

4. [a] Write Ebers Moll equations for an npn transistor and hence define common base forward short circuit current gain. 3

- [b] Drawing small signal model of a multistage amplifier consisting of CS followed by CD, derive expressions for voltage gains  $A_V$  ( $v_o/v_s$ ) and output resistance ( $R_o$ ) where terms have their usual meaning. 5

5. [a] For the circuit configuration shown in Fig. 3(a), determine the small-signal resistance  $R_X$ . 3

- [b] Compute the value of  $R_1$ ,  $R_2$ ,  $R_S$ ,  $R_D$  and W/L of transistor  $M_1$  in circuit of Fig.3(b) if the circuit is to be designed for a voltage gain of 5 with a power budget of 5mW. Assume  $\mu_n C_{OX} = 100 \mu A/V^2$ ,  $V_{TH} = 0.5V$ ,  $V_{DD} = 1.8V$  and voltage drop across  $R_S$  to be 400mV. 5

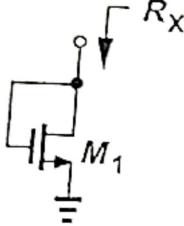


Fig. 3(a)

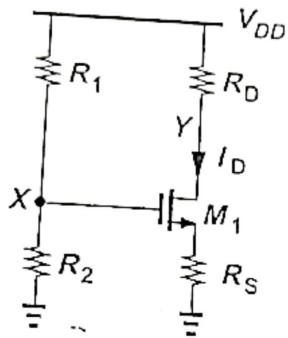


Fig. 3(b)

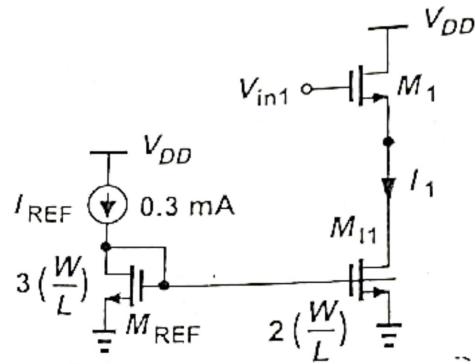


Fig. 4

6. [a] Explain the drain characteristics of an enhancement MOSFET. 5

- [b] For the circuit shown in Fig.4 determine the value of  $I_1$ . 3

THIRD SEMESTER

B.Tech (CO/SE)

SUPPLEMENTARY EXAMINATION

Feb-2018

## CO/SE-202 ANALOG ELECTRONICS

Time: 3:00 Hours

Max. Marks: 70

Note:

1. Attempt any five questions.
2. Assume suitable missing data, if any.

1[a] Explain the following :- (4 x 2 = 8)

- i. Clamping and clipping circuit
- ii. Zener and Avalanche breakdown

[b] Explain frequency response of BJT amplifier with suitable diagram. (6)

2[a] Which is a better input buffer, a BJT or FET, justify (6)

[b] Prove that  $\beta$  is always greater than unity and  $\beta = \frac{\alpha}{1-\alpha}$  (4 + 4)

3[a] [b] Describe the different components of diode current. Explain mechanism of current flow in PN junction. (6)

[b] Draw the Ebers-Moll model of the n-p-n transistor &amp; give the equations for the emitter &amp; collector current. (4 + 4)

4[a] Explain with diagram the input and output characteristics of a diode in CB configuration. (4 + 4)

[b] Find out the Q point for a fixed bias circuit having a silicon transistor with  $\beta = 100$ , supply voltage  $V_{cc} = 6V$ , Collector resistor  $R_c = 3 k\Omega$  and base resistor  $R_b = 530 k\Omega$ . (6)

5[a] Derive the condition for oscillation in a RC phase shift oscillator. Give advantages and disadvantages of it. (6 + 2)

[b] A half wave rectifier supplies a load of  $10 \text{ k}\Omega$ . The AC voltage applied to diode is (300-0-300) volt. If diode resistance is negligible, calculate  
i. RMS value of output current  
ii. Average value of output current (3 + 3)

6[a] How power amplifiers are different than normal amplifiers? What do you understand by class A, B and AB power amplifiers? (8)

[b] What is the linear amplification factor of transistor if its gain is 100? (6)

Time: 3:00 Hours

Max. Marks : 40

Note: Question no. 1 is compulsory. Answer any four from the rest.  
Assume suitable missing data, if any. All abbreviations have their usual meaning.

1. [a] Calculate the small-signal parameters of a MOSFET biased at a drain current of 0.5mA, if  $\mu_n C_{ox} = 100 \mu A/V^2$ ,  $\lambda = 0.1 V^{-1}$  and  $W/L = 10$ . 4

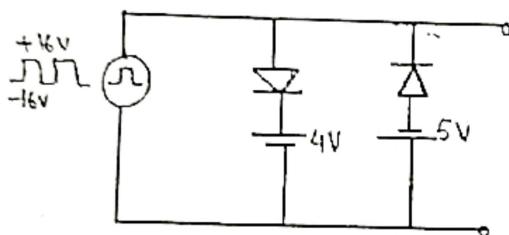


Fig. 1

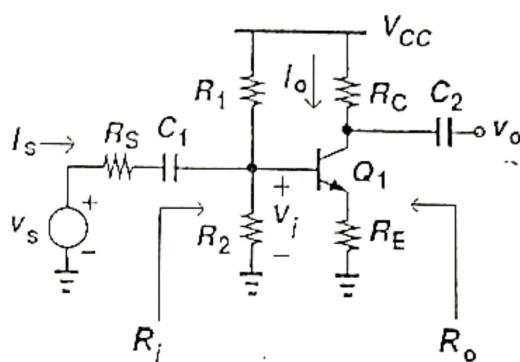


Fig. 2

- [b] Assuming the diodes to be ideal for the circuit shown in Fig.1, obtain and sketch the voltage transfer characteristics and the output voltage waveform. 4

2. For the transistor amplifier shown in Fig. 2 assume  $R_1 = 16 k\Omega$ ,  $R_2 = 9 k\Omega$ ,  $R_C = 1k\Omega$ , and  $R_E = 100 \Omega$ ,  $V_{CC} = 2.5V$  and  $\beta_F = 100$ .

- [a] Determine the Q point and identify the region of operation of transistor. 4

- [b] Derive an expression for input and output resistances of common base amplifier. 4

3. [a] Derive expressions for the voltage gains  $A_{Vs}$  ( $v_o/v_s$ ) and  $A_V$  ( $v_o/v_i$ ); current gain  $A_{Is}$  ( $I_o/I_s$ ), input and output impedances  $R_i$  and  $R_o$  respectively for the amplifier circuit of Fig. 2. 6

- [b] Why should the input impedance of an ideal voltage amplifier be infinity? 2

4. [a] Write Ebers Moll equations for an npn transistor and hence define common base forward short circuit current gain. 3

- [b] Drawing small signal model of a multistage amplifier consisting of CS followed by CD, derive expressions for voltage gains  $A_V$  ( $v_o/v_s$ ) and output resistance ( $R_o$ ) where terms have their usual meaning. 5

5. [a] For the circuit configuration shown in Fig. 3(a), determine the small-signal resistance  $R_X$ . 3

- [b] Compute the value of  $R_1$ ,  $R_2$ ,  $R_S$ ,  $R_D$  and W/L of transistor  $M_1$  in circuit of Fig.3(b) if the circuit is to be designed for a voltage gain of 5 with a power budget of 5mW. Assume  $\mu_n C_{OX} = 100 \mu A/V^2$ ,  $V_{TH} = 0.5V$ ,  $V_{DD} = 1.8V$  and voltage drop across  $R_S$  to be 400mV. 5

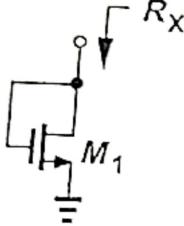


Fig. 3(a)

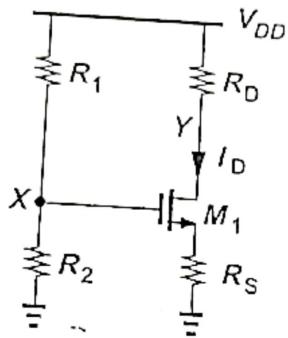


Fig. 3(b)

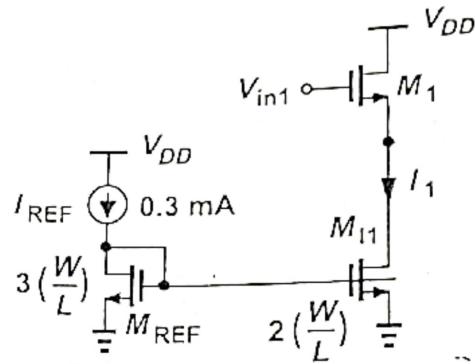


Fig. 4

6. [a] Explain the drain characteristics of an enhancement MOSFET. 5

- [b] For the circuit shown in Fig.4 determine the value of  $I_1$ . 3