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Supplementary Examination **August 2018**

B Tech(COE/IT/SE) –IV Sem

EC-262 Digital Electronics

Max marks:40 Time : 3 hrs

NOTE: Attempt **any Five** questions

Q1 (a) State and prove DeMorgan's theorem. **2**

(b) If function f_1 is given by, $f_1 = (BC + AB' + DA')$, convert this function in Product of Sum form. **2**

(c) What are self-complementing codes? Give at least two examples of self-complementing codes. What is advantage of such codes? **2**

(d) What are the various ways in which negative numbers can be Represented in binary number system? **2**

Q2.(a) Using Quine McClusky method Realize the function F given by

$$F(A,B,C,D) = \sum m(0,1,2,4,9,10,14) + d(3,8)$$ **5**

(b) A and B are two 4-bit inputs for an adder/subtractor circuit whose operation is controlled by M.
If M=0, it acts as 4-bit adder(A+B) and
if M=1 it acts as 4-bit subtractor(A-B).
Design the circuit using a 4-bit adder and additional gates. **3**

Q3.(a) Design a binary full adder circuit using 3-to-8 decoder with active low output and additional gates . **2**

(b) Design a 4-bit look ahead carry adder and explain why it is faster than normal binary adder. **3**

(c) Design a BCD adder using 4-bit binary adders. **3**

P.T.O.

Q4.(a) Convert the negative edge triggered D-flip flop into negative edge triggered J-K flip flop. 3

(b) Design the 3-bit synchronous counter which counts and repeats as per following sequence:

000, 010, 100, 110, 000 5

Q5.(a) What are Programmable Logic Devices? Differentiate between PLA, PAL and ROM. 3

(b) Explain the principle of Dual slope type ADC. 3

(c) A successive approximation type analog to digital converter has a resolution of 8 bits. If the clock rate is 100 KHz what is the maximum rate at which the samples may be converted? 2

Q6. (a) What are the important characteristics/parameters of digital integrated circuits? 2

(b) Draw the circuit for CMOS NAND and NOR gates and explain its operation. Compare the performance of CMOS with TTL and ECL in terms of the speed, power dissipation and packing density. 4

(c) What are the major Considerations while interfacing the ECL circuits with TTL and CMOS circuits in the same digital system? 2

END