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IV SEMESTER B.Tech. [CO]

SUPPLIMENTARY EXAMINATION Aug-2018

Paper Code:CO-206Title of paper: Computer Organization& Architecture

Time: 3:00Hours Max. Marks : 50

Note :Answer any FIVE questions.
Assume suitable missing data, if any.

1 [a] What is Control Unit? Discuss any two methods briefly for implementation of control unit.

[b]Register A holds the 8 bit binary 11011001. Determine the B operand and logic micro operation to be performed in order to change the value in A to
(i) 01101101 (ii) 11111101.

2.(a) Show the step by step multiplication using booth's Algo with suitable example & Draw the flow chart of booth Algo.

(a) What do you mean by instruction cycle and interrupt cycle? Draw the flowchart for instruction Cycle.

3. [a] Differentiate between hardwired and micro-programmed control units

[b]Differentiate between direct and memory address schemes

4. (a)What is biased exponent? Design a block diagram for hardware representation for floating point arithmetic operations and explain it suitable example using biased exponent.

(b) Explain the following terms with suitable examples:
i. External Interrupts ii. CISC Characteristics

iii. Program Interrupts

5. (a)Why are the read & write control lines in a DMA controller bidirectional? Under what conditions and for what purpose are these used as inputs? Under what condition & for what purpose they used as outputs? Explain the operation DMA transfer.

[b] A computer has a memory unit of 64K x 16 and a cache memory of 1 K words.

i. How many bits are there in the tag, index, block and word fields of the address format?

ii. How many bits are there in each word of cache, and how are they divided into functions?

iii. How many blocks can the cache accommodate?

Q.7 Write shorts notes on any four of the followings:

[a] Hit Rate

[b] BCD Subtraction

[d] Daisy-Chaining Priority

[e] Match logic for associative memory

(f) CISC and RISC architectures