

EXPERIMENT MANUAL

FOR

DIGITAL ELECTRONICS BASED EXPERIMENTS



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(DIGITAL ELECTRONICS BASED EXPERIMENTS)

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Note:

- Perform all the experiments using IC Trainer Kits or Bread boards only.
- Minimum of 10 experiments to be conducted.
- One project has to be submitted: To be decided by faculty teaching (Project Report and Practical Demonstration).

EXPERIMENT No.1

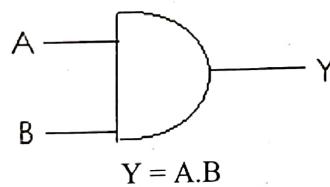
AIM: Familiarization with Digital trainer kit & its associated components.

APPARATUS: Digital trainer kit, its associated components.

THEORY: Logic Gates:

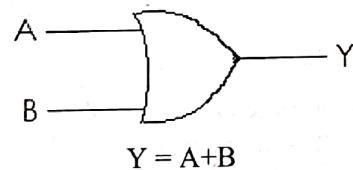
AND GATE:-

It has two inputs and one output. The AND operation is 1 only if all inputs are one Mathematically:
(Suppose A & B are the inputs & Y is the output for all the gates)



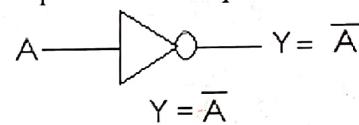
OR GATE:

The OR operation is defined as one of one or more than one input is high; the logical equation for OR is:



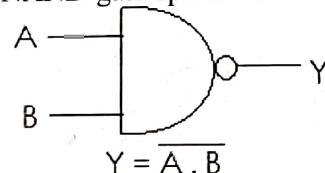
NOT GATE:

It is also called as inverter. It has one input and one output.



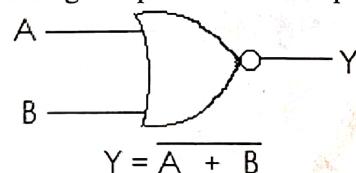
NAND GATE:

The NOT-AND operation is known as NAND-gate operation. The operation is shown by



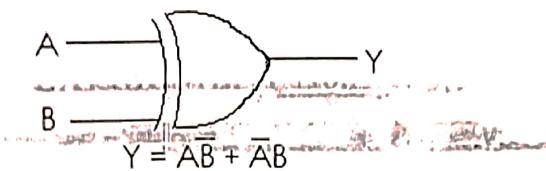
NOR GATE:

The NOT-OR operation is known as NOR gate operation. The equation is



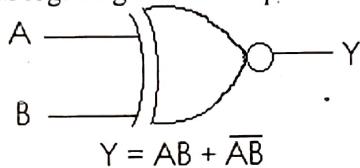
XOR GATE:

The X-OR operation is not a basic operation & can be performed by using other gates.
The operation is



X-NOR GATE:

The gate is also combination of several logical gates. The operation is given as



FLIP-FLOPS:

Edge-triggered flip-flops:

These are synchronous devices. The term synchronous means that the output changes its states only at specified points on the triggering i/p called clock. The term edge triggered means that flip-flop change only at the +ve & -ve edge.

SR-FLIP FLOP:

The S R inputs of SR flip-flops are called synchronous inputs because data on these inputs are transferred & only discrete voltages are used here as logical 0 & 1.

JK- FLIP FLOP:

This is very versatile & widely used flip-flop. The function is identical to that of S-R flip flop is set, reset & no change condition of operation. The difference is that J-K flip flop has no invalid state.

D-FLIP FLOP:

It is useful when 0 signal data list is to be stored. The simple addition of an inverter to an S-R flip flop creates a basic D-flip-flop.

T-FLIP FLOP:

In J-K F/F short circuiting of J –K terminals, resulting in T-flip flop; if T= 1, it acts as a logic switch, if T = C, the output remains same.

IC Tester:

The front panel logout is designed keeping case of operator convenient display & pleasant look in the mind first line of front panel display. It indicates the model, no while second line display is used to interact with user key can broadly be classified into two classes. Key with marking 0,1,2,3,4,5,6,7,8,9 are known as input keys.

CRO:

It is most electrical instrument. This gives visual representation of elec. Quantities. It consist of following major parts:-

1. Cathode rays tube
2. Power supply
3. Time based circuit
4. Deflection voltage.

BCD to 7 SEGMENT DECODER:

A digital display that consists of 7-segment LED's segment is used to display decimal numerals in digital system. In the IC 7447 accepter, the binary i/p & convert it into 0 to 9 numbers.

INTEGRATED CIRCUITS:-

The circuit in which active & passive components such as transistor diode, capacitor, resistor etc. are small pieces port. Semiconductor chips are IC's.

Classification of IC's:

1. Monolithic
2. Thin Film
3. Thick Film
4. Hybrid
5. Digital
6. SSI
7. VLSI

Linear IC's:

Linear IC's process analog signals. These contain several amplifier circuits. The output varies in direct proportion to its input for IC 741. The digital IC's process digital signals & are basically pulse circuit. Hence o/p is not linear with respect to input.

MULTIMETER:

It is an electrical instrument used to measure voltage, current & resistance. So it is called as volt-ohm meter. It consists of ordinary pivot-type moving galvanometer.

EXPERIMENT No. 2

AIM: Study & verification of truth tables of TTL Gates: - AND, OR, NOT, NAND, NOR.

APPARATUS:

Logic Gate Circuit Trainer, IC used 7400, 7402, 7404, 7408, 7432, 7486, connecting wires.

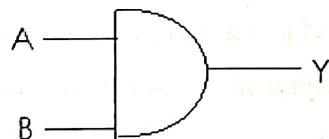
THEORY:

The digital circuit which either allows a signal to pass through or stop it is called gate. Gates which allow a signal to pass through only when some logical conditions are satisfied are called logic gate. Logic gates usually combine one or more logic variables input to produce and output. All of the possible combinations of the input variables and the corresponding outputs are normally listed in a table called a truth table.

The simple logic gates are: (i) AND (ii) OR (iii) NOT.

The compound (Universal) logic gates are (i) NAND (NOT-AND) (ii) NOR (NOT-OR)

AND GATE USING 7408: A circuit which performs an AND operation. It has N Inputs (N=2) and one output. Digital signals applied at the input terminals marked A, B. The o/p is obtained at the o/p terminal marked Y.



| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

TRUTH TABLE

In case of this basic gate output is present only when all the inputs are present. Its logical expression is given by $Y = A \cdot B$

OR GATE USING 7432:

It allows the signal to pass through when even any one of the logical conditions is satisfied.



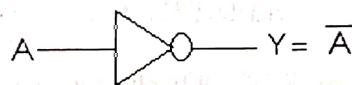
| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

TRUTH TABLE

The GATE in which output is 1 if and only one or more inputs are 1.

Its logical equation is given by $Y = A + B$.

NOT GATE USING 7404: It allows the signal to pass through when the only logical condition is not satisfied it.



| Input | Output |
|-------|--------|
| A | Y |
| 0 | 1 |
| 1 | 0 |

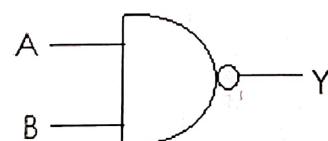
TRUTH TABLE

It is also known as inverter. It has one input (A) and one output (Y).

Its logical equation is $Y = \overline{A}$.

NAND GATE USING 7400: It combines characteristics of a NOT and an AND gate. The NOT-AND operation is known as NAND operation. A bubble on the output side of NAND gate represents NOT operation, inversion or complementation.

Its logical equation is $Y = \overline{A \cdot B}$.

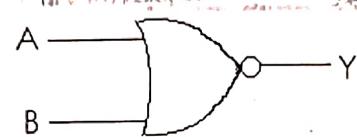


| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

TRUTH TABLE

A NAND gate is a universal gate. It serves as a building block for AND, OR and NOT gates.

NOR GATE USING 7402: It combines characteristics of a NOT and an OR gate. The NOT-OR operation is known as NOR operation.



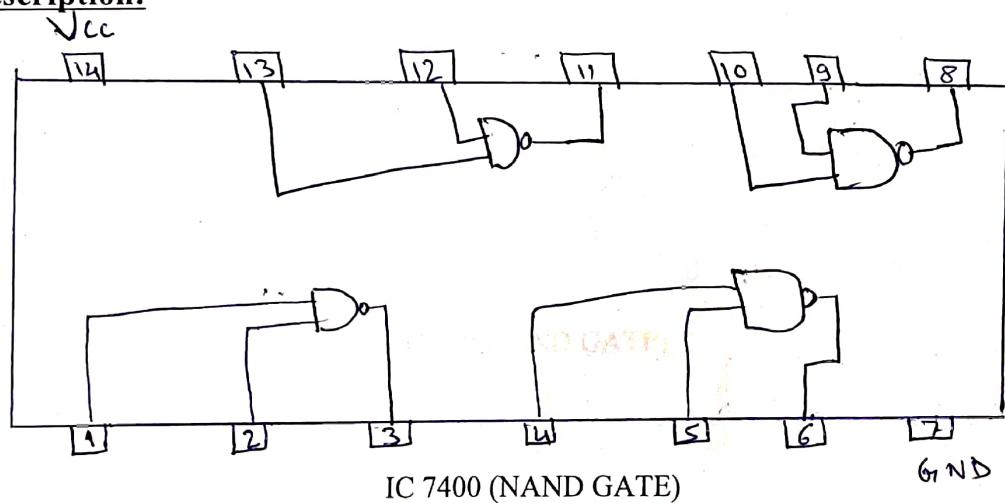
| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

TRUTH TABLE

Similar to NAND gate, a bubble on the output side of the NOR gate represents the NOT operation.

The logic equation is $Y = \overline{A + B}$.

Pin description:



IC 7400 (NAND GATE)

IC 7402 (NOR GATE)

IC 7404 (NOT GATE)

IC 7408 (AND GATE)

IC 7432 (OR GATE)

PROCEDURE:

1. Take the IC's numbered 7408, 7432, 7486.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 3

AIM: To implement all Logic gates using Universal gate IC-7400 (NAND Gate IC).

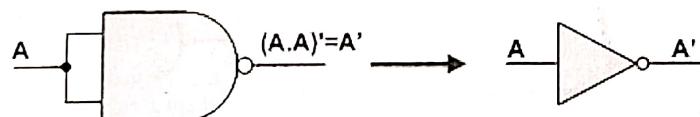
APPARATUS: Digital trainer kit, Logic gate IC 7400., Connecting wires.

THEORY:

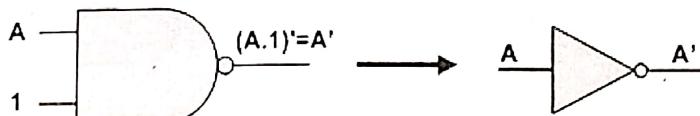
Since NAND gate is universal gate, all other logic gates can be implemented using it.

Implementation using NAND gate:

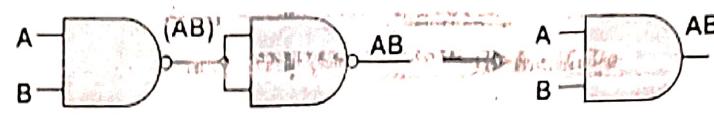
1. **NOT gate:** The input is given into short circuited pins of two inputs NAND gate and the output is inversion of input as shown in fig.
2. **AND gate:** Two NAND gates are required. Inputs given to one NAND gate produce an output which acts as input for second NAND gate and the final output is same as AND gate output.
3. **OR gate:** Three NAND gates are required. Two inputs are given to two different NAND gates the outputs of these are given as input to third NAND gate. Final output is same as of OR gate output.
4. **XOR gate:** Four NAND gates are required. The connections are made as per the given circuit diagram, the final output is same as XOR gate output.
5. **XNOR gate:** Five NAND gates are required. So we use two 7400 ICs. The final output of XOR gate (Four gates) is given as input to fifth NAND gate and the output is same as XNOR gate i.e. XNOR is inversion of XOR.



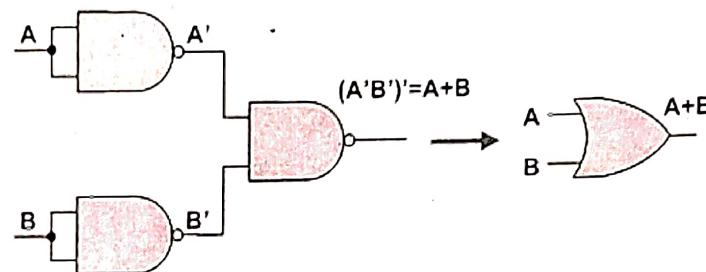
OR



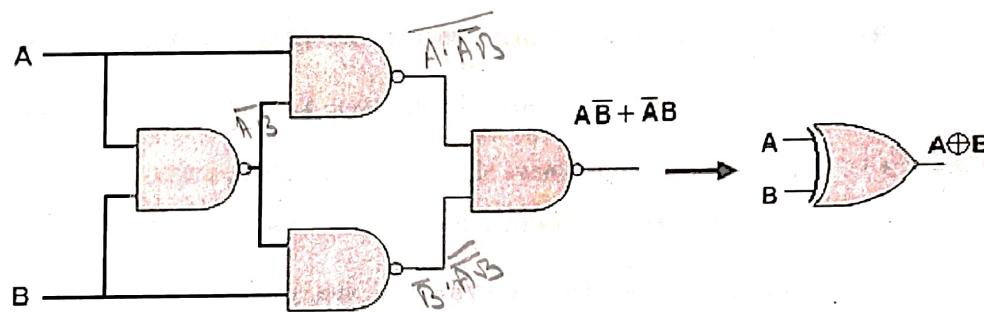
NOT GATE USING NAND GATE



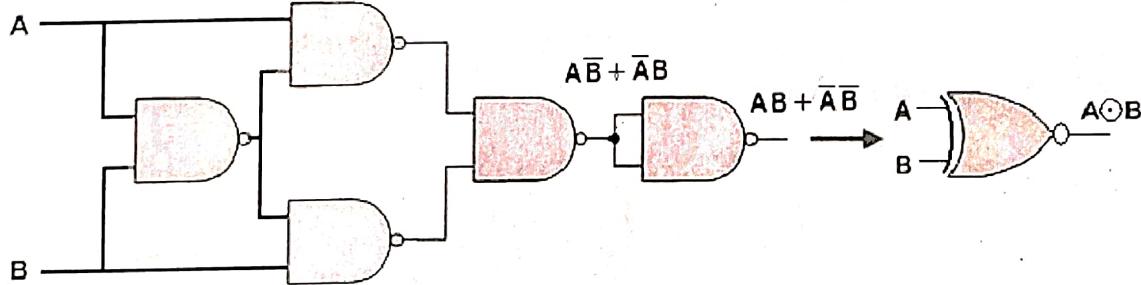
AND GATE USING NAND GATE



OR GATE USING NAND GATE



EX-OR GATE USING NAND GATE



EX-NOR GATE USING NAND GATE

PIN DESCRIPTION:

PROCEDURE:

1. Take a 14 pin NAND gate IC, a trainer kit which must be switched off and some wires.
2. Insert the IC into the 14 pin IC slot in the trainer kit.
3. Now make the connection one by one as given circuit diagrams and pin description.
4. Make ground connection and Vcc connection for voltage supply.
5. In the kit LEDs are attached with the input toggle switches and output. At low value (0) of switch LED do not glow or LED glow Green, while at high value (1) switch LED glow Red.
6. By changing inputs using toggle switches verify truth tables for all circuits.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 4

AIM: To implement all Logic gates using Universal gate IC-7402 (NOR Gate IC).

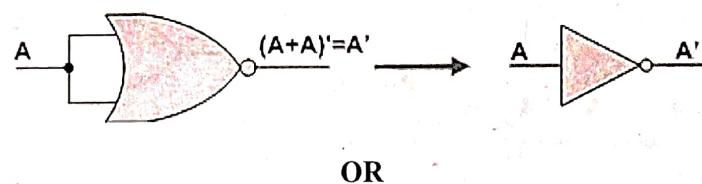
APPARATUS: Digital trainer kits, Logic gate IC's., Connecting wires.

THEORY:

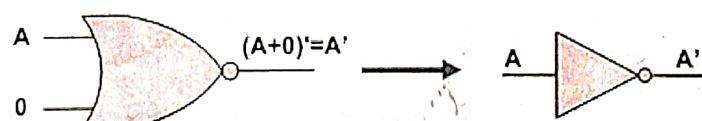
Since NOR gate is universal gate, all other logic gates can be implemented using it.

Implementation using NOR gate:

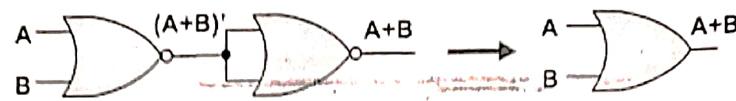
1. **NOT gate:** The input is given into short circuited pins of two inputs NOR gate and the output is inversion of input as shown in fig.
2. **AND gate:** Two NOR gates are required. Inputs given to one NOR gate produce an output which acts as input for second NOR gate and the final output is same as AND gate output.
3. **OR gate:** Three NOR gates are required. Two inputs are given to two different NOR gates the outputs of these are given as input to third NOR gate. Final output is same as of OR gate output.
4. **XOR gate:** Four NOR gates are required. The connections are made as per the given circuit diagram, the final output is same as XOR gate output.
5. **XNOR gate:** Five NOR gates are required. So we use two 7402 ICs. The final output of XOR gate (Four gates) is given as input to fifth NOR gate and the output is same as XNOR gate i.e. XNOR is inversion of XOR.



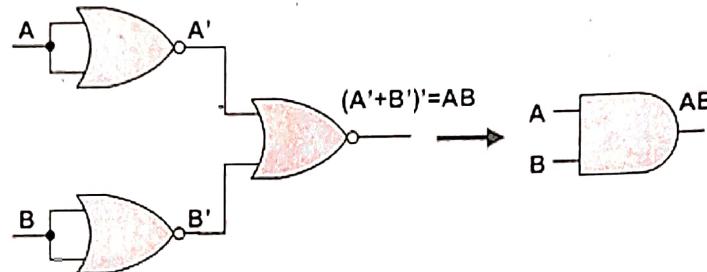
OR



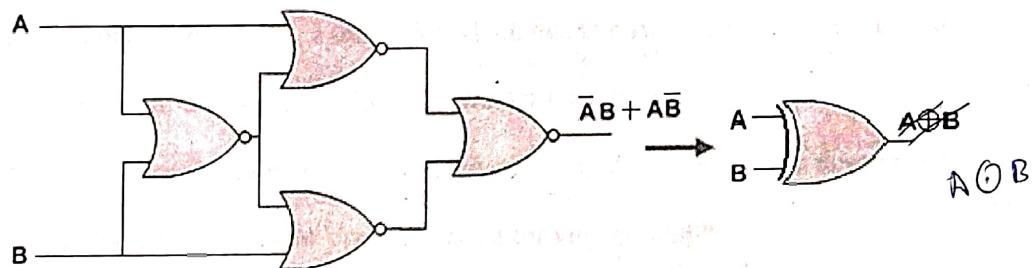
NOT GATE USING NOR GATE



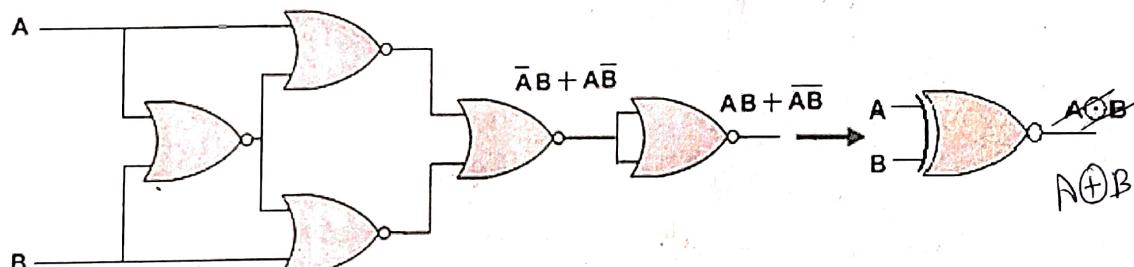
OR GATE USING NOR GATE



AND GATE USING NOR GATE



EX-NOR GATE USING NOR GATE



EX-NOR GATE USING NOR GATE

PIN DESCRIPTION:

PROCEDURE:

1. Take a 14 pin NOR gate IC, a trainer kit which must be switched off and some wires.
2. Insert the IC into the 14 pin IC slot in the trainer kit.
3. Now make the connection one by one as given circuit diagrams and pin description.
4. Make ground connection and Vcc connection for voltage supply.
5. In the kit LEDs are attached with the input toggle switches and output. At low value (0) of switch LED do not glow or LED glow Green, while at high value (1) switch LED glow Red.
6. By changing inputs using toggle switches verify truth tables for all circuits.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

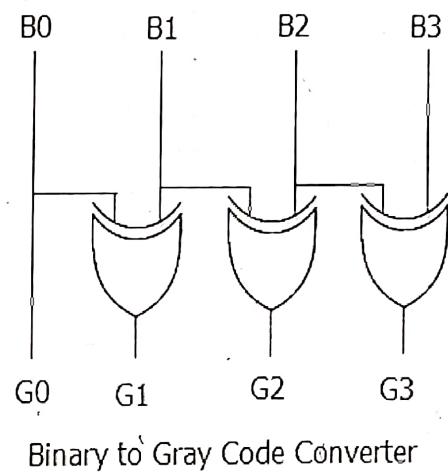
EXPERIMENT No. 5

AIM: To design Binary to Gray and Gray to Binary code converters using Logic gates.

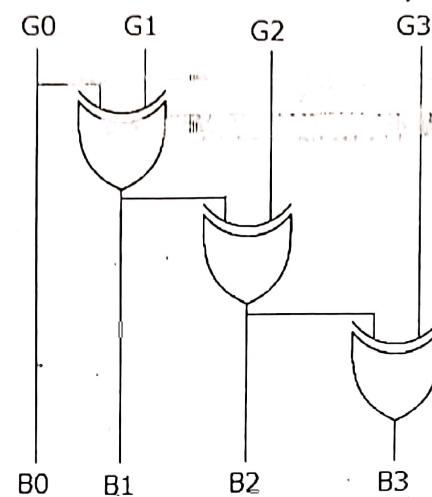
APPARATUS: Digital trainer kits, Logic gate IC 7486 (XOR Gate), Connecting wires.

THEORY:

Binary to Gray Code converter: Consider Binary code bits B₀, B₁, B₂, B₃ as inputs and Gray code bits G₀, G₁, G₂, and G₃ as outputs. For converting binary to gray code, the MSB is noted. This MSB is added to the bit in next position. The sums are recorded and carry if any generated is discarded. This procedure is repeated till last bit of binary number is reached. The Karnaugh maps will be used for Gray code outputs (G₀, G₁, G₂, and G₃) value calculation. So find minimal expressions for G₀, G₁, G₂, and G₃ and realize these using logic gates.



Gray to Binary Code converter: Consider Gray code bits G₀, G₁, G₂, and G₃ as inputs and Binary code bits B₀, B₁, B₂, and B₃ as outputs. For converting gray to binary code, the MSB is noted. This MSB is added to the bit in next position. The sums are recorded and carry if any generated is discarded. This sum is further added to the bit in next position and sums are recorded and carry if any generated is discarded. This procedure is repeated till last bit of gray code is reached. The Karnaugh maps will be used for Binary code outputs (B₀, B₁, B₂, and B₃) value calculation. So find minimal expressions for B₀, B₁, B₂, and B₃ and realize these using logic gates.



Gray to Binary Code Converter

| Sr No. | BINARY CODE | | | | | GRAY CODE | | | |
|--------|-------------|----|----|----|--|-----------|----|----|----|
| | B0 | B1 | B2 | B3 | | G0 | G1 | G2 | G3 |
| 1. | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 |
| 2. | 0 | 0 | 0 | 1 | | 0 | 0 | 0 | 1 |
| 3. | 0 | 0 | 1 | 0 | | 0 | 0 | 1 | 1 |
| 4. | 0 | 0 | 1 | 1 | | 0 | 0 | 1 | 0 |
| 5. | 0 | 1 | 0 | 0 | | 0 | 1 | 0 | 0 |
| 6. | 0 | 1 | 0 | 1 | | 0 | 1 | 0 | 1 |
| 7. | 0 | 1 | 1 | 0 | | 0 | 1 | 1 | 1 |
| 8. | 0 | 1 | 1 | 1 | | 0 | 1 | 1 | 0 |
| 9. | 1 | 0 | 0 | 0 | | 1 | 1 | 0 | 0 |
| 10. | 1 | 0 | 0 | 1 | | 1 | 1 | 0 | 1 |
| 11. | 1 | 0 | 1 | 0 | | 1 | 1 | 1 | 1 |
| 12. | 1 | 0 | 1 | 1 | | 1 | 1 | 1 | 0 |
| 13. | 1 | 1 | 0 | 0 | | 1 | 0 | 1 | 0 |
| 14. | 1 | 1 | 0 | 1 | | 1 | 0 | 1 | 1 |
| 15. | 1 | 1 | 1 | 0 | | 1 | 0 | 0 | 1 |
| 16. | 1 | 1 | 1 | 1 | | 1 | 0 | 0 | 0 |

PROCEDURE:

1. Take the IC's numbered 7486.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 6

AIM: To design Half Adder and Full Adder circuits using Logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's 7408, 7432, 7486., Connecting wires.

THEORY:

HALF ADDER: A half adder is a MSI circuit that adds two binary digits, giving a SUM bit and a CARRY bit as in the logic truth table. If A and B are the two input bits then SUM is the XOR of A & B:

$$\text{Sum} = A\bar{B} + \bar{A}B = A \oplus B$$

Similarly CARRY is the AND of A & B:

$$\text{Carry} = A \cdot B$$

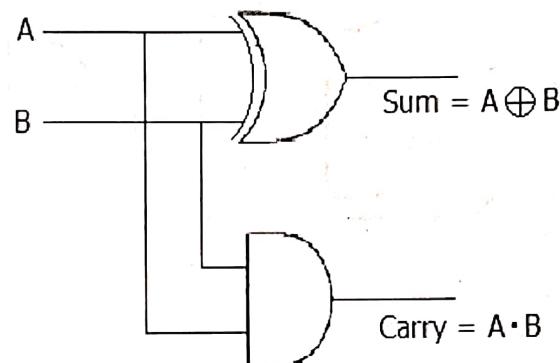


Fig: Half Adder

TRUTH TABLE (HALF ADDER)

| INPUT | | OUTPUT | |
|-------|---|--------|-------|
| A | B | SUM | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

FULL ADDER: Full adder is a MSI circuit that adds two input bits and carry from the previous stage and out a SUM bit and CARRY OUT bit. A and B are the main bits, Cin is the carry from the previous stage. SUM produced is:

$$\begin{aligned} \text{Sum} &= \bar{A} \bar{B} \text{Cin} + \bar{A} B \bar{\text{Cin}} + A \bar{B} \bar{\text{Cin}} \\ &= A \oplus B \oplus \text{Cin} \end{aligned}$$

Cout is the output carry bit and is:

$$\begin{aligned} \text{Cout} &= \bar{A} B \text{Cin} + A \bar{B} \text{Cin} + A B \bar{\text{Cin}} + A B \text{Cin} \\ &= A B + \text{Cin} (\bar{A} B + A \bar{B}) \\ &= A B + (A \oplus B) \text{Cin} \end{aligned}$$

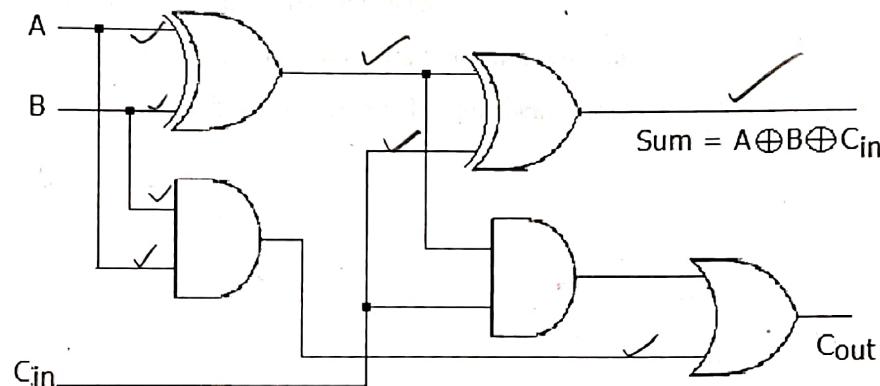


Fig: Full Adder

TRUTH TABLE (FULL ADDER)

| INPUT | | | OUTPUT | |
|-------|---|-----------------|--------|------------------|
| A | B | C _{in} | SUM | C _{out} |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

~~Objectives~~ to be studied

~~Block diagram produced~~

PROCEDURE:

5. Take the IC's numbered 7408, 7432, 7486.
6. Place them properly on their respective places.
7. Make the connections as per the circuit diagram.
8. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

4. Circuit should be properly connected.
5. Do not short circuit in the trainer kit during operation.
6. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 7

AIM: To design Half Subtractor and Full Subtractor circuits using Logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's 7404, 7408, 7432, 7486, Connecting wires.

THEORY:

HALF SUBTRACTOR: A half subtractor circuit subtracts two binary digits using XOR, NOT and AND gates giving output of difference bit and borrow bit.

$$D = X \bar{Y} + \bar{X} Y = X \oplus Y$$

$$B = \bar{X} Y$$

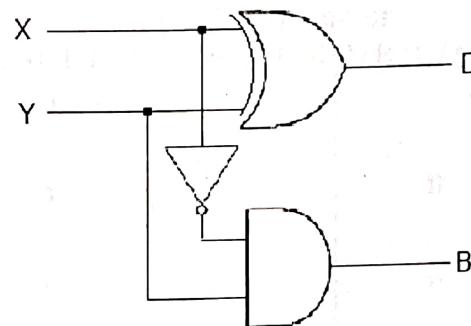


Fig: Half Subtractor

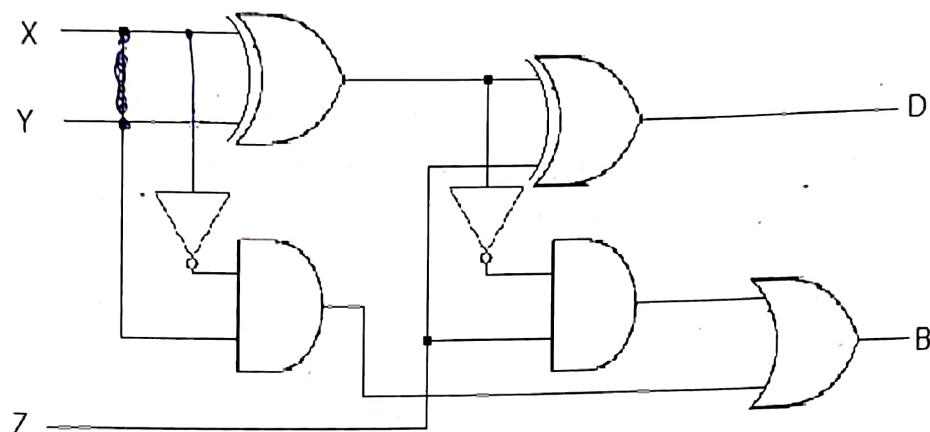
TRUTH TABLE (HALF SUBTRACTOR)

| INPUTS | | OUTPUTS | |
|--------|---|---------|---|
| X | Y | D | B |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

FULL SUBTRACTOR: A full subtractor is an arithmetic circuit that subtracts two bits and a borrow and difference bit is generated as output.

$$D = \overline{X} \overline{Y} Z + \overline{X} Y Z + X \overline{Y} \overline{Z} + X Y Z$$

$$B = \overline{X} Y + \overline{X} Z + Y Z$$



**Fig: Full Subtractor
TRUTH TABLE (FULL SUBTRACTOR)**

| INPUTS | | | OUTPUTS | |
|--------|---|---|---------|---|
| X | Y | Z | D | B |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

PROCEDURE:

1. Take the IC's numbered 7404, 7408, 7432, 7486.
2. Place them properly on their respective places.

3. Make the connections as per the circuit diagram.

4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 8

AIM: Multiplexer and Demultiplexer: Truth-table verification and realization using logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's. 7404, 7408, 7432, Connecting wires.

THEORY: MULTIPLEXER: The multiplexer is a digital circuit which has many input lines and one output line. The function of the multiplexer is to select one of the input lines and connect it to the output.

Four Input Multiplexer: A four input multiplexer is shown in figure. There are four inputs I_0, I_1, I_2 and I_3 which are selectively transmitted to output Y depending on select input combinations. Here two select inputs are required as $2^N = 4$ where N is number of select inputs i.e. $N = 2$. Each data input is routed to output Y depending upon select input combination. When $S_1 S_0 = 0, 0$ the input reaches output Y . The logic diagram for 4:1 multiplexer is given in figure.

The Boolean expression for output is:

$$Y = \overline{S_1} \overline{S_2} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

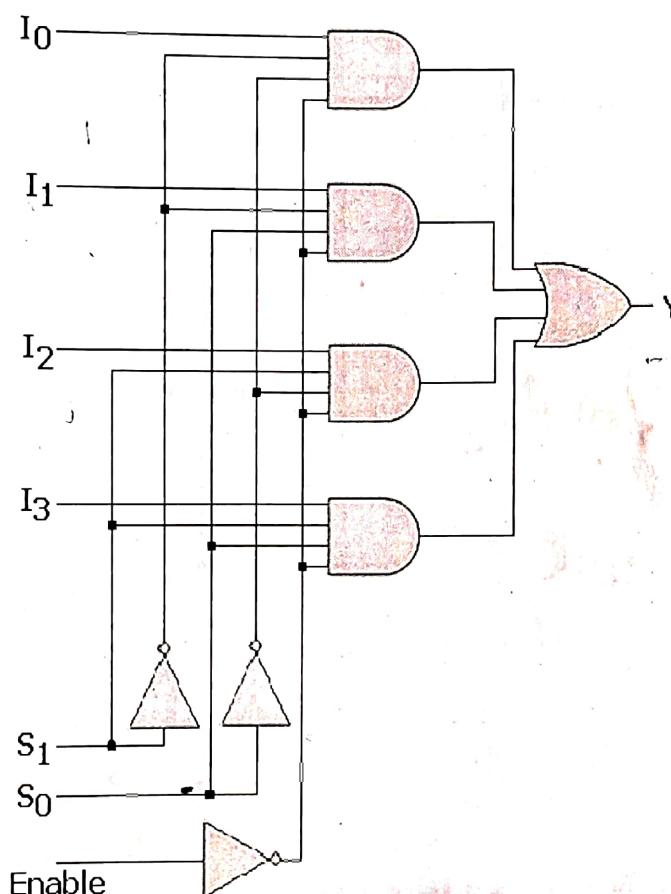


Fig: 4:1 MULTIPLEXER

TRUTH TABLE FOR 4:1 MULTIPLEXER

| Enable | Select Inputs | | Output Selected |
|--------|---------------|-------|-----------------|
| | S_0 | S_1 | |
| 0 | 0 | 0 | I_0 |

| | | | |
|---|---|---|-------|
| 0 | 0 | 1 | I_1 |
| 0 | 1 | 0 | I_2 |
| 0 | 1 | 1 | I_3 |

DEMUTIPLEXER: The demultiplexer is a digital circuit which has one input and many output lines. In other words the demultiplexer takes one input data source and selectively distributes it to 1 of N output channels. The number of select lines is S where $N = 2^S$.

1:4 Demultiplexer: Figure shows logic diagram for a demultiplexer that distributes one line (input) to four output lines. The single data input lines are connected to all AND gates. But only one of these lines will be enabled by select lines S_0, S_1 , e.g. $S_0S_1=0\ 0$, the D_0 will be available.

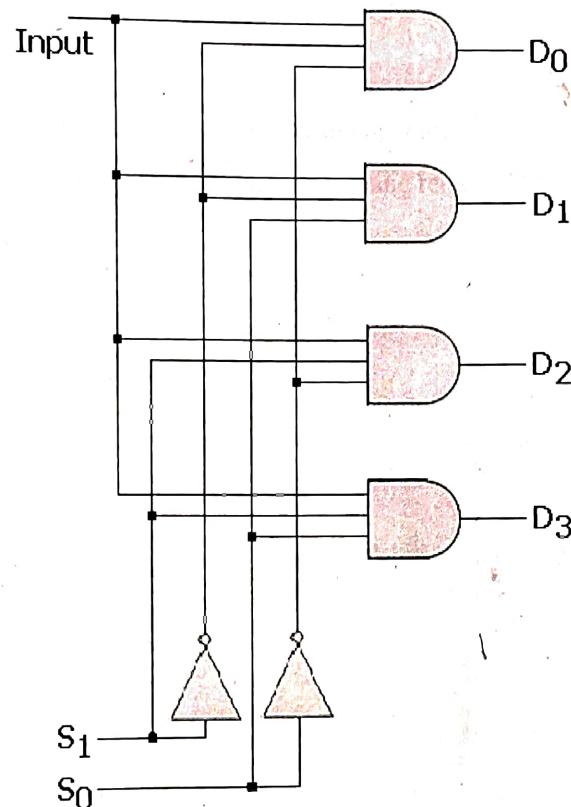


Fig: 1:4 DEMULTIPLEXER

TRUTH TABLE FOR 1:4 DEMULTIPLEXER

| Select Inputs | | Outputs | | | |
|---------------|-------|---------|-------|-------|-------|
| S_1 | S_0 | D_3 | D_2 | D_1 | D_0 |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |

| | | | | | |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

PROCEDURE:

1. Take the IC's numbered 7404, 7408, 7432.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

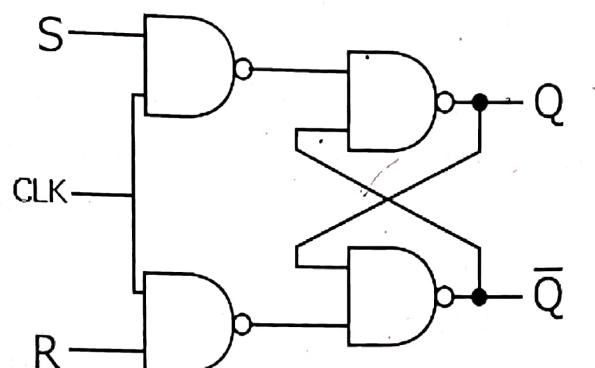
EXPERIMENT No. 9

AIM: Flip Flops: Truth-table verification and realization of SR, JK, T-type and D-type Flip-Flop using logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's. 7400, 7402, 7404, 7408, Connecting wires.

THEORY (FLIP-FLOP's):

1. **S-R Flip flop:** It is required to set or reset the memory cell in synchronism with a train of pulses known as clock. Such circuit is referred to as a clocked set reset (S-R) FLIP FLOP. Also the circuit responds to the input signal only if the clock is present.



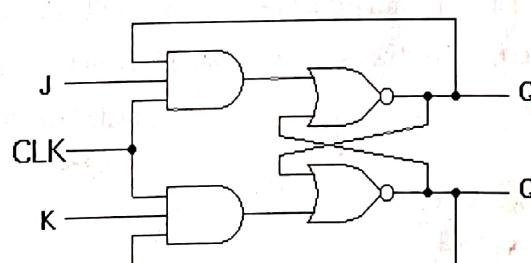
SR-FLIP FLOP

TRUTH TABLE OF THE FLIP-FLOP

| S | R | CLK | Outputs Q_{n+1} |
|---|---|-----|----------------------|
| 0 | 0 | ↑ | Q_n (No Change) |
| 0 | 1 | ↑ | 0 |
| 1 | 0 | ↑ | 1 |
| 1 | 1 | ↑ | Ambiguous |

If $S_n = R_n = 0$ and CK is applied, the o/p at the end of the clock pulse is same as o/p before the clock pulse i.e. $Q_{n+1} = Q_n$.

2. **J-K flip flop:** The uncertainty in the state of an S-R flip flop when $S_n = R_n = 1$ can be eliminated by converting it into a J-K flip flop. The data inputs are J and K which are ANDed with Q and \bar{Q} to obtain S and R.



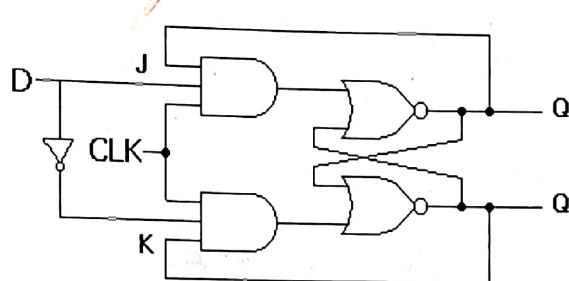
J-K FLIP FLOP

TRUTH TABLE OF THE FLIP-FLOP

| | | | OUTPUT |
|--|--|--|--------|
| | | | |

| J | K | CLK | Q_{n+1} |
|---|---|-----|-------------------|
| 0 | 0 | CLK | Q_n (No Change) |
| 0 | 1 | | 0 |
| 1 | 0 | | 1 |
| 1 | 1 | | Q_n (Toggles) |

3. **D-Type flip flop:** The ckt diagram of D type flip flop shows that it has only one i/p reference to as D-input or data input. It is truth table shows that the output Q_{n+1} at the end of the clock pulse equal the input D_n before the clock pulse.

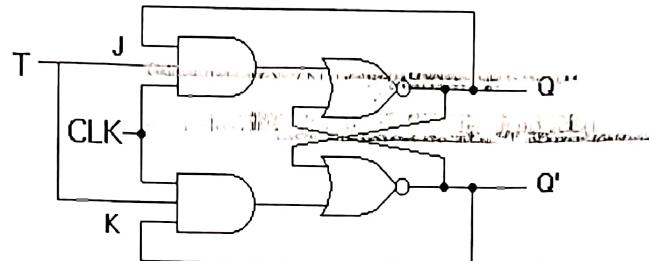


D-FLIP FLOP

TRUTH TABLE OF THE FLIP-FLOP

| D | CLK | Output Q_{n+1} |
|---|-----|------------------|
| 1 | ↑ | 1 |
| 0 | ↑ | 0 |

4. **T-Type flip flop:** In a J-K flip-flop, if $J = K$, the resulting flip flop is referred to as a T-type flip flop. It has only one input, referred to as T-input. A truth table shows that if T=1 it acts as a toggle switch. For every clock pulse, the output Q changes.



T- FLIP FLOP

TRUTH TABLE OF THE FLIP-FLOP

| T | CLK | Output Q_{n+1} |
|---|-----|---------------------|
| 1 | ↑ | Q_n |
| 0 | ↑ | $\overline{Q_n}$ |

PROCEDURE:

1. Take the IC's numbered 7404, 7408, 7432, 7486.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

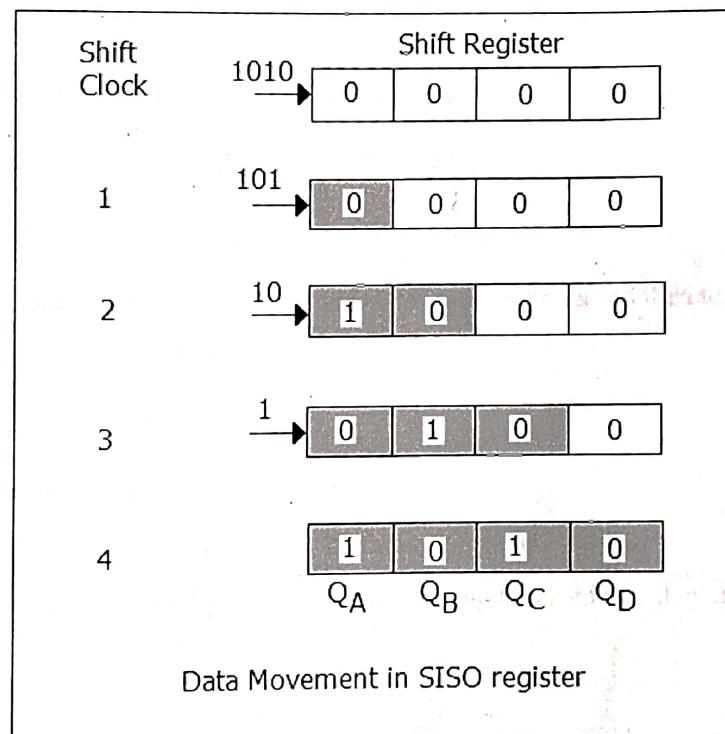
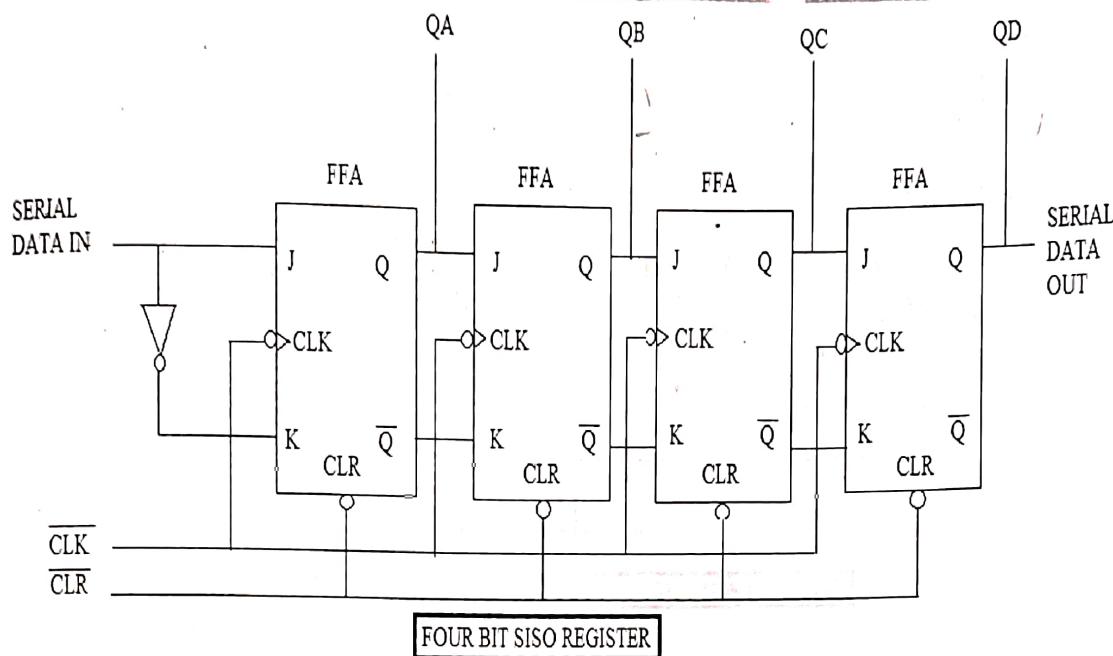
1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 10

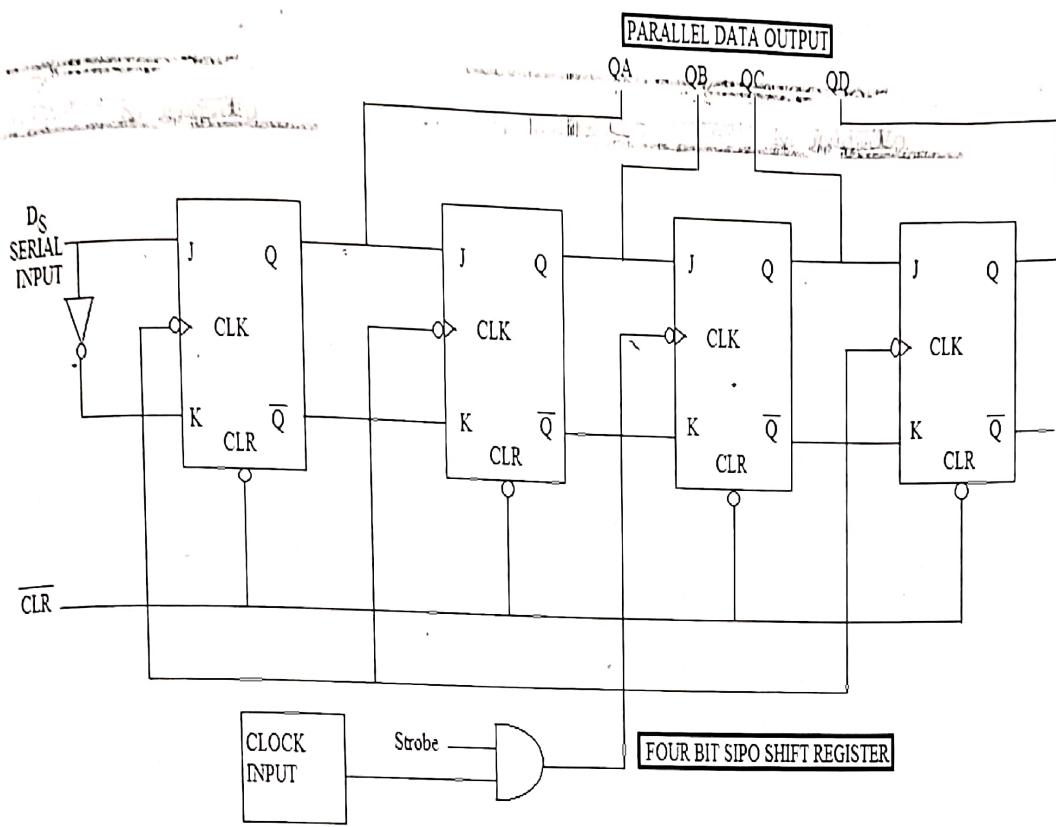
AIM: To design & verify operation of SISO and SIPO Shift Registers using JK flip flop and logic gates.

APPARATUS: Digital trainer kits, Logic gate & F/F IC's., Connecting wires.

Four Bit SISO Register:



Four Bit SIPO shift register:



PROCEDURE:

1. Take the IC's mentioned in apparatus required.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

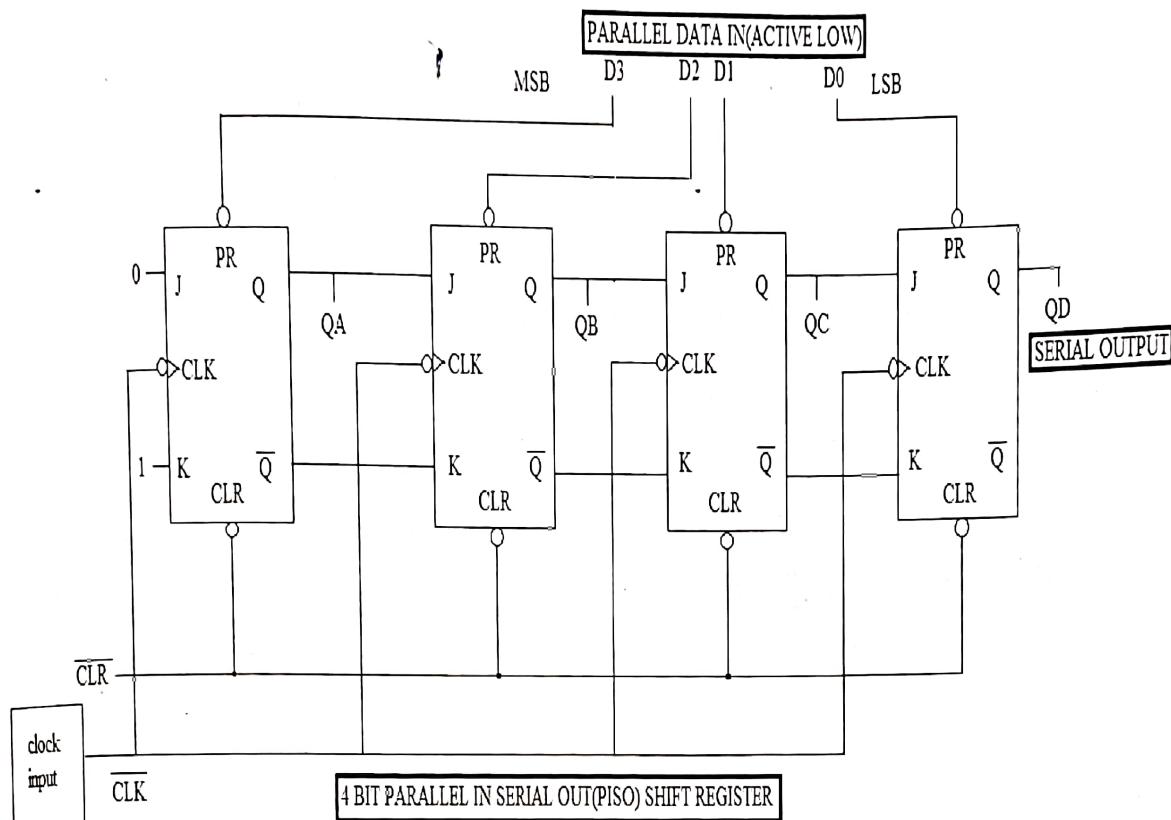
1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 11

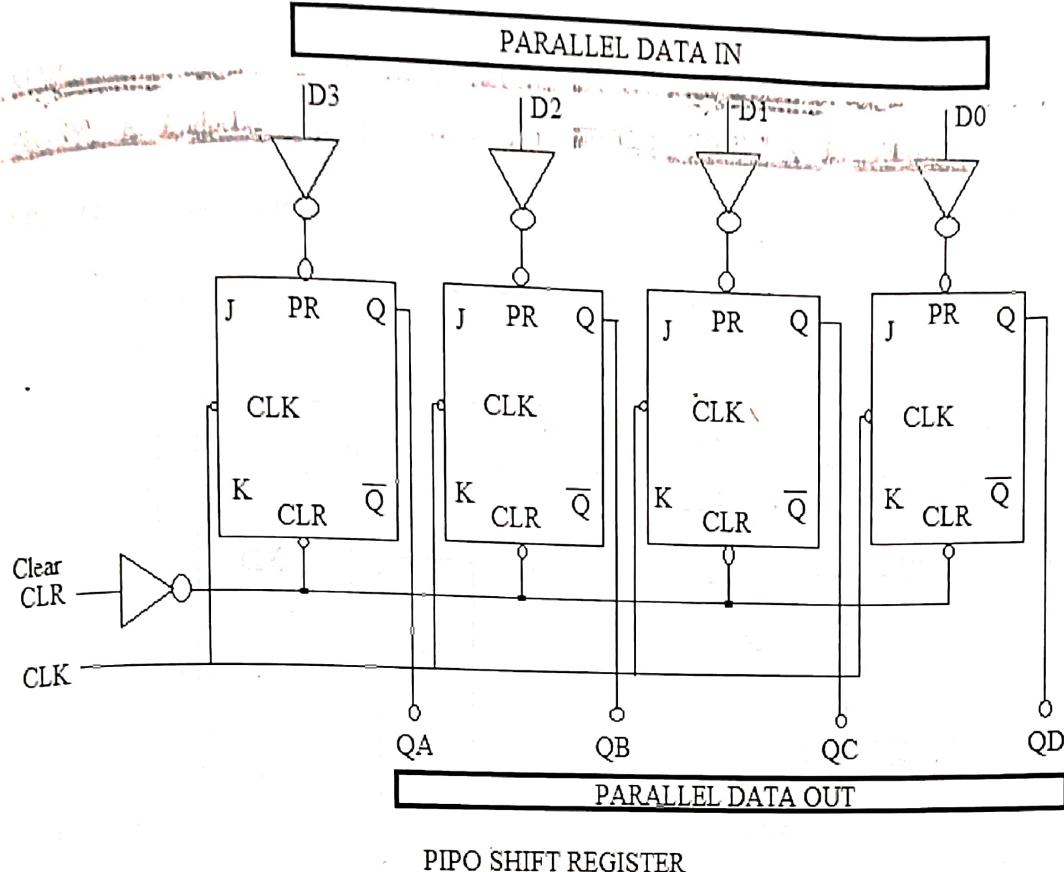
AIM: To design & verify operation of PISO and PIPO Shift Registers using JK flip flop and logic gates.

APPARATUS: Digital trainer kits, Logic gate & F/F IC's., Connecting wires.

4 Bit Parallel in Serial out (PISO) shift register:



PIPO shift register:



PROCEDURE:

1. Take the IC's mentioned in apparatus required.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

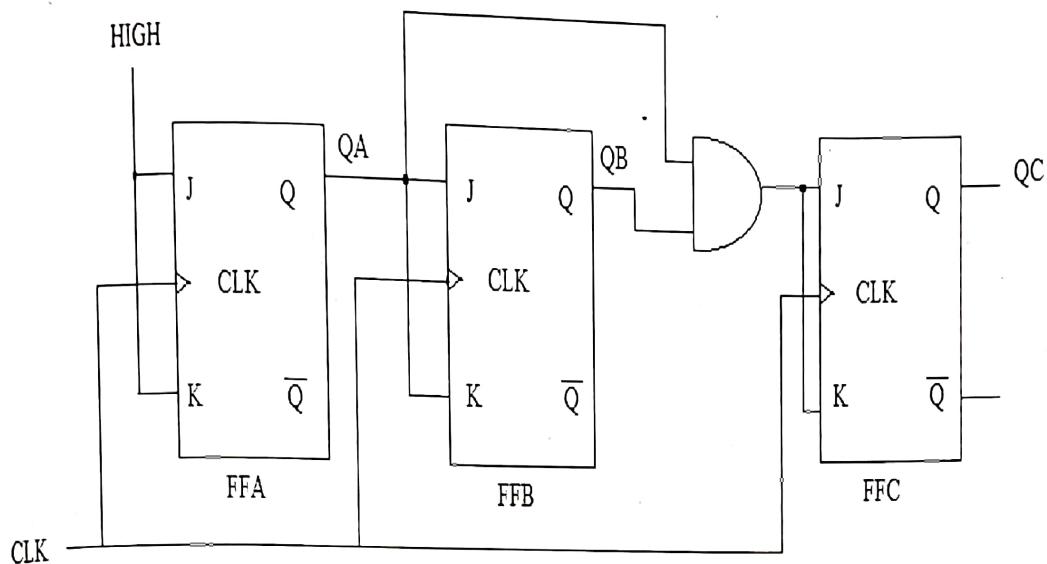
1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 12

AIM: To design & verify operation of 3-bit Synchronous binary counter using J-K flip flop.

APPARATUS: Digital trainer kits, Logic gate & F/F IC's., Connecting wires.

3 Bit Synchronous Counter:



THREE BIT SYNCRONOUS COUNTER

Table: Sequence of States for 3 Bit Synchronous Binary Counter

| Clock Pulse | Q_c | Q_b | Q_a |
|-------------|-------|-------|-------|
| 1. | 0 | 0 | 0 |
| 2. | 0 | 0 | 1 |
| 3. | 0 | 1 | 0 |
| 4. | 0 | 1 | 1 |
| 5. | 1 | 0 | 0 |
| 6. | 1 | 0 | 1 |
| 7. | 1 | 1 | 0 |
| 8. | 1 | 1 | 1 |
| 9. | 0 | 0 | 0 |

PROCEDURE:

1. Take the IC's mentioned in apparatus required.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 13

AIM: To design & verify operation of Synchronous BCD Decade counter using J-K flip flop.

APPARATUS: Digital trainer kits, Logic gate & FF IC's., Connecting wires.

Synchronous BCD Decade counter:

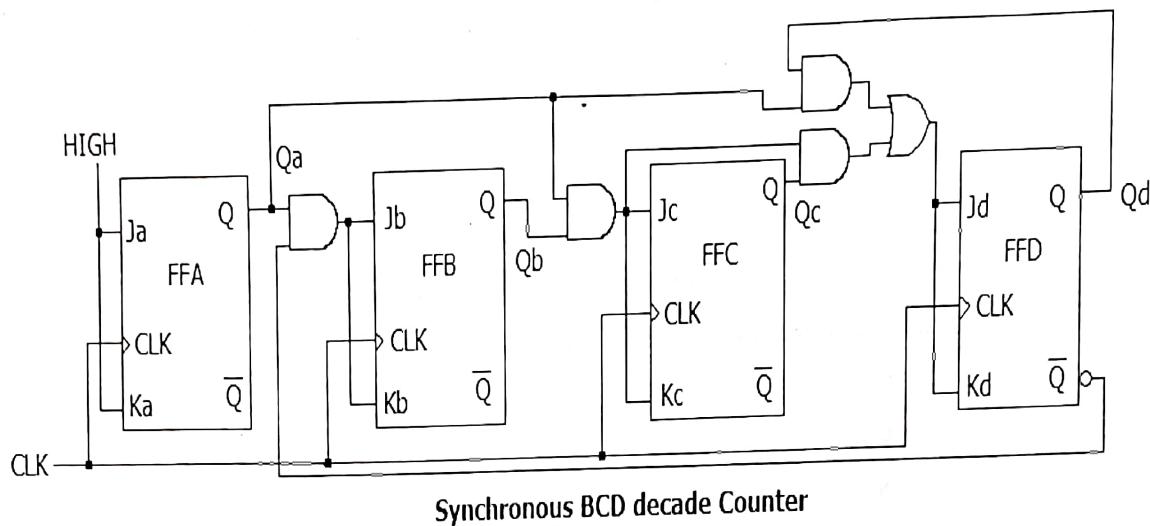


Table: Sequence of States for BCD Counter

| Clock Pulse | Q_d | Q_c | Q_b | Q_a |
|-------------|-------|-------|-------|-------|
| 1. | 0 | 0 | 0 | 0 |
| 2. | 0 | 0 | 0 | 1 |
| 3. | 0 | 0 | 1 | 0 |
| 4. | 0 | 0 | 1 | 1 |
| 5. | 0 | 1 | 0 | 0 |
| 6. | 0 | 1 | 0 | 1 |
| 7. | 0 | 1 | 1 | 0 |
| 8. | 0 | 1 | 1 | 1 |
| 9. | 1 | 0 | 0 | 0 |
| 10. | 1 | 0 | 0 | 1 |

PROCEDURE:

1. Take the IC's mentioned in apparatus required.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT No. 14

AIM: To Design BCD to Seven Segment Display circuit using IC 7447.

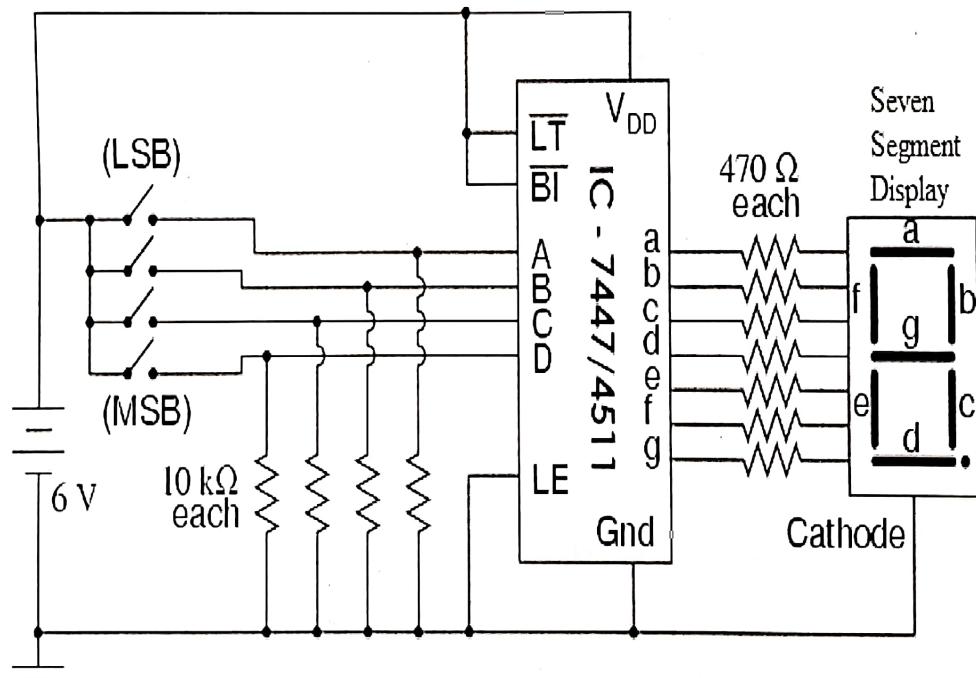
APPARATUS: Logic Trainer kit, IC 7447/4511, 7 segment display (Common cathode), Connecting leads.

THEORY:-

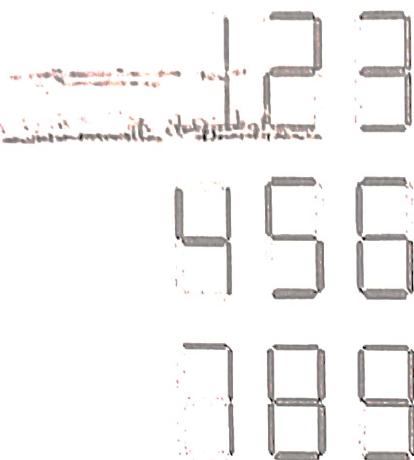
A BCD to 7-segment decoder/driver is used as a 4-bit BCD input and provide the outputs that will pass current through the appropriate segment to display the decimal digit.

For display numerical digit, a 7-segment configuration is used to form the decimal character 0 to 9 and sometimes the hex character A through F. One common arrangement uses light emitting diode (LED'S) for each segment, by controlling the current through each LED. Some segment will pass light through and other will dark so that the desired character pattern will be generated.

CIRCUIT DIAGRAM:

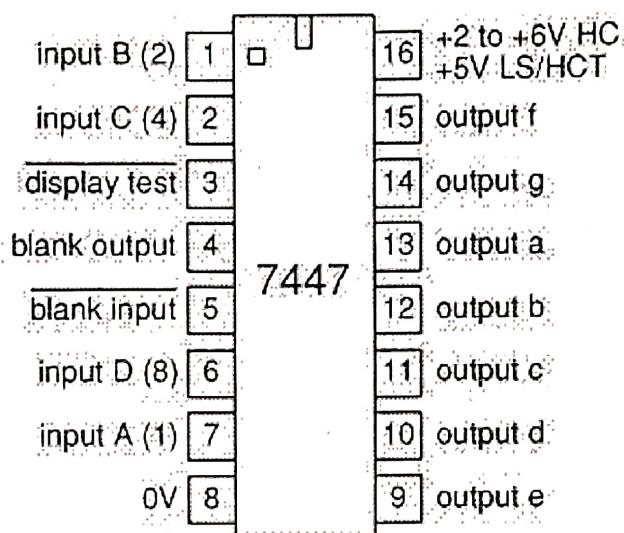


TRUTH TABLE:



| Digit Shown | 0.100 | Illuminated Segment (1 = illumination) | | | | | | |
|----------------|-------|--|---|---|---|---|---|---|
| | | a | b | c | d | e | f | g |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 3 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 6 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

PIN DESCRIPTION:



PROCEDURE:

- 1) Make the connection as shown in the figure.
- 2) Switch on the power supply,
- 3) Verify the Truth Table for BCD to seven segment display
- 4) If the LED glow, output is at logic "1" otherwise at logic "0".

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.