Total No. of Pages: 4

~~SECOND~~ SEMESTER — IV

Roll No. .....

B. Tech. [CO/IT/SE]

END SEMESTER EXAMINATION May-2018

EC262 DIGITAL ELECTRONICS

Time: 3:00 Hours *Max. Marks: 40*

Note: Answer any *FIVE* questions. Question no. 1 is compulsory. Assume suitable missing data, if any.

1 [a] Most calculators use a BCD to store the decimal values as they are entered into the keyboard and to drive the digit displays.

(i) If a calculator is designed to handle 8-digit decimal numbers, how many bits does this require?

(ii) What bits are stored when the number 375 is entered into the calculator?

[b] A combinational logic circuit has four inputs (A, B, C, D) and has one output *z*. The output is 1 if the input has three consecutive 0's or three consecutive 1's. Design combination circuit using one 4-input OR gate and four 3-input AND gates.

[c] Design positive edge triggered T flip-flop using positive edge triggered D flip-flop.

[d] Illustrate important timing parameters of flip-flop using suitable diagram.

[e] What are the important specification of digital-to-analog convertor?

[f] Simplify following Boolean expression to minimum number of literals using appropriate postulates and theorems.

$$x'y(w'+z'w)+y(x+x'zw)$$

[2x6=12]

2[a] $B_3B_2B_1B_0$ represents a binary number with B_0 as LSB. Design a logic circuit that gives HIGH output whenever the binary number is greater than 0010 and less than 1000. [3]

[b] Fig. 1 shows diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

(i) The headlights are on while the ignition is off.

(ii) The door is open while the ignition is on. [4]

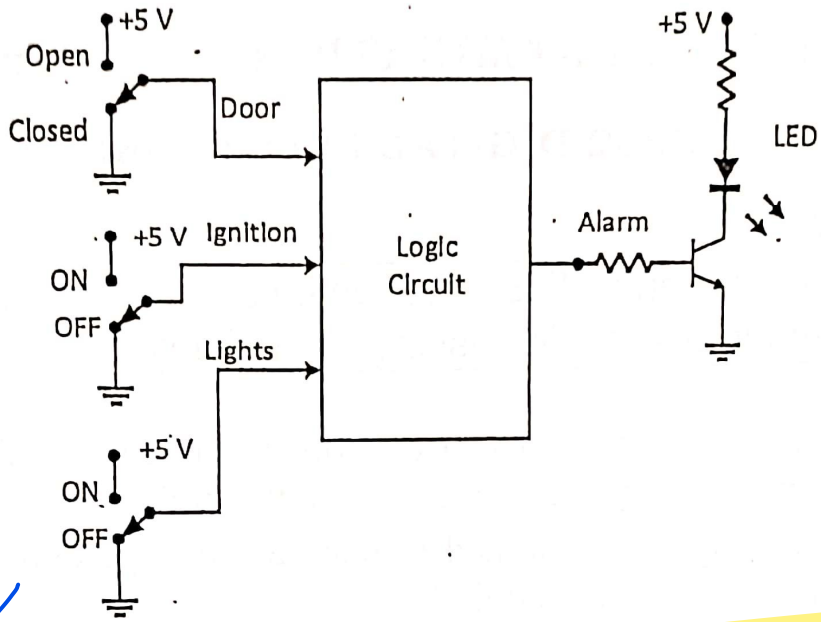

Fig. 1

3[a] Design NOR gate using CMOS logic. Also, state the advantages of CMOS. [3]

[b] Fig. 2 shows the intersection of a main highway with a secondary access road. Vehicle-detection sensors are placed along lanes C and D (main road) and lanes A and B (access road). These sensor outputs are LOW (0) when no vehicle is preset and HIGH (1) when a vehicle is present. The intersection traffic light is to be controlled according to the following logic.

(i) The east-west (E-W) traffic light will be green whenever both lanes C and D are occupied.

(ii) The E-W light will be green whenever either lanes C or D is occupied but lanes A and B are not both occupied.

(iii) The north-south (N-S) light will be green whenever both lanes A and B are occupied but lanes C and D are not both occupied.

(iv) The N-S light will also be green when either A or B is occupied while lanes C and D are both vacant.

(v) The E-W light will be green when no vehicles are present.

Using the sensor outputs, A, B, C, D as inputs, design a logic circuit to control the traffic light. There should be two outputs, N-S and E-W, that go HIGH when the corresponding light is to be green. Simplify the circuit as much as possible and show all steps. [4]

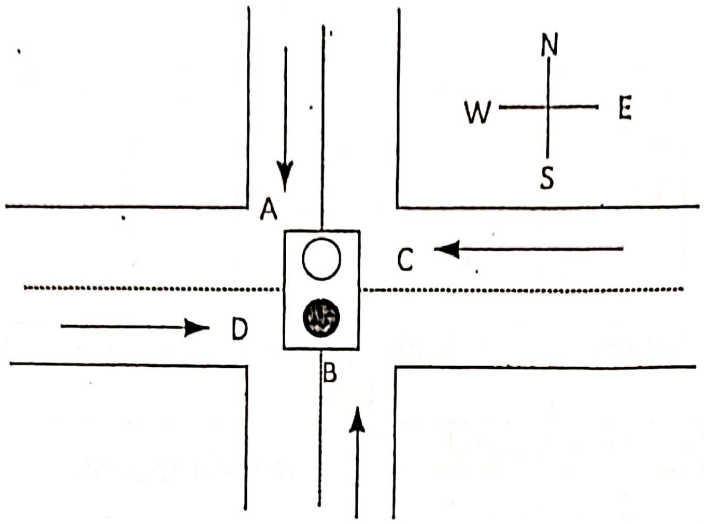

Fig. 2

4[a] Implement the following function using single 4x1 MUX and gates. [3]

$$F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$$

[b] Consider the combinational circuit below. The value of inputs at different time instants is given below. Find the corresponding values of the output F. [4]

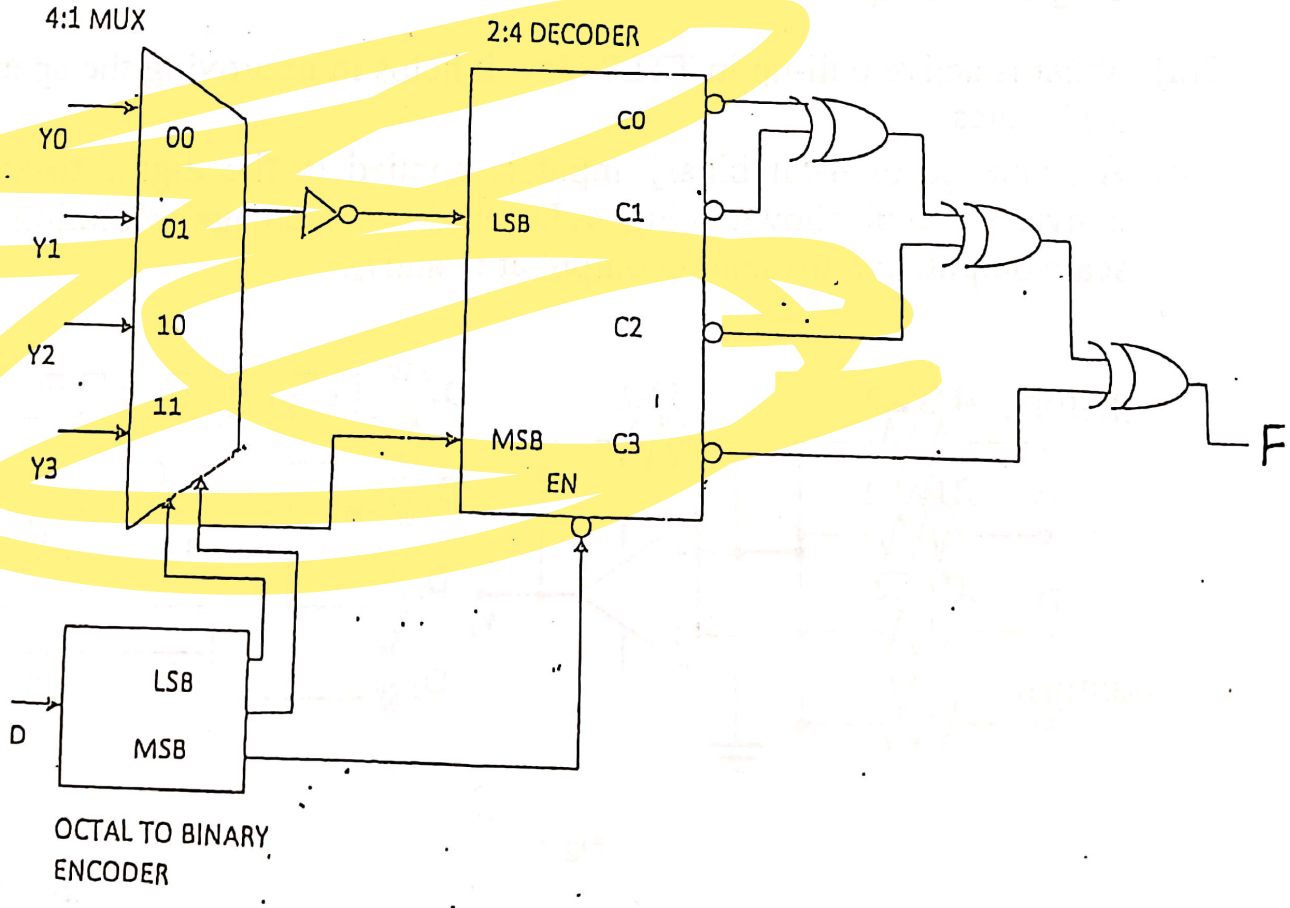

Fig. 3

Table-I

Time →	1	2	3	4	5
Y0	0	1	1	0	1
Y1	1	1	1	1	0
Y2	0	1	1	0	1
Y3	0	1	0	0	0
D	3	5	7	2	1
F	?	?	?	?	?

5[a] Design a 4-bit register, which operates according to following Table. [3]

Table-II

Mode Control		Register Operation
S_1	S_2	
0	0	Parallel load
0	1	Shift right
1	0	Shift left
1	1	No change

[b] Design a sequential circuit that detect a sequence 101. Use D flip-flop for your design. [4]

6[a] Design a 3-bit asynchronous ripple counter using JK flip-flop. [3]

[b] Design a counter for counting of 8 states. The states are represented using 3-bits. Moreover, while going from one state to next state only single bit changes. [4]

7[a] What is active pull-up in TTL? How it helps in improving the speed of TTL gates. [3]

[b] A sequence of 4-bit binary input is applied to the digital-to-analog converter circuit shown in Fig. 4. Determine percentage resolution, full-scale output, and the analog output at t_1, and t_2. [4]

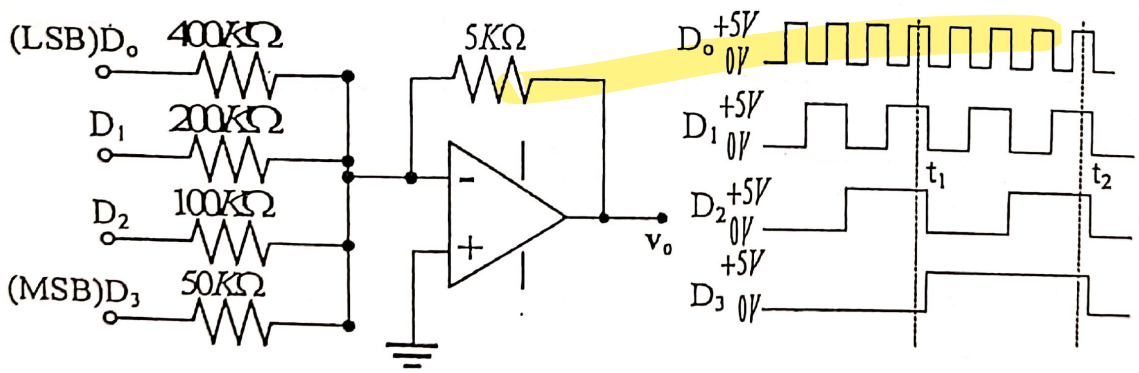

Fig. 4

---END---