Technical affairs- IIITDM Kancheepuram

System coding club

Day - 05

Digital Design Challenge

Date : 05/07/2025

Duration : 24 Hours

Challenge Brief

This challenge is an encryption - decryption challenge designed to test your wits to the maximum.

You're given a set of input-output pairs produced by an unknown encryption process, but the internals are entirely up to you. Using only Verilog, Verilator, and GTKWave, your task is to reverse-engineer the pattern, implement your own version of the encryption and decryption logic, and prove that your outputs match. There's no locked UP, no hidden module — everything in this challenge is open, inspectable, and hands-on. The only thing missing is the logic itself… and that's exactly what you have to create.

You are to construct three stages of encryption layers and similarly three stages of decryption based upon the expected input/output pair of each stage and the hints. Your

circuits designed must be according to the guidelines we provide or else it will be disregarded and not be considered for testbench evaluation by SCC.

Every one of you can test your circuits natively using test input/output pairs for your own checking and references.Once you are convinced that your circuit passes all of them sufficiently they are good enough.

Objectives

There are a set of objectives you are to achieve within your own circuits

- First and foremost , your circuit is required to pass all the public test cases we provide you.
- Your circuit will not just be combinational it will be a mix of combinational and sequential circuits the guidelines of architecture of your circuit is to be followed according to the github repository's README.md file (link to github - https://github.com/SCC-IIITDM/Encryption-Decryption-25)
- You are to make your clock speeds as fast as possible , if your clock speeds are too high it will cause the circuit to behave badly and fail , if it's too low it isn't using its full potential so choose wisely. Your first priority is to make a working circuit, the next is making it faster.

General Guidelines

- Your are supposed to have Linux i.e Ubuntu 22.04 or lesser for the installation of verilator and GTKWave , if you don't already have it please take a look a tutorial to download WSL or VirtualBox on windows as it is convenient and sufficient enough for this hackathon's timeline

- Installing the softwares are fairly straightforward , and I have detailed how to use them in the same github repository.(https://github.com/SCC-IIITDM/Encryption-Decryption-25)
- Incase of using a VirtualBox minimum allocate 20 Gb of storage and 6 or 4 Gb of RAM for smooth functioning.

Deliverables

- You are supposed to upload your verilog files and your .vcd dump from Verilator for GTKWave into a github repository, make it public and share it with us so that we can evaluate your work.

Evaluation Criteria

The Evaluation criteria is pretty straightforward it will be based on two factors:

- The correctness of your circuit is paramount.
- The clock speed of your circuit differentiates you from the others.

Addition resources or dataset if required

- WSL Ubuntu installation video How to Install Ubuntu on Windows 11 (WSL)
- VirtualBox Ubuntu Installation video :
  How to Install Ubuntu 24.04 LTS on VirtualBox in Windows 11

Note: These are videos for 24.04 Ubuntu LTS but just download 22.04 ISO image and it will still work.

Support

For any queries, reach out to:

Email: System Coding Club

Name & contact: Tarun Vignesh G (Verilog core) +91 77089 70183

WhatsApp Community: https://chat.whatsapp.com/CEjhrp1QolYLs1m4OgslMT

Submission

Please Submit here - https://forms.gle/uV7ZXBaHxTNSGAU17

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